# Low Noise Operation in Deep Depletion Mode MOS Transistors

Colin Carruthers BSc

PhD

University of Edinburgh

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# Abstract

This thesis considers the noise performance of a new design for $n$-channel *deep depletion mode* metal-oxide-semiconductor (MOS) transistors. The deep depletion mode transistor differs from conventional MOS transistors in that the conducting channel forms in a deep $n$-type well within the $p$-type substrate. The low levels of impurity concentration in the $n$-well for this novel transistor allow the distribution of the charge forming the conducting channel to be controlled by setting the gate voltage and substrate bias. It is shown that by careful choice of operating point the low frequency noise can be reduced to an order of magnitude below that normally observed in conventional MOS transistors.

Numerical simulation is used to show that this low noise operation is achieved by biasing the transistors so that the channel is made to form in the bulk away from the silicon-silicon dioxide interface.

An anomalous oscillation observed in deep depletion mode MOS transistors at temperatures lower than ambient is described. This oscillation made complete characterisation of the noise in the deep depletion transistor at low temperatures difficult, and the anomalous effect may preclude the use of such devices at low temperature.

It is shown that there are problems incorporating the deep depletion transistor in conventional buffer amplifier circuits because of the high conductance of the device. An innovative design for a cascode amplifier in-

corporating a deep depletion MOS transistors is proposed. The resulting buffer amplifier offers medium gain and excellent noise performance. Such an amplifier might be used in conjunction with advanced infra-red detection systems.

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[†]Now with IBM UK Labs.

# Contents

**Declaration** 1

**Abstract** 2

**Acknowledgements** 4

**Definition** 9

**1 Introduction** 10

1.1 The Deep Depletion mode MOS transistor . . . . . . . . . . 13

1.2 Thesis Plan and Structure . . . . . . . . . . . . . . . . . . . 15

**2 Device Fabrication and Physics** 18

2.1 Process Details . . . . . . . . . . . . . . . . . . . . . . . . 18

2.1.1 ICECREM . . . . . . . . . . . . . . . . . . . . . . . 19

2.1.2 Fabrication of Deep Depletion MOS Transistors . . . 19

2.2 Operation of Deep Depletion MOS Transistor . . . . . . . . 25

2.3 Noise Mechanisms . . . . . . . . . . . . . . . . . . . . . . . 31

2.3.1 Thermal Noise . . . . . . . . . . . . . . . . . . . . . 31

2.3.2 Shot Noise . . . . . . . . . . . . . . . . . . . . . . . 32

2.3.3 Flicker Noise . . . . . . . . . . . . . . . . . . . . . . 33

2.4 Summary . . . . . . . . . . . . . . . . . . . . . . . . . . . 39

3 **Impurity Freezeout** 40

3.1 Introduction . . . . . 41

3.2 Experimental Results . . . . . 44

3.3 Formulation of Poisson's Equation . . . . . 46

3.4 Temperature Dependence of terms in Poisson's Equation . . 47

3.4.1 Electron and Hole Concentrations . . . . . 47

3.4.2 Ionised Impurity Concentrations . . . . . 48

3.5 Numerical Formulation of Poisson's Equation . . . . . 50

3.6 Depletion Mode MOS Transistor . . . . . 52

3.7 Deep Depletion MOS Transistor . . . . . 56

3.8 Concluding Remarks . . . . . 66

4 **Experimental Technique** 67

4.1 Principles of Noise Measurement . . . . . 67

4.2 System Overview . . . . . 72

4.3 Bias Supply - Design Considerations . . . . . 75

4.4 Characteristics of Amplifier . . . . . 77

4.5 Spectrum Analyser and Filters . . . . . 79

4.6 Measurement of d.c. Characteristics . . . . . 84

4.7 Conclusions . . . . . 85

5 **Experimental Results** 86

5.1 Introduction . . . . . 86

5.2 Low Frequency Noise in Deep Depletion Mode MOS Transistors 87

5.2.1 Noise Results . . . . . 87

5.2.2 Simulation of carrier distribution . . . . . 101

5.2.3 Conclusions . . . . . 102

5.3 Conclusions . . . . . . . . . . . . . . . . . . . . . . . . . . 105

6 **Anomalous Oscillation in Depletion Mode MOS Transistors at Low Temperature** **106**

6.1 Results . . . . . . . . . . . . . . . . . . . . . . . . . . . . 106

6.2 Simulations of carrier distribution . . . . . . . . . . . . . . . 112

6.3 Discussion . . . . . . . . . . . . . . . . . . . . . . . . . . . 113

6.4 Conclusions . . . . . . . . . . . . . . . . . . . . . . . . . . 116

7 **Applications for Deep Depletion MOS Transistors** **117**

7.1 Requirement for Buffer Amplifier . . . . . . . . . . . . . . . 117

7.2 Inverter Analysis . . . . . . . . . . . . . . . . . . . . . . . 123

7.3 Cascode Amplifier Analysis . . . . . . . . . . . . . . . . . . 127

7.4 Cascode Amplifier with Bipolar Transistor . . . . . . . . . . 130

7.5 Conclusions . . . . . . . . . . . . . . . . . . . . . . . . . . 134

8 **Conclusions** **136**

8.1 Objectives and Achievements . . . . . . . . . . . . . . . . . 136

8.2 Future Work . . . . . . . . . . . . . . . . . . . . . . . . . . 138

8.3 Summary . . . . . . . . . . . . . . . . . . . . . . . . . . . 139

A **Noise in Conventional MOS Transistors** **140**

A.1 Introduction . . . . . . . . . . . . . . . . . . . . . . . . . . 140

A.2 Process Details . . . . . . . . . . . . . . . . . . . . . . . . 141

A.3 Low Frequency Noise in Enhancement Mode MOS Transistors 145

A.4 Low Frequency Noise in MOS Transistors with no Threshold Implant . . . . . . . . . . . . . . . . . . . . . . . . . . . . 153

A.5 Low Frequency Noise in Depletion Mode MOS Transistors . 155

**B Comparison with Kandiah's Results** 160

**Bibliography** 166

**Relevant Publications** 177

# Definition[†]

**noise** *n.* any undesired electrical disturbance in a circuit, degrading the useful information in a signal.

[†]From "The Collins Dictionary of the English Language".

# Chapter 1

# Introduction

One of the most important advantages of metal oxide semiconductor (MOS) transistors is their small size, and their consequent ease of integration [1]. This attribute can prove useful in certain analogue signal processing applications where silicon area may be at a premium. One such application is the silicon backplane for advanced infra-red detection systems [2]. Focal plane detector arrays fabricated in, for example, cadmium mercury telluride are mounted on a silicon integrated circuit using advanced hybrid technology. The silicon circuits supply the necessary bias conditions for the array of detectors, and some means of processing the signal from each detector. Typical interface circuits require a buffer amplifier with moderate gain, high input impedance, and low noise. To a large extent, the detector element pitch dictates the area available for this circuitry on the silicon. Such applications deal with extremely small signal currents, and conventional MOS transistors with the conducting channel close to the silicon-silicon dioxide interface [3] have proved too noisy.

Junction field effect transistors (JFETs) differ from conventional MOS transistors in that the conducting channel is constrained by the depletion

layers surrounding two reverse biased $p - n$ junctions [4]. An advantage of this type of structure is that the charge forming the conducting channel is isolated from any interfaces or junctions which could make significant contributions to the electrical noise seen in the device. Thus, the measure noise levels are in general much lower for JFETs than MOS transistors, where the charge is in intimate contact with the silicon-silicon dioxide interface [5].

There are, however, considerable problems in incorporating JFET technology in applications such as the infra-red detector interface circuitry described above. Junction FETs require additional space for device isolation [6]. This conflicts with the high packing density require by the application outlined above. An additional problem would be the extra processing steps required to fabricate the JFETs on the same wafer as the remainder of the MOS circuitry.

The aim of this research, therefore, was to see if existing MOS process technology could be used to design an MOS transistor with the inherent advantages of the JFET. The standard process used was the Philips C500 $n$-well CMOS process. Devices were fabricated at the Philips Components plant, Southampton.

Now, Buried-channel Charge-Coupled Devices (BCCDs) [7] offer lower intrinsic noise then Surface Charge-Coupled Devices (SCCDs) by isolating the charge packed from the silicon-silicon dioxide interface by a surface depletion layer. The BCCD structure is formed by fabricating the CCD gates over an $n$-well (assuming $n$-type packets). Thus, by forming an MOS transistor in an $n$-type well on a $p$-type substrate well it should be possible to bias the device such that the conducting channel is isolated from the silicon-silicon dioxide interface.

In this thesis, these devices shall be referred to as *deep depletion* MOS transistors. By depleting the surface region of these devices, they can be made to conduct in *buried channel* mode, and it is this mode of conduction that is of principal concern here. Results of noise measurements on these structures are presented and a model to explain their noise performance is developed.

There are three main objectives in this thesis.

- To show that the deep depletion mode MOS transistor offers superior noise performance when compared with conventional surface channel devices.

- To explain this improved noise performance using simulations of the charge distribution in the devices.

- To consider the suitability of the deep depletion mode MOS transistor for use in a buffer amplifier for infra-red applications.

Detailed d.c. characteristics are presented for the deep depletion mode devices. Notably, parameters such as transconductance, $g_m$, and forward conductance, $g_{ds}$, are measured at bias points where the device noise performance is known. *It is shown that an order of magnitude reduction in the low frequency noise performance is possible with little or no degradation in the transistor gain for a selected range of operating points.*

A computer model which solves Poisson's equation in one dimension is presented. Solving Poisson's equation in one dimension is shown to be an excellent means of modelling MOS transistor behaviour when they are biased in the linear region. Results of simulations on deep depletion mode devices

are used to explain observed noise performance and measured d.c. characteristics.

A number of other more conventional MOS structures are characterised in order to confirm that the measured noise in these deep depletion structures is indeed low. In particular, $n$-channel enhancement mode, 'intrinsic' enhancement mode (MOS transistors with no threshold implant in the channel region), and depletion mode mode transistors are investigated in Apendix A.

## 1.1 The Deep Depletion mode MOS transistor

Figure 1.1 shows a schematic cross-section of a deep depletion mode MOS transistor. The specific details of the device fabrication are presented in Chapter 2. For completeness a brief description of device fabrication is presented here. The starting material is a $p$-type substrate. An $n$-well is formed on this substrate by a combination of ion implantation and high temperature drive-in. Source and drain contacts are formed by diffusing donors into the $n$-well. Device fabrication then proceeds as for conventional MOS technology with gate-oxide growth, polycrystalline silicon deposition, *etc.*

The detailed operation of these deep depletion mode MOS transistors will be discussed in Chapter 2.

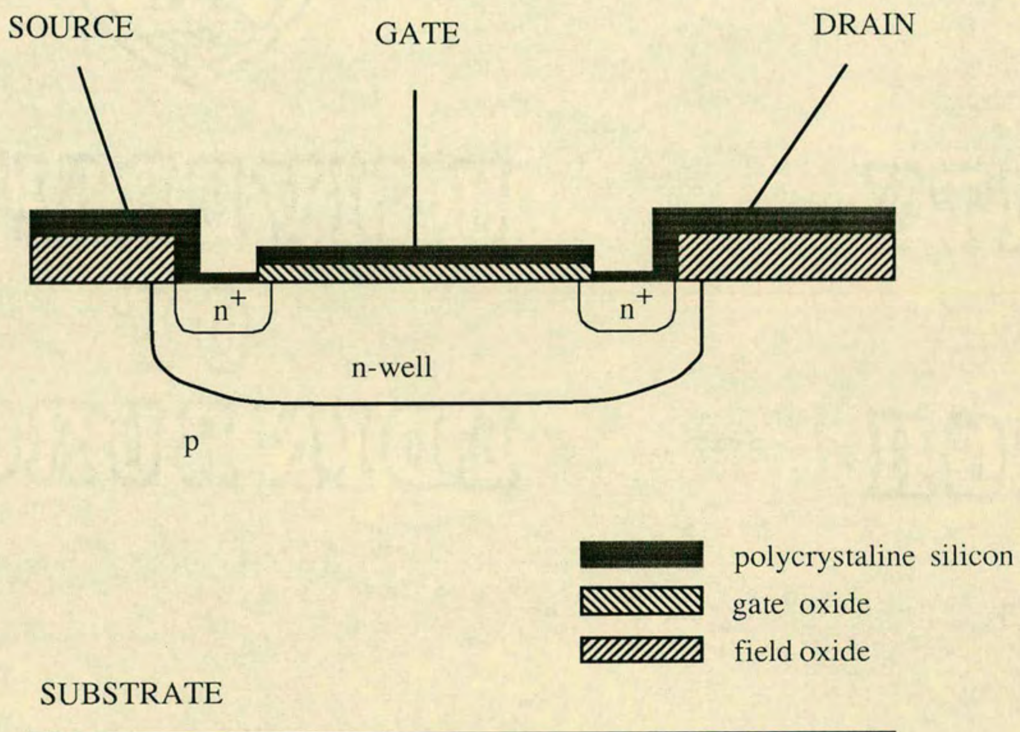



Figure 1.1: Schematic cross section of a deep depletion mode MOS transistor.

## 1.2 Thesis Plan and Structure

Chapter 2 presents an description of the fabrication of the MOS transistors studied in this thesis. A process modelling program, ICECREM, is used to simulate the doping profiles of the deep depletion MOS transistors. Doping profiles from ICECREM offer insight into the physical structure of the MOS transistors studied here. In addition, the simulated profiles can be used as input to the device modelling program discused in Chapter 3. The detailed operation of the deep depletion mode MOS transistors is discussed. The chapter is concluded by a study of noise mechanisms relevant to MOS transistors, and shows how noise sources are combined to give the characteristic noise spectral density.

Chapter 3 presents a program for solving Poisson's equation in one dimension using numerical methods. By using the profiles generated by ICECREM in Chapter 2, it is shown how this numeric solution may be used to model the spatial distribution of charge forming the channel. It is shown that solving Poisson's equation permits predictions of noise behaviour in deep depletion mode MOS transistors to be made.

Chapter 4 gives an overview of the theory and practice of noise measurements. The characteristics of the apparatus are discussed, and the techniques used contrasted with those used by some other authors.

Chapter 5 presents measured noise results for $n$-channel deep depletion mode MOS transistors described in Chapter 2. It is shown that by careful choice of bias point an order of magnitude reduction in low frequency noise levels is possible in these deep depletion mode devices. Simulations performed using the program discussed in Chapter 3 show that low noise

operation is achieved when the charge forming the channel is moved into the bulk silicon. It is shown that an optimum bias condition exists, and this bias point is investigated.

Chapter 6 describes a low frequency oscillation measured in depletion and deep depletion mode $n$-channel MOS transistors at temperatures lower than ambient. The effect was seen as a periodic and temporary increase in the channel resistance. Although the magnitude of this effect was shown to be small, it prevented complete characterisation of the noise in depletion devices at low temperature.

Chapter 7 considers possible applications for the low noise deep depletion mode MOS transistors investigated in this thesis. It is shown that the devices have poor saturation characteristics giving them a relatively high channel conductance. This conductance precludes their use in conventional buffer amplifiers such as the simple inverter. In order to exploit their low noise performance, a novel design of cascode amplifier is proposed incorporating a bipolar transistor with a deep depletion mode MOS transistor at the amplifier input. Such a design might be realised using combined bipolar and CMOS (Bi-CMOS) process technology.

Chapter 8 draws conclusions from results and analysis in the thesis, and discusses possible future areas for research.

To confirm that the measured noise levels are indeed low, measurements for a number of other MOS transistor technologies are presented in Appendix A. Specifically, $n$-channel enhancement, and $n$-channel depletion mode transistors are characterised. It is shown that the characteristics of the enhancement transistors are predictable and easy to model. Depletion mode devices are shown to exhibit similar characteristics to deep depletion devices, but

any reduction in noise as the charge is pushed away from the channel is much less pronounced. "Intrinsic" enhancement MOS transistors having no implant in the channel region are shown to have noise characteristics very similar to those for conventional enhancement transistors. This result indicates that any damage resulting from the boron implant is annealed out and does not make a significant contribution to the low frequency noise level.

# Chapter 2

# Device Fabrication and Physics

In this chapter we begin by presenting details of the fabrication of the deep depletion mode MOS transistors studied here. Simulations of the doping profiles in the MOS transistors can be used to deduce the distribution of charge which forms the conducting channel. The operation of the deep depletion mode MOS transistors is discussed. Finally in this chapter, a survey of noise mechanisms relevant to the MOS transistor is presented.

## 2.1 Process Details

In this section the process steps which lead to the fabrication of the deep depletion mode MOS transistors studied here are discussed.

A schematic cross section of the deep depletion mode MOS transistor was presented in Chapter 1. The ICECREM [8] process simulation package was used to model the expected doping profile of the deep depletion mode MOS transistor. The profiles generated are used as input to the simulations

in Chapter 3, Chapter 5, and Chapter 6. ICECREM is introduced in the following section.

### 2.1.1 ICECREM

ICECREM is a one-dimensional simulation package which can be used to model device doping profiles. The program provides a graphical user interface to the models used in SUPREM [9], a non-interactive process simulation package. The user enters details of individual process steps such as oxidation and implantation. The process steps would normally be simulated in the order in which the fabrication takes place. The order is important because of important cumulative effects which occur during processing, such as diffusion of impurities during oxidation.

After each process step the user is presented with a graphical representation of the device doping profile after that step.

By means of illustration, Figure 2.1 shows a typical dialogue between the user and ICECREM. Computer prompts are shown in bold type to distinguish them from user data. Lines starting with an asterisk are user comments, and have been added for clarity. Figure 2.1 is precisely the input used to simulate the deep depletion profile discussed in the following section (the profile is illustrated in Figure 2.2).

### 2.1.2 Fabrication of Deep Depletion MOS Transistors

All *n*-channel deep depletion mode MOS transistors studied here were formed on *p*-type wafers with a crystal orientation of <100>. This orientation is

```
Select key : title                        * For reference
  Enter text : Deep Depletion

Select key : substrate                    * Substrate details
  ornt     elem     conc
  100      boron    4.3e14

Select key : grid                         * Grid spacing and depth
  dxsi     xmax
  0.01     10

Select key : oxidize                      * Initial Oxide
  temp     time     model
  905      70       d

Select key : implant                      * Phosphorus Implant
  elem     energy   dose
  phos     80       7.2e11

Select key : oxidize                      * Drive-in
  temp     time
  1050     1440

Select key : plot                         * Request Plot

Select key : end
```

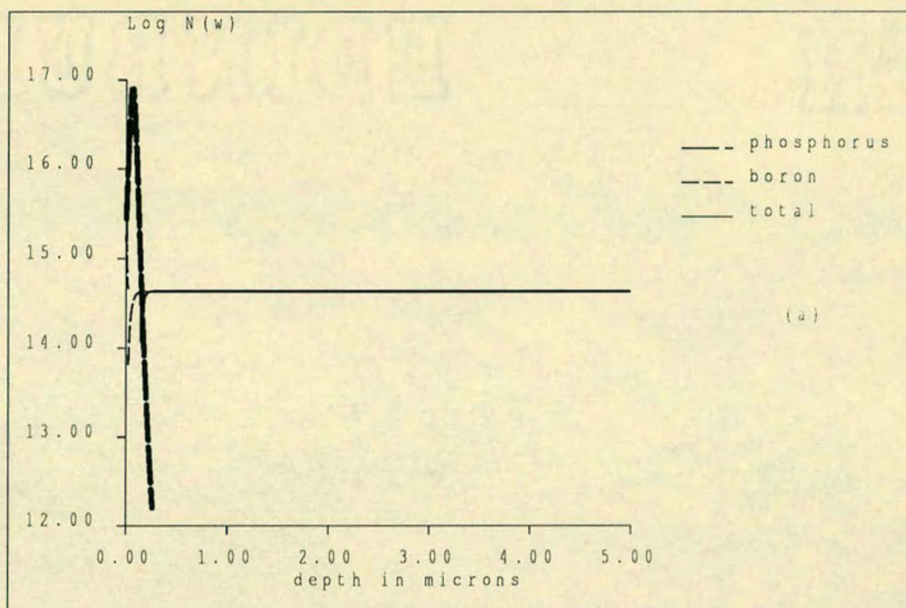
Figure 2.1: Typical user dialogue with ICECREM.

preferred over <111> since it has a lower density of atoms in the surface plane. Indeed, an oxide grown on a <100> crystal orientation can produce one tenth the trap density of an oxide of similar thickness with <111> orientation [10]. Subsequent sections will show that a low trap density is desirable for low noise transistors.

The boron substrate doping was $5.5 \times 10^{14} atoms\ cm^{-3}$, giving a sheet resistivity of $15 - 20\ \Omega\ cm^{-2}$. This substrate doping was rather lower than conventional values ($\approx 10^{15} atoms\ cm^{-3}$) [10]. However, this light doping offers the designer of analogue MOS circuits smaller source-drain capacitance, and a device threshold voltage which will be less sensitive to substrate bias. The lower substrate doping will, however, lead to a reduced source-drain punchthrough voltage. Punchthrough voltage was not a problem in this study since the devices geometries studied here were large with measured channel lengths typically in the range 6 $\mu m$ to 15 $\mu m$. The device geometries are typical of those used in analogue circuits in infra-red applications.

Deep depletion $n$-channel MOS transistors were fabricated by forming the devices in an $n$-well as shown in Figure 1.1. The well was formed by implanting phosphorus through a 300 Å oxide thickness into the silicon. The dose was $7.2 \times 10^{11}\ cm^{-2}$ at an energy of 80 $keV$. Figure 2.2 (a) shows the ICECREM doping profile immediately after the phosphorus implant. The crucial stage in the fabrication of the deep depletion MOS transistor is the long drive-in at high temperature. The wafers were heated to 1050 °C for 24 hours. This resulted in a modelled $p$-$n$ junction depth of 2.85 $\mu m$. This is illustrated in Figure 2.2 (b), which shows the ICECREM profile after the drive-in.

Some of the deep depletion devices were subjected to an additional ar-



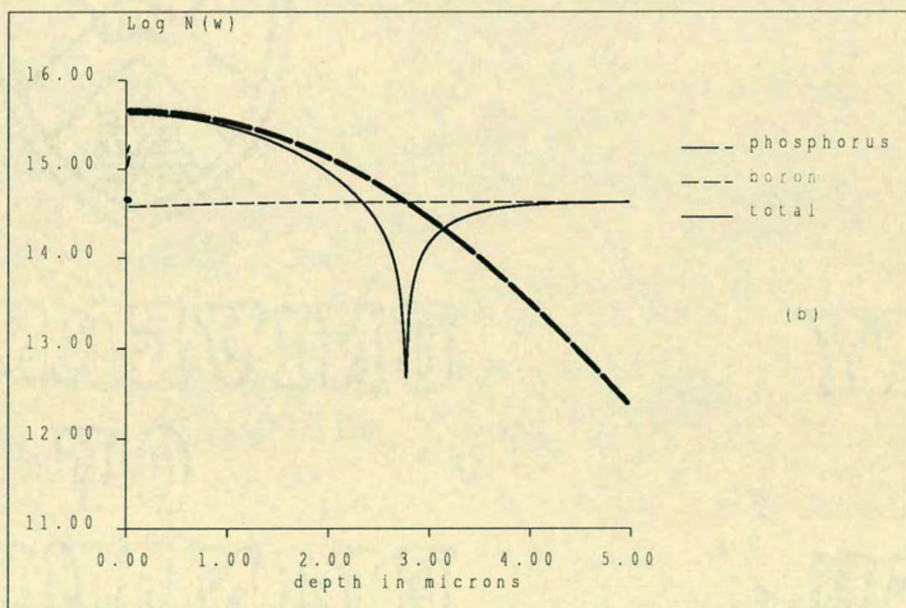




Figure 2.2: ICECREM profiles for deep depletion mode MOS transistor immediately after implant (a) and at end of fabrication (b).

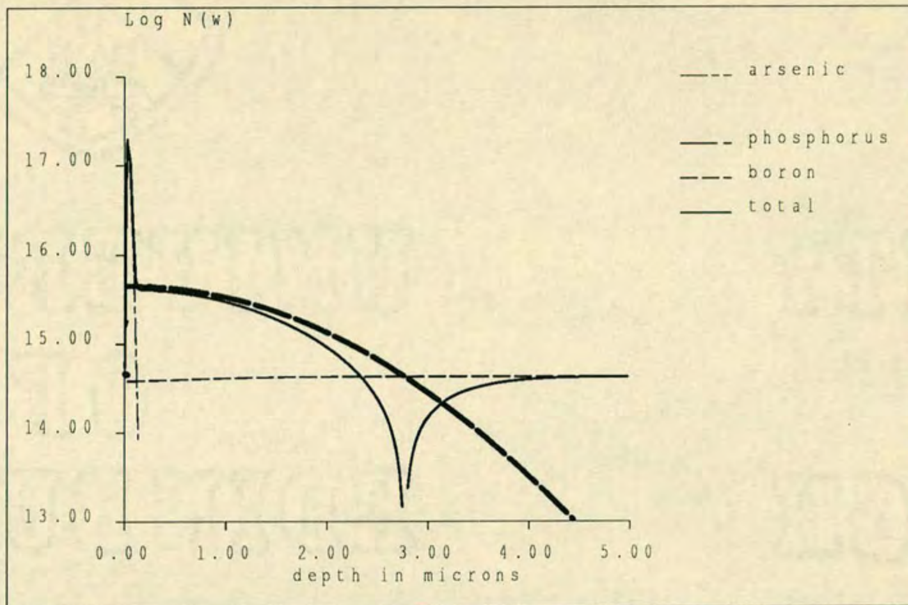



Figure 2.3: ICECREM profile for deep depletion mode MOS transistor with additional arsenic implant.

senic implant after the phosphorus drive-in. The oxide was first removed and the arsenic implanted directly into the silicon at an energy of 40 $keV$ This was then annealed at 950 °C for 30 minutes. The resulting profile as modelled by ICECREM is shown in Figure 2.3.

The two deep depletion mode profiles shown in Figures 2.2 (b) and 2.3 are based on profiles used in buried channel charge-coupled devices (BCCDs) [7, 11]. The latter doping profile with the additional arsenic implant is used in CCD applications where increased speed and charge handling capacity are required [12, 13]. The increased speed is a direct result of the bulk mobility being higher than the surface mobility.

After the deep $n$-well had been defined by implantation and drive-in, the source and drain contacts were fabricated. Phosphorus was diffused from an $n^+$ region deposited in the areas where source and drain contacts were to be

Drain connections

D1 D2 D3 D4

Gate Source

polycrystaline silicon gate
source and drain contacts
n-well implant

Figure 2.4: Plan of 4 transistors as configured on the test chip. A common gate and common source are used to reduce the pin count.

formed. This $n^+$ deposition came from $POCl_3$ gas. A 950 °C drive-in for 60 minutes gave a diffusion depth of around 0.1 $\mu m$.

Figure 2.4 shows a floor plan of part of the test chip. Four devices of each kind were fabricated on the chip. The design width of each device was 100 $\mu m$, with the channel lengths ranging from 6 $\mu m$ to 15 $\mu m$ in 3 $\mu m$ steps. Common source and drain connections were routed to each MOS transistor, with separate connections for the drain of each device.

## 2.2 Operation of Deep Depletion MOS Transistor

It is commonly reported that low frequency noise in MOS transistors arises chiefly through interaction between carriers in the channel region and traps located near the silicon-silicon dioxide interface [14, 15, 16, 17]. It follows, therefore, that if the conducting channel can be made to form away from the interface then the low frequency noise could in principle be reduced.

Figure 2.5 shows a cross-section of a deep depletion MOS transistor through the channel region. There are two depletion regions in this device. A junction depletion region of width $x_1$ is formed around the metallurgical junction between the $p$-type substrate and the $n$-type well, see Figure 2.5. Assuming for the moment that we have an abrupt junction between the $n$-type well and the $p$-type substrate, the width of this depletion region can be calculated from [4]

$$x_1 = \left[\frac{2\epsilon_{Si}}{q}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)V\right]^{\frac{1}{2}} \tag{2.1}$$

where $\epsilon_{Si}$ is the permittivity of silicon, $q$ is the electronic charge, $N_A$ and $N_D$ are the acceptor and donor concentrations, and $V$ is the built-in voltage of the $p$-$n$ junction less the applied external (reverse bias) voltage. This applied voltage will be the potential difference between the conducting channel and the $p$-type substrate. At the source end of the channel, this external voltage will be $V_{BS}$. Thus, from Equation 2.1 it can be seen that the width of this depletion region is modulated by the substrate bias, $V_{BS}$. In addition, the width of the depletion layer at the drain end of the channel will be greater than the source end since $V_{BD} > V_{BS}$ under normal bias conditions, *i.e.* $V_{BS}$ negative, $V_{DS} > 0$. For real non-abrupt doping profiles the depletion width

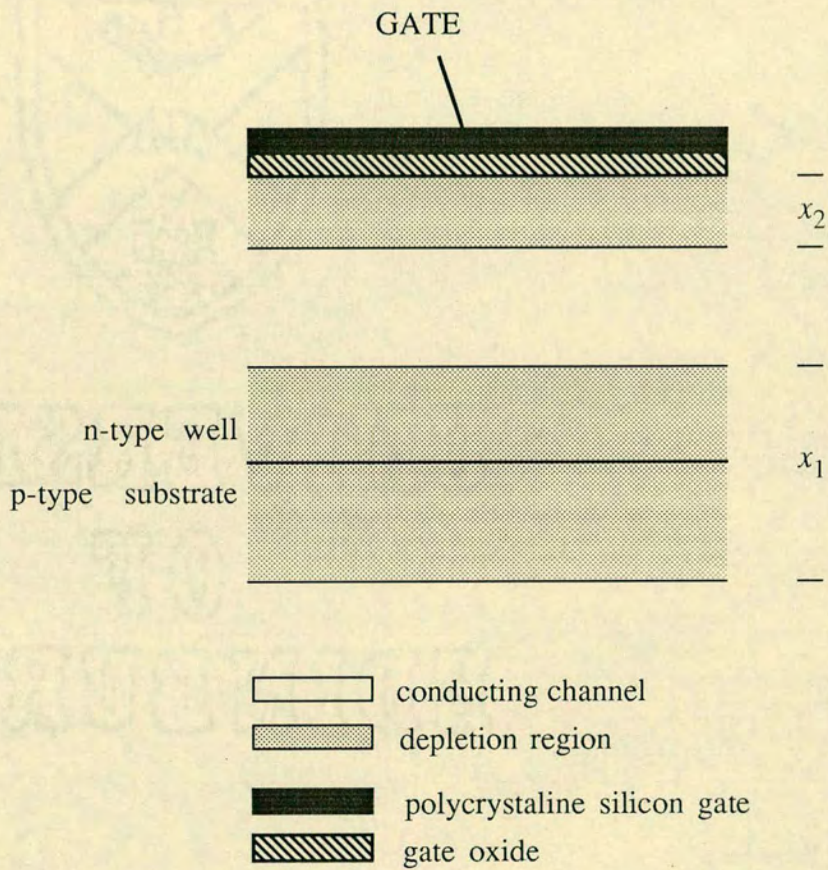



Figure 2.5: Cross section through channel of a deep depletion mode MOS transistor.

is not accurately modelled by Equation 2.1, but in general the width of the depletion region will increase with increasing substrate to channel voltage.

A second depletion region of width $x_2$ will be formed immediately under the gate. The width of this surface depletion layer at the source end of the channel can be approximated by [18]

$$x_2 = \left[\frac{2\epsilon_{Si}}{q}\left(\frac{1}{N_D}\right)(-V_{GS} + \psi_S)\right]^{\frac{1}{2}} \tag{2.2}$$

where $\psi_S$ is the surface potential. Recalling that the threshold voltage is negative for these deep depletion structures, is will be clear that the depletion width will again be largest at the drain end of the channel. Depleting the channel of free carriers by making the gate more negative is analogous to the pinch-off mechanism in a junction field effect transistor (JFET) [19].

As the gate voltage is reduced, a layer of the depleted region immediately under the gate will eventually become inverted. If the gate voltage is then reduced further, the additional voltage will be dropped over this inversion layer. As a result, the width of the surface depletion layer will have reached a maximum when the surface becomes inverted. If pinch-off has not been achieved for this gate voltage and drain bias, then the only way to reduce the drain current further would be by modulating the depletion region round the metallurgical junction by modulating the substrate bias.

It was found that a substrate bias of at least $-5$ $V$ was required in the deep depletion mode transistors in order to turn the device 'off'. If the bias was less negative than this, then the metallurgical junction depletion width was not wide enough to allow the device to turn off for any drain voltage. Measurements of the gate voltage characteristic under such conditions would show that the gate lost control of the channel when the bias was sufficiently negative for surface inversion to occur. This gate voltage was found to be

around $-5$ $V$. As will be seen in Chapter 5, the measurements on deep depletion MOS transistors were made with a substrate bias chosen so as to prevent surface inversion.

From Figure 2.5 and Equation 2.2 it is clear that for gate voltages, $V_{GS}$, less than the channel voltage plus the built in potential, the channel will be isolated from the gate oxide by a surface depletion region [20]. If the main contribution to low frequency noise in these devices comes from traps close to the silicon-silicon dioxide interface then we would expect to see a substantial improvement in the low frequency noise performance. Indeed, these structures are ideal for investigating noise performance as a function of channel position. By changing the gate voltage and substrate potential in opposite directions with respect to the source, it is possible to move the channel spatially while preserving the drain current. To achieve this, the gate and substrate voltages need to be changed by differing magnitudes. There are two reasons for this. Firstly, the coupling between the gate and the channel is substantially reduced when the charge forming the channel is moved into the bulk. This has the added effect of reducing the device transconductance, $g_m$, to a large extent. Secondly, the bulk mobility can be up 50 % higher than the surface mobility [21]. Therefore the channel will occupy less volume when it is in the bulk for a constant drain current.

Figure 2.6 shows a schematic representation of the surface and junction depletion regions to illustrate the points discussed above. The device is biased just above threshold voltage in the buried channel mode. Figure 2.7 shows a schematic of the band bending in this device at a position half way between the source and drain. The simulation program to be introduced in Chapter 3 can be used to estimate the metallurgical junction depletion layer

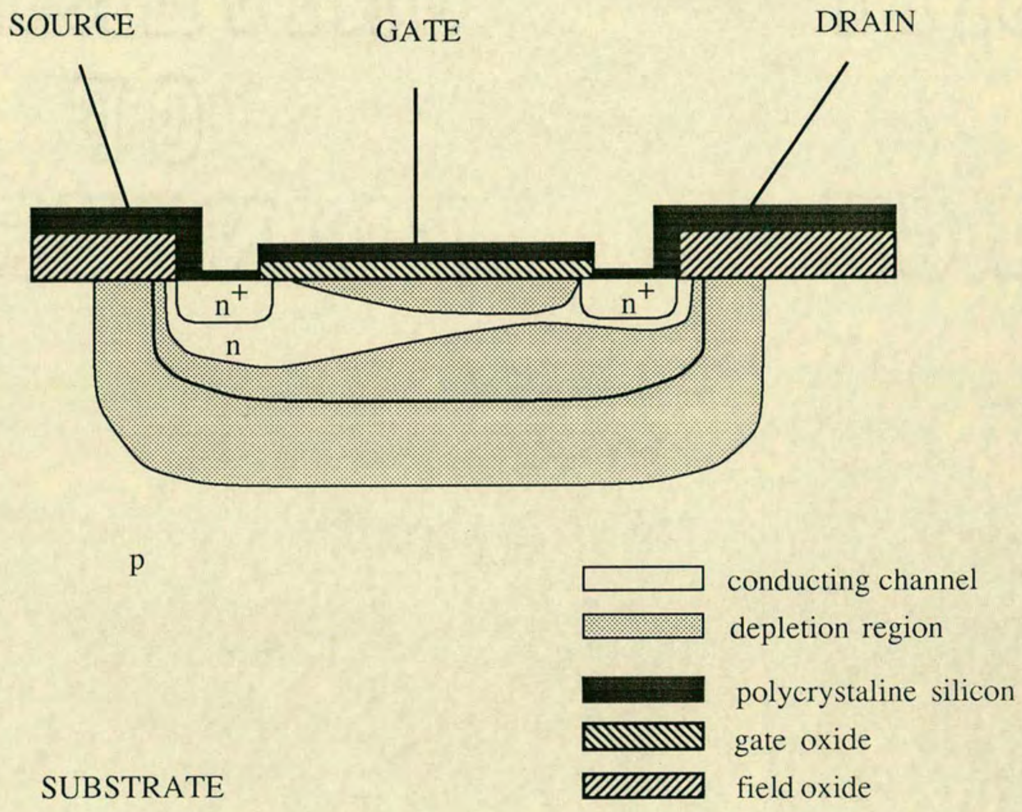



Figure 2.6: Surface and junction depletion layers in a deep depletion mode MOS transistor.

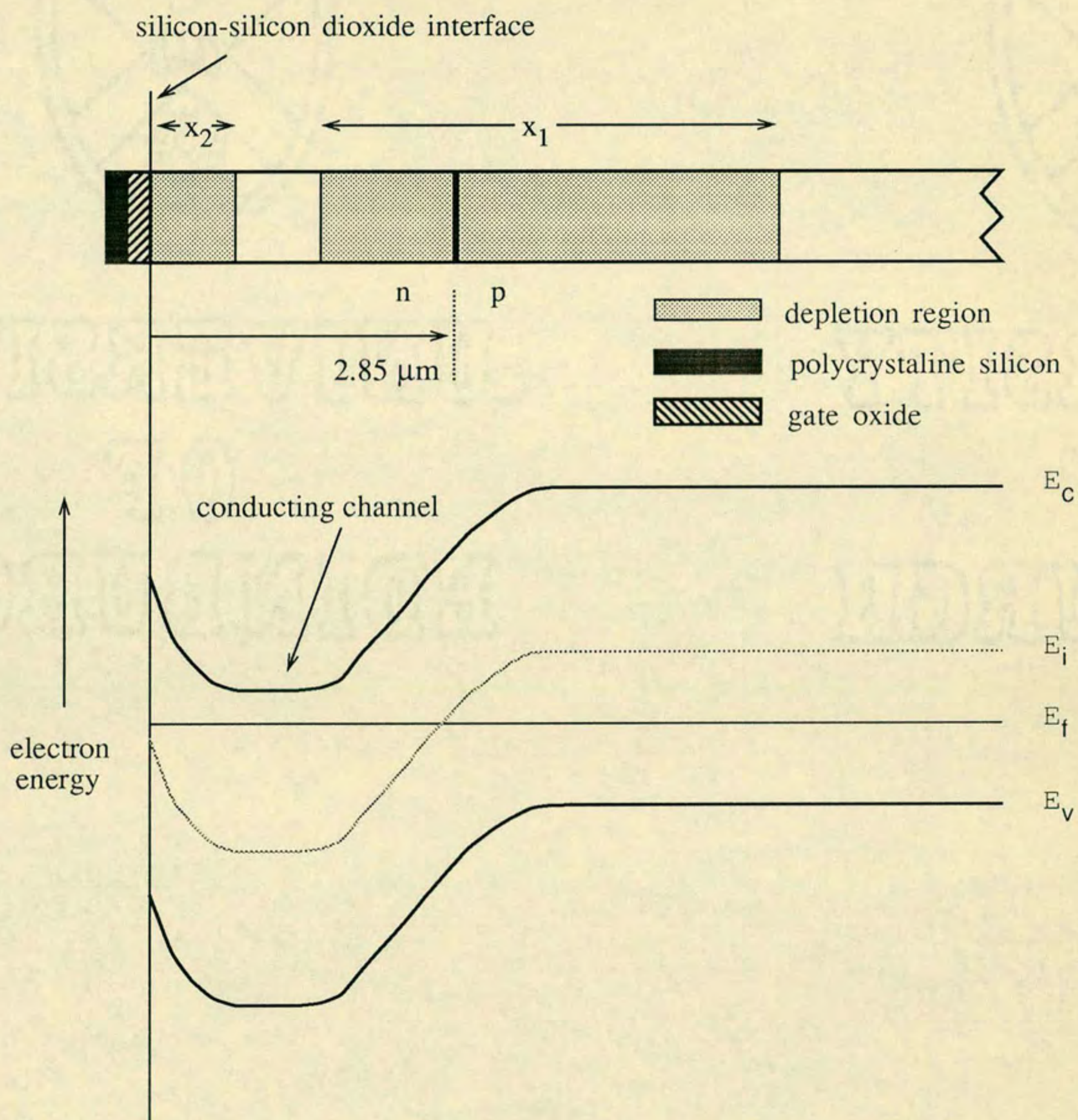



Figure 2.7: Schematic diagram showing band bending in a deep depletion mode MOS transistor biased above pinch-off in the buried channel mode. As the gate voltage is reduced, the bands at the surface will be 'pulled' up, and the width of the surface depletion layer will increase.

width, $x_1$, and the surface depletion width, $x_2$. For example, a substrate bias $V_{BS}$ of $-5V$ will result in a the metallurgical junction depletion width extending around $1.2\mu m$ up into the $n$-well. A gate voltage $V_{GS}$ of $-4V$ would result in a surface depletion width of around $0.6\mu m$. These estimates were based on the results shown in Figure 3.12.

## 2.3 Noise Mechanisms

There are three types of noise relevant to the operation of the MOS structures examined here: thermal noise, shot noise and flicker noise [22].

### 2.3.1 Thermal Noise

In 1928 Johnson [23] found experimentally, with a theoretical proof given by Nyquist [24], that the root mean square (r.m.s.) noise voltage, $v_n$, across a resistance, $R$, in thermal equilibrium at an absolute temperature, $T$, was

$$v_n = \sqrt{4kTRB_n} \tag{2.3}$$

where $k$ is Boltzmann's constant and $B_n$ is the bandwidth of the measuring system.

The voltage spectral noise density, $S_V(f)$, expresses the magnitude of the noise at each point in the frequency domain, and can be given by

$$S_V(f) = \frac{\overline{v_n{}^2}}{B_n} \tag{2.4}$$

where $\overline{v_n{}^2}$ is the mean square noise voltage. For thermal noise, this is constant throughout the frequency domain, see Figure 2.8. Thus, thermal noise is often referred to as 'white' noise. In practice quantum effects cause the

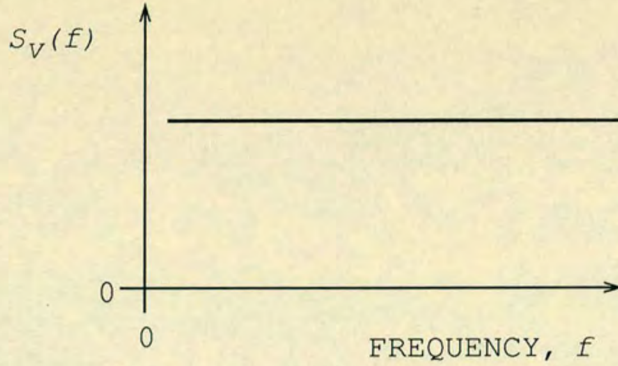



Figure 2.8: Noise spectral density for thermal noise.

thermal noise to deviate from a white spectrum at frequencies above around 100 $GHz$.

It is well known that Equation 2.3 applies to any passive two terminal network at a temperature, $T$, with a series resistance, $R$ [25]. In the context of MOS transistors biased below 'saturation' where the device appears like a linear resistance, $R$ is $1/g_{ds}$ where $g_{ds}$ is the small signal channel conductance [26]. The thermal noise level provides a white noise 'floor', *i.e.* the theoretical noise minimum for that resistance at that particular temperature.

With the MOS transistor in saturation, the equivalent input noise can be referred to the gate, and can be shown to be [27]

$$v_n = \sqrt{\frac{8}{3}kTRB_n/g_m} \tag{2.5}$$

where $g_m$ is the device transconductance.

### 2.3.2 Shot Noise

In 1918 Schottky [28] carried out the first theoretical study of fluctuations in the anode circuit of a temperature-limited thermionic diode. This study lead to the concept of the 'shot' noise source. Shot noise is also seen in solid state devices and arises from the correlated departure of carriers entering a

space-charge region separating $p$-type and $n$-type material. The magnitude of the r.m.s. shot noise current, $i_n$ is given by

$$i_n = \sqrt{2eI} \qquad (2.6)$$

where $e$ is the electronic charge and $I$ is the d.c. current flowing in the device. This equation assumes a *full* shot noise contribution to the measured noise in a device carrying a current of $I$. As will be shown in Chapter 5, under certain circumstances it is possible to have a *partial* shot noise contribution. The spectral density of shot noise is white. As we shall see later, the noise results presented here indicate that deep depletion mode MOS transistors appear to have a broad-band shot noise contribution when operated in the saturation mode.

### 2.3.3 Flicker Noise

All electronic devices carrying a direct current exhibit a low frequency 'flicker' noise in excess of the thermal or shot noise floor. In many devices the noise power increases approximately in inverse proportion to the frequency. Thus flicker noise is often called '$1/f$'[†] noise, and has been observed over an extensive frequency range with measurements having been made from $10^{-5}$ $Hz$ to 10 $MHz$ [29, 30, 31]. Theoretically, the noise must level out as zero frequency is approached for $\alpha \geq 1$, otherwise the integrated noise energy would be infinite.

It should be noted that flicker noise has been observed in a wide range of physical systems. As well as electrical devices such as semiconductors

[†] Many authors refer to low frequency noise as $1/f$ noise. However, the frequency dependence is rarely if ever $1/f$, but more generally $1/f^{\alpha}$ with $\alpha$ normally close but not equal to unity. The term flicker noise is preferred.

and thermionic valves, flicker noise has been measured in systems as diverse as the distribution of the flood levels in the river Nile [32], traffic current densities [33], and the motions of the geographic pole [34].

The noise spectral density of flicker noise can be expressed as

$$S_V(f) = \frac{C}{f^\alpha} \tag{2.7}$$

where $C$ is a constant for a given sample under a specified bias and temperature.

There can be little doubt that flicker noise is due to trapping states of some kind, but a physical model which can explain the huge range of time constants observed has remained elusive. What can be said is that trapping is more likely in the vicinity of a surface or interface because of higher trap densities, see *e.g.* [3]. Results presented here confirm this since the noise in a deep depletion MOS transistor is reduced substantially when the channel is made to form in the bulk away from the silicon-silicon dioxide interface.

Many models have been proposed to explain the high magnitude of low frequency noise observed in MOS transistors relative to, for example, bipolar transistors [35, 5]. Models suggested can be divided into two distinct categories. The first category account for flicker noise by considering fluctuations in carrier mobility. This was first suggested by Hooge [36, 37], with subsequent refinements by a number of authors, *e.g.* reference [35]. The second class of model belongs to the number fluctuation category. In this case, the low frequency noise is explained by considering physical mechanisms which lead to fluctuations in the number of free carriers in the device. The spread of time constants involved with the identified mechanism gives rise to the frequency dependency of the noise. A description of each of the two types of model follows.

Hooge's model for low frequency noise assumes that the mobility of free charge carrier fluctuate independently of one another. The net effect of this mobility fluctuation is a noise spectral density given by the empirical formula

$$S_V(f) = \frac{\alpha_H}{Nf} V^2 \tag{2.8}$$

where $\alpha_H$ is the Hooge constant with the value $\alpha_H = 2 \times 10^{-3}$, $N$ is the number of free charge carriers in the sample, and $V$ is the voltage across the sample. To account for the experimentally observed values of $\alpha_H$ less than $2 \times 10^{-3}$, the theory was modified by Hooge and Vandamme [38]. They suggested that only collisions between the charge carriers and the lattice were responsible for the flicker noise, and not surface and impurity scattering. This leads to a modification of the Hooge equation

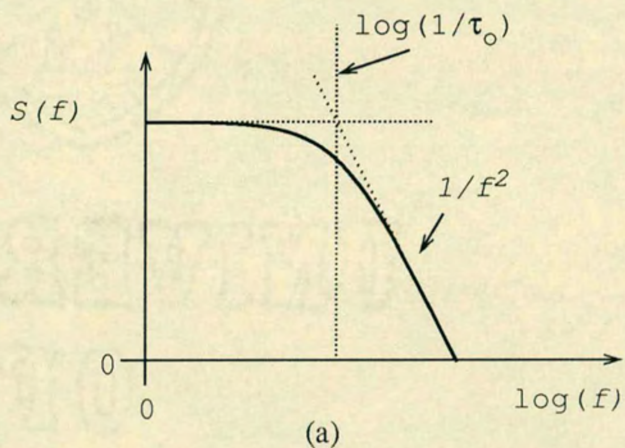
$$S_V(f) = \frac{\alpha_H}{Nf} V^2 \left[ \frac{\mu}{\mu_L} \right]^2 \tag{2.9}$$

where $\mu$ is the mobility of the charge carriers and $\mu_L$ is the mobility of the carriers if only lattice scattering occurs.

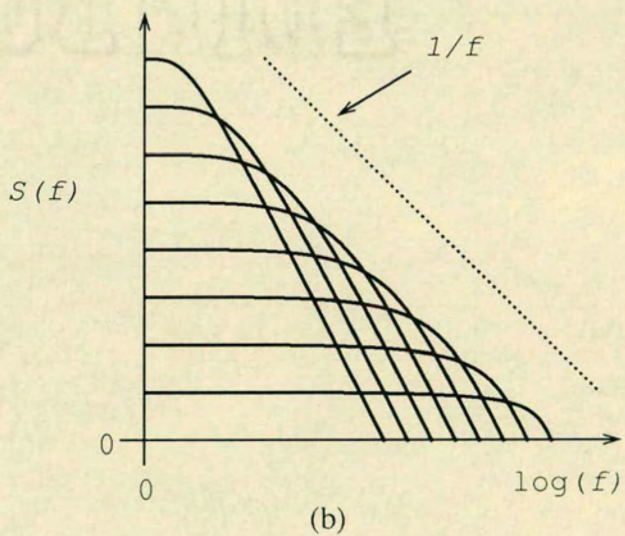
In the number fluctuation model, first proposed by McWhorter [39], the characteristic $1/f^\alpha$ spectrum is built up from a range of discrete trapping events, each associated with its own time constant, $\tau_o$. Now, a single trap with an associated time constant will give rise to a Lorentzian type spectrum, see Figure 2.9 (a). The spectral density for this single trap can be found from

$$S(f) = A \frac{\tau_o}{1 + \omega^2 {\tau_o}^2}. \tag{2.10}$$

If we now have a wide range of trapping events, then the combined effect of all the Lorentzian distributions can produce a single spectrum with a reciprocal dependence on frequency, see Figure 2.9 (b).



(a)



(b)

Figure 2.9: Pure Lorentzian spectrum (a) with a characteristic time of $\tau_o$, and $1/f$ spectrum formed by superposition of multiple Lorentzian spectra (b).

Both models have difficulty in explaining the wide frequency range over which flicker noise can be observed. No one mechanism has been identified which can explain the range of time constants observed.

Modifications to the McWhorter number fluctuation model have been proposed in order to help explain this anomaly [40, 41]. For example, instead of direct interaction with traps, the free carriers may interact indirectly by first becoming trapped in a fast surface state and then subsequently tunnelling into a trap in the oxide. Fu and Sah [41], for example, observed that flicker noise is proportional to the surface state density as the silicon-silicon dioxide interface, and not the oxide trap density. This gives a wider range of time constants than just the capture and relaxation time for the trap itself. However, the time constants for the fast surface states are normally small when compared to the time constants for the oxide traps. Hence the noise spectrum is still dominated and limited by the range of time constants associated with the oxide traps.

Further evidence that flicker noise is caused by number fluctuation and not mobility fluctuation is provided by Uren *et al* [42]. They report a deviation from a pure $1/f$ spectrum for very small area MOS transistors. In small area devices a relatively small number of surface states exist at the interface. Deviations from the $1/f$ spectrum were attributed to the decomposition of the spectrum into its discrete Lorentzian components.

A further somewhat unconventional model which attempts to explain the wide range of time constants seen is developed by Bell [43]. Bell treats flicker noise as a queueing problem. In his analysis, a key assumption is that carriers are swept away from centres from where they originated. This is reasonable since a flicker noise voltage is only normally seen in the presence of an applied

field. Another assumption is that the time taken for a carrier to recombine is determined by the time taken to find a vacant site elsewhere. Now, taking a statistical average over a large area, the number of excited carriers in the conduction band will be equal to the number of vacant sites in the valence band. However, the distribution of centres and carriers will not always be uniform throughout the area. Thus at any given instant in time in a given unit area there may be more carriers than there are free sites. This collection of carriers can be viewed as a queue waiting for a free recombination site. Classical congestion and delay queuing theory may then be applied. In this context a queue is an excess of the rate at which individuals demand service over the rate at which the service is available. The problem is analogous to that of requests arriving at a telephone exchange as described by Fry [44]. Here the arrival time of each request can be described by a Poisson distribution, *i.e.* the arrival time of any given request is not dependent on the arrival time of the previous request. To continue this analogy, a charge carrier joins the queue when it is excited into the conduction band. Now, if $n$ is the number of service outlets (base level sites in this analysis), and $r$ is the rate at which carriers are excited into the conduction band, then service queue theory dictates that for unit time the mean waiting time, $\bar{\tau}$, for service is given by

$$\bar{\tau} = \frac{k}{n - r} \tag{2.11}$$

for some constant $k$. Note that in unit time $n$ is the rate at which carriers return to the valence band. From Equation 2.11 it can be seen that as the rate of service requests (excitation) approaches the rate of service (recombination) then the queueing time (time spent in the conduction band) can have any value up to infinity.

Fry showed that the probability of waiting in a queue for a service with an exponential time spent in that service for a queuing time in the range $(t, t + dt)$ is

$$P(t, t + dt) = k_2(n - r)\exp[-(n - r)t]dt. \qquad (2.12)$$

When $(n - r)$ tends to zero, as above, the exponential term tends to unity and all times between zero and infinity are equally likely. Thus, it is the wide spread of equally likely carrier queuing times which gives rise to the 1/f type spectrum over such an extensive frequency range.

## 2.4 Summary

This chapter has described the fabrication of the deep depletion mode and other more conventional MOS transistors studied in this thesis. The ICECREM simulation package was used to generate 1-D impurity profiles for the devices. Conduction mechanisms in the deep depletion mode MOS transistor were discussed. The noise mechanisms relevant to MOS transistors were described.

# Chapter 3

# Impurity Freezeout

In this chapter a computer program is presented which solves Poisson's equation in one dimension. The model was developed by Jaeger and Gaensslen [45, 46] in order to simulate impurity freezeout effects in MOS capacitors. Emphasis in their work was on low temperature operation [47]. Modifications were made to the strategy here to enable deep depletion MOS transistors to be simulated, and to permit the output of additional parameters such as the total integrated carrier concentration under the gate. The latter parameter can be used to calculate the drain current when the device is biased in the linear region. Simulations are used to explain observed changes in MOS transistor d.c. performance such as a distortion in the gate voltage characteristic at low temperature [48], and a reduction in low frequency noise seen in depletion mode devices under certain specific bias conditions [49]. Freezeout effects at very low temperature ($< 10\ K$) are described in detail in [50]. Simulations here show that the effects of freezeout are important even at room temperature. This is particularly true for the deep depletion MOS transistors described in this thesis, since the concentration of donor impurities is low and close to the substrate doping.

## 3.1 Introduction

Many authors have used the solution of Poisson's equation to study the behaviour of MOS devices [19, 51, 52, 53]. The solution to Poisson's equation can be used, for example, to calculate the charge distribution under the gate. Further, knowledge of the charge distribution can be used to model the threshold behaviour of the device and predict capacitance-voltage characteristics. The simulation program presented here solves Poisson's equation in one dimension. The program can be used to simulate a number of *geometry independent* effects in MOS transistors device of any given doping profile when biased in the *linear* or *sub-threshold* regions. In order to simulate devices biased in the saturation or triode regions we would have to develop a two dimensional simulation program which is outwith the scope of the work presented here. Simulations performed using this program can be used to explain the reduction in measured noise in deep depletion mode MOS transistors biased in the linear region.

Most simulation programs currently available assume full impurity ionisation and often do not model fully the low temperature dependences of parameters. For example, the MINIMOS two dimensional device simulation package [54] uses models for parameters such as mobility which are only valid down to 223K (-50 °C). The model presented here can be used to simulate MOS transistors any temperature in the range 50-350K.

Table 3.1 shows the input data required in order to simulate a device at some specified bias and temperature, and lists the quantities which may be requested as output. The acceptor and donor concentrations can be generated from process data using ICECREM as discussed in Chapter 2. Alterna-

| | Quantity | Symbol | Units |
|---|---|---|---|
| INPUT | Temperature | $T$ | $K$ |
| | Substrate Bias | $V_{BS}$ | $V$ |
| | Acceptor Concentration | $N_A(x)$ | $cm^{-3}$ |
| | Donor Concentration | $N_D(x)$ | $cm^{-3}$ |
| | Grid Spacing | $H(x)$ | $cm$ |
| | Surface Potential | $\Psi_S$ | $V$ |
| | Gate Oxide Thickness | $T_{OX}$ | Å |
| OUTPUT | Gate Voltage | $V_G$ | $V$ |
| | Ionised Acceptor Concentration | $N_A^+(x)$ | $cm^{-3}$ |
| | Ionised Donor Concentration | $N_D^-(x)$ | $cm^{-3}$ |
| | Hole Concentration | $p(x)$ | $cm^{-3}$ |
| | Electron Concentration | $n(x)$ | $cm^{-3}$ |
| | Integrated Carrier Concentration | $N_C$ | $cm^{-2}$ |

Table 3.1: Simulation program input parameters and output data.

tively, an arbitrary doping profile can be generated using simple Gaussian or Error functions distributions to enable investigation of unusual structures. A further option would be to use data from Sims measurements as the basis of the profile input. Further, Buehler [55] describes a technique for measuring the doping profile by studying the d.c. characteristics of the MOS transistor. The latter options were not investigated here. Simulations of actual devices were performed using ICECREM doping profiles as input.

During simulation of a specific device the strategy is as follows. The temperature, $T$, and substrate bias, $V_{BS}$, are selected. These remain constant throughout the simulation. For each value of surface potential, Poisson's equation is solved numerically. The solution enables calculation of the gate voltage, $V_{GS}$, and the distribution of charge under the gate oxide. In addition, the program can be set to run with the surface potential, $\Psi_s$, swept over some range at user selected intervals. Intermediate data can be stored on disc files on the computer, and subsequently used to display quantities such as the integrated carrier concentration, $N_C$, variation with gate voltage, $V_{GS}$.

In the sections which follow, we examine the formulation of Poisson's equation including the temperature dependence of all relevant parameters, we present the algorithm for solving Poisson's equation numerically, the implementation of the algorithm is discussed and results are presented which show simulations of depletion mode and deep depletion mode MOS transistors. Simulations are used to explain a number of measured effects in physical devices.

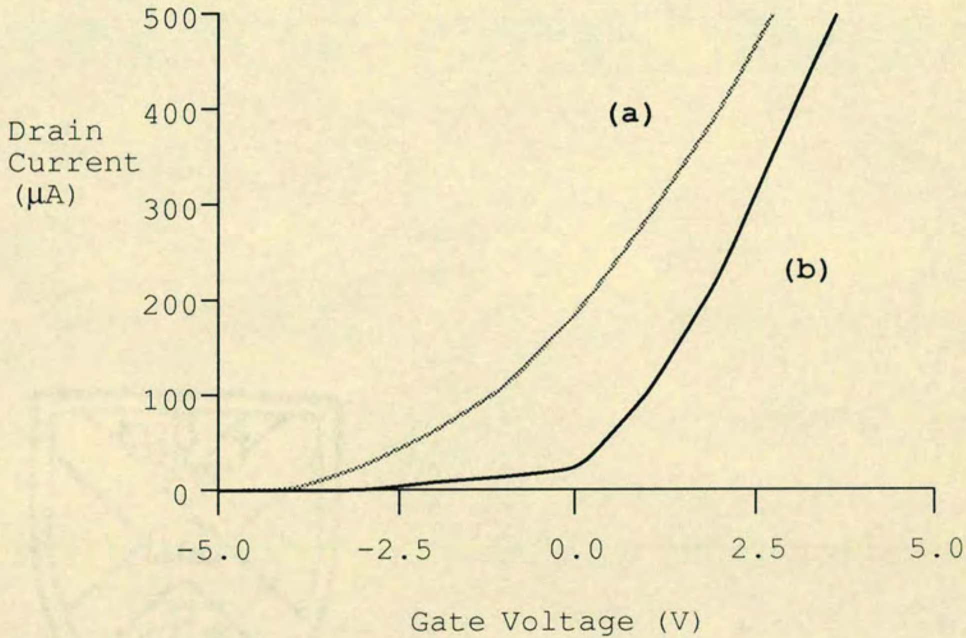



Figure 3.1: Gate voltage characteristic for depletion mode MOS transistor at 300 $K$ (a) and 77 $K$ (b). $V_{DS} = 1V$, $V_{BS} = -1V$.

## 3.2 Experimental Results

In this section results of measurements are presented which show an unusual distortion of the gate voltage characteristic in depletion and deep depletion mode MOS transistors. This effect is *not* seen in measurements for enhancement mode surface channel devices. In the sections which follow we explain this effect by considering the effects of impurity freezeout in these devices.

Figure 3.1 shows the gate voltage characteristic of a depletion mode MOS device at 300 $K$ (a) and 77 $K$ (b). At 300 $K$ a conventional device turn-off is seen with a threshold voltage, $V_{TH}$, of around $-3.5\ V$. At 77 $K$ the threshold

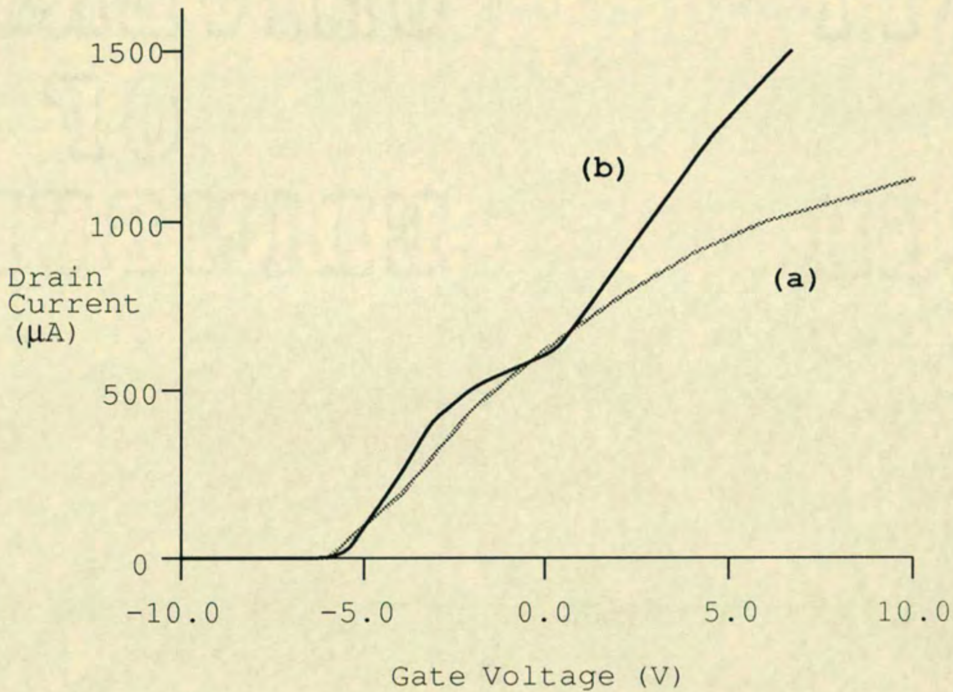



Figure 3.2: Gate voltage characteristic for deep depletion mode MOS transistor at 300 $K$ (a) and 77 $K$ (b). $V_{DS} = 500mV$, $V_{BS} = -15V$.

voltage at first sight appears as though it is much more positive at around 0 $V$. As the gate attempts to turn the device off, however, it seems to lose control of the charge forming the channel. The result is a discontinuity in the characteristic at a gate voltage of around 0 $V$. Below $-2$ $V$ the gate appears to regain control of the channel and the device turns off normally once again.

Figure 3.2 shows a similar effect in a deep depletion mode MOS transistor. At 300 $K$, Figure 3.2 (a), we see a gate voltage characteristic yielding a threshold voltage of around $-6$ $V$. Once again, at 77 $K$ in Figure 3.2 (b)

the gate appears to have difficulty in depleting the channel of free charge. We now develop a program which solves Poisson's equation in one dimension. Output from simulations is used to show that the above effect can be attributed to impurity freezeout.

## 3.3 Formulation of Poisson's Equation

In the following analysis, let us define $x$ as the distance into the silicon substrate with $x = 0$ at the silicon-silicon dioxide interface. In addition, let the total charge density $\rho(x)$ to be the sum of the electron, hole and ionised impurity concentrations, so that

$$\rho(x) = q(p - n + N_D^- - N_A^+) \tag{3.1}$$

where $N_D^-$ and $N_A^+$ are the ionised impurity concentrations. In order to calculate the variation of carrier concentrations with distance $x$ into the semiconductor we need to solve Poisson's equation

$$\frac{d^2\Psi}{dx} = -\frac{q}{\varepsilon_s kT}\rho(x) \tag{3.2}$$

for a set of well defined boundary conditions. For the present problem, these boundary conditions are zero electric field in the substrate of the MOS transistor, and some specified potential at the silicon-silicon dioxide interface. Using the above notation, we can express these boundary conditions as

$$\left.\frac{d\Psi}{dx}\right|_{x\rightarrow\infty} = 0 \tag{3.3}$$

$$\Psi_{(x=0)} = \Psi_S \tag{3.4}$$

where $\Psi_S$ is the surface potential. For an arbitrary doping profile, Poisson's equation cannot be solved exactly in closed form. However, finite difference

methods can be used to obtain a numerical solution. Naturally, the solution to a set of difference equations is only an approximation to the exact analytical solution. The accuracy of the numerical solution depends on the resolution of the mesh chosen in any simulation.

Before examining the algorithm for the numerical solution to Poisson's equation, the temperature dependence of each of the terms in the equation are considered.

## 3.4 Temperature Dependence of terms in Poisson's Equation

In this section, the temperature dependence of each of the terms in Poisson's equation is discussed. From Equation 3.1, the charge density in the silicon is given by the sum of the free charge and the ionised impurity concentrations in the semiconductor. We now consider how temperature influences each of these concentrations.

### 3.4.1 Electron and Hole Concentrations

The concentration of electron and holes is given by

$$n = n_i \frac{\exp\{(E_{F_n} - E_i)/kT\}}{\xi\{(E_{F_n} - E_C)/kT\}} \tag{3.5}$$

$$p = n_i \frac{\exp\{(E_i - E_{F_p})/kT\}}{\xi\{(E_V - E_{F_p})/kT\}} \tag{3.6}$$

in which $\xi$ is a degeneracy correction factor with spatial dependence. Note the introduction of quasi-Fermi levels for electrons, $E_{F_n}$, and holes, $E_{F_p}$, in the expressions for carrier concentrations. When the substrate bias,

$V_{BS}$, is non-zero these quasi-Fermi levels are spaced symmetrically at $E_F \pm qV_{BS}/2kT$. At low temperatures and high channel concentrations the Fermi level may enter the conduction or valence bands. Under such conditions the values of hole and electron concentrations are adjusted by this degeneracy correction factor. From Wolf [56] we obtain

$$\xi(x) = 1 + 0.2709 \exp(-0.8173x). \tag{3.7}$$

The dependence of the intrinsic carrier concentration, $n_i$, on temperature was described by Barbar [57] as

$$n_i = 2.5 \times 10^{19} (m_c m_v)^{\frac{3}{4}} (T/300)^{\frac{3}{2}} \exp(-E_G/2kT). \tag{3.8}$$

Barber further derives empirically the following relationship describing the temperature dependence of the energy bandgap in silicon, $E_G$, as

$$E_G = 1.170 + 1.059 \times 10^{-6} T - 6.050 \times 10^{-7} T^2, \quad T \leq 170K \tag{3.9}$$

$$E_G = 1.179 - 9.025 \times 10^{-5} T - 3.050 \times 10^{-7} T^2, \quad T > 170K. \tag{3.10}$$

Figure 3.3 shows this temperature dependence.

Bludau, Onton and Heinke [58] derive the following expressions for the variation of electron and hole effective mass with temperature:

$$m_c = 1.045 + 4.5 \times 10^{-4} T \tag{3.11}$$

$$m_v = 0.523 + 1.4 \times 10^{-3} T - 1.48 \times 10^{-6} T^2. \tag{3.12}$$

### 3.4.2 Ionised Impurity Concentrations

The temperature dependence of the ionised donor and acceptor concentrations can be modelled using Fermi-Dirac statistics [4]. The ionised impurity

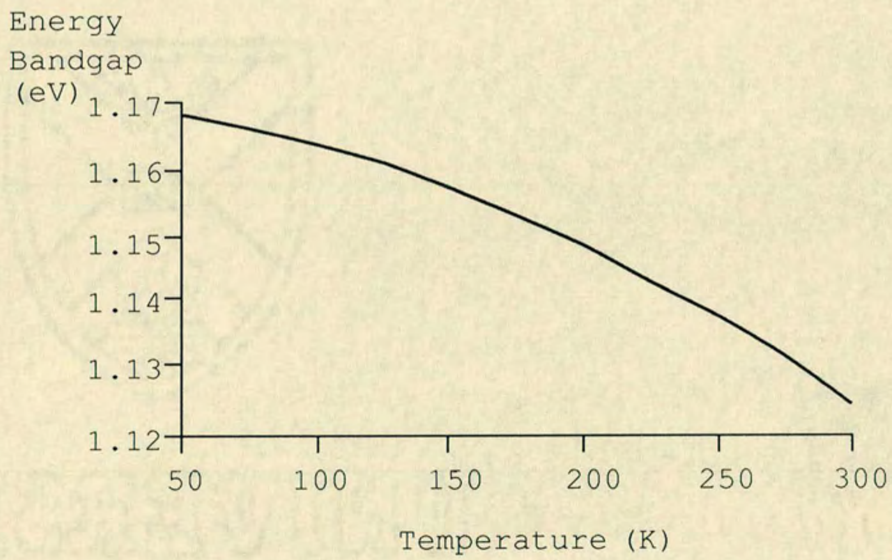



Figure 3.3: Temperature dependence of energy bandgap in silicon.

concentrations can then be given by

$$N_D^- = \frac{N_D}{1 + 2\exp(\frac{E_{F_n} - E_D}{kT})} \quad (3.13)$$

$$N_A^+ = \frac{N_A}{1 + 4\exp(\frac{E_A - E_{F_p}}{kT})} \quad (3.14)$$

noting the inclusion of quasi-Fermi levels for electrons, $E_{F_n}$, and holes, $E_{F_p}$, and that the differing degeneracy factors for the conduction and valence bands.

The temperature dependences of all the above parameters are taken into consideration in the simulation program.

## 3.5 Numerical Formulation of Poisson's Equation

The numerical approach adopted to solving Poisson's equation is now presented. Let us define the function $F$ to be the following

$$F = \frac{d^2\Psi}{dx} + \frac{q}{\varepsilon_s kT}\rho(x) = 0. \quad (3.15)$$

The solution of Poisson's equation is found by iteratively adjusting $\Psi$ until $F$ approaches zero (Newton's method [59]). Taking the first two terms in the Taylor series for $F$ we have that

$$F(\Psi + \Delta\Psi) \approx F(\Psi) + \frac{\delta F}{\delta\Psi}\Delta\Psi = 0. \quad (3.16)$$

Approximating $F(\Psi)$ to $F(\Psi + \Delta\Psi)$ in the above equation, and again forcing this to zero we have

$$\Delta\Psi = -\left[\frac{\delta F}{\delta\Psi}\right]^{-1} F(\Psi). \quad (3.17)$$

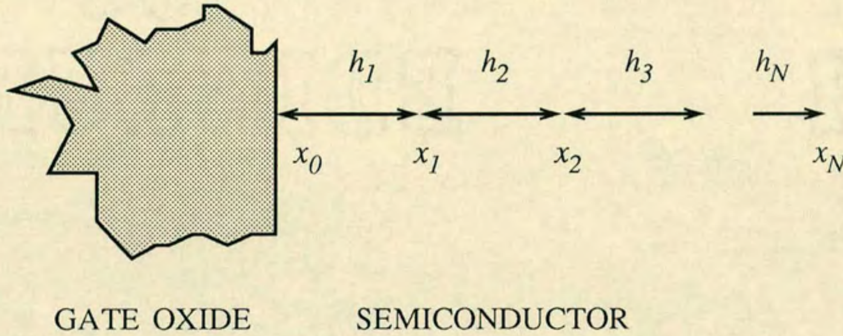



Figure 3.4: Grid of $N$ points as used by simulation program. Depth $x_0 = 0$ is taken to be at the silicon-silicon dioxide interface. The grid can be non-uniform, and the space between point $x_{j-1}$ and $x_j$ is $h_j$.

We now specify a mesh of $N$ points starting from the silicon-silicon dioxide interface and moving into the bulk, Figure 3.4. By taking a discrete approximation to Poisson's equation we produce a set of $N$ simultaneous equations from Equation 3.17

$$\Delta\Psi_j = -\left[\frac{\delta F_j}{\delta\Psi_k}\right]^{-1} F(\Psi_k) \tag{3.18}$$

or, more fully,

$$\begin{bmatrix} \Delta\Psi_1 \\ .. \\ \Delta\Psi_N \end{bmatrix} = -\left[\frac{\delta F_j}{\delta\Psi_k}\right]^{-1} \begin{bmatrix} F_1(\Psi_1, \Psi_2, .., \Psi_N) \\ .. \\ F_N(\Psi_1, \Psi_2, .., \Psi_N) \end{bmatrix} \tag{3.19}$$

Now, $\left[\frac{\delta F_j}{\delta\Psi_k}\right]$ is a tridiagonal matrix and $[\Delta\Psi_j]$ can be determined using

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Gaussian Elimination [51].

An initial try for $\Psi_1$ to $\Psi_N$ is obtained by letting $\rho(x) = 0$ and assuming full impurity ionisation. $\Psi$ is adjusted iteratively until $F$ at each mesh point is below some error bound, $\epsilon$, selected by the user. In *pseudo-code*, the program is

choose $\Psi_S$;

guess initial $\Psi_J$ by setting $\rho(x) = 0$;

**repeat**

calculate $\delta F/\delta\Psi$;

calculate $\Delta\Psi_j$ using Gaussian Elimination;

$\Psi_j = \Psi_j + \Delta\Psi_j$;

Calculate $F$;

**until** $|F_j| < \epsilon$;

$\Psi_j$ will then hold the computed value for the potential at the $j$th mesh point. In the sections which follow a number of simulations are presented for $n$-channel depletion and deep depletion mode MOS transistors.

## 3.6 Depletion Mode MOS Transistor

From the preceding analysis it should be clear that the degree of freezeout becomes more pronounced as the device operating temperature is reduced. The simulations in this section therefore show the freezeout in a depletion mode transistor at 77 $K$ and 130 $K$.

The input profile was that generated by ICECREM in Chapter 2. The profile used can be seen in Figure A.3. Figure 3.5 shows the output for

$V_{GS} = -1\ V$, $V_{BS} = -5\ V$. The output has been divided into three sets of data. The Figure 3.5 (a) shows the total donor concentration (continuous line) and the ionised impurity concentration (dashed line) as a function of depth. Figure 3.5 (b) shows the total free carrier (electron) concentration per $cm^3$. Figure 3.5 (a) illustrates that the degree of freezeout is greatest in the bulk. Near the surface the band bending is such that it tends to re-ionise the frozen out donors. The electrons are swept away from their donor sites towards the channel region by the field. Although the maximum carrier density is in the bulk for this gate voltage, the channel does appear to be touching the surface (where depth=0).

Now, Figure 3.6 shows the same device also at 77 $K$ but with a somewhat more negative gate voltage, $V_{GS} = -4\ V$. By comparing Figure 3.5 and Figure 3.6 we may deduce

- The overall degree of freezeout is less when the gate voltage, $V_{GS}$ is more negative (and closer to the device threshold voltage, $V_{TH}$).
- The channel has moved from being in contact with the silicon-silicon dioxide interface to being a buried channel.

Recalling the mechanisms for buried channel conduction from Chapter 2, we can explain these observations by considering the width of the surface depletion layer. As the voltage between the gate and the channel is increased then so does the width of the surface depletion layer. The band bending in this depletion layer is such that it tends to re-ionise donors which are frozen out. The more negative the gate voltage the greater the band bending. This forces more donors to ionise and release their carriers into the channel. This explains the unusual distortion seen in the gate voltage characteristic

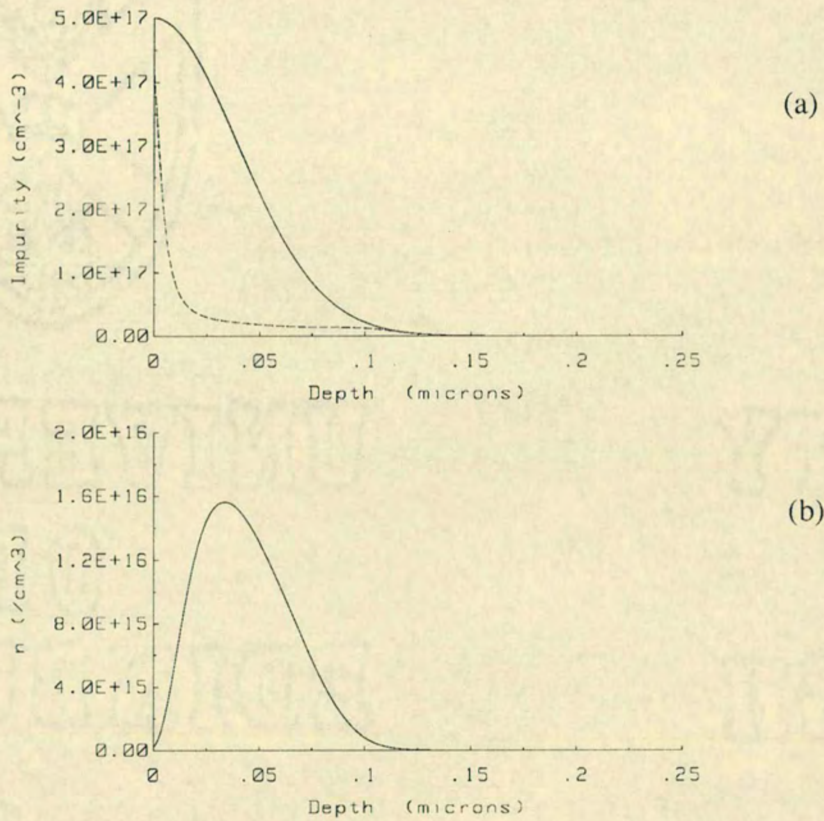



Figure 3.5: Simulation program output for depletion mode MOS transistor at 77 $K$ with $V_{GS} = -1\ V$, $V_{BS} = -5\ V$. Plot (a) shows the implanted donor impurity concentration (continuous line) and ionised impurity concentration (dashed line), and (b) shows the free carrier concentration.

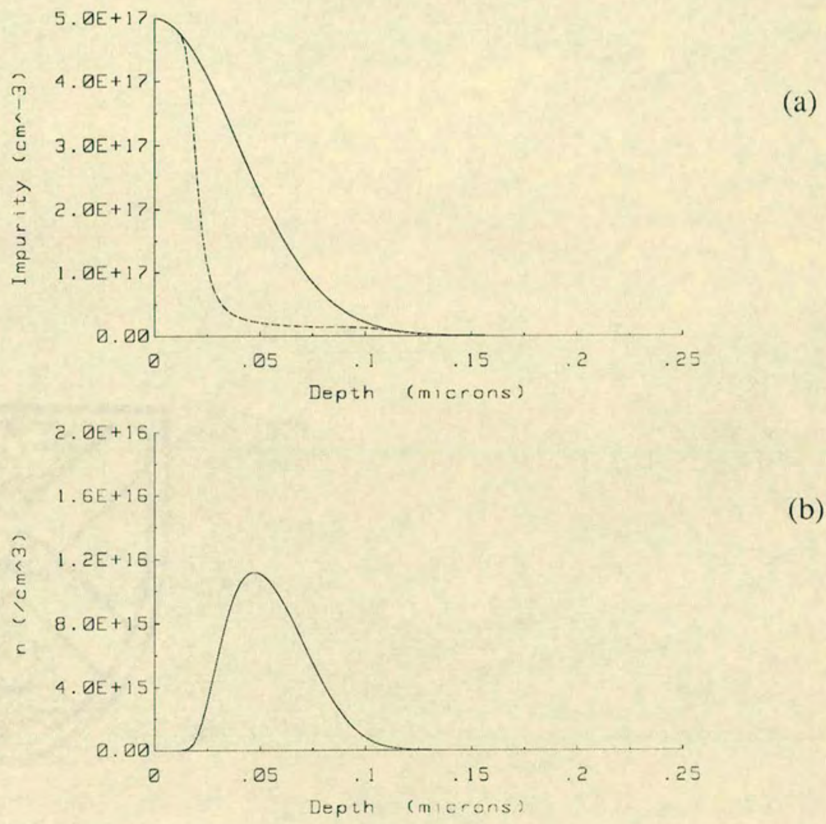



Figure 3.6: Simulation program output for depletion mode MOS transistor at 77 $K$ with $V_{GS} = -4$ $V$, $V_{BS} = -5$ $V$. Plot (a) shows the implanted donor impurity concentration (continuous line) and ionised impurity concentration (dashed line), and (b) shows the free carrier concentration.

in all kinds of depletion mode structures at low temperature, as discussed in Section 3.2.

Figure 3.7 and Figure 3.8 show simulations for the same doping profile but this time with a device operating temperature of 130 $K$. Figure 3.7 has a gate voltage of $-1$ $V$ whereas Figure 3.8 has a gate voltage of $-4$ $V$. In general, the degree of freezeout is less than that seen in the previous examples for temperatures of 77 $K$. However, the gate can still be seen to be modulating the extent of the freezeout in the surface region. Again, the donors near the surface tend to re-ionise as the gate attempts to deplete the channel region of carriers.

We now move on to consider carrier freezeout in deep depletion mode MOS transistors.

## 3.7 Deep Depletion MOS Transistor

In the previous section it was shown how a depletion mode MOS device could be biased to give a channel which was isolated from the silicon-silicon dioxide interface by the surface depletion region. In this section a series of simulations are presented for deep depletion mode devices. It is shown that a buried channel in these devices can be attained both at 77 $K$ and at room temperature.

The input doping profile was that generated by ICECREM for deep depletion devices, see Figure 2.2. Figure 3.9 shows the simulation program output for a simulation on this structure at 77 $K$. The gate voltage for this simulation is $V_{GS} = -1$ $V$ and the substrate potential is $V_{BS} = -5$ $V$. Figure 3.10 shows the same device with a gate voltage of $-4$ $V$. It can be seen

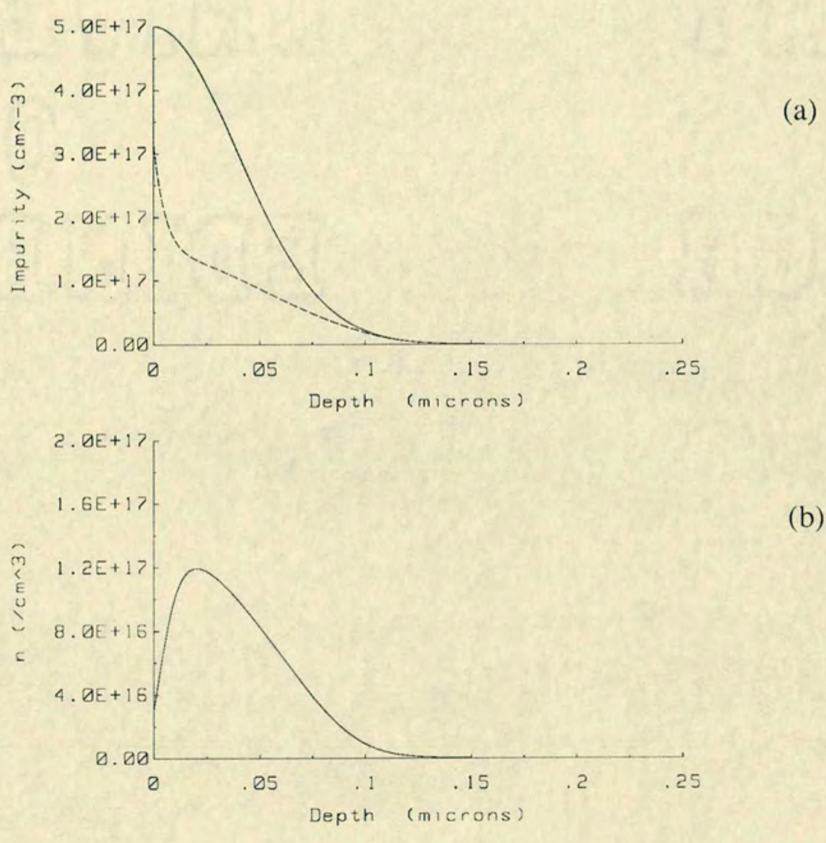



Figure 3.7: Simulation program output for depletion mode MOS transistor at 130 $K$ with $V_{GS} = -1\ V$, $V_{BS} = -5\ V$. Plot (a) shows the implanted donor impurity concentration (continuous line) and ionised impurity concentration (dashed line), and (b) shows the free carrier concentration.

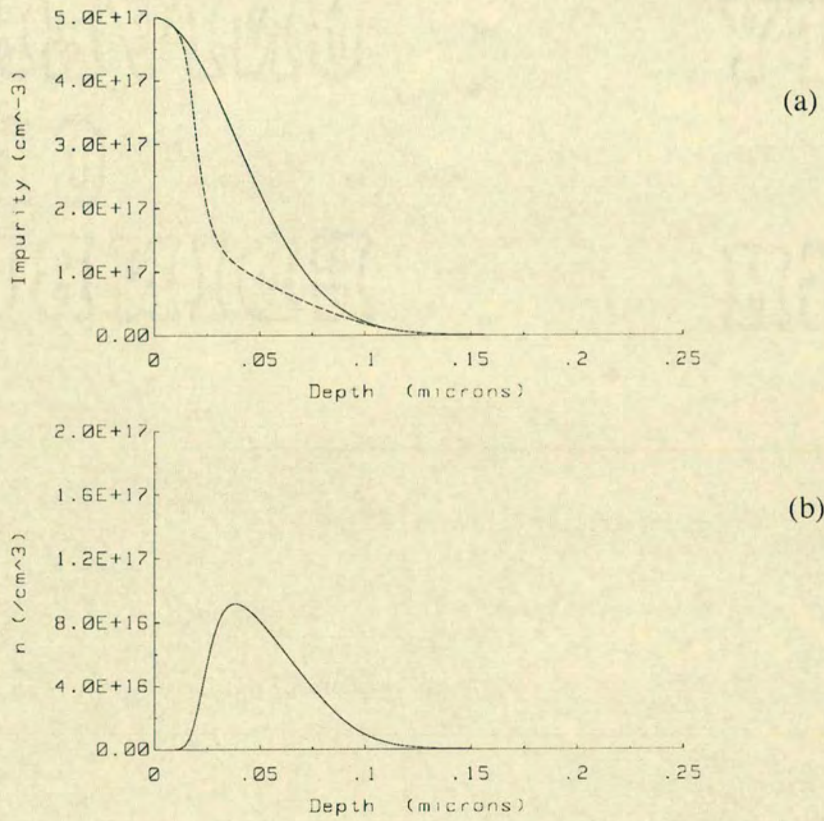



Figure 3.8: Simulation program output for depletion mode MOS transistor at 130 $K$ with $V_{GS} = -4\ V$, $V_{BS} = -5\ V$. Plot (a) shows the implanted donor impurity concentration (continuous line) and ionised impurity concentration (dashed line), and (b) shows the free carrier concentration.

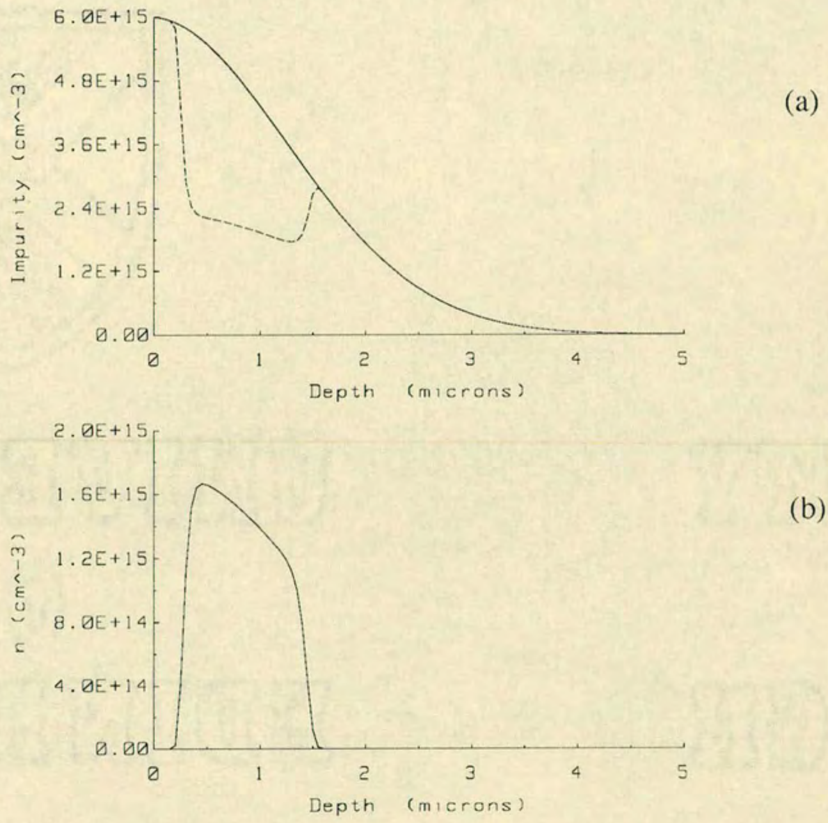



Figure 3.9: Simulation program output for deep depletion mode MOS transistor at 77 $K$ with $V_{GS} = -1\ V$, $V_{BS} = -5\ V$. Plot (a) shows the implanted donor impurity concentration (continuous line) and ionised impurity concentration (dashed line), and (b) shows the free carrier concentration.

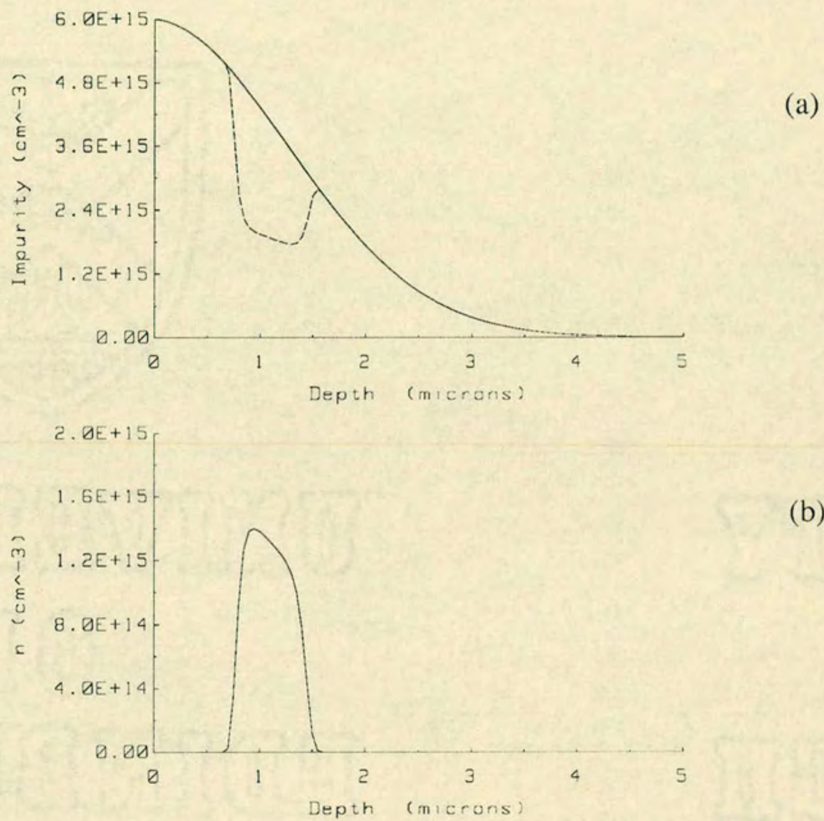



Figure 3.10: Simulation program output for deep depletion mode MOS transistor at 77 $K$ with $V_{GS} = -4\ V$, $V_{BS} = -5\ V$. Plot (a) shows the implanted donor impurity concentration (continuous line) and ionised impurity concentration (dashed line), and (b) shows the free carrier concentration.

that once again the degree of freezeout reflects the band bending and depletion layer widths. However, unlike the previous examples for a depletion mode device, it is possible to have a buried channel for a much wider range of gate voltages. Also, it can be seen that the overall degree of freezeout is less in deep depletion devices. This is due to the lower concentration of donors in these devices ($6 \times 10^{15} cm^{-3}$ at the surface as opposed to $5 \times 10^{17} cm^{-3}$ in the depletion mode MOS transistors discussed previously).

Figure 3.11 and Figure 3.12 show simulations for the same device at room temperature ($300\ K$) with gate voltages of $-1\ V$ and $-4\ V$ respectively. In these examples there is little or no freezeout apparent (the dashed lines and the heavy lines in the graph (a) of these figures are coincident), and the donor implant is fully ionised throughout the device. Again, it can be seen how the gate controls the position of the channel by modulating the width of the surface depletion region. The substrate side of the channel remains relatively stationary in these simulations since the substrate bias, $V_{BS}$, remains unchanged at $-5\ V$.

Finally, simulated results are compared with the measured results presented earlier in this chapter. Figure 3.13 shows the *integrated* carrier concentration under the gate, $N_C$, for a range of gate voltages at room temperature, (a), and at liquid nitrogen temperature, (b). The integrated carrier concentration is found by integrating the carrier concentration over the depth of the silicon, and as such it represents the free charge available for conduction. Thus, the integrated carrier concentration is given by

$$N_C = \int_0^\infty n(x)\, dx \tag{3.20}$$

where $n(x)$ is the free electron concentration at the depth $x$ into the semiconductor measured from the silicon-silicon dioxide interface. In practice,

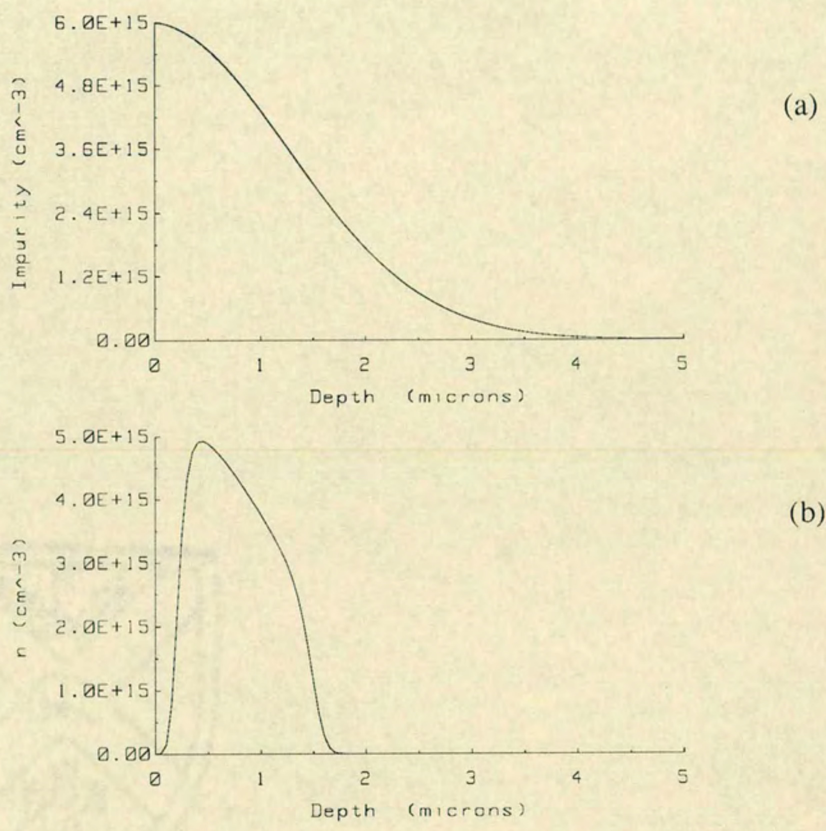



Figure 3.11: Simulation program output for deep depletion mode MOS transistor at room temperature with $V_{GS} = -1\ V$, $V_{BS} = -5\ V$. Plot (a) shows the implanted donor impurity concentration (continuous line) and ionised impurity concentration (dashed line), and (b) shows the free carrier concentration.

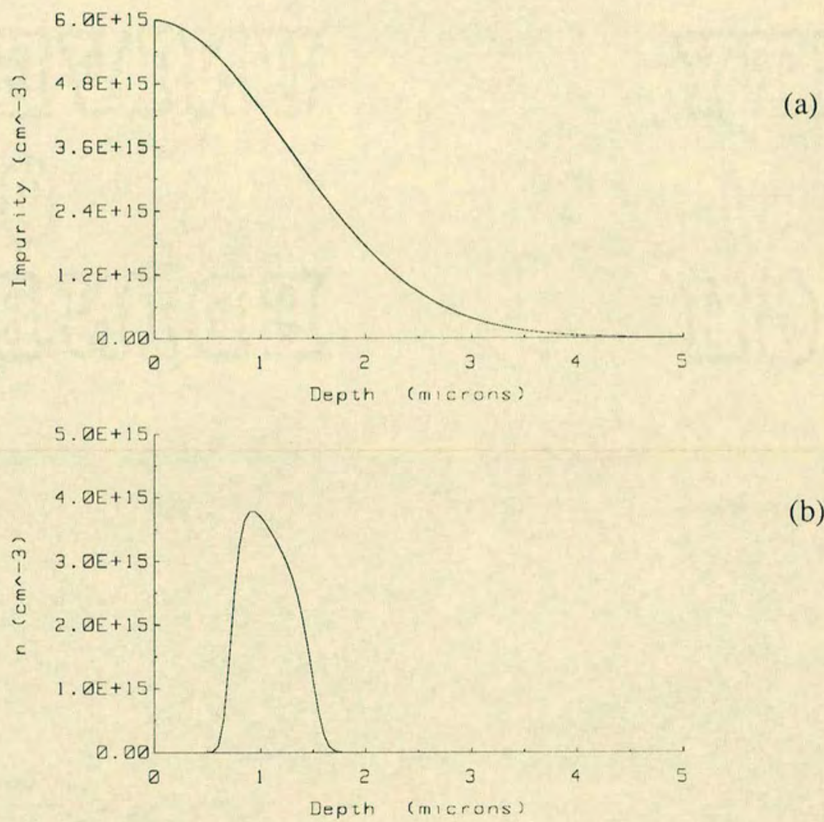
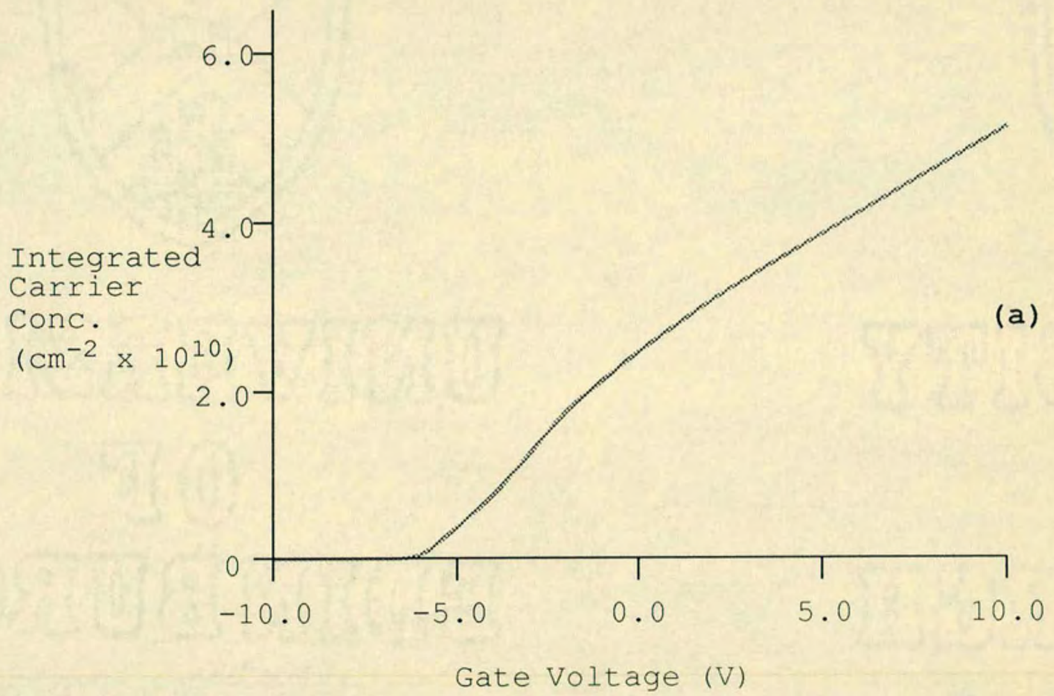



Figure 3.12: Simulation program output for deep depletion mode MOS transistor at room temperature with $V_{GS} = -4\ V$, $V_{BS} = -5\ V$. Plot (a) shows the implanted donor impurity concentration (continuous line) and ionised impurity concentration (dashed line), and (b) shows the free carrier concentration.



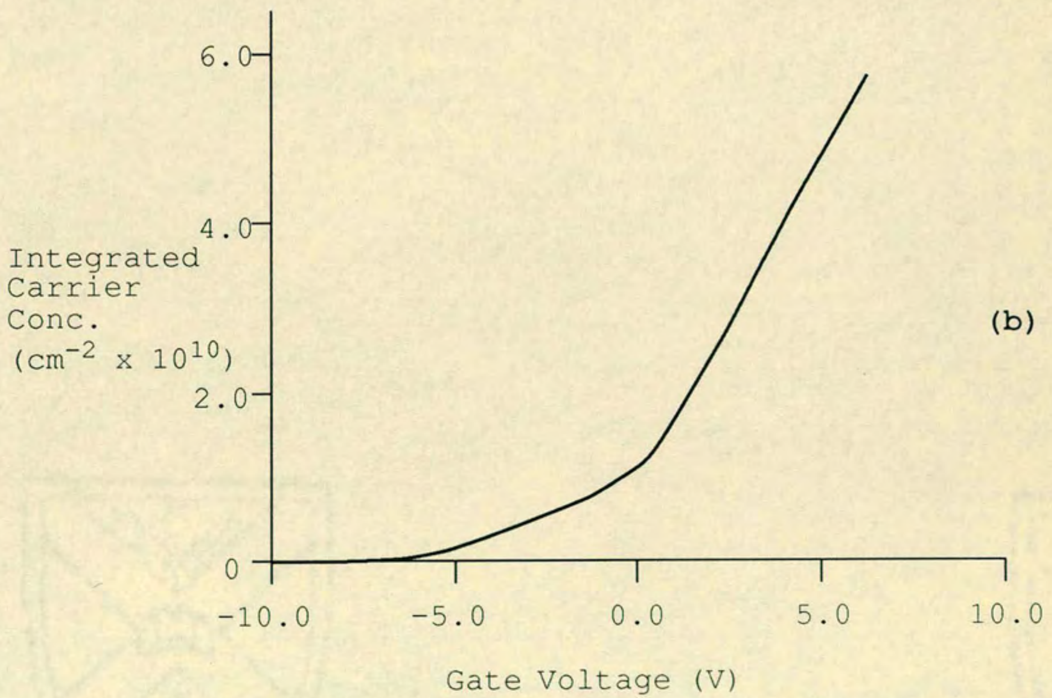




Figure 3.13: Simulated integrated carrier concentration in deep depletion mode MOS transistor at 300 $K$ (a) and 77 $K$ (b).

the program only knows the carrier concentration at specific points on the one dimensional grid. Simpson's method [60] can be used to calculate an approximation to the integrated carrier concentration over the extent of the grid. The integrated carrier concentration could in principle be used to calculate the drain current in the device being simulated. The current density in the channel at a distance $y$ from the source terminal can be given by

$$J_{DS}(y) = e\ \mu_n\ n(x,y) \cdot -\frac{dV}{dy} \tag{3.21}$$

where $e$ is the electronic charge, $\mu_n$ is the carrier mobility. Note that the mobility will depend on the position $(x, y)$ in the channel. If the width of the channel is $W$, then the drain current, $I_{DS}$, can be found from

$$I_D = W \int_0^\infty e\ \mu_n\ n(x,y) \cdot -\frac{dV}{dy} dx. \tag{3.22}$$

Returning to Figure 3.13, (a) shows the simulated integrated carrier concentration at room temperature for gate voltages in the range $-10.0$ to $10.0\ V$. Figure 3.13 (b) shows the integrated carrier concentration at $77\ K$ over the same gate voltage range. The substrate potential in the simulations was set to $-5\ V$. The two graphs show completely different behaviours. At room temperature, Figure 3.13 (a), a characteristic is observed which is analogous to the gate voltage characteristic in an $n$-channel depletion mode MOS transistor. At liquid nitrogen temperature, Figure 3.13 (b), a much 'softer' characteristic is seen with a distinct turning point seen at a gate voltage of around $0\ V$. The difference in the simulated characteristics is similar to that seen in the measured gate voltage characteristics at $300\ K$ and $77\ K$, see Figure 3.2.

Further examination of the simulation output can explain this unusual gate voltage characteristic as follows. At gate voltages greater than $0\ V$ for a

temperature of 77 $K$, the degree of carrier freezout is high. As the gate voltage is reduced, the band bending is such that some of the 'frozen-out' donors near the surface are forced to re-ionise. Their previously trapped charge is swept away by the fiels and into the channel region. As the gate voltage is reduced further, more and more of the donors ionise. Thus, the gate has difficulty in controlling the channel. This is seen in the measurements as a 'flattening' of the characteristic in measurements (*eg* Figure 3.2 (b)) and simulations (Figure 3.13 (b)). The increase in ionisation as the gate voltage is reduced can be seen by comparing Figure 3.9 (a) for $V_{GS} = -1\ V$ with Figure 3.10 (a) for $V_{GS} = -4\ V$.

## 3.8 Concluding Remarks

By means of illustration it has been shown how this simulation program can be a useful tool in the investigation of conduction mechanisms in depletion and deep depletion mode MOS transistors. Using simulations, a qualitative explanation of the unusual distortion in the gate voltage characteristic has been offered. In Chapter 5, simulations will be used to explain the changes in noise performance as deep depletion mode devices are biased such that the channel is made to move away from the interface into the bulk.

# Chapter 4

# Experimental Technique

This chapter details the approach to noise measurements adopted here, and describes the equipment used in these experiments. A number of contrasting experimental techniques are described and justification is given for the chosen strategy. Component modules of the measurement apparatus used to generate the noise spectra presented here are described in detail.

## 4.1 Principles of Noise Measurement

There are two fundamentally different approaches to performing noise measurements. In the first approach, a calibrated noise source is used whose output magnitude can be adjusted to determine the *equivalent* gate input noise, $v_{eq}$, for the transistor under test. Figure 4.1 shows the experimental configuration of this common arrangement. With switch S closed the calibrated noise source is out of circuit and the output noise power of the device under test (DUT) is recorded on the power meter at a 'spot' frequency set by the filter. The bandwidth of this filter is narrow when compared with its centre frequency. Switch S is now opened and the 3 dB attenuator is

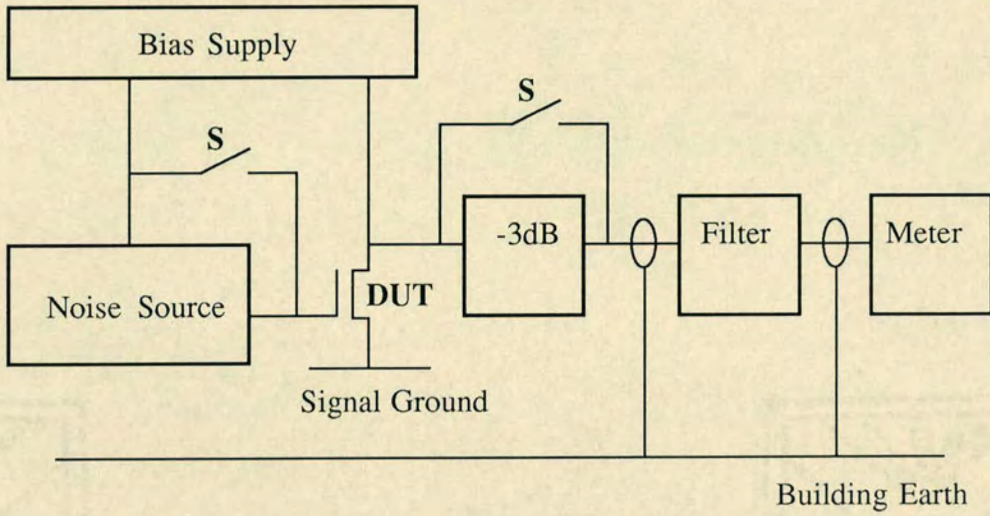



Figure 4.1: Block diagram showing circuit for measuring equivalent gate input noise in an MOS transistor.

introduced between the device under test and the filter. The magnitude of the 'white' noise source is varied until the noise measured at the output returns to its previous level. The magnitude of the calibrated noise source is then a measure of the equivalent gate input noise. The noise source can take the form of a temperature-limited vacuum diode [61] or a pseudo-random sequence generator [62].

The temperature-limited vacuum diode is a shot noise source [63] and can be of simple construction with a pure tungsten filament. The magnitude of the broad-band noise current in the diode is given by

$$i_{n,shot} = \sqrt{2eI} \tag{4.1}$$

where $I$ is the direct current flowing through the diode. A current of 10 $mA$ would give a noise current level of 56.6 $pA/\sqrt{Hz}$. Noise sources of this kind are only useful for frequencies above 1 $kHz$. Below this frequency the noise

spectrum is dominated by flicker noise generated by the thermionic diode. The magnitude of this flicker noise is not well defined. This precludes the use of such valves as calibrated noise source at low frequencies.

A pseudo-random sequence generator can be formed using a shift register with feedback *via* an exclusive OR gate from two outputs of the register [64]. Cox [62] describes the operation of an Automatically Calibrated Universal Measuring Equipment for Noise in Semiconductors (ACUMENS) developed by the Instrumentation and Applied Physics Division at the United Kingdom Atomic Energy Research Establishment. In ACUMENS, the output of three such shift registers of varying lengths is mixed to provide a random signal. The magnitude $v_n$ of the noise at frequency $f$ can be given by [62]

$$v_n = \sqrt{A/2f_o}\frac{\sin(\pi f/f_o)}{\pi f/f_o} \tag{4.2}$$

where $A$ is the amplitude of the step waveform and $f_o$ is the frequency of the pseudo-random sequence generator. If $f_o \gg f$ then Equation (4.2) can be simplified to

$$v_n = \sqrt{A/2f_o}. \tag{4.3}$$

Having measured the equivalent gate input noise voltage, *a priori* knowledge of the transconductance, $g_m$, and the small signal channel conductance, $g_{ds}$, of the device under test can be used to calculate the noise current, $i_n$, in the channel or the noise voltage, $v_n$, across the source and drain. For example, in Figure 4.2, the noise current in the channel, $i_n$, can be found from

$$i_n = g_m v_{eq} \tag{4.4}$$

where $g_m$ is the gain of the (assumed noiseless) MOS transistor, and $v_{eq}$ is the measured equivalent gate input noise voltage.

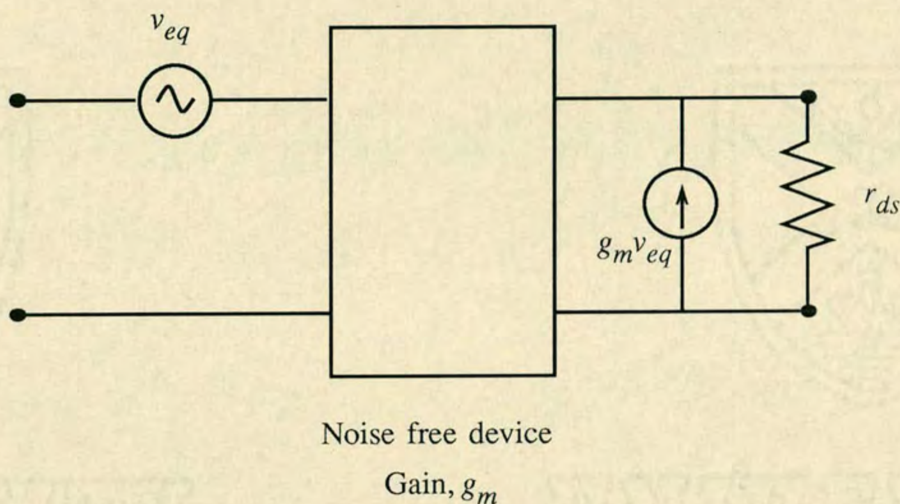



Figure 4.2: Relationship of equivalent gate input noise, $v_{eq}$ to absolute noise current in the channel, $i_n$ in an MOS transistor.

The main advantage in using this strategy to measure noise is that precise knowledge of the effective noise bandwidth of the filters and accurate calibration of the power meter are not prerequisites. However, relating the measured equivalent gate input noise back to mechanisms in the channel requires precise knowledge of the device transconductance, $g_m$. It will be shown in Chapter 5 that the $g_m$ of a MOS transistor is strongly dependent on its operating point. This is particularly true in depletion mode and deep depletion mode MOS transistors. In these structures, a reduction in $g_m$ is observed when the conducting channel is made to move into the bulk through choice of gate and substrate voltages. Under such conditions, there is no longer close coupling between the gate and the charge forming the channel. For a constant absolute noise current in the channel, this leads to an *increase* in equivalent gate noise voltage. Undesirable second order effects

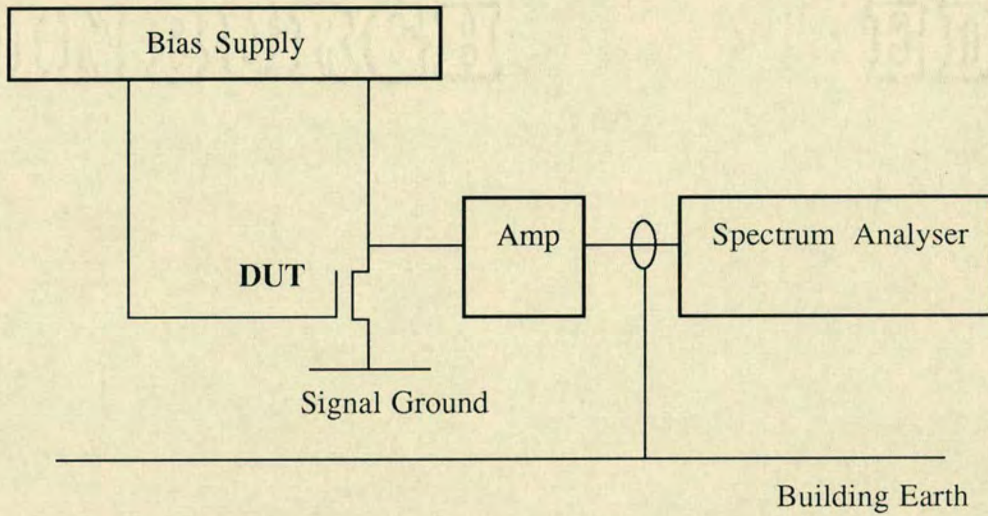



Figure 4.3: Block diagram showing circuit for measuring absolute noise voltage in an MOS transistor.

such as this can be misleading and make meaningful analysis of the results of equivalent gate input noise measurements difficult.

An alternative technique for measuring noise is now discussed. Figure 4.3 illustrates the configuration used. With a knowledge of the precise characteristics of the band-pass filters in the spectrum analyser it is possible to measure directly the noise voltage across the device under test without having to resort to using a calibrated noise source and 3 dB attenuator. A measure of the absolute noise power over a range of frequencies provides more insight into the noise mechanisms in the device under test and offers design engineers a pertinent indication of device noise performance.

The use of a spectrum analyser to perform noise measurements is discussed in [65]. The calibration and performance of the spectrum analyser, including the characteristics of the internal filters, are discussed in detail in

Section 4.5. The following section presents an overview of the noise measuring system used to obtain the results in Chapter 5.

## 4.2 System Overview

This section presents a general description of the noise measuring system used here. The following sections describe the design and calibration of the component parts of the system.

All noise measurements presented here were performed using the facilities in the Electro-Optic Division at Philips Components, Southampton. In addition, some noise results are presented in Appendix B for Philips MOS transistors made on the ACUMENS noise measurement system at AERE Harwell by Dr K. Kandiah.

Figure 4.3 shows a block diagram of the apparatus developed for this research. Bias voltages and currents are delivered to the device under test by a battery bias supply in order to avoid pick-up from the mains voltage. Absolute noise voltage in the device is measured across the source and drain of the transistor. An amplifier of known gain is used to match the magnitude of the noise voltage fluctuations to the input sensitivity of the spectrum analyser. The spectrum analyser comprises 50 band-pass filters in the range 2 $Hz$ to 160 $kHz$ which provides a noise spectrum of sufficient detail. By knowing the gain of the amplifier, the effective bandwidth of each filter and the input sensitivity of the spectrum analyser it is possible to calculate directly the magnitude of the absolute noise voltage across the channel.

In this technique, it is assumed that the source and drain contact resistance is much smaller than $1/g_{ds}$ of the channel. This assumption is

reasonable, since typical values for the contact resistance are in the range of a few tens of ohms, whereas the noise measurements here are generally for $1/g_{ds}$ of several $k\Omega$ to several 10 $k\Omega$.

A number of precautions were necessary to prevent interference and pick-up from external sources, particularly electrically powered equipment elsewhere is the laboratory. The device under test, the battery bias supply and the amplifier were all placed inside a double-layer mu-metal Faraday box, approximately 0.5 m x 0.5 m x 0.5 m. The outer layer was connected directly to the building earth. The inner layer was set to signal ground, at the same potential as the source of the device under test. The amplifier output was connected to the spectrum analyser input *via* a tri-axial cable [66]. This cable had the inner and outer screens connected to the inner and outer layers of the Faraday box respectively. Dominant interference came from the mains electricity supply with radiation detected by the 50 $Hz$, 100 $Hz$ and 160 $Hz$[†] filters. Additionally, the 12.5 $kHz$ filter detected interference from the raster scan on the cathode-ray tube display of the spectrum analyser. In practice, the interference from the spectrum analyser display was always below the thermal noise 'floor' of the device under test. Interference from the mains electricity supply could be reduced to around 70 $nV/\sqrt{Hz}$ by using the Faraday box as described above. At this level, the interference was only important when measuring noise in enhancement mode MOS transistors biased with very low drain currents in the linear region, or in deep depletion mode MOS transistors operated in the buried channel mode. In

[†]There is no filter with a centre frequency of 150 $Hz$ in this system. However, radiation at the third harmonic of mains frequency is detected by the 160 $Hz$ filter which has an effective bandwidth of 37 $Hz$.

the latter case, the noise could be as low as 10 $nV/\sqrt{Hz}$ at 50 $Hz$. However, as we shall see in Section 4.5, the bandwidth of the spectrum analyser filters was small enough to ensure that interference of this kind was only detected by one filter. When performing noise measurements at such low levels the program on the controlling computer effectively removed the interference by averaging the results from the two filters adjacent to the filter detecting the interference.

System calibration was confirmed on a daily basis. The calibration procedure also ensured that electrical interference was at a minimum. The procedure was to replace the device under test with a 1 $k\Omega$ resistor and measure the thermal noise across the terminals. We have seen that the thermal noise across any resistance, $R$, at temperature, $T$, can be given by

$$v_n = \sqrt{4kTRB_n} \tag{4.5}$$

where $k$ is Boltzmann's constant and $B_n$ is the bandwidth of the measuring system. For a 1 $k\Omega$ resistor at 300 $K$, $v_n$ is 4.06 $nV/\sqrt{Hz}$. For MOS devices biased in the linear region the channel is ohmic and Equation 4.5 then becomes

$$v_n = \sqrt{4kT\frac{V_{DS}}{I_{DS}}B_n} \tag{4.6}$$

where $V_{DS}$ is the voltage applied across the source and drain terminals of the device and $I_{DS}$ is the measured drain current. Thus the level of the thermal noise floor for an MOS transistor biased in the linear region provides confirmation of system calibration during the actual measurement of a physical device.

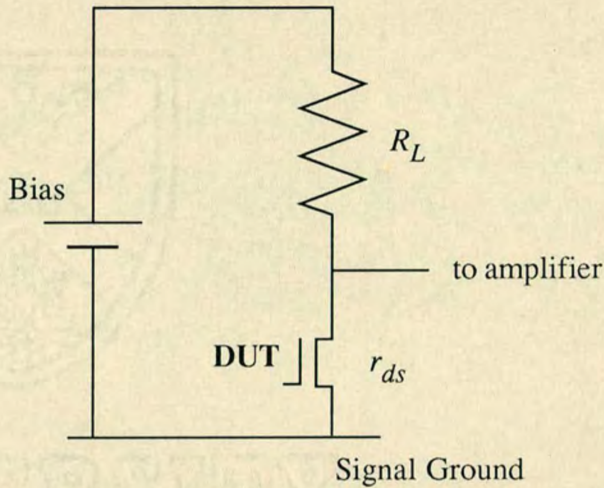



Figure 4.4: Choice of load resistor, $R_L$. For correct measurement of noise in MOS transistor channel, $R_L$ must be chosen so that $R_L \gg r_{ds}$.

## 4.3 Bias Supply - Design Considerations

There were two main considerations when designing the bias supply. Firstly, it should not introduce any additional noise into the system. As will be shown in Section 4.4, the noise floor of the measuring system is dictated by the input noise of the amplifier, at about 0.8 $nV/\sqrt{Hz}$.

Secondly, the output impedance of the bias supply had to be much greater than the small-signal drain to source resistance, $r_{ds}$, of the device under all test conditions. If this condition is not met then any noise voltage developed across the source and drain would be reduced by $R_L$ and the observed noise characteristic would be dominated by the thermal noise voltage in $R_L$. In terms of Figure 4.4, this implies that $R_L \gg r_{ds}$. In addition, the bias supply was required to feed separate substrate and gate voltages of up to $\pm$ 9 $V$ and supply drain currents in the range 0.1 to 500 $\mu A$. In order to minimise

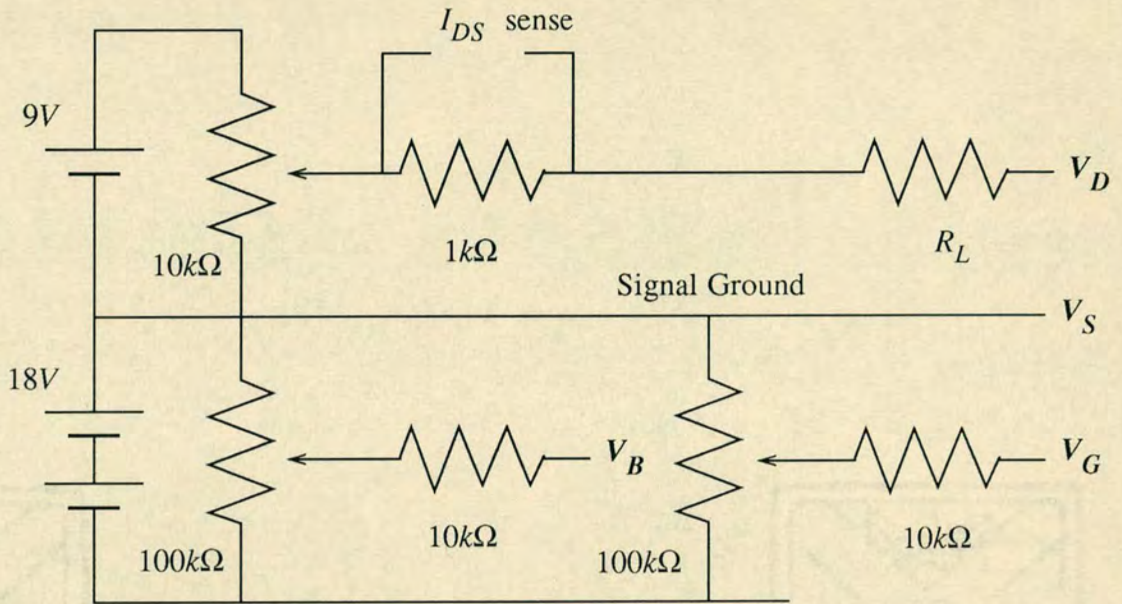



Figure 4.5: Schematic diagram of bias supply. The metal case of the bias supply was connected to signal earth, $V_S$.

the noise contribution from the bias supply it was decided to design a circuit using purely passive components. Figure 4.5 shows a schematic circuit diagram for the bias supply. It comprises three potential dividers, one each for the gate voltage, $V_{GS}$, substrate bias, $V_{BS}$, and drain voltage, $V_{DS}$. All potentiometers are multi-turn wire-wound to give maximum resolution. Potentiometers with composition material tracks were rejected since they were found to introduce excess low frequency noise. The inherent inductance of wire-wound potentiometers was not a problem in the frequency measurement range. The load resistance $R_L$ can be selected from $10k\Omega$, $100k\Omega$, $1M\Omega$ and $10M\Omega$ and must be chosen carefully for each bias point to ensure that $R_L \gg r_{ds}$. The $1k\Omega$ resistor in series with $R_L$ was provided to allow $I_{DS}$ to be measured using a Fluke digital multimeter. Connections were also provided to allow measurement of $V_{DS}$, $V_{GS}$ and $V_{BS}$. The Fluke digital mul-

timeters used were found to be a source of low frequency and broad-band noise. Care was taken to ensure that all such meters were disconnected and isolated from the system during noise measurements.

Several types of battery were considered for use in the bias supply. Lead-acid batteries were rejected after test measurements because of noise at low frequencies when delivering currents greater than around 100 $\mu A$. The origin of this noise may be gas bubbles forming at the plate surfaces within the cell. The rate of hydrogen and oxygen production within the cell increased at higher current values. Nickel-cadmium cells also exhibited low frequency noise, and both nickel-cadmium and alkaline-manganese batteries suffered a gradual drift in voltage over several hours before reaching a pseudo-steady state. Zinc-carbon (Leclanché) cells also had a low frequency noise contribution. However, it was discovered that by momentarily shorting the terminals on a new zinc-carbon cell before use, the magnitude of the low frequency noise could be reduced. The reason for this is not known. (Lithium-manganese batteries and mercury cells were not investigated here). The batteries used for the bias supply in these experiments were Ever Ready zinc-carbon PP9 cells with a nominal voltage of 9 $V$.

## 4.4 Characteristics of Amplifier

Voltage amplification is required to match the magnitude of the noise fluctuations observed across the channel of the device under test with the input sensitivity of the spectrum analyser. The voltage gain of the amplifier required was 60 dB $\pm$ 3 dB over the range 0.5 $Hz$ to 200 $kHz$. A Brookdeal 5004A Ultra-Low Noise Preamplifier was found to be adequate for this pur-

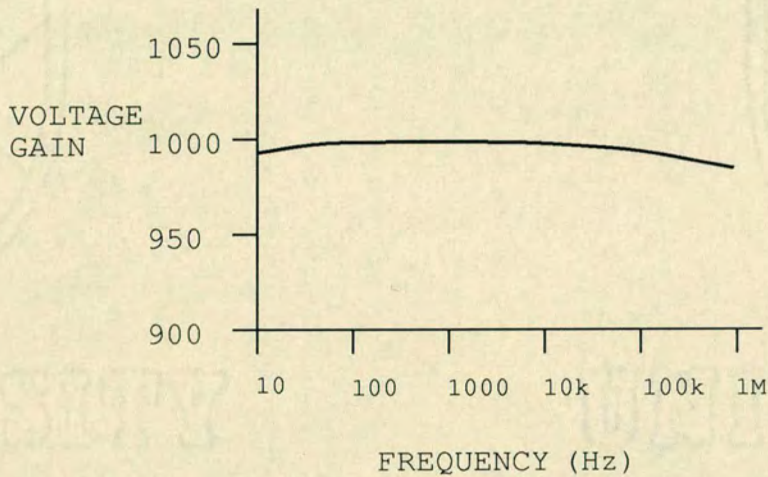



Figure 4.6: Voltage gain of Brookdeal 5004A amplifier over measurement range.

pose. The range of filters offered by the spectrum analyser restricted measurements to frequencies between 2 $Hz$ and 160 $kHz$, and Figure 4.6 shows the voltage gain over this frequency range.

The input stage to this amplifier is a differential circuit with an input impedance of 5 MΩ in parallel with 50 pF. The input stage can be floated to help prevent ground loops. The effective input noise at 1 $kHz$ is 800 $pV/\sqrt{Hz}$, although at 10 $Hz$ this value rises to 4 $nV/\sqrt{Hz}$. These noise levels were generally at least an order of magnitude below the specific value being measured and so presented no problem in the experiments

The amplifier is powered by a Brookdeal 'Powerbin' supply using four 9 V zinc-carbon or nickel-cadmium batteries and is positioned inside the Faraday box along with the device under test and the bias supply.

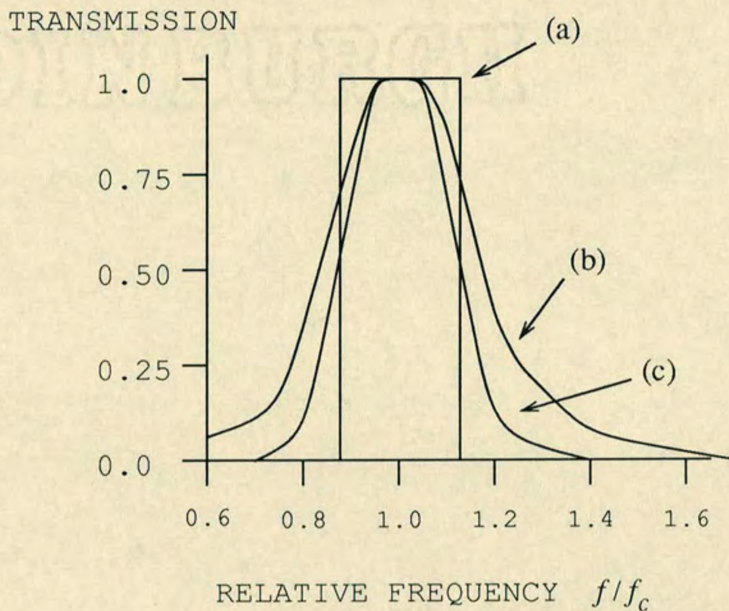



Figure 4.7: Filter responses (a) of ideal filter and (b) practical filter. (c) shows response of practical filter squared.

## 4.5 Spectrum Analyser and Filters

In this section, the performance of the discrete band-pass filters incorporated in the spectrum analyer is described and their use in electrical noise measurements is discussed. The characteristics of the band-pass filters available in the Brüel and Kjær Digital Frequency Analyser (type 2131) is treated below.

An ideal band-pass filter is one which has zero attenuation within its band-pass range and infinite attenuation at all other frequencies. Figure 4.7 compares an ideal filter and a practical filter. There are two definitions of a practical filter in common use. Firstly, the *3 dB bandwidth* is defined by the points at which the power transmission is 3 dB below the maximum transmission level. At these points on the filter characteristic the power

transmission will be halved.

An alternative definition of filter bandwidth is the *effective noise bandwidth.* This is the bandwidth of the ideal filter which would pass the same amount of white noise power as the practical filter. Since power transmission is proportional to the square of the voltage transmission, the practical filter and ideal filter have the same effective noise bandwidth when the area under the ideal filter characteristic is equal to the square of the area under the practical filter, Figures 4.7 (a) and (c).

We now derive an expression for the effective noise bandwidth for filters in the Brüel and Kjær spectrum analyser. Filters are switchable between octave and third octave. Now, an octave is defined as the interval between two frequencies, $f_U$ and $f_L$, having a ratio of two, that is

$$\frac{f_U}{f_L} = 2. \tag{4.7}$$

Third octaves are defined by the ratio of frequencies

$$\begin{aligned} \frac{f_U}{f_L} &= 2^{\frac{1}{3}} \\ &\approx 1.26. \end{aligned} \tag{4.8}$$

Now, the bandwidth of the filter is given by

$$B = f_U - f_L \tag{4.9}$$

and the centre (or pass) frequency of the filter is given by

$$f_C = \sqrt{f_U f_L}. \tag{4.10}$$

It follows that

$$B = K f_C \tag{4.11}$$

where $K$ is a constant depending on the ratio of $f_U/f_L$. For third-octave filters,

$$K = 2^{\frac{1}{6}} - 2^{-\frac{1}{6}} \qquad (4.12)$$

$$\approx 0.232.$$

Table 4.1 shows the fifty filter centre frequencies and their respective bandwidths as given by Equation 4.11. These centre frequencies are those recommended by the International Electrotechnical Commission (IEC) [67]. In this document each filter centre frequency is calculated relative to 1000 $Hz$ with individual frequencies given by

$$f_C = 1000 \times 10^{\frac{n}{10}} \qquad (4.13)$$

for third octave filters where n = 0, ± 1, ± 2, *etc.* Filters in the range 2 $Hz$ to 200 $Hz$ in this equipment are all active circuits comprising three stagger-tuned Wien-bridge amplifiers. Higher frequency third-octave filters are all passive networks.

Now, the relative accuracy of a single noise reading using an instrument of averaging time $\tau$ and noise bandwidth $B_n$ is given by [22]

$$\frac{\Delta v_n}{v_n} = \frac{1}{2B_n\tau}. \qquad (4.14)$$

Note that the relative accuracy is not a function of the filter centre frequency as might be expected, but merely dependent on the effective noise bandwidth of the filter.

Averaging times, $\tau$, for each measurement could be selected on the spectrum analyser. Available averaging times were $T$ seconds where $T$ is some power of two up to 128 $s$. The averaging time used for noise results presented

| Centre Frequency ($Hz$) | Effective Bandwidth ($Hz$) | Root Bandwidth ($\sqrt{Hz}$) | Centre Frequency ($Hz$) | Effective Bandwidth ($Hz$) | Root Bandwidth ($\sqrt{Hz}$) |
|---|---|---|---|---|---|
| 2 | 0.46 | 0.68 | 630 | 145 | 12.0 |
| 2.5 | 0.58 | 0.76 | 800 | 183 | 13.5 |
| 3.15 | 0.73 | 0.85 | 1000 | 230 | 15.2 |
| 4 | 0.92 | 0.96 | 1250 | 290 | 17.0 |
| 5 | 1.16 | 1.08 | 1600 | 370 | 19.2 |
| 6.3 | 1.45 | 1.20 | 2000 | 460 | 21.5 |
| 8 | 1.83 | 1.35 | 2500 | 580 | 24.1 |
| 10 | 2.30 | 1.52 | 3150 | 730 | 27.0 |
| 12.5 | 2.90 | 1.70 | 4000 | 920 | 30.3 |
| 16 | 3.70 | 1.92 | 5000 | 1160 | 34.1 |
| 20 | 4.60 | 2.14 | 6300 | 1450 | 38.1 |
| 25 | 5.8 | 2.41 | 8000 | 1830 | 42.8 |
| 31.5 | 7.3 | 2.70 | 10000 | 2300 | 48.0 |
| 40 | 9.2 | 3.03 | 12500 | 2900 | 53.9 |
| 50 | 11.6 | 3.41 | 16000 | 3700 | 60.8 |
| 63 | 14.5 | 3.81 | 20000 | 4600 | 67.8 |
| 80 | 18.3 | 4.28 | 25000 | 5800 | 76.2 |
| 100 | 23 | 4.80 | 31500 | 7300 | 85.4 |
| 125 | 29 | 5.39 | 40000 | 9200 | 96.0 |
| 160 | 37 | 6.08 | 50000 | 11600 | 108 |
| 200 | 46 | 6.78 | 63000 | 14500 | 120 |
| 250 | 58 | 7.62 | 80000 | 18300 | 135 |
| 315 | 73 | 8.54 | 100000 | 23000 | 152 |
| 400 | 92 | 9.59 | 125000 | 29000 | 170 |
| 500 | 116 | 10.8 | 160000 | 37000 | 192 |

Table 4.1: Spectrum analyser centre frequencies and bandwidths

| Centre Frequency ($Hz$) | Effective Bandwidth ($Hz$) | Relative Accuracy (%) |
|---|---|---|
| 2 | 0.46 | 13.0 |
| 10 | 2.30 | 5.8 |
| 100 | 23 | 1.8 |

Table 4.2: Relative accuracy at a number of frequencies for an averaging time of 64 s.

here was $\tau = 64\ s$. Table 4.2 shows the relative accuracy at a number of frequencies at the lower end of the spectrum for this averaging time. This was found sufficient to provide adequate resolution and reproducibility at frequencies down to 2 $Hz$. Increasing the averaging time to 128 $s$ (the maximum offered by the spectrum analyser) improved the accuracy to 9.2 % at 2 $Hz$. However, spot noise values quoted here are at 10 $Hz$ and it was felt that the benefits of increasing the averaging time to 128 $s$ were minimal.

A Hewlett-Packard 9836 Series 200 desk-top computer was used to control the noise measuring system. An HP BASIC [68] program was written to analyse results, present these results graphically and store the data on disc for future analysis. HP BASIC is a fast semi-compiled language with emphasis on hardware interfacing and as such is ideal for such control and instrumentation applications. For each noise spectrum, the computer read in 50 real numbers into an array. These numbers corresponded to the noise level in dB relative to 1 $\mu V$ detected by each of the 50 filters in the spectrum analyser over the selected averaging time. From these values, the absolute

noise voltage, $v_n$, in $V/\sqrt{Hz}$ could be calculated using

$$v_n = A\frac{10^{\frac{N_{dB_n}}{20}-6}}{B_{w_n}} \tag{4.15}$$

where $N_{dB_n}$ is the noise for filter $n$ in dB relative to 1 $\mu$V, $B_{w_n}$ is the bandwidth of filter $n$ and $A$ is the the voltage gain of the amplifier. This calculation enabled a direct plot of absolute noise voltage against frequency to be displayed.

## 4.6 Measurement of d.c. Characteristics

In addition to noise measurements made on the apparatus described in the preceding sections, d.c. characteristics of the MOS transistors were obtained using a Hewlett-Packard 4145 Semiconductor Parameter Analyser [69]. Specifically, values of the device transconductance, $g_m$, and forward conductance, $g_{ds}$, were required in order to establish the suitability of these devices as circuit elements.

The 4145 parameter analyser was configured to have four independent channels, each one capable of forcing a specified voltage and measuring the current in that channel. One channel was assigned to each of the source, drain, gate and substrate on the device under test.

Device d.c. characteristics measured by the 4145 were read *via* the HP-IB connection into a desk-top microcomputer. The data was stored on disc and could be used subsequently to obtain parameters such as device transconductance at particular bias points used in the noise measurements.

## 4.7 Conclusions

In this chapter we have described in detail the measurement systems used for characterising device noise behaviour. We have described the design of the noise measurement apparatus and shown how this could be used to measure the absolute noise voltage across the source and drain terminals of a MOS transistor. A brief description of the Hewlett-Packard 4145 Semiconductor Parameter Analyser was given. In the following chapter we use measurements made on the apparatus described above to investigate the noise performance of a wide range of MOS transistor structures.

# Chapter 5

# Experimental Results

This chapter presents experimental results showing noise behaviour of the MOS transistor structures described in Chapter 2. It is shown that by careful choice of bias point extremely low noise operation is possible in deep depletion mode MOS transistors while maintaining acceptable circuit parameters. Simulations are used to explain the improved noise performance by considering the spatial distribution of charge forming the channel. This mode of low noise operation is a key finding in this research.

## 5.1 Introduction

The experiments yielding the noise results presented here were all performed using the apparatus described in Chapter 4. Appendix A presents results for conventional enhancement mode and depletion mode $n$-channel MOS transistors. A number of additional results which were obtained by K. Kandiah on his own measuring equipment [70] are given to support the results and conclusions of this research. These results are shown in Appendix B.

## 5.2 Low Frequency Noise in Deep Depletion Mode MOS Transistors

This section presents detailed noise results for deep depletion mode structures. It is found that simulations can be used to explain the measured reduction in low frequency noise.

### 5.2.1 Noise Results

The noise performance of the deep depletion MOS transistors described in Chapter 1 is now described. In Section 2.1.2, it was observed that two types of deep depletion MOS transistor were designed and fabricated for these experiments. The deep phosphorus well was identical in both cases, but the second type had an additional arsenic implant near the silicon-silicon dioxide interface. The arsenic implant is normally used in CCD applications where a high charge carrying capacity is required. This increased charge carrying capacity will be shown in simulations later in this section.

For all operating conditions the devices with the additional arsenic implant were found to have an inferior noise performance. Figure 5.1 shows a typical comparison between a deep depletion MOS transistor with the arsenic implant (A) and an identical structure without such an implant (B). Drain voltage, drain current, substrate bias, and design geometry were identical for each measurement. The gate voltage for (A) was more negative since the transistor with the additional donor implant naturally had a lower threshold voltage. The noise in the MOS transistor with the implant is around 1.5 times higher throughout the frequency measurement range. The increase in thermal noise floor can be explained by considering the increase in $1/g_{ds}$

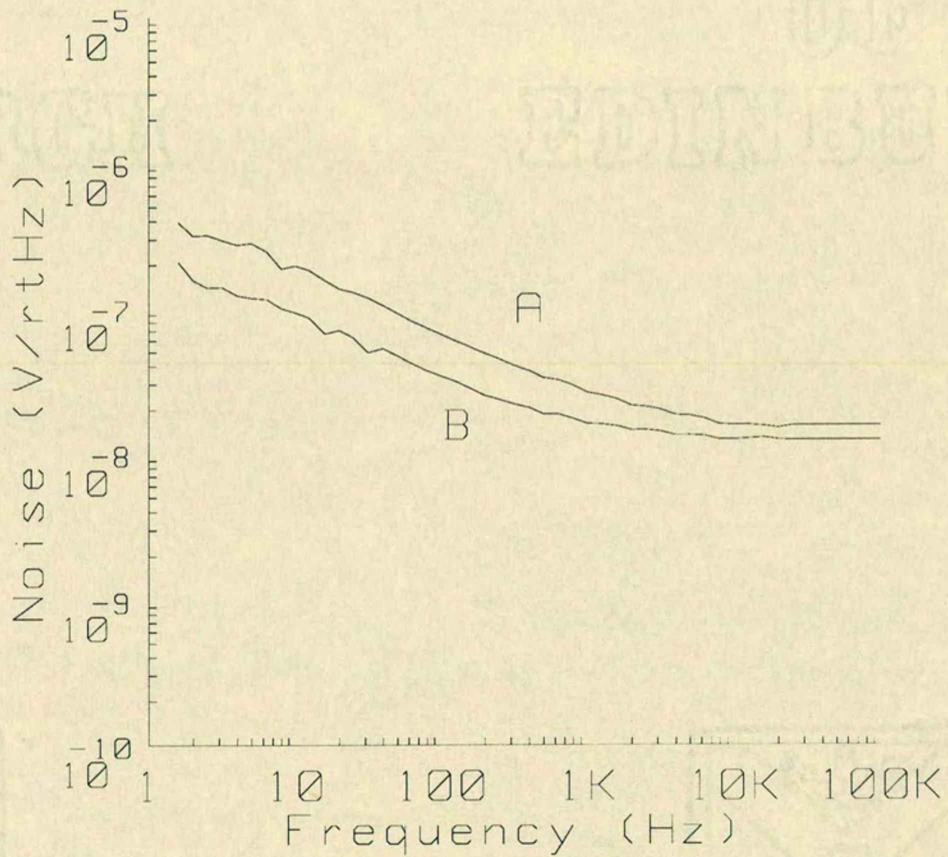



Figure 5.1: Noise spectra for shallow depletion (A) and deep depletion (B) MOS transistors. $I_{DS} = 24.0\ \mu A, V_{DS} = 0.1\ V$.

for the device in Figure 5.1 (A). The measured $1/g_{ds}$ is 13.8 $k\Omega$ without the implant, and 26.4 $k\Omega$ with the implant, giving a theoretical increase in thermal noise from 15.1 $nV/\sqrt{Hz}$ to 20.9 $nV/\sqrt{Hz}$. This corresponds with the measured increase seen in Figure 5.1.

The increase in low frequency noise could be due to a number of factors. One possibility is that the arsenic implant introduces bulk defects resulting in additional trapping in the bulk and an increase in low frequency noise. However, in Appendix A it will be shown that any damage caused by the *boron* implant in the case of enhancement mode transistors could be annealed out. Another possibility is that the increase in noise was due to the fact that the charge distribution in the device with additional donors has a greater proportion of the carriers closer to the interface. This is confirmed in the output of simulations for the two types of deep depletion mode transistor shown in Figure 5.2. It can be seen that the simulation of the shallow depletion mode transistor in Figure 5.2 (b) shows a much greater proportion of the charge adjacent to the silicon-silicon dioxide interface. Further experimental work would be required to establish the cause of this increased noise. Results presented in the rest of this section are all for deep depletion devices *without* the arsenic implant.

We begin by taking a detailed look at the noise behaviour in these deep depletion MOS transistors as the channel is moved spatially in the bulk. It is shown that by careful choice of bias conditions it is possible to achieve extremely low output noise in these devices.

Figure 5.3 shows the noise spectra for a saturated $100 \times 15$ $\mu m$ gate area deep depletion device under three different gate voltages, $V_{GS}$, and substrate bias points, $V_{BS}$, at room temperature. Drain voltage and current were kept

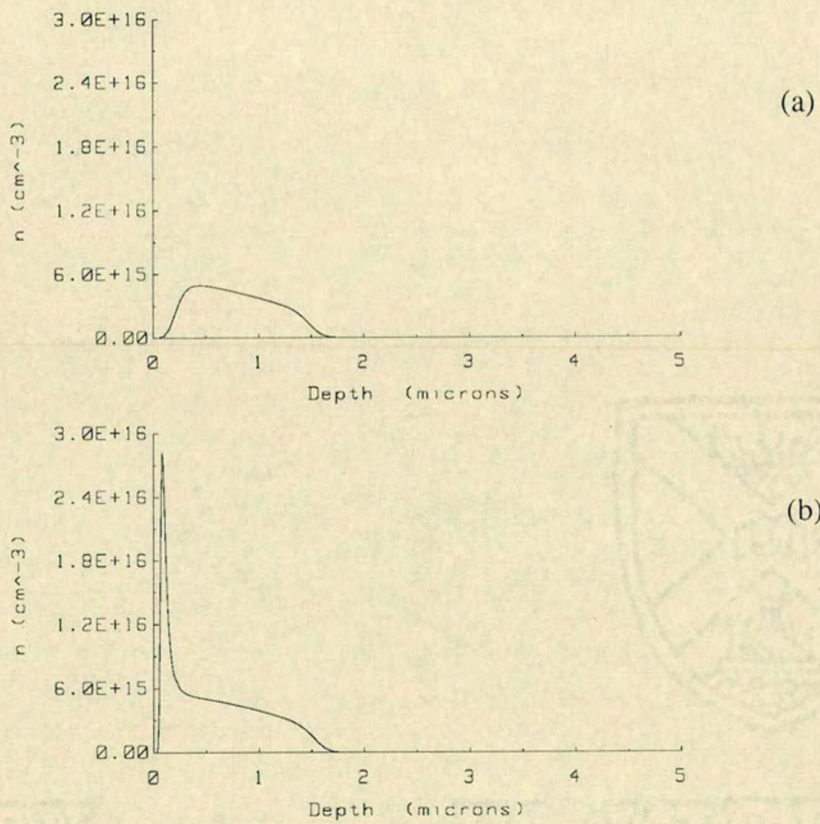



Figure 5.2: Simulations showing charge distribution in (a) deep depletion and (b) shallow depletion mode MOS transistors.

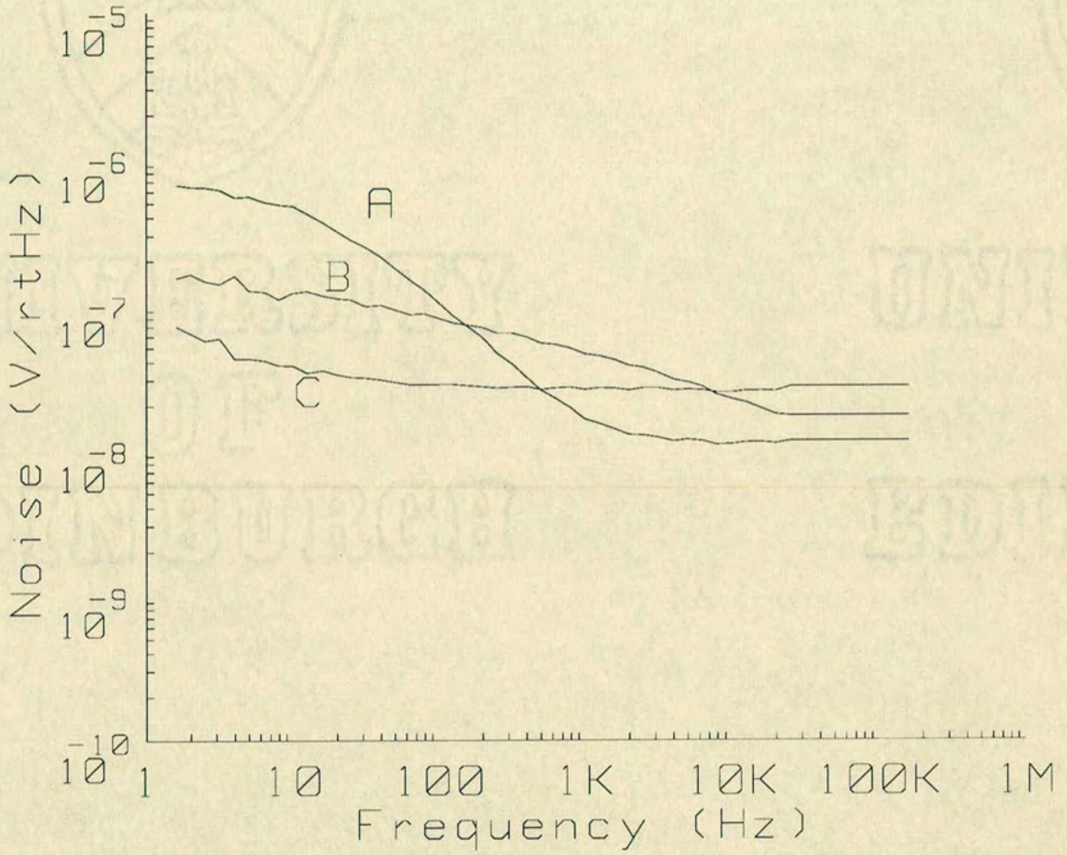



Figure 5.3: Noise spectra for deep depletion mode MOS transistor under three bias conditions. $V_{DS} = 0.50\ V$ , $I_{DS} = 96.7\ \mu A$.

| | | |
|---|---|---|
| (A) | $V_{GS} = -2.00\ V$ | $V_{BS} = -2.00\ V$ |
| (B) | $V_{GS} = -2.49\ V$ | $V_{BS} = -0.45\ V$ |
| (C) | $V_{GS} = -2.70\ V$ | $V_{BS} = -0.30\ V$ |

constant.

It can be seen that as $V_{GS}$ was made more negative, and $V_{BS}$ made more positive to maintain the drain current, the characteristics of the noise change considerably. Figure 5.3 (A) is typical of the observed spectrum over a wide range of $V_{GS}$ and $V_{BS}$ values. The characteristic is dominated by a time constant of around 100 $ms$ giving a plateau below 10 $Hz$ and a sharp roll-off above this frequency. At frequencies above 5 $kHz$ the 'white' thermal noise floor is observed.

Let us first consider what is happening at low frequencies. At frequencies below 100 $Hz$ a substantial reduction in noise is observed as the gate voltage is reduced. Indeed, a 700 $mV$ shift in $V_{GS}$ gives us an order of magnitude reduction in noise at 10 $Hz$. It will be shown that this improvement is due to the conducting channel being pushed away from the high density of traps near the interface. At still more negative gate voltages, a flat noise spectrum is seen with very little structure at lower frequencies, Figure 5.3 (C). The noise levels in Figure 5.3 (C) are considerably lower than those presented for enhancement mose transistors earlier in this chapter.

At high frequencies, above 1 $kHz$, an increase in noise is seen. There are two mechanisms contributing to this noise floor. Analysis of the d.c. characteristics has shown that the device tends to move further into saturation when the channel moves into the bulk. However, the increase in $1/g_{ds}$ is not sufficient to explain the observed increase in white noise. It is thought that there is a small shot noise contribution when the device is in the saturation region, probably arising at the drain end of the channel through carrier injection into the associated depletion regions. Now,

$$v_{n,shot} = \frac{1}{g_{ds}} i_{n,shot}$$

$$= \frac{1}{g_{ds}}\sqrt{2\, e\, I_{DS}\, \Delta f} \tag{5.1}$$

if full shot noise is experienced. For plot C in Figure 5.3, $I_{DS} = 96.7\ \mu A$ and $g_{ds} = 145.6\ \mu A/V$ giving a full shot equivalent noise voltage of $v_{n,shot} = 38.2\ nV/\sqrt{Hz}$. Similarly, it can be shown that the thermal noise for this operating point is $v_{n,thermal} = 10.64\ nV/\sqrt{Hz}$. The observed floor is in fact around 24 $nV/\sqrt{Hz}$, which is lower than the value predicted by Equation 5.1 indicating that there is not a full shot noise contribution in this case. A shot noise contribution of this kind was not seen in any measurements of enhancement mode MOS transistors, see Appendix A.

Similar noise characteristics to those described above have been seen in deep depletion mode MOS transistors biased further into the saturation region, Figure 5.4, and in the linear region, Figure 5.5. In both cases the overall characteristic shape is similar to that of Figure 5.3. However, in Figure 5.5 where the MOS transistor is biased in the linear region, there appears to be no shot noise contribution since the white noise floor is constant for all three bias points. This provides confirmation that device saturation is indeed a necessary condition for there to be a shot noise current contribution.

The measurements in Figures 5.3, 5.4, and 5.5 were all made on devices taken from the same silicon wafer. To confirm that the measured reduction was real and reproducible, similar measurements were performed on devices taken from separate wafers in the same process batch, and on devices from a completely different batch. Some of these measurements are now presented. Figure 5.6 shows a device taken from a separate wafer in the same batch. The bias was made as close as possible to that used for the spectra in Figure 5.3 but the threshold voltage was found to be slightly different resulting in a

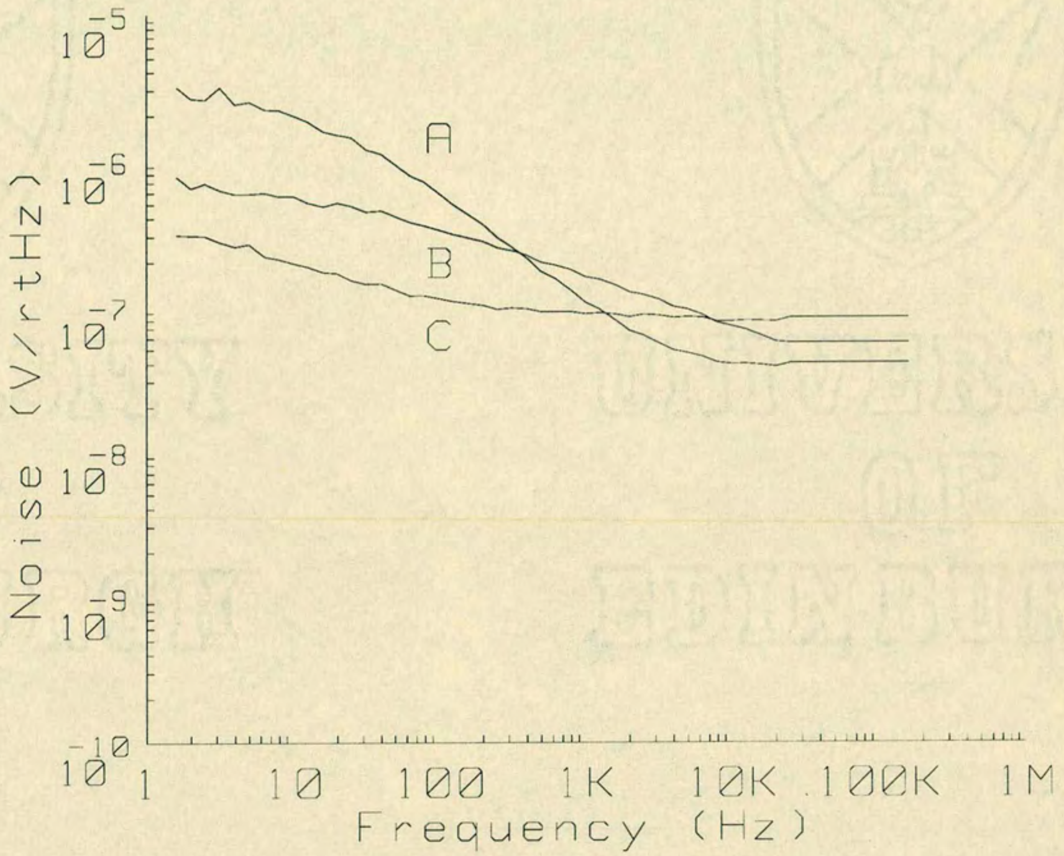



Figure 5.4: Noise spectra for deep depletion mode MOS transistor under three bias conditions in saturation. $V_{DS} = 0.75\ V$ , $I_{DS} = 96.8\ \mu A$.

| (A) | $V_{GS} = -1.16\ V$ | $V_{BS} = -9.50\ V$ |
|---|---|---|
| (B) | $V_{GS} = -2.82\ V$ | $V_{BS} = -0.65\ V$ |
| (C) | $V_{GS} = -2.90\ V$ | $V_{BS} = -0.55\ V$ |

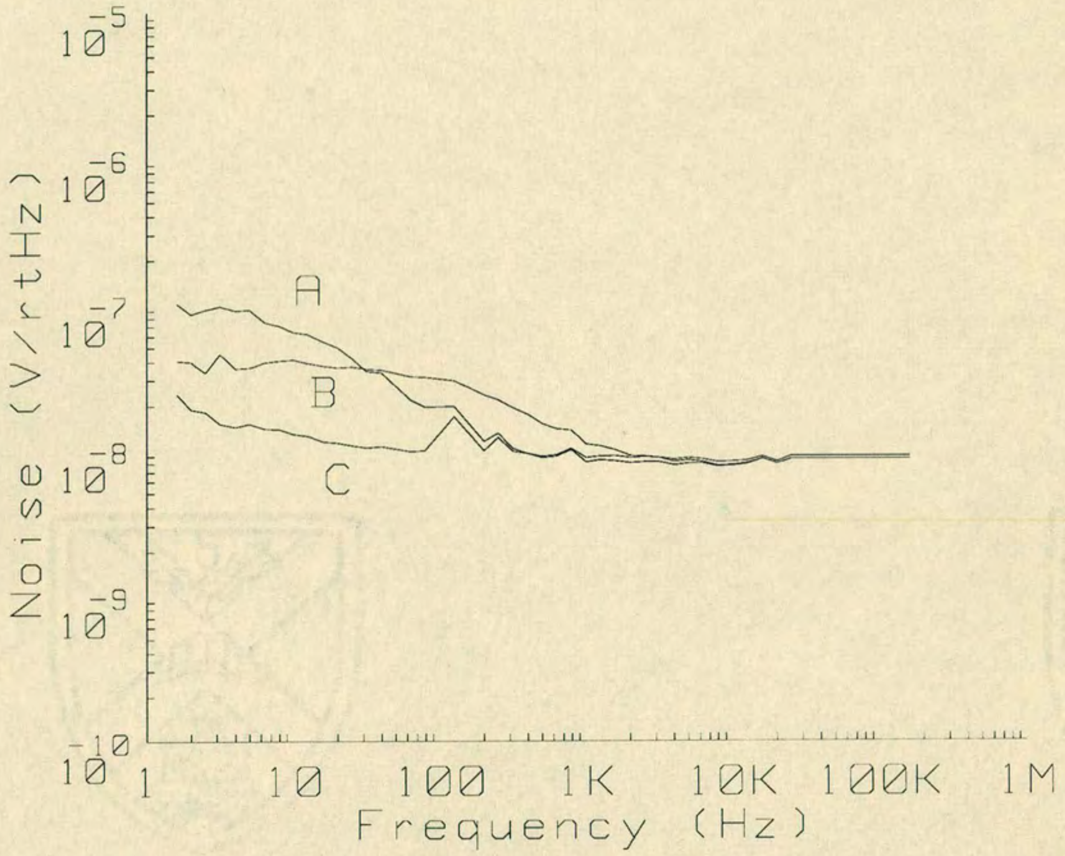



Figure 5.5: Noise spectra for deep depletion mode MOS transistor under three bias conditions in the linear region. $V_{DS} = 0.05\ V$ , $I_{DS} = 11.5\ \mu A$.

| | | |
|---|---|---|
| (A) | $V_{GS} = -2.39\ V$ | $V_{BS} = -0.70\ V$ |
| (B) | $V_{GS} = -2.45\ V$ | $V_{BS} = -0.55\ V$ |
| (C) | $V_{GS} = -2.51\ V$ | $V_{BS} = -0.45\ V$ |

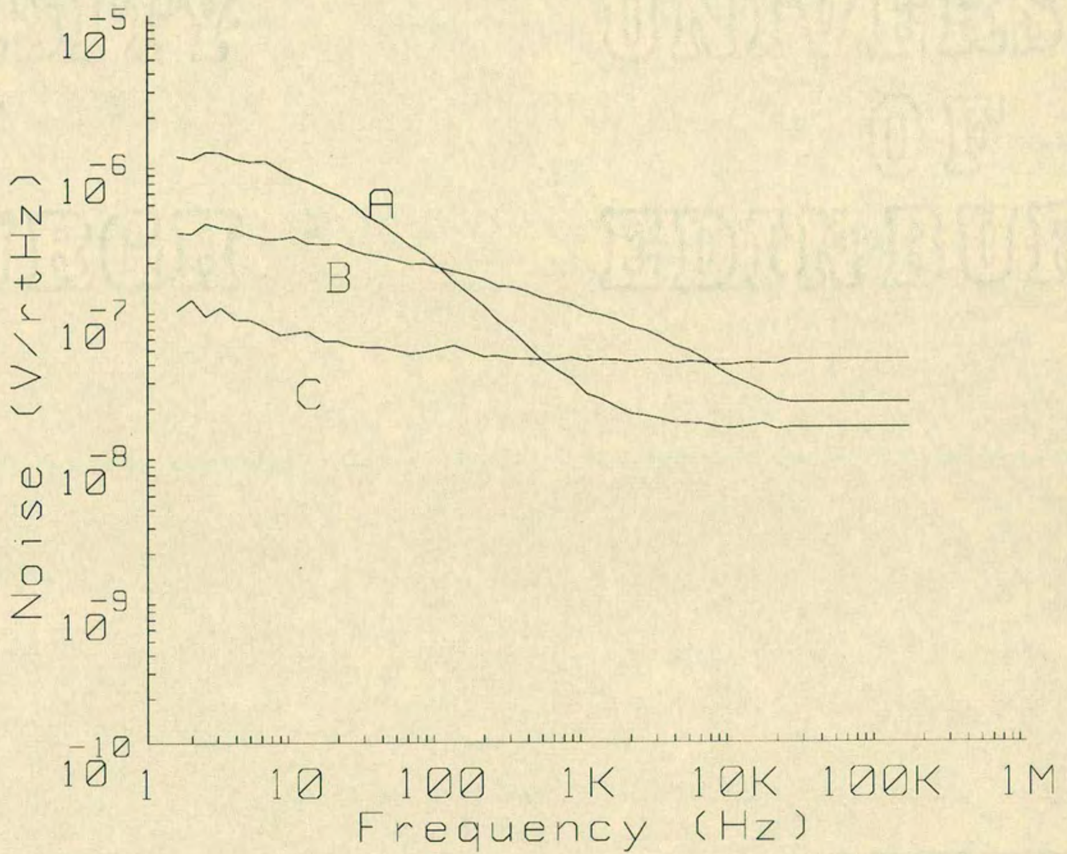



Figure 5.6: Noise spectra for deep depletion mode MOS transistor under three bias conditions. $V_{DS} = 0.50\ V$ , $I_{DS} = 101.9\ \mu A$.

| (A) | $V_{GS} = -2.00\ V$ | $V_{BS} = -2.00\ V$ |
|---|---|---|
| (B) | $V_{GS} = -2.52\ V$ | $V_{BS} = -0.45\ V$ |
| (C) | $V_{GS} = -2.67\ V$ | $V_{BS} = -0.30\ V$ |

marginally higher drain current for similar gate voltage and substrate bias. Figure 5.7 shows similar data for a device taken from a wafer on a separate run. In conclusion, the measured reduction in noise is real and can be reproduced from batch to batch.

Before we use computer simulations to explain these observed changes in noise characteristics, the variations of the transconductance, $g_m$, with the required gate voltage and substrate potentials to reduce the low frequency noise are presented. Figure 5.8 (A) shows device transconductance as a function of gate voltage, and Figure 5.8 (B) shows spot noise measurements made at 10 $Hz$ as a function of gate voltage. The data in Figure 5.8 (B) is taken from the same measurement set as the plots in Figure 5.3 A reduction in $g_m$ is observed when the channel moves into the bulk since the gate effectively loses some control of the charge forming the channel. Comparing Figures 5.8 (A) and (B), it can be seen that the device noise falls off before the $g_m$ is reduced. This means that low noise operation with high gain is possible if the gate voltage is arranged to be around $-2.5$ $V$ for this device. This would provide a transconductance, $g_m$, of around 50 $\mu A/V$ with an output noise voltage of less than 70 $nV/\sqrt{Hz}$. A similar effect is seen when the device is biased further into saturation, Figure 5.9. With a gate voltage of $-2.9$ $V$ in this instance a $g_m$ of around 50 $\mu A/V$ is possible with a noise voltage at 10 $Hz$ of approximately 200 $nV/\sqrt{Hz}$.

One problem is that this 'window of opportunity' is rather small, and does depend on the process run and particular drain bias conditions. For example, the optimal gate voltage moved from $-2.5$ $V$ to $-2.9$ $V$ when the drain voltage was moved from 0.50 $V$ in Figure 5.8, to 0.75 $V$ in Figure 5.9. This may mean that each application circuit would require the exact oper-

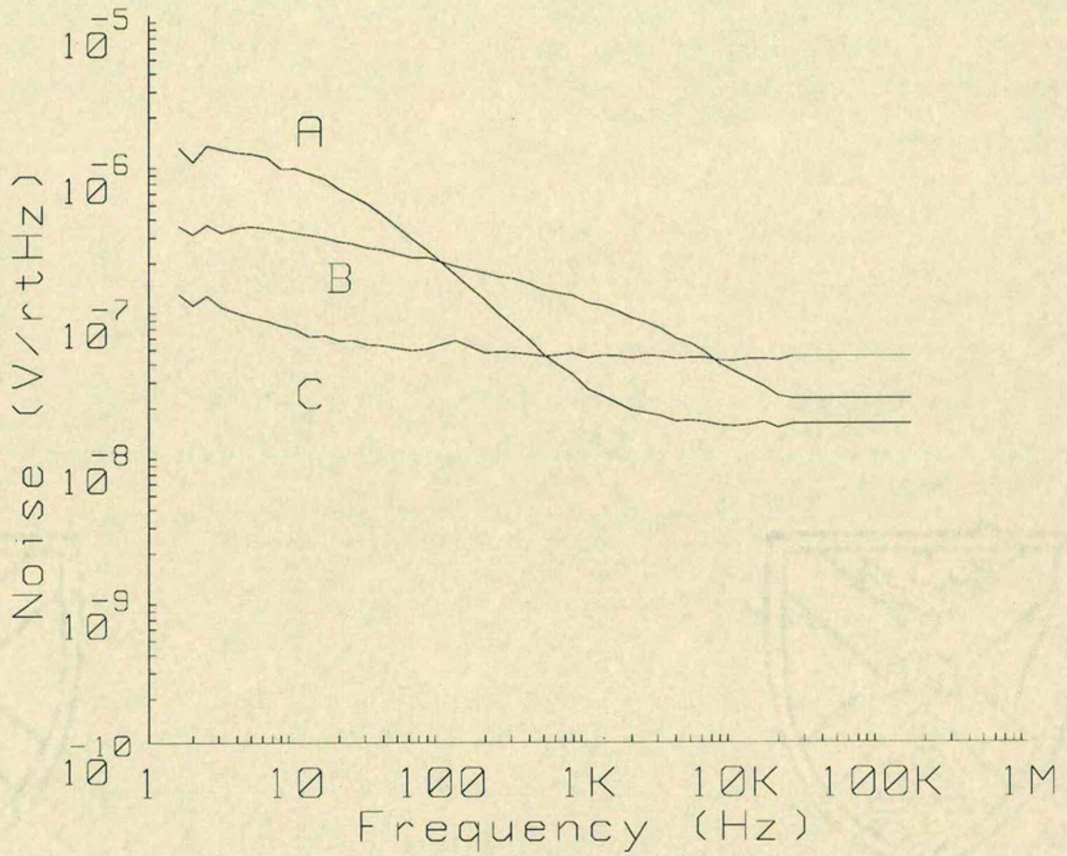



Figure 5.7: Noise spectra for deep depletion mode MOS transistor under three bias conditions. $V_{DS} = 0.50\ V$ , $I_{DS} = 96.4\ \mu A$.

| (A) | $V_{GS} = -1.98\ V$ | $V_{BS} = -2.00\ V$ |
|---|---|---|
| (B) | $V_{GS} = -2.50\ V$ | $V_{BS} = -0.45\ V$ |
| (C) | $V_{GS} = -2.67\ V$ | $V_{BS} = -0.30\ V$ |

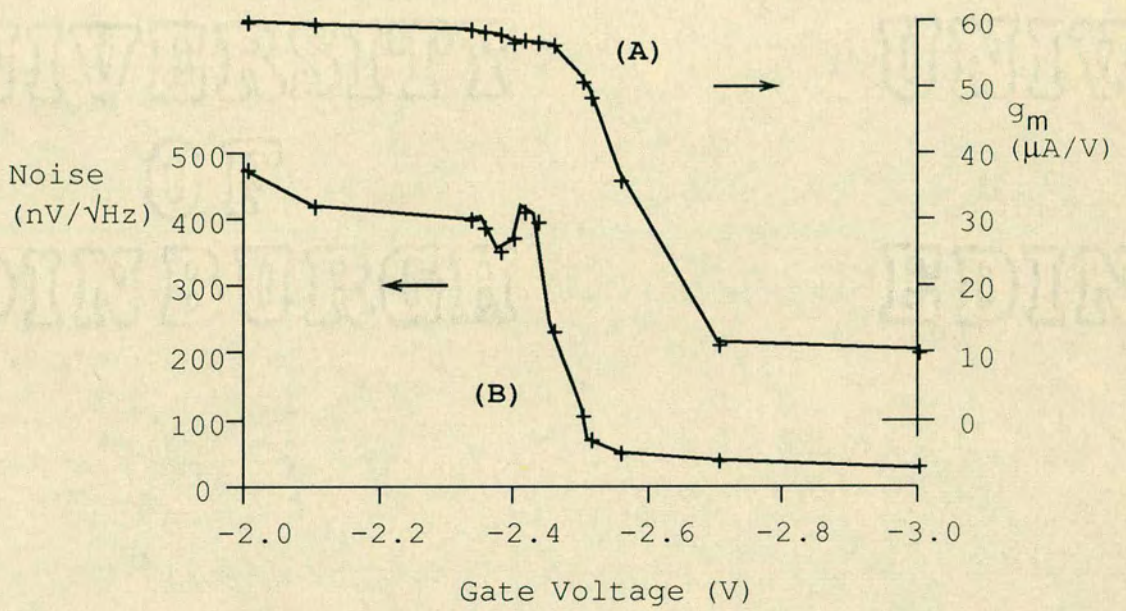



Figure 5.8: Dependence on gate voltage of (A) device transconductance and (B) noise voltage at 10 $Hz$ for deep depletion mode MOS transistor in saturation mode. $V_{DS} = 0.50\ V$ , $I_{DS} = 96.7\ \mu A$.

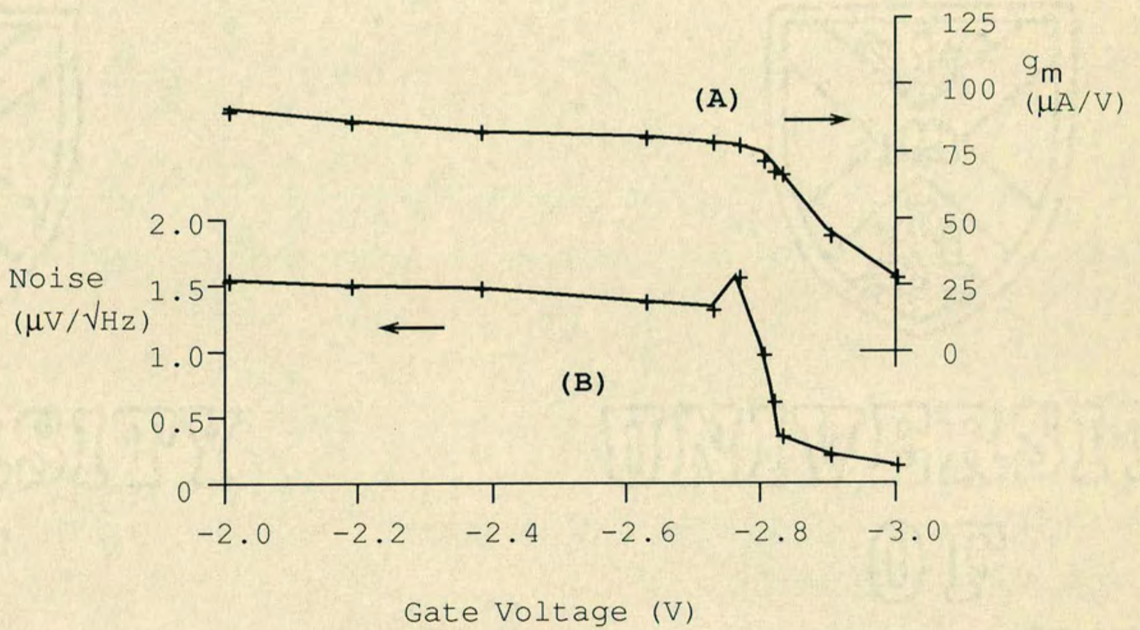



Figure 5.9: Device transconductance (A) and noise voltage at 10 $Hz$ (B) dependence on gate voltage in deep depletion mode MOS transistor, saturation mode. $V_{DS} = 0.75\ V$ , $I_{DS} = 96.8\ \mu A$.

ating point to be adjusted for optimal noise performance with acceptable gain.

The noise peak maxima in Figure 5.8 (B) and Figure 5.9 (B) are real. Just before the noise voltage at low frequencies is reduced as the gate voltage is made more negative, we see a maximum in the form of a Lorentzian type distribution sweeping up the frequency domain. The time constant of the distribution is a very strong function of gate voltage resulting in a sharp peak when we examine the noise magnitude at one particular frequency as a function of gate voltage. The Lorentzian distribution shift can be seen in Figures 5.3, 5.4, 5.5, 5.6 and 5.7. It is particularly evident in Figure 5.5. A similar shift in a Lorentzian distribution as a function of gate voltage has been measured by Hayat and Jones [71]. They attribute the Lorentzian distribution to a generation-recombination process *via* mid-gap surface states. These states are most active and make the greatest contribution to the flicker noise when the Fermi level is close to their energy level.

Watanabe's results show a similar peak at a particular gate voltage as the gate attempts to turn off the channel [72]

### 5.2.2 Simulation of carrier distribution

The simulation program, described in Chapter 3, can be used to confirm that the observed reduction in noise in deep depletion mode MOS transistors is indeed caused by the channel charge leaving the proximity of the silicon-silicon dioxide interface. It was observed in Chapter 3 that the simulation program uses a one dimensional model and as such can only be used to simulate geometry independent effects, or devices biased in the linear region. In Figure 5.5 it was shown that the improvement in noise performance has

been seen in deep depletion mode MOS transistors biased in the linear region. Figure 5.10 shows two noise spectra for a deep depletion MOS transistor with constant drain voltage and drain current. The gate voltage and substrate bias in (A) are set to the point just before we see a reduction in noise at 10 $Hz$, and in (B) just after. Figure 5.11 shows simulations for this device under these two bias conditions. It can be seen that in Figure 5.11 (a) the conducting channel appears to be touching the silicon-silicon dioxide interface, whereas in Figure 5.11 (b) the channel is isolated from the surface. It can be concluded that the reduction in noise is indeed caused by the conducting channel leaving the proximity of the interface.

### 5.2.3 Conclusions

It has been shown that the noise performance of deep depletion mode MOS transistors can be optimised by carefully choosing the operating point. Simulations were used to show that the reduction in noise can be attributed to the spatial movement of the charge forming the channel. Specifically, as the gate voltage was made more negative, and the substrate bias more positive, the conducting channel could be made to move into the bulk silicon away from the silicon-silicon dioxide interface. By controlling the position of the channel in this manner, it was possible to reduce the level of the low frequency noise by an order of magnitude.

Unfortunately, no simple analytical method exists for predicting the spatial distribution of charge in a MOS transistor. This is particularly true when the device is biased in the saturation region. The free carrier concentration is a strong function of applied bias, ambient temperature and impurity profile. Therefore, one or two dimensional numerical simulation

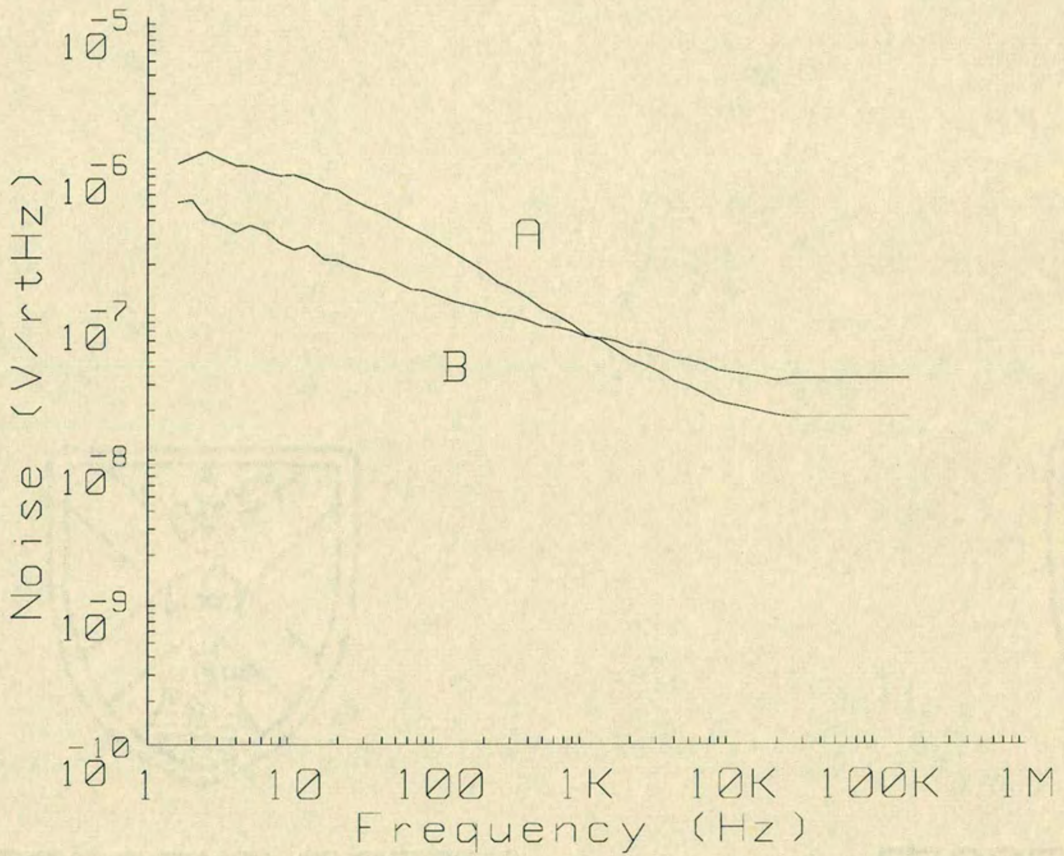
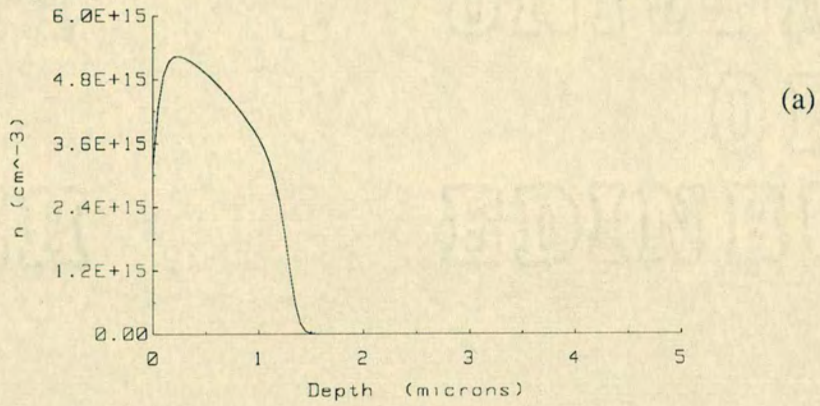



Figure 5.10: Noise spectra for deep depletion mode MOS transistor under two bias conditions. $V_{DS} = 1.00\ V$ , $I_{DS} = 455\ \mu A$.

| | | |
|---|---|---|
| (A) | $V_{GS} = 0.00\ V$ | $V_{BS} = -9.46\ V$ |
| (B) | $V_{GS} = -1.00\ V$ | $V_{BS} = -1.00\ V$ |



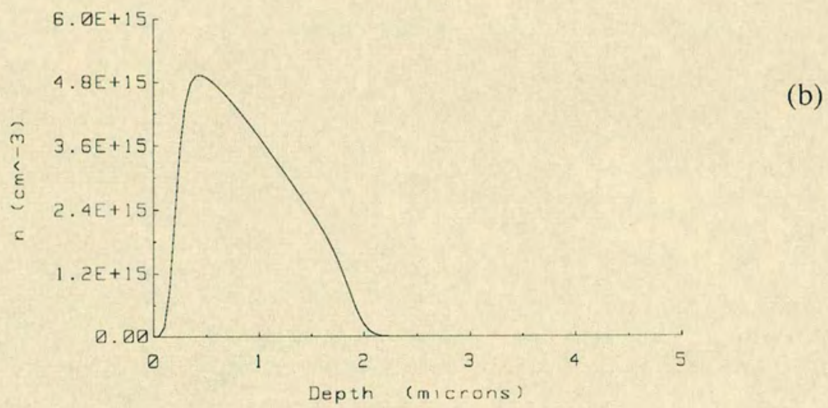




Figure 5.11: Simulations showing free carrier distribution for deep depletion mode MOS transistor under bias conditions shown in Figure 5.10.

| | | |
|---|---|---|
| (a) | $V_{GS} = 0.00\ V$ | $V_{BS} = -9.46\ V$ |
| (b) | $V_{GS} = -1.00\ V$ | $V_{BS} = -1.00\ V$ |

models must be used to explain noise characteristics such as those described above. Such models must also be used to assist in the prediction of noise performance in devices of a given impurity profile.

## 5.3 Conclusions

This chapter has presented results for $n$-channel deep depletion mode MOS transistors. It was shown that the position of the channel in deep depletion mode devices could be manipulated by modulating the gate voltage and substrate potential. It was shown that an order of magnitude reduction in the low frequency noise was possible in deep depletion mode devices. With the help of numerical simulations, it was shown that this reduction occurred when the channel was isolated from the silicon-silicon dioxide interface. This reduction was measured when the device was biased in both the linear and saturation regions.

# Chapter 6

# Anomalous Oscillation in Depletion Mode MOS Transistors at Low Temperature

In this chapter a low frequency oscillation in depletion mode and deep depletion mode MOS transistors at temperatures below ambient is described. This oscillation made complete analysis of the noise performance of these devices at low temperatures impossible. The effect may also preclude the use of these devices as circuit elements at temperatures lower than ambient.

## 6.1 Results

In this section results are presented showing an anomalous oscillation in depletion and deep depletion mode MOS transistors. Devices in the experiments were cooled by immersing them directly into liquid coolant. The

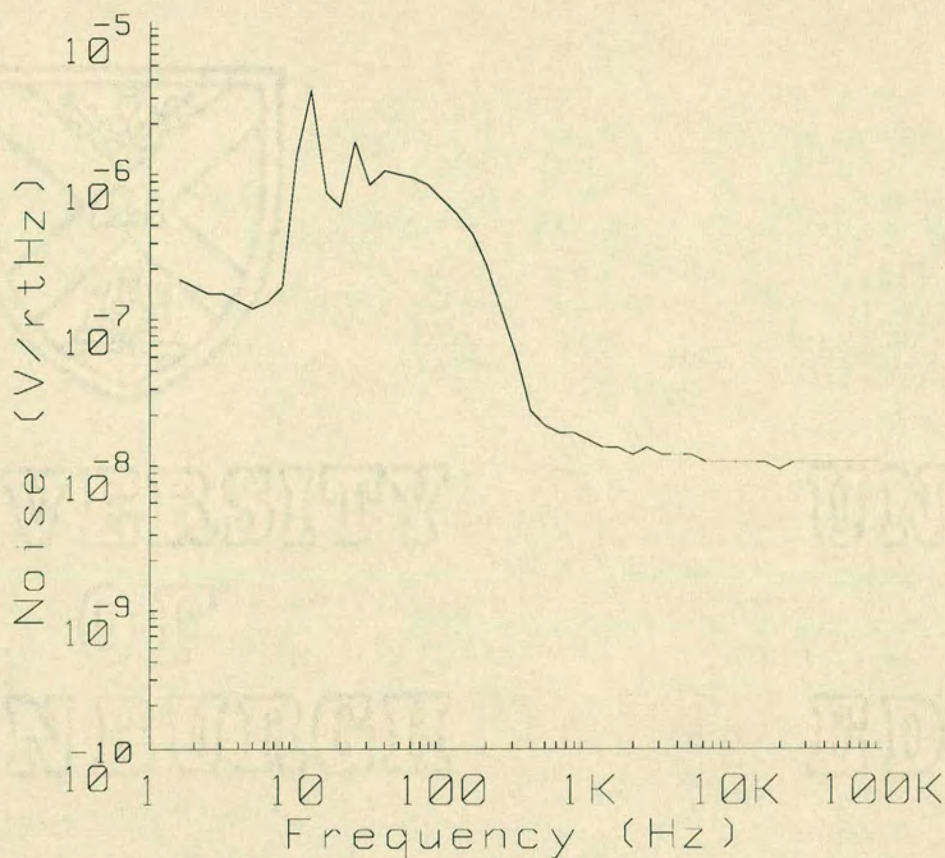



Figure 6.1: Noise spectrum for deep depletion MOS transistor cooled to liquid nitrogen temperature (77 $K$). $V_{DS}$ = 100 $mV, I_{DS} = 7.1\ \mu A$.

original aim of the experiments was to measure the noise characteristics of depletion mode MOS transistors at low temperature. The coolants used were liquid nitrogen (77 $K$), oxygen (90 $K$) and Freon† (196 $K$). The test transistors were mounted inside sealed packages to prevent the coolant from coming into contact with the surface.

Figure 6.1 shows the noise spectrum for a phosphorus doped deep depletion mode MOS transistor biased in the linear region at liquid nitrogen temperature. The oscillation can be seen as a broad band feature super-

†**Freon is a Registered Trademark.**

Figure 6.2: Oscilloscope trace showing $V_{DS}$ for deep depletion MOS transistor at liquid nitrogen temperature. $I_{DS} = 7.1\ \mu A$. Scale is 62.5 mV per division vertical, 20 ms per division horizontal.

imposed on the expected noise spectrum comprising the thermal noise floor above around 1 kHz and increased noise at low frequency. Maxima at around 13 Hz and 26 Hz were observed with additional components at frequencies up to around 300 Hz. Figure 6.2 shows an oscilloscope trace showing the drain voltage, $V_{DS}$, for the same device.

It can be seen that Figure 6.1 is the Fourier Transform of Figure 6.2. The width of the pulse in Figure 6.2 is reflected by the broad band increase in measured noise voltage in Figure 6.1.

In keeping with other noise measurements in this thesis, the device was operated in a constant current configuration, so the periodic increase in drain voltage seen in the time domain in Figure 6.2 reflect a periodic increase in channel resistance. The frequency of oscillation was not at all coherent, and

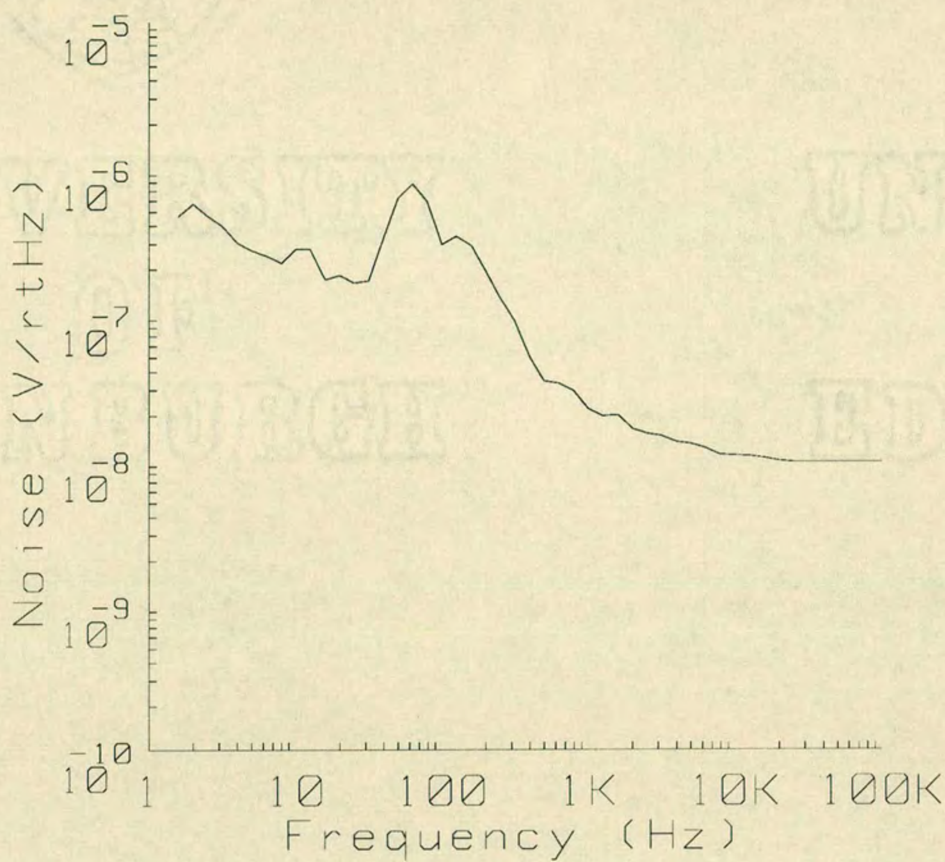



Figure 6.3: Noise spectrum for deep depletion MOS transistor at liquid oxygen temperature (90 $K$). We see an increase in oscillation frequency when compared to liquid nitrogen temperature (77 $K$). $V_{DS} = 100\ mV, I_{DS} = 16.9\ \mu A$.

at times could be quite erratic. At times, for example, the frequency would be observed to double, and very occasionally the frequency would be reduced completely with only occasional increases in resistance seen. An increase in temperature, however, gave an increase in frequency of this anomalous oscillation. For this sample, the frequency of oscillation moved from around 12 Hz to 80 Hz when the temperature was raised from 77 $K$ to 90 $K$, Figure 6.3.

The period of the 'oscillation' bursts is independent of drain and gate

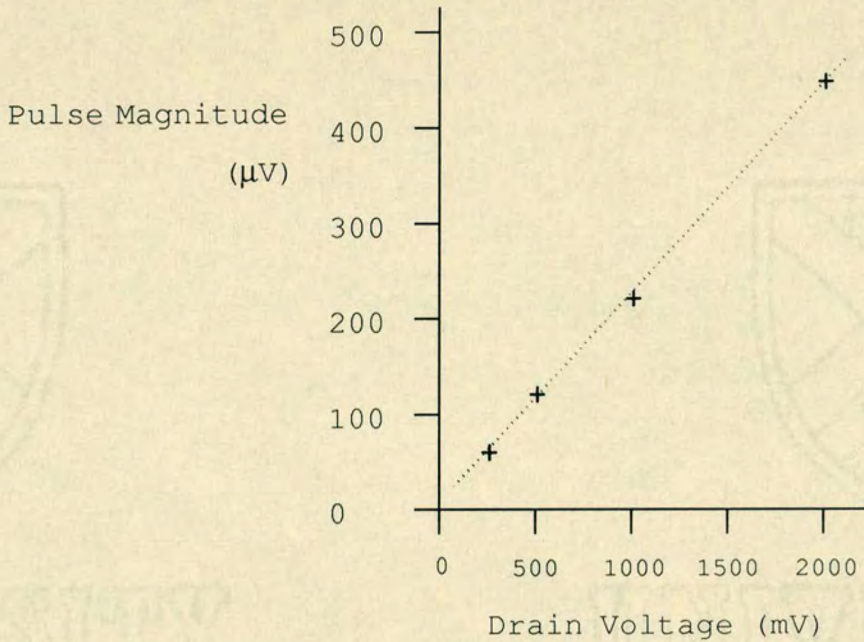



Figure 6.4: Linear dependence of peak magnitude on drain voltage.

bias, but the magnitude is a strong function of drain voltage. At and below the threshold voltage, the peak is lost in the thermal noise measured across the source and drain terminals. Above threshold, but with a zero drain voltage, the oscillation cannot be detected. As the drain voltage and current are increased, then so does the magnitude of the peak.

To illustrate this dependence on drain voltage, Figure 6.4 shows how the magnitude of the peak varies with drain voltage. The gradient of the straight line is approximately $2 \times 10^{-4}$. This means that each 'spike' corresponds to a momentary increase in channel resistance of around 0.02 %. This increase in channel resistance could be attributed to either a reduction in carrier mobility or a reduction in the number of free carriers. In the following section we use the simulation program described in Chapter 3 to investigate the magnitude of the temperature fluctuation required to give a reduction

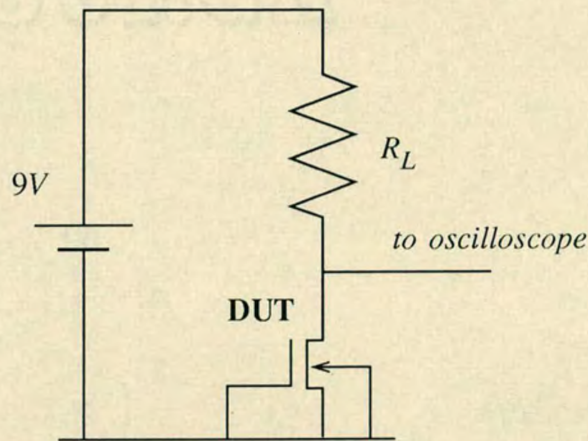



Figure 6.5: Simplified bias supply comprising load resistor and zinc-carbon battery.

in the carrier concentration of 0.02 %.

It was also possible that the oscillation was somehow introduced by the bias supply, the amplifier or the spectrum analyser. In order to eliminate this possibility, the bias supply was replaced by a single battery and load resistor, Figure 6.5, and the gate and substrate were connected directly to the source. With the transistor biased in this manner it was possible to measure the oscillation directly using only an oscilloscope connected across the source and drain terminals. In addition, the oscillation has *never* been observed in $n$-channel enhancement mode MOS transistors or devices with no implant in the channel. In summary, the effect was *only* measured in $n$-channel MOS devices with a phosphorus or arsenic implant in the channel region. It is concluded, therefore, that the effect is directly related to the device technology and is not introduced by the instrumentation.

## 6.2 Simulations of carrier distribution

If the crystal lattice in the region of the channel was to cool momentarily then some proportion of the ionised donors would freeze out causing a reduction in the free carrier concentration. This would have the effect of increasing the channel resistance. In order to maintain the drain current, any constant-current bias supply would increase the drain voltage to compensate. The resulting increased power consumption would heat the channel region of the MOS transistor. This would in turn re-ionise the frozen out donors, and pseudo-equilibrium would be restored.

In the previous section, it was observed that the magnitude of this effect corresponds to a change in the channel resistance of 0.02 %. Simulations are now used to calculate what temperature shift would be required in order to decrease the free carrier concentration by 0.02 %. The doping profile input to the simulation program was that generated for deep depletion structures by ICECREM. The temperature was set to be 77 $K$, the substrate bias, $V_{BS}$, to -5 V and the surface potential, $\Psi_S$, to 3 V. From previous simulation runs with this profile, it was known that these conditions would correspond to the device biased above threshold voltage. A solution for this temperature was obtained and the gate voltage, $V_G$, noted. The temperature was then reduced in small steps. For each temperature the surface potential was iteratively adjusted until the gate voltage was at the same bias as that noted for the 77 $K$ solution. The key results from the simulations are presented in Table 6.1.

It can be seen that the shift in temperature required for a 0.02 % shift in the integrated carrier concentration, $N_C$, is 4 $mK$. The magnitude of the

| Temperature ( $K$ ) | $N_C$ ( $cm^{-2}$ ) | $\Delta N_C$ ( % ) |
|---|---|---|
| 77.000 | $1.636388 \times 10^{11}$ | — |
| 76.996 | $1.636068 \times 10^{11}$ | -0.02 |

Table 6.1: Results from simulations to calculate temperature shift required for a 0.02 % reduction in free carrier concentration.

required temperature shift emphasises the low level of this anomalous effect. However, even this small oscillation was sufficient to effectively 'drown out' the background low frequency noise and make its measurement impossible.

## 6.3 Discussion

Despite extensive measurements, the physical origins of this anomalous oscillation remain obscure. The effect was *only* measured in $n$-channel depletion mode MOS transistors, and *only* at low temperatures. Steps were taken to ensure that the oscillation was not an artifact of the instrumentation.

If the oscillation was caused by some kind of thermal effect, then one might expect the frequency to be a function of device power dissipation. Measurements to date have failed to show any such power dependence. Table 6.2 shows the average measured frequency at a number of operating points. It can be seen there is no change in the measured oscillation frequency as the power dissipation is varied over this range.

Another possibility is that the oscillation was caused by some kind of thermal impedance oscillation between the sample and the nitrogen bath. Such an oscillation in the context of germanium infra-red detectors is de-

| Power Dissipation ( $\mu W$ ) | Oscillation Frequency ( $Hz$ ) |
|---|---|
| 4.0 | 24.7 |
| 15.8 | 23.8 |
| 58.3 | 26.0 |
| 230 | 24.4 |

Table 6.2: Oscillation frequency at a number of operating points.

scribed in [73]. However, attaching a relatively large thermal mass in the form of a copper or steel bar to the sample made no difference to the oscillation frequency.

Coon and Perera [74] observe a similar oscillation in silicon *p-i-n* diodes. In their experiments, *p-i-n* diodes are cooled to near liquid helium temperature (4.2 $K$). Figure 6.6 illustrates the bias configuration used in their experiments. At such low temperatures, the diodes no longer exhibit their normal rectifying properties. In addition, a voltage which is significantly higher than usual is required to initiate conduction. They attribute this conduction threshold to impact ionisation of carriers trapped in local states. For the samples studied, this conduction threshold could be as high as several tens of volts. When conduction commences the line capacitance begins to charge up. The onset of conduction leads to a reduction in the voltage across the diode which once again 'switches off' when the voltage falls to the conduction threshold. The result is repetitive firing or pulsing at a rate which is dependent on the applied voltage. In their experiments, Coon and Perera have observed times between successive pulses in the range 7 min-

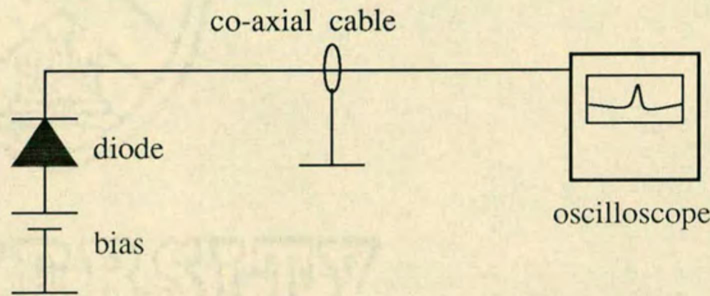



Figure 6.6: Experimental configuration used by Coon and Perera.

utes to 30 $ns$. The firing rate was a strong function of applied voltage. The effect has been likened to repetitive firing in neurons. The authors imagine a network of such elements where the pulses may be initiated or modulated by external stimuli. They envisage such a network forming the basis of the central processor in a neural computer. Experimental results illustrate silicon diodes being used to demonstrate logical operations and bifurication (periodic repetition of a double pulse).

The oscillation mechanism observed in the *p-i-n* diodes at liquid helium temperature could be related to the oscillation observed in deep depletion devices in these experiments. This opinion is based on their terminal performance, rather than identified physical mechanisms.

Measurements on similar MOS transistors performed by Kandiah [70] failed to show an oscillation like the one measured here. In his experiments the samples were cooled by mounting the device on top of a cold finger which was immersed in liquid nitrogen, whereas devices in the experiments here

were immersed in liquid nitrogen in sealed packages. Another difference is that the device under test in Kandiah's experiments forms an active component in the bias network and as such is always biased in the saturation region [62]. In these experiments the bias supply and device were passive with the transistor biased in the linear region or near saturation.

In his experiments, Kandiah observed a tendency for the deep depletion transistors to exhibit an increase in noise for a substrate bias, $V_{bs}$ of around $-5\ V$ at low temperatures [70]. He has suggested that this may offer some insight into the mechanism causing the anomalous oscillation in these experiments.

Das and Ghosh [75], and Canfield and Forbes [76] present results showing a very similar effect in GaAs MISFETs at room temperature. In a later work, Canfied and Forbes describe a technique for suppressing these oscillation by fabricating buried channel GaAs MISFETs [77]

## 6.4 Conclusions

Phosphorus-doped MOSFET devices can exhibit an anomalous low frequency oscillation at low temperatures. The physical mechanism appears obscure and further work to establish the nature of the effect should be undertaken.

Similar oscillations have been observed by other authors in *p-i-n* diodes at very low temperatures, and in GaAs transistors at room temperature.

# Chapter 7

# Applications for Deep Depletion MOS Transistors

In this chapter the use of deep depletion mode MOS transistors as circuit elements is discussed. It is shown that there are fundamental difficulties in incorporating the deep depletion devices in conventional amplifier circuits while retaining their very low noise performance. However, a novel design for a low noise buffer amplifier using a deep depletion transistor at the input is presented.

## 7.1 Requirement for Buffer Amplifier

There are a number of measurement and instrumentation applications which require a low noise, small signal, buffer amplifier with moderate gain. For example, such circuits might be used in conjunction with detectors in X-ray spectrometry or infra-red detection systems [62]. In this study, we assume that there is a requirement for a simple integrated amplifier stage with a voltage gain of 10 and an input noise of less than 1 $\mu V/\sqrt{Hz}$ at 10 $Hz$.

This was precisely the specification of the Electro-Optic Division of Philips Components, Southampton. The buffer amplifier was required for use in an advanced focal plane array infra-red detection system. An important feature is that the entire system comprising detector array, bias supplies, readout circuitry, and buffer amplifiers are all incorporated on a single silicon chip using hybrid technology. Figure 7.1 shows a typical application circuit [78]. Other imaging techniques involve the use of charge-coupled device readout strategies [79, 80, 81]. The circuit comprises a cadmium-mercury-telluride (CMT) photo-diode, a number of MOS transistors, and a storage capacitor. The storage capacitor may be fabricated using MOS technology. When the circuit is being used as part of an infra-red detection system, infra-red radiation is focused onto the CMT diode. This diode would normally form an element of a two-dimensional array of detectors. Such an array may be used to form a visible image of the infra-red components of a scene. In order to form this image it is first necessary to extract from the system a measure of the photo-current in each diode. This photo-current is a strong function of the magnitude of the infra-red radiation falling on that diode. Cadmium-mercury-telluride is chosen because it is possible to choose the wavelength of maximum sensitivity by varying the relative concentration of the elements from which the CMT crystal is composed [82].

The operation of the circuit in Figure 7.1 is as follows. The initial condition is with MOS transistors $T1$, $T2$, and $T3$ biased in the 'off' state. In addition, the storage capacitor has been charged to some predefined potential by the address and reset transistors, $T2$ and $T3$. No current will be flowing in the photo-diode and the diode will self-bias to its open-circuit potential of around 20 $mV$. A positive voltage is then applied to the gate

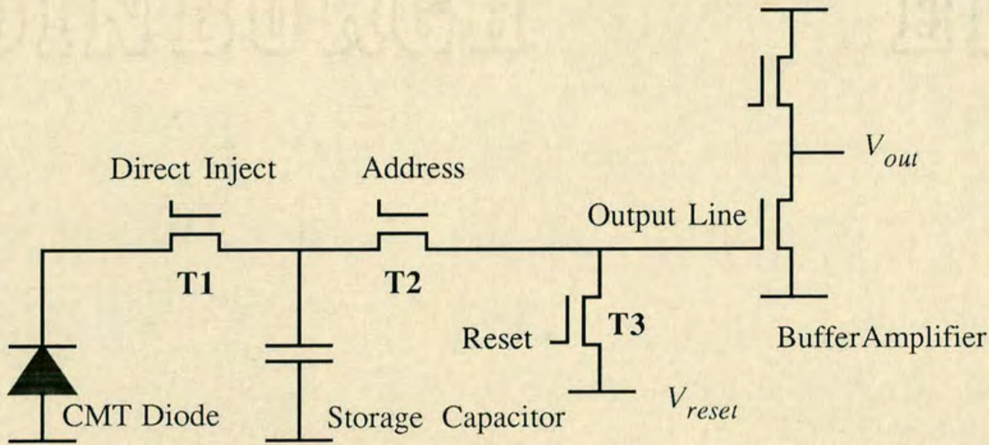



Figure 7.1: Schematic diagram showing direct injection current readout.

of the direct injection transistor, $T1$. The photocurrent will flow from the capacitor through the direct inject MOS transistor $T1$ into the diode. This has the net effect of discharging the capacitor to some extent. The duration of the pulse applied to the direct inject gate is known as the *stare time*. Clearly the magnitude of this pulse and the duration of the stare time must be chosen so as to avoid complete discharge of the capacitor which would cause the system to saturate. After the stare time, the address MOS transistor, $T2$, is switched fully on. If the output line capacitance is significantly lower than the storage capacitor, then the line should be charged up to the potential of the capacitor. A buffer amplifier can then be used to monitor the voltage on the output line, see Figure 7.1.

A key parameter in this class of configuration is the *injection efficiency* denoted by $\eta_{INJ}$. The injection efficiency is the fraction of the signal current which is injected into the direct inject MOS transistor. Clearly, this parameter requires to be maximised for a given diode and process technology. A

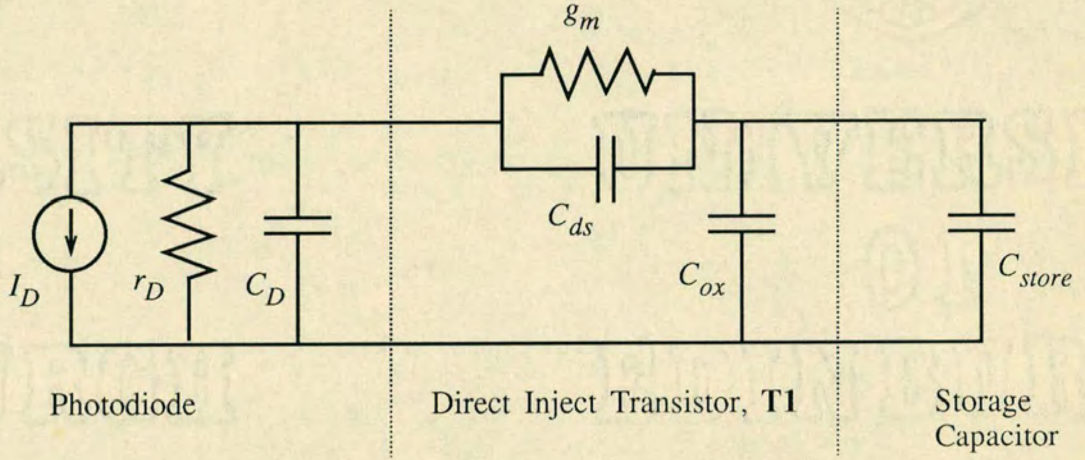



Figure 7.2: Equivalent a.c. circuit for the photodiode, the direct inject MOS transistor, $T1$, and the storage capacitor. See text for notation.

poor injection efficiency means that less of the signal and associated noise from the detector are injected, and hence the buffer amplifier and readout circuitry noise will become more significant.

Figure 7.2 shows the equivalent a.c. circuit for the photodiode, the direct inject MOS transistor, $T1$, and the storage capacitor. In this figure, $I_D$ is the photocurrent in the diode, $R_D$ and $C_D$ are the diode resistance and capacitance respectively, $g_m$ is the transconductance of the direct inject transistor, and $C_{ds}$ and $C_{ox}$ the source-drain and oxide capacitance. $C_{store}$ is the charge storage capacitor. An assumption here is that the input impedance of the direct inject MOS transistor will be given by $1/g_m$. The injection efficiency, $\eta_{INJ}$, and bandwidth, $f_{BW}$, of the system can be expressed as [2]

$$\eta_{INJ} \approx \frac{g_m R_D}{1 + g_m R_D} \left( \frac{1}{1 + \omega / 2\pi f_{BW}} \right) \tag{7.1}$$

with

$$f_{BW} = \frac{1 - g_m R_D}{2\pi R_D C_D} \tag{7.2}$$

where $g_m$ is the transconductance of the direct inject MOS transistor, $R_D$ and $C_D$ are the diode resistance and junction capacitance respectively, and $\omega$ is the radial operating frequency of the circuit. The important point to note is that both the injection efficiency, $\eta_{INJ}$, and bandwidth, $f_{BW}$, of the system can be increased by increasing the transconductance, $g_m$, of the direct inject MOS transistor †.

Another technique for increasing the transconductance of the direct inject MOS transistor is to increase the channel current, or increasing the channel width to length ratio of the transistor. Clearly, the channel current is limited to photo current flowing in the diode. Such currents may be very small indeed with typical values in the range of a few or few tens of nano-amps [2]. At such low currents the device transconductance is not a strong function of geometry making the latter approach of limited use.

One technique for increasing the transconductance is to use the buffered direct injection current readout circuit as shown in Figure 7.3. This circuit is sometimes referred to as the Rockwell Circuit [2]. The additional amplifier is used to increase the injection efficiency by effectively decreasing the input impedance of the direct injection MOS transistor. With the conventional direct injection scheme described above, any change in photo current, $\Delta I_D$, is accommodated for by a small change in the voltage at the source of the

† Another way to increase both the injection efficiency, $\eta_{INJ}$, and bandwidth, $f_{BW}$, of the system would be to increase the detector diode resistance, $R_D$. The diode resistance is in general fixed for a given diode. The performance and technology implications of increasing the resistance are outwith the scope of this thesis. Instead, attention is drawn to techniques for increasing the transconductance of the direct inject MOS transistor.

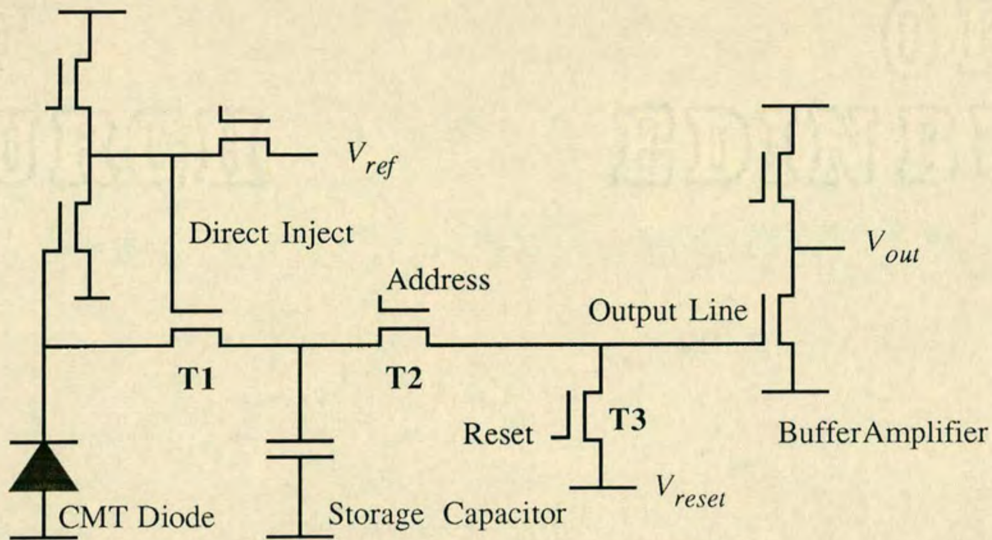



Figure 7.3: Schematic diagram showing buffered direct injection.

direct injection MOS transistor. With buffered direct injection, however, the voltage change needed for any change in the photo current can be reduced significantly, as follows. If the voltage gain of the buffer amplifier is defined to be $A_V$, then the gate voltage of the direct injection MOS transistor would change by $-A_V$ times the voltage shift required at the source of the direct inject transistor, $T1$. Hence, the majority of the voltage shift required can be made to occur at the gate. If the gain of this feedback buffer amplifier was 50, for example, then only 1/50th of the voltage shift would occur at the source. This would have the effect of increasing the transconductance, $g_m$, of the direct inject MOS transistor by 50.

In the following sections, we consider simple amplifier circuits which may be employed at the output of the circuit. A similar amplifier may also be employed in the feed-back loop used in the buffered direct injection scheme shown in Figure 7.3.

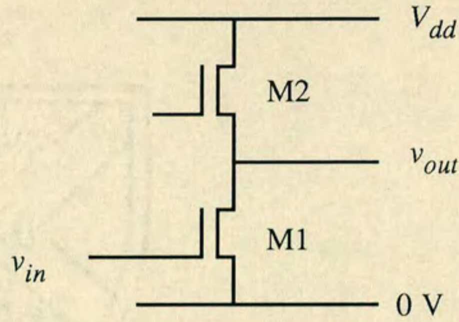



Figure 7.4: Simple inverter.

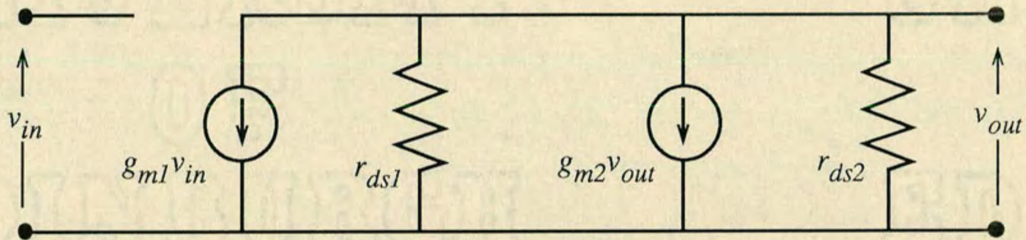



Figure 7.5: Small signal equivalent circuit for inverter.

## 7.2 Inverter Analysis

The inverter is the most basic of all voltage amplifier stages. Figure 7.4 shows a schematic circuit diagram for a simple inverter. Typically the inverter will employ the common source configuration as shown here. In integrated form the load may be either an active resistor or may be a current sink. In the latter configuration, an additional voltage supply is required to hold the gate voltage of the load transistor at some potential.

Figure 7.5 shows the small signal equivalent circuit for the inverter illustrated in Figure 7.4. The inverter can be described as two voltage controlled current sources, $g_{m1}v_{in}$ and $g_{m2}v_{out}$, in parallel with channel resistances $r_{ds1}$ and $r_{ds2}$.

Now, considering the components of small signal currents in the circuit it can be seen that

$$v_{in}g_{m1} + v_{out}/r_{ds1} + v_{out}g_{m2} + v_{out}/r_{ds2} = 0 \tag{7.3}$$

The voltage gain of the inverter circuit is defined as $A_v = v_{out}/v_{in}$. Setting $r_{ds} = 1/g_{ds}$, from Equation 7.3 it can be seen that

$$A_v = v_{out}/v_{in} = \frac{-g_{m1}}{g_{ds1} + g_{ds2} + g_{m2}} \tag{7.4}$$

In the analysis of inverter circuits employing conventional enhancement mode MOS transistors the transconductance, $g_m$, is generally much greater than the channel conductance, $g_{ds}$, and the voltage gain can be approximated by $-g_{m1}/g_{m2}$. However, deep depletion mode MOS transistors have a $g_{ds}$ comparable to the $g_m$ making it imperative to use Equation 7.4 in full to calculate the gain.

Similarly, the small signal output resistance can be found from the equivalent circuit to be

$$r_{out} = \frac{1}{g_{ds1} + g_{ds2} + g_{m2}} \tag{7.5}$$

Typical values for $g_m$ and $g_{ds}$ for both enhancement and deep depletion mode devices are summarised for convenience in Table 7.1. The values for the deep depletion transistor are for a device biased in the buried channel low noise régime. Before calculating the gain for an inverter incorporating deep depletion devices in its realisation, we need to examine how $g_m$ and $g_{ds}$ scale with device geometry.

Now, the device transconductance can be found from

$$g_m = \left.\frac{\delta I_D}{\delta V_{GS}}\right|_{V_{DS},const}$$

| Transistor type | Geometry ($\mu m$) | $g_m$ ($\mu A/V$) | $g_{ds}$ ($\mu A/V$) |
|---|---|---|---|
| Deep Depletion | $100 \times 15$ | 30 to 5 | 140 |
| Enhancement [83] | $10 \times 10$ | 50 | 0.5 |

Table 7.1: Typical transistor parameters.

$$= \sqrt{2K'\frac{W}{L} \mid I_D \mid} \ (1 + \lambda V_{DS})$$

$$\approx \sqrt{2K'\frac{W}{L} \mid I_D \mid} \tag{7.6}$$

where $K'$ is the process gain factor. Note that Equation 7.6 is valid only when the device is biased in the saturation region.

Similarly,

$$g_{ds} = \left.\frac{\delta I_D}{\delta V_{DS}}\right|_{V_{GS},const}$$

$$= \frac{I_D \lambda}{1 + \lambda V_{DS}}$$

$$\approx I_D \lambda \tag{7.7}$$

where $\lambda$ is the channel length modulation factor which is inversely proportional to the channel length $L$. The important point to note from Equation 7.7 is that the device conductance is proportional to $I_D$ and inversely proportional to the channel length through $\lambda$.

Equations 7.6 and 7.7 can now be used to scale the parameters in Table 7.1 to enable the calculation of the inverter gain.

Consider first the case where both $M1$ and $M2$ in Figure 7.4 are deep depletion mode MOS transistors. In order to obtain useful gain it is usual to have a $\frac{W_1}{L_1}$ of greater than unity and a $\frac{W_2}{L_2}$ of less than unity [84]. If $M1$ is a 100 $\mu m$ × 15 $\mu m$ transistor then the parameters in Table 7.1 may be used directly. As an example of dimensions for the load transistor $M2$, let us consider a deep depletion transistor with a $\frac{W_2}{L_2}$ of $\frac{10}{50}$. In this case,

$$g_{m2} = \sqrt{2K'\frac{W_2}{L_2} \mid I_D \mid}$$

$$\approx 5.20 \; \mu A/V. \tag{7.8}$$

Similarly,

$$g_{ds2} = g_{ds1}(\frac{L_2}{L_1})$$

$$\approx 42.0 \; \mu A/V. \tag{7.9}$$

This latter result gives a channel resistance $r_{ds}$ of around 23.8 $k\Omega$.

From these values we can calculate the voltage gain of the inverter circuit using Equation 7.4 to be approximately −0.16. Clearly, this is well below the required gain of -10.

We now consider the case where the load transistor $M2$ is an enhancement mode transistor. If $g_{ds2} = 1.0 \; \mu A/V$ and $g_{m2} = 26.1 \; \mu A/V$ then the gain is still dominated by the high $g_{ds1}$ in the denominator of Equation 7.4.

Any attempt to reduce $g_{ds1}$ by increasing the channel length, $L$, has only limited effect since the transconductance, $g_{m1}$, is also reduced with $L$.

It is concluded that the high channel conductance of the deep depletion transistor precludes their use in the simple inverter circuit.

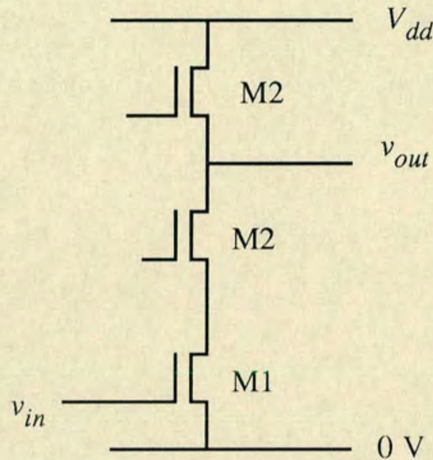



Figure 7.6: Block diagram of cascode stage.

## 7.3 Cascode Amplifier Analysis

It was shown above that the simple inverter was not able to utilise deep depletion mode MOS transistors in its realisation. We now turn our attention to the cascode amplifier. This type of amplifier offers the analogue circuit designer two distinct advantages over the simple inverter. Firstly, a reduction in the Miller capacitance is obtained. Clearly this reduction would be useful in the design of high frequency systems. A second advantage of the cascode stage is an increase in the output impedance. In this section we examine the reasons for this increase with a view to investigating the possibility of using low noise deep depletion mode structures in the construction of the amplifier.

Figure 7.6 shows a cascode amplifier. The construction is similar to the simple inverter but with the inclusion of an additional common-gate transis-

tor between the driver and the load. This transistor is $M2$ in Figure 7.6. $M2$ is included to keep the small signal resistance looking back into the drain of $M2$ larger than that of $M1$ alone. We now proceed to deduce the small signal equivalent circuit with a view to predicting the circuit gain.

Figure 7.7 (a) shows the equivalent circuit for the cascode amplifier. The circuit can be viewed as two voltage controlled current sources, $g_{m1}v_{in}$ and $g_{m2}v_1$, each in parallel with their respective channel resistance, $r_{ds1}$ and $r_{ds2}$. The series combination of this pair is in parallel with $r_{ds3}$ and the small signal output voltage $v_{out}$.

Figure 7.7 (b) shows the same equivalent circuit, but with the single current source $g_{m2}v_1$ replaced with two identical current sources. This step follows the current-source rearrangement and substitution rules described by Allen and Holberg [83]. Finally, in Figure 7.7 (c) the current source $g_{m2}v_1$ in Figure 7.7 (b) has been replaced by an equivalent resistor of value $1/g_{m2}$ over the internal voltage $v_1$. We may do this substitution since the voltage dependent current source was dependent on $v_1$.

Using nodal analysis, we have

$$[1/r_{ds1} + 1/r_{ds2} + g_{m2}]\, v_1 - 1/r_{ds2}v_{out} = -g_{m1}v_{in}$$

$$-[1/rds1 + g_{m2}]\, v_1 + (1/r_{ds2} + 1/r_{d}s3)v_{out} = 0 \qquad (7.10)$$

Solving for $A_v = v_{out}/v_{in}$, and setting $g_{ds} = 1/r_{ds}$

$$A_v = \frac{-g_{m1}(g_{ds2} + g_{m2})}{g_{ds1}g_{ds2} + g_{ds1}g_{ds3} + g_{ds2}g_{ds3} + g_{m3}g_{ds3}}. \qquad (7.11)$$

There are two cases two consider. In the first instance we shall calculate the gain for a cascode amplifier with a deep depletion mode MOS transistor as the common gate transistor, $M2$, and another deep depletion transistor at

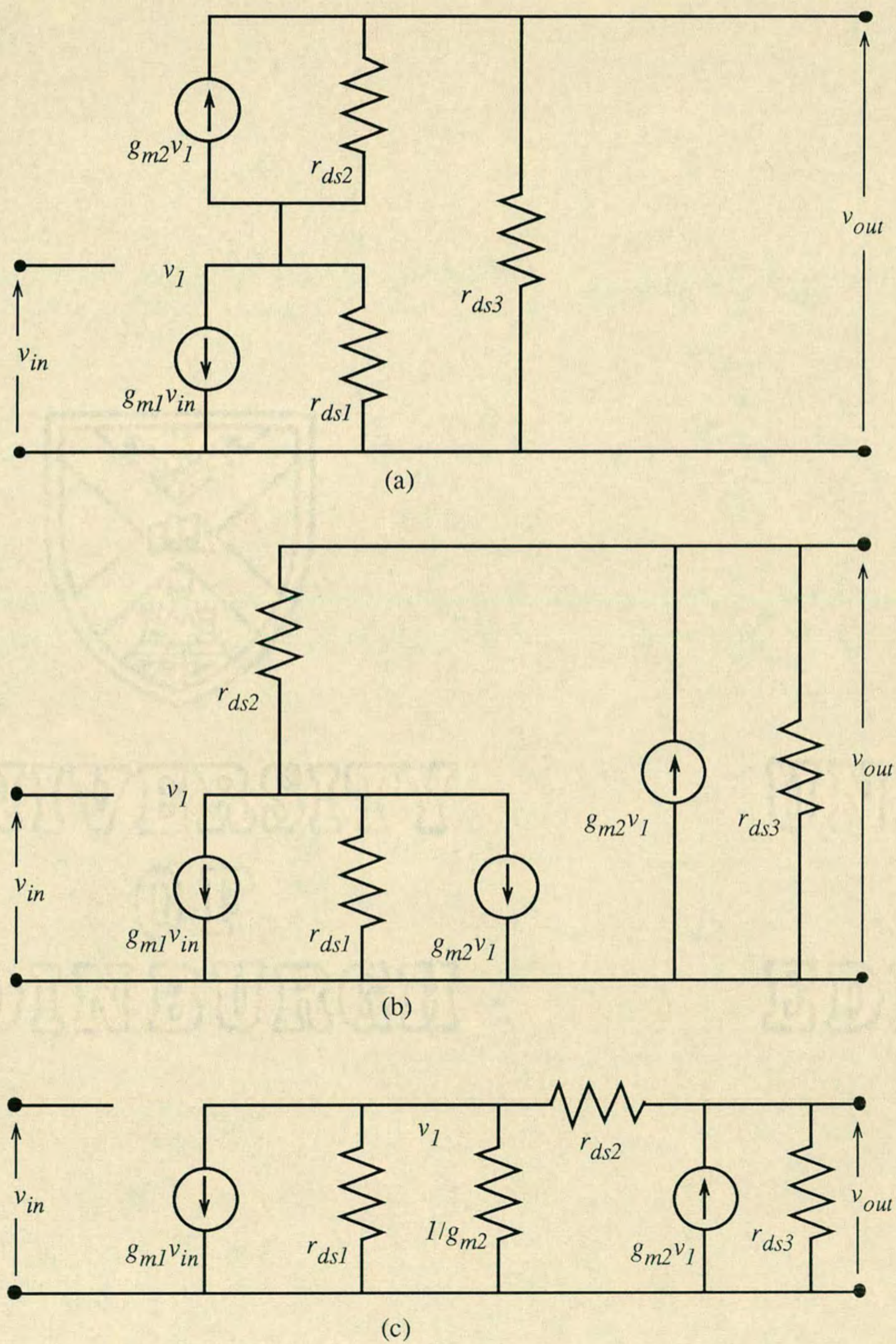



Figure 7.7: Equivalent circuits for cascode stage amplifier. The transformations leading to equivalents (b) and (c) are described in the text.

the input, $M1$. Secondly, we shall compute the gain with an enhancement mode transistor as $M2$ and a deep depletion transistor at the input, $M1$ †.

In both cases it will be assumed that the input transistor is a deep depletion mode device to keep the noise low, and that the load is an enhancement mode transistor.

If the input transistor $M1$ has a $\frac{W_1}{L_1}$ of $\frac{100}{15}$ as before then $g_{m1}$ is around $30\mu A/V$ and $g_{ds1}$ can be as high as $140\mu A/V$. The enhancement load $M3$ will be assumed to have a $g_{m3}$ of $1\mu A/V$ and a $g_{ds3}$ of $26.1\mu A/V$.

Considering first a deep depletion transistor for $M2$ with a $\frac{W_2}{L_2}$ of $\frac{100}{15}$ then the gain can be found form Equation 7.11 to be $A_v = -0.18$. With an enhancement transistor $M2$ with a $\frac{W_2}{L_2}$ of $\frac{10}{10}$ the situation is improved slightly but the gain is still only $A_v = -0.3$.

Once again, it is the high values for the device conductance in the deep depletion mode devices which makes their use in the circuit difficult.

## 7.4 Cascode Amplifier with Bipolar Transistor

In the preceding sections it was shown that the use of deep depletion mode devices at the input of either an inverter or a cascode stage amplifier prevents the circuit from delivering useful gain. Ideally, the transistor $M2$ in Figure 7.6 should have an input resistance somewhat lower than the value

† If $M1$ is an enhancement transistor and $M2$ a deep depletion mode transistor, then $A_v$ can be shown to be $-1.88$. But this configuration offers no useful improvement in noise performance. Indeed, in this case the high value of conductance $g_{ds2}$ in the bottom line of Equation 7.11 will make the gain substantially lower than the simple inverter without the cascode.

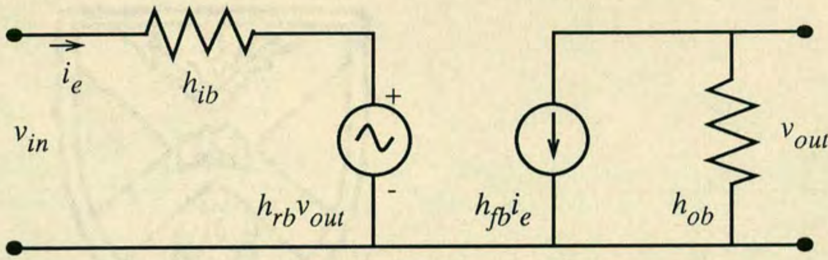



Figure 7.8: $h$-parameter equivalent circuit for bipolar transistor biased in common base mode.

for $1/g_{ds1}$ for the input transistor. In this way the majority of the current in $M1$ will be diverted through $M2$, thereby improving the overall circuit gain. In this section the use of a bipolar transistor as $M2$ is investigated.

If a combination of a deep depletion mode transistor and a bipolar transistor are to be realised on the same integrated circuit then the designer will be required to turn to a merged bipolar MOS process. A number of manufacturers have developed commercial merged bipolar CMOS processes [85, 86, 87]. These processes are often referred to as 'BiCMOS'. There are a number of reasons for developing a combined process. Bipolar transistors offer certain performance advantages over MOS transistors particularly at high frequencies. Advantages include faster switching characteristics, and higher gain. Alternatively, MOS transistors offer improved packing density, better scaling of parameters with geometry, and lower power consumption. With increased integration the trend has been towards complete systems on one chip incorporating both analogue and digital components. The advantages offered by BiCMOS processes have made such integration possible.

The $h$-parameter equivalent circuit for a bipolar transistor in common base configuration is shown in Figure 7.8. The common base configuration

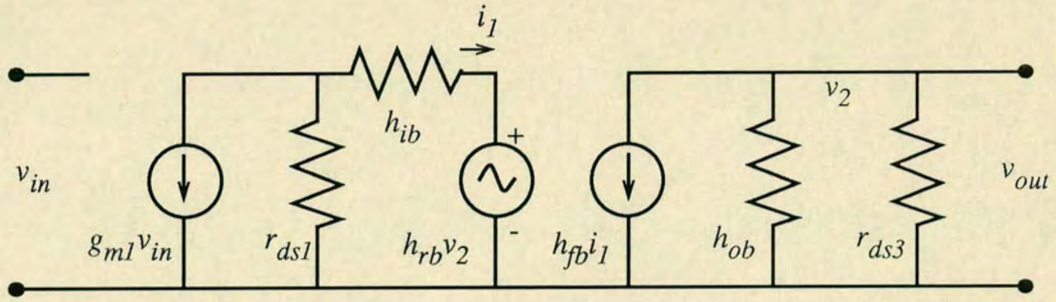



Figure 7.9: Equivalent circuit for the cascode stage amplifier incorporating a bipolar transistor.

| $h$-parameter | Definition | Typical value |
|---|---|---|
| $h_{ib}$ | common base input impedance | 3.6 Ω |
| $h_{rb}$ | reverse voltage feedback ratio | $1.45 \times 10^{-4}$ |
| $h_{fb}$ | forward current transfer ratio | -0.994 |
| $h_{ob}$ | common base output admittance | $0.45 \times 10^{-6} mho$ |

Table 7.2: Definition of $h$-parameters for a bipolar transistor in common base mode, and typical values.

offers both a low input impedance and a current gain, $h_{fb}$, which is close to unity. The $h$-parameter equivalent circuit model can be used to deduce the small signal equivalent circuit for the cascode stage amplifier incorporating a bipolar transistor. Figure 7.9 shows the equivalent circuit of the complete amplifier. The circuit may be viewed as comprising two separate subcircuits. In the left subcircuit there is a current source $g_{m1}v_{in}$ over $r_{ds1}$ representing the input transistor and an impedance of $h_{ib}$ looking into a voltage source of $h_{rb}v_2$. From Table 7.2, it can be seen that $h_{ib}$ is only a few ohms and $h_{rb}v_2$ is a fraction of a millivolt even when internal voltage $v_2$ is several volts.

The right subcircuit is a current source $h_{fb}i_1$ in parallel with $h_{ob}$ and $r_{ds3}$. The equivalent circuit in Figure 7.9 may be used to derive an expression of the gain of the circuit, and to calculate its noise performance.

As before, the small-signal voltage gain of the circuit, $A_v$, is defined as $v_{out}/v_{in}$. Now, noting that $h_{fb}i_1$ in Figure 7.9 may be replaced by $h_{fb}g_{m1}v_{in}$, the voltage gain can be shown to be

$$A_v = \frac{v_{out}}{v_{in}} = \frac{h_{fb}g_{m1}}{h_{ob} + g_{ds3}}. \tag{7.12}$$

Using the values in Table 7.1 and Table 7.2 the gain is around $A_v = -29.8$. This figure is considerably better than the original requirement for a gain of $A_v = -10$.

The noise performance can also be derived from the equivalent circuit in Figure 7.9. We begin by assuming that there is an equivalent root mean square input noise voltage, $\sqrt{e_n^2}$, in series with the gate of each device. For clarity, we shall adopt the shorthand notation

$$e_n = \sqrt{e_n^2} \tag{7.13}$$

The noise will be dominated by the noise in the two MOS transistors, $M1$ and $M3$. Now, the output noise voltage, $e_{out}$, can be found from

$$e_{out}^2 = e_{n1}^2 \left( \frac{h_{fb}g_{m1}}{h_{ob} + g_{ds3}} \right)^2 + e_{n3}^2 \tag{7.14}$$

where $e_{n1}^2$ is the r.m.s. input noise voltage of transistor $M1$, $e_{n3}^2$ is the r.m.s. input noise voltage of transistor $M3$, the $h$ parameters are those for the bipolar transistor, and the $g$ parameters are those for the enhancement and deep depletion mode transistors respectively. We now divide the r.m.s. output noise voltage squared, $e_{out}^2$, by the square of the voltage gain, $A_V$ as given by Equation 7.12. From the definition of voltage gain, this yields the

square of the equivalent input noise voltage, $e_{eq}^2$, as

$$e_{eq}^2 = e_{n1}^2 \left[ 1 + \left( \frac{h_{ob} + g_{ds3}}{h_{fb} g_{m1}} \right)^2 \frac{e_{n3}^2}{e_{n1}^2} \right]. \quad (7.15)$$

Taking square-roots,

$$e_{eq} = e_{n1} \left[ 1 + \left( \frac{1}{A_v} \right)^2 \frac{e_{n3}^2}{e_{n1}^2} \right]^{\frac{1}{2}}. \quad (7.16)$$

Substituting $e_n$ for $v_n g_{ds}/g_m$, where $v_n$ is the absolute noise voltage *across* the channel, we have

$$e_{eq} = v_{n1} \left[ 1 + \left( \frac{1}{A_v} \right)^2 \frac{v_{n3} g_{ds3} g_{m1}}{v_{n1} g_{ds1} g_{m3}}^2 \right]^{\frac{1}{2}}. \quad (7.17)$$

As before, $v_{n1}$ is the r.m.s. noise voltage across $M1$, *etc.* Now, from Equation 7.17 it can be seen that the equivalent gate input noise depends mainly on $v_{n1}$ since $g_{ds1} > g_{m1}$ and $g_{ds3} \ll g_{ds1}$. Now, with $v_{n1} = 2 \times 10^{-7}\ V/\sqrt{Hz}$ at $10\ Hz$ (taken from Figure 5.8), and $v_{n3} = 1 \times 10^{-5}\ V/\sqrt{Hz}$ the equivalent gate input noise can be calculated as $e_{eq} = 9.33 \times 10^{-7}\ V/\sqrt{Hz}$. This is below the target specification of $1 \times 10^{-6}\ V/\sqrt{Hz}$.

## 7.5 Conclusions

The analysis in this section has shown that it is possible to make use of a low noise deep depletion transistor in a buffer amplifier design by incorporating a bipolar transistor into a cascode stage. The bipolar transistor was necessary to isolate the high channel conductance of the deep depletion device from the output stage. The noise was shown to be dominated by that in the input transistor, making the deep depletion device operated in buried channel mode ideal for this purpose. It was shown that a buffer amplifier with a voltage gain of around $-30$ was possible, with an equivalent input noise

voltage of less than 1 $\mu V/\sqrt{Hz}$. This cascode circuit could prove useful in key low noise signal processing applications.

# Chapter 8

# Conclusions

This chapter summarises the objectives of this thesis and shows how those objectives were achieved. Suggestions are made as to possible areas for further study.

## 8.1 Objectives and Achievements

The aim of this thesis was to investigate the noise performance of deep depletion MOS transistors and make recommendations for their use in analogue circuits and systems. Specifically, there was a requirement for a low noise buffer amplifier for use with advanced infra-red detection systems. The specification was such that the amplifier could not be realised in conventional (*i.e.* surface channel) MOS technology.

A noise measurement system was developed to enable rapid characterisation of MOS transistor noise under a variety of operating conditions. Detailed measurements were performed on deep depletion MOS devices. Further measurements were performed on more conventional MOS transistors, and these results are presented in Appendix A. It was appropriate to study

$n$-channel enhancement, intrinsic, and depletion mode MOS transistors devices in order to give some perspective to measurements on deep depletion structures.

The following four points may be deduced from this thesis regarding noise performance in MOS transistors and circuits.

- It was shown that an order of magnitude reduction in noise was possible with deep depletion mode MOS transistors. By biasing the device so that the conducting channel was isolated from the silicon-silicon dioxide interface by the surface depletion region, it was possible to achieve low noise with no significant loss in gain. Simulations were used to show how the noise could be reduced by varying the position of the channel in this manner.

- An anomalous oscillation was detected in deep depletion and depletion mode transistors at temperatures lower than ambient. The effect was similar to oscillations seen in GaAs transistors under certain bias conditions, and in *p-i-n* diodes at very low temperatures. A precise physical model which explains this oscillation has remained elusive.

- A novel cascode circuit incorporating a bipolar transistor was proposed in which the input transistor was a deep depletion mode transistor. The circuit was able to deliver acceptable gain while exploiting the low noise of deep depletion MOS transistor, yielding an extremely low noise buffer amplifier.

- Noise results in enhancement and intrinsic MOS transistors demonstrated that implantation damage resulting from threshold control implants could be removed by careful annealing (Appendix A).

One of the original objectives of this research was to design a buffer amplifier using the existing process technology at Philips Components Southampton. This objective was not met, since there exists no method for fabricating a suitable bipolar transistor using existing process steps. The low output impedance of the deep depletion mode MOS transistor precluded the use of this kind of device in circuits using existing technology.

Three papers and reports were published reporting significant results from the experimental work of this thesis [88, 49, 89]. These works are reproduced at the end of the thesis in the "Relevant Publications" section. In addition, a number of (unpublished) internal reports were produced for the Electro-Optic Division, Philips Components, Southampton. These reports enabled engineers to consider significant results while designing infra-red detection systems.

## 8.2 Future Work

This section offers suggestions for future research resulting directly from this thesis

Time did not permit a detailed study of the effects of process technology on noise behaviour. Clearly the deep depletion mode device can offer significant improvements in noise performance. Further research should be undertaken to investigate alternative profiles for forming a buried channel. For example, the $n$-well in the deep depletion devices fabricated here extends almost 3 $\mu m$ into the silicon substrate. It should be possible to achieve similar noise performance with an $n$-well which does not extend to the same extent. Indeed, such a profile could offer a superior channel conductance,

$g_{ds}$, because the channel would be confined to a smaller volume.

The deep depletion device could perhaps be further improved by implanting the channel region closest to the surface with boron. The presence of additional acceptors here would help isolate the $n$-channel from the surface. Such a profile would enable more of the charge forming the channel to reside close to the gate. This would have the effect of keeping the gain, $g_m$ of the device high, since this depends on a tight coupling between the gate and the channel.

Clearly the cause of the anomalous oscillation seen in deep depletion mode MOS transistors requires further investigation. Although the magnitude of the effect is small it effectively prevented detailed measurement of the noise characteristics of these devices at low temperature.

## 8.3 Summary

The thesis has analysed the deep depletion mode MOS transistor. This device has been shown to have a noise performance superior to that of conventional MOS transistors. The improvement in noise performance was explained by means of device simulation. A unique application circuit was discussed which used the noise performance of the deep depletion MOS transistor to good effect.

# Appendix A

# Noise in Conventional MOS Transistors

## A.1 Introduction

This appendix presents noise results for conventional enhancement mode and depletion mode $n$-channel transistors.

Section A.2 describes the process details for the three types of MOS transistor characterised in this appendix.

Section A.3 presents results for enhancement mode MOS transistors. These devices have a boron implant to give a threshold voltage, $V_T$, of around $+0.9\ V$. In this conventional type of structure the charge forming the conducting channel is in close proximity to the silicon-silicon dioxide interface. In Chapter 2 it was shown that traps near this interface were responsible for noise contributions at low frequency. Consequently, the measured low frequency noise level in these devices is predicted to be relatively high [14, 90].

In Section A.4 results are presented for specially fabricated MOS transistors identical to those in Section A.3, but with no threshold voltage control implant. These 'intrinsic' MOS transistors are also enhancement mode structures since the substrate is lightly doped $p$-type with an acceptor concentration of around $5 \times 10^{14}$ $atoms/cm^{-3}$. The aim of investigating this kind of structure was to see if implantation damage resulting from the boron implant and remaining after the anneal results in an additional low frequency noise contribution.

Section A.5 examines the noise in $n$-channel depletion mode structures. These devices were fabricated on the same wafers as the $n$-channel enhancement and intrinsic MOS transistors described above.

## A.2 Process Details

In this section the process steps which lead to the fabrication of the MOS transistors studied in this appendix are discussed. The $n$-channel devices can be divided into three categories: enhancement mode, intrinsic, and depletion mode.

Figure A.1 shows schematic cross sections of the three types of MOS transistors studied here. Figure A.1 (a) shows an $n$-channel enhancement mode MOS transistor. Here, boron is implanted into the channel to increase the threshold voltage, and provide better threshold voltage uniformity from device to device. Figure A.1 (b) shows an intrinsic enhancement mode transistor. In this device, there is no threshold voltage control implant in the channel. An $n$-channel depletion mode MOS transistor is shown in Figure A.1 (c), where an arsenic implant in the channel provides a 'normally

on' type of device.

The $n$-channel MOS transistors studied here were formed on $p$-type wafers with a crystal orientation of <100>. The boron substrate doping for the $n$-channel devices was $5.5 \times 10^{14} atoms\ cm^{-3}$, giving a sheet resistivity of $15 - 20\ \Omega\ cm^{-2}$.

Enhancement mode transistor channel regions received a boron implant to increase the acceptor concentration under the gate, see Figure A.1 (a). The implantation dose was $4.5 \times 10^{11}\ atoms\ cm^{-2}$ with an energy of $3.0\ keV$ through the 750 Å gate oxide. Figure A.2 shows the doping profile of these transistors as predicted by ICECREM. At the surface, the implanted boron concentration is reduced due to boron being drawn into the oxide during the anneal step.

Intrinsic enhancement MOS transistors are those with no threshold voltage control implant in the channel region, see Figure A.1 (b). These were fabricated in a similar way to the enhancement mode devices described above, but an additional mask was employed to block the boron implant. The aim of studying these structures was to see if the boron implant in enhancement-mode devices introduces additional traps or bulk defects. Bulk defects would have the effect of increasing the measured low frequency noise in the enhancement mode devices [91].

Depletion mode transistors were formed by implanting arsenic into the substrate in the channel region. This is shown in Figure A.1 (c). The dose was $1.56 \times 10^{12}\ atoms\ cm^{-2}$ at an energy of $40\ keV$. After the implant, the wafers were subjected to a 20 hour drive-in at 900 °C. The ICECREM predicted profile for this process is shown in Figure A.3. The junction depth is predicted to be 0.15 $\mu m$ which at first sight seems to be rather shallow

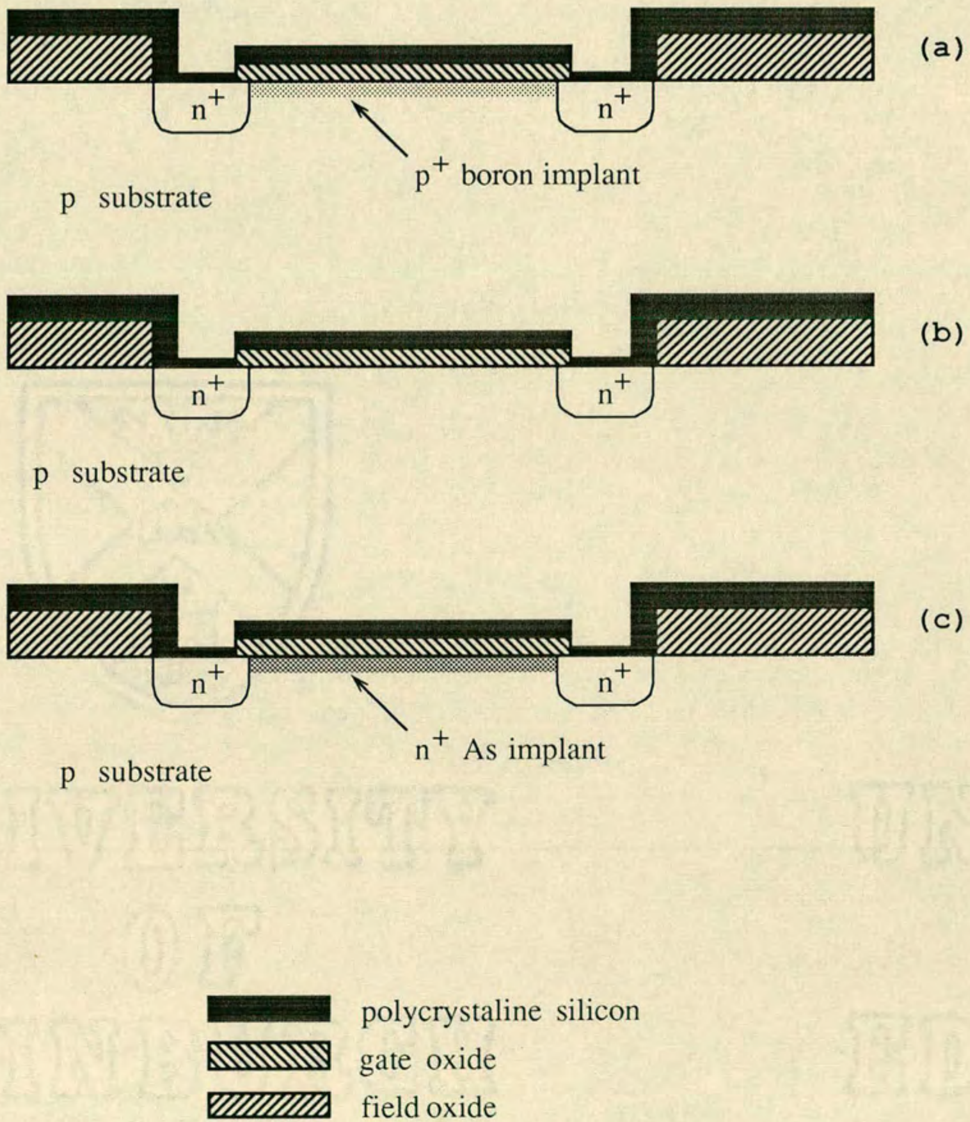



Figure A.1: Schematic cross section of $n$-channel MOS transistors. Enhancement mode (a), intrinsic (b), and depletion mode (c).

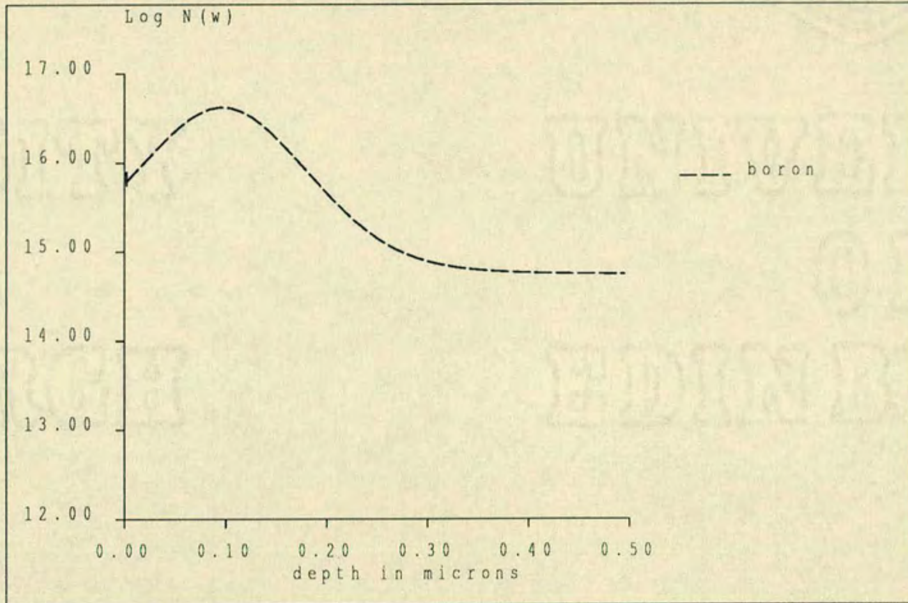



Figure A.2: ICECREM profile for enhancement mode MOS transistor. $N(w)$ is the doping concentration at depth $w$.

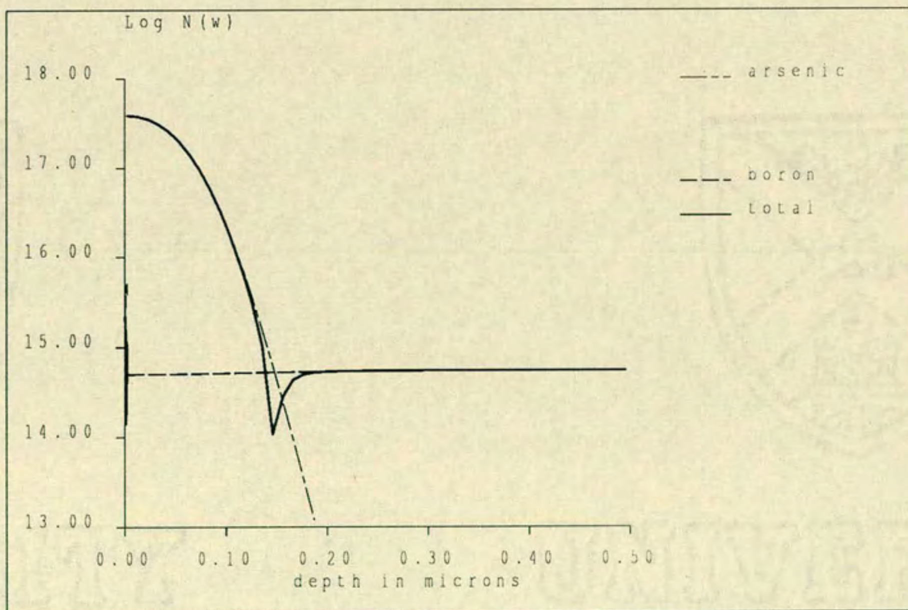



Figure A.3: ICECREM profile for depletion mode MOS transistor.

considering the long drive-in time. The depth can be explained by considering the low diffusivity, $D$ of arsenic in silicon [1] when compared with boron or phosphorus. At 900 °C, $D$ is $5 \times 10^{-17}$ $cm^2s^{-1}$ for arsenic, whereas $D$ is $1 \times 10^{-15}$ $cm^2s^{-1}$ for boron and $3 \times 10^{-16}$ $cm^2s^{-1}$ for phosphorus.

After the enhancement or depletion profiles had been defined by implantation and drive-in the source and drain contacts were fabricated. Phosphorus was diffused from an $n^+$ region deposited in the areas where source and drain contacts were to be formed. This $n^+$ deposition came from $POCl_3$ gas. A 950 °C drive-in for 60 minutes gave a diffusion depth of around 0.1 $\mu m$.

## A.3 Low Frequency Noise in Enhancement Mode MOS Transistors

In this section the noise behaviour in enhancement mode MOS transistors is examined.

Initially, the low frequency noise behaviour is investigated when the device is biased well into the linear region and the channel behaves like a purely resistive element. This can be achieved by using a small drain voltage, or a large positive gate voltage. Here the latter method is chosen, using a gate voltage of 5 $V$. Figure A.4 shows the spot noise at 10 $Hz$ dependence on drain current for an enhancement mode transistor with a designed channel length of 15 $\mu m$ and width of 100 $\mu m$. Note that since we are in the linear region of device operation, the horizontal axis could equally well have been drain voltage. A linear dependence of noise on drain voltage is seen when the device is biased in this region. This is is good agreement with models developed by many authors, including Kandiah [5] and Vandamme [92].

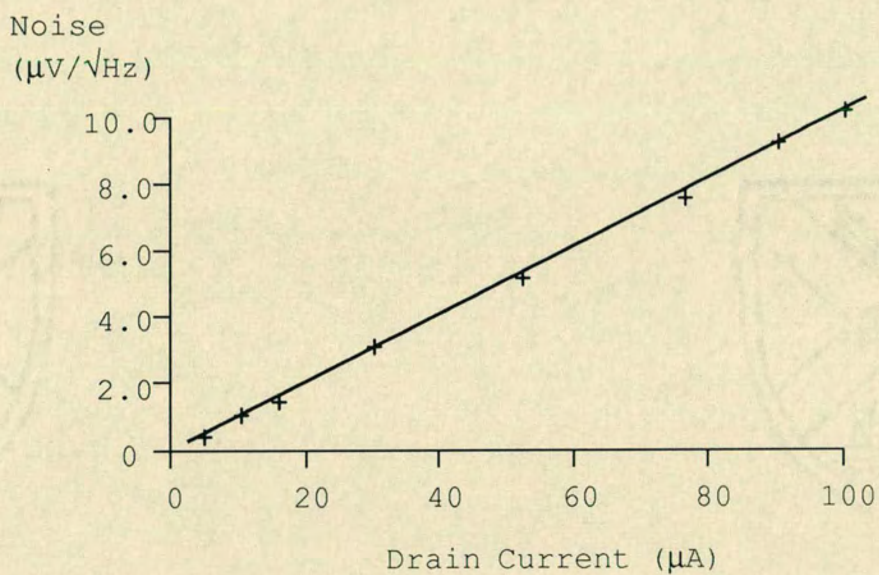



Figure A.4: Spot noise at 10 $Hz$ dependence on drain current in enhancement mode MOS transistor. $V_{GS} = 5\ V, V_{BS} = 0\ V$.

We now consider the noise performance when the device is biased at a range of operating points from the linear region through to saturation. Figure A.5 shows a number of measured noise spectra for an enhancement mode MOS transistor with a channel length of 15 $\mu m$ and width of 100 $\mu m$, as above. The gate voltage and substrate bias were kept constant, and the drain voltage increased in order to observe noise performance as the device changed from being biased in the linear region, through 'triode' operation, and into saturation mode.

With reference to Figure A.5, it can be seen that as $V_{DS}$ is increased then the low frequency part of the noise spectrum also increases. As the device enters saturation, the noise characteristic also appears to saturate. To clarify this observation, Figure A.6 (A) shows the drain voltage characteristics for the same bias points used for the noise spectra, and Figure A.6 (B) shows the 'spot' noise as detected by the 10 $Hz$ filter at each of these drain voltages[†].

Figure A.6 (B), showing the low frequency spot noise dependence on drain voltage, $V_{DS}$, can be divided into three regions. At drain voltages below 300 $mV$ for this gate bias, a linear dependence of noise on drain voltage is observed, as in Figure A.4. The transistor is biased in the linear region for drain voltages in this range, see Figure A.6 (A). At drain voltages between 300 $mV$ and 600 $mV$ the noise increases rapidly with drain voltage. This corresponds to the device biased in the 'triode' region [93]. At higher drain voltages the noise does indeed appear to saturate as the device enters saturation. Similar results are shown for a buried channel mode MOS transistor

[†]**Note that two additional data points in the saturation region are included in Figure A.6. These were omitted from Figure A.5 to aid clarity.**

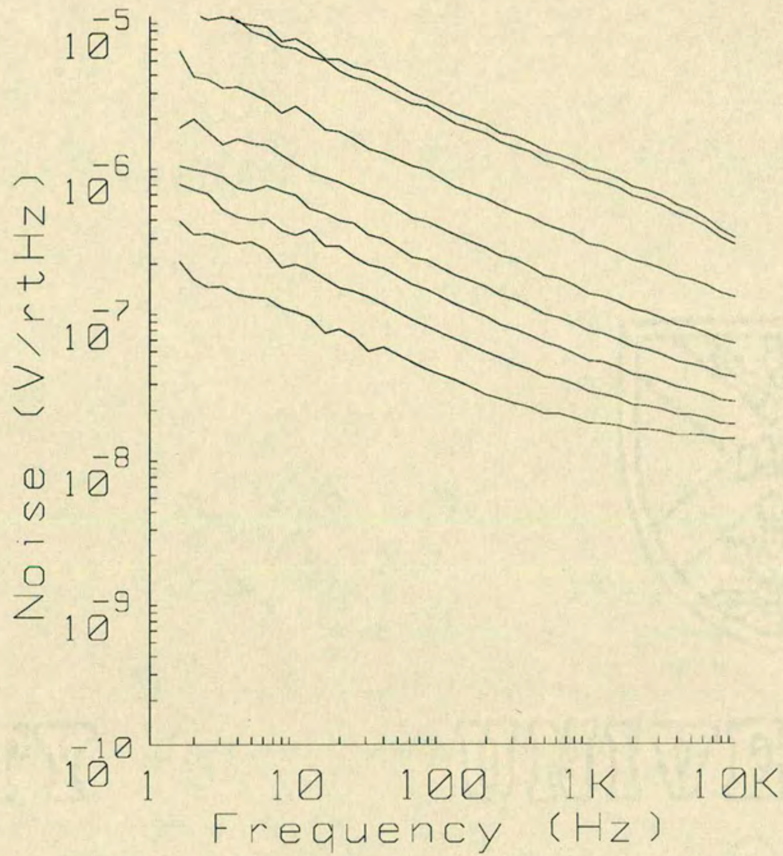



Figure A.5: Noise spectra for enhancement mode MOS transistor at 300 $K$. $V_{GS} = 1.59\ V, V_{BS} = 0\ V$.

| *top plot* | $V_{DS} = 0.80\ V$ | $I_{DS} = 27.5\ \mu A$ |
|---|---|---|
| ⋮ | $V_{DS} = 0.60\ V$ | $I_{DS} = 27.1\ \mu A$ |
| ⋮ | $V_{DS} = 0.40\ V$ | $I_{DS} = 25.3\ \mu A$ |
| ⋮ | $V_{DS} = 0.30\ V$ | $I_{DS} = 22.4\ \mu A$ |
| ⋮ | $V_{DS} = 0.20\ V$ | $I_{DS} = 17.4\ \mu A$ |
| ⋮ | $V_{DS} = 0.15\ V$ | $I_{DS} = 14.0\ \mu A$ |
| ⋮ | $V_{DS} = 0.10\ V$ | $I_{DS} = 10.0\ \mu A$ |
| *bottom plot* | $V_{DS} = 0.05\ V$ | $I_{DS} = 5.4\ \mu A$ |

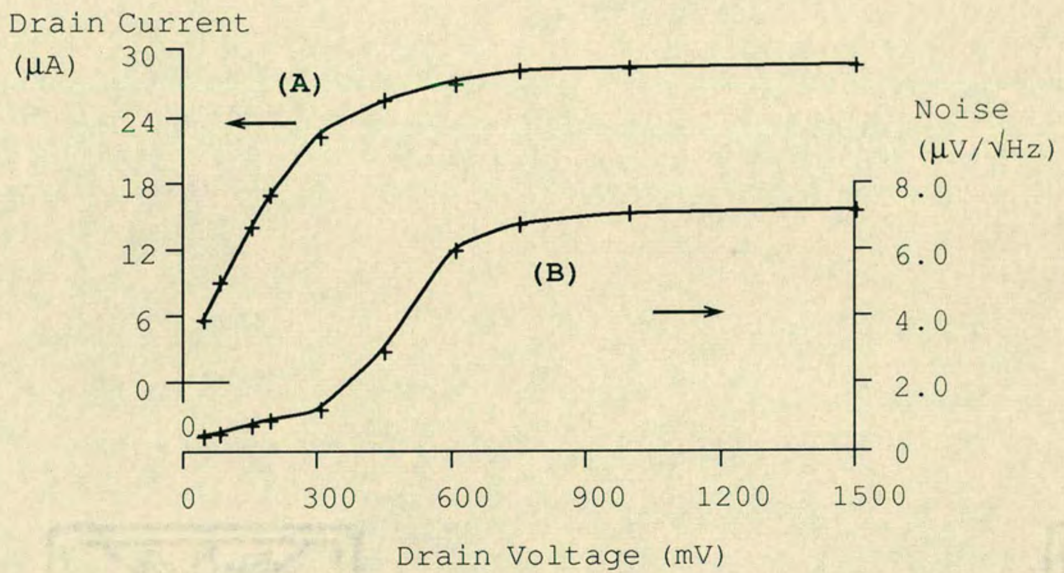



Figure A.6: Drain current (A) and spot noise at 10 $Hz$ (B) variation with drain voltage for an enhancement mode transistor. $V_{GS} = 1.59\ V, V_{BS} = 0\ V$.

in reference [94].

These results are significant because, as can be seen by comparing Figure A.6 (A) and Figure A.6 (B) the drain current increases and begins to saturate before there is a rapid increase in noise with drain voltage. For example, at a drain voltage of 450 $mV$ for this sample, the device output conductance, $g_{ds}$, is 7.42 $\mu A/V$ giving a $1/g_{ds}$ of approximately 135 $k\Omega$, and the 10 $Hz$ noise is around 3 $\mu V/\sqrt{Hz}$ compared with its saturation value of approximately 7 $\mu V/\sqrt{Hz}$. Designers of specific circuit elements may be able to use this finding to improve device performance while maintaining acceptable circuit parameters.

It is generally accepted [5, 95, 96] that low frequency noise *power* shows a reciprocal dependence on device area. This dependence was seen in measurements on enhancement mode MOS transistors designed with square gate geometries. Figure A.7 shows the noise power plotted against the reciprocal of area.

Finally in this section the effects of operation at lower temperatures will be discussed. Operation at temperatures lower than ambient can lead to improved device performance, particularly in enhancement mode MOS transistors [27, 97, 98, 99]. In Chapter 2 it was shown that reducing the device temperature from room temperature to 77 $K$ (liquid nitrogen temperature) should lead to a reduction in thermal noise voltage by a factor of around two. This figure is actually 1.97 for a room temperature of 300 $K$. Figure A.8 compares the noise characteristics of a 100 $\mu m$ by 15 $\mu m$ transistor biased in the linear region at 300 $K$ (curve A) and 77 K (curve B). The thermal noise voltage floor above 10 $kHz$ shows the expected reduction. A reduction in the low frequency noise is also observed. Results on samples from the same

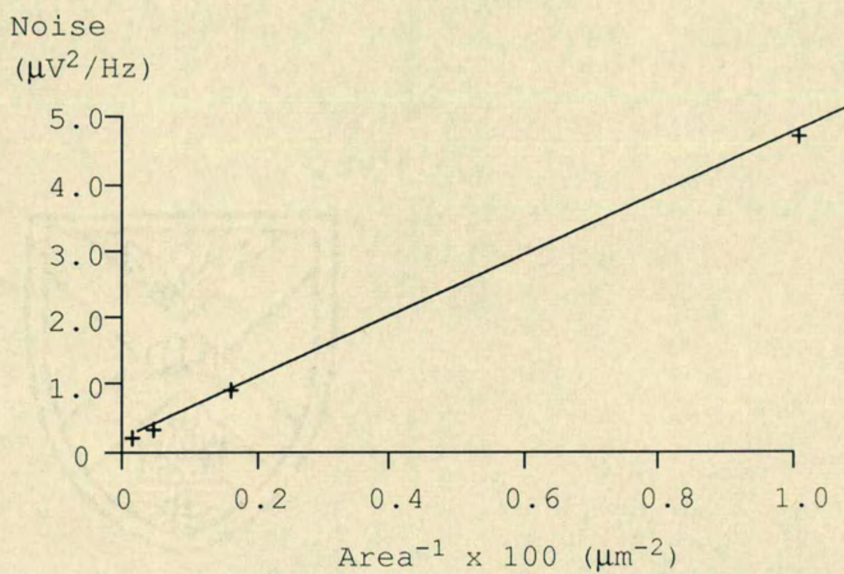



Figure A.7: Noise power variation with 1/area for enhancement mode MOS transistor. $V_{DS} = 0.2\ V, V_{BS} = -4.5\ V, T = 77\ K$. A similar dependence is seen at room temperature.

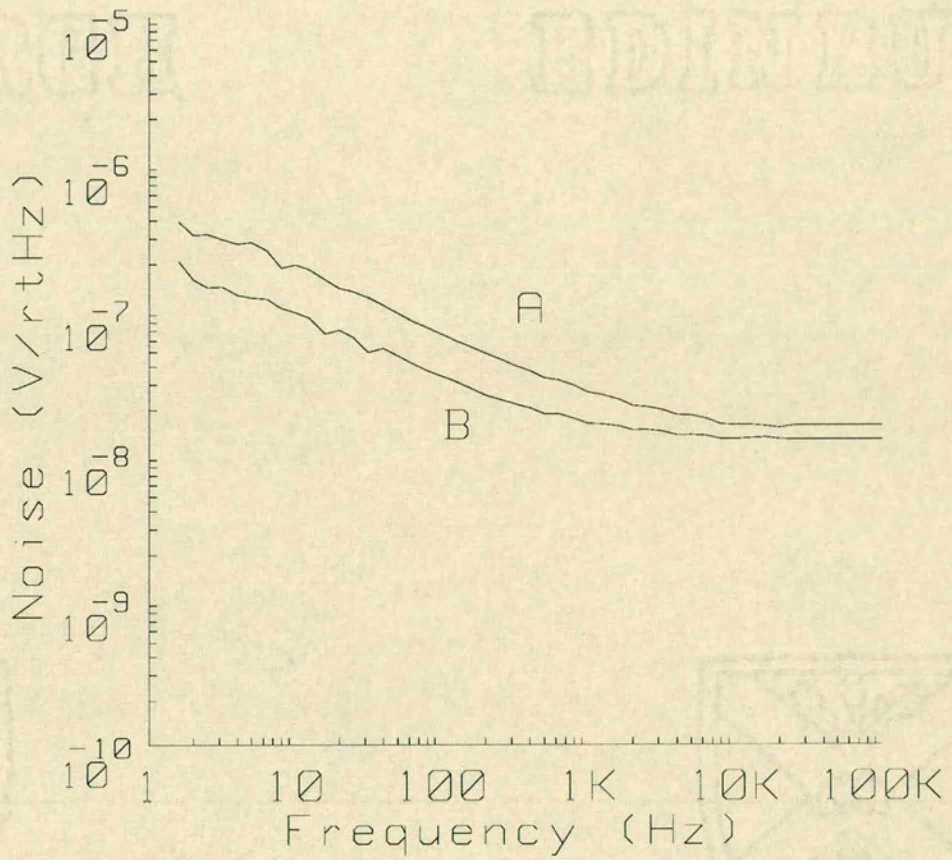



Figure A.8: Enhancement mode MOS transistor at 300 $K$ (A) and 77 $K$ (B).

fabrication batch measured by K. Kandiah using the ACUMENS system at the Atomic Energy Research Establishment (A.E.R.E) in Harwell [62] show a similar dependence [70]. A more extensive comparison of the experimental results obtained for this thesis and complementary results obtained by Kandiah can be found in Appendix B.

## A.4 Low Frequency Noise in MOS Transistors with no Threshold Implant

The 'intrinsic' surface channel MOS transistors examined here were fabricated on exactly the same wafers as the enhancement mode structures described above. An extra mask was introduced to selectively block the boron threshold implant from some devices on the test chip. In this way it was possible to compare characteristics of enhancement and intrinsic MOS transistors which had been subjected to exactly the same process conditions in terms of oxide growth, annealing, polycrystalline silicon deposition, and other steps.

Extensive measurements on the two types of device have revealed very little difference in either the d.c. or noise characteristics once adjustments have been made for the shift in threshold voltage. By means of illustration, Figure A.9 shows noise spectra for a 100 $\mu m$ by 15 $\mu m$ MOS transistor with no boron threshold implant. The bias conditions are identical to those for the enhancement transistor shown in Figure A.5, except for a negative gate voltage shift of around 1.2 $V$. to compensate for the difference in threshold voltage. By comparing Figure A.9 with Figure A.5 we see that the noise characteristics are indeed very similar. The close correlation between the

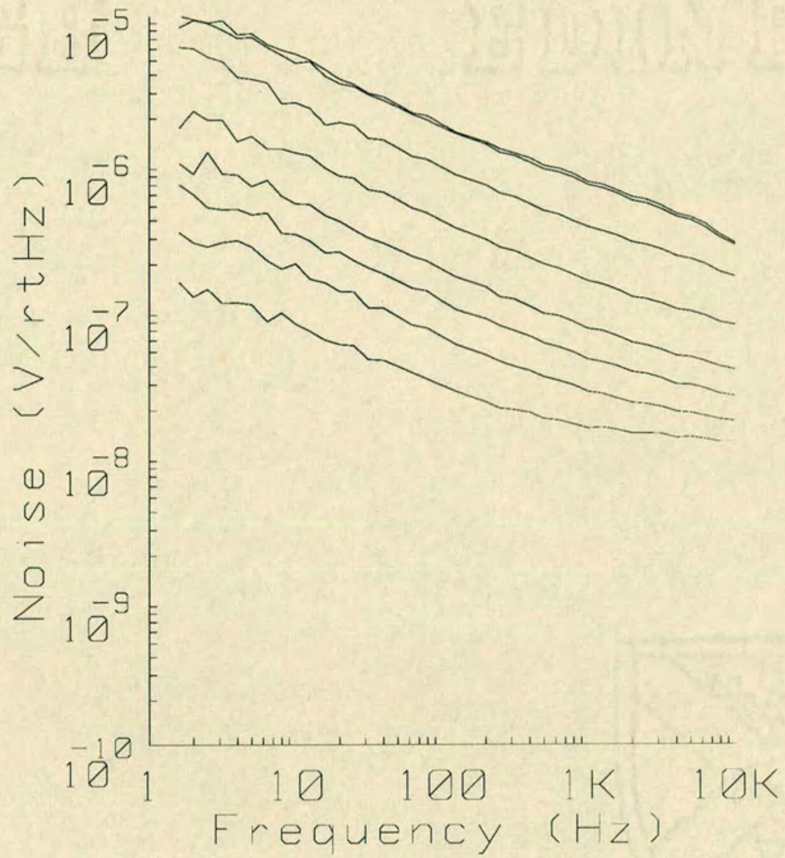



Figure A.9: Noise spectra for 'intrinsic' enhancement mode MOS transistor at 300 $K$. $V_{GS} = 0.4\ V, V_{BS} = 0\ V$.

| *top plot* | $V_{DS} = 0.80\ V$ | $I_{DS} = 25.8\ \mu A$ |
|---|---|---|
| ⋮ | $V_{DS} = 0.60\ V$ | $I_{DS} = 25.4\ \mu A$ |
| ⋮ | $V_{DS} = 0.40\ V$ | $I_{DS} = 24.5\ \mu A$ |
| ⋮ | $V_{DS} = 0.30\ V$ | $I_{DS} = 22.5\ \mu A$ |
| ⋮ | $V_{DS} = 0.20\ V$ | $I_{DS} = 18.1\ \mu A$ |
| ⋮ | $V_{DS} = 0.15\ V$ | $I_{DS} = 14.7\ \mu A$ |
| ⋮ | $V_{DS} = 0.10\ V$ | $I_{DS} = 10.6\ \mu A$ |
| *bottom plot* | $V_{DS} = 0.05\ V$ | $I_{DS} = 5.7\ \mu A$ |

two types of device is seen in all bias, geometry and temperature dependences. It is concluded from these measurements that any damage due to the boron implant remaining after the anneal does not adversely influence the noise performance. This is a significant result because it would be difficult to increase the anneal time further due to the high solubility of boron in silicon-silicon dioxide. Already in Figure A.2 a reduction in the boron concentration can be seen at the surface due to boron being drawn into the oxide during subsequent high temperature processing steps. With additional high temperature treatment then the boron level at the surface would be further reduced, and the effectiveness of the implant controlling the threshold voltage would be reduced.

The nature of silicon crystal growth naturally leads to fluctuations in the substrate doping [10]. It is concluded from these experiments that the boron implantation step should be retained to provide a degree of threshold voltage control with no degradation in noise performance. It should be emphasised that these conclusions can only be applied to the Philips Southampton process where the devices were fabricated.

## A.5 Low Frequency Noise in Depletion Mode MOS Transistors

The noise characteristics of depletion mode MOS transistors are now presented. It will be shown that the noise behaviour of depletion mode transistors is substantially different from the enhancement mode structures described above. In Chapter 3 it was observed that in depletion and deep depletion mode devices it was possible to set the gate voltage and substrate

bias so that the majority of the charge forming the channel was isolated from the surface. By controlling the bias in this way, it is possible to see what influence channel proximity to the surface has on device noise characteristics.

Figure A.10 shows the noise spectra for a 100 $\mu m$ by 15 $\mu m$ depletion mode MOS transistor. Once again, the bias conditions are identical to those used for the enhancement and intrinsic MOS transistors in Figure A.5 and Figure A.9 with an appropriate shift in the gate voltage to compensate for the negative threshold voltage. Comparing Figure A.10 with Figure A.5 and Figure A.9 it can be seen that the spectra for the depletion mode device are completely different. Instead of the $1/f^n$ type of dependence observed in the case of the enhancement and intrinsic MOS transistors, we see a Lorentzian type distribution with some characteristic time constant, $\tau_o$. This gives a flat plateau at frequencies below $1/\tau_o$ and a steep roll-off at frequencies above $1/\tau_o$. The slope of this steeper section of the spectra is close to $1/f^2$, but this gradient is reduced where the noise characteristic meets the thermal noise floor.

Figure A.11 (A) shows the drain characteristic for the device, and Figure A.11 (B) shows the spot noise at 10 $Hz$ as a function of drain voltage. Once again, the data points in Figure A.11 are drawn from the same set of results as the data in Figure A.10. As in the case of enhancement mode MOS transistors, the drain current is observed to saturate *before* the low frequency noise reaches a maximum. A drain voltage of 600 $mV$ would result in a $g_{ds}$ of 1.42 $\mu A/V$, giving a $1/g_{ds}$ of 106 $k\Omega$, with a noise voltage, $v_n$, of around 7 $\mu V/\sqrt{Hz}$ at 10 $Hz$. These parameters are both inferior to those for the enhancement structure described in section A.3. This is due to the 'softer' characteristics seen in depletion mode MOS transistors [19], and is

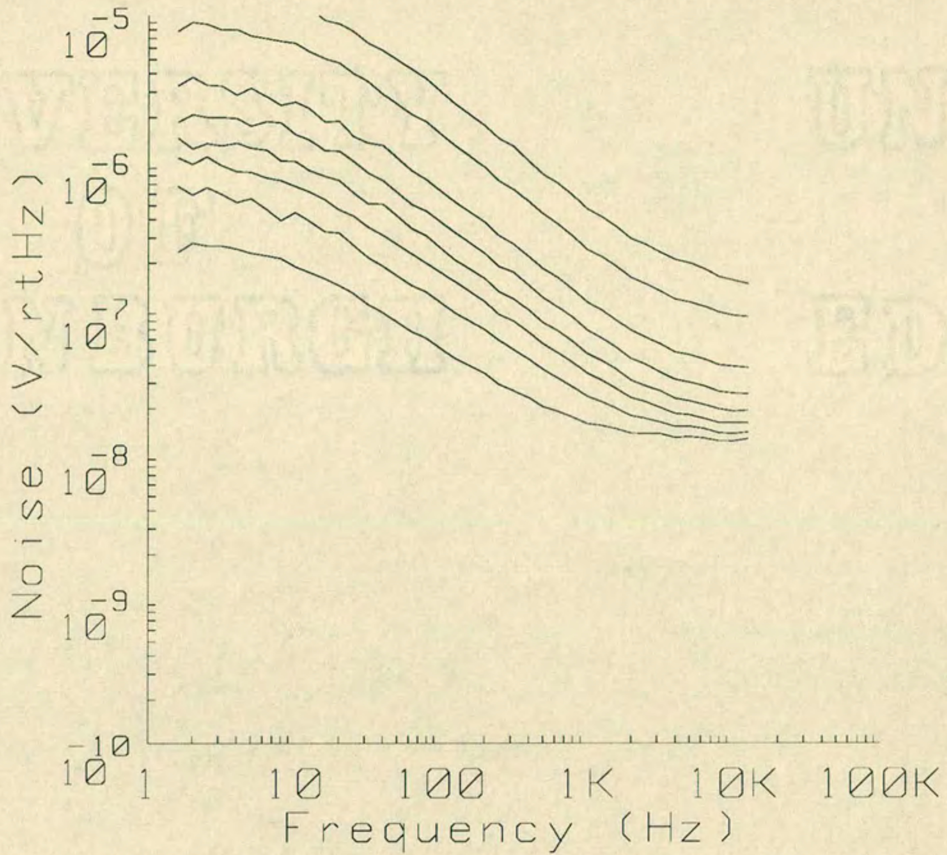



Figure A.10: Noise spectra for depletion mode MOS transistor at 300 $K$. $V_{GS} = -3.09\ V, V_{BS} = -5.0\ V$.

| | | |
|---|---|---|
| *top plot* | $V_{DS} = 0.80\ V$ | $I_{DS} = 37.1\ \mu A$ |
| ⋮ | $V_{DS} = 0.60\ V$ | $I_{DS} = 34.8\ \mu A$ |
| ⋮ | $V_{DS} = 0.40\ V$ | $I_{DS} = 28.8\ \mu A$ |
| ⋮ | $V_{DS} = 0.30\ V$ | $I_{DS} = 23.9\ \mu A$ |
| ⋮ | $V_{DS} = 0.20\ V$ | $I_{DS} = 17.7\ \mu A$ |
| ⋮ | $V_{DS} = 0.15\ V$ | $I_{DS} = 13.8\ \mu A$ |
| ⋮ | $V_{DS} = 0.10\ V$ | $I_{DS} = 9.6\ \mu A$ |
| *bottom plot* | $V_{DS} = 0.05\ V$ | $I_{DS} = 5.0\ \mu A$ |

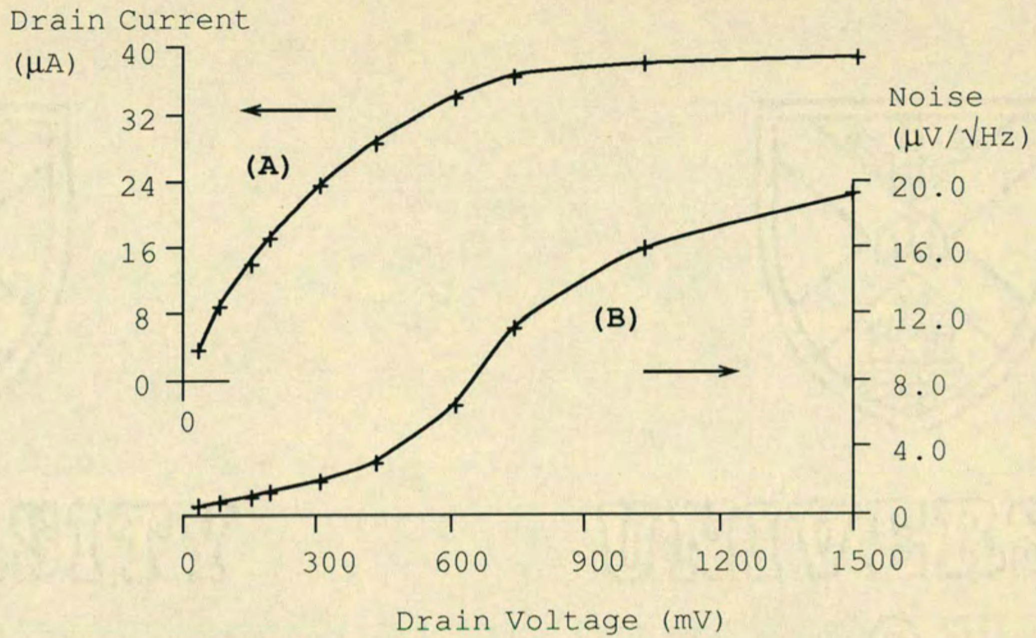



Figure A.11: Drain current (A) and noise voltage at 10 $Hz$ (B) dependence on drain voltage in depletion mode MOS transistor. $V_{GS} = -3.09\ V, V_{BS} = -5.0\ V$.

caused by the spatial distribution of charge forming the channel.

Figure A.12 shows two noise spectra for a depletion mode MOS transistor. In this case, *both* the drain voltage and drain current were kept constant, and the gate voltage and substrate bias adjusted simultaneously. As the gate voltage was made more negative and the substrate bias increased to maintain the drain current the characteristic shape of the noise spectrum changed. In Figure A.12 (A), the gate voltage is -1.61 $V$ and the substrate bias $-2.0\ V$. In Figure A.12 (B), the gate voltage is made more positive ($-1.06\ V$) and the substrate more negative ($-9.42\ V$). Under this latter bias condition the conducting channel is predicted to be touching the interface and a 'classical' $1/f$ type of spectrum is observed.

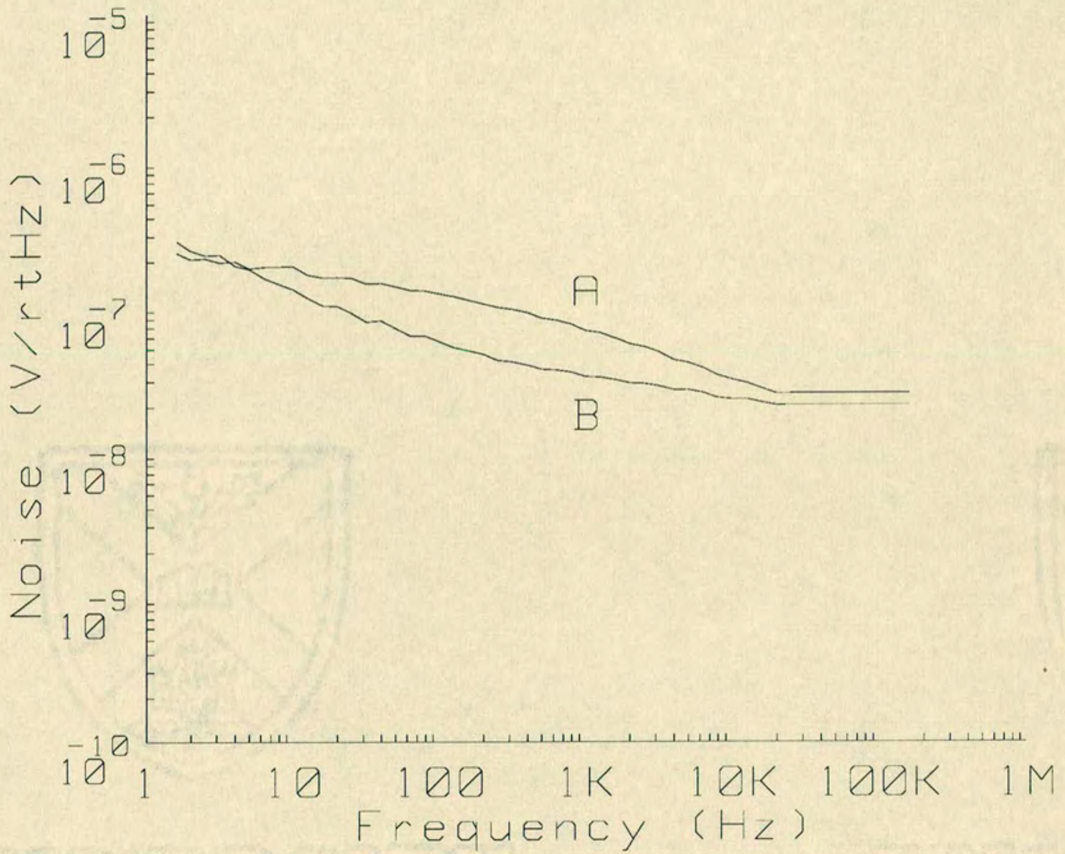



Figure A.12: Noise spectra under bulk conduction (A) and surface conduction (B) in depletion mode transistor. $V_{DS} = 1.0\ V, I_{DS} = 282.0\ \mu A$.

| (A) | $V_{GS} = -1.61\ V$ | $V_{BS} = -2.00\ V$ |
|---|---|---|
| (B) | $V_{DS} = -1.06\ V$ | $V_{BS} = -9.42\ V$ |

# Appendix B

# Comparison with Kandiah's Results

This appendix considers measurements made by K. Kandiah on devices similar to the MOS transistors measured here. In some cases the devices are in fact the identical transistors. Kandiah's measurements were performed using the ACUMENS system at A.E.R.E. Harwell [62].

Note that ACUMENS measures *equivalent* gate input noise voltage. It was observed in Section 4.1 that with this technique the noise voltage must be related back to mechanisms in the channel through the device transconductance, $g_m$, since the gate noise is coupled to the channel noise current *via* this parameter. In order to compare Kandiah's results with the results in the thesis it is first necessary to convert his equivalent noise voltages into *absolute* noise voltages by considering both the transconductance, $g_m$, and the channel conductance, $g_{ds}$, for the device under test. A summary of Kandiah's most important results is now presented.

- For enhancement mode MOS transistors biased in strong inversion, the

measured low frequency noise is not a strong function of drain voltage, drain current, substrate bias, or temperature.

- For depletion mode devices, the noise is at a minimum for temperatures between about 120 $K$ and 140 $K$. This minimum is similar to that seen in JFETS [100, 101].

- Kandiah observes an increase in noise in depletion mode devices as the substrate bias is decreased (*i.e.* made more negative), see Figure B.1. The bias network employed by ACUMENS will automatically increase the gate voltage to maintain the selected drain current. This is consistent with results here since increasing the substrate bias has the effect of pushing the channel towards the silicon-silicon dioxide interface.

A complete comparison of all Kandiah's results is not possible since the ACUMENS system is designed primarily for devices biased into the saturation mode. The system developed in this research for noise measurements is best employed with MOS transistors biased in the linear and triode (or near saturation) regions. In saturation mode, a high value for $1/g_{ds}$ means that the noise voltage developed across the channel is effectively 'shorted out' by the input impedance of the amplifier. A degree of overlap did prove possible, however, and a direct comparison of results obtained on the two measurement systems has been performed.

Figure B.2 shows the noise in an enhancement mode MOS transistor at a number of frequencies for a range in temperature. Note that this plot illustrates the weak dependence of noise on temperature in enhancement mode devices. Figure B.3 shows the noise spectrum measured at liquid nitrogen temperature (77 K) on the same transistor using the apparatus described

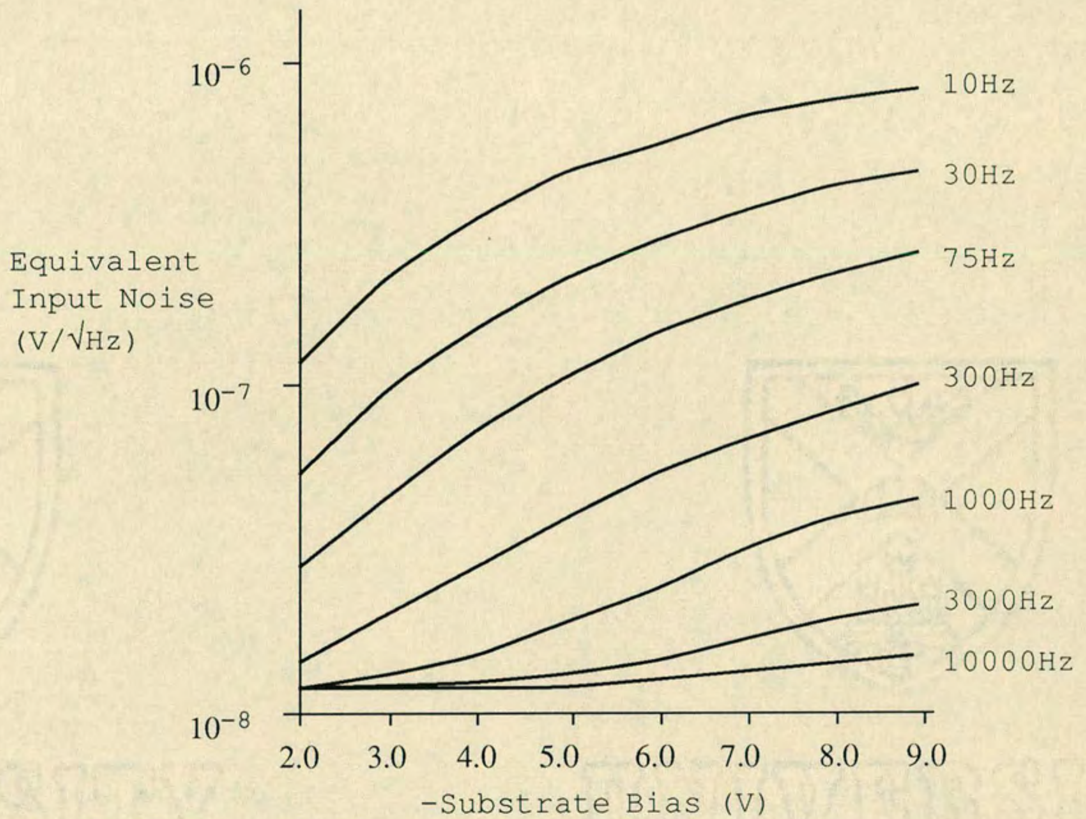



Figure B.1: Noise in depletion mode MOS transistor as measured by Kandiah on ACUMENS [70]. $T = 129.1\ K$, $I_{DS} = 300\mu A$, $V_{DS} = 2\ V$.

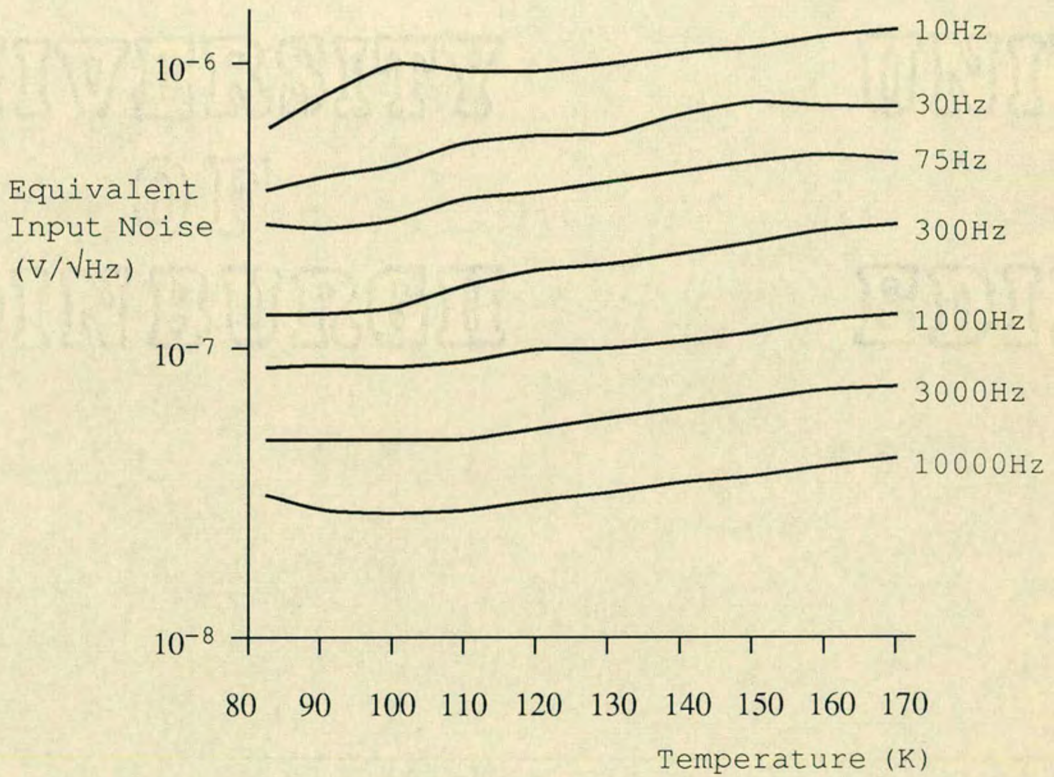



Figure B.2: Noise in enhancement mode MOS transistor as measured by Kandiah on ACUMENS [70]. $I_{DS} = 300\mu A$, $V_{DS} = 2\ V$, $V_{BS} = -2\ V$.

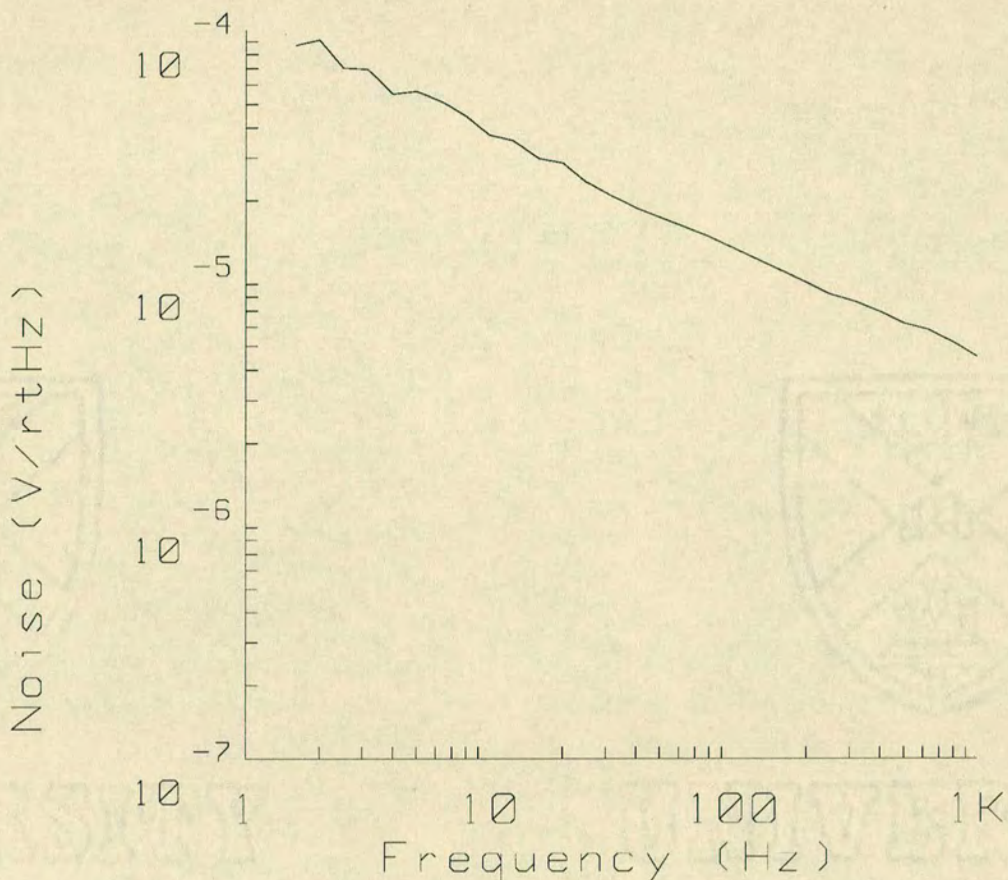



Figure B.3: Noise in enhancement mode MOS transistor at 77 $K$.

$I_{DS} = 300\mu A$, $V_{DS} = 2\ V$, $V_{BS} = -2\ V$.

in Chapter 4. Although the two sets of data are at different temperatures (77 K and 80 K) a comparison between these two graphs is valid since Figure B.2 shows that there is little dependence of the low frequency noise on temperature.

Now, the noise as measured by the 10 $Hz$ filter at 80 $K$ in Figure B.2 is around 0.55 $\mu V/\sqrt{Hz}$. In Figure B.3, the noise at 10 $Hz$ is around 40 $\mu V/\sqrt{Hz}$. In order to compare these results it is necessary to convert the former from an equivalent noise voltage to an absolute noise voltage. To recap, the absolute noise voltage, $v_n$, can be found from the equivalent noise

voltage, $v_{eq}$, using

$$v_n = v_{eq} \frac{g_m}{g_{ds}} \tag{B.1}$$

Further, the transconductance, $g_m$ of this device at liquid nitrogen temperature and operating point is 140 $\mu A/V$, and the conductance is 2.5 $\mu A/V$. Using this relationship, Kandiah's result yields an absolute voltage of 30.8 $\mu V/\sqrt{Hz}$ at 10 $Hz$. This is within 25 % of the result in Figure B.3.

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# Relevant Publications

A total of three external papers were published during the course of the research for this thesis. These papers are reproduced on the pages which follow.

The first [88] reports the anomalous oscillation seen in depletion and deep depletion mode MOS transistors at temperatures lower than ambient.

The second [49] presents the most important results in Chapter 5. The paper shows that by careful choice of bias point the low frequency noise in s deep depletion mode MOS transistor may be reduced by careful choice of operating point.

The final paper [89] was an invited paper presented at the meeting of the Electrochemical Society of America in Hawaii. The paper gives an overview of noise mechanisms in MOS transistors with the emphasis on low temperature operation. Low noise operation in deep depletion mode MOS devices is discussed.

# ANOMALOUS OSCILLATION IN DEPLETION-MODE MOSFETs AT LOW TEMPERATURE

*Indexing terms: Semiconductor devices and materials, MOS devices, FETs*

Results are presented which show unusual behaviour in silicon, *n*-channel depletion-mode MOSFETs having phosphorus doping. At 77 K these devices exhibit a low-frequency oscillation whereby the MOSFET channel periodically turns high resistance for a short period.

*Introduction:* The operation of MOSFET analogue circuits at low temperature yields improved bandwidth and reduced thermal noise.[1,2] Parameters such as saturation current and transconductance for enhancement-mode devices are increased due to carrier mobility improvements.

There are many applications for low-temperature analogue MOS circuits. One such application is in the design of interface circuits for use with infra-red detection systems where the entire assembly is cooled, for example, to liquid nitrogen temperature.[3]

Conventional surface-channel MOS structures are too noisy for use as components in circuits of this kind. Interaction between charge carriers and surface states near the silicon/silicon dioxide interface increases low-frequency (or flicker) noise.[4]

Depletion-mode devices offer potentially superior noise performance at low temperature, since the conducting channel can be made to form away from the interface.[5,6] This is due to donor atoms such as phosphorus or arsenic 'freezing out' close to the surface. The degree of freeze-out is controlled not only by temperature, but also by band-bending due to applied gate voltage and substrate bias.

*Measurements and discussion:* Devices in these experiments were cooled by immersing them in liquid nitrogen (77 K), oxygen (90 K) or Freon (196 K). The samples were enclosed in sealed packages to keep the coolant away from the surface.

Fig. 1*a* shows a noise spectrum plot for an *n*-channel, boron-doped, silicon, enhancement-mode MOSFET at liquid nitrogen temperature biased in the linear region. The slope of the low-frequency section of the plot is close to $-1/2$, showing that the noise power is proportional to $1/f$. Our results have shown that the operation of *n*-channel enhancement devices at any temperature down to 77 K would not offer any significant improvement in low-frequency noise performance.

Fig. 1*b* shows the noise spectrum for a phosphorus-doped, depletion-mode MOSFET biased in the linear region at liquid nitrogen temperature. Superimposed on the $1/f$ noise region there is a broadband feature containing structure at around 12 Hz. Fig. 2 shows an oscilloscope trace showing the AC component of drain-source voltage on the same device. The device was operated in a constant-current configuration, so the spikes in the time domain reflect an increase in channel resistance. The frequency of oscillation is not at all coherent, and at times can be quite erratic. An increase in temperature, however, gives an increase in frequency of this anomalous effect. For this sample, the frequency of oscillation moved from around 12 Hz to 80 Hz when the temperature was raised from 77 K to 90 K.

The period is independent of drain and gate bias, but the magnitude is a strong function of drain current. At zero drain bias, the oscillation cannot be detected. As the drain current is increased, then so does the magnitude of the peak. At threshold voltage and below, the peak is lost in the thermal noise of the channel.

The oscillation has not been observed in depletion-mode devices at 196 K or room temperature, nor has it been observed in $n$-channel enhancement devices at any temperature.

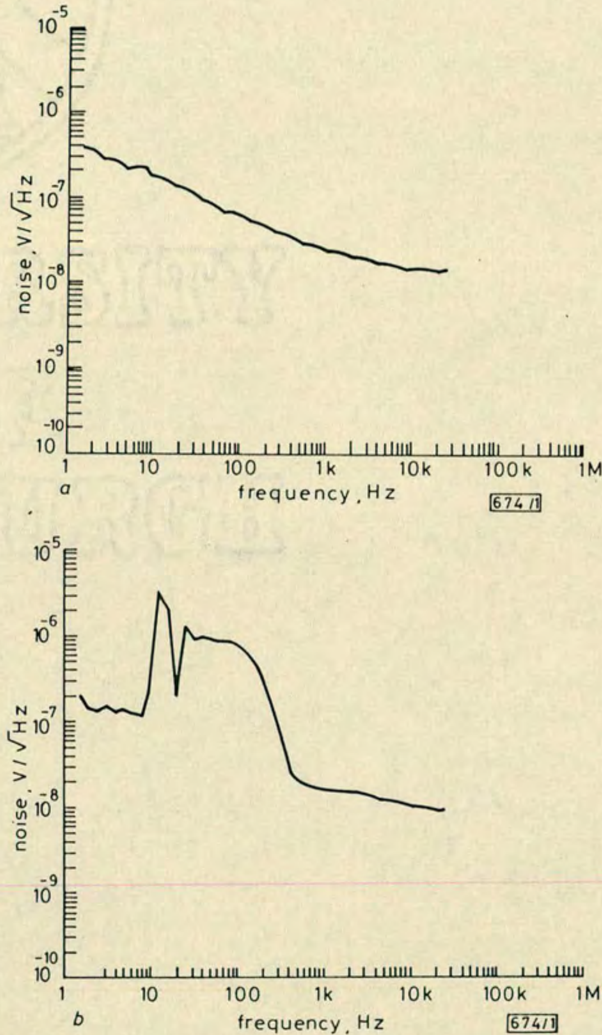


**Fig. 1**

*a* Noise characteristic of enhancement-mode MOSFET at 77 K
*b* Noise characteristic of depletion-mode MOSFET at 77 K

It is difficult to conceive of a physical mechanism which could account for this phenomenon. One possible explanation is as follows.

If for some reason the ionised donors in the channel region were to suddenly freeze out, then this would have the effect of increasing the channel resistance. To maintain the drain current, the constant-current bias supply would increase the drain voltage to compensate. The resulting increased power consumption would heat the channel region of the MOSFET. This would in turn reionise the frozen-out donors, and pseudo-equilibrium would be restored.

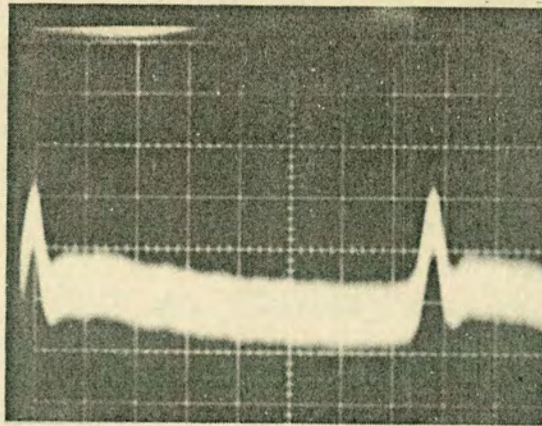


**Fig. 2** *Oscilloscope trace showing anomalous voltage oscillation*
10 ms/div, 50 $\mu$V/div

If the oscillation were caused by a thermal effect of this kind, then one might expect the frequency to be a function of device power consumption. Measurements to date have failed to show any such power dependence.

No references to oscillations of this kind in silicon have been found in the literature. However, Canfield and Forbes[7] have presented results showing a very similar effect in GaAs MISFETs at room temperature.

Future experimental work will include measurements over a wide range of temperatures by placing samples in a variable-temperature nitrogen cryostat.

*Conclusions:* Phosphorus-doped MOSFET devices can exhibit an anomalous low-frequency oscillation at low temperatures. The physical mechanism appears obscure, and further work to establish the nature of the effect is being undertaken.


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C. CARRUTHERS *8th December 1986*
J. MAVOR

*Department of Electrical Engineering*
*University of Edinburgh*
*The King's Buildings*
*Mayfield Road, Edinburgh EH9 3JZ, United Kingdom*


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7 CANFIELD, P., and FORBES, L.: 'Gate-bias-dependent low-frequency oscillations in GaAs MISFETs', *IEEE Electron Device Lett.*, 1985, **EDL-6**, pp. 227–228

# LOW-NOISE OPERATION OF BURIED CHANNEL MOS TRANSISTORS

*Indexing terms: Semiconductor devices and materials, Transistors, MOS structures and devices*

Results are presented which show that extremely low-noise performance is possible in buried *n*-channel transistors. By careful choice of operating point, low-noise operation with useful gain is possible. The use of these devices as circuit elements is discussed.

*Introduction:* By implanting impurities into the surface region of a MOS transistor of a type complementary to that of the substrate, a 'buried' conducting channel may be formed away from the high trap density associated with the silicon/silicon dioxide interface.[1] Many authors[2,3] have reported significant improvements in noise performance possible when using buried channel MOS transistors. Results presented here confirm that the characteristics of the output noise are very strongly dependent on device bias conditions, particularly gate voltage and substrate potential. Moreover, by careful choice of operating conditions, a low-noise regime has been identified at which the spot noise measured at the output is equivalent to a root-mean-square voltage of $30\,nV/\sqrt{(Hz)}$ at 10 Hz. The results will be of particular interest to designers of low-noise analogue circuits employing MOS technology.

*Experimental details:* The buried channel transistors used in these experiments were fabricated on a *p*-type $20\,\Omega$cm, $\langle 100 \rangle$ substrate. An *n*-type well was formed by implanting phosphorus ions into the silicon at an energy of 80 keV and a total dose of $7{\cdot}2 \times 10^{11}$ atoms/cm$^2$. A 24 h drive-in at 1050°C gave a metallurgical junction depth of $2{\cdot}85\,\mu$m and a donor concentration of $5{\cdot}2 \times 10^{15}$ atoms/cm$^3$ at the silicon/silicon dioxide interface. Buried channel devices were formed by implanting an arsenic source and drain into this *n*-well. Results presented here are for devices of $100 \times 15\,\mu$m and a gate oxide thickness of 750 Å.

Noise measurements were performed using a Brüel & Kjœr digital frequency analyser type 2131 with a Brookdeal 5004 preamplifier. Transistors were biased using a simple battery power supply, and absolute noise was measured across the channel. A Hewlett-Packard 4145 semiconductor parameter analyser was used to obtain the DC characteristics.

*Experimental results:* For positive gate voltages, the conducting channel forms such that it is close to or touching the silicon/silicon dioxide interface. The observed noise behaviour is similar to that measured for an enhancement (surface channel) transistor.* We now investigate what happens to noise performance when the channel is formed away from the interface.

Fig. 1 shows the noise spectra for a saturated $100 \times 15\,\mu$m gate area buried channel device under three different gate voltages ($V_{GS}$) and substrate bias points ($V_{BS}$). Drain voltage and current were kept constant. It can be seen that as $V_{GS}$ was made more negative (and $V_{BS}$ made more positive to maintain the drain current), the characteristics of the transistor noise change considerably.

* KANDIAH, K.: 'Low frequency noise measurements in field effect transistors'. Department of Electronics, University of Southampton, to be published

Fig. 1$a$ is typical of the observed spectrum over a wide range of $V_{GS}/V_{BS}$ values. The characteristic is dominated by a time constant of around 100 ms, giving a plateau below 10 Hz and a sharp roll-off above this frequency. At frequencies above 5 kHz we observe the 'white' thermal noise floor.

As $V_{GS}$ is made more negative, the low-frequency contribution to the noise spectrum is reduced and the characteristic corner frequency identified above is increased (Fig. 1$b$). At still more negative gate voltages, we observe a flat noise spectrum with very few components at lower frequencies (Fig. 1$c$).

A similar dependence is observed for a nonsaturated device (Fig. 2). This indicates that the measured reduction in low-frequency noise is not directly related to the saturation mechanism.

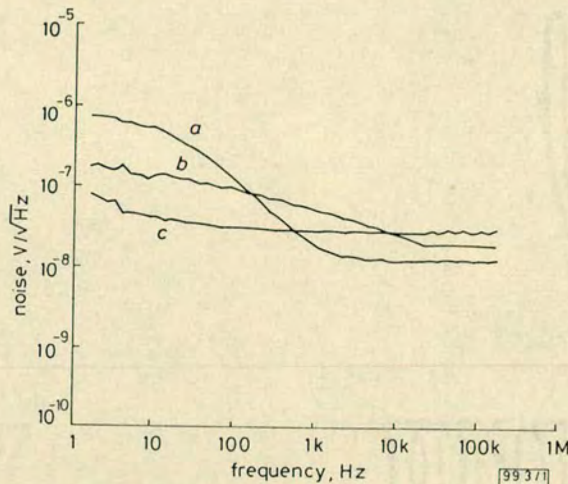


**Fig. 1** *Output noise spectra for buried channel MOS transistor in saturation region*

$a$ $V_{GS} = -2{\cdot}0$, $V_{BS} = -2{\cdot}00$ V
$b$ $V_{GS} = -2{\cdot}5$ V, $V_{BS} = -0{\cdot}45$ V
$c$ $V_{GS} = -2{\cdot}7$ V, $V_{BS} = -0{\cdot}30$ V
$V_{DS} = 500$ mV, $I_{DS} = 96{\cdot}7\,\mu$A

Fig. 3$a$ shows device transconductance as a function of gate voltage, and Fig. 3$b$ shows spot noise measurements made at 10 Hz as a function of gate voltage. We see a reduction in $g_m$ when the channel moves into the bulk, since the gate effectively loses some control of the charge forming the channel. Comparing Figs. 3$a$ and $b$, it can be seen that the device noise falls off before the $g_m$ is reduced. This means that low-noise operation with high gain is possible if the gate voltage is arranged to be around $-2{\cdot}5$ V for this device. Similar results have been observed in a number of devices across wafers and in two independent process production runs.

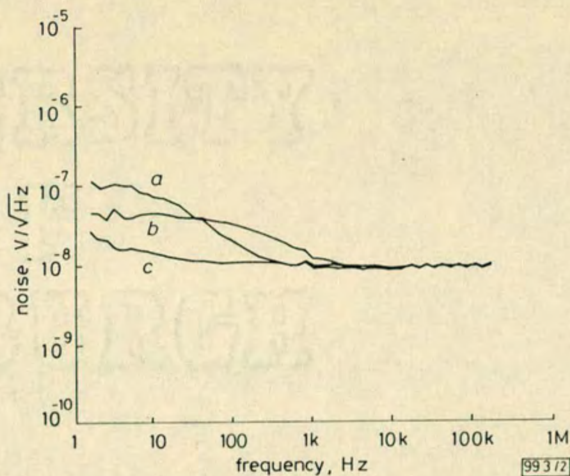


**Fig. 2** *Output noise spectra for buried channel MOS transistor below saturation*

*a* $V_{GS} = -2{\cdot}39\,V$, $V_{BS} = -0{\cdot}70\,V$
*b* $V_{GS} = -2{\cdot}45\,V$, $V_{BS} = -0{\cdot}55\,V$
*c* $V_{GS} = -2{\cdot}51\,V$, $V_{BS} = -0{\cdot}45\,V$
$V_{DS} = 50\,mV$, $I_{DS} = 11{\cdot}5\,\mu A$

*Conclusions:* We have seen that, by careful choice of operating point, buried channel MOS transistors can return useful gain with extremely low-noise operation, some three orders of magnitude below that for a typical enhancement-mode transistor at 10 Hz. However, the present devices have relatively poor saturation characteristics, with $r_{ds} \simeq 7\,k\Omega$ for operation in the low-noise regime. Such a low value of $r_{ds}$ precludes their use in conventional NMOS and CMOS analogue circuit designs. However, when realised in a combined bipolar-CMOS process,[4] the high input impedance of a buried channel MOS transistor can be combined with the increased $g_m$ of bipolar structures to provide an amplifier with low noise, high input impedance and high gain. The buried channel devices may also find application in certain common gate circuits, or in circumstances where low $1/f$ noise intermediate value resistors are required. It is evident that further work is required to produce a MOS transistor having such low-noise performance but with more acceptable circuit parameters.

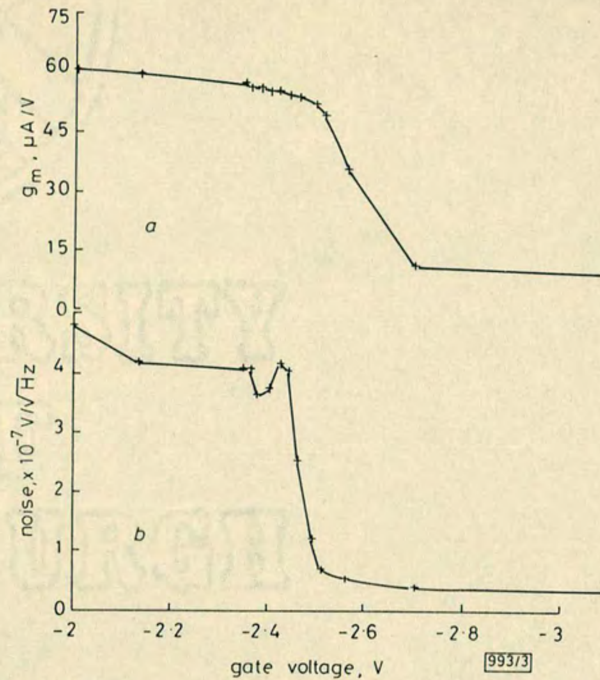


**Fig. 3** *Buried channel MOS transistor performance with gate voltage*

(*a*) Transconductance and (*b*) output noise voltage at 10 MHz
$V_{DS} = 500\,mV$, $I_{DS} = 96{\cdot}7\,\mu A$

*Acknowledgments:* One of us (CC) is indebted to the UK SERC in support of his studentship. The authors gratefully acknowledge the material support and facilities of Mullard Ltd., Southampton. We also appreciate valuable discussion with Mr. K. Kandiah.

C. CARRUTHERS
J. MAVOR

*1st September 1987*

*Department of Electrical Engineering*
*University of Edinburgh*
*The King's Buildings*
*Mayfield Road, Edinburgh EH9 3JL, United Kingdom*

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# MOS TRANSISTORS - NOISE PERFORMANCE AT LOW TEMPERATURE

Colin Carruthers and John Mavor

Department of Electrical Engineering
University of Edinburgh
The King's Buildings
Mayfield Road
Edinburgh
EH9 3JL
Scotland

*An overview of noise mechanisms in metal-oxide-semiconductor (MOS) transistors is presented. Results are given showing the noise performance of conventional enhancement mode and depletion mode MOS transistors under a wide range of operating conditions and temperatures. A potentially low noise buried channel, deep depletion MOS transistor is described. It is shown that by careful choice of bias conditions the conducting channel can be made to form away from the silicon-silicon dioxide interface resulting in extremely low output noise. The use of these devices as circuit elements is discussed.*

## 1. INTRODUCTION

MOS transistors are playing an increasingly important role in analogue circuits and systems [1], particularly at low temperatures for some key applications. Advantages of operation at temperatures below ambient include higher speed due to increased electron and hole mobility, improved thermal noise behaviour due to reduced phonon scattering, and greater packing density due to improved heat dissipation [2]. There are many applications for low noise analogue MOS circuits, including high resolution X-ray and gamma ray spectrometry [3] and advanced infra-red detection [4]. In the latter example, the entire assembly of detector and interfacing circuitry can be cooled to, for example, liquid nitrogen temperature for improved focal plane performance. For these requirements, the analogue circuit designer needs a detailed understanding of MOS characteristics and noise behaviour

– at a range of operating bias points and temperatures of interest – to be able to implement the necessary low noise, high gain input buffers.

This paper presents an overview of noise mechanisms relevant to MOS transistor operation. The process details for the MOS devices studied are discussed. A strategy for measuring noise is given and detailed noise measurements for MOS transistors presented. Finally, the potential use of the devices studied as circuit elements is treated.

## 2. PROCESS DETAILS

This section outlines the main process steps used to fabricate the devices used in these experiments. Three types of n-channel MOS transistors are considered here: enhancement mode, depletion mode and deep depletion. Figure 2.1 shows a schematic cross section of these transistors. As we shall see, the deep depletion devices can offer extremely good noise performance when bias conditions are chosen to ensure that the conducting channel is kept away from the silicon-silicon dioxide interface. All devices were fabricated on a p-type $20\Omega - cm < 100 >$ substrate. The enhancement mode MOSTs were boron implanted through a 750 Å oxide at an energy of 3.0 $keV$ with a total dose of $4.5 \times 10^{11}$ $atoms\ cm^{-2}$. Depletion mode devices were formed by implanting arsenic into the silicon at 40 $keV$ with a dose of $1.56 \times 10^{12}$ $atoms\ cm^{-2}$, followed by a 20 hour drive-in at 900 °C giving a junction depth of 0.15 $\mu m$. Buried channel (deep depletion) devices had a phosphorus implant at 80 $keV$ and a dose of $7.2 \times 10^{11}$ $cm^{-2}$, followed by a 24 hour drive-in at 1050 °C giving a junction depth of 2.8 $\mu m$.

## 3. NOISE MECHANISMS

There are three types of noise mechanism relevant to the operation of the MOS structures examined here [5]: thermal noise, shot noise and flicker (or $1/f$) noise.

### 3.1 Thermal Noise

In 1928 Johnson [6] found experimentally, with a theoretical proof given by Nyquist [7], that the root mean square (rms) noise voltage, $v_n$, across a

resistance, $R$, in thermal equilibrium at an absolute temperature, $T$, was

$$v_n = \sqrt{4kTRB_n} \tag{3.1}$$

where $k$ is Boltzmann's constant and $B_n$ is the bandwidth of the measuring system.

It is well known that this equation applies to any passive two terminal network at a temperature, $T$, with a series a.c. resistance, $R$. In the context of MOS transistors biased below 'saturation' where the device appears like a resistance, $R$ is $1/g_{ds}$ where $g_{ds}$ is the small signal channel conductance. The thermal noise level provides a white noise 'floor', *i.e.* the theoretical noise minimum for that resistance at that particular temperature.

### 3.2 Shot Noise

Schottky [8] carried out in 1918 the first theoretical study of fluctuations in the anode circuit of a temperature-limited thermionic diode. Shot noise is also observed in solid state devices and arises from the correlated departure of carriers entering the space-charge region separating p and n type material. The magnitude of the rms shot noise current, $i_n$, is given by

$$i_n = \sqrt{2eI} \tag{3.2}$$

where $e$ is the electronic charge and $I$ is the dc current flowing in the device. As we shall see, the noise results presented here indicate that buried channel MOS transistors appear to have a broad-band shot noise contribution when driven in the saturation mode.

### 3.3 Flicker Noise

All electronic devices carrying a direct current exhibit a low frequency 'flicker' noise in excess of the thermal or shot noise floor. In many devices the noise power increases approximately in inverse proportion to the frequency. Thus flicker noise is often called '$1/f$' noise, and has been observed over an extensive frequency range with measurements having been made from $10^{-5}$ $Hz$ to 10 $MHz$ [9, 10]. Theoretically the noise must level out as zero frequency is approached otherwise the integrated noise energy would be infinite.

There can be little doubt that flicker noise is due to trapping states of some kind but a physical model which can explain the huge range of time

constants observed has remained elusive. What can be said is that trapping is more likely in the vicinity of a surface or interface. As we shall see, results presented here confirm this since the noise in a deep depletion MOS transistor is reduced substantially when the channel is made to form in the bulk away from the silicon-silicon dioxide interface.

## 4. EXPERIMENTAL TECHNIQUE

This section describes the approach to noise measurements adopted here. A number of contrasting experimental techniques are described and justification for the chosen strategy is given.

### 4.1 Principles of Noise Measurement

There are two fundamentally different approaches to performing noise measurements. In the first approach, a calibrated noise source whose magnitude can be altered is used to determine the *equivalent* gate input noise for the transistor under test. Figure 4.1 shows the experimental configuration. With switch S closed the calibrated noise source is effectively shorted out and the noise power is measured at some specific frequency. Switch S is now opened and the 3 dB attenuator is introduced between the device under test and the amplifier. The magnitude of the white noise source is varied until the noise measured at the output is at its previous level. The magnitude of the calibrated noise source is then a measure of the equivalent gate input noise. The noise source can take the form of a pseudo-random binary sequence generator [3] or a temperature-limited vacuum diode [11]. Vacuum diode noise sources are only useful for frequencies above 1 kHz. Below this frequency the noise spectrum is dominated by flicker noise. *A priori* knowledge of the device transconductance, $g_m$, and the small signal channel conductance, $g_{ds}$, can be used to calculate the noise current, $i_n$, in the channel or noise voltage, $v_n$, across the transistor output source and drain terminals.

The main advantage in using this strategy to measure noise is that precise knowledge of the effective noise bandwidth of the filters and accurate calibration of the rms power meter are not prerequisites. However, as we shall see in section 5 the $g_m$ of a MOS transistor is a dependent on operating point. This is particularly true in depletion mode and buried channel MOS transistors where we see a reduction in $g_m$ when the conducting channel is forced to move into the bulk and there is no longer tight coupling between

the gate and the charge forming the channel. For a constant absolute current this leads to an *increase* in equivalent gate noise voltage. Undesirable second order effects such as this can be misleading and make meaningful analysis of results of noise measurements difficult.

An alternative technique for measuring noise is now discussed. By knowing the precise characteristics of the band-pass filters in Figure 4.1 and by using a calibrated noise power meter it is possible to measure directly the noise power in the device under test without having to resort to using the calibrated noise source and 3 dB attenuator.

This is essentially the strategy adopted here. However, the discrete band-pass filters and power meter in Figure 4.1 are replaced by a 50 channel spectrum analyser.

## 4.2 System Overview

This section presents a general description of the noise measuring system used here.

Figure 4.2 shows a block diagram of the apparatus. Bias voltages and currents are delivered to the device under test by a battery bias supply. Absolute noise voltage is measured across the source and drain of the transistor. A Brookdeal Ultra-Low Noise Pre-amplifier was used to match the magnitude of the noise voltage fluctuations to the input sensitivity of the spectrum analyser. The spectrum analyser used was a Brüel and Kjær Digital Frequency Analyser type 2131. The spectrum analyser comprises 50 band-pass filters ranging from 2 $Hz$ to 160 $kHz$. By knowing the gain of the amplifier, the effective bandwidth of each filter and the input sensitivity of the spectrum analyser it is possible to calculate directly the magnitude of the absolute noise voltage across the channel.

A measure of the absolute noise power as a range of frequencies provides insight into the noise mechanisms in the device under test and offers design engineers a pertinent indication of device noise performance.

A number of precautions were necessary to prevent interference and pick-up from external sources, particularly electrically-powered equipment elsewhere in the laboratory. The device under test, the battery bias supply and the amplifier were all placed inside a double-skinned Faraday box approximately 500 mm x 500 mm x 500 mm. The outer skin was connected to the building earth. The inner skin was allowed to float at signal ground and as such was at the same potential as the source of the device under test. The amplifier output was connected to the spectrum analyser input *via* a tri-axial cable. This cable had the inner and outer screens connected to the inner and outer skins of the Faraday box respectively. Dominant interference came form the (UK) mains electricity supply with spikes detected by

the 50 Hz and 160 Hz filters, and from the raster scan on the screen of the spectrum analyser at 11 kHz.

A Hewlett-Packard 4145 Semiconductor Parameter Analyser was used to obtain the DC characteristics.

## 5. EXPERIMENTAL RESULTS

This section describes the most important results obtained from measurements on enhancement, depletion and deep depletion mode MOS transistors.

### 5.1 Enhancement Mode MOS Transistor

Consider first the n-channel enhancement-mode MOS transistors. With a gate voltage ($V_G$) at zero, the source and drain junctions are isolated by a reverse-biased pn-junction. As $V_G$ is increased from zero, a depletion region forms along the length of the channel. With $V_G$ continuing to increase, the surface potential $\phi_S$ changes from positive to negative and the concentration of minority carriers (electrons) will exceed the hole density. Under these conditions, the region underneath the gate is said to be inverted. It can be shown that for small drain voltages, $V_D$, the drain current, $I_D$, is given by [12]

$$I_D = \mu_N C_O \frac{W}{L}[(V_G - V_T)V_D - \frac{{V_D}^2}{2}] \tag{5.1}$$

where $\mu_N$ is the effective carrier mobility. For larger $V_D$ the device operates in the 'saturation' regime, and

$$I_D = \mu_N C_O \frac{W}{L}\frac{(V_G - V_T)^2}{2} \tag{5.2}$$

As temperature is lowered the carrier mobility is improved as impurity scattering is reduced [1]. In moving from room temperature (300K) to liquid nitrogen temperature (77K) the mobility improvement can be as high as a factor of 5. However, for high fields the improvement is limited to the ratio of the carrier saturation velocities and can be as low as 1.5. Figure 5.1 shows the drain voltage characteristic of an enhancement-mode device at 300K (curve A) and 77K (curve B). By taking the ratio of saturation currents we can see that the increase in mobility is around a factor of three.

Figure 5.2 compares the noise characteristics of an enhancement-mode transistor biased in the 'linear' region at 300K (curve A) and 77K (curve B). Each plot can be divided into two regions. At frequencies above 1 kHz the

noise is constant and equal to the thermal noise in the channel. At 300K the channel resistance is equal to 16 $k\Omega$ giving $v_n = 16\ nV/\sqrt{Hz}$. At 77K (Figure 5.2(B)), $v_n$ falls to $\approx 8\ nV/\sqrt{Hz}$. The measured thermal-noise 'floor' is in fact slightly higher than this value since the device is entering saturation. Below 1 kHz, the noise shows a reciprocal dependence on frequency. The magnitude of this low frequency flicker noise is a strong function of carrier concentration and energy at the surface. At low currents, the output noise voltage is directly proportional to $I_{DS}$, Figure 5.3.

## 5.2 Depletion Mode MOS Transistor

The behaviour of depletion and deep depletion MOSTs at low temperature is substantially different. At temperatures lower than ambient partial 'freezeout' of the donor implant causes a reduction in substrate bias sensitivity and an unusual distortion of the gate voltage characteristic [2]. Figure 5.4 shows drain current as a function of gate voltage for a deep-depletion MOST at 300K and 77K. The gate voltage characteristic at 77K is distorted since the degree of donor freezeout is a strong function of applied gate voltage, $V_{GS}$.

For positive gate voltages, the conducting channel forms such that it is close to or touching the silicon-silicon dioxide interface. Observed noise behaviour is similar to that measured for an enhancement (surface channel) transistor [13]. We now investigate what happens to noise performance when the channel is formed away from the interface.

Figure 5.5 shows the noise spectra for a saturated 100 $\mu m$ by 15 $\mu m$ gate area buried channel device under three different gate voltages ($V_{GS}$) and substrate bias points ($V_{BS}$) at room temperature. Drain voltage and current were kept constant. It can be seen that as $V_{GS}$ was made more negative (and $V_{BS}$ made more positive to maintain the drain current) the characteristics of the transistor noise change considerably. Figure 5.5 (A) is typical of the observed spectrum over a wide range of $V_{GS}/V_{BS}$ values. The characteristic is dominated by a time constant of around 100 ms giving a plateau below 10 Hz and a sharp roll-off above this frequency. At frequencies above 5 kHz we observe the 'white' thermal noise floor.

As $V_{GS}$ is made more negative, the low frequency contribution to the noise spectrum is reduced and the characteristic corner frequency identified above is increased, Figure 5.5 (B). At still more negative gate voltages, we observe a flat noise spectrum with very little structure at lower frequencies, Figure 5.5 (C).

A similar dependence is observed for a non-saturated device, Figure 5.6. This indicates that the measured reduction in low frequency noise is not directly related to the saturation mechanism.

Figure 5.7 (A) shows device transconductance as a function of gate voltage, and Figure 5.7 (B) shows spot noise measurements made at 10 Hz as a function of gate voltage. We see a reduction in $g_m$ when the channel moves into the bulk since the gate effectively loses some control of the charge forming the channel. Comparing Figures 5.7 (A) and (B), it can be seen that the device noise falls off before the $g_m$ is reduced. This means that low noise operation with high gain is possible if the gate voltage is arranged to be around -2.5V for this device. Similar results have been observed in a number of devices across wafers and in two independent process production runs.

A similar reduction in noise has been observed in deep depletion MOS transistors at 192K, liquid Freon temperature. Below this, at 90K (liquid oxygen) and 77K (liquid nitrogen) certain bias conditions can cause a low frequency oscillation to dominate the noise performance of depletion and deep depletion MOS transistors [14]. Figure 5.8 shows such an oscillation in the frequency domain.

## 6. CONCLUSIONS

We have seen that by careful choice of operating point buried channel MOS transistors can return useful gain with extremely low noise operation, some three orders of magnitude below that for a typical enhancement mode transistor at 10 Hz. However, the present devices have relatively poor saturation characteristics with $r_{ds} \approx 7\ k\Omega$ for operation in the low noise regime. Such a low value of $r_{ds}$ precludes their use in conventional NMOS and CMOS analogue circuit designs. However when realised in a combined bipolar-CMOS process [15], the high input impedance of a buried channel MOS transistor can be combined with the increased $g_m$ of bipolar structures to provide an amplifier with low noise, high input impedance and high gain. The buried channel devices may also find application in certain common gate circuits, or in circumstances where low 1/f noise intermediate value resistors are required. It is evident that further work is required to produce a MOS transistor having such low noise performance but with more acceptable circuit parameters.

## ACKNOWLEDGEMENTS

One of us (CC) is indebted to SERC (UK) in support of his studentship. The authors gratefully acknowledge the material support and facilities of

Mullard Ltd, Southampton, United Kingdom. We also appreciate valuable discussion with Mr. K. Kandiah.

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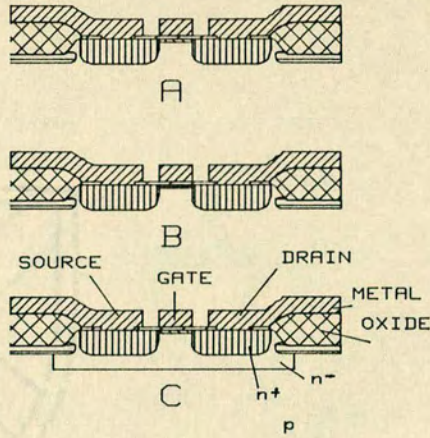
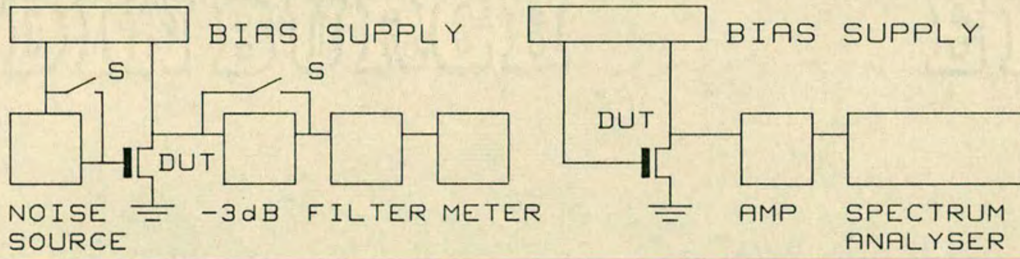


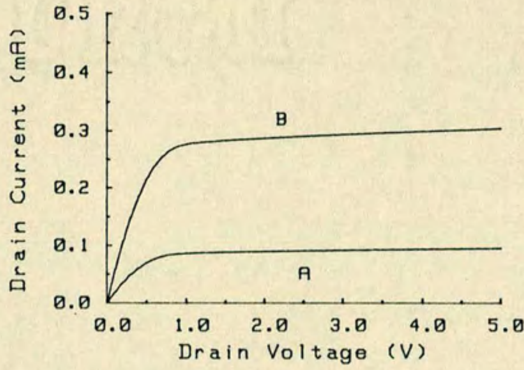

**2.1** Schematic Cross Section of Measured Devices.

A Enhancement Mode
B Depletion Mode
C Deep Depletion Mode

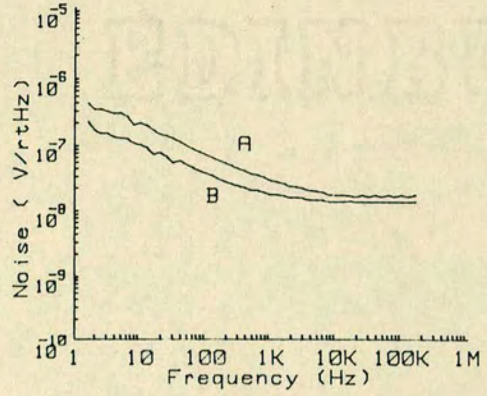



**4.1** Circuit for Measuring Equivalent Gate Noise Voltage.

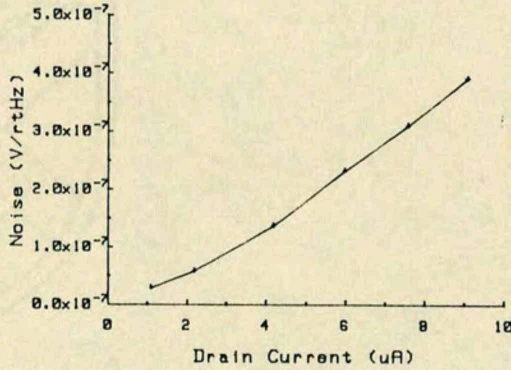
**4.2** Schematic Diagram of Noise Measuring Equipment.



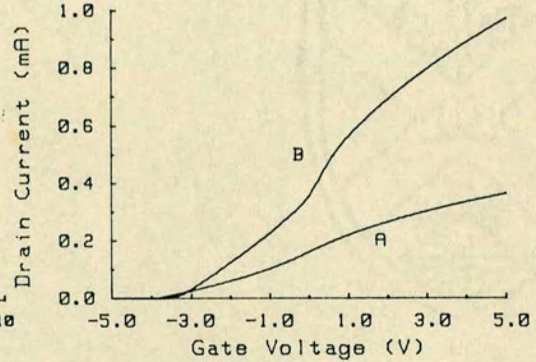

**5.1** Measured Drain-voltage Characteristics for Enhancement Mode MOS Transistor. (100x15 μm) at 300K (A) and 77K (B).
$(V_{GS} - V_T) = 1.25$ V, $V_{BS} = -5$ V.




**5.2** Noise Spectrum for Enhancement Mode MOS Transistor (100x15μm) at 300K (A) and 77K (B).
$V_{DS} = 100$ mV, $I_{DS} = 10$ μA, $V_{BS} = 0$ V.

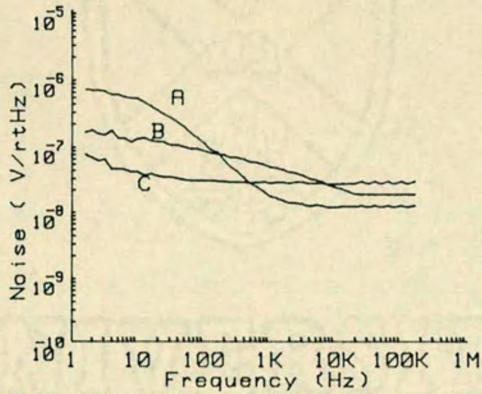



**5.3** Noise Dependence on $I_{DS}$ in Enhancement Mode MOS Transistor at 77 K, f = 20 Hz.




**5.4** Gate-voltage Characteristic for Deep Depletion Mode MOS Transistor. (100x15 μm) at 300K (A) and 77K (B).

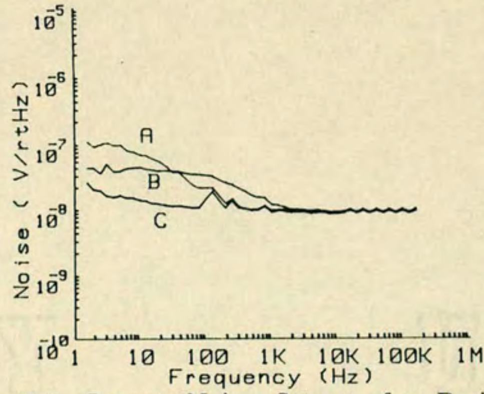
$V_{DS} = 100$ mV, $V_B = -5$ V.




**5.5** Output Noise Spectra for Buried Channel MOS Transistor.
Saturation Region.

(A) $V_{GS} = -2.0$ V, $V_{BS} = -2.00$ V;
(B) $V_{GS} = -2.5$ V, $V_{BS} = -0.45$ V;
(C) $V_{GS} = -2.7$ V, $V_{BS} = -0.30$ V;

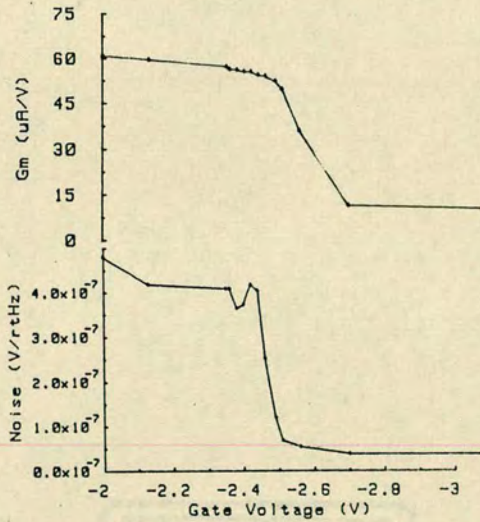
$V_{DS} = 500$mV, $I_{DS} = 96.7\mu$A.




**5.6** Output Noise Spectra for Buried Channel MOS Transistor.
Below Saturation.

(A) $V_{GS} = -2.39$ V, $V_{BS} = -0.70$ V;
(B) $V_{GS} = -2.45$ V, $V_{BS} = -0.55$ V;
(C) $V_{GS} = -2.51$ V, $V_{BS} = -0.45$ V;

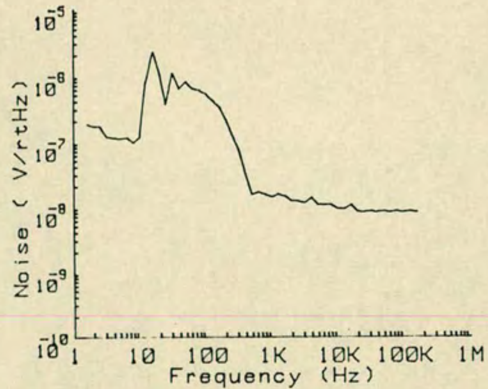
$V_{DS} = 50$mV, $I_{DS} = 11.5\mu$A.




**5.7** Buried Channel MOS Transistor Performance with Gate Voltage.

(A) Transconductance, and
(B) Output noise voltage at 10 Hz.

$V_{DS} = 500$mV, $I_{DS} = 96.7\mu$A.




**5.8** Noise spectrum showing Anomalous Oscillation in Depletion Mode MOS Transistor at 77K.
$V_{DS} = 125$ V, $I_{DS} = 10\ \mu$A, $V_{GS} = 0$ V, $V_{BS} = -5$ V.