FABRICATION OF MICROCHANNELS FOR USE IN MICRO-BOILING EXPERIMENTS

by

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Acknowledgements

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Abstract

Increased power densities in VLSI chips have led to a need to develop cooling methods that can cope with the increased heat produced by such chips. Currently one of the more attractive methods to meet this goal is through the use of two phase flow of a fluid as changing phase of the material allows high heat transfer rates for a low temperature change. To bring this technology to commercialisation a greater understanding of the underlying physics involved at the microscale is required as there is much debate within literature as to what occurs during two phase flow heat transfer at these scales. The work conducted as part of this thesis is a step towards improving the understanding of the mechanisms involved with this process.

This thesis describes the fabrication of a novel microchannel structure, which can be used to experimentally characterise two phase heat transfer as it occurs. The final process reported for these microchannels structures provides the basis of a technology for the fabrication of microchannels with increased sensor densities.

Two types of microchannel devices have been fabricated for this project. The first device of these was an array of parallel microchannels formed by the reactive ion etching (RIE) of silicon, which was then bonded with Pyrex glass. These microchannels were simple in that sensors were not integrated for local measurement. However the production of these devices incorporated fabrication techniques such as anodic bonding and inductively coupled plasma RIE that were essential to the fabrication of more complex devices.

The second device built was a single microchannel that contained an integrated heater and several temperature sensors. The use of wafer bonding enabled the device to take full advantage of both bulk and surface micromachining technology as the placement of the temperature sensors on the channel floor would not be possible with conventional bulk micromachining. The initial microchannel structures demonstrated that wafer bonding could be used to fabricate novel devices, but they highlighted the difficulty of achieving strong anodic bonds due to the presence of dielectric films throughout the fusion bonded wafer stack used in the channel fabrication. To improve the performance of the device the process was optimised through the use of in-situ, non-destructive test structures. These structures enabled the uniformity and strength of the bonds to be optimised through visualisation over the whole wafer surface. The integrated sensors enabled temperature measurements to be taken along the channel with a sensitivity 3.60 ΩK^{-1} while the integrated heater has delivered a controllable and uniform heat flux of 264 kWm^{-2}.

Declaration

I hereby declare that the research recorded in this thesis and the thesis itself was composed and originated entirely by myself in the School of Engineering at the The University of Edinburgh.

List your exceptions and sign before your printed name.

Fig. 4.17 Measurement taken by Dario Bogojevic

Fig. 5.2 Measurement taken by Dario Bogojevic

Gerard Cummins

Contents

List of figures

List of tables

Chapter 1
Introduction

1.1 Introduction

The invention of the transistor in 1947, followed by the development of the integrated circuit in 1958 have underpinned the rapid and continued improvements in performance since seen in the semiconductor industry. This improved performance has been achieved through the reduction of minimum feature size with each successive generation of integrated circuits.

1.2 Moore's Law

Gordon Moore of Intel Corporation observed a trend in 1975 that the number of transistors per chip had been doubling annually for a period of 15 years which has continued to the present day to become known as Moores Law [5]. Decreasing feature size of transistors has enabled more transistors for a given area and this increased integration has lead to the development of more complex processors. For example the first microprocessor developed by Intel in 1971 (the Intel 4004) operated at 108 KHz and contained 2300 transistors with a minimum feature size of 10 μm whereas one of the more recent microprocessors (an Intel Xeon processor) contains 820,000,000 transistors with a minimum feature size of 45 nm operated at a frequency of 3 GHz [6].

1.3 Greater integration

Parameters taken from data sheets provided by Intel, AMD and other microprocessor manufacturers have been used to create Fig. 1.1, which illustrates how the number of transistors packed onto successive microprocessor generations follows an exponential trend as predicted by Moore's law.

The driving force for this pattern is the continuing demand for increased computing perfor-

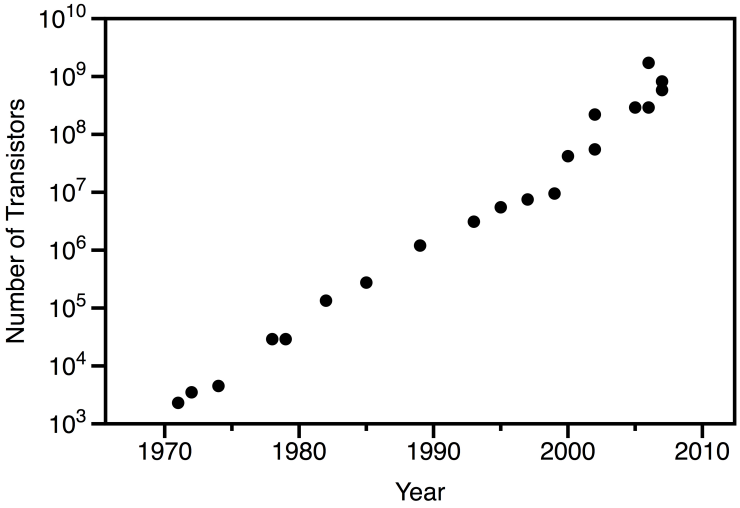


Figure 1.1: *Number of transistors per processor over four decades*

mance and functionality at reduced cost that has been achieved by reducing the minimum feature size of transistors over time as shown in Fig. 1.2.

These trends cannot continue indefinitely due to the fundamental limits of physics. Continued scaling without proper consideration of these limits can lead to issues affecting reliability, yield and susceptibility to noise. An example of the effect of nearing some of these limits is that as devices scale down they become even more vulnerable to smaller particles and defects that affect yield.

Scaling of the transistors is not a trivial exercise. However, these concerns are outweighed by the economic benefits and the improved performance. Scaling is usually carried out in accordance with one of two approaches, which are constant voltage and constant electric field scaling.

1.3.1 Constant voltage scaling

Constant voltage scaling involves reducing the lateral dimensions of a MOSFET while maintaining the operating (V_{DD}), gate source (V_{GS}) and threshold (V_t) voltages at a fixed value. A reduction in the gate length L and width W by a factor of ζ, where $0 \ll \zeta \ll 1$ will result in a change of drain current in saturation (I_D) by a factor of ζ^{-1} giving a current of I'_D due to the scaling of the width, length and oxide thickness (t_{ox}) by the same amount. This is demonstrated below, where ϵ_{ox} is the permittivity of the gate oxide and μ is the mobility of the charge

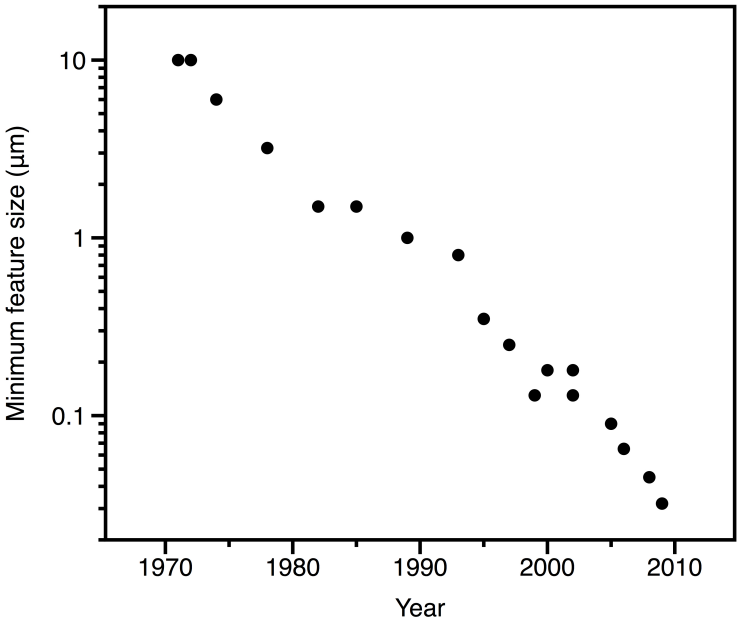


Figure 1.2: *Minimum transistor feature size over four decades*

carriers.

$$I_D = \frac{1}{2}\mu\frac{\epsilon_{ox}}{t_{ox}}\frac{W}{L}(V_{GS} - V_t)^2 \tag{1.1}$$

$$I'_D = \frac{1}{2}\mu\frac{\epsilon_{ox}}{\zeta t_{ox}}\frac{\zeta W}{\zeta L}(V_{GS} - V_t)^2 \tag{1.2}$$

$$I'_D = \frac{1}{\zeta}I_D \tag{1.3}$$

However the gate capacitance (C_G) and propagation delay (τ) are changed by a factor of ζ and ζ^2 respectively.

$$C'_G = \frac{\zeta L \zeta W \epsilon_{ox}}{\zeta t_{ox}} \tag{1.4}$$

$$C'_G = \zeta C_G \tag{1.5}$$

$$\tau' = \frac{V_{DD} C'_G}{I_{D'}} \tag{1.6}$$

$$\tau' = \frac{V_{DD} \zeta C_G}{\frac{1}{\zeta} I_D} \tag{1.7}$$

$$\tau' = \zeta^2 \tau \tag{1.8}$$

The scaling of the gate capacitance allows the transistor to be switched at a higher frequency due to the reduction in the propagation delay (τ) by a factor of ζ^2. Constant voltage scaling of transistors also changes the total power (P) consumed by a factor of $\frac{1}{\zeta}$ with the reduction in die size causing the power density (P_A) to increase by a factor of $\frac{1}{\zeta^3}$. Hence more heat is generated and this requires more efficient heat removal methods to ensure reliable operation.

$$P' = I'_D V_{DD} \tag{1.9}$$

$$P' = \frac{1}{\zeta} P \tag{1.10}$$

$$P'_A = \frac{P'}{A'} \tag{1.11}$$

$$P'_A = \frac{\frac{1}{\zeta} P}{\zeta W \zeta L} \tag{1.12}$$

$$P'_A = \frac{1}{\zeta^3} \frac{P}{A} \tag{1.13}$$

$$P'_A = \frac{1}{\zeta^3} P_A \tag{1.14}$$

Furthermore the decrease in transistor dimensions results in an increase of the vertical electric field across the depletion layer that may lead to the electric field increasing such that dielectric breakdown occurs. These undesirable effects can both be alleviated by also scaling the drain source voltage with the geometry, which is called constant electric field scaling.

1.3.2 Constant electric field scaling

Constant electric field scaling involves reducing the gate width W, length L, gate oxide thickness t_{ox} as well as the supply (V_{DD}), drain source (V_{DS}) , threshold (V_t) and gate source (V_{GS}) voltages by the scaling factor ζ. This results in the drain current I_D decreasing by ζ, while the electric field, propagation delay reduces to $\zeta\tau$ and power density (P_A) remains unchanged.

$$I'_D = \frac{1}{2}\mu\frac{\epsilon_{ox}}{\zeta t_{ox}}\frac{\zeta W}{\zeta L}(\zeta V_{DS})^2 \tag{1.15}$$

$$I'_D = \zeta\frac{1}{2}\mu\frac{\epsilon_{ox}}{t_{ox}}\frac{W}{L}(V_{GS} - Vt)^2 \tag{1.16}$$

$$I'_D = \zeta I_D \tag{1.17}$$

$$P' = I'_D V'_{DD} \tag{1.18}$$

$$P' = \zeta I_D \zeta V_{DD} \tag{1.19}$$

$$P' = \zeta^2 P \tag{1.20}$$

$$P'_A = \frac{P'}{A'} \tag{1.21}$$

$$P'_A = \frac{\zeta^2 P}{\zeta L \zeta W} \tag{1.22}$$

$$P'_A = P_A \tag{1.23}$$

$$P'_{dyn} = C'_L V'^2_{DD} f_{sw} \tag{1.24}$$

$$P'_{dyn} = \zeta C_L \zeta V^2_{DD} f_{sw} \tag{1.25}$$

$$P'_{dyn} = \zeta^2 P_{dyn} \tag{1.26}$$

$$\tau' = \frac{V'_{DD}C'_G}{I'_D} \tag{1.27}$$

$$\tau' = \frac{\zeta V_{DD}\zeta C_G}{\zeta I_D} \tag{1.28}$$

$$\tau' = \zeta\tau \tag{1.29}$$

Operating the circuit at a lower voltage reduces the energy consumed but at the cost of switching speed. However, the trade-off between supply voltage scaling and switching speed can be optimised by adjusting the lateral and vertical dimensions along with the applied voltage. Alternatively if a higher clock frequency is desired above other criteria then scaling the supply voltage by a smaller factor than the other parameters can be used to achieve this goal. This may explain the increase in power density observed in microprocessors over time as shown in Fig. 1.4. However this is not beneficial for reducing the dynamic power consumption (P_{dyn}) and delay time as it leads to an increase in the channel electric field and a higher drain current.

1.4 Power density

Scaling down transistors has enabled the functionality and performance of microprocessors to be increased but this often comes at the cost of increased power density as processor architecture is often optimised for computational capacity and speed and not power dissipation. Switching transistor circuits at ever increasing frequencies is often utilised to improve the performance as shown in Fig. 1.3.

Increasing transistor numbers and clock frequencies leads to larger power dissipations and an urgent need for more efficient heat removal. Increasing packing densities also increases the number of transistors per unit area that are switching at any one time leading to an increase of the power density over the last two decades [7] as illustrated by Fig. 1.4.

The four sources of power dissipation associated with MOSFETs and MOSFET circuits are dynamic (P_{dyn}), short-circuit (P_{short}) , leakage ($P_{leakage}$) and static power dissipation (P_{static}) [8] and the sum of these describe the total power dissipated as shown below.

$$P = P_{dyn} + P_{static} + P_{leakage} + P_{short} \tag{1.30}$$

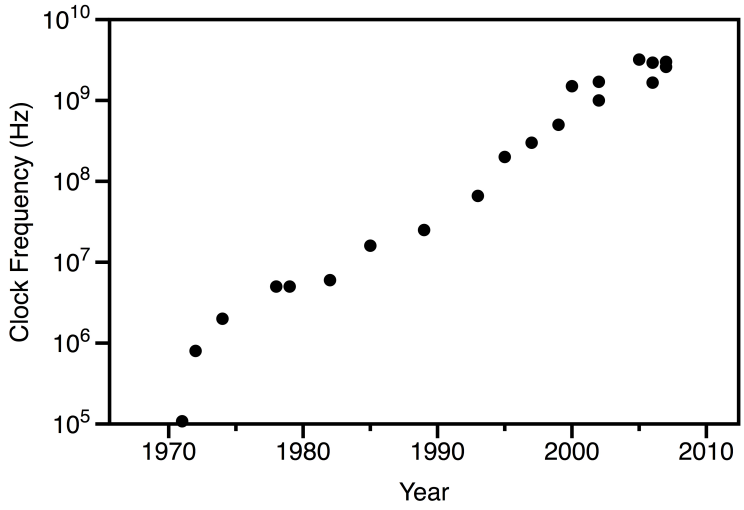


Figure 1.3: *Increasing processor operating frequency over four decades*

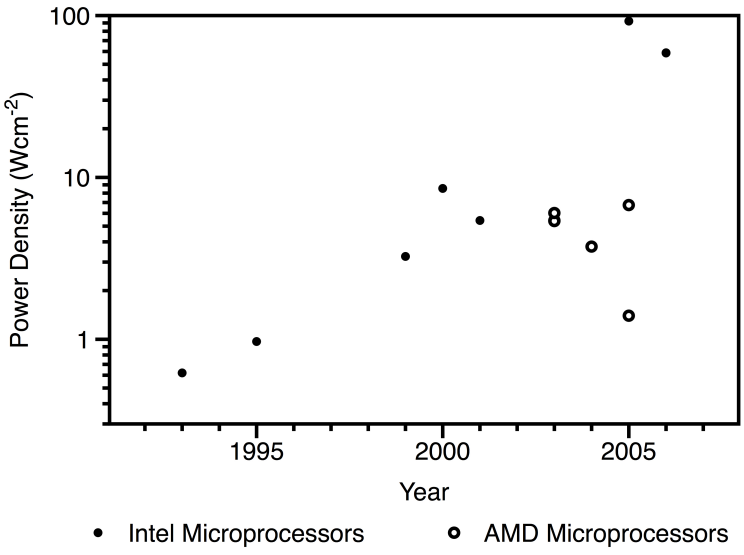


Figure 1.4: *Increasing processor power density over two decades*

In the following sections the cause of each method of power dissipation will be discussed in addition to solutions for reducing their effect.

1.4.1 Dynamic power dissipation

Dynamic power dissipation occurs when various parasitic capacitances or load capacitances are charged and discharged in a CMOS circuit, such as the inverter shown in Fig. 1.5 as the circuit switches between states. This output current varies with each transition and initially shows a transient spike in current due to the short circuit current, which is described in subsection 1.4.3. This transient current is followed by the dynamic current due to the charging and discharging of the capacitances, which is noted as $I_{dynamic}$ in Fig. 1.5.

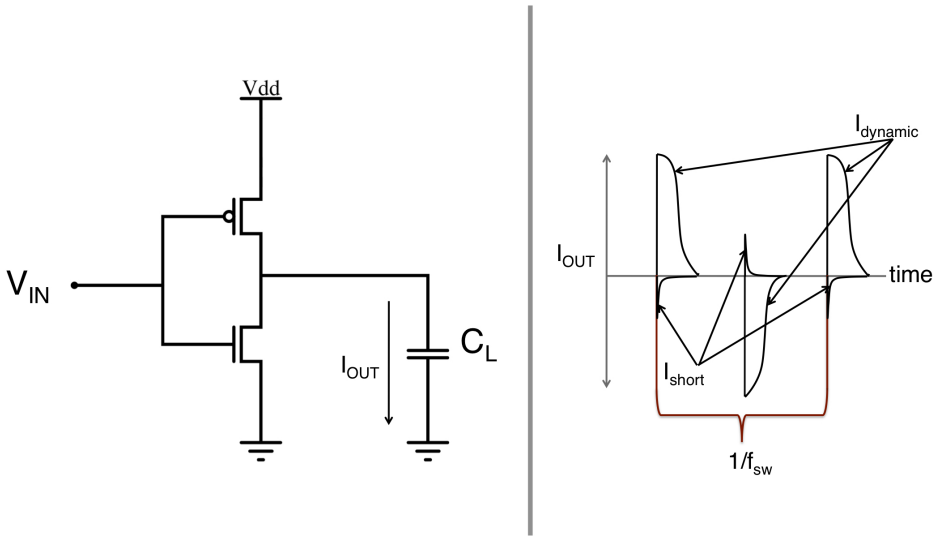


Figure 1.5: *Loaded CMOS inverter showing typical currents due to switching*

The energy consumed by this process is given by $E_{cap} = 0.5V_{DD}^2 C_L$ and it can be observed that the energy consumed depends only on the supply voltage (V_{DD}) and the total output load capacitance (C_L)[8]. However, the power also depends on the switching frequency (f_{sw}) as shown in equation 1.31 and as this is increased the charging and discharging of the load capacitance (C_L) occurs more rapidly so that the dynamic power dissipated (P_D) increases.

$$P_{dyn} = V_{DD}^2 C_L f_{sw} \tag{1.31}$$

Methods proposed to reduce power dissipation include minimising parasitic capacitances and

optimisation of the circuit design. One method by which the latter can be achieved is by the careful selection of the logic family used to implement the microprocessor [9] on the basis that the number of state transitions that occur is a function of the logic family used. The selection of logic family is made by determining the probability that an output will be in 0 in one clock cycle and 1 in the next, assuming that all inputs are independent. For example, the probability that the output of a 2 input NAND gate is at 0 is $\frac{1}{4}$ and $\frac{3}{4}$ for 1 where as the probability that a 2 input XOR gate is at 1 is $\frac{1}{2}$. Using this information the transition probability can be calculated using equation 1.32 where N is the number of inputs and N_0 is the number of zero entries in the truth table for the outputs.

$$p_{0\leftarrow 1} = \frac{N_0(2^N - N_0)}{2^{2N}} \tag{1.32}$$

Hence the transition probability for the NAND gate would be $\frac{3}{16}$, whereas for the XOR it's $\frac{4}{16}$. Implementation of microprocessors is often implemented using NAND logic as it reduces the transistor switching between clock cycles and thus the dynamic power consumption [8] [9].

1.4.2 Leakage power dissipation

Leakage power dissipation is a result of either scaling down the threshold voltage or the device geometry. With the minimum feature size of some transistors now being below 90 nm this leakage power is dissipated in the form of waste heat [10] and the two sources of leakage current that contribute most to leakage power dissipation are sub-threshold leakage current and gate oxide tunnelling [11].

Sub-threshold leakage is the dominant cause of leakage power dissipation and is due to the diffusion of charge carriers between the source and drain when the gate voltage is lower than the threshold voltage. This leakage power has become more noticeable due to scaling of the threshold voltage and the dimensions between the source and drain. The drain-source diffusions and the n-well diffusions can act as parasitic diodes in MOSFETS with an example of this in the profile of a MOSFET inverter shown in Fig. 1.6.

The reverse biased diode located at the n-well and substrate contributes a leakage current I_L that causes the leakage power dissipation P_L [8]. The power due to this leakage current can be expressed as $P_L = I_L V_{DD}$, where P_L is the power due to the leakage current and I_L is the

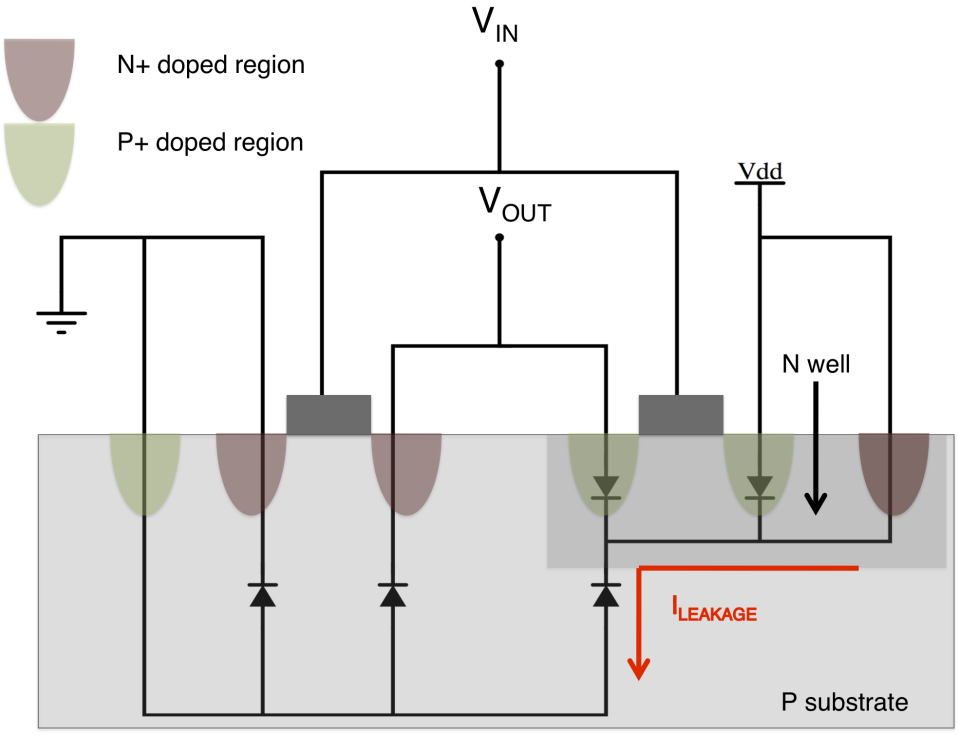


Figure 1.6: *Side profile of a CMOS inverter showing the leakage current due to parasitic diodes*

value of the leakage current, which can be calculated using the diode equation.

$$I_L = i_s(\exp^{\frac{qV}{kT}-1}) \tag{1.33}$$

Gate oxide tunnelling results from the thinning of the gate-oxide associated with transistor scaling. This results in a higher electric field across the oxide. The combination of a thin dielectric and a high electric field results in the tunnelling of electrons through the oxide. This leakage current (I_g) has been reduced in recent years with the transition from a silicon dioxide gate dielectric to high-k dielectric materials such as hafnium oxide [12]. Assuming that gate oxide tunnelling is minimal in comparison to other sources of leakage power the total power consumed by the transistors is given below, where α is the probability that switching occurs.

$$P = \alpha(0.5V_{DD}^2 C_L f_{sw}) + I_{st}V_{DD} + I_{sh}V_{DD} + I_{leakage}V_{DD} \tag{1.34}$$

1.4.3 Short circuit power dissipation

Short circuit power dissipation occurs when the transistor switches between high and low states when the input signal has a finite rise time resulting in a short circuit path forming between V_{DD} and ground. During this time both PMOS and NMOS transistors are on, which allows a short circuit current to flow as shown in an unloaded CMOS inverter in Fig. 1.7. The short circuit period is defined by the length of time it takes for the input signal voltage V_{IN} to move between the threshold voltage of the NMOS transistor (V_{TN}) and $V_{DD} - |V_{TP}|$. The longer this period is the greater the mean current and hence the short circuit power dissipation.

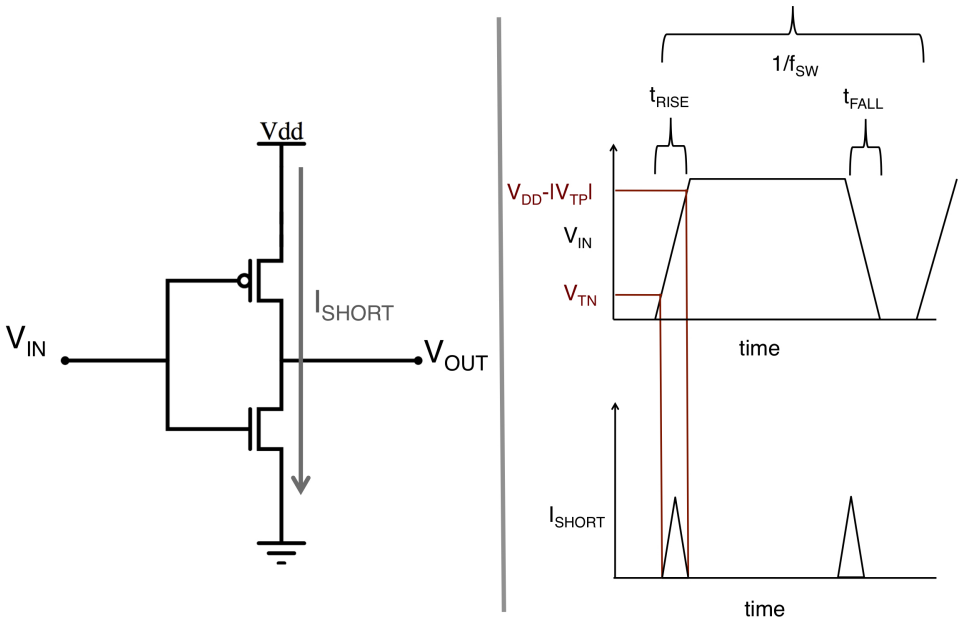


Figure 1.7: *Unloaded CMOS inverter showing short circuit current as a function of rise and fall time of input signal*

The power consumed due to this short circuit current is given below, where τ_R is the rise-time of the input signal, β is the effective transistor strength and V_t is the threshold voltage.

$$P_{sh} = \frac{\beta}{12}(V_{DD} - 2V_t)^3 \tau_R f_{sw} \tag{1.35}$$

The short circuit power consumption can be reduced by making the rise-times of the output greater than that of the input signals equal by having a large load capacitance at the output node. This ensures that at the transition point between the PMOS and NMOS operation that the drain source voltage of the PMOS negligible due to the effect of this charged capacitive load.

This allows the circuit to finish switching states before the output signal changes and prevents short circuit power dissipation [9]. Increasing capacitive load leads to a much slower circuit and may cause problems in the fanout gates. Choosing a capacitive load such that the input and output signal rise times is considered a good compromise.

1.4.4 Static power dissipation

Static power consumption rarely occurs in current processors but is mentioned here for completeness. However, it can be observed under conditions such as circuits where rail to rail swings do not feed other circuits, or when the circuits are built using pseudo-NMOS logic, such as the inverter shown in Fig. 1.8 or utilise analog bias circuits. Static power consumption can be reduced by ensuring that these circumstances do not occur within a circuit design.

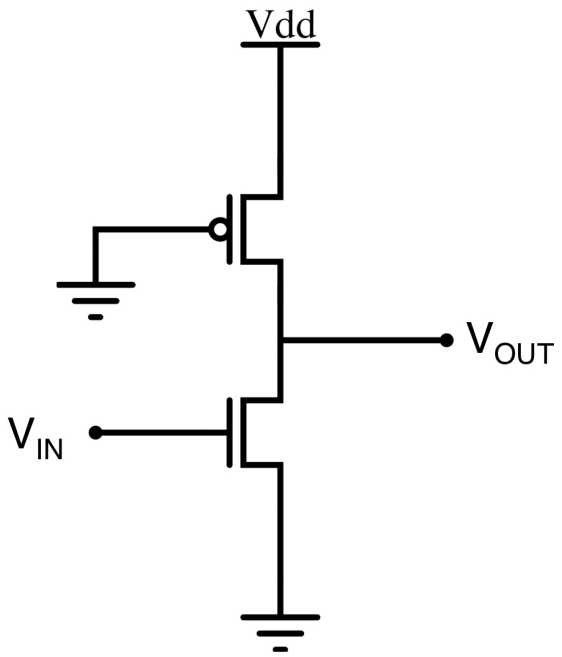


Figure 1.8: *Unloaded pseudo-NMOS inverter*

1.4.5 Other causes of power dissipation

Other sources of power dissipation present in integrated circuits include Joule heating caused by current flowing through interconnects. Although this accounts for a small fraction of the total power dissipated in the chip it can contribute to the temperature as the interconnects and transistors often have several layers of electrical and thermally insulating materials between

them and the substrate surface.

The heat generated as a result of processor operation has to be removed to ensure continual and optimal performance of the microprocessor. Higher temperature reduces the lifetime of the device leading to an increased risk of electromigration [13], poor signal integrity and noise [14]. Mechanical stress of the device may also occur due to the non-uniform temperature distribution encountered across the chip that may lead to further degradation of chip reliability. A worst-case scenario would be the occurrence of thermal runaway on the chip as a vicious cycle of rising temperature causing increased leakage power dissipation. Unless the heat generated by next generation microprocessors can be successfully removed it will be no longer be possible to reliably use them.

Most of the advances in processor performance discussed so far have been achieved by scaling down transistor geometry and voltages. However, over the last few decades several methods have emerged that enable the trend of increasing microprocessor performance with time to be maintained without the need for further scaling of transistor parameters, which can result in increase heat fluxes. Some of these methods include low power circuit design, the use of multi-core processors and improved chip packaging. These will be discussed in more detail in the following sections.

1.5 Chip design

Low power chip design methodology has in the past few years become increasingly used outside of the area of portable electronics design to address the rising power densities inherent with most modern processors [15] [16] [17]. There are many circuit based techniques to reduce the power consumed in digital CMOS circuits such as careful selection of the logic gates to implement the microprocessor, minimising switching capacitances and utilisation of dynamic or pass-gate logic. These and other methods are discussed in more detail by Chandraksan [9] [18].

Other methods of power reduction include techniques such as clock gating and dynamic supply voltage scaling [19]. Clock gating uses a control signal to block a clock signal from a logic block when it is not in use reducing clock signal activity that enables a reduction in active power consumption. For this to be a viable technique the power consumed by the control signal logic must be less than the power savings achieved by gating the clock signal.

Dynamic supply voltage is a technique where logic is used to detect either the highest supply voltage available or processor demand. In the case of a low supply voltage or low processor demand the processor is operated at a lower voltage resulting in lower power consumption but also in lower performance. When a greater demand on processing resources is detected then a high voltage is supplied to the processor resulting in optimal performance. This method allows savings in power consumption to be made but it is only suitable for devices that are not in constant use.

Many current systems have also begun to use on chip thermal sensing to improve device performance. A temperature sensor detects when the chip or parts of the chip are approaching a specified temperature limit and sends a signal to a controller so that it can either power down, slow down or reconfigure the chip if possible to reduce the temperature [20] [21] [22]. This method increases the complexity of the design and sacrifices performance in exchange for a lower heat flux on the chip surface.

1.5.1 Multi-core processors

Another method where processor performance can be increased without further scaling and increased power density is to use a multi-core design for the processor that involves placing two or more processors on the same die. This allows a greater number of operations per second to be achieved without the need for increased transistor density or operating frequency. The main motivation for this development comes from the greatly diminished gains in single core processor performance that have resulted from increasing operating frequency in recent years [23].

Usually the multiple cores are fabricated on the same die with the primary advantage for this arrangement is that the signals degrade less than they would if the cores were situated separately on the same motherboard. This also removes the need to use higher voltages to drive external signals. The placement of the cores on the same die can also allow the use of smaller dies through the use of shared common circuits. Multiple core architecture require novel parallel programming techniques to ensure that each processor is working simultaneously on part of the overall program to ensure the full potential is utilised. This is a challenging task and is the focus of much current research.

There is a limit to the improvement in performance possible with this architecture due to the

use of parallelised software. With each core added to the chip the complexity of the software increases until a point is reached where the return on additional cores diminishes. Amdahl's Law models the relationship between the expected increase in speed of an algorithm implemented for parallel processing relative to the serial processing version of the algorithm under the assumption that the problem size does not change when parallelised. In the case of parallelisation this can be modelled by the equation shown below where $P_{PARALLEL}$ refers to the proportion of the program that can be made parallel, S is the increase in speed in solving the problem defined as the ratio of the execution time of the sequential algorithm (T_{SEQ}) to that of the parallel algorithm (T_{PAR}) and N_{proc} is the number of processors.

$$S = \frac{1}{(1 - P_{PARALLEL}) + \frac{P_{PARALLEL}}{N_{proc}}} \tag{1.36}$$

Using equation 1.36 it can be shown that parallelisation is ideal for massively parallel problems such that $P_{PARALLEL}$ is large or the number of processors, N is small. Amdahl's law shows that the return on increasing the number of processor cores on a chip is minimal after a certain number of processors for a given program. This is shown graphically in Fig. 1.9.

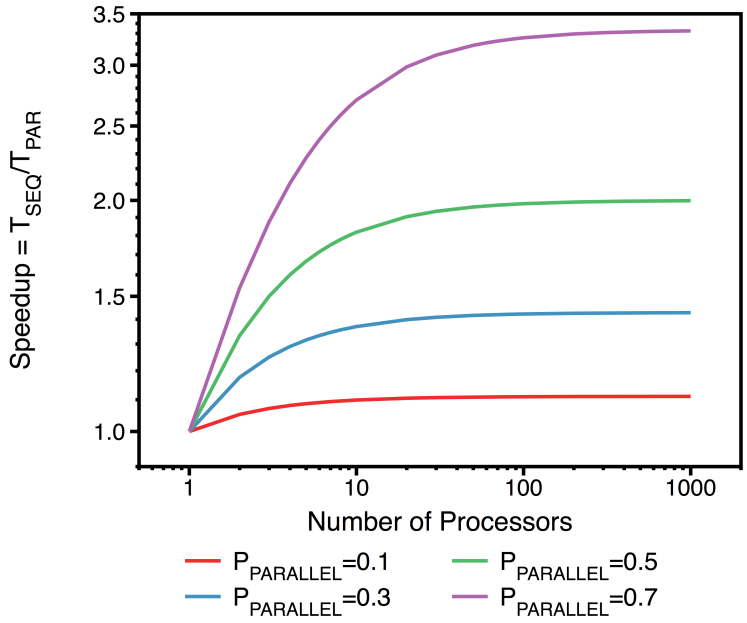


Figure 1.9: *Speedup of a program as a function of program parallelization and number of processors*

Multi-core processors have become increasingly widespread in recent years despite the in-

creased complexity in implementing software for these chips such that most new model laptops and PCs use multi-core processors as do the latest game consoles. For example the Sony Playstation 3 uses an 8 core processor called ”Cell” that has been developed by Sony, IBM and Toshiba [24].

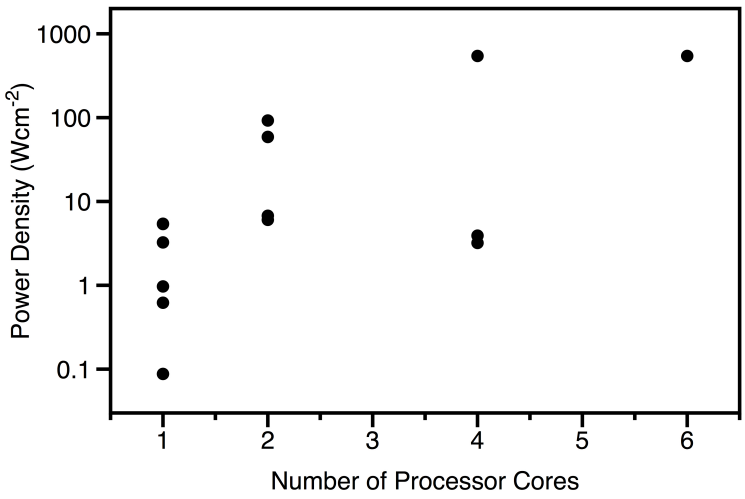


Figure 1.10: *Power density versus number of processor cores*

Although the multi-core approach offers an alternative to frequency scaling to increase processor performance it is not the ultimate solution due to the shared issue of increased power density. As can be seen from Fig. 1.10 the power density of multi-core processors taken from relevant data sheets show that it can be the same as single-core processors and in some cases higher again demonstrating the need for a suitable means of heat removal.

1.5.2 Packaging

Although methods such as transistor scaling and multi-core architectures ensure increased performance, the problem of high power densities remains. Without a means of transferring the waste heat away at a rate equal or greater than the rate it is being generated, the processors will not be able to operate for long. The problem of high heat flux has been historically been addressed over the past five decades through the use of improved thermal management systems that have an important role of ensuring components continue to operate at the desired temperature and ensure optimal performance.

Currently the most commonly used method of thermal management involves the forced convection of air using fans to transfer heat from heat sinks mounted on the chip packaging to the

surrounding environment. Within the next few years the heat fluxes generated will exceed the heat transfer limits of forced convection air cooling and a replacement technology to current fan based cooling will be needed [25] [26].

There are several thermal management methods that could be used for next generation processors. Many of these involve utilising the latent heat of vaporisation of a working fluid to remove these high heat fluxes. Such two phase cooling systems will be discussed in greater detail in Chapter 2. One of the most promising of these methods is called two phase flow in microchannels and it has been the subject of much research over the last few decades. However, it is still an immature technology and little is still known about how boiling heat transfer exists at the micro-scale.

1.6 Microboiling project

This thesis is concerned with the fabrication of micro-channels for two-phase flow of liquid studies. These devices are designed to contribute to increasing the understanding of boiling heat transfer at the micro-scale and aid in the optimisation of micro-fluidic thermal management systems for possible use in microprocessor heat transfer. This was carried out as part of a larger EPSRC funded project consisting of academic and industrial partners, which included Queen Mary College, University of London, Brunel, Nottingham and Heriot-Watt Universities, the University of Edinburgh, ANSYS, Thermacore and BAE Systems.

The objectives of the project included a study of two phase flow patterns and heat transfer in single and multiphase flow, simulations for flow boiling and condensation, the investigation of several methods of heat transfer enhancement, development of optimal design methods for micro-heat exchangers for a variety of applications and the development of prototype systems for cooling microprocessor chips. These objectives were carried out using either experimental or numerical methods by the various project partners.

Queen Mary College, University of London (QMUC) developed a model for the condensation of liquid in non-circular microchannels and compared the model against experimental results [27]. Nottingham University developed numerical models to describe a number of conditions. These include the nucleation of growth of bubbles in various channel geometries under both uniform and non-uniform heating conditions, the effect of thermal interactions between neighbouring channels on heat transfer and the behaviour of thin liquid and vapour films in mi-

crochannels during evaporation and condensation [28] [29] [30] [31] [32] [30]. ANSYS were interested in incorporating the models developed in future products.

Brunel University aimed to investigate flow boiling of various working fluids at heat fluxes up to 2 MWm^{-2} in a single silicon microchannel with cross sectional dimensions in the range of 0.1 to 1 mm. Temperature sensors and heaters would be integrated with this silicon microchannel, which was fabricated at the University of Edinburgh. The design and fabrication process of these devices are described in Chapters 4 and 5 [33] [34].

Khelil Sefiane's research group at the University of Edinburgh investigated flow boiling under similar conditions in silicon microchannel arrays. These silicon microchannels were also fabricated at the University of Edinburgh and the initial devices are described in Chapter 3. These devices were used to determine the thermal and flow interactions between adjacent channels, develop optimal feeder and collector manifold designs, determine the effect of non-uniform heating on flow boiling and identify the major parameters that affect the stability of boiling regimes in microchannel arrays. The final devices produced contained integrated heating and sensing elements alongside with optimal manifold and channel geometries[35] [36] [37] [38] [39].

Heriot Watt University also investigated flow boiling in microchannel arrays. However, these microchannels were fabricated from copper, using traditional manufacturing methods [40]. Because of the manufacturing methods used the dimensions of these channels were larger than the ones used by Brunel and Edinburgh. The results of this study were compared to those conducted at Brunel and Edinburgh. BAE and Thermacore used the results of the experimental studies at Brunel, Edinburgh and Heriot Watt to develop improved products. Additionally the results from the experimental studies were used to verify and improve the models, the results of which were then used to improve the experimental designs [33] [29].

1.7 Conclusions

Since 1975 Moore's law has predicted the development of successive generations of integrated circuits. Shrinking transistor size has influenced the explosive growth of the semiconductor industry by allowing increased performance, complexity and functionality with significant decreases in cost. This has lead to the near ubiquitous presence of the microprocessor in many applications. The semiconductor industry is finding it increasingly challenging to follow Moore's law in recent years due to the approaching fundamental limits of physics, which impede further

scaling down of CMOS transistors. Although improvements in chip performance have been obtained through the use of novel chip architectures and designs the problem of the heat flux at the chip surface due to the power dissipated by transistors still exists. If a viable solution is not found the increased heat fluxes predicted will inhibit optimal operation of VLSI systems.

Power density is expected to exceed 100 Wcm^{-2} for the 14nm chip generation [41] according to the ITRS, which would be beyond the ability of any forced convection and heat sink based thermal management system. Thermal management methods that allow greater heat transfer rates than possible with current forced convection based systems offer a solution.

Chapter 2
Thermal management

2.1 Thermal management of integrated circuits

The last fifty years have seen an increase in transistor density driven by advances in silicon processing technology that have enabled the continuous scaling of transistor sizes. This in turn has allowed an increasing demand for greater performance, functionality and speed from successive generations of microprocessors to be delivered.

The semiconductor industry has sought to maintain this trend through the use of multiple processor cores integrated on a single die as the limits of Moore's law approach. The increased complexity and performance of the CPU comes at the cost of greater power consumption. To ensure the reliability of these devices over the desired product lifetime it is necessary that the surface temperature of the chip does not become excessive due to the increase in power dissipation. This can be accomplished with the use of thermal management systems with the goal of these systems to transport the heat at the chip surface such that its temperature is maintained at an appropriate level. Many cooling methods have been developed within the past two decades to meet the challenge of cooling the next generation of microprocessors that are expected to produce heat fluxes exceeding $100\ Wcm^{-2}$ [25] [42] [43] [44] [45]. This is beyond the capability of the current commonly used systems and is hence currently a research topic of much interest.

2.2 Heat transfer mechanisms of cooling devices

Thermal management systems utilise a combination of heat transfer mechanisms to remove heat. These include conduction that involves the transfer of thermal energy within solids from a region of high to low temperature. Convection which is the transfer of thermal energy through fluids from areas of high to low temperature and radiation which transfers thermal energy through infrared energy. Heat sinks and single phase microchannels use convection to transfer heat into the environment with conduction being employed by heat sinks and heat spreaders.

Radiation is not commonly used as a method of heat transfer for microprocessors due to the low heat transfer rates that can be achieved [46].

Phase change is defined as the transition of matter from one state to another by the release or absorption of latent heat energy. This property of water and other materials has been increasingly applied to heat transfer applications in recent years and have been identified as an attractive possibility for meeting future thermal management requirements. Examples of applications of this approach include spray cooling, jet cooling, heat pipes and two phase flow microchannels.

2.3 Cooling devices for microprocessors

This section reviews the current method used to cool microprocessors and some of the cooling technologies that are being developed to meet the needs of the next generation microprocessors. This includes the ability of the chosen heat transfer system to deal with conditions such as a highly non-uniform power distribution across the surface of the chip that reduces the efficiency of thermal management methods [47]. Future thermal management solutions will need to be able to dissipate heat fluxes that are expected to be between 100 and 1000 Wcm^{-2}, while ensuring that the surface temperature of the chip does not exceed the operating temperature recommended by the manufacturer.

2.3.1 Overview

Using the classification suggested by Webb it is possible to divide thermal management systems into two categories of direct and indirect heat removal [45]. Direct heat removal is defined as an *"ambient heat sink that is directly attached to the hot source"*. This includes heat sink/fan systems and thermoelectric cooling. Indirect heat removal is defined as "*an ambient heat sink that is remote from the hot source, and uses a "working fluid" to transport heat from the hot source to the heat sink"*. This includes heat pipes, two phase flow in microchannels and many other methods as detailed in Fig. 2.1.

2.3.2 Heat sinks

Presently the most common technology used to cool microprocessors is "direct heat removal" in the form of a heat sink system mounted onto the processor packaging as shown in Fig. 2.2. This

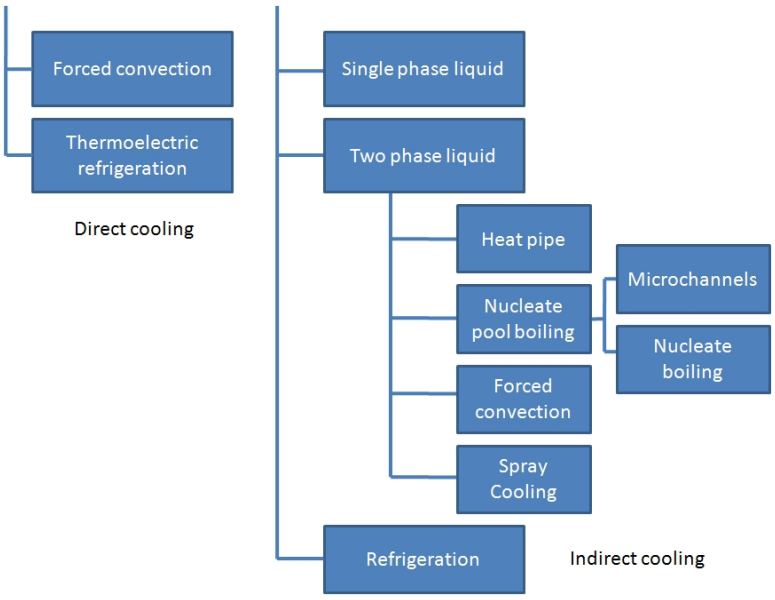


Figure 2.1: *Direct and indirect thermal management methods*

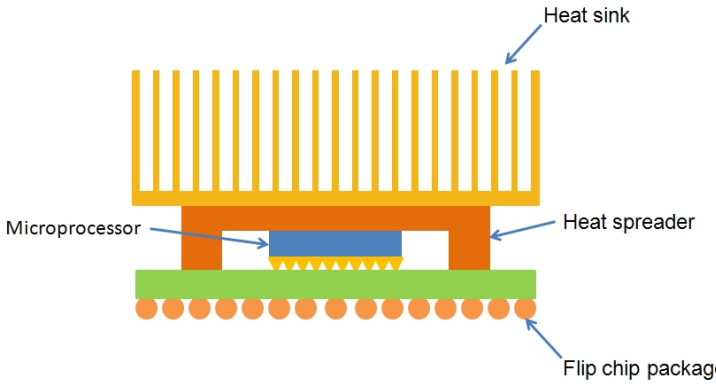


Figure 2.2: *Typical heat sink structure for microprocessor heat removal*

is a relatively cheap and well understood solution. However, it will not be able to effectively cool next generation microprocessors due to the high heat fluxes these devices will dissipate. Heat sinks consist of a base region that is in contact with the chip with fins extending out from the base increasing the surface area for heat transfer to the air. Heat is conducted through the base into the fins and is transferred to the air flowing between the fins via convection. In some cases an intermediate heat spreader is used to reduce the heat flux by increasing the surface area that the heat sink is in contact with [48].

Heat sink performance is a function of several parameters such as the surface area, fin size, fin density, thermal conductivity of the heat sink material and air flow velocity. Using a fan

to force air over the fins can increase the heat transfer rate but at the expense of system cost, size and noise produced. Unlike other methods of thermal management heat sink and fan systems can operate irrespective of orientation. This is important when the growing market for portable computing is considered. Increasing the flow of air over the heat sink by increasing the fan speed or size can improve the heat transfer rates but is eventually limited by the thermal properties of air. One drawback of this approach is that it tends to lead to an increase in noise which may not be desirable.

Optimisation studies have improved cooling performance by employing greater numbers of fin with increasing heights while decreasing the fin spacing and increasing the thermal conductivity by switching from aluminium to copper. Further optimisation along these lines is not expected to meet future thermal management requirements as in recent years further studies have led to ever diminishing improvements in performance [45] [49].

2.3.3 Thermoelectric cooling

Thermoelectric cooling is a direct method of cooling that can be directly integrated onto the heat source. It is based on the principles discovered by Seebeck in 1821 and expanded on by Peltier in 1834 whereby heat can be transferred against the thermal gradient from one side of a device to the other by the application of an electric potential. This has been used to create solid-state heat pumps where a positive potential applied to the n-type thermoelectric material induces cooling and the heat transfer rate is a function of the current passing through the device and the number of couples comprising the device. The structure of such a thermoelectric cooler is shown in Fig. 2.3.

For applications involving the cooling of electronic devices, the cooler side of the thermoelectric device is placed in contact or integrated with the hot surface to allow heat transfer between the cooler and the device. To improve heat transfer the hot side of the thermoelectric cooler is in contact with some other means of transferring the heat to the ambient environment such as a heat sink and fan. A responsive direct current source is applied to the thermoelectric device to ensure the temperature of the electronic devices is kept within a suitable operating range.

Coefficient of performance is a measure of the efficiency of a refrigeration system and is given by

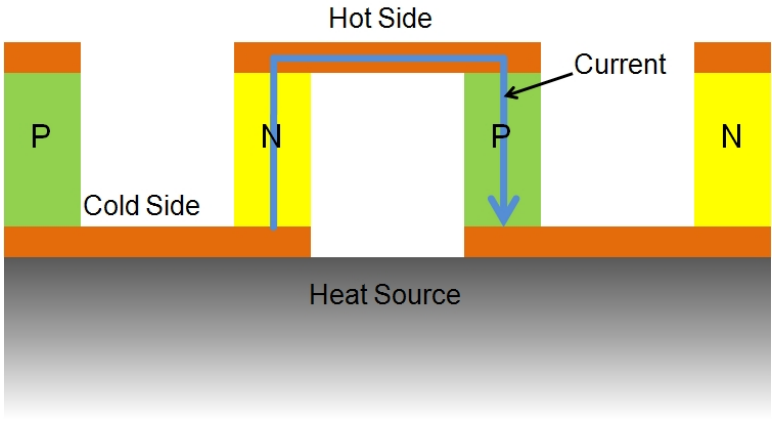


Figure 2.3: *Structure of a thermoelectric cooler*

$$C.O.P = \frac{Q}{W} \tag{2.1}$$

where Q is the cooling power in Watts and W is the work put into the system also in Watts. In the case of thermoelectric coolers a COP less than one means that the work put into the system is greater than the heat removed. In this case the heat that needs to be removed from the hot end of the cooler can be shown to be $Q + W$. This leads to an even greater heat transfer problem at the hot end of the thermoelectric cooler than at the surface of the chip that is being cooled [50].

Scaling down the devices should lead to better performance as the cooling density of a Peltier device is inversely proportional to its length. However, shrinking down the materials used can be problematic due to poor manufacturing yields limiting how much the cooler side can be scaled by [44]. Thermoelectric refrigeration offers the promise of a low volume cooling solution that can be directly integrated onto the device [51] for some applications. The solid-state nature of the devices may also be attractive in some applications due to the absence of moving parts and working fluids. However thermoelectric devices are not expected to be viable for the thermal management needs of next generation microprocessors due to their high cost, the limited heat fluxes of $5-10\,Wcm^{-2}$ they can remove [52] [53] and a coefficient of performance which is less than one.

2.4 Liquid cooling

Liquid cooling can greatly increase the rate of heat removal and reduce device temperature in comparison to conventional heat sink systems [44]. As with cooling systems in general, liquid cooling can be divided into direct and indirect heat removal categories. Additionally these cooling methods can also be categorised depending on whether they are single or two phase. Two phase methods utilise the latent heat of evaporation to ensure higher heat transfer rates than is achievable with single phase cooling.

Direct heat removal methods place the working liquid in contact with the high heat flux source. This has the advantage of a lower thermal resistance between the device surface and the coolant. However the coolant must be chemically and electrically compatible and because of this dielectric coolants such as FC-72 are often used. Indirect liquid heat removal uses an intermediary layer between the device and the coolant. This layer should be a good thermal conductor to minimise the thermal resistance and allows a greater coolant choice.

2.4.1 Single phase cooling

The work conducted by Tuckerman and Pease [54] started research into the use of single phase flow heat transfer in microchannels. This allows improved heat transfer rates compared with air cooling. Much research has been conducted in recent years to develop and optimise practical single phase flow heat transfer systems utilising microchannels. Single phase liquid cooling with water has been reported to remove heat fluxes from between 100 to 780 Wcm^{-2} depending on the geometry of the microchannels [55].

Most single phase cooling systems consist of a pump that forces the working fluid through a microchannel array that is either in direct or indirect contact with the heat source. The liquid must be sub-cooled entering the microchannels and must remain sub-cooled as it flows through the channels to remove the heat. The single phase cooling system also incorporates a heat exchanger to remove the heat from the liquid before returning it to the inlet of the microchannel array.

Microchannel heat sinks have been fabricated using wide ranging technologies with arrays of parallel channels consisting of rectangular, triangular, circular or trapezoidal cross sections with hydraulic diameters between 100 to 1000 μm being reported [56] [57] [58] [59]. Micro-

fabrication techniques, primarily the etching of silicon have been used to construct several of these devices obtaining smaller and more precise geometries than is possible with traditional machining. Microfabrication has also been used in the development of micro-pumps that are attractive as they have the potential to provide a smaller, more integrated and less noisy system than is possible with a conventional pump [60]. However micro-pumps reported in literature for analytical microfluidic systems may not be appropriate due to the high flow rates and high pressures experienced. Pumps are an important competent that enable the cooling systems to be orientation insensitive as the liquid is not dependant on gravity to flow through the microchannels.

The heat transferred by single phase flow through a microchannel heat sink may be determined using equation 2.2, where q is heat transfer, Nu is the Nusselt number, k is the thermal conductivity of the liquid, A is the area of the heatsink wetted, D_h is the hydraulic diameter of a microchannel and ΔT is the mean difference between the temperature of the fluid and the substrate.

$$q = \frac{Nuk\Delta TA}{D_h} \tag{2.2}$$

Thermal resistances of less than 0.1^oCW^{-1} have been reported for such single phase cooling systems [61] that is a significant improvement over air cooled heat sinks. This reduction in thermal resistance can be attributed to the fact that the microchannel heat sinks can be either directly attached to the chip with only tens of micrometers of materials between the heat source and bottom of the channels or etched directly into the back of the chip.

2.4.2 Two phase cooling

Two phase cooling promises even higher heat transfer rates than can be achieved with either air cooled fin heatsinks or single phase liquids. It utilises the principle of latent heat of evaporation associated with liquid changing into a gaseous state during the boiling process. Boiling is defined as evaporation that takes place at a solid-liquid interface. This is considered a convection mode of heat transfer and large heat fluxes can be removed without altering the temperature of the liquid as the absorbed heat primarily contributes to changing the phase in the form of vapour bubble nucleation and growth. The heat is transferred by these bubbles through the liquid to the heat exchanger where the heat is released through condensation and removed from the system

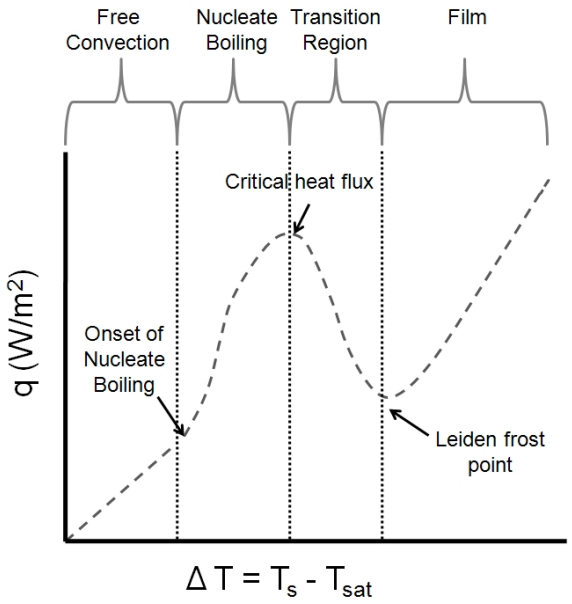


Figure 2.4: *Typical features of a boiling curve*

to the external environment.

Critical heat flux can be used to measure the performance of two phase cooling solutions and is defined as the maximum heat flux that can be transferred without encountering a reduction in heat transfer efficiency as shown in the typical boiling curve of Fig. 2.4. If the temperature is increased beyond this value then the density of bubbles on the boiling surface starts to form an insulating thin layer of vapour that prevents the liquid from being in contact with the chip surface. This leads to a reduction in the heat transfer is observed causing an increased chip surface temperature as shown in the film region of Fig. 2.4.

Fig. 2.5 shows that heat fluxes removed with traditional air cooled heat sinks are in the range $1 - 10\ Wcm^{-2}$, whereas methods of thermal management based on the principle of the latent heat of vaporisation can remove heat fluxes greater than $100\ Wcm^{-2}$. The use of patterned surface enhancement features [62] [63] [64] [65] [66] [67] can increase the high heat transfer coefficients even further. These raised, sunken or roughened features act as vapour traps and provide more sites to facilitate bubble nucleation in predefined areas [67]. Improvements of heat transfer coefficients by a factor of four have been reported under favourable conditions using these structures [63].This approach has been investigated to address the challenge of cooling the next generation of electronics [67] [66] [68].

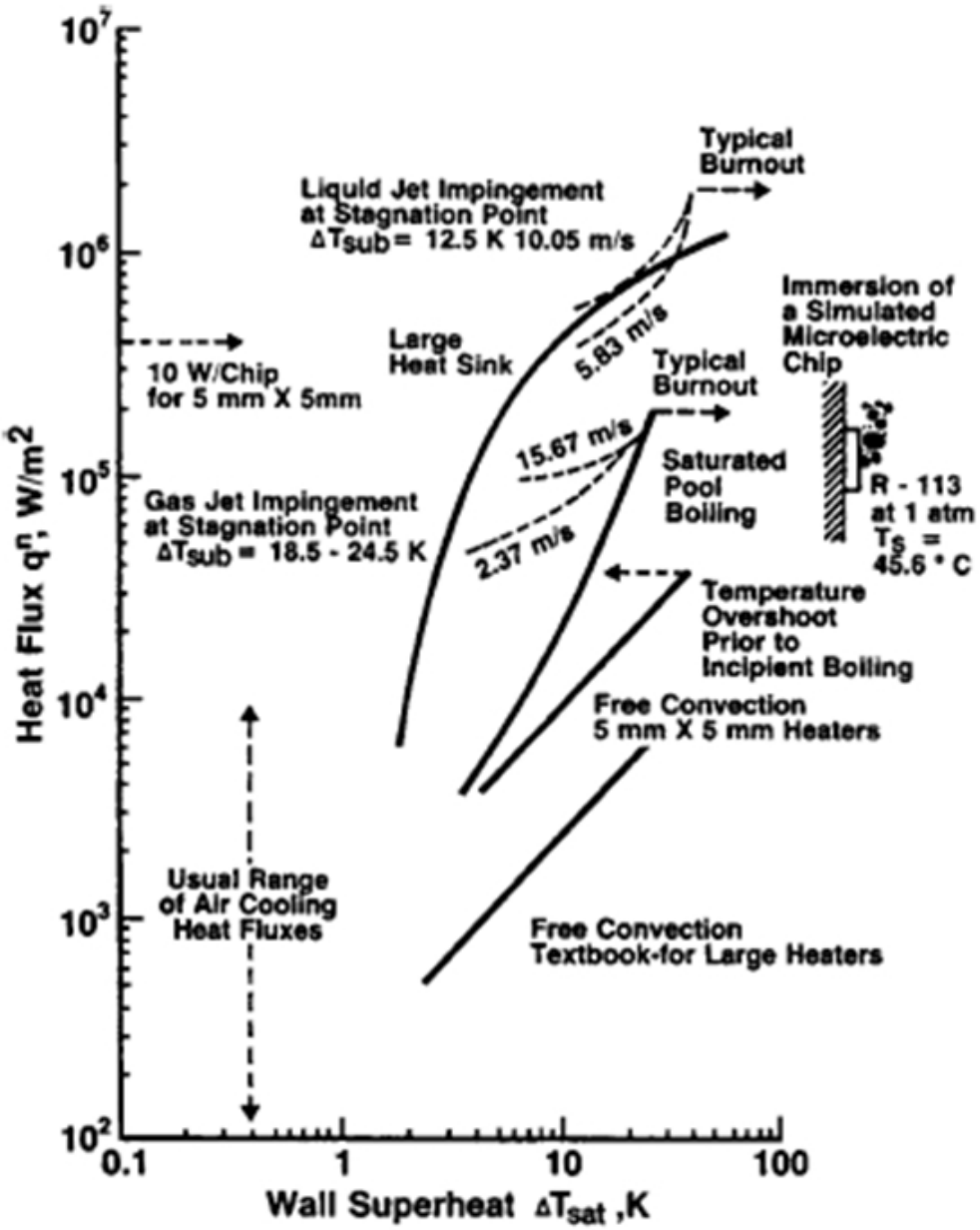


Figure 2.5: *Heat flux ranges of various thermal management methods [1]*

2.4.2.1 Heat pipes

Heat pipes are a well established and commercially successful indirect method of passive heat removal that consist of a sealed evacuated tube most commonly made of copper that is partially filled with a working fluid such as water. Heat pipes consist of three zones, a condenser, an evaporator and an adiabatic zone.

As the heat pipe is evacuated the internal pressure is fixed by the vapour pressure with the evaporator zone existing at a slighter higher temperature and pressure compared to the rest of the device due to the tapered internal geometry of the heat pipe. This pressure gradient allows the vapour to flow along to the condenser zone when heat is applied to the evaporator end. The cooler environment in this region allows the vapour to condense and for the latent heat of condensation to conduct to the external environment. The wick structure present on the internal surface of the heat pipe transports the working fluid back to the evaporator zone through capillary action and this closed loop cycle continues as long as heat is applied and the heat pipe remains sealed.

Heat pipes are orientation dependent devices that limits their use to certain applications. Heat sinks are usually used in conjunction with heat pipes to enable the latent heat energy of condensation to be quickly removed from the condenser end and this adds to the size of the thermal management system. The effectiveness is limited by the length of the pipe with the shorter the pipes the poorer the performance. This is demonstrated by pipes less than 1 cm in length having a cooling performance comparable to the thermal conductivity of a solid piece of metal. This means that heat pipes are most suited to applications where a large device area is not a disadvantage. Larger areas may also be desirable if a heat spreader is used in conjunction with a heat pipe, this combination has been reported to result in thermal conductivity comparable to diamond [69].

2.4.2.2 Jet impingement cooling

Jet impingement cooling involves projecting jets of liquid coolant onto the hot spots on the surface of integrated circuits [70]. The jet hits the surface and spreads out as a thin liquid film that then evaporates causing localised cooling to occur. This in turn leads to high temperature gradients being created across the surface with the size of these cooler spots being affected by the velocity and diameter of the jet. Heat fluxes of between 90 [70] and $108\ Wcm^{-2}$ [71] have

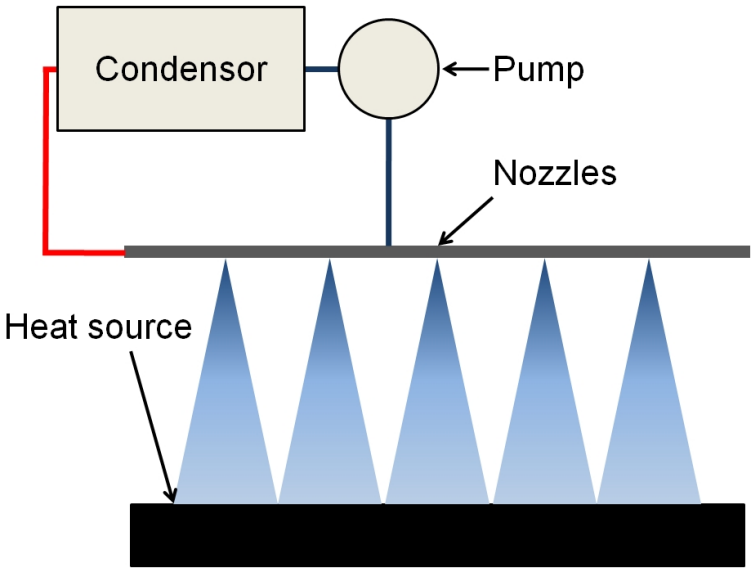


Figure 2.6: *Spray cooling*

been removed using this method.

The localised cooling produced by this method makes it suitable for cooling of transient or steady state hot spots although multiple jets would be required for a large area that would increase complexity. Disadvantages associated with this method include sensitivity to orientation, the possibility of damage to the die surface due to the momentum imparted by the jet impacting the surface and the formation of high stresses due to the localised high temperature gradients generated within the chip. These factors have resulted in jet impingement cooling being considered a too aggressive thermal management system, which as a consequence has not lead to it being widely adopted for the future heat transfer needs of the microelectronic industry.

2.4.2.3 Spray cooling

Spray cooling is superficially similar to jet impingement in that they both involve the coolant being directed onto the high heat flux surface. However, in the case of spray cooling, the liquid hits the surface as a uniformly applied mist of droplets that do not lead to localised cooling and the subsequent formation of temperature gradients. Improved temperature uniformity as well as the use of a low momentum spray makes this a less aggressive cooling method that is much less prone to damaging the chip. Chip-level spray cooling has been reported to remove heat fluxes of 160 Wcm^{-2} [72].

Spray cooling can be divided into those using pressure sprays formed by liquid moving through a nozzle at a high pressure and those using atomised sprays created by a high pressure air stream that breaks up the liquid into a spray. Although atomised sprays have better cooling performance they bring with them greater complexity when incorporated into a closed loop electronic cooling system due to the difficulty in separating the evaporated coolant from the air used to form the spray [73].

2.4.2.4 Two phase flow in microchannels

While the work conducted by Tuckerman and Pease [54] related to the use of microchannels in single phase heat transfer, similar studies have been carried out with two-phase flow through microchannels for heat transfer applications. The heat removed by this method is much greater than can be realised with forced air convection or single phase flow in microchannels. The use of two phase flow in microchannels with heat fluxes of between 300 [74] and $400\ Wcm^{-2}$ has been reported [75].

The behaviour of two phase flow in the microchannels is not well understood at typical microchannel dimensions ($\leq 100\ \mu m$) as many of the assumptions used in traditional macroscale heat transfer theory are no longer valid at the microscale. This has impeded the development of two phase flow microchannel arrays for commercial use. Further experimental data is required to develop a greater insight into two-phase behaviour at these scales.

The microchannels used in previous experimental studies have been produced using a variety of technologies. Metal substrates have been used in some studies, for example Mudawar and Bowers [76] formed channels by drilling 0.5 mm diameter holes in a block of copper. An array of parallel channels with depth of 0.7 mm and width varying from 200 to 600 μm was created by Peng [77] from grooves machined into a stainless steel block that also acted as heater with thermocouples attached to the backside of the block allowed the temperature to be monitored.

The use of silicon has attracted much interest in recent years due to its good thermal conductivity and the ability to achieve repeatable channel geometries smaller than can be achieved with conventional manufacturing through the use of silicon processing techniques. Smaller geometries allow novel fluid behaviour to be observed [78] [79]. Further advantages to using silicon including the possibility of directly integrating heating and sensing elements into the microchannels. This enables localised monitoring of performance rather than the averaged mea-

surements usually used in the past as well as the possibility of manufacturing the microchannel in the same substrate as the integrated circuit (IC) [80].

Single microchannels and arrays have been fabricated for experimental studies with integrated heaters and sensors to allow on chip measurements. Zhang [81] used the $50\ \mu m$ thick silicon on a silicon on insulator wafer to dictate the depth of the channels with the insulator acting as an etch stop. On chip thermometers and heaters were initially fabricated on the opposite side to the channels using doped silicon with an anodically bonded cover-plate allowing inspection of the channels [81] . To the best of the author's knowledge most microchannel heatsinks with integrated sensors and heaters have the sensors positioned on the backside of the wafer with the heater and not in the channels. Other examples of fabricated microchannels include those by Kuo [65], Jensen [63] and others [81] [82] [83].

Although most studies have been carried out under uniform heating conditions this does not accurately reflect the conditions on the surface of a microprocessor. Some studies have been conducted under non-uniform heating conditions [84] [85] but more needs to be done due to the unique challenges posed by this environment. Nonuniform temperature distributions can limit the reliability of microprocessors due to thermal gradients and associated stresses, as well as limit the effectiveness of some microchannel heatsinks. Crosslinked microchannel structures have been found to improve temperature uniformity for 1-D heat flux distributions. Whereas 2-D heat fluxes are best dealt with by using an optimised microchannel heatsink and these have been found to improve temperature uniformity across non-uniformly heated surfaces and lead to improved heat removal [84] [85].

Microchannel heatsinks that utilise two phase flow appear more likely to meet the future thermal management needs of the IC industry than other methods as they offer low thermal resistance, minimal area and volume, high heat removal coefficients and can be fabricated as part of the IC itself. The lack of understanding of boiling at the microscale has inhibited the development and optimisation of the heat-sinks with further optimisation required to develop microchannels suited for non-uniform heat distributions.

2.5 Conclusions

Thermal management methods based on two-phase fluid flow are often agreed to be the best solution for dealing with the heat fluxes predicted to be generated by microprocessors in the fu-

ture. Of the these methods heat-pipes are not suitable for the relatively small surface area of microprocessors and both jet impingement and spray cooling are relatively complex to implement making them of less commercial interest. This leaves two phase flow boiling in microchannels as the method thought to offer the most promise.

Two phase microchannel cooling is simpler to fabricate and implement and offers comparable heat transfer coefficients to jet impingement and spray cooling. The use of surface enhancement in conjunction with two phase microchannels offers greater improvements still. However there is a need for greater understanding of the mechanisms involved with boiling at the scales involved to improve the major issues affecting widespread adoption of this method such as temperature non-uniformity. Such experimental studies require microchannels that allow direct measurement of wall temperature and observation of boiling. Novel microfabrication processes are required to create devices that will meet these and other requirements. The following chapters describe the work undertaken to contribute to achievement of these goals.

Chapter 3
Silicon microchannels

3.1 Introduction

Advancing the understanding the behaviour of two phase flow at the microscale can be better achieved through the use of a controlled environment. Microfabrication is best suited to create such environments as it can routinely create structures with a smaller tolerance and more accurate dimensions than conventional fabrication techniques producing more repeatable results across multiple devices. Microchannels are suitable structures for use with fluids as the direction of flow is controlled. Additionally multiple designs of varying dimensions can be produced on the same wafer allowing the relationship between heat transfer and channel dimensions to be determined.

3.2 Silicon microchannel arrays

Microchannels have been fabricated using a variety of methods [86] with the most common being bulk micromachining and surface micromachining. Laser micromachining, micro-moulding and the patterning of epoxies have also been used to a lesser extent. While this thesis is focussed on the use of microchannels for improving the understanding of liquid heat transfer at the microscale they have many applications in microfluidics [87] [88] in areas such as biological and chemical analysis. This section will describe some of the methods suitable for fabricating microchannels, together with their advantages and disadvantages.

3.2.1 Bulk micromachined channels

Bulk micromachining is a widely used method of fabricating structures by the patterned etching of substrates [89] [90]. Etching can occur either using wet isotropic or anisotropic etching and dry isotropic or anisotropic etching with Fig. 3.1 showing typical etch profiles.

Isotropic etching, where the etch rate is not direction dependant, can use either an aqueous or gaseous etchant. One commonly used silicon etchant is a mixture of hydrofluoric acid (HF),

(a) Wet anisotropic etching (b) Dry anisotropic etching (c) Isotropic etching

Figure 3.1: *Typical etch profiles*

nitric acid (HNO_3) and acetic acid (CH_3COOH) with the shape of the resulting channel determined by the ratio of these acids [4] [90]. An example of a dry isotropic etchant would be xenon difluoride gas which also etches silicon.

Wet anisotropic etching is where the crystal planes of silicon etch at different rates. Examples of such etchants for silicon include potassium hydroxide (KOH), ammonium hydroxide, tetramethyl ammonium hydroxide (TMAH) and ethylene diamine pyrochatechol (EDP) [4] [91] [92]. The resulting etch geometry largely depends on the slowest etching crystal planes with a trapezoidal or triangular cross section easily achieved, with vertical sidewalls being possible with (111) silicon substrates.

Dry anisotropic etching includes plasma based etching, reactive ion etching (RIE), sputter etch and ion beam etching. Plasma etching involves applying a RF voltage across two electrodes. The reactant gas that is usually based on fluorocarbon chemistry is situated between these electrodes and with an applied electric field due to the RF voltage is used to generate the plasma. Vertical sidewalls are easily achieved when using this method to etch a wide variety of materials. Another variant of this technique that has become of great use in the micromachining industry is a deep reactive ion etching (DRIE) process developed at Bosch [93], which utilises alternating cycles of etching and passivation to achieve anisotropic features.

These etching methods can be used to pattern the substrate to form microchannels, which can then be sealed using either wafer-bonding [94] [95] [96], or by thin film deposition as shown in Fig. 3.2 [97] [98]. Bulk micromachining has been used to fabricate microchannels for heat transfer studies with many of them produced by sealing the channels using wafer-bonding [99] [100] [101] [102].

Optical inspection of the channel is possible with sealing methods if Pyrex glass is chosen as

(a) Etching substrate via etch holes

(b) Sealing channel through thin film growth or deposition

Figure 3.2: *Bulk micromachining of microchannels using thin film deposition to seal channels*

the capping wafer for wafer-bonding or if the thin film covering the channel is transparent. This is advantageous for many applications where the activity within the channel needs to be observed. Other advantages with the wafer-bonding method is that it is not limited to simple structures as complex microchannel structures such as stacked microchannels can be created using this approach [100]. Additionally with wafer-bonding the channel size, depth and shape are not constrained by the need for etch holes or wet etching.

A disadvantage with sealing the channel using wafer-bonding is that it requires the surface of both wafers to undergo rigorous cleaning processes to remove any particulates or other forms of contamination [103]. Voids in the bond as a result of unwanted particulates may lead to leakage of fluid from the channels or in some extreme cases the delamination of the capping wafer with both of these being very undesirable.

3.2.2 Surface micromachined channels

Surface micromachining involves the use of successive thin film deposition and selective etching steps to build structures on the substrate [104] and has been used to fabricate microchannels with a variety of materials [105] [106] [107] [108]. Channels are usually formed as shown in Fig.fig:surfacemicromachinedprocess, where a sacrificial material is deposited and patterned (Fig. 3.3(a)) using materials such as aluminium [109], silicon oxide [110] and poly-

(a) Patterning of sacrificial layer

(b) Thin film deposition

(c) Removal of sacrifical layer

Figure 3.3: *Typical process for surface micromachined channels*

mers [104] [111]. A second material is deposited over the sacrificial layer (Fig. 3.3(b)) and the sacrificial layer etched away, leaving a microchannel (Fig. 3.3(c)).

It is easier to integrate temperature sensors for localised measurements with surface micromachined channels [112] [113] [114] by forming the temperature sensors on the substrate surface and building the channels around them. The accuracy of measurements taken using these channels can be improved by reducing heat loss from the channel into the substrate by suspending the channel above the substrate using sacrificial etching [81].

This method also allows visual inspection of the channels through the use of transparent thin films. This method allows relatively simple construction and the integration of electronics. However the main disadvantage is that the height of surface micromachined channels are limited by the thickness of the sacrificial layer and because of this the typical height of surface micromachined channels are between 1 and 5 μm.

3.2.3 Other methods

Examples of other microchannel fabrication methods include SU-8 [115] [116] [117], moulding of plastic substrates, laser micromachining [118] [119] [120] and LIGA.

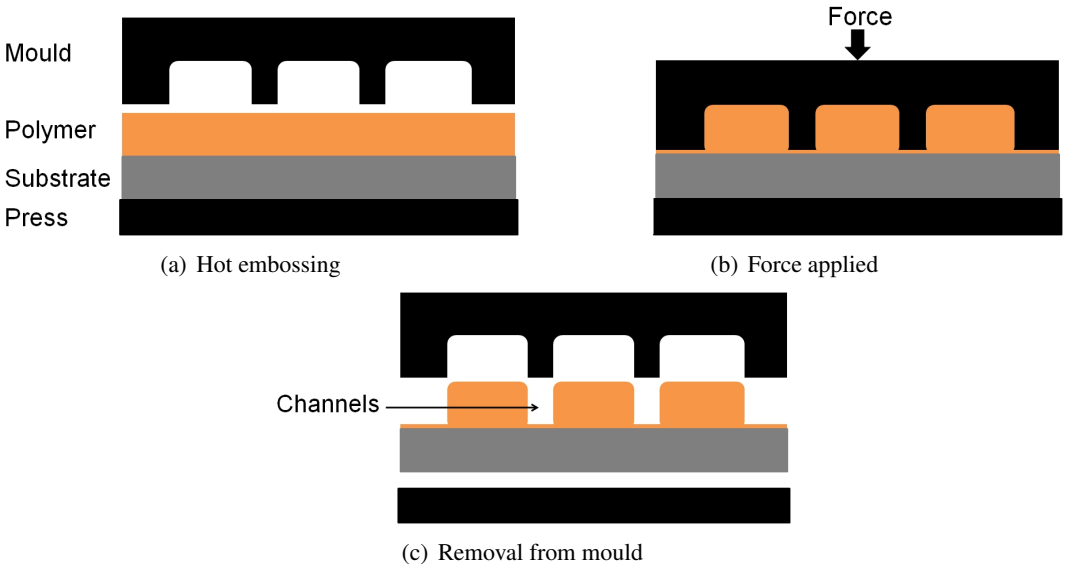
3.2.3.1 SU-8

SU-8 is a negative photoresist that can be used to achieve high aspect ratio structures [121] [122]. The SU-8 is spun onto a substrate like any resist and patterned using photolithography to form the desired structure. The height of the structures can be controlled by adjusting either the spin-coating process or the composition of the SU-8, although many suppliers do provide several premixed solutions for different heights. SU-8 film thicknesses of $1.5mm$ have been reported [115]. As the SU-8 only forms the sidewalls of the channels some means of sealing the channels is required.

Although SU-8 is mechanically, thermally and chemically resilient the most suitable bonding that can be performed with this material is adhesive bonding. Adhesive bonding allows low temperature bonding, with bond strengths of up to 8 MPa reported [117]. When heated the SU-8 can form an adhesive bond with a Pyrex cover-plate but as with other forms of adhesive bonding care must be taken to ensure against clogging of channels and possible contamination of the channel [86]. Additionally application of the capping wafer may also cause distortion of the sidewalls. The advantages of using SU-8 include the relatively rapid and low cost nature of the fabrication.

3.2.3.2 Hot embossing

Hot embossing is another method that can be used for microchannel formation. Pressing a master-mould into a soft material such as a polymer forms a negative impression of the master-mould, forming the channel. Nickel has been widely used in the past as the master-mould material with silicon becoming more commonly used [123] [124]. Recently polymers such as fully cured SU-8, other epoxy resins and PDMS have been also been utilised for this purpose [125] [126] [127]. The mould can be used to reproduce many devices from polymer materials such as PMMA. The number of channels that can be created with a mould depends on the lifetime, care and usage of the mould with nickel moulds lasting longer than cheaper polymer moulds.



(a) Hot embossing (b) Force applied

(c) Removal from mould

Figure 3.4: *Hot embossing process*

A typical hot embossing process is illustrated in Fig. 3.4. The polymer coated substrate is softened by placing it into the embossing system and heating to just above the glass transition temperature of the polymer in a vacuum. Simultaneously the mould is also heated up to the same or a slightly higher temperature and then pressed into the polymer as shown in Fig. 3.4(b). The mould and polymer are then cooled to below the glass temperature and separated as shown in Fig. 3.4(c) [128]. This method is best suited for simple, planar microchannels with low to medium aspect ratios. However, the structures formed by this approach may be subject to high residual stresses [122].

3.2.3.3 Laser micromachining

Laser micromachining patterns substrates through the use of laser ablation and has been used to form microchannels [129]. The ablative mechanism is a combination of photochemical and photothermal reactions and relies on the absorption of photons by the substrate to successfully remove material. The wavelength, material and pulse duration all play a part in determining the quality of the resulting structures [120] [122]. The choice of wavelength is especially important to minimise any unwanted thermal damage as longer wavelengths result in thermal reactions dominating the ablation mechanism. Optimisation of the wavelength for the material being machined maximises the absorption of the laser energy. Another factor which affects the resulting structure quality is the duration of the laser pulse as shorter pulses result in less

thermal damage to the substrate at the expense of machining speed while larger pulses cause more thermal damage but quicker machining.

The most commonly used method of laser micromachining of channels is serial processing which is also known as direct writing which has no need for an expensive mask as the laser is guided across the substrate by a data file generated by a CAD program. Serial micromachining is best suited for small batch sizes. Laser micromachining can be used to produce complex designs including three dimensional shapes or structures with varying wall shapes and aspect ratios on a variety of substrates [118] [130] [119] [131].

3.2.3.4 LIGA

LIGA (Lithographie, Galvanoformung, Abformung) is another method that has been also used to develop microchannels [132] [133] [134] [135]. This process involves the use of x-ray lithography, electroplating and micromoulding to create devices with heights of several millimetres and aspect ratios up to 200 [136]. A wide range of materials including metals, plastics and ceramics [137] [138] [139] [140], are compatible with this method. However, x-ray lithography and the creation of micro-moulds make this a costly process.

3.2.4 Selection of machining method

Each of the approaches discussed above have advantages and disadvantages that are summarised in Table 3.1. These along with the design of the device to be fabricated and the available resources, determine which approach is most appropriate. The microchannels fabricated for this project were bulk micromachined from silicon enabling high aspect ratio structures to be created which is not possible using surface micromachining.

Silicon was selected as the base material as it has a good heat conductivity of 150 WmK^{-1}, a thermal expansion coefficient 7 times lower than copper and 10 times lower than aluminium and is easily patterned. More importantly it also offers the future possibility of microchannel heat sinks to be directly integrated onto microprocessors . Polymers and SU-8 would not be suitable for heat transfer microchannels as they are thermal insulating materials. Additionally, the chemical and thermal constraints imposed by these materials would limit the process steps usable.

Method	Advantages	Disadvantages
wafer-bonding of bulk etched channels	Deep channels possible, simple method, stacked channels possible	Stringent cleaning requirements for wafer bonding
Thin film sealed bulk etched channels	Simple method, stacked channels possible	Limited width of channel possible
Surface micromachined channels	Simple method	Limited height, fragile structures, thin-film stress may be problematic
SU-8 channels	High aspect ratios rapid fabrication mechanically stable	Adhesive wafer bonding may lead to clogged channels
Hot embossed channels	Rapid fabrication, variation of aspect ratio across substrate possible	Limited to polymers and other soft materials, stress in post-released structure
Laser micromachined channels	Rapid fabrication, complex geometries possible, can machined wide variety of substrates	Possibility of thermal damage and alteration of substrate material properties
LIGA formed channels	Large aspect ratios possible, variety of materials can be used	Expensive

Table 3.1: *Comparison of microchannel fabrication techniques*

	Design 1	Design 2	Design 3	Design 4	Design 5	Design 6
Channel width (μm)	50	50	100	100	150	150
Wall width (μm)	50	100	50	100	50	100
Channel depth (μm)	300	300	300	300	300	300
Channel length (cm)	1.5	1.5	1.5	1.5	1.5	1.5
Number of channels	100	66	66	50	50	40
Cooling area (cm^2)	2.25	2.25	2.25	2.25	2.25	2.25
Hydraulic diamater (μm^2)	85.71	85.71	150	150	200	200

Table 3.2: *Design parameters of microchannel arrays*

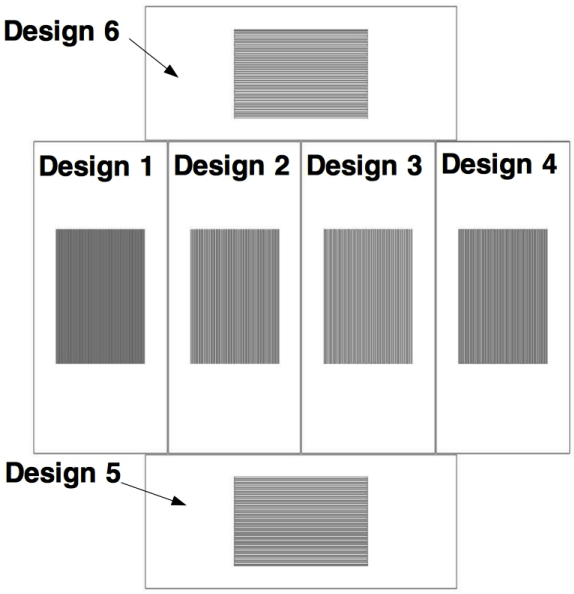


Figure 3.5: *Mask design for microchannel arrays*

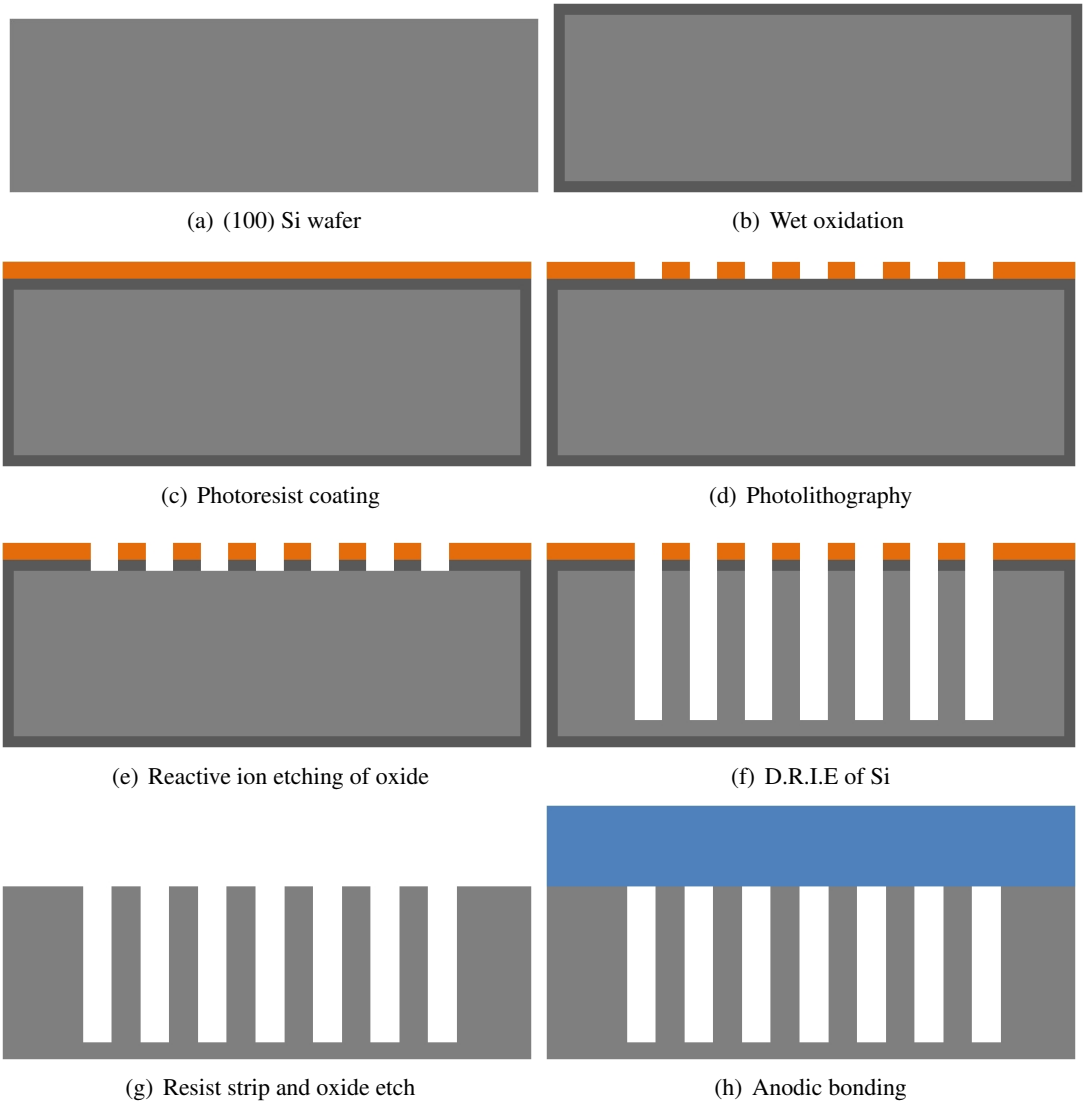
3.3 Design

Initially six designs of rectangular microchannels were selected to be fabricated, with the dimensions differing as shown in Table 3.2. Tests carried out on these designs by the project collaborators in University of Edinburgh were used to determine the optimal geometry[2].

The mask layout was arranged so that all the arrays could be fitted on the one wafer as shown in Fig. 3.5. The large areas surrounding the microchannels were designed to help improve the anodic bond between the arrays and the Pyrex capping wafer.

3.4 Fabrication

Fabrication of these microchannels consisted of a series of thermal oxidation, photolithography and etching steps. This section gives an overview of this process with further detail available in the runsheet shown in the Appendix A (Table A.1).



(a) (100) Si wafer (b) Wet oxidation

(c) Photoresist coating (d) Photolithography

(e) Reactive ion etching of oxide (f) D.R.I.E of Si

(g) Resist strip and oxide etch (h) Anodic bonding

Figure 3.6: *Fabrication process for silicon microchannel array*

The microchannel arrays were fabricated on 3 inch, p-doped, (100) silicon wafers. A 2.5 μm thick oxide was grown (Fig. 3.6(b)) and measured using a Nanospec AFT spectrophotometer. The wafers were coated with 1.5 μm of SPR-350 positive photoresist (Fig. 3.6(c)) which was exposed and developed (Fig. 3.6(d)). The exposed oxide was etched to form a hard mask using the Plasmatherm reactive ion etcher (Fig. 3.6(e)). RIE is selected to pattern the oxide rather

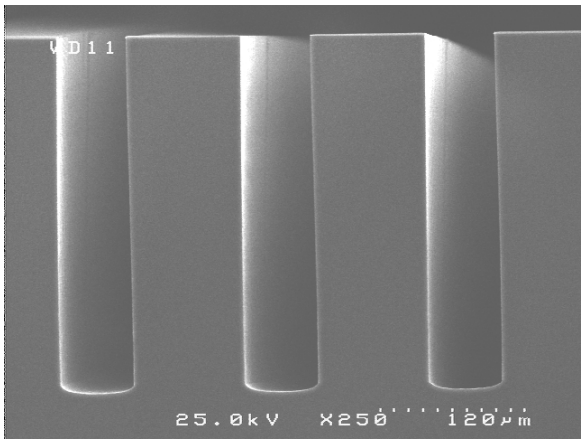


Figure 3.7: *Side profile of anisotropically etched channels*

than anisotropic wet etching to ensure minimal undercutting and a rectangular cross-section. An oxide hard mask was used rather than a photoresist mask as the selectivity of the silicon to this photoresist is 50:1 making it unsuitable as a mask layer when etching the desired 300 μm deep silicon channels.

The exposed silicon was anisotropically etched using the Bosch process down to a depth of 300μm (Fig. 3.6(f)) which was measured using a Vickers CSS microscope and it was found that the depth of the channels varied by $\pm 1\%$ across the wafer. The Bosch process utilises a repeating sequence of steps to etch deep, near vertical structures with aspect ratios of up to 20:1. The first step uses C_4F_8 passivation gas to coat the wafer with a thin $(C_xF_y)_n$ polymer layer. This passivation polymer layer is removed where it is perpendicular to the direction of the ion energy which exposes the underlying silicon. This silicon is isotropically etched by SF_6 before the sequence repeats. Adjusting the duration and process parameters of the etch and passivation steps can be used to optimise the process performance [141] [142] [143]. An example of the channels formed using the Bosch process is shown in Fig. 3.7.

Any photoresist remaining on the wafers after etching is removed using an O_2 plasma (Fig. 3.6(g)). The remaining oxide hard mask layer is then removed by placing the silicon wafers into hydrofluoric acid (HF) for 5-10 minutes and rinsing afterwards (Fig. 3.6(g)). To ensure a good quality anodic bond any particulates or organic residue are removed from the wafer surfaces by placing the silicon and Pyrex wafers into a piranha etch (1 part of hydrogen peroxide (H_2O_2) to 2 parts of sulphuric acid (H_2SO_4)) for 10 minutes. The wafers are then removed and rinsed thoroughly in de-ionised water. Finally the glass and silicon wafers are dried in a LTEC Marangoni drier.

The wafers are manually aligned using the wafer flats on the chuck before being loaded into the Suss Microtec SB8 substrate bonder for anodic bonding (Fig. 3.6(h)). After bonding the wafers are diced along the inlet and outlet of the microchannels so that each die measures 1.5 mm by 1.5 mm. The channels may be filled with grit and residue from dicing and must be flushed out using IPA and de-ionised water and dried afterwards.

3.5 Results

3.5.1 Bond delamination

It was noted that the anodic bond between the silicon and the glass for the microchannel arrays of design 5 and 6 as defined in Table 3.2 often delaminated after wafer dicing as shown in Fig. 3.8. These arrays were situated at the top and bottom of the wafer respectively (the bottom is considered nearest to the major flat of the wafer). The cause of the delamination may be a result of the forces applied by the dicing saw and pressurised water and air or the smaller bonding area resulting from wider channel. The percentage area of the microchannel array in comparison to the total die area is shown in Table 3.3.

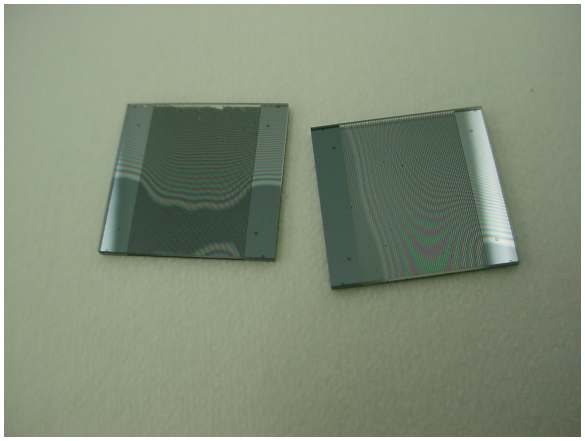


Figure 3.8: *Delamination of anodic bond post dicing*

The anodic bond strength is largely dictated by the voltage, temperature and pressure applied to the Pyrex-wafer stack. As temperature increases within the bonding chamber the sodium oxide within the glass breaks down into sodium and oxygen ions. The negative oxygen ions are attracted towards anode and upon reaching the silicon-glass interface they react with the silicon to form a thin layer of silicon oxide that creates the bond between the glass and silicon.

Device design	Percentage area of microchannels
1	33.33
2	22
3	44
4	33.33
5	50
6	40

Table 3.3: *Percentage area of device composed of microchannels for each array design*

The initial anodic bond recipe can be divided into two parts with the first one occurring when an initial voltage of -1000 V is applied to the wafers from the central pin for 15 seconds to create a small bond at the wafer centre. This ensures that misalignment does not happen when the clamps are removed. Afterwards the second part occurs when a constant voltage of -400 V is applied across the wafers using both Y-shaped electrodes and central pin electrodes. This voltage is terminated when the measured current flowing between the anode and cathode drops to 5% of the maximum measured current. The change in current is a useful indicator of successful bond propagation. The temperature remains at $400°C$ during bonding.

Several techniques exist to determine the quality and strength of bonded wafers. One technique used to characterise these bonds involved the fabrication of equally spaced, raised titanium structures of known dimensions across the bare surface of a silicon wafer. This predefined patterned surface method is based on the principle that the void formed around each structure is proportional to the bond strength at that point as shown by the following equation

$$G_C = \frac{3h_1^3\delta_b^2}{c_1 a^4(1+\gamma\eta^3)} \tag{3.1}$$

where the void length (a) formed due to a step of a height, δ_b was used to calculate the interfacial surface energy (G_C) of the bond [144]. Properties such as glass thickness ($h1$) and compliance (c_1 as well as the compliance ratio (γ) and height ratio (η) of the two substrates also affect the surface energy of the bond. This method is discussed in greater depth in Chapter 6.

A plot of the variation of bond surface energy over the wafer surface created using the void measurements is shown in Fig. 3.9 and the average surface energy over the wafer was found to be $7.04 \times 10^3 Jm^{-2}$. This measurement was repeated three times and the average surface energy over these runs was $6.34 \times 10^3 Jm^{-2}$. The strongest parts of the bond are situated near

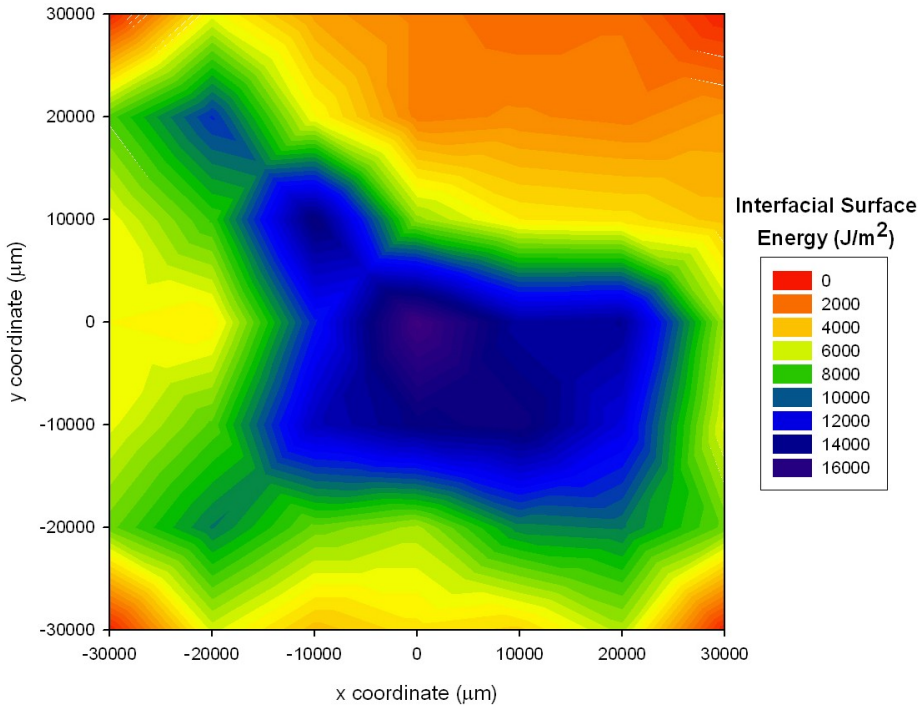


Figure 3.9: *Map of interfacial surface energy over wafer area for anodic bond recipe*

the centre of the wafer due to the initial bond that is formed only using the central pin electrode.

The wafers become fully bonded together during the second part of the bonding sequence. This second bond uses the Y-electrodes and the central pin electrodes. The Y-electrode consists of three electrodes with an angle of 120° between them. This electrode is shown in Fig. 3.10. During this stage of the bonding process the electrodes are at a potential of -400 V with the bond propagating out from the electrodes to bond the entirety of the wafers together. Consequently the area directly under the Y-electrode undergoes the bonding process for the longest period of time as the bonding wave propagates out to the edges. This can explain the bond energy pattern observed in Fig. 3.9 where the strongest areas of surface energy are also arranged in a Y-shape like the electrodes. This indicates that the bond strength is affected by distance from the bonding electrodes with this recipe.

The bond energy nonuniformity is suspected to be a contributing factor in the delamination of the type 5 and 6 microchannel arrays after dicing as the location of the maximum surface energy mimics the Y-shaped pattern of the electrode, which may result in either a surface energy gradient or low surface energy across them. Whether the effect of channel geometry is also a contributing factor is inconclusive.

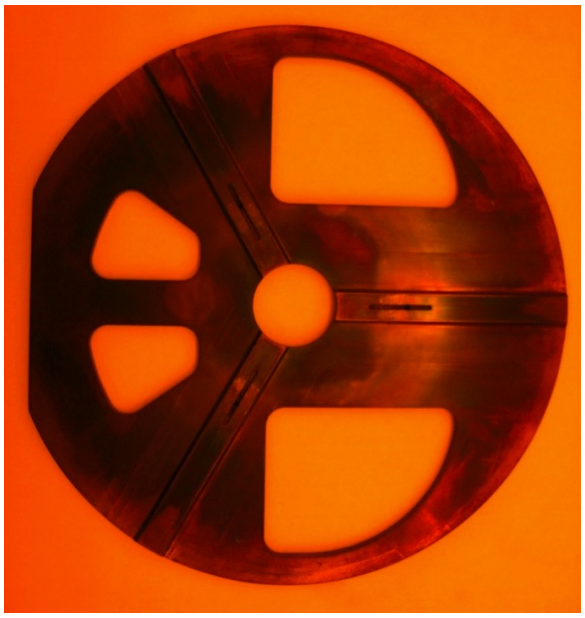


Figure 3.10: *Y-electrode used during anodic bonding*

3.5.2 Heat transfer

Collaborators on the project characterised the heat transfer performance of these microchannels [2] for both single and two phase heat transfer experiments as illustrated in Fig. 3.11. The experiments were carried out under uniform heat flux conditions by placing the microchannel heat sinks in contact with a copper block heated by a resistive heater. The heat flux was measured by four thermocouples embedded into the copper block 6 mm apart. Heat fluxes of approximately $175\ Wcm^{-2}$ were removed with these devices under uniform heating conditions. Information on the uncertainty of the measurements was not provided.

The relationship between the temperature and pressure drop within the channel was also investigated with these devices and some of these results are shown in Fig.3.12. Pressure drops within microchannels caused by the onset of two phase flow as not desirable if these systems are to become widely used.

A disadvantage of this device was that due to the use of external sensing the thermal resistance between the silicon chip and the copper block led to misleading average chip temperatures and slow response times. This was solved by using both an integrated heater and sensors in future designs as shown in Fig. 3.13. The heater is designed in such a way to enable the delivery of non-uniform heating conditions, which is closer to the conditions present on a microprocessor [38] [37] [2].

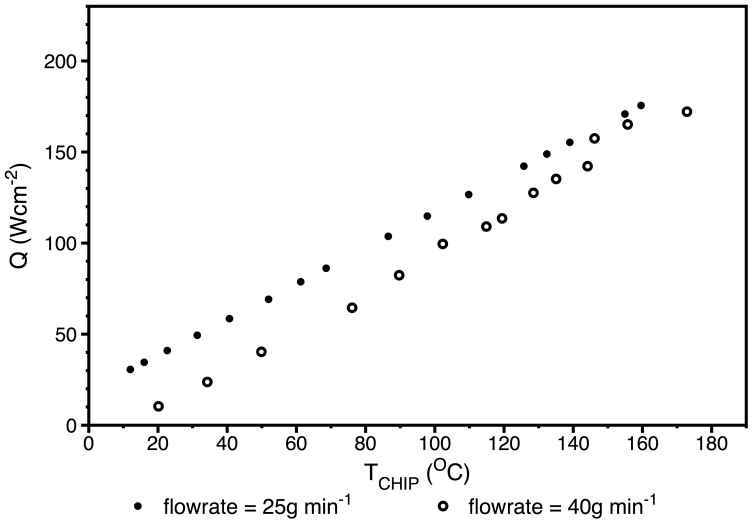


Figure 3.11: *Heat transfer as a function of temperature and flow rate using 100 μm wide silicon microchannels with 100 μm thick walls [2]*

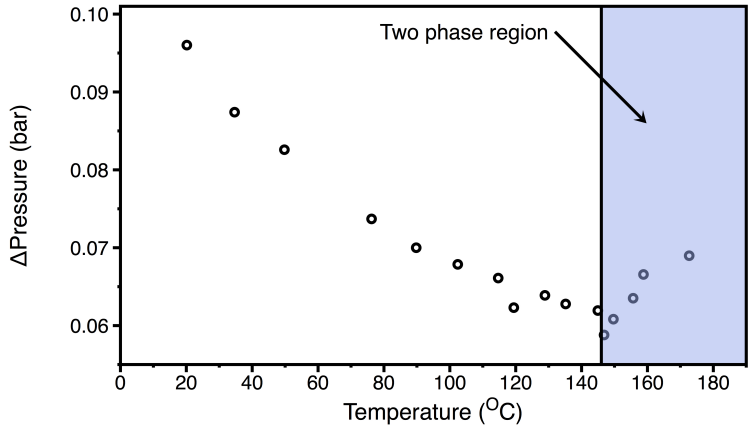
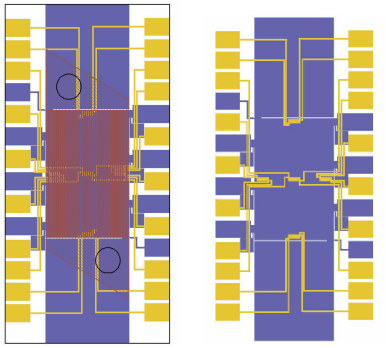


Figure 3.12: *Pressure drop as a function of temperature using 100 μm wide silicon microchannels with 100 μm thick walls [2]*



(a) Top View (b) Bottom View

Figure 3.13: *Schematic of silicon microchannel array (red) with integrated sensors (yellow) and heater (blue)*

The many contradictions between previous studies on the cause of various flow regimes, flow instabilities and heat transfer mechanisms have impeded the development of two phase flow cooling technologies. These microchannels in conjunction with external measurements and high speed imaging contributed towards the development of a better understanding of two phase flow, heat transfer mechanism, instabilities and bubble dynamics. These devices also informed decisions made during future design iterations with colleagues.

3.6 Conclusions

A process for the fabrication of silicon microchannels using bulk micromachining and anodic bonding has been successfully demonstrated. These microchannels have been used to successfully remove heat fluxes up to 175 Wcm^{-2} under uniform heating conditions.

However some of the devices produced on each wafer did not have a sufficient bond strength to withstand the forces exerted by the dicing process. The need for a characterised process for the bonder required that the bonding process was optimised. Additionally the lack of integrated sensing elements sometimes lead to misleading average chip temperatures and also offered no further understanding of the effects of boiling at the microscale [2]. Use of integrated temperature sensors potentially enables localised heat flux measurements and together with an integrated heater could be used to approximate non-uniform heating conditions that are similar to the actual heat distributions experienced with microprocessors [38] [37] [2].

Chapter 4
Silicon microchannels with integrated tantalum sensors

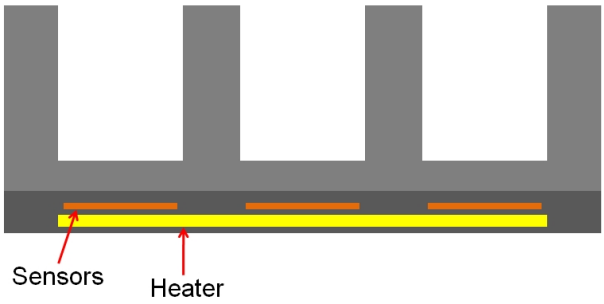
4.1 Introduction

The use of anodic bonding to seal the silicon microchannel arrays as described in the previous chapter allows optical observation of the boiling process at the microscale leading to a qualitative understanding of the boiling processes. However, the lack of any quantitative measurements limits what can be understood about the process. Measurements can be obtained through the use of sensors. External sensors cannot provide a direct measurement close to the boiling site as they are usually located away from the site and often the larger size and external location of these sensors leads to a spatially averaged measurement. The use of integrated sensors near the channel surface provides the best option for increased understanding of boiling at the microscale. The design, number and location of sensors can affect the accuracy and quality of the measurement with the best solution being a series of small sensors that enables multiple, discrete, local measurements. This is more desirable for this application because of the scale and size of the nucleated bubbles.

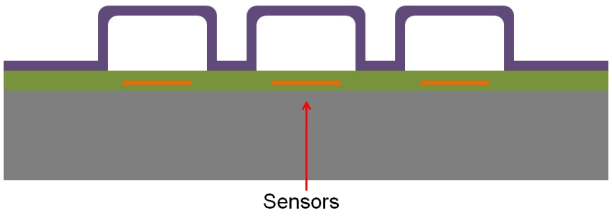
This chapter describes the design and fabrication of a microchannel that incorporates a series of sensors to allow localised measurements of temperature and heat flux. Although the design is for a single microchannel this process can be easily adapted for a micro channel array design.

4.2 Sensor integration

Sensors and heaters have been previously integrated with channels with the location of these integrated elements determined by how the channels were manufactured. Bulk micromachined channels usually have the sensors and heaters on the back of the substrate with a mass of silicon separating them from the channel floor as shown in Fig. 4.1(a) [65] [145] [146] [147]. The greater the thickness of the silicon between the floor of the channel and the sensing elements



(a) Bulk micromachined channels with integrated heating and sensing



(b) Surface micromachined channels with integrated heating and sensing

Figure 4.1: *Methods of integrating sensors with channels*

increases the spatial averaging of the measurements due to thermal conduction. This limits the spatial resolution of the measurements and inaccurate measurements will be obtained if this averaging is not taken into account. Thinning the silicon or bordering the device with deep channels that act as a thermal insulator to impede lateral thermal conduction are some techniques that can be used to decrease this averaging effect.

Sensors and heaters integrated into surface micromachined channels are often placed either on the back of the substrate like those found with the bulk micromachined channels or more commonly on the floor of the channel as shown in Fig. 4.1(b) [148] [112] [149]. The latter can be achieved by fabricating the channel around the sensors. This significantly reduces the effect of any heat spreading on measurements as well as allowing direct measurements. However, the surface micromachined channels are usually shallow and fragile and not suitable for experiments such as those planned for the channels described here.

4.3 Specifications

To facilitate visualisation of boiling it was desirable that the microchannel had a transparent cover to enable recording of bubble nucleation with a high speed video camera. To provide the desired heat flux of 200 Wcm^{-2} it was required that the heaters have a resistance of 1-10 Ω and could operate safely up to 50 V to give a maximum power of 250 W. The temperature sensors were required to have a resistance that was $\gg$ 700 Ω for high sensitivity.

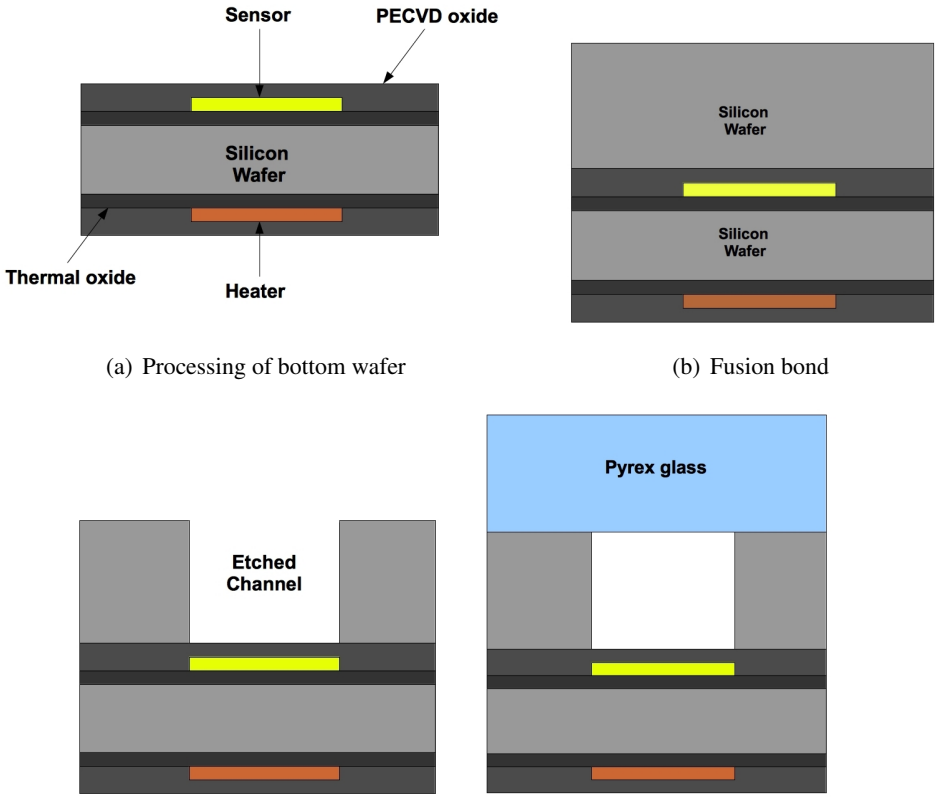
4.4 Design

A simplified process flow for the fabrication of the microchannels is shown in Fig. 4.2. The process flow can be summarised as the fusion bonding of two polished double sided wafers where one of the wafers has been processed to form heaters and sensors. After fusion bonding the channel is formed by etching through the top wafer down to the interface between the two silicon wafers. Finally a Pyrex wafer is bonded to the top silicon wafer to provide a transparent seal for observation of microboiling within the channel.

The resulting wafer stack is shown in Fig. 4.3. The heater, sensors and channel were designed to meet the above specifications. This final design originally required four light-field mask layers along with one each for the channel, the sensor, the interconnects and the heater.

4.4.1 Channel

Each device consists of a single channel with a reservoir at either end and as Fig. 4.4 shows three devices could be fabricated on each wafer. Each channel is 1.5 mm wide, 40 mm long and 385 μm deep. The depth is defined by the thickness of the silicon wafer. This gives a hydraulic diameter of these channels of 606 μm. The reservoirs have a length and width of 5 mm. Each channel is bordered by a groove that impedes lateral heat conduction from the channels ensuring the output of the heater is better targeted. The last feature of this mask design is the alignment marks situated at the right and left edges.



(a) Processing of bottom wafer

(b) Fusion bond

(c) Channel etching

(d) Anodic bonding

Figure 4.2: *Fabrication process for bulk micromachined channels with integrated sensors and heaters*

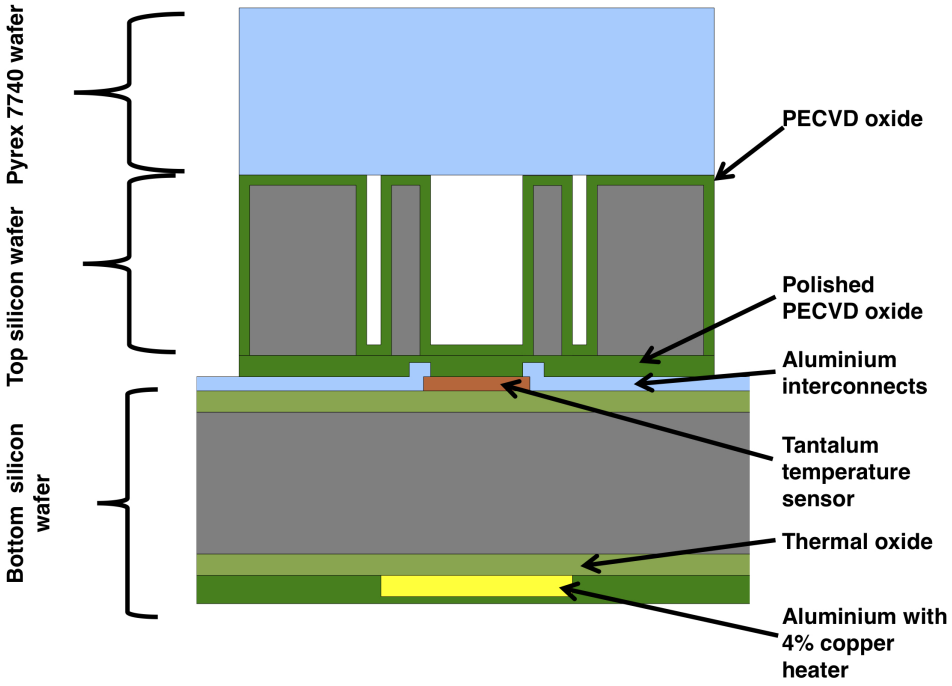


Figure 4.3: *Cross sectional diagram of device structure*

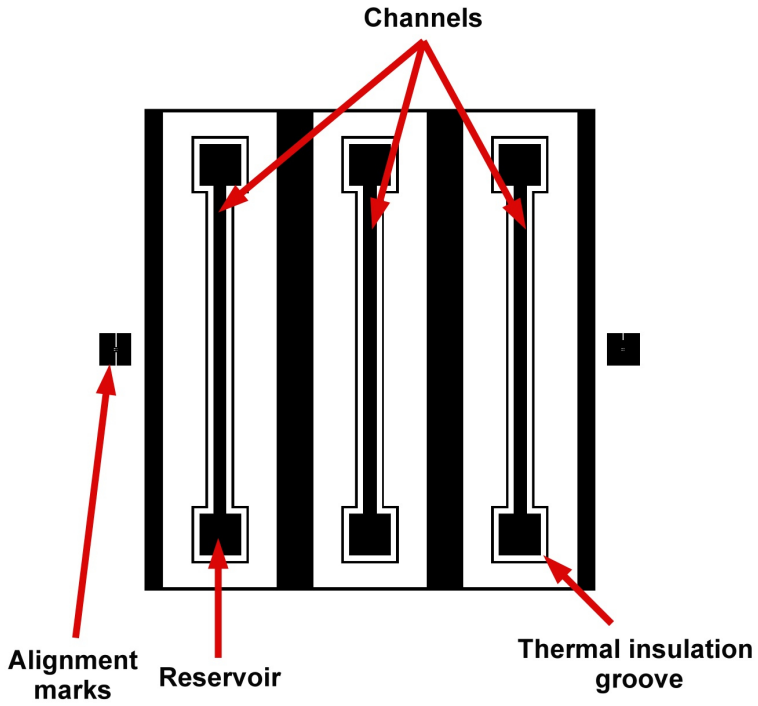


Figure 4.4: *Channel mask layout*

Material	Resistivity at $20^{O}C$ ($\mu\Omega cm$)	TCR ($^{\circ}C^{-1}$)
Aluminium	2.38	3600
Platinum	10.6	3927
Nickel	6.84	6900
Tantalum	13.1	4400

Table 4.1: *Resistive properties of some metals [4]*

4.4.2 Temperature Sensors

Local temperature measurements are required for the heat transfer experiments with the microchannels. This requires micro-scale sensors which are integrated with the channel. These sensors can be based upon either resistive or thermoelectric principles of operation. Thermoelectric temperature sensors otherwise known as thermocouples are based on the Seebeck effect and have similarities with the thermoelectric refrigerators mentioned in Chapter 2. These sensors are operated in a manner reverse to that of the refrigerators. In thermocouples a voltage is generated by a temperature difference between two junctions composed of two dissimilar materials. Resistive temperature sensors operate by utilising the change in resistance of a material due to changing temperature. This approach was selected to measure the temperature as these sensors are easier to fabricate and design as only one metal layer is required.

The values of the sheet resistance and the thermal coefficient of resistance (TCR) of the sensor material are key parameters in the design of these sensors. For many metals the resistance increases with increasing temperature (positive TCR) whereas materials such as some ceramics have a negative TCR.

Most materials have low TCRs which is an attractive attribute for many applications. However, for sensors this can lead to problems with poor signal to noise ratios. Conducting materials such as metals have relatively high TCRs which improves sensor performance. Table 4.1 details the temperature coefficient of resistivity for metals commonly used to fabricate micro-sensors at room temperature.

Platinum is often used in high quality temperature sensors because of its high TCR. However, as platinum is an expensive material and was not available in the sputter tools it was decided that initial sensors would be fabricated using tantalum. This metal was chosen as it has a TCR and resistivity similar to that of platinum.

The sensors were designed for high sensitivity and accuracy. The change in resistance as a

function of temperature may be calculated as follows

$$R = R_0[1 + \alpha_R(T - T_0)] \tag{4.1}$$

where α_R is the temperature coefficient of resistivity, R_0 is the resistance at the initial temperature T_0. Likewise the sensitivity (α_T) of the resistance with respect to changing temperature may be given by

$$\alpha_T = \frac{dR}{dT} \tag{4.2}$$

Equation 4.2 shows that a high resistance for a given TCR results in a larger change in resistance for a set rise in temperature which potentially makes the measurement more sensitive.

$$\frac{dV}{dT} = I\frac{dR}{dT} \tag{4.3}$$

The temperature is determined by recording the change in voltage across the resistor for a given current. The rate of change of voltage with respect to temperature can be calculated by using Ohm's law in conjunction with equation 4.2 to give equation 4.3.

$$R = \frac{V_1 - V_3}{I_2} \tag{4.4}$$

Designing the resistors for use with Kelvin measurement techniques enables accurate measurement of resistance as required for resistive thermometry. As shown in Fig. 4.5 the resistor uses four terminals for Kelvin measurement with two of the terminals used for current flow, one as a current source and the other as a sink while the others two terminals are used as voltage taps. The current flows between these two pads while the voltage is measured across the voltage pads. A negligible current flows through the voltage path due to the high input impedance of the voltmeter, which ensures that the effect of any parasitic resistances is small in comparison to the sensor resistance and can be neglected. This arrangement ensures that only the resistance between the voltage taps is measured using Ohm's law in the form given by equation 4.4.

A large resistance is achieved by using a thin, narrow and long linear resistor. A serpentine

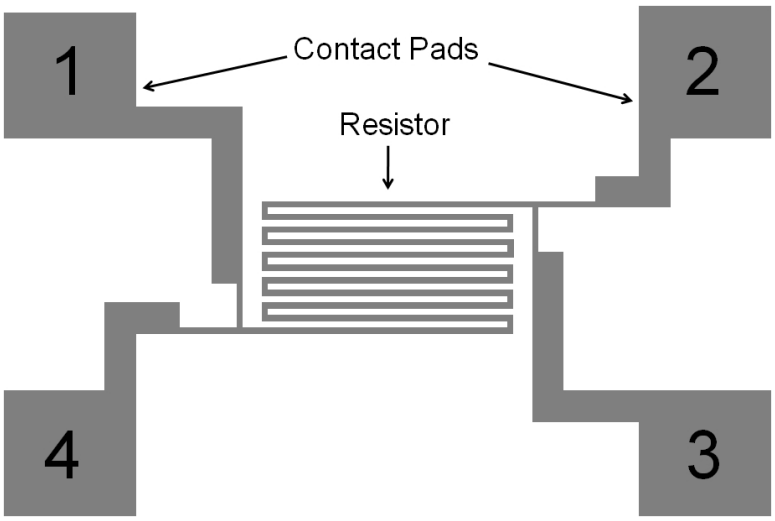


Figure 4.5: *Schematic of sensor layout*

layout coupled with a thin film enabled these requirements to be met while keeping the footprint of the sensor as small as possible to increase the spatial resolution of the measurement. The geometry of the sensors was initially designed using an estimated sheet resistance value of $3\Omega/\square$ to give a resistance of 4000 Ω. As shown in Fig. 4.6 nine temperature sensors are spaced with a pitch of 5 mm along the length of the channel floor. The sensor track is 15 μm in width with a 20 μm space between neighbouring turns with the sensor footprints all having the same 1.5 mm width as the channel. The sensor connections extended out to the edge of the device to the four contact pads used for Kelvin measurements with the paths aligned to lie under the interconnects as shown by Fig. 4.7.

The interconnect layer was designed so that all the sensors were connected together by a continuous metallisation to facilitate simultaneous anodization of the tantalum sensors at a later stage. The interconnect layer also provides an electrical connection from the sensors within the channel to the external instrumentation. It has been designed to be aligned with and cover part of the sensor mask layer to offer a level of redundancy by mirroring some of the layout of the sensor connections to the electrical contact pads at the edge of the device. This improves reliability in the case of a localised failure of one of the metal layers and also reduces the contact resistance. The interconnects to the contact pads were 100 μm in width, with the length varying.

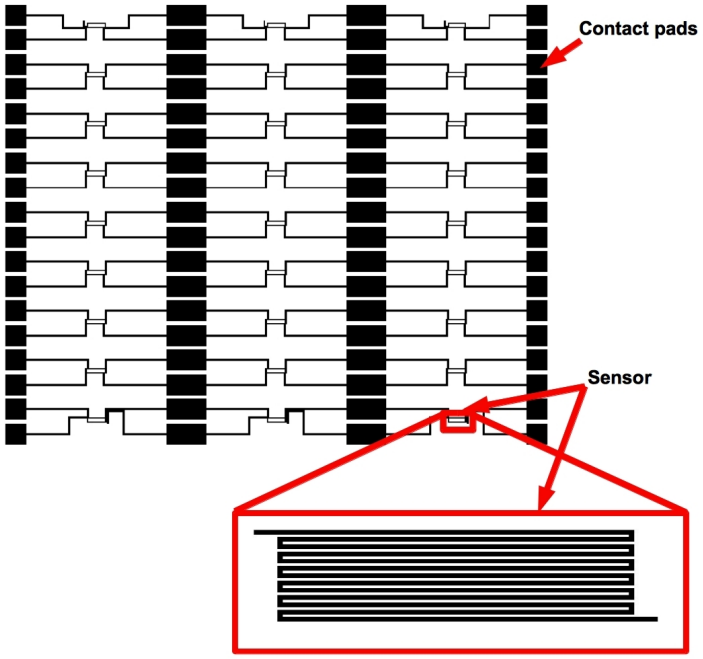


Figure 4.6: *Sensor mask layout*

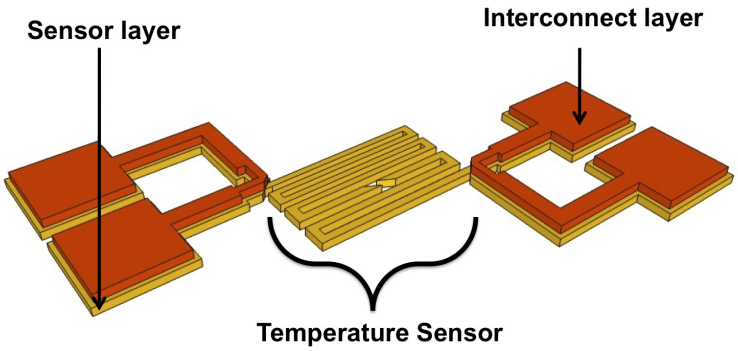


Figure 4.7: *Schematic of arrangement of sensor and interconnect layers*

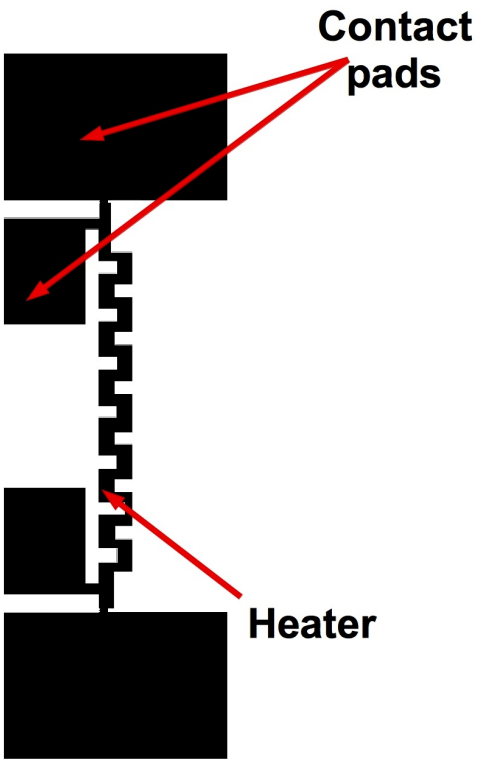


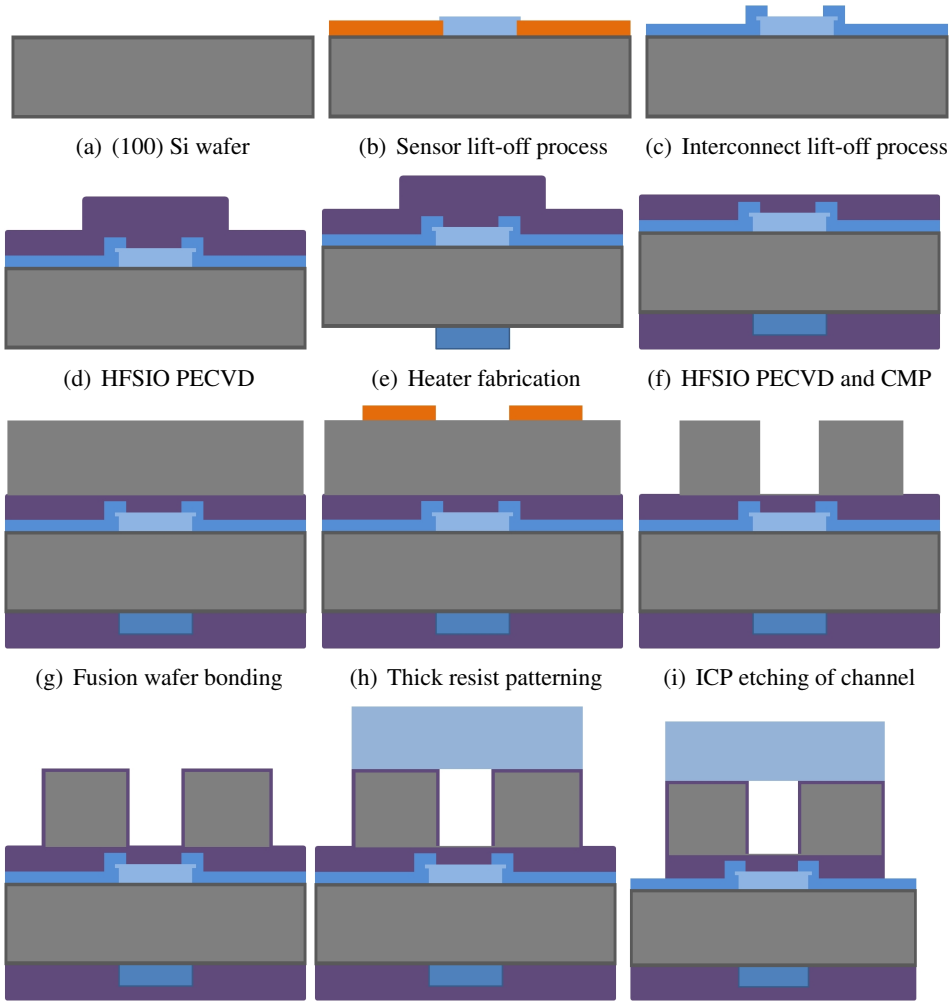
Figure 4.8: *Schematic of heater layout*

4.4.3 Heater

The heater shown in Fig. 4.8 consists of a resistor that is fabricated on the other side of the wafer to the sensors and aligned to be directly underneath the channels. It Joule heats the working fluid flowing through the channel and the heat dissipated by the resistor when current flows can be calculated as

$$P = I^2 R \tag{4.5}$$

The serpentine pattern of the heater was wider than the channel to ensure a uniform heat distribution along the length and width of the channel. Each turn of the heater was 574 μm wide with a gap of 23 μm between each turn designed to ensure a uniform temperature distribution across the channel. The heater footprint was 2.5 by 34 mm. Two large pads were used to terminate the heater for current sourcing and sinking with two smaller pads available for voltage taps (200



(a) (100) Si wafer (b) Sensor lift-off process (c) Interconnect lift-off process

(d) HFSIO PECVD (e) Heater fabrication (f) HFSIO PECVD and CMP

(g) Fusion wafer bonding (h) Thick resist patterning (i) ICP etching of channel

(j) HFSIO PECVD coating of exposed surfaces (k) Anodic bonding (l) Etch contact pads clear

Figure 4.9: *Detailed fabrication process flow for bulk micromachined channels with integrated elements*

μm wide) for Kelvin measurement of the resistance. The heater resistance was designed to be 10 Ω based on aluminium sheet resistance of 0.04 $\Omega/\square$ for a 1 μm film thickness. The heater was designed to be operated with 50 V across the heater with a current of 5 A, giving a heat flux of 250 W and current density of $8.710 \times 10^5 Acm^{-2}$.

4.5 Fabrication

The fabrication process is shown in Fig. 4.9. The first step is to grow 0.5 μm film of thermal oxide to provide electrical insulation between the sensors and the heaters on a 3 inch, N doped

(100) Si wafer. Double sided polished wafers are used to facilitate alignment, exposure and patterning during the double sided photolithography used in the process.

4.5.1 Tantalum deposition and patterning

Two methods of patterning the tantalum film which were reactive ion etching and lift-off were investigated. The film is sputtered onto the silicon dioxide using a Balzers BAS450PM. The thickness of the deposited film is 0.87 μm which has an average sheet resistance of 2.04 $\Omega/\square$.

4.5.1.1 Reactive ion etching of Tantalum

A layer of SPR-350 resist of 1.5 μm thickness is deposited and patterned on a film of tantalum. The exposed tantalum is then etched using a silicon tetrachloride plasma created within the STS multiplex RIE etcher at a measured rate of 0.01 $\mu m\ min^{-1}$. The etch uniformity is poor with this process but this can be improved by unloading the wafers out of the etch chamber every 20 to 30 minutes and rotating them by 90^O before reloading them and continuing the etch. An aluminium film of average thickness 0.5 μm is then sputtered onto the patterned tantalum and another 1.5 μm of SPR-350 photoresist patterned. The aluminium is etched using the same recipe as the tantalum and the etch rate was measured to be 0.017 $\mu m\ min^{-1}$.

It was expected that a further 0.3 μm of the tantalum sensors would be etched during the patterning of the aluminium. However, the tantalum sensors etched faster than expected with the sensor surface becoming roughened and in some parts etched away entirely with the average thickness changing from 0.87 to 0.29 μm over the course of the aluminium etch. The increased etch rate led to variation in resistor thickness across the wafer, causing the resistance of the sensors to increase, open circuits to form and in some cases etch away the tantalum sensors entirely. Because of this the patterning of the sensor layers by plasma etching was replaced by a lift-off process which enables the patterning of one metal layer without affecting previously patterned layers.

4.5.1.2 Lift off patterning

Lift off is a method of patterning materials that works by first by patterning a sacrificial material, in this case the resist upon which the material to be patterned is then deposited. After deposition the sacrificial layer is removed taking with in the material deposited on it but leaving

the patterned material layer. Although lift off patterning is a useful technique it is less generally used in industry due to problems that can occur with the method such as the retention and redeposition of the deposited material. Retention occurs when unwanted parts of the material remain attached to the wafer, either due to the sacrificial layer not being total removed or the material being well connected to the material deposited on the substrate. Redeposition occurs when particles of the deposited material on the sacrificial layer are removed only to re-attach at some other point on the substrate when the wafer is rinsed and dried [122].

A coating of AZ5214E negative photoresist is spun on the wafer using the 3 inch wafer track. The wafer is primed using HMDS adhesion promoter and baked before the resist is manual dispensed and spun at a speed of 3000 rpm. Next the resist undergoes a pre-exposure bake step when it is baked for 1 minute at 110°C. The resist is patterned by exposing it for 8 seconds and baked to activate the crosslinking agents in the exposed areas of the resist [150]. After the image reversal bake the wafers are flood exposed using the KS mask aligner for 45 seconds. AZ726 MIF is then used to manually develop the wafers, they are removed from the developer bath after 1 minute, 10 seconds and washed thoroughly using deionised water. The wafers are then gently dried using nitrogen gas. The average thickness of the resist after this processing is measured to be 6.2 μm using the Dektak surface profilometer.

After the lift-off resist is developed the wafers are subjected to a 1 minute descum using an oxygen plasma and a 5 minute argon mill. This ensures the good adhesion of the metal layer and the removal of any residual resist from the exposed areas. After tantalum sputtering, the wafer is placed in an ultrasonic bath of ACT resist stripper until clear of all unwanted metal. It is then thoroughly washed with deionised water to remove any flakes of metal which may have adhered to the surface and cause shorting at a later stage. Then it is washed with acetone, followed by IPA and again rinsed with deionised water one final time before being blown dry using nitrogen. The wafer is inspected under a microscope before proceeding to the next step. The lift off process is repeated to pattern the interconnects patterned in a 0.5μm thick aluminium layer that is deposited by sputtering for 90 minutes with the OPT.

4.5.1.3 Anodization

PECVD oxide is to be deposited on the sensors after patterning however PECVD has been known to produce rough and porous films. The presence of pinholes in the PECVD film may allow the sensors to come in contact with the working fluid resulting in electrolysis occurring

which would damage the sensors [151]. Other deposition methods such as CVD could not be used even though they produce pinhole free, smooth films as they require temperatures in excess of 450°C which are not suitable for the metal layers.

The selection of tantalum as the sensor material has an additional benefit in that it can be used to form tantalum pentoxide which is a high dielectric material with a permittivity between 8 and 25. This material acts as a protective coating for sensors [151] adding an extra level of assurance that contact between non-dielectric liquids and the conductive sensors cannot occur. Tantalum pentoxide can be produced through techniques such as reactive sputtering and anodization. Anodization was used to grow the tantalum pentoxide on the sensors as it can produce a reproducible conformal pinhole free coating at room temperature without the need for a separate patterning step [152]. Additionally the anodization process allows control of the passivation layer thickness and density through electrical means [153]. Anodizing is defined as the oxidation of metals by an electrolytic reaction, this process affects only the surface layers of the materials.

$$J = D \exp B \frac{V}{h} \tag{4.6}$$

The growth rate of a tantalum pentoxide film by anodization can be calculated using equation 4.6, where J is the current density, V is the potential applied across the electrodes and D, B and h are constants [154]. The oxide growth mechanism is due to a chemical reaction between the oxygen ions in an electrolytic gel and the tantalum film [152] that is controlled by the current density and the voltage [154]. The gel used to anodize the tantalum is composed of citric acid which had been mixed in a gel composed of DI water, digol glycol and sodium carboxyl methyl cellulose. This gel is manually deposited in a serpentine pattern to cover the sensors. Care should be taken to ensure that the gel does not contact the positive electrode causing a short circuit.

The growth rate of the film is determined by the current density which should be set between 1 and 10 $mAcm^{-2}$ for tantalum as a lower current density would result in a slow film growth rate while a higher current density would lead to unwanted overheating of the gel and possible damage. The applied voltage determines the film thickness for a given temperature and previously described work determines this to be in the region of 1.6 to 1.9 nmV^{-1} [155].

The oxide is grown when a voltage is applied between the tantalum anode and the electrolyte

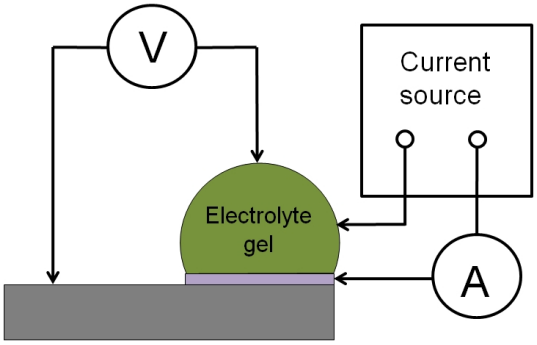


Figure 4.10: *Experimental setup for anodization of tantalum*

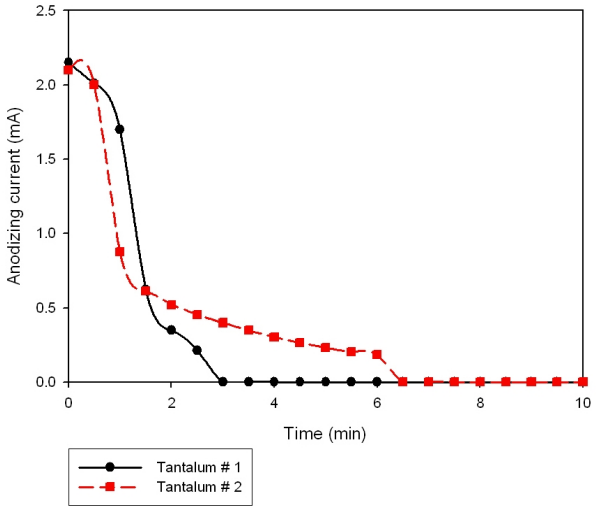


Figure 4.11: *Examples of anodization curves*

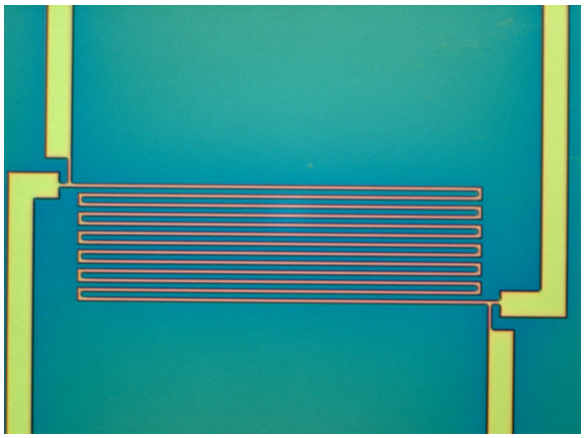


Figure 4.12: *Fabricated tantalum sensor*

which is the cathode. A current of 2 mA and a constant potential of 60 V is applied using the experimental set up shown in Fig. 4.10. The decay of current as shown in Fig. 4.11 was concurrent with increasing tantalum pentoxide thickness. The difference in the curves is due to a variation in gel area caused by manual application. However, the electrolytic reaction with the tantalum resistors is the one of interest and the variation in surface area of the tantalum sensors between batches is negligible so it is expected that the difference in tantalum pentoxide is minimal.

Given the current density of 0.11 $mAcm^{-2}$ and using similar growth rates characterised when initially developing this process [155] estimated the thickness of the pentoxide to be between 96 nm to 115 nm. After anodization the electrolyte gel is washed off with deionized water. This is followed by IPA and acetone and drying with nitrogen. The completed sensors with interconnects are shown in Fig. 4.12.

4.5.1.4 PECVD oxide deposition

PECVD high frequency silicon oxide (HFSIO) is deposited after the anodization of the tantalum to act as an extra layer of dielectric insulation. PECVD HFSIO is also attractive to use as it is a low temperature deposition method and produces lower intrinsic stresses. Wafer stresses are calculated by measuring the change in wafer bow due to film deposition and inserting the measurements into the Stoney equation

$$\sigma = \frac{1}{R}\frac{E}{6(1-\nu)}\frac{T^2}{t} \tag{4.7}$$

where σ is stress, R is the radius of curvature, t the thickness of the thin film and E, ν and T are the Young's modulus, poisson's ratio and thickness of the substrate respectively.

Radii of curvature of the wafers after a deposited oxide thin film of average thickness 2.4 μm were measured with the Dektak surface profilometer to be between 12.1 and 58.8 metres which translates into a stress between 1.5 and 7.6 GPa. This thickness allowed chemical mechanical polishing to planarize the wafer surface at a later stage as required by the fusion bonding process and to ensure that there are no artefacts remaining due to conformal coating of the sensors which may disrupt fluid flow or lead to the creation of unwanted artificial nucleation sites. To reduce the intrinsic stress of the thin films further the wafers are placed into an annealing furnace for 17 hours at 435$^{\circ}C$ [156] [157].

4.5.2 Heater

The heaters are fabricated on the opposite side of the wafer to the sensors. The PECVD layer protects the sensors from damage while the heaters are fabricated. The heaters are created on this bare surface by sputtering a 1 μm film of aluminium with 4% copper onto the thermal oxide. Aluminium with 4% copper is sputtered for the heater as it has a low resistivity suitable for Joule heating and it has been shown to have a lower diffusivity, which results in a reduced risk of electromigration compared to aluminium. Electromigration is a failure mechanism associated with integrated circuits that occurs under high temperature, high current density conditions such as during the operation of the heater. This phenomenon results in metallic ions migrating under the influence of thermal and electrical forces, which leads to either gaps in the metallic path or spreading of the metal to neighbouring tracks occurring resulting in open or short circuits respectively. This reduces the reliability and lifetime of the devices. The current density in the heater was calculated to reach $8.710 \times 10^5 A\ cm^{-2}$ at the maximum current of 5 A. For a conducting material such as aluminium the likelihood of electromigration increases with a high current density (usually in the range of 10^6 to $3 \times 10^6 A\ cm^{-2}$). The average sheet resistance of the film was measured to be approximately $1 \times 10^{-1} \Omega/\square$.

The sputtered metal film is coated with a 1.5 μm film of SPR-350 photoresist which is exposed and developed using steps described in Chapter 3 with the exposed metal etched in the STS Multiplex RIE Etcher for 60 minutes. The resist is removed by barrel ashing for 30 minutes and then placed in an ultrasonically agitated water bath of ACT-CMIS resist stripper for 15 minutes to ensure a clean and resist free surface. An example of a completed heater is shown

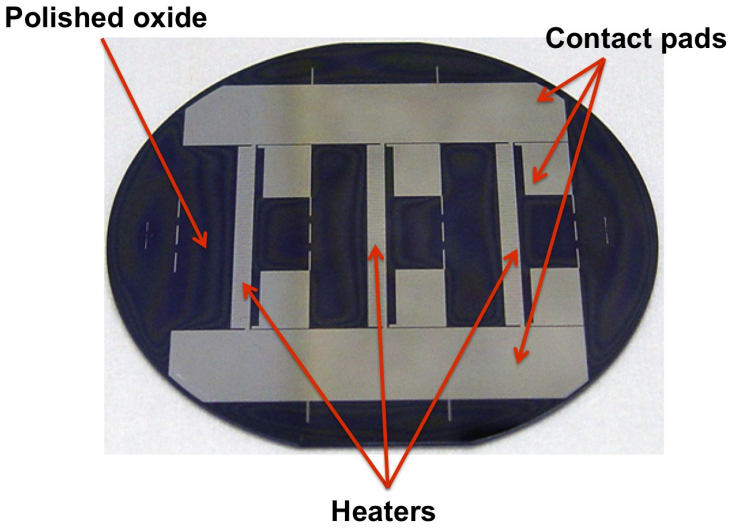


Figure 4.13: *Underside of partially fabricated wafer showing heaters*

in Fig. 4.13. Finally the backside of the wafer is coated with 2.5 μm of PECVD HFSIO before the wafer is again annealed at 435°C for 17 hours to reduce the intrinsic stress.

4.5.3 Fusion bonding

Fusion bonding is defined as the joining together of two wafers using applied temperature and involves several preparatory steps including polishing, cleaning, bonding and finally annealing. It is used to adhere a virgin double sided polished silicon wafer to the processed wafer containing the sensors and heaters after the last PECVD oxide film is annealed. The following sections detail this process.

4.5.3.1 Polishing

The surface of the processed wafer is polished to ensure that the deposited oxide has an average surface roughness (Ra) of less than or equal to 0.5 nm. This is achieved using chemical mechanical polishing (CMP), which utilises a chemical reaction to increase the mechanical removal rate of a material and is a commonly used method for planarising wafers. The wafers are polished for 6 minutes on the sensor side and 4 minutes on the heater side reducing the average oxide thickness by 1 μm to a total thickness of 1.98 μm on the bonding surface.

The heater side is also polished to ensure that the PECVD oxide layers on either side of the

processed wafer of a similar thickness. This provides a better balancing of the intrinsic stresses acting on either side resulting in a radius of curvature of $\geq$10 metres which is compatible with fusion bonding. Alternatively it was found that a peak to valley measurement across the wafer surface of $\leq$10 μm was also desirable for successful bonding.

4.5.3.2 Cleaning

The wafers must be thoroughly clean for fusion bonding to ensure that the surface is free of any contaminants, residue or particulates to reduce the risk of voids forming at the interface of the two wafers during bonding. This is achieved by dipping the wafers in a dilute (1:10) solution of TMAH for 5 minutes to remove any particulates from the polishing process by slightly under-etching the surrounding material. Next the wafers are rinsed in deionised water after removal from the solution. The bonding surface are then further cleaned in the SSEC wafer scrubber using jets of DI water and an ultrasonically agitated film of DI water and finally spun dry.

4.5.3.3 Bonding and annealing

Bonding the wafers together requires the cleaned surfaces to be activated using an oxygen plasma and placed in contact which each other (see Chapter 6 for more details). The bonding surfaces of the two wafers are manually aligned by the wafer flats and brought into contact and a point load is applied for 5 minutes to allow the bond to propagate to the edges.

Afterwards an infrared camera is used to inspect the quality of the bond especially to identify the presence of any voids or particulates. If the bond is found to be of sufficient quality it is placed in a furnace for 17 hours at 435$^{\circ}C$ to increase the strength of the bond. However, if voids or particulates are present the wafers are carefully separated and the polishing and cleaning are repeated until a good bond is achieved.

4.5.4 Channel

The selectivity of the standard SPR-350 photoresist to silicon when etched in the STS ICP etcher is 1:50 which means to etch through the silicon wafer to form the channel requires a resist thickness of 7 μm. The SPR 220-7 thick resist was is instead used as it has a selectivity of 1:84 to silicon.

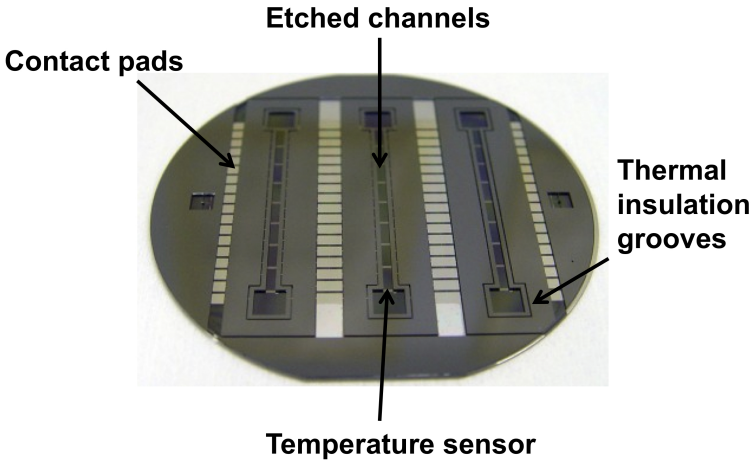


Figure 4.14: *Partially processed wafer showing etched channels with integrated temperature sensors*

The bonded wafer is coated with resist which is patterned using photolithography and the resist is developed exposing the channel. The exposed silicon is etched which creates the channel in the bonded wafer.

The process for coating the bare surface of the bonded wafer stack with SPR 220-7 differs from that of SPR 350 resist and is detailed in the runsheets in AppendixA in Table A.2. The final thickness was measured using the Nanospec after exposure and development and found to be 7.2 μm . A STS multiplex ICP deep etcher is used to etch through the exposed silicon areas on the top wafer. The standard etch recipe used for the earlier microchannel arrays described in Chapter 3 is again used and takes approximately 4 hours to etch through the top wafer.

After etching the resist is removed by ashing it for 30 minutes using an Electrotech barrel asher but occasionally not all the resist is removed. This may have been due to a reaction between the resist and the fluorine radicals hardening and chemically changing the outer layer of resist. If this is the case the residual resist can be removed by placing the bonded wafer into an ultrasonic bath of ACT CMI-S resist stripper. An example of the wafer at this stage of fabrication with etched channels is shown in Fig. 4.14.

It was important for the experimental results that the sidewalls have the same wetting characteristics as the channel floor which could be achieved by coating the sidewalls with a hydrophobic thin film of oxide. Ideally thermal oxidation would have been preferred for this as it would provide a more uniform film than PECVD. However, as the wafers were bonded and contained metals this was not possible. A 0.1 μm film of PECVD HFSIO is deposited to coat the sidewall,

floor and top of the channels.

4.5.5 Anodic bonding

A $500\mu m$ thick Pyrex 7440 wafer is drilled with 6 holes for fluid inlet and outlet ports for each channel. The glass wafer is cleaned as outlined in Chapter 3. After the Piranha etch the wafer is rinsed in DI water and dried using the Marangoni drier. The silicon wafer stack is carefully washed with DI water, then rinsed with IPA and Acetone and again washed again using DI water before being carefully dried using compressed air.

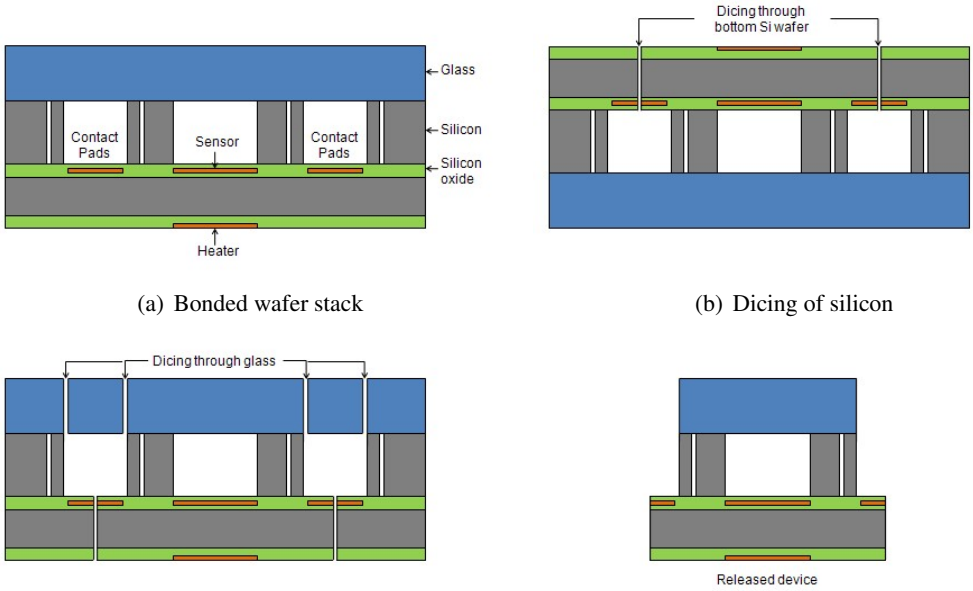
After both wafers are satisfactorily clean they are manually aligned to ensure optimal placement of the inlet and outlet holes over the reservoirs and anodically bonded together using an anodic bond recipe with parameters set to a maximum temperature of $400°C$, a peak voltage of 1000 V and a pressure of 800 mbar. The bonding voltage is removed when the current dropped below 5% of the initial current, which indicated that the bond had successfully propagated across the wafer surface.

4.5.6 Dicing

Wafer dicing these devices is a multi-stage process as the three channels need to be separated from one another by cutting through both the bottom silicon wafer and the top glass wafer and exposing the bond pads as shown in Fig. 4.15. To achieve this the wafer is first secured on adhesive tape during the silicon dicing and the wafer is then placed with the heater facing the saw. A diamond coated saw suitable for silicon dicing is used to cut down to a depth of a 380 μm from the heater side of the bottom wafer through to the top side of the same wafer. A 40 to 50 μm wide cut is made along the scribe lines shown in Fig. 4.15(b).

The wafer is then removed from the dicing saw and the adhesive tape is peeled off from the wafers. The wafer is remounted but this time the glass wafer faces the saw and the saw blade is changed to one more suitable for dicing glass. This saw results in thicker, rougher cuts of widths ranging from 120 to 200 μm depending on the speed at which the blade rotates.

The camera of the dicing saw is not focussed on the glass but on the silicon wafer underneath which is used to align the wafer to the saw and to determine where to dice the glass as shown in Fig. 4.15(c). After sawing the diced devices are rinsed and dried thoroughly with deionized



(a) Bonded wafer stack

(b) Dicing of silicon

(c) Dicing of glass

(d) Released device

Figure 4.15: *Dicing procedure*

water and compressed deionized air after being removed from the dicing saw to flush out any debris from the channels. The adhesive tape is then removed from the separated devices.

4.5.7 Oxide removal

Oxide is removed from the sensor pads and the heater using a Plasmatherm PK2440 RIE etcher. The process will also etch the glass cover-plate which is protected with SPR 220-7 resist applied with a fine paintbrush. The resist is then covered with Kapton tape to protect the glass around the holes and the exposed oxide underneath as well as acting as extra masking.

Once the metal pads are exposed the Kapton tape is removed and the resist stripped using ACT-CMIS resist stripper and the die rinsed with DI water and dried. The etch process is repeated on the heater side and an example of the finished microchannels are shown in Fig. 4.16.

4.6 Results

Once the fabrication process is completed the resistances of the sensors and heaters of each device are measured using a probe station. The average resistance of the tantalum sensors

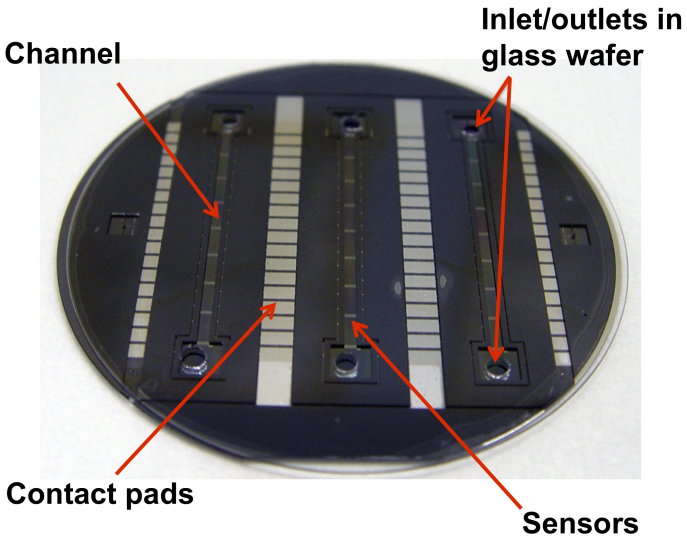


Figure 4.16: *Finished microchannels with integrated sensors*

is 2.37 $k\Omega$ and the aluminium heater resistance 7.6 Ω which met the required specifications. The tantalum sensors were unexpectedly found to have a negative thermal coefficient of resistance (TCR) [34]. As shown in Fig. 4.17 where the resistance drops by approximately 18.45Ω over $41°C$ giving a negative temperature sensitivity of $0.44\Omega°C^{-1}$ and the TCR was $-1.2 \times 10^{-4}\ °C^{-1}$.

A negative TCR is undesirable as the experimental rig developed at Brunel University required resistive temperature sensors with a positive TCR. It is speculated [158] [159] [160] that the negative TCR may be due to changes in the grain structure of the metal due to the number of high temperature steps during processing. Some of these steps such as the fusion bond annealing subject the sensors to high temperatures over a large period of time

4.6.1 Fabrication Issues

4.6.1.1 Adhesion

It was observed for some batches that, particularly on the bond pads that the aluminium peels off the underlying tantalum, an example of which is shown in Fig. **??**. The locations of the peeling aluminium varied between wafers of the same batch and the aluminium usually adhered to the tantalum where this problem was not observed. These reasons made the author suspect that this peeling is caused by residual resist from the lift-off process.

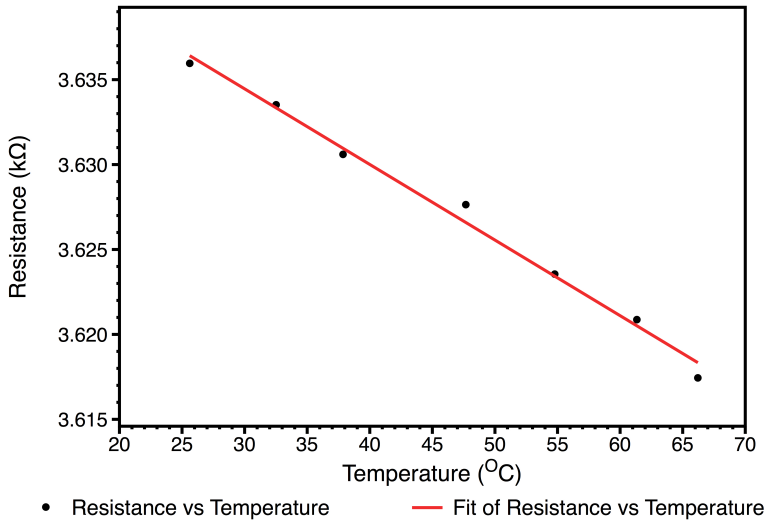


Figure 4.17: *Resistance as a function of temperature for tantalum sensor*

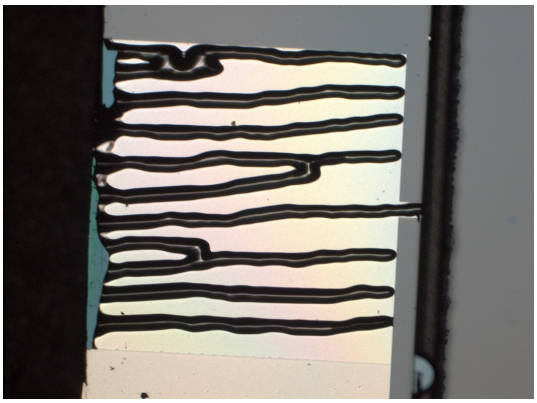


Figure 4.18: *Example of poor adhesion between tantalum and aluminium on sensor contact pad*

A more thorough and longer cleaning step after the lift-off resist has been developed and is used to reduce the risk of this occurring. Other adhesion problems were noticed when the wafers were exposed to mechanical stresses such as those present during CMP and dicing. These forces could cause the aluminium pads to be removed in their entirety.

4.6.1.2 Anodic Bond Strength

The initial result of anodic bonding between a 500 μm thick wafer of Pyrex 7740 and the fusion bonded wafer stack was not of good quality. For one batch the bonding resulted in a large void forming between the glass and silicon wafer stack in the centre which is shown in Fig. 4.19 and

running the wafers through the bonding process again did not seem to improve upon this.

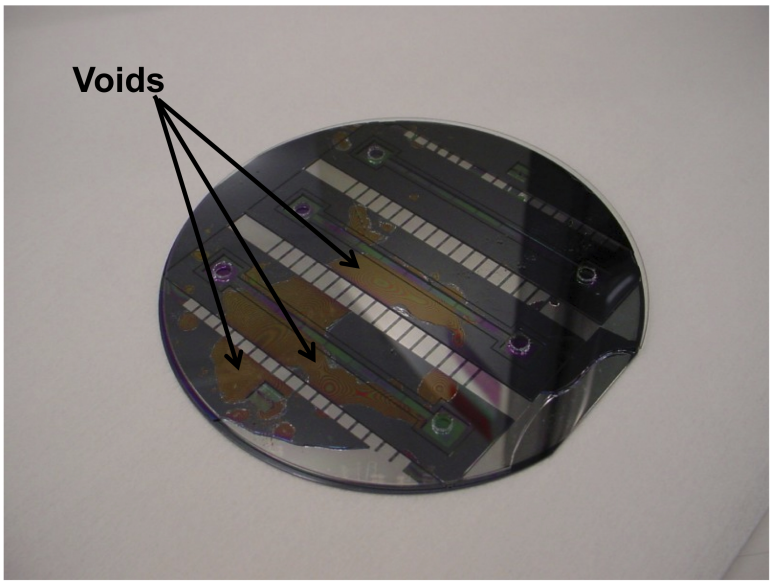


Figure 4.19: *Example of voids in anodic bond*

It was also found that even when the bond quality appeared to be good that the resulting bond strength was not sufficient for the pressure required by the experiments. Often the bond between the Pyrex and the microchannel device was observed to slowly delaminate from the edges of each die towards the centre after the wafer dicing step. This was most likely due to the multiple layers of PECVD oxide present throughout the wafer stack causing a drop in voltage across the bond interface leading to a lower bond strength and the presence of oxide at the bonding interface acting as an impediment to the bonding process. Further work was required to improve and optimise the anodic bonding process for such wafer stacks.

4.7 Conclusions

A design for a microchannel that meets the required specifications has been designed and fabricated taking into account the technology available. The process consists of multiple steps such as waferbonding, etching, metal deposition and photolithography and produced these channels for microscale boiling experiments. This fabrication process successfully demonstrates that creation of bulk micromachined channels with integrated sensors is possible and these devices have been used to characterise fluid flow for boiling studies.

Areas where the design and fabrication of these devices could be improved have been identified.

The most important issues needing to be addressed in the next iteration of the process include the choice of material used in fabricating the sensors, improving the adhesion of metals and the quality and strength of the anodic bond. The next chapter describes the solutions developed to address these and other issues.

Chapter 5
Silicon microchannels with integrated nickel sensors

5.1 Introduction

The previous chapter detailed the design and fabrication process of a microchannel with integrated sensors and heaters. Although these devices were successfully fabricated the tantalum sensors produced had a negative TCR that was not desirable due to the design of the experimental rig. Other areas where improvements to the process were desirable included increasing the anodic bond strength between glass and silicon wafers and improving the adhesion of the contact pads metallisation. Solutions to these issues were provided by the addition or alteration of steps in the fabrication process that are detailed in this chapter.

5.2 Fabrication

Most of the new process remains relatively unchanged from the one described in Chapter 4 and the cross section of the resulting device shown in Fig. 5.1 is similar to that of the original devices shown in Fig. 4.3. One of the more obvious changes is that the sensors are constructed from nickel and not tantalum.

5.2.1 Sensor Fabrication

5.2.1.1 Introduction

The temperature sensors of the previous devices were fabricated from tantalum that was chosen as it had a TCR and resistivity close to that of platinum. Platinum would have been the first choice for the sensor material as it is considered the standard material for use in resistive thermometry but was not chosen for reasons of cost and availability. After the devices were fabricated it was found that the tantalum sensors had a negative TCR.

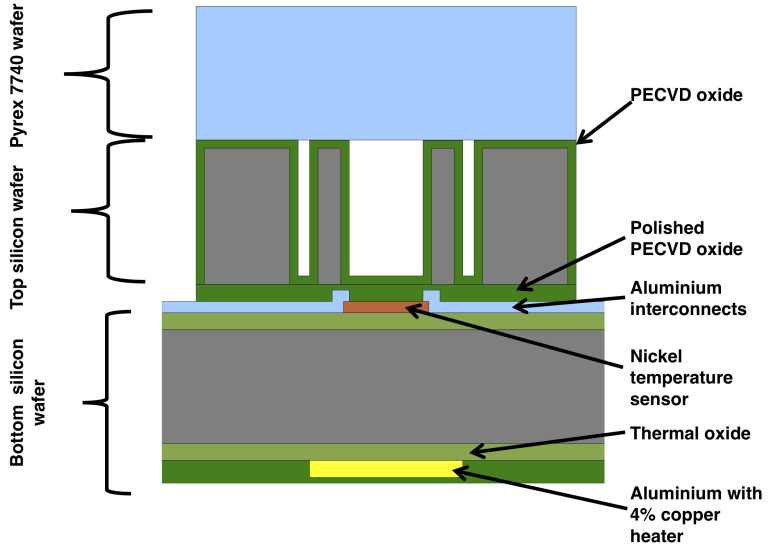


Figure 5.1: *Layers of microchannel with integrated nickel sensors*

A suitable alternative was required and from Table 4.1 it can be calculated that nickel had a resistivity of 6.84 $\mu\Omega cm^{-1}$, which is less than that of platinum (10.6 $\mu\Omega cm^{-1}$). However, the TCR of nickel (6900 $^oC^{-1}$) was higher than that of platinum (3927 $^oC^{-1}$) and this is desirable for good sensor sensitivity and accuracy as described in the previous chapter.

5.2.1.2 Fabrication

The nickel sensors were fabricated using the lift-off process described in Chapter 4 for the tantalum sensors with the deposition of a 250 Å seed layer of titanium onto the silicon dioxide using the Balzers followed by 0.6 to 0.8 μm of nickel without breaking the vacuum.

The average sheet resistance of the nickel film with the titanium adhesion layer was 0.46 $\Omega/\square$, which compares with 1.41 to 1.88 $\Omega/\square$ for a tantalum film. To meet the required specifications for sensor resistance the film thickness of the sensors was reduced from 0.87 to 0.26 μm. The sheet resistance of the 0.26 μm film of titanium and nickel was measured to be 1.544 $\Omega/\square$ resulting in an average room temperature sensor resistance of 615 Ω. The relationship between the resistance of a sensor for a current of 1 mA as a function of temperature is shown in Fig.5.2 and from this it can be calculated that the sensor has a positive TCR and the sensitivity is 0.27 $\Omega^O C^{-1}$.

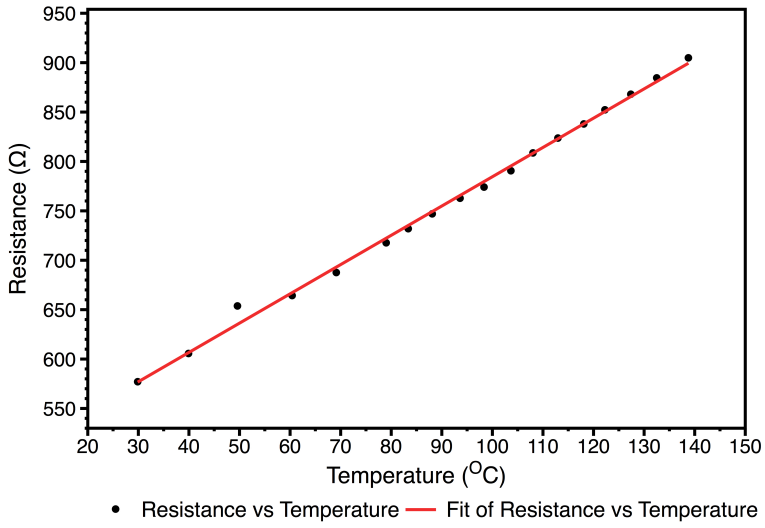


Figure 5.2: *Resistance of a sensor as a function of temperature for a current of 1 mA*

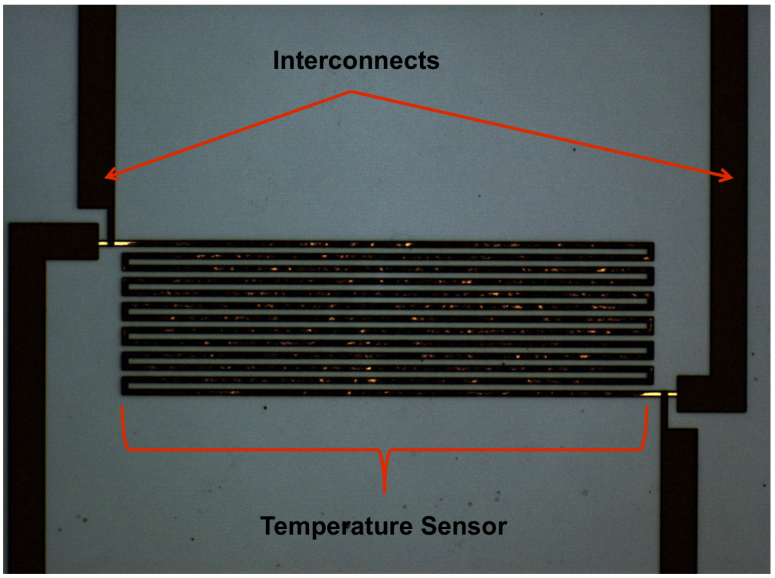
5.2.2 Interconnects

5.2.2.1 Introduction

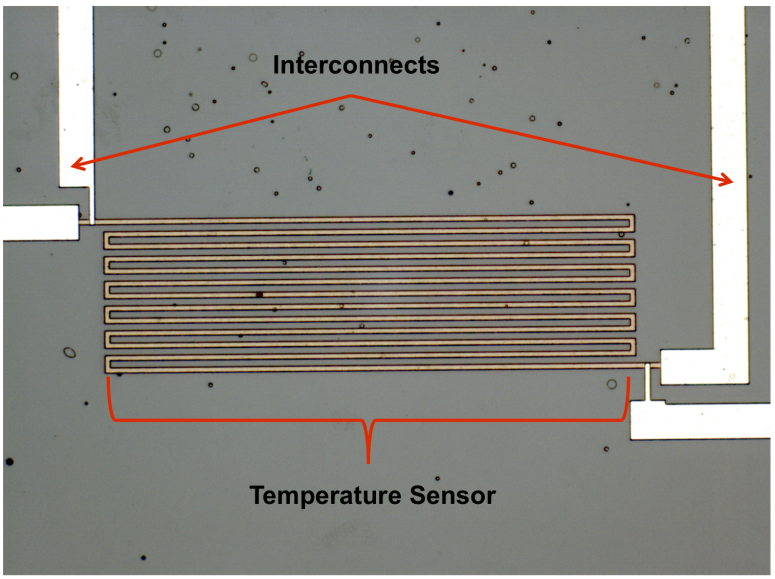
Unfortunately the interconnects and sensors became mottled brown in colour after annealing as shown in Fig. 5.3(a). This was caused by the aluminium layer unexpectedly alloying with the underlying nickel in the furnace. A poor electrical connection when probing was observed in addition to this colour change. The quality of the electrical contact could be enhanced by either gently scratching the surface of the pads when probe measurements were being taken or by passing 0.1 mA through the sensors at a compliance of 40 V causing this surface barrier to electrically break down but neither of these methods were desirable long-term solutions for the poor electrical contact.

5.2.2.2 Barrier layer

The alloying can be inhibited through the use of an intermediate diffusion barrier layer. Titanium nitride is widely used as a barrier layer material within the microfabrication industry as the small grained structure of titanium nitride makes it harder for diffusion to occur from one side of the barrier to the other [161]. Both discolouration of the interconnects and reduction in the quality of electrical contact at the sensor pad were no longer observed when titanium nitride was used as a barrier layer as seen from the interconnects in Fig 5.3(b).



(a) Interconnect with no titanium nitride and sensor



(b) Interconnect with titanium nitride and sensor

Figure 5.3: *Appearance of interconnects after annealing*

5.2.2.3 Fabrication

The titanium nitride barrier layer was deposited with the OPT Plasmalab 400 by sputtering in a nitrogen atmosphere. A sheet of this film was sputtered on an oxidised wafer for the same deposition time as used in the process. The sheet resistance of this film was 2.30 $10^3\Omega/\Box$ and the thickness was 0.25 μm.

Finally a 0.5 μm thick aluminium layer for the interconnect was deposited onto the titanium nitride in the OPT without breaking the vacuum to form the interconnect and contact pads. The aluminium sheet resistance was 0.015 $\Omega/\Box$.

5.2.3 PECVD oxide

5.2.3.1 Introduction

The next stage of the process is to coat the sensors and interconnects with high frequency PECVD silicon dioxide (HFSIO) using the STS PECVD tool. This protects the sensors and interconnects (from here on referred to as the top side) during the remaining fabrication steps such as the sputtering of the bottom side with 0.9 μm of Al 4 $\%$ Si to fabricate the heater as well as acting as an electrically insulating layer. This PECVD oxide is later planarised for fusion bonding to ensure an average surface roughness of $\leq$ 0.5nm.

5.2.3.2 Fabrication

During the fabrication of previous devices some of the contact pads on some wafers were damaged during CMP which is not desirable. This was prevented from occurring by increasing the PECVD oxide thickness from 2.5 μm to $4\mu m$. This is sufficient to planarise the silicon dioxide covering the 1.1 μm thick interconnect and sensor layers.

After annealing the PECVD oxide for 17 hours at 435 °C an Al 4 $\%$ Si film is deposited and patterned on the backside of the wafer. The average resistance of a heater was 7 Ω and the heater was then coated with a 4 μm film of PECVD oxide and annealed a second time to reduce stress within the film.

Only when the necessary cleaning and surface activation steps had been carried out and the wafer flatness and bow values requirements for a good fusion bond were met was the processed

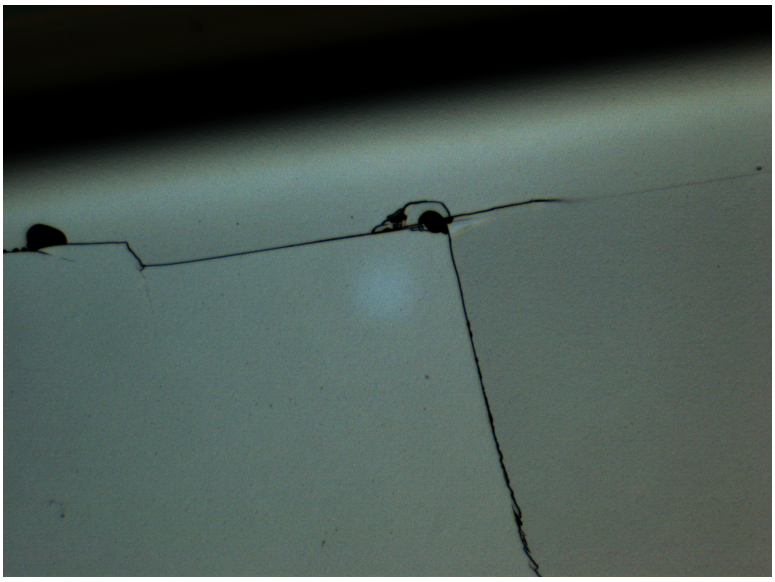


Figure 5.4: *Example of hairline crack formation*

wafer placed in contact with a virgin, double sided polished wafer. SPR 220-7 thick resist was spun and patterned on the unprocessed top surface of the wafer stack after it had been further annealed to strengthen the fusion bond. The exposed silicon was etched in the STS ICP etcher for 3-4 hours to form the channel.

5.2.3.3 Thin film stress issues

Stress is an important issue in microfabrication that must not exceed the elasticity of the constituent layers if cracks or buckling are to be avoided. The stress was calculated throughout the fabrication process using the Stoney equation and the wafer radius of curvature (flatness). Before and after both annealing steps the wafer flatness was measured with the Dektak surface profilometer to be 92.1 and 56.0 metres respectively giving a stress of 0.115 MPa at deposition and 57.9 kPA after annealing. The oxide layer was then polished on both sides to an average thickness of 3.35 μm. This resulted in a convex radius of curvature of 49.6 m and a net compressive stress of 0.112 MPa.

Hairline cracks such as those shown in Fig. 5.4 began to appear on the top wafer midway through etching and rapidly propagated across the wafer surface as the etching continued. Only the top wafer was affected by these cracks as the bottom wafer appeared to be unaffected after visual inspection with a microscope using both a visible and infrared light.

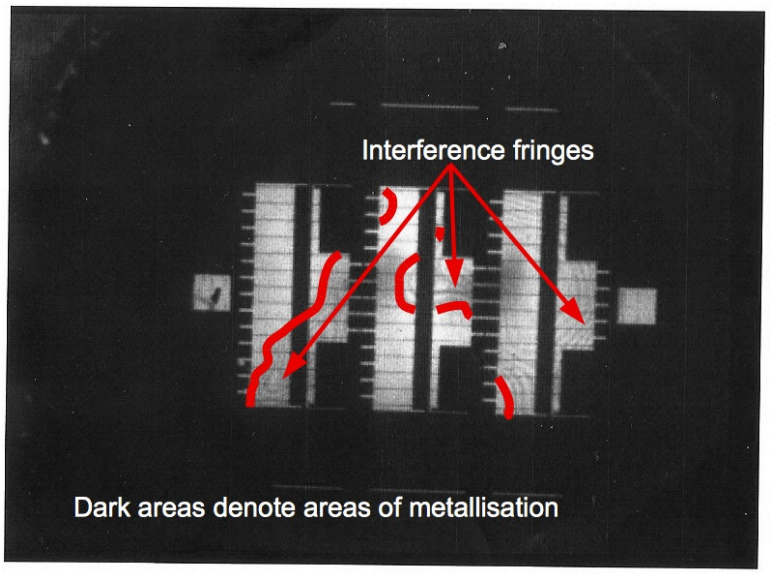


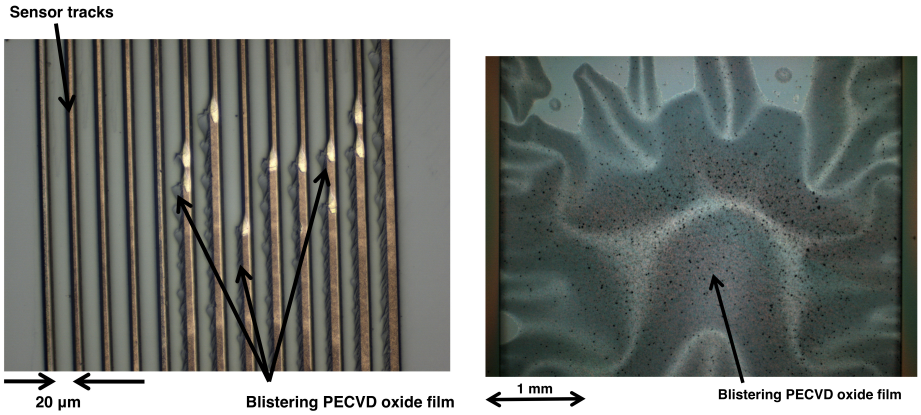
Figure 5.5: *Image taken with infrared source of wafer stack showing interference fringes at wafer interface due to crack*

The infrared light source allowed imaging of the bond interface between the silicon wafers that showed interference fringes as seen in Fig 5.5. The presence of these fringes suggested a void had formed at the bond interface. No sign of the crack propagating to the bottom wafer could be seen with this method. However, this was not conclusive as the metal within the wafer stack acts as a barrier to the transmission of infrared light shown by the dark areas in Fig.5.5.

The stress at which the cracks appear is unknown due to the removal of the silicon but as the Young's modulus of a (100) silicon wafer is given as 129.5 GPa and the shear modulus as 70 GPa [162] [122] any fracturing of the wafer would be a result of the stress acting on the wafer exceeding this value.

To reduce these excessive stresses the thickness of the PECVD oxide films on both sides of the wafer was reduced. The average thickness of the PECVD oxide deposited onto the next batch was 3.6 μm on the sensor and the heater side. The wafer curvature measured for this wafer after deposition of PECVD on both sides was 10.8 m corresponding to a stress of 42.4 kPa before the second annealing.

The processed wafer was successfully fusion bonded to a bare (100) Si double sided polished wafer and annealed again to increase the bond strength. This wafer was successfully etched down to the PECVD oxide film protecting the sensors. However it was observed that this oxide film blistered at certain points along the channel and examples of this blistering are shown in



(a) Effect of stress on thin film near sensor (b) Effect of stress on thin film in reservoir

Figure 5.6: *Delamination of PECVD oxide layer due to stress*

Fig. 5.6. This blistering effect is a sign that excessive compressive stresses exist within the oxide causing the film to peel away.

The oxide thickness at the blistering was measured using the Nanospec and compared with that of the average oxide thickness taken before fusion bonding. This showed that although some oxide remained, the average thickness of the remaining adhered oxide film was reduced to 1.75 μm from a thickness before fusion bonding of 3 μm. This indicates that the stress occurred within the PECVD oxide film and was excessive enough to cause blistering to occur.

5.2.3.4 Stress Reduction

By balancing the stresses acting on opposite sides of the wafer it was possible to reduce the net stress and the wafer bow. This was accomplished by keeping the PECVD oxide film thickness as equal as possible on both sides throughout the process and annealing these films simultaneously instead of sequentially. This ensures that one side of the wafer was not annealed twice which would have resulted in this side having a lower stress than the other.

A 0.1 μm film of oxide was deposited onto the sensors to act as a thin protective layer while the wafer is handled and processed while fabricating the heaters on the other side. After the heaters are formed the wafer is placed back into the STS PECVD chamber and coated so that a 3.1 μm layer of PECVD exists on both sides. A typical radius of curvature of the wafer after these steps was 9.23 m giving a net stress of 25 kPa.

The wafer was loaded into the annealing furnace to reduce the stress of the oxide films. The

wafers were kept in the furnace for 24 hours further reducing the average stress to 10.2 kPA. The PECVD oxide thin film was then polished down to an average thickness of 1.5 μm before fusion bonding. These changes to the order of the PECVD oxide deposition and annealing steps resulted in the intrinsic thin film stresses acting on the wafer being more balanced and results in a lower net stress than achieved with the process described in Chapter 4.

5.2.4 Anodic Bonding

5.2.4.1 Introduction

Anodic bonding is used to cap the microchannels and contain the working fluid. It is important that this bond remains intact but it was observed that the glass often delaminated from the silicon when the devices described in Chapter 4 were diced. This delamination started at the edges and crept towards the centre over time and if the device was used in tests this failure mechanism accelerated. Improving the anodic bond strength to ensure this does not happen was a priority for this modified process.

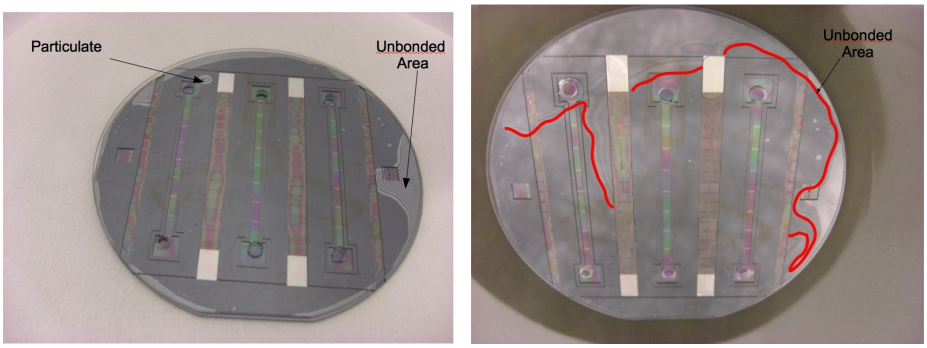
5.2.4.2 Recipe characterisation

Results published by Go [163] and Plaza [164] indicated that the anodic bond strength is most sensitive to changes in the recipe temperature and applied voltage. Increased temperature leads to increased breakdown of the sodium oxide within the glass into constituent ions as well as increasing the mobility of these ions. The voltage leads to increased electric field strength that drives the mobile ions towards the bonding interface.

	Recipe Parameters				*Interfacial Surface Energy (Jm^{-2})*	
Recipe	Temperature $^{\circ}C$	Voltage (V)	Tool Pressure (mbar)	% of Max. Current	Average	Standard Dev.
1	400	400	400	5	6.34E+03	2.88E+03
2	425	1000	800	5	5.95E+03	3.84E+03
3	450	1250	800	2	5.44E+03	4.02E+03

Table 5.1: *Anodic bonding recipe parameters and resulting surface energy*

This information was used to improve the strength and reliability of the anodic bond. The changes to the initial recipe are summarised in Table 5.1 and included increasing the temperature from 425 to 450$^{\circ}C$ and voltage from 1000 to 1250 V as well as decreasing the percentage of maximum current at which the recipe terminates from 5% to 2%.



(a) Before dicing through silicon wafer (b) After dicing through silicon wafer

Figure 5.7: *Spread of bond delamination due to dicing*

Measurements of the average surface energy produced by recipe 2 between a single, bare silicon and glass wafers were performed using the mesa test structures described in Chapters 4 and found to be 5950 Jm^{-2} but this dropped to 5440 Jm^{-2} for recipe 3. Additionally the standard deviation of bond energy across the wafer surface increased from 3840 to 4020 Jm^{-2}. This was unexpected as the increase in temperature and voltage was expected to result in an increased bond energy while the increased bond duration caused by dropping the percentage of maximum current was thought to result in a more spatially uniform bond.

5.2.4.3 Bond delamination

The new bonding recipe did not prevent the wafer dicing forces from initiating delamination at the edges of the die and spreading inwards as shown in Fig. 5.7. It was expected that the presence of multiple dielectric layers would result in a reduction in bond strength compared to bonding glass to silicon but how much they would affect bonding was unknown. The drop in bond strength due to dielectric layers is caused by a reduction in bonding voltage across the wafer stack that leads to a reduction in the electric field across the silicon-glass interface that attracts the ions required to form a bond.

These dielectric layers exist at three locations in the wafer stack as shown in Fig. 5.1. The bottom and middle dielectric layers which cover the heater and sensors respectively provides mechanical protection during fabrication, electrical insulation between fluid and the sensors during operation and aid in the planarisation of the wafer surface for fusion bonding as well as the reduction of the intrinsic stress. The top layer of dielectric at the silicon-glass interface was deposited primarily to provide the same thermal and wetting properties on the channel wall as

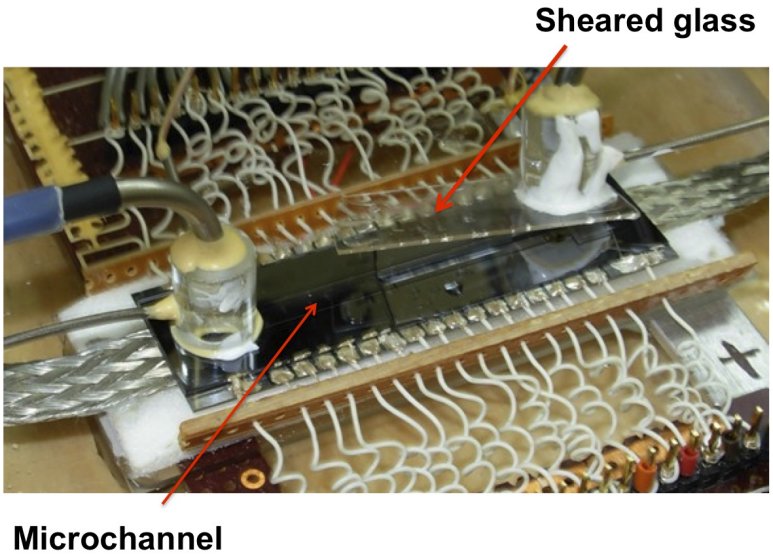


Figure 5.8: *Shearing of glass from silicon*

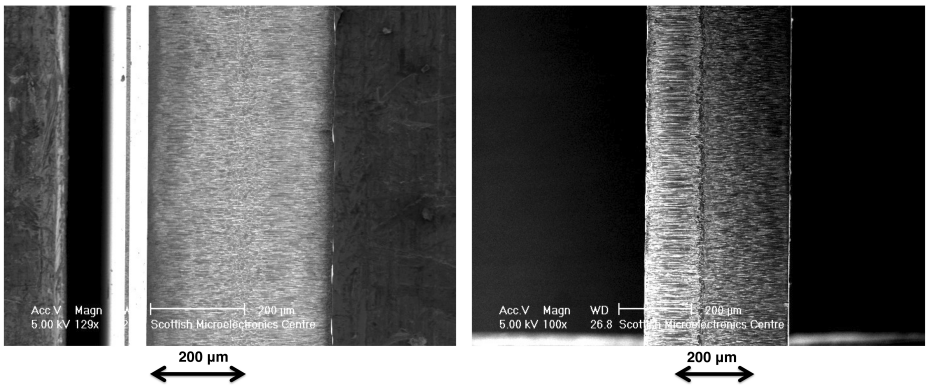
exist on the channel floor.

5.2.4.4 Removal of PECVD oxide film at anodic bonding interface

The device was tested to confirm whether the anodic bond could endure the experimental conditions by applying pressure to the channels with nitrogen gas up to 3 bars for one day at room temperature. No drop in pressure was detected under these conditions. The channel was also evacuated down to -1 bar and again no leak was detected. Next the working fluid flowing into the channel was heated from 45 to 70 $^{\circ}C$ using a preheater and pressurised to 1.37 bar using nitrogen gas. The flow-rate was increased from 30 to 90 ml/min when a leak developed at the inlet before the glass sheared off as shown in Fig. 5.8.

Some oxide remained on the top of the channel after the glass sheared off. The top of the channel was placed under the Nanospec and the average thickness of the remaining oxide was measured to be 538 Å . This demonstrated that the bond started to weaken and separate within the thin oxide layer that coated the channel.

It was thought that this oxide layer, as well as causing a lower electric field across the bond interface, also impeded the process by which the bond between the silicon and glass is formed leading to an even weaker bond. This could explain why nearly half of the 0.1 μm of oxide was sheared from the silicon as the oxygen ions would have had to diffuse through the oxide



(a) PECVD coated sidewall - no etching (b) PECVD coated sidewall - top layer etched

Figure 5.9: *Effect of etching of top PECVD on sidewall homogeneity*

layer to reach the silicon underneath to form the bond. The presence of this oxide meant that the timescales of the bonding process would need to be longer.

To address this the next batch of devices had the PECVD oxide at the anodic bonding interface removed using the Plasmatherm PK2440 RIE etcher. Collaborators at Brunel University tested the bond of one of these modified devices using the same experimental conditions as before and no leaks were detected within the device.

5.2.5 Effect of etching on sidewall coating

5.2.5.1 Introduction

Removing the PECVD oxide from the top silicon wafer using dry etching demonstrated to improved quality of the anodic bond. However it affected the PECVD deposited on the sidewalls of the channel as shown in Fig. 5.9 resulting in a channel with less uniform wetting and thermal insulating properties on the sidewalls. The extent of how much the PECVD oxide coating on the channel sidewalls was affected was unknown. To determine this test channels were fabricated on two silicon wafers using the same mask as the device channels.

5.2.5.2 Fabrication of test channels

These test channels were formed using the same steps used for the process wafers but with additional SPR 220-7 carefully and manually applied to the exposed photoresist in order to create bridges across the thermal isolation features. This is necessary to prevent the channels

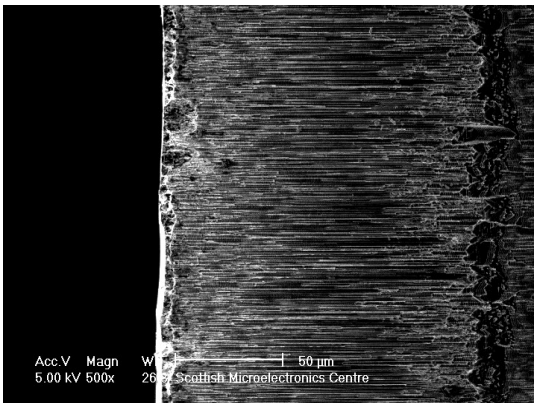


Figure 5.10: *SEM image of a PECVD oxide coated channel after etching of surface PECVD oxide*

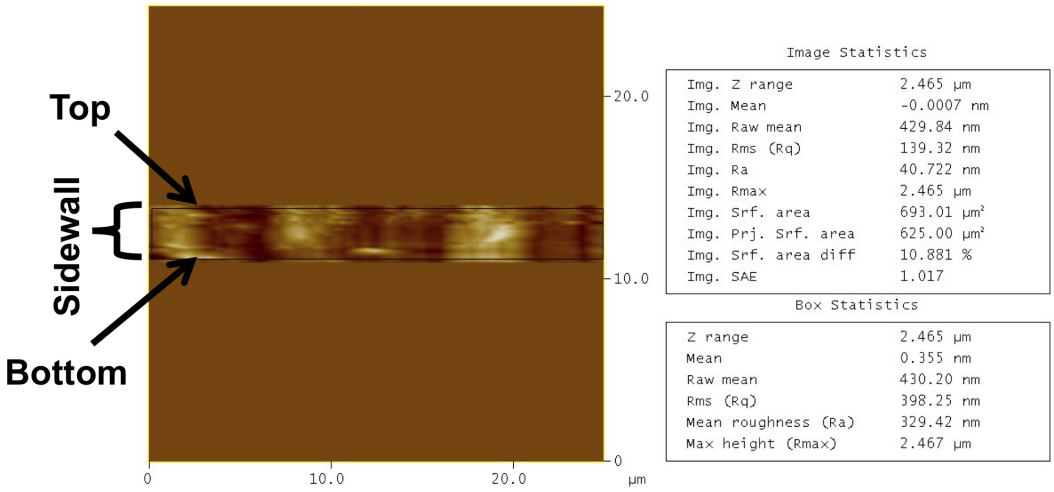
from sliding out from the bulk upon removal from the handle wafer after the through wafer etch. A handle wafer was used to protect the chuck of the tool and support the channel which was held in place using cool grease. This provided adequate thermal conductivity between the two wafers to prevent hot spots forming during etching that could lead to large local variations of the etch rate and selectivity.

The exposed silicon was etched all the way through with the same recipe as before on the STS ICP etcher. After etching the resist was removed by placing the wafer in an ultrasonically agitated bath of ACT CMIS resist stripper. Subsequently the cool grease was removed by soaking the wafer in acetone upon the wafers separated and the wafer was washed with DI water and dried with CDA.

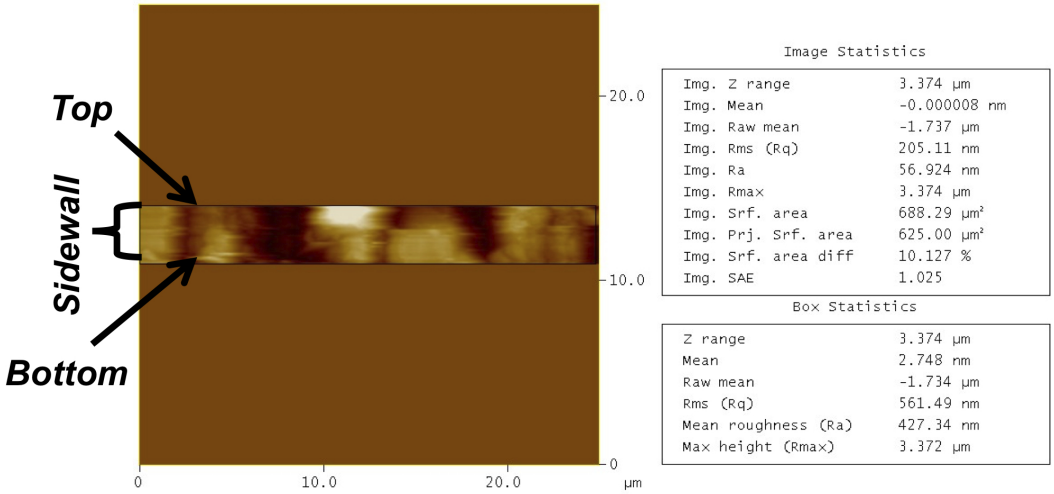
These two patterned wafers were coated with a 0.1 μm layer of PECVD oxide and one had the oxide etched off the top surface. The wafers were then cleaved for measurement and imaging.

5.2.5.3 Surface roughness measurement

The two samples sidewalls were imaged using a Philips Scanning Electron Microscope (SEM). The sample where the 0.1 μm thick film of PECVD oxide was etched off showed a distinct change in the appearance of the sidewalls as shown in Fig. 5.10. The image appears to show the removal of material from the sidewalls down to a depth of approximately 145 μm from the top of the channel. This was not present with the unetched sample and is attributed to the effect of the reactive ion etching of the top PECVD layer.



(a) AFM scan of unetched channel sidewall



(b) AFM scan of etched channel sidewall

Figure 5.11: *AFM scan of channel sidewalls*

The surface roughness of each channel sidewall was measured with an atomic force microscope (AFM). Due to difficulties in ensuring that the stylus was placed at the same point on the sidewalls, these measurements are best used as a guide because the step coverage for PECVD oxide does not result in a uniformly thick film on the sidewalls. The deposition rate of the PECVD oxide is proportional to the arrival angle of the reactants. A 380 μm deep and 1.5 mm wide channel would result in an arrival angle of 76 degrees assuming the reactants do not migrate [161]. This would mean that the film thickness does gradually decrease with distance down the sidewall and may result in an opening at the bottom of the sidewall.

The channels were formed using the Bosch process that also acts as a contributing factor to the

variation of sidewall surface roughness with depth. As seen from Fig. 5.11(a) the average surface roughness of the unetched PECVD coated channel was 329 nm, and from Fig. 5.11(b) the PECVD coated channel which removed the HFSIO coating from the top had a surface roughness of 427 nm. The effect of the etching of the HFSIO coating may explain the 100 nm between roughness measurement on the sidewall.

5.2.5.4 Conclusion

Microboiling experiments require that the entire channel is coated in the same material to facilitate the extraction of heat transfer parameters. However, the current process cannot guarantee a uniform coating along the sidewalls due to the use of PECVD and the etching away of the top film of PECVD oxide to improve the anodic bonding. However, improving the anodic bond reliability was considered of greater importance. The use of local oxidation of silicon offers a possible solution to achieve a more uniform film thickness down the channel sidewalls but this is not possible as the temperatures involved are not suitable for use with metal layers. A further iteration of the design of the fabrication process would be required to use this and such a process is proposed in Chapter 7.

5.2.6 Sensor and heater redesign

5.2.6.1 Introduction

When connecting the device into the test rig it was observed that the sensor performance was compromised by a current flow between the sensor and heater. It was suspected that this current flow was due to a parasitic conductive path due to metal smearing between the sensor and heater due to wafer dicing cut resulting in a noticeable reduction in the isolation resistance between them as the voltage is increased. The next generation of devices required changes to the design of the device to ensure that this leakage path is removed.

5.2.6.2 Measurement

A constant current of 1 mA was forced through the sensors and the resistance measured. However, the sensor resistance began to change when the heater was activated. Fig. 5.12 shows the increase in sensor resistance as the heater voltage is ramped up to 20 V. This effect was

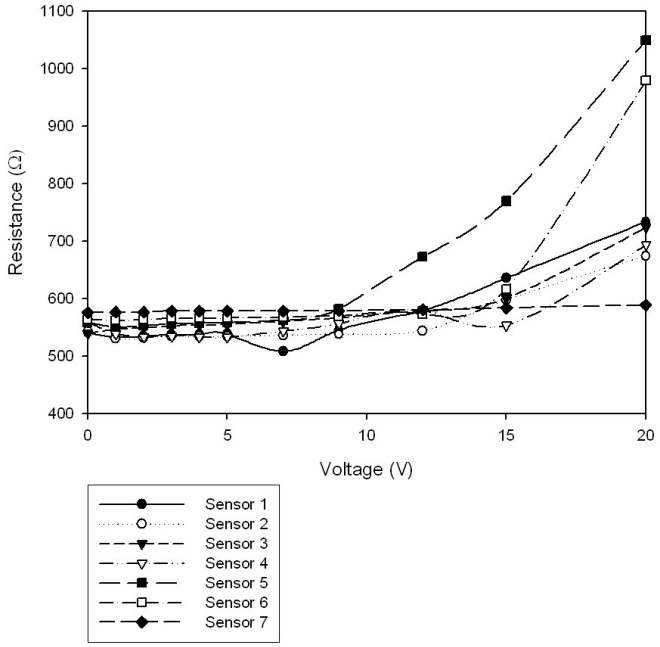


Figure 5.12: *Effect of heater voltage sweep on the sensor resistance*

unexpected and was not attributable to the increased temperature caused by the heater as not all sensors on the device tested showed an increase in resistance with heater voltage and those that did increased by different rates.

5.2.6.3 Results of experiments to determine the cause of the parasitic leakage path

Experiments were carried out where the resistance between the sensor contact pads and the heater was measured as the voltage between them was ramped from 0 to 40 V. The resistance across the device edge decreased from approximately 1.1 MΩ to 10 kΩ as the voltage was increased as shown in Fig. 5.13.

Next the edges of the device were dipped in fuming nitric to remove any possible organic contaminants across the diced sides. No significant changes in isolation resistance were observed. Then the device was dipped into aluminium etchant to remove any aluminium from the diced sides while keeping the titanium, nickel and titanium nitride in place. An increase in resistance was observed when the resistance was measured again.

Finally the device was dipped into a dilute solution of piranha etch to remove all metal from the edge and the measurement repeated. Fig. 5.13 shows that the isolation resistance of the etched

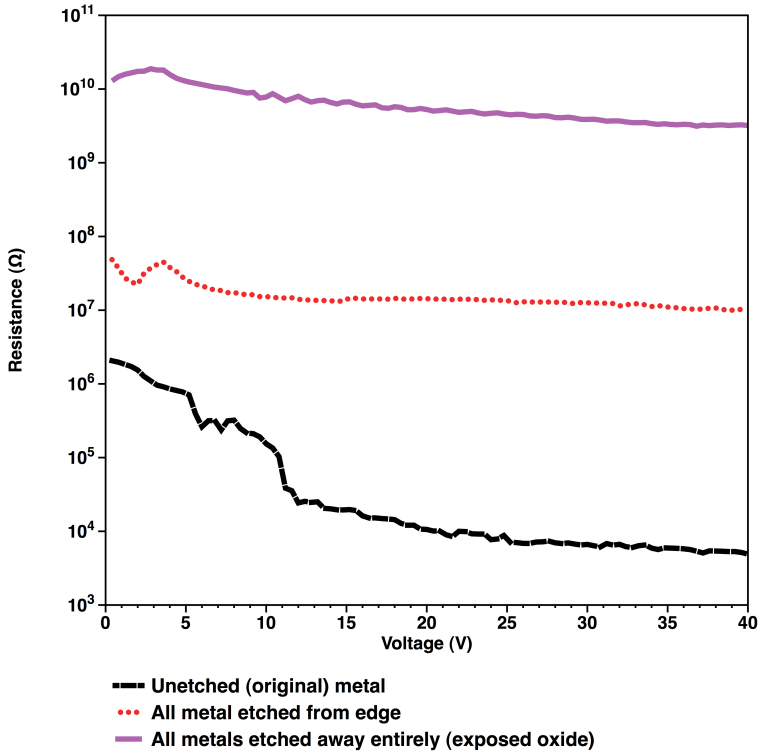


Figure 5.13: *Isolation resistance measured across sensor and heater as a function of voltage after metal etchings*

device increased to $\geq$ 10 MΩ as well as the resistance being more independent of the applied voltage. Finally all the metal contact pads were removed and the measurements taken. A probe was applied to the exposed oxide where the contact pad once was and although there was still a leakage current the measured isolation resistance at 40 V had increased to approximately 10 GΩ. Point measurements of the exposed oxide still show the existence of a leakage resistance through the oxide although this is now less dependent on the heater voltage.

As a significant change in resistance was only observed when the edges were dipped in Piranha etch and not when dipped fuming nitric suggests that the parasitic conductive path was most likely due to some form of metallic contamination formed along the edge of the wafer when being diced.

5.2.6.4 Solution

To prevent the formation of these conductive paths the layout of the sensors, heaters and interconnects were altered to remove any metal in a 120 μm strip about the dicing lines.

The process used involved SPR-350 being spin-coated onto the heater side and patterned with the exposed strip of metal etched using the standard aluminium etching recipe in the STS metal etcher. Etching the sensor pads is more complex as they consist of a sandwich of titanium, nickel, titanium nitride and aluminium layers. The aluminium and titanium nitride were etched with the same recipe as the heater in STS metal etcher for 30 minutes, but the nickel could not be successfully etched in the STS-etcher as the etch chemistry is not compatible. This layer was instead removed by wet etching with nickel etchant for 10 minutes and rinsing and drying with DI water and CDA. The STS etcher was then used for a further 10 minutes to remove the titanium adhesion layer and the wafer is then visually inspected under a microscope to check all the exposed metal has been removed.

5.2.6.5 Results

The use of this additional mask to remove the metal from the dicing line resulted in good isolation between the heater and the sensors. Measurements of devices created using this mask consistently had high leakage resistances similar to Fig.5.13.

5.3 Conclusions

This modified fabrication process has successfully produced devices with nickel temperature sensors with a positive TCR. The stress within the silicon wafer stack due to PECVD oxide was successfully lowered by adjusting the deposition sequence to ensure thin film compressive and tensile stresses did not damage the device.

Additionally the removal of the oxide from the top of the microchannels was shown to result in an improved anodic bond. Further improvements to the bonding recipe were inhibited by the limited information available on how the various recipe parameters and the presence of dielectric films affect the bond strength. The next chapter addresses this issue that in turn enables this aspect of the recipe to be optimised.

Due to time constraints these devices were not able to be used for two phase flow boiling experiments. However, the technology to create these devices has been successfully developed and is available for future studies.

Chapter 6
Wafer bonding

6.1 Introduction

Wafer bonding is of central importance to the fabrication of these microchannel devices. Fusion bonding makes possible the integration of the temperature sensors with the bulk micromachined channels while anodic bonding enables a protective glass cover to be attached to the silicon microchannels permitting optical inspection of fluid flow in the channel. Therefore it is important that these processes are well characterised to ensure a good bond can be consistently attained. Fusion bonding of the two silicon wafers was consistently successful when the relevant criteria of surface roughness and wafer bow are met but the reliability, quality and strength of the anodic bonding process was affected by the presence of the dielectric films throughout the wafer stack.

This chapter describes the steps taken to improve reliability, quality and strength of the anodic bonding process. First an overview of wafer bonding and its characterisation is detailed. Test structures which can be used to quantify the bond strength between silicon and Pyrex under various conditions are discussed. Using one of these test structures in conjunction with experimental design methods enabled the effect of the various recipe parameters and experimental conditions on the average bond strength to be analysed and the bond strength optimised.

6.2 Waferbonding

6.2.1 Overview

Methods of wafer bonding include anodic [3], eutectic [165], fusion [166] [167], adhesive [168] and thermocompressive [169] [170] [171] bonding. These methods are summarised in Table 6.1. Anodic bonding and eutectic have been widely adopted as bonding takes place at relatively low temperatures permitting the use of materials such as aluminium without damage. Similarly the development of several low temperature processes [172] [173] [174] [175] has been reported since the early 90's has increased the use of fusion bonding.

Method	Bonding conditions	Advantages	Disadvantages
Fusion bonding	High temperature schemes ($600 - 1200°C$) and low temperature schemes. Little or no pressure	High bond strength, hermetic sealing	Very clean and smooth surfaces needed, high temperatures not suitable for electronics
Anodic bonding	$150 - 450°C$ 200-1500 V Little or no pressure	High bond strength, hermetic sealing	High temperatures and voltages may damage electronics
Adhesive bonding	$20 - 400°C$, low to medium pressure	High bond strength, compatible with electronics wafers	Limited temperature stability with some adhesives, issues with hermeticity
Eutectic bonding	Low temperature ($200 - 400°C$), low to medium bond pressure	High bond strength, hermetic, compatible with electronic wafers	Native oxides inhibit bonding
Thermocompressive bonding	$350 - 600°C$, high bonding pressure	Hermetic sealing, compatible with electronic wafers	Smooth surfaces required, high pressures needed

Table 6.1: *Comparison of common wafer bonding methods*

6.3 Fusion bonding

6.3.1 Introduction

Fusion bonding is a three stage process, the first is the preparation of the bonding surfaces, the second is bringing the surfaces in contact and the final stage is the anneal step. It occurs when two clean, smooth, planar surfaces are brought into contact at room temperature. The two surfaces quickly adhere to one another through weak intermolecular forces such as hydrogen bonds or Van der Waals forces.

For fusion bonding the bonding surfaces must be carefully cleaned to ensure any particulates or contaminants are removed. Usually the cleaning stage also activates the surfaces for bonding. The two wafers are then brought into contact with each other at room temperature by applying a small pressure at the centre of the wafers to squeeze out the thin film of air between the wafers. Contact initiates the bonding wave which proceeds to propagates out towards the wafer edges. Within a few minutes a weak bond is developed between the two wafers. Typically the wafers are then annealed to strengthen the bond [167]. The following sections describe these steps in more detail.

6.3.1.1 Bonding material

The fusion bonding required for the devices in this thesis was exclusively between silicon and silicon dioxide. Although a wide variety of materials can be bonded, certain factors must be

taken into account when bonding two dissimilar materials to minimise any negative consequences. If the bonded substrates have dissimilar coefficients of thermal expansion then the annealing stage may result in the generation of thermal strain that if excessive may damage the wafers. Further strain between bonded wafers may be generated if wafers are misaligned relative to the crystal orientation of the other wafer.

6.3.1.2 Smoothness and Flatness

A fusion bond is formed due to the effect of room temperature, weak intermolecular forces between the wafers that act over a short distance and are inversely proportional to the cube of the distance (d_g) between the wafers.

$$F \propto \frac{1}{d_g^3} \tag{6.1}$$

This makes the use of flat and smooth wafer surfaces essential for a good bond. It was recommended that surface roughness (R_A) must be no greater than 1 to 0.5 nm on each surface to ensure that the force between wafers is sufficient to initiate bonding [176]. The wafer bow must also be low so they can deform elastically when placed in contact, with a radius of curvature of 10 metres having been found to be satisfactory [176].

The flatness of the surfaces can be defined using the total thickness variation (TTV) h and this must meet a critical value to provide the required amount of deformation. The TTV is affected by several parameters such as radius of curvature (R), wafer thickness (t), Young's modulus (E) and the surface energy (γ) of the bonded pair [166].

$$h < \frac{R^2}{\sqrt{1.2Et^3/\gamma}} \tag{6.2}$$

This relationship may be further simplified by using the approximation [166].

$$h < 2.6\sqrt{\frac{R\gamma}{E}} \tag{6.3}$$

6.3.2 Chemical mechanical polishing

6.3.2.1 Introduction

Chemical-Mechanical Polishing (CMP) was used to meet the smoothness requirement for wafer bonding. It has been widely used in the IC and MEMS industries [177] [178] [179] [180] as it allows the surfaces to be sufficiently planarised without causing any subsurface damage that can occur with polishing techniques based solely on mechanical principles.

During the CMP process the wafer to be polished is held in place using a vacuum while an external pressure (usually on the order of 0.1-1 bar) is applied to press the wafer against the polishing pad. The polishing pad and wafer holder are then rotated while a slurry of silica particles suspended in an alkaline aqueous solution is dripped onto the pad. CMP depends on both the chemical and mechanical agents associated with the slurry to polish the surfaces. The chemical etchants present in the slurry attack the native oxide present on the silicon while the abrasive particles aid in the removal of the weakened oxide.

6.3.2.2 Polishing mechanism

Various models of the reaction between the wafer, pad, and slurry have been proposed [181] [182]. The most widely accepted explanation as to how the slurry attacks the silicon dioxide is shown in Fig. 6.1 [183] [184]. The polishing slurry consists of silica particles suspended in an alkaline solution which flows over the wafer surface leading to the formation of hydroxyls with the silicon dioxide on the wafer surface (Fig. 6.1(a)). These hydroxyl bonds aid in the formation of hydrogen bonds between the suspended particles and wafer (Fig. 6.1(b)). The hydrogen bonds react with the silicon oxide producing water and a Si-O bond between the wafer and the particle (Fig. 6.1(c)). The particle moves away from the wafer and bringing some of the silicon dioxide with it (Fig. 6.1(d)).

6.3.3 Cleaning

6.3.3.1 Introduction

A good quality fusion bond requires a bonding surface to be free of any contaminants or particulates. Possible sources of contaminants include hydrocarbons from air or plastic wafer boxes and metallic ionic contamination from wafer tweezers. The presence of contaminants or partic-

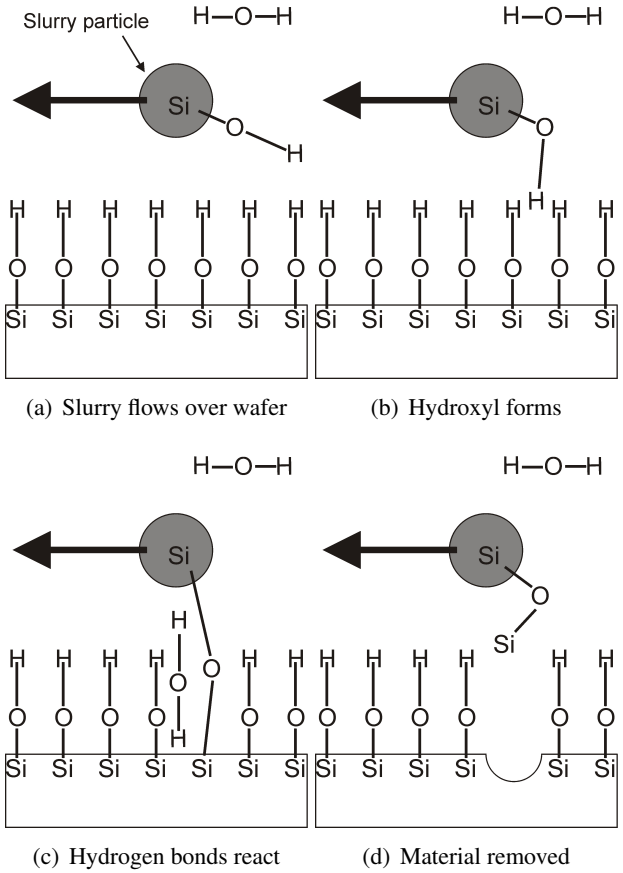


Figure 6.1: *Chemical-mechanical polishing mechanism*

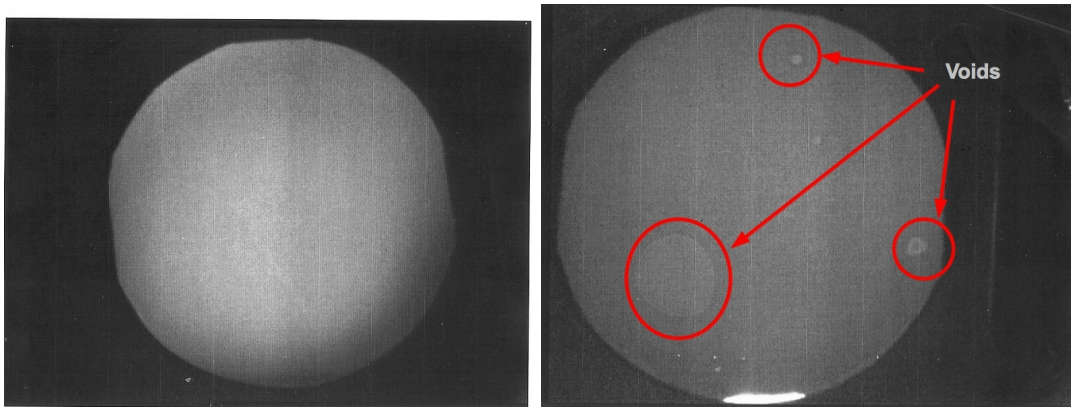
ulates will lead to voids forming at the bond interface or if of sufficient size or frequency may inhibit the formation of the bond.

6.3.3.2 Cleaning processes

Chemical cleaning processes commonly used in the microfabrication industry include RCA1 (40% NH_4OH:30%H_2O_2:H_2O = 1:1:5, 70-80^{O}C),RCA2 (37% NH_4OH:30%H_2O_2:H_2O = 1:1:6, 70-80^{O}C) [185] [186] [187] [188] [189] or plasma treatments such as 0_2 and NH_3 [176] [167] [190]. These cleaning methods result in the wafer surface becoming hydrophobic through the formation of a thin silicon oxide layer.

Hydrophobic bonding which will be discussed later requires a different cleaning method to prevent a hydrophilic surface forming. The preferred cleaning method for wafers undergoing this bonding procedure is to dip them in concentrated HF.

6.3.4 Wafer contact



(a) Fusion bond (b) Fusion bond with void

Figure 6.2: *Images of bond interface taken with IR detector/source setup*

The contact step involved the wafers being aligned after cleaning and brought into contact. At contact a point load is usually applied at the centre of the wafer to push them together such that the distance between them becomes sufficiently small so that the attractive weak intramolecular forces becomes dominant and acts on the wafers. At this point any air between the wafers is pushed out from between them as the localised pre-bond propagates out to the edge of the wafers. Representative images of a good fusion bond after contact and one of a bond with a void are shown in Fig. 6.2(a) and 6.2(b) respectively.

6.3.4.1 Annealing

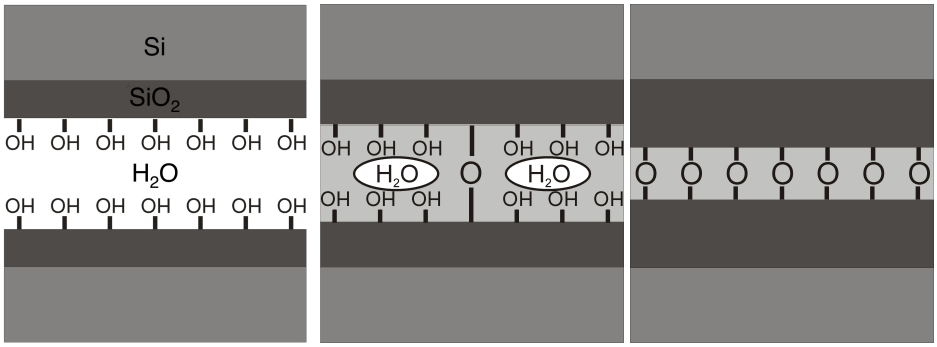
The last step is the annealing of the bonded pair at temperatures up to $1200°C$ to increase the bond strength. The temperature used affects the bond strength with three distinct temperature ranges being identified which each effect it differently [191]. The mechanisms of these areas depend on whether the bond is a hydrophobic or hydrophilic bond.

Annealing may generate interfacial intrinsic voids which start appearing when the annealing temperature rises above $400°C$ and begin to disappear above $900°C$. These voids are commonly found when the wafers being bonded do not have an intermediate oxide layer and although they are often attributed to gassing from hydrocarbon contamination. However, there is not universal agreement with this theory [103] [192]. Etching cavities into one of the wafer surfaces has been shown to reduce the risk of intrinsic voids due to annealing [103] and high temp $>800°C$ can reduce voids by reflowing the interfacial oxide [193].

6.3.5 Mechanism of fusion bonding

Fusion bonding can be divided into a number of subcategories depending on the presence of oxide on the bonding surface and the annealing temperature. The two main forms of this bonding are hydrophobic and hydrophilic bonding.

6.3.6 Hydrophilic bonding



(a) Room temperature bonding - hydoxyls formation

(b) Wafer annealing - initial Si-O-Si bonds formed between wafers

(c) Annealing continues - water driven from bond interface

Figure 6.3: *Mechanism of hydrophilic fusion bonding*

The increase in bond strength during the annealing stage for hydrophilic bonding is a result of silanol (Si-OH) surface groups being converted into siloxane (Si-O-Si) groups [193] [103] [194]. This reaction is closely related to the annealing temperature and the steps occurring during this reaction are shown in Fig. 6.3.

Although the cause of the bonding force is not universally agreed the most commonly suggested theory is that the surface force on the wafer is due to a hydrophilic film (usually a silicon oxide layer) that enables the bonding surface to be coated with both Si-OH and Si-O-Si bonds. The number of Si-OH bonds can be increased by the use of cleaning agents such as RCA or an O_2 plasma clean. The wafers are brought into contact and the Si-O-Si bonds react with water present at the interface in accordance with

$$Si - O - Si + H_2O \rightarrow Si - OH + HO - Si \tag{6.4}$$

This results in an increased number of hydroxyl (-OH) groups extending into the interfacial region and hence hydrogen bonds across the contacted surfaces, as represented by Fig. 6.3(a).

The presence of Si-OH, Si-H, Si-O and O-H bonds on the pre-annealed wafers has been verified through the use of infrared spectroscopy. This reaction occurs between temperature range lies between room temperature and $300°C$ where the bond strength does not differ much from the pre-anneal bond strength. Annealing between $300°C$ and $1000°C$ strengthens the bond by enabling the dehydration reaction of hydroxyl (-OH) groups and the formation of Si-O-Si bonds between the contacted surfaces to occur.

Wafer annealing at temperatures ($> 200°C$) causes the OH bonds to dehydrate which strengthens the bond by forming Si-O-Si bonds between the wafers as shown in Fig. 6.3(b). The underlying chemical reaction of this process is

$$Si - OH + HO - Si \rightarrow Si - O - Si + H_2O \tag{6.5}$$

At temperatures around $800°C$ it is thought that the surfaces deform easily and any remaining trapped water oxidises the surface [103]. The final annealing region starts at $1000°C$ with the bond strength approaching that of crystalline silicon in this region. Saturation of the bond strength occurs within a few minutes at annealing temperatures greater than $800°C$ whereas at the lower annealing temperatures the bond strength is known to slowly increase over a period of hours [172], [195] [191]. Annealing in these regions produces more siloxane bonds and the water produced by this reaction diffuses out as hydrogen gas from the interface, escapes from the edges or reacts with surrounding material. Any water or hydrogen that is not removed from the interface tends to accumulate and form defects. Fig. 6.3(c) shows that if the water successfully diffuses away from the interface through the oxide layer and reaches the underlying silicon substrate it reacts to form silicon oxide and hydrogen

$$Si + H_2O \rightarrow SiO_2 + H_2 \tag{6.6}$$

A form of direct bonding similar to this was used to produce the microchannels described in the previous chapter. Both wafers had an oxide layer on their bond side, one with a thick layer of PECVD that protected the sensors while the other had a thin native oxide. The thin native oxide made it easier for water to diffuse across to the underlying silicon to form the buried oxide needed for a reliable bond and also reduces the risk of hydrogen voids as they can better dissolve into the oxide.

6.3.7 Hydrophobic bonding

The mechanism for hydrophobic bonding differs from that of hydrophilic bonding [3] [196] [166] due to the absence of an intermediate oxide layer. The bonding surfaces are usually activated by etching them with hydrofluoric acid before bonding to remove any oxide on the wafers and to cover the surface with hydrogen or fluorine bonds. These bonds are highly reactive making it vital that bonding is carried out immediately after removal from the acid as failure to do so may result in contamination. These dangling chemical bonds form a weak bond between the wafers at room temperature because of van der Waal's forces. The hydrogen bonds start to realign as the temperature reaches 150-300^oC. When the annealing furnace has risen to 400^oC the desorption of hydrogen from the wafers initiates the following reaction:

$$Si - H + Si - H \rightarrow Si - Si + H_2 \tag{6.7}$$

Additional increases in the temperature eventually cause the silicon from one wafer to diffuse into the other at micro-gaps dotted across the surface resulting in a bond strength which can reach that of bulk silicon. The risk of voids forming within the interface is greater than with hydrophilic bonding due to the absence of an intermediate oxide layer and because of the generation of hydrogen.

6.4 Anodic bonding

6.4.1 Introduction

Anodic bonding is based on an electrostatic principle to form a bond between a sodium rich glass and a conductive substrate usually silicon [197] at temperatures that are often less than those used with fusion bonding. A basic design for an anodic bonder will have a high voltage power supply, a heat source and usually some means of applying pressure to the wafer stack. As shown in Fig. 6.4 the Pyrex/silicon wafer stack is placed between the two electrodes and heated.

The anodic bonder used throughout the course of this project was a Suss Microtec SB8 substrate bonder. This machine allows precise and repeatable control of the bonding parameters in a vacuum. Although it has the capability to align wafers with a Karl Suss mask aligner this was

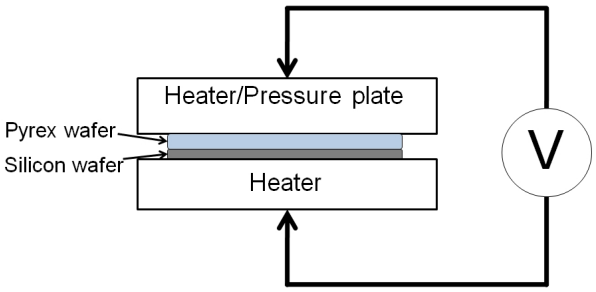
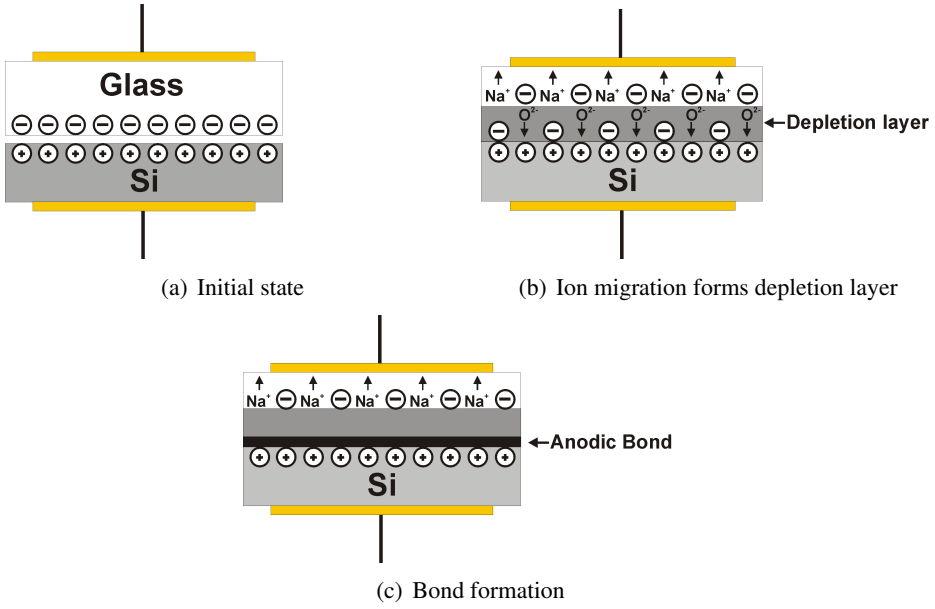


Figure 6.4: *Diagram of anodic bonder*



(a) Initial state

(b) Ion migration forms depletion layer

(c) Bond formation

Figure 6.5: *Mechanism of anodic bonding*

not used during the course of this work. Instead the wafers were manually aligned either by using the wafer flats or holes drilled into the glass for fluid inlet or outlets.

6.4.2 Mechanism of anodic bonding

The means by which the bond occurs is not fully understood but the most accepted explanation is that it is due to a combination of electric, chemical and thermal effects. It is has been widely proposed that the electric potential applied across the wafers pulls them together by means of an electrostatic force as represented in Fig. 6.5(a). Temperatures ($\geq 400°C$) used during anodic bonding result in the sodium dioxide present in the glass breaking down into sodium (Na^+) and oxygen ions (O^{2-}). The temperature and applied voltage (300 - 1000 V) drive the sodium ions in the glass towards the cathode and the oxygen ions in the opposite direction towards

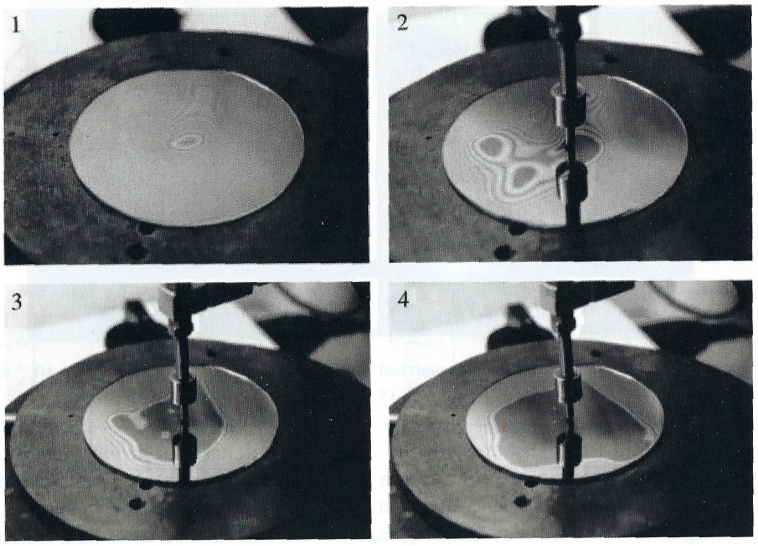


Figure 6.6: *Propagation of anodic bond with time [3]*

the silicon. This forms a depletion layer at the glass-silicon interface as shown in Fig. 6.5(b). A large drop in applied voltage occurs across this depletion layer and the high electric field generated pulls the silicon and glass closer together. The high temperatures aids the formation of silicon oxide at the glass/silicon interface as illustrated by Fig. 6.5(c) and in accordance with

$$Si + 2O^{-2} \rightarrow SiO_2 + 4e^- \tag{6.8}$$

Fig. 6.6 show the bond propagating out with time from the point where the voltage is applied.

6.4.3 Bonding glass to specific materials

The first anodic bonds were performed between metal foil and glass and since then other materials have been bonded to glass. Examples include silicon nitride, silicon oxide, sapphire and various metals with bonding of Pyrex to silicon being the most common [198] [199] [200] [201].

Bonding dielectric thin films such as silicon nitride or oxide films to glass has been the subject of much research and each of these studies have shown that bonding to dielectric thin films does not produce bond strengths comparable to those achieved by bonding silicon to glass. Previous work on anodic bonding to these materials indicates that the electrostatic force decreases as the dielectric thickness increases resulting in the bond strength dropping [201].

6.5 Bond strength measurement

6.5.1 Introduction

Determining the effect of the recipe parameters and the material choice on the bond strength requires characterisation. Several techniques exist to determine the quality and strength of bonded wafers. The method used depends on the requirements of the user, the type of bonding, the range of bond strengths expected and whether non-destructive testing is permissible.

6.5.2 Bond quality

Bond quality is usually assessed by inspecting for voids present at the bond interface. Bond inspection with anodic bonds can be easily performed due to the presence of transparent Pyrex. However this is not the case with fusion bonding as the required wavelength of light (λ) to propagate through the bonded silicon is inversely proportional to the band-gap energy (Eg) of silicon, where h and c are the Planck constant and speed of light respectively.

$$\lambda > \frac{hc}{Eg} \tag{6.9}$$

and this has a value of 1.12eV at room temperature. This means that wavelengths of greater than 1.10 μm are required to see through silicon [103], which can be provided by using an infra-red (IR) light source. The setup shown in Fig. 6.7 allows inspection of the bonding interface through silicon.

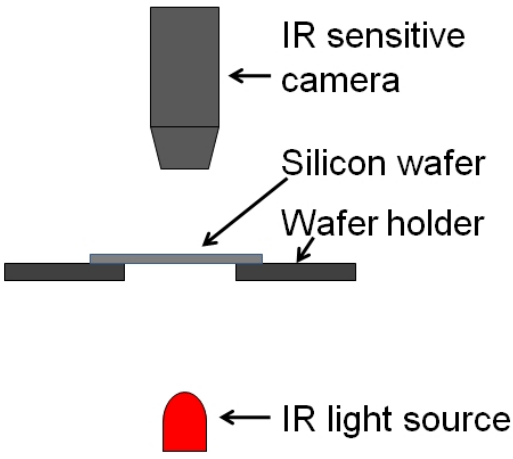


Figure 6.7: *Schematic of set-up used for inspection of bonds using infra-red*

Limitations of IR transmission are that the light is blocked from transmitting through to the detector if metal is present in the path of the light (metal appears opaque on the resulting images as it absorbs the light). Another limitation is that only voids or bubbles with heights greater than $\frac{\lambda}{4}$ can be detected. An example showing the absorption of light due to the presence of metal and the interference pattern of a typical interfacial void are shown in Fig. 6.8.

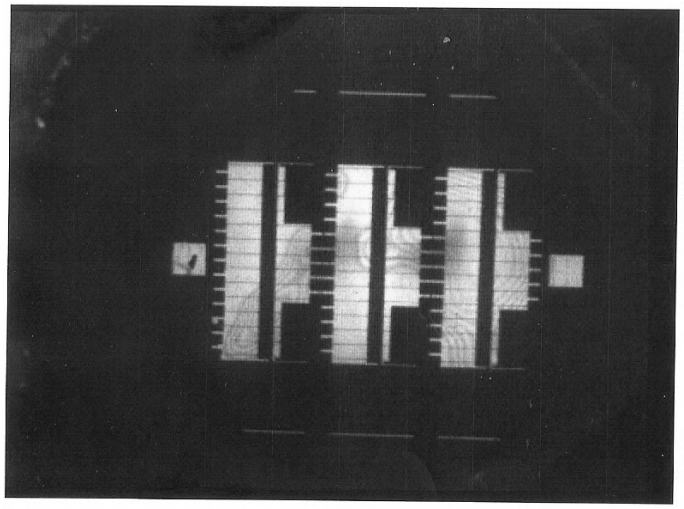


Figure 6.8: *Example showing blocking of infrared light by the presence of patterned metal layers within the wafer stack*

6.5.3 Bond strength

6.5.3.1 Introduction

Optical inspection of the bond interface allows the quality of the bond to be easily and quickly determined however quantitative measurements of factors such as bond strength are often more desirable. The bond strength can be measured in many ways and the various methods have their own advantages and disadvantages. An overview of some of these is presented in table 6.2.

6.5.3.2 Tensile testing

A standard method for measuring the bond strength is mechanical tensile testing. This involves dicing the bonded wafer into test samples which are then mounted onto studs and fixed in place with an adhesive. The studs are placed into a tensile testing machine where the studs are pulled apart. The bond is strained until it fractures at a certain force. This force divided by the area of the test sample gives the tensile strength at which the bond fractures.

Method	Advantages	Disadvantages
Tensile testing	Quick, well understood method	Expensive equipment needed, mounting of sample can affect result, sample may crack in substrate and not interface, destructive
Blister test method	Quick, wide range of bond strengths and types can be examined	Destructive
Knife edge testing	Cheap, direct method	Difficult to insert knife, destructive method
Chevron test structure	In-situ	Destructive, expensive microfabrication required to make structures
Predefined step test structure	Non destructive, in situ measurements.	Measured cheaply using microscope, expensive microfabrication needed to make structures
Cavity test structure	Non destructive, in situ measurements	Measures electrostatic pressure and only infers bond energy

Table 6.2: *Comparison of some bond strength measurement methods*

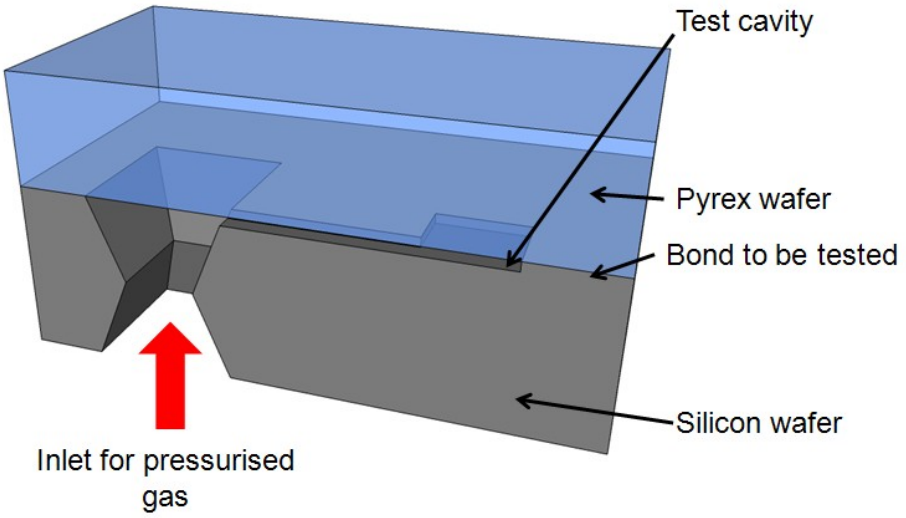


Figure 6.9: *Blister test structure*

This method has been used to measure the bond strength of fusion bonded and anodically bonded wafers. The tensile testing machine is a useful technique but does not always give an accurate measurement as the result can vary with the sample geometry and how the sample is mounted on the stud. A false result may also occur if the adhesive bond fixing the sample to the stud gives way before the sample bond. Other disadvantages of this method is that it requires the use of expensive equipment as well as the destructive nature of the test.

6.5.3.3 Blister test method

The blister test method was first proposed in 1961 for the testing of polymer adhesion by Dannenberg [202] and was developed by Shimbo [203] for waferbonding. Since then it has been used to characterise both fusion [204] and anodic [205] bonding. The blister test structure is shown in Fig. 6.9 and works by applying a load to the bond interface by pressurising a cavity situated at the interface. The pressure is gradually increased until fracture occurs at the bond. The bond strength can be calculated using this fracture pressure and the geometry of the cavity. This test structure can be used on both strong and weak bonds but it cannot be used on wafer stacks with unbonded areas. Unbonded areas may lead to gas leaks and hence erroneous fracture pressures. Recently non-destructive varieties of this test structure have also been reported [206] [207].

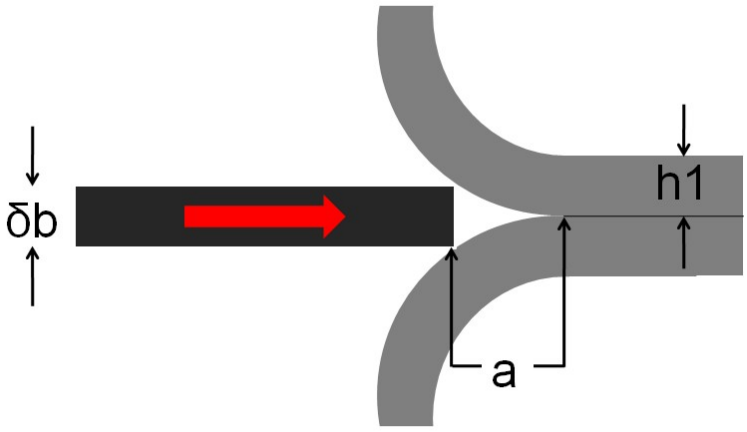


Figure 6.10: *Knife edge testing of bond strength*

6.5.3.4 Knife edge testing

The method was originally proposed by Maszara [208] and entails forcing bonded wafers apart at the wafer interface by the insertion of a thin metal blade of thickness δb as shown in Fig. 6.10. The void formed is related to the strength of the bond. Fusion bonds often use the same infrared inspection setup previously mentioned to determine the void length while ordinary microscopy can be used for anodic bonding. The length of the void is often measured against a known scale such as the width of the test structure for simplicity.The surface energy of the bond can be calculated from the void length.

$$G_C = \frac{3E\delta^2 t^3}{16a^4} \tag{6.10}$$

Where a is the crack length, t is the thickness of the wafer, E is the Young's modulus of the wafers and δ is the thickness of the inserted blade as shown in Fig. 6.10.

Disadvantages associated with these measurements include the difficulty inserting the blade between strongly bonded wafers without damaging the blade or causing unwanted damage to the

wafers. This may be circumvented by using an automated blade insertion machine. However this increases the cost of using this method. This method is limited to measuring relatively weak bonds and cannot successfully be used on bonds that require annealing to achieve full bond strength as the blades can break during insertion [209] [210]. However, recent publications have proposed means of overcoming this limitation [144] [211] [212].

6.5.3.5 Predefined step structure

These test structures are an extension of the knife edge method previously described. Originally developed by Knechtel [213] based on work previously reported by Horning et. al [214] they enable a non-destructive determination of the bond toughness.

Knechtel described two types of structures which both consist of mesas or raised steps. Single step test structures determine the bond strength by measuring the dimensions of the void formed around the structures after bonding with the greater the void the lower the bond strength. Multi-step structures consist of a series of steps with increasing distance between neighbouring structures. The bond strength is determined from the minimum sized gap between adjacent multi-step structures at which bonding occurs. The single step structure therefore provides an analogue measurement of the bond strength whereas the multi-step structure provides a discrete measurement. Although this is an immature measurement technique it allows non destructive, cheap and rapid tests of bond strength to be performed in situ. This method will be discussed in greater depth later in this chapter.

6.5.3.6 Chevron structure

The chevron test is a popular test structure and is similar in principle to the tensile test. As in tensile testing a load is applied to the specimen that has been patterned with chevron shaped notch as shown in Fig. 6.11. The load is gradually increased often using a tensile testing machine eventually forming a crack at the chevron tip. The crack propagation is stable up to a certain force. The increasing length of the crack decreases the stiffness of the sample until the crack reaches a critical length where the growth of the crack becomes unstable causing the sample to fracture [215] [216] [217] [218].

The critical crack length does not depend on material properties as only the critical length, load and the geometry of the chevron matter. Many models for several chevron designs have been

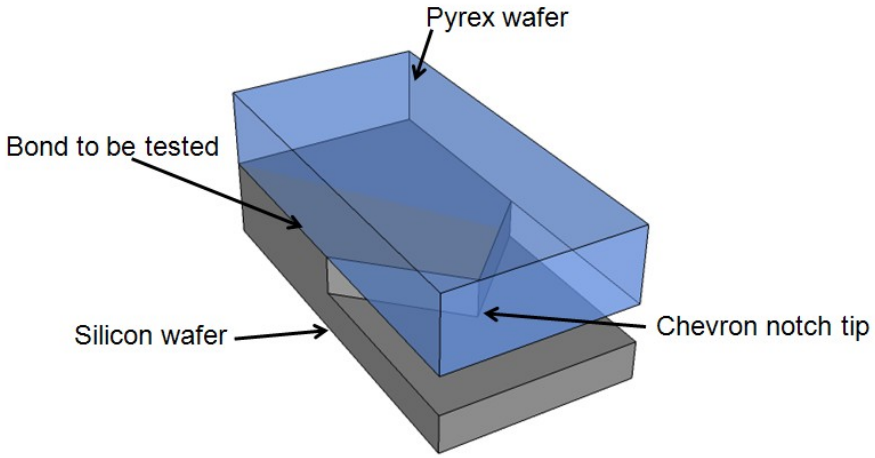


Figure 6.11: *Chevron test structure*

proposed for calculating the bond energy with varying degrees of success [215].

This method is a more accurate means of testing the bond strength than tensile testing [217]. Detrimental effects such as increased expense and the introduction of data scatter due to gluing the sample to the mount may be encountered with this method if a tensile testing machine is used to apply the load. An advantage of the chevron structure is that any strength or type of bond can be examined [215] and that the test structure can use small samples with samples of 1.5 mm by 1.5 mm having been reported [218].

6.5.3.7 Other methods

Nondestructive test structures based on cavities have also been reported. These allow the electrostatic pressure exerted during the bonding process to be characterised and not the bonding strength [219]. These test structures consist of a variety of cavities of different shapes and sizes. The bond quality is determined by whether the electrostatic pressure during the bonding process is sufficient to overcome the stiffness of the cavity and hence pull the cavity floor and the glass together forming a bond. The smaller the test structure bonded the greater the bond quality as these structures would have a higher stiffness.

	Recipe Parameters				
Recipe	Temperature ($^{\circ}C$)	Voltage (V)	Pressure (mbar)	% of Max. Current	Average Surface Energy (Jm^{-2})
1	400	400	150	5	$6.34E+03$
2	425	1000	800	5	$5.95E+03$
3	450	1250	800	2	$5.44E+03$

Table 6.3: *Comparison of average surface energy of various bonding recipes*

6.6 Anodic bond strength optimisation

6.6.1 Introduction

Anodic bonding was an important part of the device fabrication and to ensure the reliability of these devices it was necessary to characterise the initial recipes used and to optimise them for improved bond strength. Bonding took place between various combinations of materials including glass to silicon, glass to dielectric and glass to fusion bonded wafers and was characterised for each of these combinations.

6.6.2 Experiments

6.6.3 Bond strength measurement experiments: silicon to glass

6.6.3.1 Introduction

The microchannels in Chapter 3 consisted of etched silicon bonded to glass. Initially it was necessary to characterise the anodic bond as the substrate bonder had only been recently commissioned and the bond strength produced by the recipe provided by the manufacturer was unknown.

Subsequent recipes detailed in later chapters for the other microchannels used similar parameter values to those used by Go [144],Lee [198] and Tatic-Lucic [220] in an attempt to further improve the resulting bond strength. The values of these recipe parameters are compared in Table 6.3.

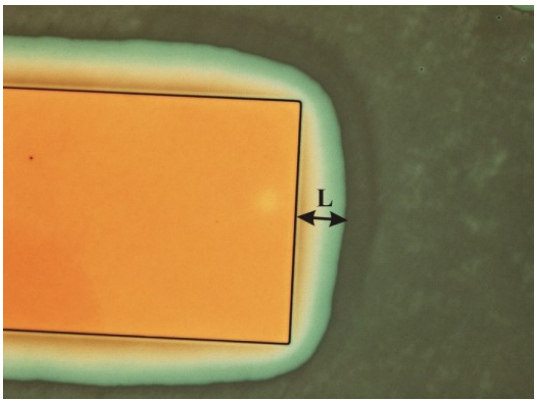


Figure 6.12: *Test structures for interfacial toughness measurement*

6.6.3.2 Fabrication of test structures

The average bond strength was determined using single predefined step test structures placed at regular intervals over the surface of a silicon wafer as shown in Fig. 6.12. These predefined steps have been previously used for the measurement of anodic bond surface energy [213]. Test structures were fabricated using titanium, which were measured to have an average thickness of 2781 $\mathring{A}$. Titanium was chosen because of its relative inelasticity which minimises any deformation of the mesa due to the load applied during bonding.

For the interfacial surface energy measurements these structures allow a continuous measurement of the void around the structure caused by bonding. The mask design used to pattern the titanium film arranges the $500\mu m$ wide and $1500\mu m$ long mesas in a checkerboard pattern across the surface. The repeated pattern of these structures on the wafer allows information regarding the bond uniformity and quality over the surface of the wafer to be determined

The test structures were formed using the lift off process with the resist being stripped using ACT-CMIS resist stripper and rinsed thoroughly with deionized water, acetone and IPA. The wafers were then rinsed a final time with deionized water and dried with compressed air. The glass wafers are cleaned by submerging them in a 2:1 piranha etch solution for 5 minutes and rinsing with deionized water. The wafers are dried using the LTEC Marangoni drier and measurements of the step height taken using the Dektak surface profilometer.

6.6.3.3 Method

After the test structures had been fabricated the silicon and glass wafer were manually aligned using their flats on the loading chuck of the bonder. The desired recipe parameters were entered into the machine, saved and the wafers loaded into the bonding chamber.

Images of the voids at the test structures were taken using the Reichart microscope camera and the void length was determined by using the width of the test structure as a reference length. The void length has been shown to be related to the interfacial surface energy of the bond (γ) [144] [215] [221]. An equation defining this relationship was developed by Go [144] which used the void length (L) along with the thickness of the glass wafer (h), the height of the test structures (δ_b).

$$\gamma = \frac{3h^3\delta_b^2}{c_1 L^4(1+\kappa\eta^3)} \tag{6.11}$$

The compliance of each wafer (c_1) can be found using their respective Young's modulus (E) and Poisson's ratio (ν).

$$c_i = \frac{8(1-\nu_i)}{E_i} \tag{6.12}$$

The ratios of the compliances and heights of the two wafers are given by κ and η respectively.

$$\kappa = \frac{c_1}{c2} \tag{6.13}$$

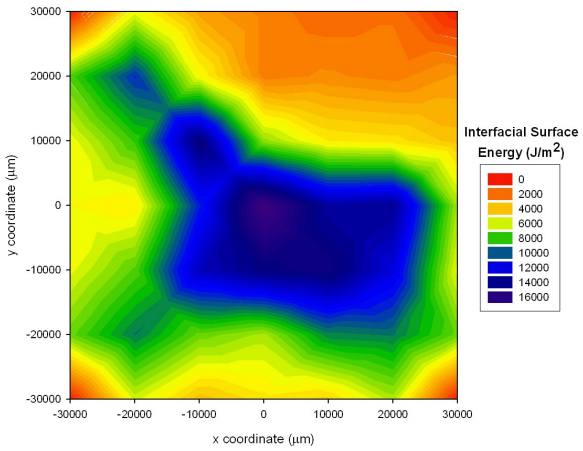
$$\eta = \frac{h_1}{h_2} \tag{6.14}$$

To obtain surface plots from the data it was necessary that the interfacial surface toughness values for the areas with no mesa structures be extrapolated. The extrapolated value of a square was found by using the average value of the neighbouring squares where measurements were taken. Some of the surface plots produced from the data are shown in Fig. 6.13. Each recipe was run three times to determine the repeatability of the bonding process. The values of surface energy were calculated using Equation 6.11. The calculated values are higher than typically

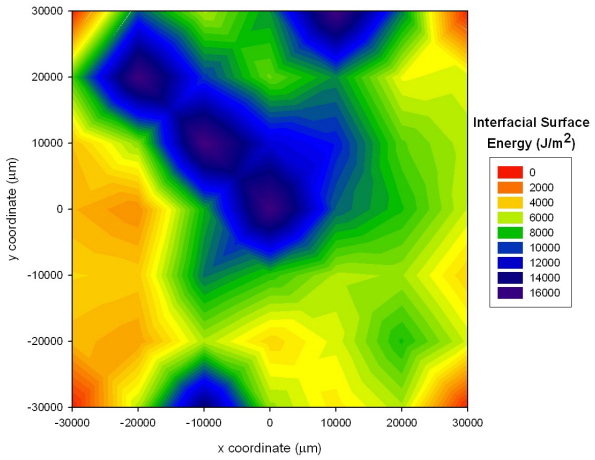
reported results and a contributing factor which explains this may be related to the validity of the model for wafer to wafer bonding. The model assumes that the bonded wafers behave as beams but this has been shown to not always be a valid assumption due to geometrical factors such as shape, length and width. Experiments have shown that a comparison between measurements taken on beam-like samples and those from whole bonded wafer samples result in shorter crack lengths being formed on whole bonded wafers and hence higher bond energies [222]. Finite element analysis carried out using the knife edge method showed that such assumptions can lead to errors of up to 25% between the results calculated using models with the beam like behaviour assumption and finite element models [223].

Fig. 6.13(a) and Fig. 6.13(b) show spots of high surface energy which correspond to areas close to or directly underneath the central or Y-shaped electrodes. It was also noted that the third recipe resulted in a more uniform surface energy over the wafer. This may be attributed to the use of a higher temperature that increased the mobility of the ions and the use of a higher voltage resulting in a greater electric field attracting more of the mobile ions within the glass to the wafer interface. Furthermore the bond lasts for longer and has more time to propagate out from the electrodes as the bonding conditions are terminated when the measured bonding current reaches 2% of the maximum current ensuring a more uniform distribution of surface energy.

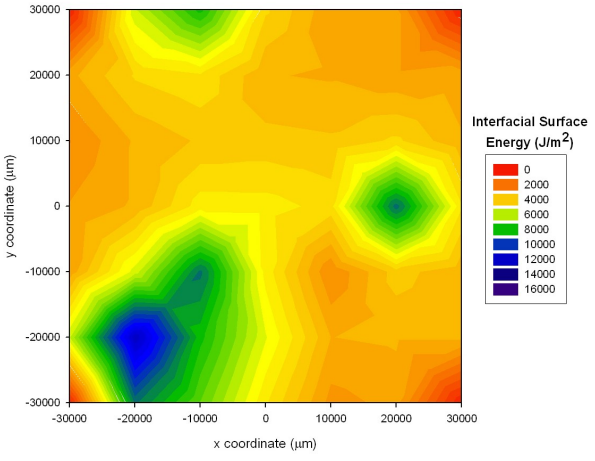
Fig. 6.14 shows the average of surface energy of each of the three recipes over the the three measurements taken. Recipe 3 as well as producing the most spatially uniform surface energy also has the lowest variation between the three runs with a standard deviation of 1117 Jm^{-2} compared to 1281 and 2876 Jm^{-2} for recipe 2 and 1 respectively. Although recipe 3 uses the highest temperature, voltage and pressure and lowest percentage of maximum current of the three recipes it has the lowest mean bond energy of the three runs at 5405 Jm^{-2}. This suggests that the effect of the parameters and the interactions between the parameters on the final bond energy is not linear and non-intuitive. This approach while useful as a first attempt does not lead to a better understanding of how the recipe parameters affect the bond strength or how to counter the issues encountered with anodic bonding during the micro-channel fabrication. These measurements also do not take into account the effect of the dielectric layers within the wafer-stack on the final bond strength, which is thought to be a major contributing factor to the bond delamination observed.



(a) Recipe 1



(b) Recipe 2



(c) Recipe 3

Figure 6.13: *Interfacial surface energy over 3" wafer for various anodic bonding recipes*

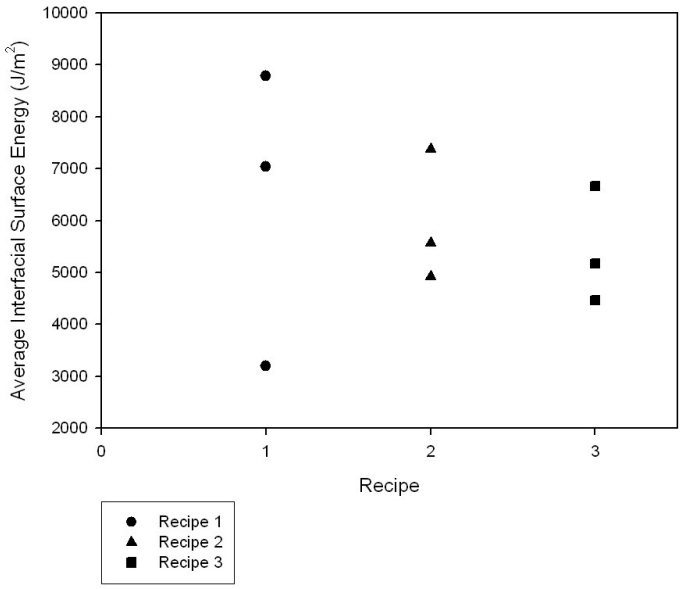


Figure 6.14: *Average surface energy of bonding recipes*

6.6.4 Bond strength measurement experiments: dielectric to glass

6.6.4.1 Introduction

The location of the anodic bond delamination described in section 5.2.4.4 occurred within the 0.1 μm film of PECVD oxide between the silicon and Pyrex 7740 and previous results [224] [201] suggest that the presence of a dielectric layer affects the bond strength detrimentally. However, the sensitivity of the anodic bond strength to the presence of this dielectric layer is unknown for this process. The previous tests demonstrated the non-linear nature of the anodic bonding process and experimental design techniques were used to gain a better understanding of the effect of bonding parameters such as temperature, load pressure and voltage on the bond strength between the glass and dielectric. It was necessary to know this for any future improvement of the recipes. The same mesa structures as described in section 6.6.3 were again used.

6.6.4.2 Design of Experiment

The effect of the four factors of interest on the bond strength could be determined using traditional methods of experiment design where one factor is varied one at a time between the values of interest while the other factors remain constant. This allows a controlled comparison of one changing factor with all the other factors but this is not desirable as it is time consum-

ing, costly, not suitable for multiple factors and unable to guarantee reproducibility of results. Full-factorial methods whereby all possible permutations of factor levels are investigated is also time consuming, for example 4 factors with 3 levels each would require 3^4 i.e. 81 experiments to be run.

The best solution is found by another design of experiment method that is based on orthogonal arrays that also enables the independent evaluation of the effect of each of the factors on the system. The factors are allocated to columns when designing the array with each factor associated with a number of levels and each row of the array representing the combination of factor levels to be run in the experiment. An example is shown in Table 6.4. The result of one row is not of primary interest with this method of experimental design. Instead it is the average change in response over a number of experimental runs that is of interest. This allows independent assessment of factor levels from a reduced number of experimental runs [225].

One such method that used orthogonal arrays is based on the Taguchi method. This method, named after Genechi Taguchi is based on fractional factorials where only a portion of the experiments that would be carried out using the full factorial method are investigated. This reduces the number of experiments, the time and cost spent. The Taguchi method is primarily used in off-line quality control which means that the goal of this method is to enable the design of a process such that it meets a specified target with a minimum of variation i.e. the process is robust and repeatable [225].

In this experiment each of the four controllable factors were assigned three levels, A L9(4^3) design was generated from these requirements. The four control factors used were the dielectric thickness, bonding temperature voltage and applied pressure, each factor had three levels. The resulting array and the associated control factor settings are shown in Table 6.4. The duration allowed for the bond to propagate throughout the glass-dielectric interface was initially set at 30 minutes for initial experiments [226].

6.6.4.3 Method

The single sided, N doped (100) silicon wafers were coated with a dielectric film of 0.5, 1 or 1.5 μm thickness using the STS PECVD tool. The mesa structures were fabricated on this film using the same lift-off process used for the tantalum and nickel sensors as detailed in section 6.6.3.2.

Recipe	t (μm)	T (° C)	V (V)	P (mbar)
1	0.5	350	-750	500
2	0.5	400	-1000	750
3	0.5	450	-1250	1000
4	1.0	350	-1000	1000
5	1.0	400	-1250	500
6	1.0	450	-750	750
7	1.5	350	-1250	750
8	1.5	400	-750	1000
9	1.5	450	-1000	500

Table 6.4: *A L9 Taguchi matrix with the parameter values used in in bond strength optimisation*

The two wafers were placed in contact with each other on the bonding chuck. The wafer stack was covered with a graphite shim and clamped in place before loading into the anodic bonder chamber. The anodic bond recipe was modified using the parameters specified by the relevant experimental run detailed in Table 6.4. After the recipe had run its course the wafers were removed and let to cool before images were taken of the voids formed around the mesas using the Reichart microscope. The length of these voids at the midpoint along the width of the mesas were calculated from the image by using the known width of the test structure as a reference.

6.6.4.4 Results

Initially the bonding recipes ran for 30 minutes but not all wafers were fully bonded after removal from the substrate bonder. The more complete bonds were found to occur when the dielectric film was thinner with unbonded areas and weak bonds occurring in most of the thicker film wafers as shown in Fig 6.15. From past experience of bonding silicon to glass, a wafer can be said to have been bonded fully when the resistance is such that the current applied to the wafer has reached 5% or less than of the peak applied current which usually occurred after approximately 15 minutes for silicon-glass bonding . The reason that several wafers were incompletely bonded is most likely due to a combination of the there being insufficient bonding time for the bond to propagate across the wafer and also the dielectric film impeding the depletion layer necessary for the bonding process from forming. The voids formed around mesa structures on these unbonded wafers could not be measured with any confidence resulting in an unbalanced orthogonal array. Hence the lack of results for these recipes would have affected

the validity of any Taguchi analysis performed using them.

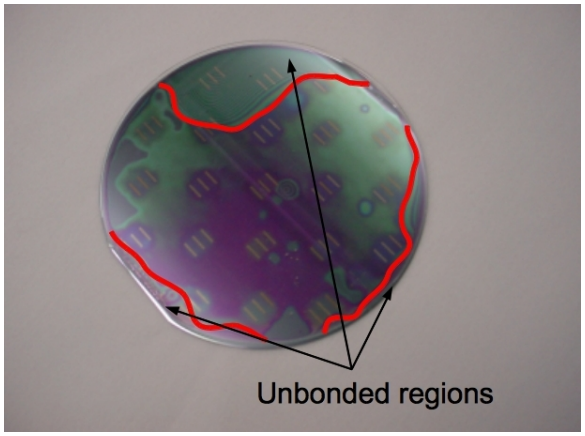


Figure 6.15: *Partially bonded wafer*

The experiments were repeated with the recipe run time increased from 30 minutes to 1 hour. Measurements of the length of the void formed around a mesa were initially taken at five points across the wafer, these points were the centre, left most, right most, top and bottom squares. The mean void length ($\bar{L}$) was calculated and these results are shown for both nitride and oxide films in Tables 6.5. From the void lengths the bond surface energy could be calculated and these results were inserted into the orthogonal array generated with the Taguchi method.

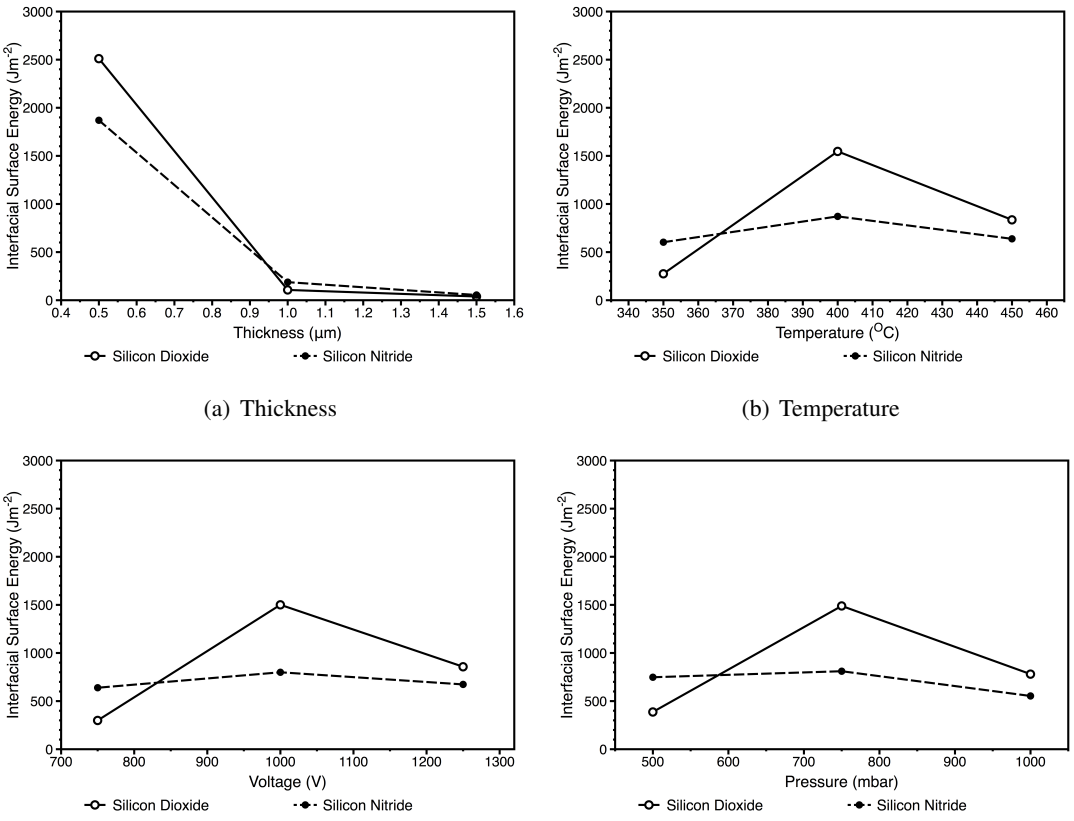
	Recipe Parameters				$\bar{L}$ (μm)		*Surface Energy* (Jm^{-2})	
Recipe	t (μm)	T ($\circ$ C)	V (V)	P (mbar)	Nitride	Oxide	Nitride	Oxide
1	0.5	350	-750	500	66.6	80.6	1.75E+3	8.16E+2
2	0.5	400	-1000	750	62.6	52.9	2.24E+3	4.39E+3
3	0.5	450	-1250	1000	67.9	62.0	1.62E+3	2.33E+3
4	1.0	350	-1000	1000	18.2	270	3.16E+1	6.50E+0
5	1.0	400	-1250	500	98.4	109	3.68E+2	2.41E+2
6	1.0	450	-750	750	121	147	1.63E+2	7.40E+1
7	1.5	350	-1250	750	185	328	2.91E+1	2.96E+0
8	1.5	400	-750	1000	277	257	5.86E+0	7.95E+0
9	1.5	450	-1000	500	128	134	1.28E+2	1.05E+2

Table 6.5: *Initial results of the recipe matrix used in bond strength optimisation experiments - Nitride and Oxide films, 1 hour bonding*

These results were only used to generate main effects plots to determine the sensitivity of the bond surface energy to the each of the four factors. The calculated values of the bond energy may be higher than expected and again this is attributable to the model used. Additionally a possible source of error to consider is that the wafer compliance term of equation 6.12 only considers the compliance of the silicon wafer and does not take into account either the effect of

the intrinsic residual stress of the dielectric layers or the thermal stress due to any mismatch of thermal coefficient of expansion between the dielectric layers and the Pyrex.

Comparing Fig. 6.16(a) with the graphs of the other factors shown in Fig. 6.16(b) to 6.16(d) it can be seen that the presence of the dielectric layers at the bond interface appears to have the most significant effect on the bond energy. These interfacial dielectric films act as an impediment to the formation of high strength bonds in several ways such as the drop in potential across the dielectric film and the longer timescales required as they act as a barrier to the ions which have to diffuse across the film to form the bond with the underlying silicon [227], [201].



(a) Thickness

(b) Temperature

(c) Voltage

(d) Pressure

Figure 6.16: *Results of Taguchi optimisation for oxide and nitride films*

The detrimental effect of a dielectric film at the interface on the bond strength can be seen from Fig. 6.16(a) where the surface energy decreases with increasing oxide film thickness as expected and drops from 2512 Jm^{-2} for a 0.5 μm down to 39 Jm^{-2} for a 1.5 μm giving a 98 $\%$ drop in bond energy while a drop of 97 $\%$ for nitride was observed. The relationship between the two is nonlinear as the bond strength appears to be inversely proportional to the square of

the thickness of the dielectric. The silicon nitride films tend to act as good diffusion barriers and this may contribute for the weaker bond strengths observed for thicker films in comparison to oxide films of a similar thickness. This is consistent with previously published works that state it is difficult to obtain a better bond strength for an anodically bonded nitride film than it is for oxide [201] [224] [228]. This variation in behaviour between the oxide and nitride films is reflected in the results shown in Fig. 6.16(a) through to 6.16(d) where a lower bond energy is observed for all factors compared to the equivalent results for the oxide film. This can explain why the microchannel devices lacking the 0.1 μm oxide film at the glass silicon interface did not result in the glass shearing off under experimental conditions while those with the 0.1 μm film present did. The removal of this film improved the yield of the devices. However, this is not the only dielectric layer within the wafer stack to be anodically bonded. The effect of the PECVD oxide layers protecting the heaters and sensors must also be taken into account when optimising the anodic bonding process.

It can also be seen between Figs 6.16(b), 6.16(c) and 6.16(d) that the relationship of the bond energy to the temperature, voltage or pressure are similar for both the nitride and oxide films. In each case the relationship is non-linear as it initially increases before an optimal value is reached and after which the bond energy decreases.

The thickness of dielectric films at the interface is the most significant effect on the process followed by the temperature. Increased temperatures lead to increased decomposition of sodium oxide within the alkali glass and hence greater ion mobility. The voltage is the next most sensitive factor. A higher voltage leads to an increased bond strength as a stronger electric field increases the rate of migration of bonding ions. Higher bond strength from increased load pressure would lead to improved contact between the glass and silicon wafers at higher loads.

6.6.5 Investigation of anodic bonding to fusion bonded wafers

6.6.5.1 Introduction

Etching of a fusion bonded wafer stack is key to forming the microchannel devices described in this thesis. The silicon wafer stack contains two dielectric layers with one sandwiched between the silicon wafers and the other at the bottom of the wafer stack. The purpose of these layers was to protect the temperature sensors and heaters and to provide a smooth and flat surface to ensure a good fusion bond.

The extent to which the dielectric layers at these locations affect the bond strength was unknown. It was not thought that they interfere with the actual process of bond formation like the film previously placed at the bond interface but it is expected that they still lead to a lower bond due to a drop in potential across the wafer. Whether the effect of the layers present in the silicon wafer stack is stronger than those of those at the glass-silicon interface was unknown.

6.6.5.2 Design of Experiment

The sensitivity of the anodic bond surface energy to changes in the thickness of these oxide layers and the recipe parameters was determined using a fractional factorial design. This experimental design allowed the effect that several factors have on the process to be varied simultaneously to study the changes to the main effect and the low-order interactions between the factors that may go undetected using a more traditional approach.

The main effects and low-order interactions can be estimated and tested from measuring the response of only a few carefully chosen factorial combinations but at the expense of detecting high-order interactions. It is assumed that the interactions between many factors are rarely complex so discarding the high-order interactions is very unlikely to negatively affect the results. Additionally the use of a fractional design rather than a full factorial design avoided a large number of expensive and time consuming experimental runs.

A two level fractional factorial design was used with a centre point as this allowed both linear first order effects to be fitted and for curved second order effects to be detected [225]. Previous experiments used a Taguchi design only allowed factors to be analysed independently of each other and did not highlight the effect of interactions between parameters have on the process.

The four factors of interest for the experiment were the total thickness of oxide throughout the wafer stack, the applied voltage, the bonding temperature and the percentage of maximum current at which the bonding is aborted. The effect of pressure on the system was not incorporated into the design of experiment as it had been reported in literature that of the anodic bonding process was the least sensitive to changes in load pressure. This was not seen in the previous experiments but this was expected to be due to the presence of the dielectric at the interface dominating the bonding and altering the bonding process and did not reflect the standard silicon-glass bonding process. Pressure was replaced with the percentage of maximum measured current as this indicates when to cut-off the anodic bonding process, it determines the

No.	Oxide Thickness (μm)	Voltage (V)	Temperature (^{O}C)	Percentage of I_{max}
1	0	1000	425	1
2	7	800	425	1
3	7	1000	425	5
4	0	800	400	1
5	0	1000	400	5
6	0	800	425	5
7	7	1000	400	1
8	7	800	400	5
9	3.5	900	413	3

Table 6.6: *Fractional factorial experimental runs*

duration of the bonding process which has been demonstrated to have a significant effect on the quality of the bond in all previous experiments.

A two-level fractional factorial design for such an experiment resulted in 9 runs, one of them being the centre run. The experimental runs and the parameters used within the recipes are shown in Table 6.6.

6.6.5.3 Method

Some bonded silicon wafer stacks had one of the constituent wafers coated with PECVD oxide films of thickness 3.5 μm on both sides. This PECVD oxide was polished for 2 minutes on both sides using the Presi CMP polisher. All of the wafers to be bonded were cleaned and fusion bonded together. The bonded wafers were annealed in a furnace at 435 ^{O}C for 17 hours. After removal from the annealing furnace the titanium mesas were fabricated as before.

The 500 μm thick wafers of Corning 7740 were placed in a Piranha etch for 10 minutes before being removed and rinsed thoroughly with deionised water and dried in the Maragoni drier. The Corning 7740 wafer and the silicon wafer stacks were manually aligned on the anodic bonder loading chuck and clamped in place using the supplied clamping plate. The wafers were then loaded into the substrate bonder using the experimental values detailed in Table 6.6. The load pressure was then applied to the wafers and kept constant at 800 mbar for all runs. After unloading the wafers images were taken of the voids formed around the mesa structures for use in calculating the surface energy of the bond.

No.	Oxide Thickness (μm)	Voltage (V)	Temperature (^{O}C)	Percentage of I_{max}	Interfacial Surface Energy (J/m^2)
1	0	1000	425	1	1.80E+4
2	7	800	425	1	1.07E+4
3	7	1000	425	5	1.25E+4
4	0	800	400	1	1.26E+4
5	0	1000	400	5	1.21E+4
6	0	800	425	5	1.15E+4
7	7	1000	400	1	9.12E+3
8	7	800	400	5	1.49E+4
9	3.5	900	413	3	1.32E+4

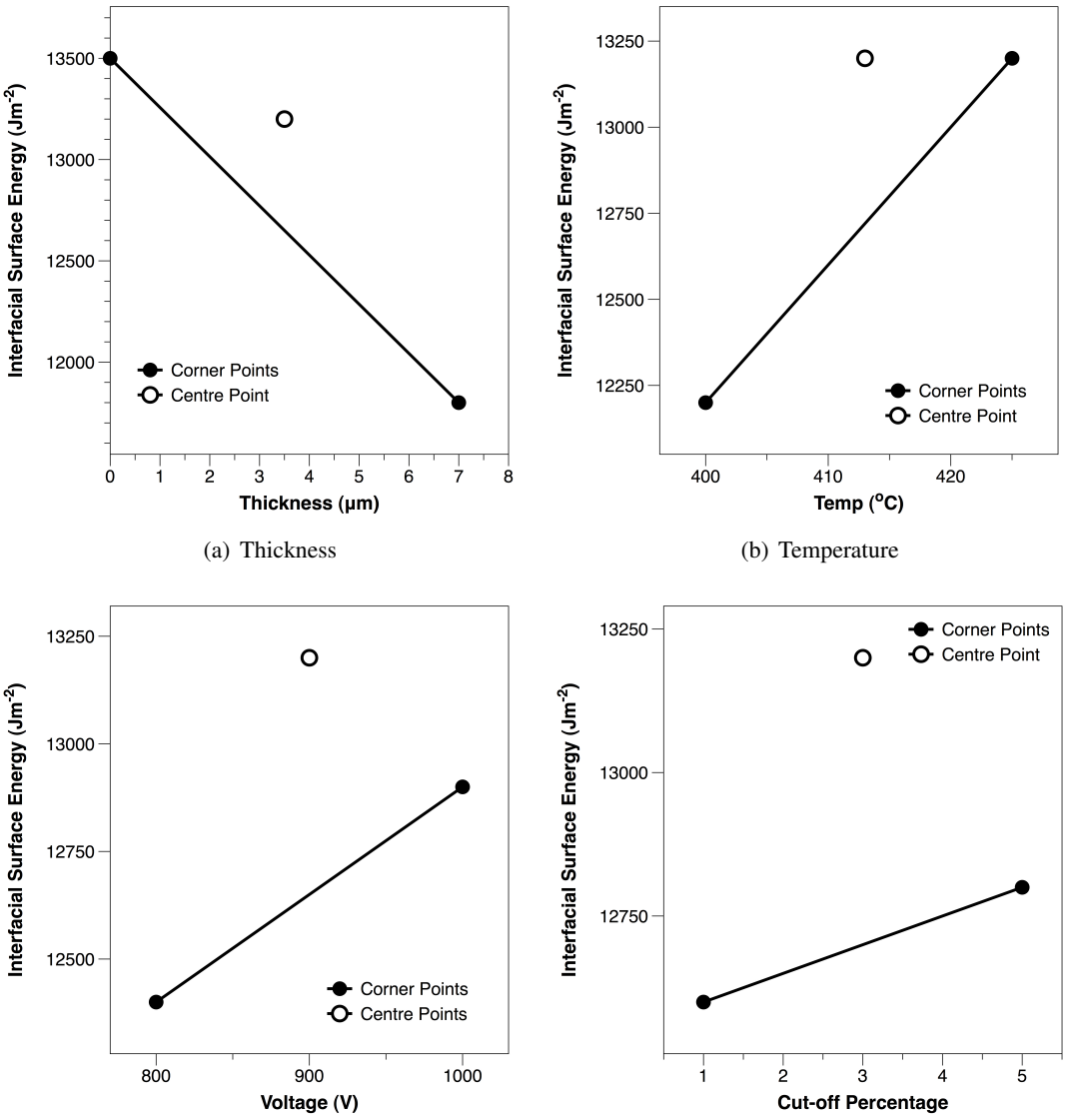
Table 6.7: *Results of fractional factorial experimental runs for anodic bonding to fusion bonded wafer characterisation*

6.6.5.4 Results

Images of the voids formed around the centre raised step at each of the 21 sites located at regular intervals across the wafer were taken with an optical microscope and the length of the voids calculated using the known width of the steps as a reference. The void length was taken from the midpoint along the width of the step where its dimension was at maximum. The length of the voids were inserted into Equation 6.11 to find the interfacial surface energy at that point. The thickness of the silicon wafer was 760 μm due to the use of the fusion bonded wafer stack. The effect of the oxide layers on the wafer compliance was ignored as it was assumed that the stresses acting on one side of the bottom wafer are cancelled out by the equal but opposite stresses acting on the other side.

The average bond strength was used in conjunction with factorial analysis to see the effect of the changing parameters on the bond. The results are shown in Fig. 6.17(b) to 6.17(a) for all four parameters and the interactions between these factors were also evaluated. The calculated bond energies were again noticeably higher than expected which may again be explained by the limitations of the model proposed by Go and also due to the compliance of the fusion bonded wafer stack not including the effect of the intrinsic stress due to the oxide layers and fusion bonding.

As expected an increase in the thickness of the oxide layers results in a decrease in average in. Figure 6.17(a) shows the surface energy dropped from 1.35E+04 to 1.18E+04 Jm^{-2} when the total oxide thickness was increased from 0 to 7 μm, a 13% reduction in bond energy. The smaller drop in percentage bond energy per unit thickness for these wafers compared to those



(a) Thickness

(b) Temperature

(c) Voltage

(d) Cut-off Percentage

Figure 6.17: *Effect of varying recipe parameters on bond energy for a fusion bonded wafer*

where the dielectric film is located at the anodic bond interface

This translates to a 1.85% compared to a 98% decrease in percentage difference of bond energy per unit thickness when a dielectric film is at the bond interface. The smaller drop per unit thickness is due to the location of the dielectric film as the bond forms without a disrupting interfacial oxide barrier layer at the glass-silicon interface. However a drop in surface energy still occurs due to the oxide films causing a drop in potential across the entire wafer stack with a lower potential across the anodic bond interface. The reduced potential across the bond

interface results in a reduction of bond energy.

Increased voltage and temperature results in an increased surface energy as shown in Figure 6.17(c) and 6.17(b) respectively. Increasing the temperature from 400 to 425^oC results in the bond energy increasing from 1.22E+04 to 1.32E+04 Jm^{-2}. Increasing the voltage from 800 to 1000 V causes the bond energy to increase from 1.24E+04 to 1.29E+04 Jm^{-2}. This is expected with the reactions that occur during silicon to glass bonding. The fact that this occurs for fusion bonded wafer stacks further demonstrates that the presence of oxide at any point in a fusion bonded wafer stack other than at the bond interface results in the normal anodic bonding reactions occurring with only the resulting bond energy dropping with increased oxide thickness.

The interactions between the various factors are shown in Fig. 6.18. Previous studies of the anodic bonding process have only taken the main effect of the various factors into account and not the interactions between them. Parallel lines suggest a lack of interaction between factors. None of the lines are parallel in Fig. 6.18, meaning that the interactions between the factors effects the bond strength along with the levels of the factors themselves, this needs to be taken into account when developing recipes in future.

The left most column in Fig. 6.18 contains plots showing the interaction between the voltage, temperature and percentage of maximum current with the dielectric thickness. Some of these plots show that the average surface energy does not decrease with increasing dielectric thickness for certain factor levels. Increased average surface energy is observed when the voltage is either set to 1000 V, the temperature is 400^oC or the percentage is 5$\%$. Optimising the anodic bond recipe for a dielectric thickness of 7 μm is not as straightforward as setting the factors to these values as these factors do not operate independently of each other. As shown in the voltage row when the voltage is 1000 V and the temperature is 400^oC or when the voltage is 1000 V and the percentage is 5$\%$ the anodic bond energy decreases.

Although the drop in bond energy due to presence of oxide layers could be counteracted by increasing the applied voltage and temperature there are further limits to this approach that need to be recognised. Of the two, the bond strength was reported to be most sensitive to temperature [144] which is shown by the results of the experiment. Besides the limitations to this imposed by the coupled nature of the various factors there were also limits imposed by the glass. The thermal coefficients of expansion (TCE) of silicon and glass are well matched

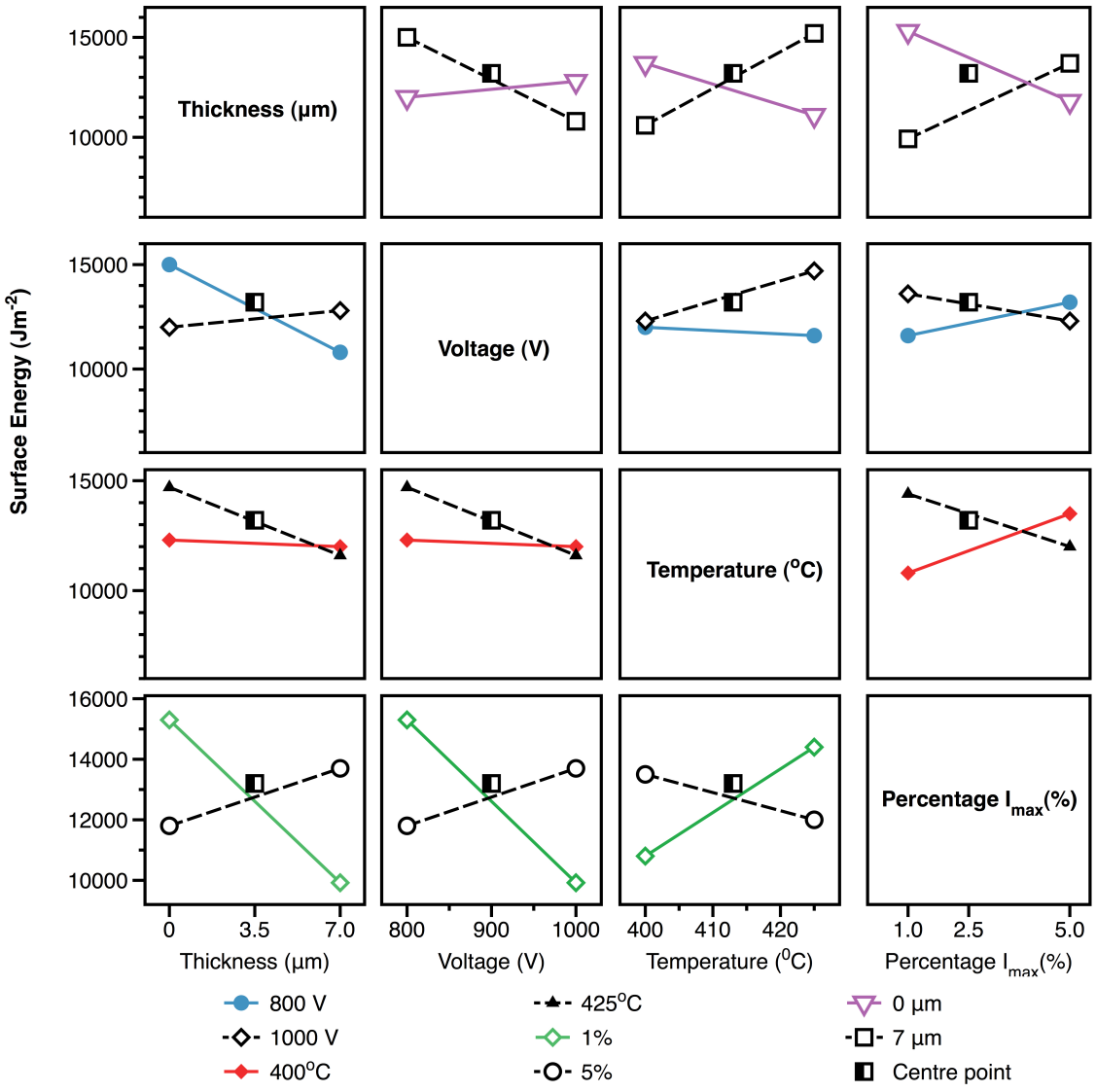


Figure 6.18: *Interactions of various experimental factors*

only over a range of temperatures with the length of this range depends on the type of alkali glass used. For the glass used for these experiments was Corning 7740 has a TCE that is well matched with silicon up to $300°C$, above this the TCE of the two materials begin to diverge. If the bonding temperature is significantly increased to compensate for the drop in bond energy due to the oxide layers then the difference between the TCE of the two materials may induce thermal stresses at the bond interface which may limit the reliability and quality of the bond.

Another factor which may limit the bond strength of the sealed microchannel wafers but has not been considered as a factor in these tests is the presence and geometry of etched features in the wafer [229]. The mechanical forces exerted by dicing saw have also been demonstrated to be the initiating factor for bond delamination. The extent to which the delamination spreads from the diced edges into the remainder of the bonded area varies depending on a variety of factors such as the handling of the finished device and quality of the bond.

6.7 Conclusions

Test structures have been successfully used to improve the understanding of anodic bonding of glass to silicon and to thin film dielectrics. Improved understanding of the process lead to improvements in the reliability and strength of the bonds. The test structures offer advantages over previous methods used to achieve similar process optimisation. The primary benefit being the ability to run non-destructive in-situ anodic bond measurements on process wafers. The main limitation of this method is the lack of a robust and accurate model to allow accurate conversion of experimental measurements of void length into bond energy.

Experiments were conducted on the substrate bonder to characterise the bonding of dielectric thin films to glass and fusion bonded wafer stacks to glass wafers for use. It was successfully demonstrated that the presence of dielectric thin films at the bond interface leads to weak and poor bonds as the dielectric films at this location impede the bonding process. It was also found that for fusion bonded wafer stacks that the bond strength drops by 13% when the total thickness of the oxide within the stack is increased from 0 to 7 μm and that although temperature and voltage were shown to have a noticeable effect on the bond strength the relationship between the factors was not independent. The development of an optimised recipe is shown to be non-trivial due to the complex interactions between the factors. Previous studies of the anodic bonding process using Taguchi methods did not consider the effect of these interactions and

concerned themselves solely with the main effects of the factors.

Chapter 7
Conclusions and future work

7.1 Introduction

A process for fabricating novel bulk micromachined microchannels with integrated sensors has been developed and successfully produced devices that enabled thermal engineers to better characterise the boiling process in microchannels [38] [37] [34]

7.2 Summary of achievements

Several processes of increasing complexity have demonstrated that the fabrication of bulk micromachined channels with integrated sensors is possible [34]. To the author's knowledge the integration of thin film temperature sensors on the floor of bulk micromachined channels was not achieved previous to this work. The process consisted of multiple steps such as wafer bonding, etching, metal deposition and photolithography.

These devices were used to characterise fluid flow for boiling studies with the simplest microchannel design shown to remove heat fluxes up to 175 Wcm^{-2} under uniform heating conditions. These results from these experiments increased the understanding of the boiling process at the microscale and enabled improved heat transfer system design for applications such as heat removal for next generation microprocessors. [2] [38] [37].

After each iteration of the design and process any areas for improvement were identified and addressed to produce devices with nickel temperature sensors with a positive TCR, reduction of the net stress within the silicon wafer stack due to PECVD oxide by altering the deposition sequence and removal of the oxide from the top of the microchannels to improve the anodic bond.

Previously the limited information available on how the various recipe parameters affect the bond strength impeded any attempt to improve the anodic bond strength. Optimisation of the anodic bonding process for bonding to dielectric thin films and to silicon wafer stacks was

achieved by using test structures. The test structures enabled non-destructive in-situ anodic bond measurements on process wafers, which is an advantage over other types of characterisation methods for bonding. The improved understanding of the effect of various recipe parameters on the process gained by the use of these test structures will lead to stronger and more reliable bonds. However, this work has shown that the development of an optimised recipe is non-trivial due to the complex interactions between the factors. These interactions were not uncovered by previous studies of the anodic bonding process using Taguchi methods as they concerned themselves solely with the main effects of the factors.

7.3 Future work

As with any process there is room for further improvement. This section suggests means for adding extra functionality or improving the fabrication process.

7.3.1 Integration of additional elements

Integration of additional elements or the redesign of present elements can add increased functionality to the microchannels. This would further improve the understanding of boiling at the microscale. Two examples discussed in the following sections are redesigning the heater to approximate non-uniform heating and the integration of pressure sensors in addition to the temperature sensors.

7.3.1.1 Non-uniform heating

Non-uniform heating of the microchannel would contribute to the optimal design of two phase flow heat transfer systems for next generation microprocessors. Microprocessors generate a non-uniform heat flux over the surface which should be reflected in future microchannel designs.

Heaters that can achieve this have been successfully created with other microchannel devices based on the fabrication process developed for this project and could easily be integrated without changing the fabrication process. One means that was used to achieve this involved redesigning the heater so that it has multiple current and voltage contact pads as shown in 7.1. This ensures that current only flows and heat is generated only through part or all of the

heater. [2] [36].

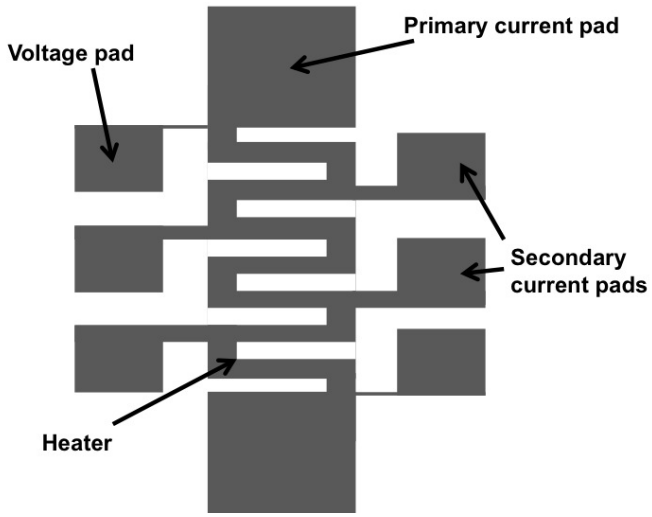


Figure 7.1: *Schematic of non-uniform heater*

7.3.1.2 Pressure sensors

The integration of pressure sensors to the microchannels can be used to determine how both pressure and fluid flow are affected by boiling at the microscale. Again, this would lead to greater improvements in the design of future heat transfer systems.

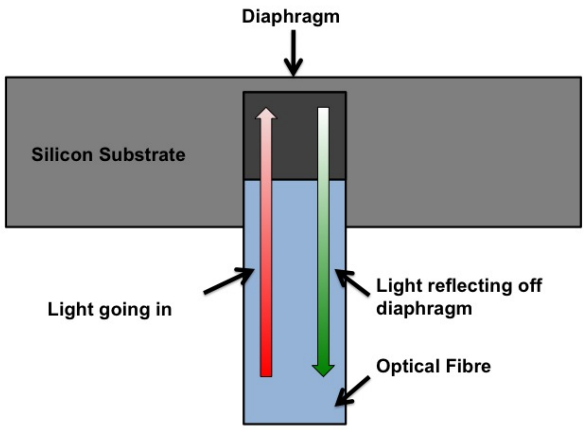


Figure 7.2: *Pressure sensor design*

Some pressure sensors consist of a diaphragm, which deflects upon a change in pressure. This change in deflection can be detected by electrostatic, piezoresistive or optical means. The

majority of optical pressure sensors reported in literature are interferometric and consist of a thin, reflective diaphragm coupled to an optical fibre as shown in 7.2. The intensity of the reflected light exhibits a sinusoidal response when the diaphragm deflects due to a change in external pressure.

The diaphragm can be created by etching from the backside of the same wafer containing the heater and the sensors as shown in 7.3. The cavity terminating in the diaphragm should be fabricated within the gap between the turns of the heater and due to the tapered profile produced by wet anisotropic etching it would be recommended that it be etched using the Bosch process. These recommendations should minimise any disruption to the design and operation of the heater, which would not be desirable for any heat transfer experiments.

7.3.1.3 Conclusion

Other additional features that could enhance the final device include a condenser and micro-pump. This would allow the entire closed loop system that would be required for future microprocessors to be placed on a single chip. Implementing these additional features would be challenging and would require modification of the fabrication process already detailed.

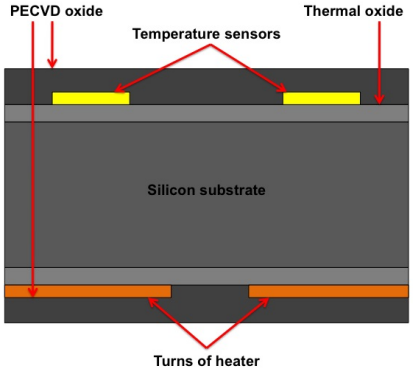
7.3.2 Improvements to future fabrication processes

There are areas where the current fabrication process could be improved such as fabricating the sensors without the use of lift-off processing, ensuring a more uniform oxide thickness along the channel sidewalls and reducing the thickness of the oxide layers to achieve a more reliable anodic bond. Changes such as these may allow quicker and more reliable fabrication.

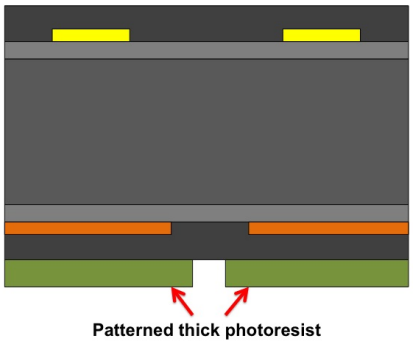
7.3.2.1 Sensor fabrication

Sensor fabrication was performed using a lift-off process, which is not generally used in the semiconductor industry due to the issues associated with it such as the retention, redistribution and incomplete removal of sacrificial metal. As noted in Chapter 4 the use of a lift-off process was not the initial choice for patterning the metal sensor layer so replacing all the lift-off processing with etching could improve the fabrication and reliability of the sensors.

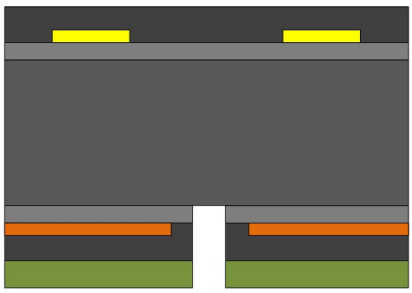
Etching could be used either one of two ways to fabricate the temperature sensors. The first



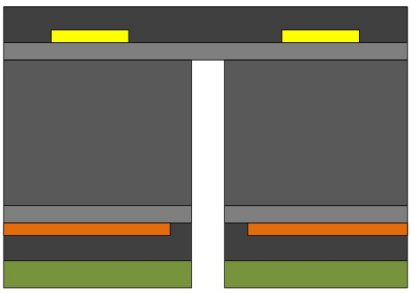
(a) Silicon wafer with fabricated temperature sensors and heater



(b) Patterning of thick photoresist



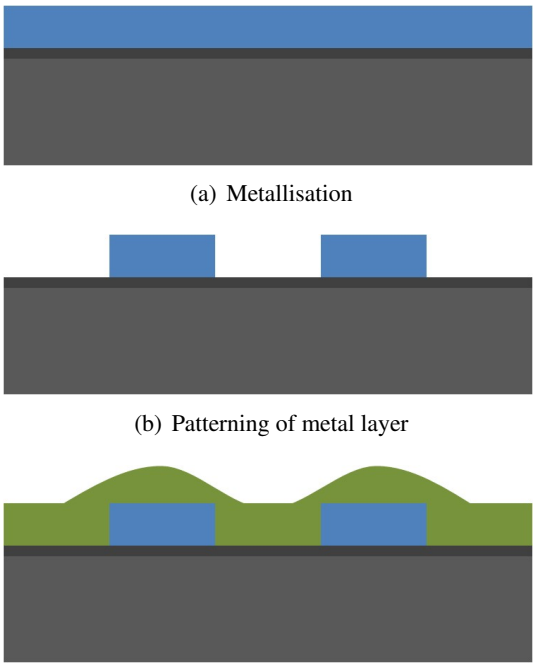
(c) Reactive ion etching of silicon oxide



(d) ICP etching of silicon

Figure 7.3: *Pressure sensor diaphragm fabrication*

method results in a single layer metal sensor and the second in a multi-layer metal sensor and interconnect. Deposition and patterning of a single metal layer as illustrated in Fig. 7.4 produces the single layer metal sensor. This method is the simplest of the two but the choice



(a) Metallisation

(b) Patterning of metal layer

(c) Deposition of dielectric layer

Figure 7.4: *Single metallisation layer sensor fabrication*

of metal may make this method undesirable within the context of the device design. The metal chosen must meet the needs of both the temperature sensor (a good TCR and high resistivity) and the interconnects (a low resistivity). A compromise in either the choice of metal used or performance of either the sensor or the interconnects has to be made as the needs of the sensor and the interconnect are contradictory.

Deposition of at least three layers is required to construct the multi-layer metal sensor with two of these layers being metals and the other an intra-layer dielectric. The fabrication process for a multi-layer metal sensor is illustrated in Fig. 7.5 and involves the deposition and patterning of the first metal layer that is subsequently coated with a dielectric film. Electrical contact between the two metal layers is achieved through the use of etch holes in the dielectric film that are filled to form plugs composed of the second metal layer. The possibility of voids forming in the plugs connecting the two metal layers leading to poor electrical contact and reliability issues along with the need to planarize the intra-layer dielectric before the second metallization because of the morphology of the underlying first metal layer adds extra complexity, time and expense to the fabrication of these sensors. However, this method would be the more preferable of the two for future microchannel devices as the use of two separate metals enables the independent optimisation of the sensors and interconnects.

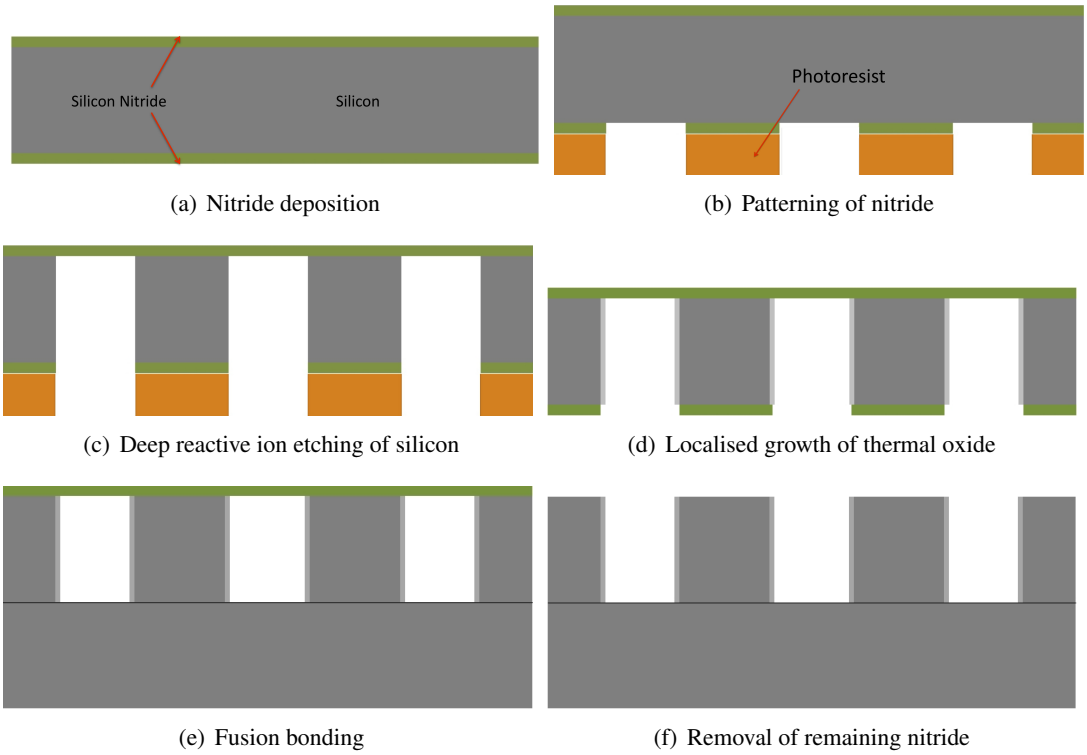
(a) Patterned metal film

(b) Deposition and planarization of PECVD oxide

(c) Etching of plugs in PECVD oxide

(d) Patterning of second metal film and final PECVD layer

Figure 7.5: *Multi-layer metallization process for future sensor fabrication*



(a) Nitride deposition (b) Patterning of nitride

(c) Deep reactive ion etching of silicon (d) Localised growth of thermal oxide

(e) Fusion bonding (f) Removal of remaining nitride

Figure 7.6: *Parallel microfabrication process*

7.4 Improving sidewall deposition

Etching away the top layer of PECVD oxide has been previously shown to improve the anodic bond as detailed in section 5.2.5.1. However, this removes the PECVD oxide coating the top of the sidewalls. Unfortunately PECVD oxide does not guarantee the same wetting and thermal properties along the channel walls due to this sidewall etching and the nonuniform coating of trenches inherent with CVD. Thermal oxidation ensures uniform and conformal coating of the sidewall but the presence of the existing metal layers prevents its use. Experiments carried out have shown that the surface roughness of a $0.1\mu m$ thick thermal oxide film grown on a deep etched channel sidewall is 0.17 μm compared to $0.5\mu m$ for a PECVD coated channel.

Currently a blank double sided polished silicon wafer is fusion bonded with a processed silicon wafer on which the sensors and heaters have been fabricated on opposite sides. After the fusion bonding has successfully taken place the channel is etched. Processing the bottom wafer and top wafer as two separate batch of wafers with one batch forming the channel and the other the sensors and heater could allow thermal oxide to be grown on the channel sidewalls. The main difficulty of etching the channels before fusion bonding is the presence of the thermal

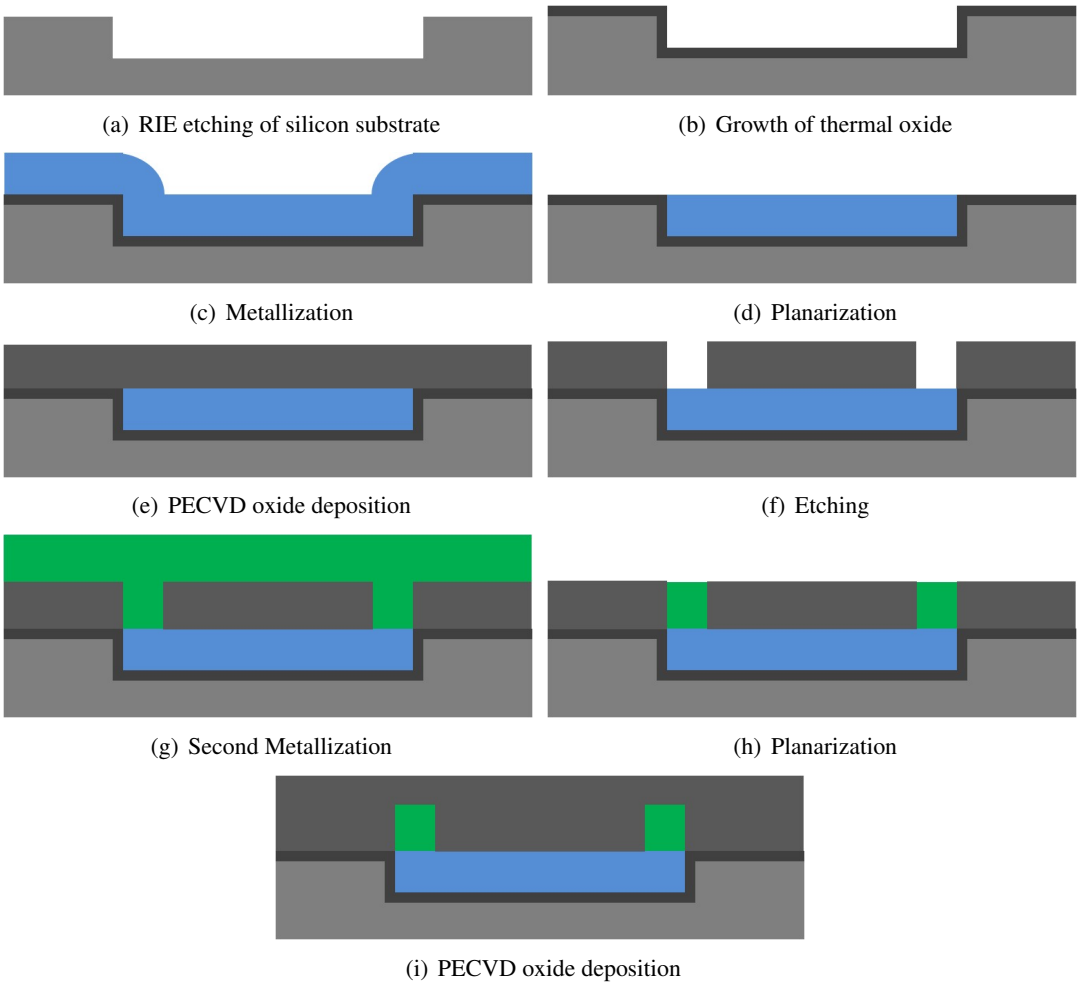
isolating structures. This requires that the wafer is supported during process by a handle wafer or other means to prevent the channel from sliding out from the wafer after it is removed from the etching tool. This will need to be taken into account with any proposed process if a redesign of the masks is not possible.

Any proposed processing scheme must protect the wafer surfaces for bonding and allow the reliable fabrication of any isolated structures. A proposed fabrication process illustrated in Fig. 7.6 may meet these requirements. Stoichiometric nitride would be grown on a blank, double sided polished, (100) silicon wafer in a furnace as shown in Fig. 7.6(a) that protects the silicon bonding surface from attack. The use of similar protective layers has been highly effective in the past in protecting the bonding surface [230]. The wafer would be coated with thick resist that is patterned and developed to expose areas of nitride that would be etched away to the underlying silicon. The patterned nitride and resist layers as shown in Fig. 7.6(b) would act as a masking layer during deep etching of the silicon with the Bosch process as represented in Fig. 7.6(c).

Stripping the resist after etching allows the nitride mask to act as a diffusion barrier to prevent any oxidation from occurring via the local oxidation isolation method (LOCOS). The sidewalls are oxidised in the furnace to grow a 0.1 μm thick layer of oxide as in Fig. 7.6(d). The use of thermal oxidation rather than PECVD oxide would allow a more uniform layer to be formed but LOCOS leads to the formation of a birds beak structure at the edges of the nitride mask due to lateral oxidation. Due to the requirements of surface roughness demanded by both fusion and anodic bonding some means or either preventing, removing or minimising this effect may need to be investigated.

Next the KS-MA8 would be used to precisely align and pre bond the two wafers as seen in Fig. 7.6(e). Afterwards the remaining nitride should be removed before annealing of the bond as the long duration, high temperature nature of the annealing stage will cause unwanted changes in the intrinsic stress of the PECVD nitride layer. Removal of this nitride must ensure that the surface roughness of the exposed silicon allows anodic bonding to be performed.

This microfabrication process may offer other advantages due to the presence of the channels during fusion bonding such as a reduced risk of intrinsic voids formation [103] and a more compliant wafer that facilitates the bond formation [231].



(a) RIE etching of silicon substrate
(b) Growth of thermal oxide
(c) Metallization
(d) Planarization
(e) PECVD oxide deposition
(f) Etching
(g) Second Metallization
(h) Planarization
(i) PECVD oxide deposition

Figure 7.7: *Damascene process for future sensor fabrication*

7.4.0.2 Reducing the oxide thickness

Sensors could also be fabricated by employing the damascene process where trenches are etched into the surface of the wafer, that are then coated with a metal layer to fill in the trenches and finally planarized to remove the excess metal [183]. These steps are illustrated in Fig. 7.7.

The use of a planarized metal layer to produce sensors would be advantageous as thinner layers of PECVD silicon oxide would be achieved. For the current process the PECVD coating the sensor after CMP is approximately 2 μm but by using a damascene process could possibly reduce this to 1.2 μm. These films would require a shortened CMP time for fusion bonding and result in an increase in the anodic bond strength as indicated in Chapter 6.

7.5 Anodic bonding

Delamination of the anodic bond was observed to be initiated by the dicing of the glass. This is partially attributable to the mechanical forces acting on the bond interface coupled with the low anodic bond strength produced by the presence of dielectric thin films within the wafer stack. Chapter 6 indicated that reducing the dielectric film thickness led to an improvement in anodic bond strength, but these experiments did not take the channel geometry into account that is expected to degrade the bond strength [229]. Further experiments that take into account the geometry of structures etched into the substrate are needed to develop design rules which will lead to better anodic bonding.

The test structures used to determine the bond energy could also be developed further. The relationship between the void formed around these test structures and the bond energy is beyond a doubt but the model used to calculate the bond energy from the measured void dimensions is based upon assumptions that be may not be valid. Finite element models not based on these assumptions have been developed but these are computationally intensive and have not been used to validate existing models. A compact model developed for these test structures without the existing assumptions could lead to more accurate characterisation of future bond recipes.

7.6 Conclusion

The work described in this thesis has successfully led to the development of processes for fabricating simple microchannels as well as microchannels with integrated sensors. A detailed description of the reasoning behind the design and the steps used in the fabrication process has been presented. A novel feature of the more complex process is that waferbonding has enabled sensors to be placed along the bottom of the bulk micromachined channel facilitating the localised measurements of the heat-flux and temperature changes due to two phase flow heat transfer. Both the simple channels and more complex channels have been used in such studies [36] [34]. Several issues identified in the initial batch of devices that featured tantalum sensors such as the negative TCR of the sensors, low anodic bond strength and thin film stresses were successfully corrected in the subsequent batch featuring nickel sensors.

Further improvement of the anodic bond was hindered by a lack of understanding of the effect of the presence and location of dielectric thin films within the silicon wafer stack on the bond

strength. Characterisation of the effect of these layers on the bonding process was successfully carried out using design of experiment methods. This work will enable improved bonding recipes to be developed between Pyrex glass and fusion bonded wafer stacks containing dielectric films of various thicknesses.

Appendix A
Runsheets

A.1 Runsheet for silicon microchannels

The section contains the runsheet detailing the fabrication process of the silicon microchannels discussed in Chapter 3.

Runsheet for silicon microchannels with integrated tantalum temperature sensors

Step	Process	Tool	Process details	Comments
1	Oxidation	Furnace Tube 10	Grow 250 nm thermal oxide, Recipe WETOX14 for 40 mins	
2	Measurement	Nanospec	Measure film thickness uniformity	
3	Coating	3 inch track	Recipe 1-2-1	1.5 μm of SPR 350 resist baked at 90^{O}C for 60s
4	Photolithography	Karl Suss MA8	Proximity contact with spacers, 8 second exposure	
5	Develop	3 inch track	Recipe 9-1-1	Baked at $115°C$ for 60s
6	Etching	Plasmatherm	Etch exposed oxide for approximately 100 minutes	
7	Measurement	Nanospec		Measure exposed areas to ensure oxide removal
8	Etching	STS ICP etcher	Etch 300 μ m	Approximately 100 minutes with SCUBA 61 recipe
9	Measurement	Vickers microscope	Measure channel depth	
10	Ashing	Barrel asher	Remove resist	60 minute
11	Etching	Wet Deck	48 % HF solution used to remove oxide	

Runsheet for silicon microchannels with integrated tantalum temperature sensors

Step	Process	Tool	Process details	Comments
12	Measurement	Nanospec		Measure to ensure all oxide is removed
13	Cleaning	Wet Deck	Glass dipped in piranha etch solution for 10 minutes. Followed by DI water rinse for silicon and glass and drying in Marangoni drier	Piranha etch is 1 part of H_2O_2 to 2 parts of H_2SO_4.
14	Bonding	Karl Suss SB8		
15	Dicing	Disco Dicing Saw		Rinse after dicing to remove grit and debris from channels

A.2 Runsheet for silicon microchannels with integrated tantalum sensors

The section contains the runsheet detailing the fabrication process of the silicon microchannels with integrated heater and tantalum temperature sensors discussed in Chapter 4.

Runsheet for silicon microchannels with integrated tantalum temperature sensors

Step	Process	Tool	Process details	Comments
1	Oxidation	Furnace Tube 10	Grow 500 nm thermal oxide, Recipe WETOX14 for 40 mins	
2	Measurement	Nanospec	Thickness measurement	
3	Measurement	Dektak Profilometer	Wafer bow measurement	
4	Coating	3 inch track	Program 1-8-9,Manual dispense of AZ2514E	
5	Coating	3 inch track	Program 1-9-9	
6	Photolithography	Karl Suss MA8	Proximity contact w spacers, 8 second exposure	Sensor mask
7	Coating	3 inch track	Program 9-9-5	
8	Photolithography	Karl Suss MA8	Proximity contact w spacers, 45 second exposure	
9	Develop	Wet Deck	Manual develop for 1.1 with AZ726 MIF	
10	Deposition	Balzers sputterer	0.6-0.8 μm Tantalum	
11	Stripping	Wet Deck	Ultrasonic bath of ACT-CMIS	Continue until clear
12	Measurement	Dektak Profilometer	Measure Topology	

Runsheet for silicon microchannels with integrated tantalum temperature sensors

Step	Process	Tool	Process details	Comments
13	Coating	3 inch track	Program 1-8-9, Manual dispense of AZ2514E	
14	Coating	3 inch track	Program 1-9-9	
15	Photolithography	Karl Suss MA8	Proximity contact w spacers, 8 second exposure	Interconnect mask
16	Coating	3 inch track	Program 9-9-5	Bake for 2 minutes at $120°C$.
17	Photolithography	Karl Suss MA8	Proximity contact w spacers, 45 second exposure	
18	Develop	Wet Deck	Manual develop for 1.1 mins with AZ726 MIF	
19	Deposition	OPT sputterer	0.5 μm of aluminium	
20	Stripping	Wet Deck	Ultrasonic bath of ACT-CMIS	Continue until clear
21	Measurement	Dektak Profilometer	Measure Topology	
22	Anodization	Wet Deck	Electrical parameters of 2mA and 60V	
23	Cleaning	Wet Deck	DI water followed by Acetone and IPA	
24	Deposition	STS PECVD	2.5 μm of HFSIO	

Runsheet for silicon microchannels with integrated tantalum temperature sensors

Step	Process	Tool	Process details	Comments
25	Measurement	Nanospec	Thickness measurement	
26	Measurement	Dektak Profilometer	Wafer bow measurement	
27	Annealing	Furnace 8	17 hours at 435°C	
28	Measurement	Dektak Profilometer	Wafer bow measurement	Turn wafer over to process other side
29	Deposition	Balzers sputterer	1.0 μm of Al w 4% Cu	
30	Coating	3 inch track	Program 1-2-1	
31	Photolithography	Karl Suss MA8	Proximity contact w spacers, 8 second exposure	Heater mask
32	Develop	3 inch track	Program 9-1-1	
33	Etching	STS Al etcher	Etch for 60 minutes with 3SBD1 recipe	
34	Ashing	Barrel Asher	Ash until removed	
35	Measurement	Dektak Profilometer	Measure Topology	
36	Deposition	STS PECVD	2.5 μm of HFSIO	
37	Measurement	Nanospec	Thickness measurement	

Runsheet for silicon microchannels with integrated tantalum temperature sensors

Step	Process	Tool	Process details	Comments
38	Measurement	Dektak Profilometer	Wafer bow measurement	
39	Annealing	Furnace 8	17 hours at 435°C	
40	Measurement	Dektak Profilometer	Wafer bow measurement	
41	Polishing	Presi Polisher	Topography removal	
42	Cleaning	Wet Deck	10:1 solution of DI water to TMAH for 2 mins	Particulate removal
43	Measurement	Nanospec	Thickness measurement	
44	Measurement	Dektak Profilometer	Wafer bow measurement	
45	Cleaning	SSEC Wafer Scrubber	DI water rinse	
46	Surface Preparation	Plasmatherm	Plasma activation by 2 mins of oxygen plasma	
47	Bonding	Bonding Rig	Contact wafers	Bond processed wafer to another bare wafer
48	Measurement	IR lightsource and camera	Void detection	Separate wafers if void present

Runsheet for silicon microchannels with integrated tantalum temperature sensors

Step	Process	Tool	Process details	Comments
49	Measurement	Dektak Profilometer	Wafer bow measurement	
50	Annealing	Furnace 8	17 hours at 435°C	
51	Measurement	Dektak Profilometer	Wafer bow measurement	
52	Coating	3 inch track	Program 1-8-1, followed by 9-1-1 on coating track, 1-9-9 on developer track twice	Manual dispense of SPR 220-7
53	Photolithography	Karl Suss MA8	Proximity contact w spacers, 45 second exposure	Channel mask
54	Develop	Wet Deck	Manual develop with 1.5 minutes with MF 26A	
55	Etching	STS ICP etcher	380 μm etching, approximately 3.5 to 4 hour etch	
56	Ashing	Barrel Asher	Ash until removed	
57	Deposition	STS PECVD	0.1 μm of HFSIO	
58	Measurement	Nanospec	Thickness measurement	
59	Cleaning	Wet Deck	Acetone, IPA followed by DI water. Dried with compressed air.	

Runsheet for silicon microchannels with integrated tantalum temperature sensors

Step	Process	Tool	Process details	Comments
60	Bonding	Karl Suss BA8	Recipe: $400°C$, a peak voltage of 1000 V and a pressure of 800 mbar.	
61	Dicing	Wafer dicer	Glass dice and silicon dice	
62	Coating	Wet Deck	Manual application of SPR 220-7 on sensor side	
63	Etching	Plasmatherm		Etch oxide from sensor pads
64	Stripping	Wet Deck	Ultrasonic bath of ACT-CMIS	Continue until clear
65	Coating	Wet Deck	Manual application of SPR 220-7 on heater side	Etch oxide from heater pads
66	Etching	Plasmatherm		
67	Stripping	Wet Deck	Ultrasonic bath of ACT-CMIS	Continue until clear

A.3 Runsheet for silicon microchannels with integrated nickel sensors

The section contains the runsheet detailing the fabrication process of the silicon microchannels with integrated heater and nickel temperature sensors discussed in Chapter 5.

Runsheet for silicon microchannels with integrated nickel temperature sensors

Step	Process	Tool	Process details	Comments
1	Oxidation	Furnace Tube 10	Grow 500 nm thermal oxide, Recipe WETOX14 for 40 mins	
2	Measurement	Nanospec	Thickness measurement	
3	Measurement	Dektak Profilometer	Wafer bow measurement	
4	Coating	3 inch track	Program 1-8-9, manual dispense of AZ2514E	
5	Coating	3 inch track	Program 1-9-9	
6	Photolithography	Karl Suss MA8	Proximity contact w spacers, 8 second exposure	Sensor mask
7	Coating	3 inch track	Program 9-9-5	
8	Photolithography	Karl Suss MA8	Proximity contact w spacers, 45 second exposure	
9	Develop	Wet Deck	Manual develop for 1.1 mins with AZ726 MIF	
10	Deposition	Balzers sputterer	0.025 μm titanium	
11	Deposition	Balzers sputterer	0.25 μm nickel	
12	Stripping	Wet Deck	Ultrasonic bath of ACT-CMIS	Continue until clear

Runsheet for silicon microchannels with integrated nickel temperature sensors

Step	Process	Tool	Process details	Comments
13	Measurement	Dektak Profilometer	Measure Topology	
14	Coating	3 inch track	Program 1-8-9, Manual dispense of AZ2514E	
15	Coating	3 inch track	Program 1-9-9	
16	Photolithography	Karl Suss MA8	Proximity contact w spacers, 8 second exposure	Interconnect mask
17	Coating	3 inch track	Program 9-9-5	
18	Photolithography	Karl Suss MA8	Proximity contact w spacers, 45 second exposure	
19	Develop	Wet Deck	Manual develop for 1.1 mins with AZ726 MIF	
20	Deposition	OPT sputterer	0.25 μm of titanium nitride	
21	Deposition	OPT sputterer	0.5 μm of aluminium	
22	Stripping	Wet Deck	Ultrasonic bath of ACT-CMIS	Continue until clear
23	Measurement	Dektak Profilometer	Measure Topology	
24	Coating	3 inch track	Program 1-2-1	

Runsheet for silicon microchannels with integrated nickel temperature sensors

Step	Process	Tool	Process details	Comments
25	Photolithography	Karl Suss MA8	Proximity contact w spacers, 8 second exposure	Edge metal removal mask
26	Develop	3 inch track	Program 9-1-1	
27	Etching	STS Al etcher		
28	Stripping	Wet Deck	Ultrasonic bath of ACT-CMIS	
29	Cleaning	Wet Deck	DI water followed by Acetone and IPA	
30	Deposition	STS PECVD	0.1 μm of HFSIO	
31	Measurement	Nanospec	Thickness measurement	
32	Measurement	Dektak Profilometer	Wafer bow measurement	
33	Measurement	Dektak Profilometer	Wafer bow measurement	Turn wafer over to process other side
34	Deposition	Balzers sputterer	1.0 μm of Al w 4% Cu	
35	Coating	3 inch track	Program 1-1-1	
36	Photolithography	Karl Suss MA8	Proximity contact w spacers, 8 second exposure	Heater mask
37	Develop	3 inch track	Program 1-1-1	
38	Etching	STS Al etcher	Etch for 60 minutes with 3SBD1	

Runsheet for silicon microchannels with integrated nickel temperature sensors

Step	Process	Tool	Process details	Comments
39	Stripping	Wet deck	Ultrasonic bath of ACT-CMIS	
40	Coating	3 inch track	Program 1-2-1	
41	Photolithography	Karl Suss MA8	Proximity contact w spacers, 8 second exposure	Edge metal removal mask
42	Develop	3 inch track	Program 9-1-1	
43	Etching	STS Al etcher		
44	Stripping	Wet deck	Ultrasonic bath of ACT-CMIS	
45	Measurement	Dektak Profilometer	Measure Topology	
46	Coating	3 inch track	Program 1-1-1	
47	Photolithography	Karl Suss MA8	Proximity contact w spacers, 8 second exposure	Edge metal removal mask
48	Develop	3 inch track	Program 1-1-1	
49	Etching	STS Al etcher		
50	Stripping	Wet Deck	Ultrasonic bath of ACT-CMIS	
51	Deposition	STS PECVD	4 μm of HFSIO	Deposited on heater side
52	Measurement	Nanospec	Thickness measurement	
53	Measurement	Dektak Profilometer	Wafer bow measurement	

Runsheet for silicon microchannels with integrated nickel temperature sensors

Step	Process	Tool	Process details	Comments
54	Deposition	STS PECVD	4 μm of HFSIO	Deposited on sensor side
55	Measurement	Nanospec	Thickness measurement	
56	Measurement	Dektak Profilometer	Wafer bow measurement	
57	Annealing	Furnace 8	17 hours at 435$^{\circ}C$	
58	Measurement	Dektak Profilometer	Wafer bow measurement	
59	Polishing	Presi Polisher	Topography removal	
60	Cleaning	Wet Deck	10:1 solution of DI water to TMAH for 2 mins	Particulate removal
61	Measurement	Nanospec	Thickness measurement	
62	Measurement	Dektak Profilometer	Wafer bow measurement	
63	Cleaning	SSEC wafer scrubber	DI water rinse	
64	Surface Preparation	Plasmatherm	Plasma activation by 2 mins of oxygen plasma	
65	Bonding	Bonding Rig	Contact wafers	Bond processed wafer to another bare wafer

Runsheet for silicon microchannels with integrated nickel temperature sensors

Step	Process	Tool	Process details	Comments
66	Measurement	IR lightsource and camera	Void detection	Separate wafers if void present
67	Measurement	Dektak Profilometer	Wafer bow measurement	
68	Annealing	Furnace 8	17 hours at 435°C	
69	Measurement	Dektak Profilometer	Wafer bow measurement	
70	Coating	3 inch track	Program	Manual dispense of SPR 220-7
71	Photolithography	Karl Suss MA8	Proximity contact w spacers, 45 second exposure	Channel mask
72	Etching	STS ICP etcher	380 μm etching	
73	Ashing	Barrel Asher	Ash until removed	
74	Deposition	STS PECVD	0.1 μm of HFSIO	
75	Measurement	Nanospec	Thickness measurement	
76	Etch	Plasmatherm	Blanket etch 0.1 μm of HFSIO from wafer surface	
77	Cleaning	Wet deck	DI water clean	
78	Bonding	Karl Suss BA8	Recipe: Brunel 2	
79	Dicing	Wafer dicer	Glass dice and silicon dice	

Runsheet for silicon microchannels with integrated nickel temperature sensors

Step	Process	Tool	Process details	Comments
80	Coating	Wet Deck	Manual application of SPR 220-7	
81	Etching	Plasmatherm		
82	Stripping	Wet Deck	Ultrasonic bath of ACT-CMIS	Continue until clear
83	Coating	Wet Deck	Manual application of SPR 220-7	
84	Etching	Plasmatherm		
85	Stripping	Wet Deck	Ultrasonic bath of ACT-CMIS	Continue until clear

Appendix B
List of Publications

B.1 Publications arising from this work

1. D. Bogojevic, K. Sefiane, A. Walton, J. Christy, G. Cummins, and H. Lin, Investigation of Flow Distribution in Microchannels Heat Sinks, *Proceedings of the 10th UK National Heat Transfer Conference*, 2007

2. G. Cummins, H. Lin, and A. Walton, Measurement and optimisation of bond strength for anodic bonding of glass to dielectric thin films, *Proceedings of International Conference on Microelectronic Test Structures*, pp. 111-116, 2008

3. S. Gedupudi, G. Cummins, H. Lin, A. Walton, K. Sefiane, T. Karayiannis, and D. Kenning, Fabrication of Silicon Microchannel With Integrated Heater and Temperature Sensors for Flow Boiling Studies, *ASME Proceedings of First International Conference on Micro/Nanoscale Heat Transfer*, pp. 747-753, 2008,

4. D. Bogojevic, K. Sefiane, A. Walton, H. Lin and G. Cummins, Two-Phase Flow Instabilities in a Silicon Microchannel Heat Sink, *International Journal of Heat and Fluid Flow*, vol. 30, no. 5, pp 854-67, October 2009

5. D. Bogojevic, K. Sefiane, A. Walton, H. Lin and G. Cummins, D. Kenning and T. Karayiannis, Experimental investigation of non-uniform heating on flow boiling instabilities in a microchannels based heat sink, *Proceedings of the 7th International ASME Conference on Nanochannels, Microchannels and Minichannels*, PART A, pp 56-67, 2009

6. D. Bogojevic, K. Sefiane, A. Walton, J. Christy, G. Cummins and H. Lin, Investigation of Flow Distribution in Microchannels Heat Sinks, *Heat Transfer Engineering*, vol. 13, pp 1049-1057, November 2009

7. C. Hutter, D. Kenning, K. Sefiane, T. Karayiannis, H. Lin, G. Cummins, A. Walton, Experimental pool boiling investigations of FC-72 on silicon with artificial cavities and integrated temperature microsensors, *Experimental Thermal and Fluid Science*, vol. 34, no. 4, pp 422-433, May 2010

8. D. Bogojevic, K. Sefiane, A. Walton, H. Lin, G. Cummins. D. Kenning, T. Karayiannis, Experimental investigation of non-uniform heating effect on flow boiling instabilities in a microchannel-based heat sink, *International Journal of Thermal Sciences*, vol. 50, no. 3, pp 309-324, March 2011

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