Sheet Resistance and Electrical Linewidth Test Structures for Semiconductor Process Characterisation

Stewart Smith

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Abstract

Microelectronic test structures are used to characterise and control microfabrication processes. This thesis is primarily concerned with the use of electrical measurement of linewidth and sheet resistance to characterise a wide range of different technologies. These range from advanced interconnect and photolithography techniques to ion-beam induced deposition, MEMS process integration and structures for use as metrology standards.

The thesis first examines the use of the cross-bridge electrical linewidth structure to measure the sheet resistance and critical dimensions of copper damascene interconnect. This was achieved through computer simulation of current flow in the structures and served to highlight the effects of the damascene process on the measurement. As a result layout design rules have been defined which minimise the errors introduced by diffusion barrier layers and dishing.

Mono-crystalline silicon linewidth structures are being developed to meet the requirements for traceable metrology standards. The proposed test structures are fabricated using a wet etch process and have unusual geometries which affect their operation. Computer simulation has shown that the effects of surface interface charge and substrate biasing are the key issues that need to be addressed for accurate extraction of sheet resistance. This work has identified that increased doping of the silicon starting material reduces these effects.

The use of on-mask electrical linewidth structures for alternating aperture phase shifting mask metrology has been investigated. The results compare very favourably, in terms of repeatability, with those obtained using the more common CD-SEM technique. Photolithographic simulation of submicron test structure layouts has been used to investigate the effects of applying optical proximity correction to cross-bridge linewidth structures. The effects of severe asymmetries on the Greek cross sheet resistance structure have also been examined.

Finally the thesis presents examples of process characterisation using resistive test structures. In the first of these examples cross-bridge linewidth structures are used to quantify the effects of a bulk silicon, wet etch solution, which was designed to passivate metal interconnect, on the dimensions of aluminium tracks. This is followed by an investigation of the use of novel sheet resistance test structures to characterise the deposition of platinum in a focused ion beam system. The platinum sheet resistance has been characterised in terms of the main process parameters which facilitates the fabrication of resistive elements of a known value.

Acknowledgements

This thesis is dedicated to my parents. Unfortunately my Father did not get to see it finished but he was always there with encouragement for me in whatever I was doing.

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Acronyms and abbreviations

AFM	Atomic Force Microscope/Microscopy
APS	Ammonium Persulfate
AR	Anti-Reflective
AltPSM	Alternating aperture Phase Shifting Mask
BSE	Back Scattered Electrons
CAD	Computer Aided Design
CD	Critical Dimension
CD-SEM	Critical Dimension Scanning Electron Microscopy
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Planarisation
CVD	Chemical Vapor Deposition
DC	Direct Current
DUT	Device Under Test
ECD	Electrical Critical Dimension
FIB	Focused Ion Beam
FPP	Four Point Probe
HF	Hydrofluoric Acid
HPIB	Hewlett Packard Interface Bus
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
KOH	Potassium Hydroxide
LMIS	Liquid Metal Ion Source
MEEF	Mask Error Enhancement Factor
MEMS	MicroElectroMechanical System
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NA	Numerical Aperture
NIST	National Institute of Standards and Technology
NaOH	Sodium Hydroxide
OPC	Optical Proximity Correction

PSM	Phase Shifting Mask
PVD	Physical Vapor Deposition
RC	Resistor/Capacitor
RIE	Reactive Ion Etch
SE	Secondary Electrons
SEM	Scanning Electron Microscope/Microscopy
SMU	Source/Monitor Unit
SOI	Silicon-On-Insulator
TEM	Transmission Electron Microscope
TMAH	TetraMethyl Ammonium Hydroxide
TWB	TMA/Taurus WorkBench
ULSI	Ultra Large Scale Integration
VLSI	Very Large Scale Integration
VMU	Voltage Monitor Unit
VSU	Voltage Source Unit

"One measures a circle, beginning anywhere."
Charles H. Fort, Lo!, 1931.

Chapter 1
Introduction

This chapter presents a brief examination of the history of microelectronics from the first transistors and integrated circuits to the ever increasing complexity predicted by Moore's law and the associated technology roadmaps. It goes on to introduce the concepts behind the use of microelectronic test structures for process control and characterisation. The chapter ends with a description of the thesis structure and the contents of the chapters that follow.

1.1 Background

The history of microelectronics effectively began with the creation, at the Bell Telephone Laboratories, of the point contact transistor by Bardeen and Brattain in 1947. Around the same time, Shockley developed the theory behind the bipolar junction transistor, though this was not successfully fabricated until 1951 [1]. Similarly the effect of electric fields on the conductivity of semiconductors was demonstrated by Shockley and Pearson in 1948, but it took over ten years before the first Si/SiO_2 MOSFET, which is now so widely used, was demonstrated by Kahng and Atalla [2].

Discrete transistors quickly found applications in hearing aids and transistor radios where their small size and low power consumption made them ideal replacements for thermionic valve technology [3]. However they were not small enough for some applications and the impetus was there for the work, carried out at Texas Instruments by Kilby and at Fairchild Semiconductor by Noyce, which led to the production of the first integrated circuits at the end of the 1950's [4]. Kilby's circuits consisted of transistors fabricated using the mesa technique, where the collector contact is made to the backside of the wafer, and bonded gold wire interconnect. Noyce's ICs more closely resembled present day chips because they used a planar fabrication technique, developed by Hoerni at Fairchild, where oxide masking and diffusion were used to form the transistors [5]. His chip also included interconnect created by photolithographic definition of evaporated aluminium in a process very similar to that used today.

The initial circuits were oscillators and simple digital flip-flops using two or three active devices along with passive elements but by 1971 the technology had advanced to the stage where the first microprocessor, the Intel 4004, was fabricated with 2300 transistors [6]. In 1965 Moore published a paper on the state of the semiconductor industry which predicted that the number of devices in an integrated circuit would double each year [7]. This prediction became known as "Moore's Law" and was revised in 1975 to state that the number of transistors per chip would double every 18 months [8]. More recently the slope has changed again to give a doubling of circuit complexity approximately every two years which leads to the prediction that within the next ten years microprocessors will exist which contain one billion transistors [9].

The increases in integration and chip complexity have come about as a result of the scaling of the transistors, in particular the scaling of the gate length of MOSFETs, and this has driven the advances in technology. More recently however limits been placed on the scaling of interconnect which has encouraged advanced interconnect technologies such as low-κ dielectrics and copper metallisation [10]. The International Technology Roadmap for Semiconductors (ITRS) charts the requirements for future technologies and the most recent release covers the technology nodes extending to 2007 where 65nm interconnect half-pitch lengths are expected with MOS gate lengths approaching 25nm [11, 12]. The increases in complexity have placed a premium on testing for process control and verification and the most recent roadmap focuses heavily on future metrology requirements [13, 14]. Much of the work in this thesis examines similar issues with advanced microfabrication technologies and the effects they have on the use of test structures for the measurement of sheet resistance and electrical linewidth.

1.2 Microelectronic Test Structures

Microelectronic test structures are typically included in Integrated Circuit (IC) designs to enable measurements of process or device parameters for characterisation or process control. There are many different applications, each requiring a different type of test structure, and examples include:

- Process verification and development [15],
- SPICE parameter extraction [16]
- Yield or defect analysis [17]
- Reliability and failure rate analysis [18]
- Matching [19]
- Equipment or material characterisation [20, 21]
- Photomask metrology [22]

Parametric test structures are typically measured electrically using DC measurement methods and appendix A describes the techniques used to make low level resistance measurements.

The major use of test structures is to extract device and process parameters at the end of the production line in order to verify that the process has been successful [23]. If the parametric test results are satisfactory then the product wafer can be passed on for functional testing. If the results do not meet the specifications, for example if the threshold voltages of the MOS transistors fall outside the specified range, then the wafer is scrapped. In this way expensive functional testing is not applied to badly processed wafers. The data obtained from wafers which fail the process verification tests can also be used to identify the source of the problem [24]. For example, wafer maps showing the variation of a parameter across the wafer [25] can be used to determine which process step or piece of equipment is the cause of the failures.

The main problem with the inclusion of test structures is that they take up valuable space on a wafer which could be occupied by product. In the initial stages of process development whole wafers will be covered by test chips as the development engineers attempt to characterise the process. However, in a mature process the wafer will include only the minimum number of structures required for the purposes of process verification. Test patterns can be introduced into a process either as individual structures placed in the scribe channels between the product die or as "drop ins" which are complete test structure chips. Drop in test chips will replace one or more of the product die on the wafer and their use must be traded off against the loss of product.

Scribe channel, or kerf, test structures can be fabricated without a change of mask in a step and repeat photolithography system but the space available is more limited [26]. Figure 1.1 illustrates the use of drop in die and test structures in the scribe channels.

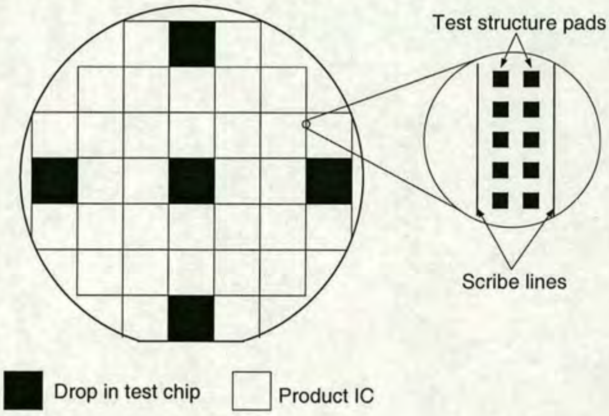


Figure 1.1: *Schematic diagram of a silicon wafer with product and drop in die along with test structures in the scribe channels.*

Electrical test structures are connected to the test equipment through metal pads (typically 80-120μm square) which can be contacted either with manual probe needles moved by micromanipulators or through the use of a probe card. The probe pads are typically arranged in a $2 \times N$ array where the pitch of the pads is twice their width. This arrangement allows a large number of structures to be tested using a probe card with a standardised $2 \times N$ array of probe tips [27]. A test chip layout with this pad arrangement can be seen in figure 1.2.

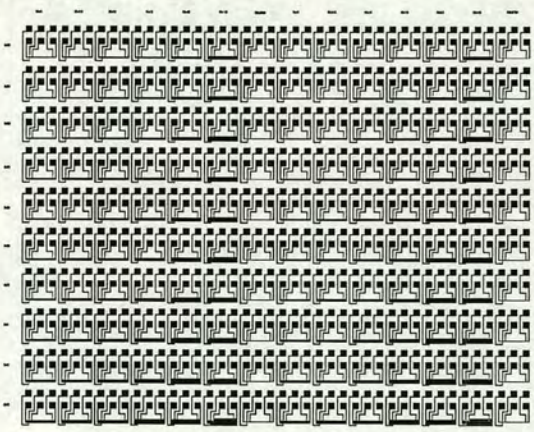


Figure 1.2: *Test chip layout illustrating the* $2 \times N$ *probe pad arrangement.*

Probe cards are generally used with an automatic probe station which can step the probe tips between die on a wafer or between test structures on a chip. This is then integrated with computer controlled measurement equipment to create a completely automated test system.

1.3 Thesis Plan

This section briefly outlines the contents of the chapters which follow. Chapter 2 reviews the literature concerned with test structures and metrology while chapters 3 to 6 investigate a number of novel applications of the sheet resistance and electrical linewidth test structures. Finally, chapter 7 reviews the conclusions made in the previous chapters and suggests possibilities for future work.

Chapter 2: Background. The measurement of sheet resistance and linewidth is described with special attention being paid to the Greek cross and cross-bridge test structures. Examples from the literature of other electrical test structures for the measurement of linewidth and misalignment are also examined.

Chapter 3: Sheet Resistance and Electrical Linewidth Measurement of Copper Damascene Interconnect. This chapter presents the results of 2-D and 3-D computer simulations which model the effects of diffusion barrier layers and CMP induced dishing on the measurement of electrical linewidth in a copper damascene interconnect process. Simulations of Greek and box cross test structures show that the copper damascene process leads to non-uniformities in the sheet resistance and errors in the measurement of linewidth. Suggestions of rules for the layout of these structures which will minimise these errors are presented.

Chapter 4: Test Structures for Use as Linewidth Measurement Standards. This chapter details the need for traceable metrology standards for linewidth measurement before going on to review the previous work on the use of cross-bridge test structures fabricated in mono-crystalline silicon for this purpose. The main part of this chapter describes simulations of silicon test structures which investigate the effects of geometry, fixed surface charge, and substrate biasing on the measurement of sheet resistance.

Chapter 5: Electrical Linewidth Test Structures for Advanced Lithography. The first half of this chapter examines the use of on-mask electrical linewidth test structures for alternating phase shifting mask metrology and presents the results of electrical and SEM measurements made on such a mask. The second part simulates the photolithographic process in order to examine the effects of applying optical proximity correction to cross-bridge test structure layouts. This section also presents the results of simulations of Greek cross structure with very large asymmetries.

Chapter 6: Examples of Process Characterisation Using Resistive Test Structures. Two examples of the manner in which sheet resistance and electrical linewidth structures can be used to characterise microfabrication processes are presented in this chapter. In the first of these, cross-bridge linewidth structures are used to assess the effect of a TMAH based, bulk silicon wet etch solution on aluminium interconnect. The second example presents a methodology for the characterisation of the sheet resistance of platinum deposited by a focused ion beam system. This enables the deposition of metal straps with a known resistance for circuit modification.

Chapter 7: Conclusions and Future Work In this chapter the conclusions drawn from the work reported in the preceding chapters are reviewed. Suggestions for future work on the topics covered in this thesis are also made.

Chapter 2
Background

2.1 Sheet Resistance Measurement

2.1.1 Resistivity

Resistivity is probably the most basic parameter for a conductor or semiconductor material and it is denoted by the symbol ρ with units of Ω-m. A bar of conducting material with uniform resistivity ρ is shown in figure 2.1 and the resistance between the electrodes is given by

$$R = \frac{\rho l}{wd} \tag{2.1}$$

where l is the length of the conducting bar while w and d are the width and thickness respectively.

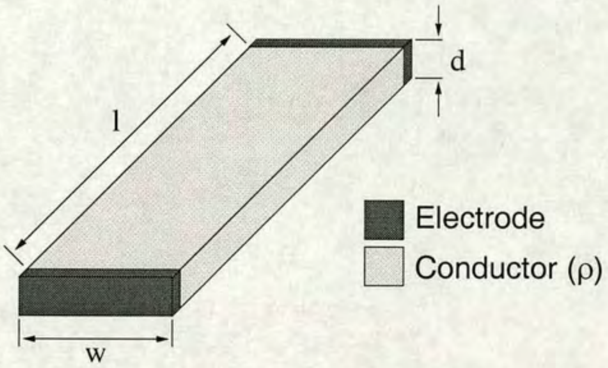


Figure 2.1: *Schematic diagram illustrating the dimensions of a simple bar of conducting material*

One of the most common techniques used to measure resistivity is the four-point probe (FPP) method where four point contacts are made to the surface of the material being measured [28]. The probe tips are generally arranged in a straight line with an equal spacing s as shown in figure 2.2.

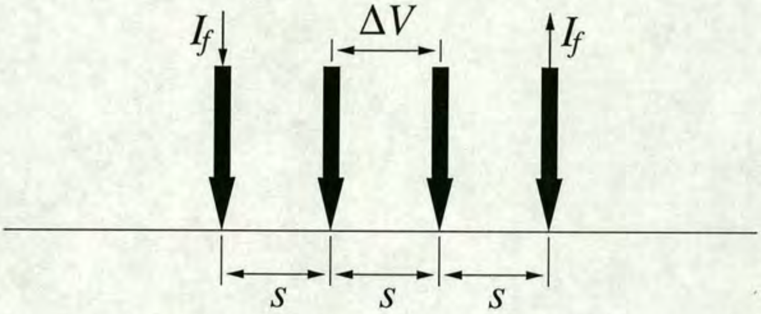


Figure 2.2: *In-line four-point probe measurement setup*

A current I_f is forced between the two outer probes and the potential difference ΔV between the two inner probes is measured. Typical values for the tip spacing range from 0.5 to 1.5mm. If the sample being measured can be considered semi-infinite (i.e. the thickness, width and length of the sample are each much greater than the tap spacing) then the resistivity can be calculated using [29]

$$\rho = 2\pi s \left\{ \frac{\Delta V}{I_f} \right\} \tag{2.2}$$

However, this technique is commonly used to measure samples which are not semi-infinite and in that case a correction factor F is added to the equation to correct for the sample geometry [28, 30, 31].

2.1.2 Sheet Resistance

Most applications of the four-point probe technique for testing materials in a microfabrication environment represent a special case where the thickness t of the conducting material is much less than the tap spacing. In this case, the equation for resistivity can be reduced to

$$\rho = \frac{\pi t}{\ln(2)} \frac{\Delta V}{I_f} \approx 4.532t \frac{\Delta V}{I_f} \tag{2.3}$$

For example, this will apply to wafers coated with a thin film of aluminium or a diffused or implanted conducting layer at the surface. Because of the difficulty in measuring the thickness of such a conducting layer they are often characterised by their sheet resistance R_S which is expressed in units of ohms per square. The sheet resistance is calculated from four-point probe measurements as

$$R_S = \frac{\rho}{t} = \frac{\pi}{\ln(2)} \frac{\Delta V}{I_f} \tag{2.4}$$

The sheet resistance represents the resistance of a square area of conducting film (i.e. $w = l$). The resistance of a bar (as shown in figure 2.1) of this material can then be found by multiplying the sheet resistance by l/w. The sheet resistance of a sample which has a non-semi-infinite geometry can be found using the generic formula

$$R_S = k \frac{\Delta V}{I_f} \tag{2.5}$$

where k is a correction factor which depends on the shape of the sample and the positioning of the probe tips [31].

The four-point probe technique is typically only useful with large uniform samples where the correction factors for the geometry and probe positions of each measurement are well known. This requires large unpatterned areas which may be undesirable in a microfabrication process. However, it has recently been demonstrated that the sheet resistance can be extracted from a small area of silicon film by reconciling the electrical measurements with the results of computer simulations of similar test geometries [32].

2.1.3 Van der Pauw Structures

A more practical method of measuring the sheet resistance of a thin film, given that the sample is too small for the FPP technique, is to use a van der Pauw type test structure. Van der Pauw developed a method for measuring the resistivity (or sheet resistance) of an arbitrary shaped thin film sample with four contacts along the sample boundary [33, 34]. The method requires that the contacts be small, tending towards point contacts, and the sample material be homogeneous in thickness and resistivity. If the sample is as illustrated in figure 2.3 with contacts A, B, C and D then $R_{(AB,CD)}$ is defined as

$$R_{(AB,CD)} = \frac{V_D - V_C}{I_{AB}} \tag{2.6}$$

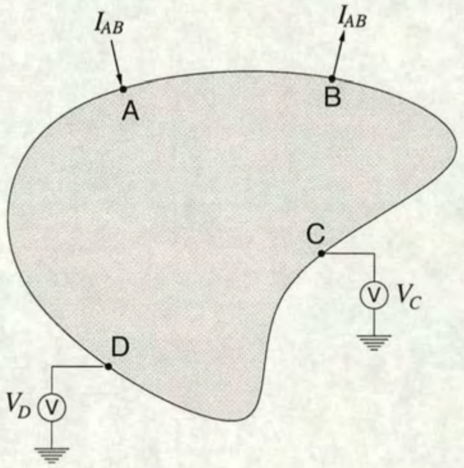


Figure 2.3: *Van der Pauw resistivity test structure with arbitrary shape and contact placement.*

It should be noted that "V_X" is the voltage, relative to ground, measured at contact "X" whereas "I_{XY}" refers to conventional current forced in terminal "X" and out of terminal "Y". This notation is used from now on in this thesis. If $R_{(BC,DA)}$ is defined similarly then

$$\exp(-R_{(AB,CD)}\frac{\pi t}{\rho}) + \exp(-R_{(BC,DA)}\frac{\pi t}{\rho}) = 1 \tag{2.7}$$

which can be solved numerically to find ρ.

If the sample has 90° rotational symmetry and the contacts are equally spaced around the boundary then $R_{(AB,CD)} = R_{(BC,DA)}$ and the formula reduces to

$$\rho = \frac{\pi t}{\ln(2)} R_{(AB,CD)} \tag{2.8}$$

This is similar to equation (2.3) for the resistivity extracted with a four-point probe technique and can of course be changed to an expression for sheet resistance by dividing both sides by t as in (2.4).

Using equation (2.8) as a starting point is is possible to derive an alternative form of the general van der Pauw formula (2.7)

$$\rho = \frac{\pi t}{\ln(2)} \frac{R_{(AB,CD)} + R_{(BC,DA)}}{2} f \tag{2.9}$$

where f is a correction factor which is a function of the ratio $r = R_{(AB,CD)}/R_{(BC,DA)}$ and can be found by numerical solution of

$$\cosh\left\{\frac{r-1}{r+1}\frac{\ln(2)}{f}\right\} = \frac{1}{2}\exp\left\{\frac{\ln(2)}{f}\right\} \tag{2.10}$$

2.1.4 Greek Cross Structures

One of the main sources of error in van der Pauw measurements is that the contacts are non-ideal and have a finite size [35]. Van der Pauw found that the effect can be reduced by using a “clover leaf” shaped sample as shown in figure 2.4.

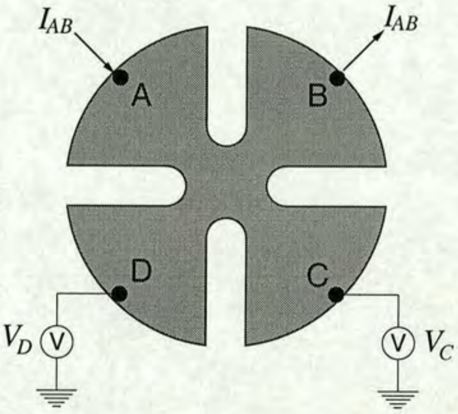


Figure 2.4: *Van der Pauw resistivity test structure with clover leaf shape to reduce the error caused by non-ideal contacts*

These measurement techniques and structures were developed for the measurement of the resistivity of large discrete samples of semiconductor materials. The next development in this field was the evolution of structures which could be made using standard microfabrication techniques, and on the same scale as microelectronic devices, in order to measure the sheet resistance of thin films or diffused layers. The Greek cross sheet resistor is a special case of the four-terminal van der Pauw structure which meets these requirements [36–38]. The layout of such a structure is illustrated in figure 2.5.

References [36] and [38] describe methods for the numerical analysis of the geometry of such a structure. It has been demonstrated that the sheet resistance error is dependent on the ratio of the arm length L to the arm width W. Provided that $L/W \geq 1$ the error will be less than 1% but generally the standards documents for these structures

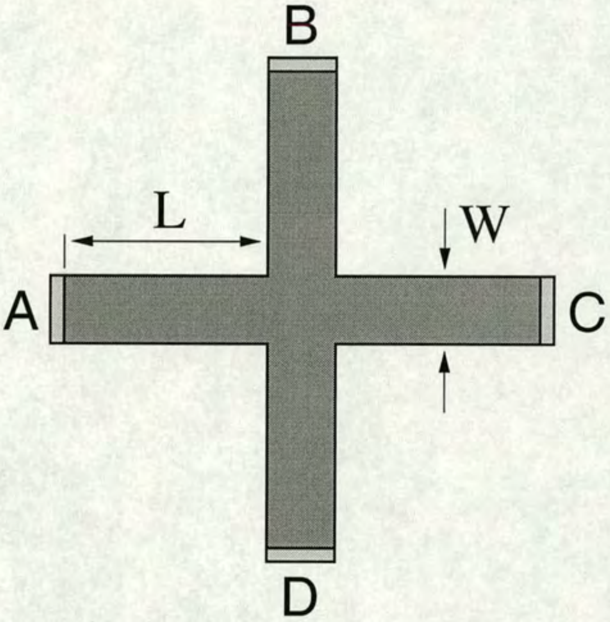


Figure 2.5: *Greek cross four-terminal sheet resistance test structure.*

recommend that $L \geq 2W$ [39, 40].

Initial experimental results for these structures were published in reference [37]. Although extraction of sheet resistance from an ideal structure would only need one resistance measurement in practice four measurements are required, two at the "zero-degree" measurement position

$$R_0(+I) = \frac{V_D - V_C}{I_{AB}} \tag{2.11}$$

$$R_0(-I) = \frac{V_C - V_D}{I_{BA}} \tag{2.12}$$

and two at the "ninety-degree" orientation

$$R_{90}(+I) = \frac{V_C - V_B}{I_{DA}} \tag{2.13}$$

$$R_{90}(-I) = \frac{V_B - V_C}{I_{AD}} \tag{2.14}$$

These results are averaged together to get $R(\pm I)$ which is used to calculate the sheet resistance with

$$R_S = f\left\{\frac{\pi R(\pm I)}{\ln(2)}\right\} \tag{2.15}$$

As in equation (2.9) f is a correction factor for asymmetry in the structure and is calculated using (2.10) where

$$r = \frac{R_0(+I) + R_0(-I)}{R_{90}(+I) + R_{90}(-I)} \tag{2.16}$$

The asymmetry is quantified in reference [37] with the asymmetry factor F_A which can be calculated from r using

$$F_A = 2\frac{r-1}{r+1} \tag{2.17}$$

The paper also compares values of F_A and the corresponding correction factor f, showing that for $F_A \leq 10.74\%$ (0.1074) the correction required $(1 - f)$ will be less than 0.1% of the uncorrected value, effectively reducing the equation for sheet resistance to

$$R_S = \frac{\pi R}{\ln(2)} \tag{2.18}$$

where R is the average resistance denoted $R(\pm I)$ above.

The reason for taking two measurements at each orientation with the current directions reversed is that it will highlight any measurement offsets in the test equipment (see section A.1). The zero offset factor F_0 is defined as

$$F_0 = \frac{(|R_0(+I) - R_0(-I)| + |R_{90}(+I) - R_{90}(-I)|)}{2R(\pm I)} \tag{2.19}$$

Small values of F_0 indicate that the measurement is not greatly affected by offset voltages in the test system being used.

It is interesting with such a structure to look more closely at what is actually occurring during the measurement and this can be done through computer simulation and visualisation. A Greek cross structure with $W = 1\mu$m and $L = 2\mu$m has been simulated in two dimensions using the interconnect simulation package Raphael (see section A.3.2). The structure is divided up into a grid and the potential difference and current are calculated for each node in the grid as part of the simulation. Figure 2.6 shows the results of plotting contours of equal potential in a simulated Greek cross structure. The structure is being measured by forcing a current between terminals A and B, and measuring the voltages at C and D.

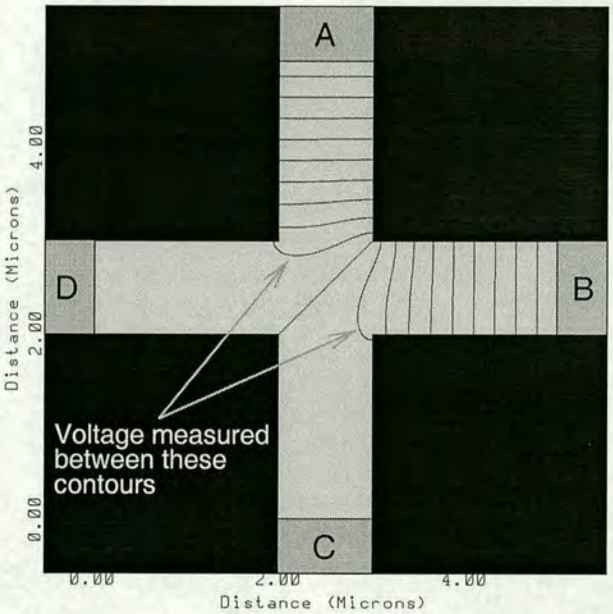


Figure 2.6: *Equipotential contours in a Greek cross structure. The contour spacing is 50mV, running from 1V at terminal A to 0V at terminal B*

This shows that the potentials being sensed at terminals C and D are the same as those found in the internal corner of the cross between the force terminals A and B. The result of this is that the Greek cross structure measures the sheet resistance of this small area of the conducting film and will be affected by any short range non-uniformities of resistivity. Interconnect materials such as polysilicon, aluminium and copper have a grain structure and the material resistivity can vary from grain to grain. Reference [41] presents the results of simulations of the effects of grain structure on a number of different cross geometries. It was found that the variability of the value of R_S extracted from a Greek cross increases as the size of the cross, and therefore the area where the measurement occurs, decreases towards the grain size. A similar effect can be achieved by altering the geometry of the structure to give a box or quadrate cross [36] as this again increases the area over which the measurement is made. Figure 2.7 shows the voltage contours observed in a simulated box cross structure. It is clear that the voltage is being sensed over a much larger area and will provide an average value of sheet resistance for the box section of the cross.

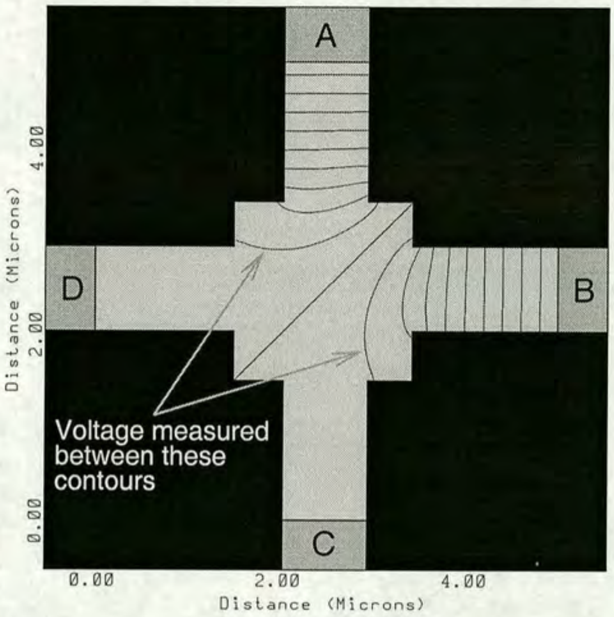
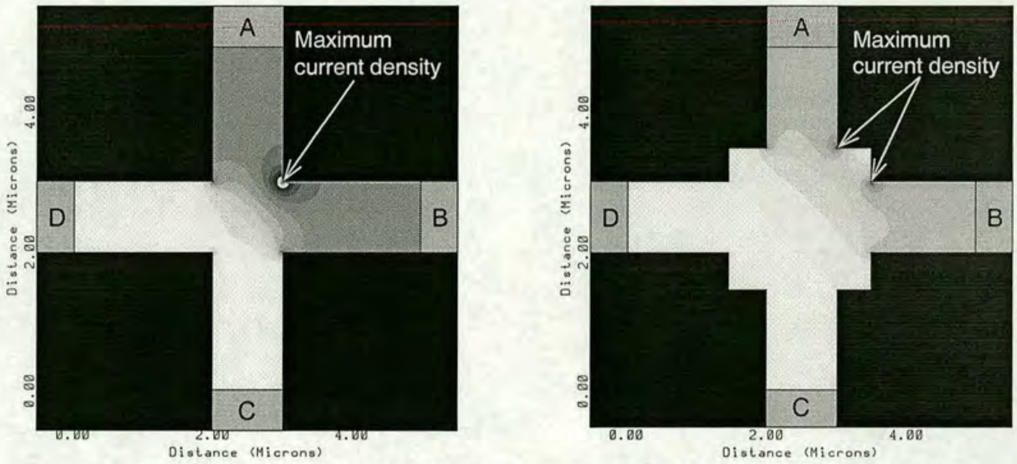


Figure 2.7: *Equipotential contours in a box cross structure. The contour spacing is 50mV, running from 1V at terminal A to 0V at terminal B*

A further issue with these structures is current crowding which can occur in the internal corner between the forced terminals of a small Greek cross. The scalar values of current at each node in a simulated structure can be plotted as contours in the same way as the potential. The current density is highest where the voltage contours were closest together as can be seen for both a Greek and a box cross structure in figure 2.8.

In both structures the highest currents are observed at the the internal corners between the forced terminals. If the current density in these areas becomes high enough this can affect the measurement especially in a Greek cross where the voltage is actually being measured in this area of maximum current. High currents in narrow armed crosses can also lead to joule heating which will change the resistance of the conducting film [42, 43]. Reference [44] presents results showing that there is an optimum value of current which gives the highest measurement repeatability. If it is too low the resolution of the voltmeter will limit the accuracy whereas too high a current will tend to cause the effects which have been discussed above. Therefore it is important that the correct test structure and measurement strategy are chosen for each application or process.

Greek cross structures and variants such as the box cross are widely used in the



(a) Contours of current for a Greek cross structure.

(b) Contours of current for a box cross structure.

Figure 2.8: *Simulated measurements of cross type sheet resistance structures. Current is forced between A and B, and the voltage is measured at C and D.*

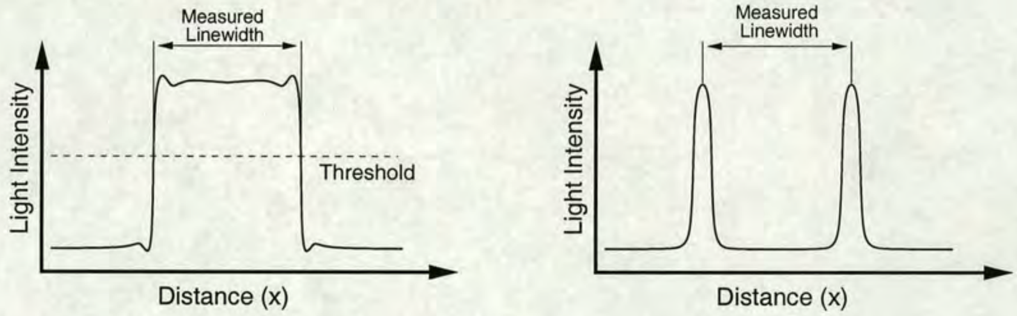
characterisation of thin film sheet resistances. In particular, they are an integral part of the structures used to measure electrical linewidth, as described in the next section [45, 46]. The small size and the fact that no dimensional information is required for the measurement means that cross type sheet resistance structures have been widely used for a range of different applications [20, 47–54]. Adaptions to the structure have also allowed the measurement of vertical sheet resistance for layer thickness measurements [55, 56] and, more recently, the *thermal* sheet resistance of materials used in microsystems fabrication [57]

2.2 Linewidth Measurement

The measurement of linewidth or Critical Dimension (CD) is essential for the characterisation and control of lithographic and etching processes in microfabrication. There are four main methods of measuring linewidth; optical, scanning electron or scanning probe microscopy, and electrical measurement. This section will look at each in turn but will focus mainly on electrical linewidth measurements as these form a large part of the body of work presented in this thesis.

2.2.1 Optical Linewidth Metrology

There are a number of different methods for optical CD measurement. In a *video scan* system an image of the feature being measured is obtained using a digital video camera connected to a microscope. This image is manipulated to provide a profile of the intensity of reflected light across the feature from which a value of the linewidth can be extracted. A similar profile is produced by a *slit scan* system where the sample is illuminated through a narrow slit which is stepped across the feature. The reflected light intensity is measured by a photodetector and plotted against the slit position. In both these cases the linewidth is measured by applying a threshold which defines the line edges as illustrated in figure 2.9(a). *Laser scanning* is a further method for optical CD measurement where the beam from a laser is scanned across the sample and scatters off the line edges producing an intensity signal in a photodetector mounted alongside the microscope objective. This system produces an intensity profile with two peaks at the line edges as is shown in figure 2.9(b).



(a) Optical CD measured by applying a threshold to a light intensity profile

(b) Optical linewidth measurement in a laser scan system.

Figure 2.9: *Light intensity profiles produced by different optical metrology systems illustrating measurement techniques.*

Optical measurement of linewidth is becoming less useful as feature sizes reduce because it is limited by the wavelength of the light being used. However, it is still the first choice for metrology on large features and there are developments using deep ultra-violet light sources or near-field microscopy which could lead to it being used in sub-micron process control [13, 58]. In addition there are methods which use the scattering of laser light from diffraction gratings [59] and from digital holograms [60–62] to measure the dimensions of the features which make up the diffractive structures. This can enable a measurement resolution well below the wavelength of the light being used.

2.2.2 Scanning Probe Microscopy

Scanning probe microscopy covers a range of different systems but the most common is the Atomic Force Microscope (AFM) because, unlike the scanning tunnelling microscope, it can be used to image both conducting and insulating surfaces.[63, 64] The AFM consists of a micromachined probe tip suspended on a cantilever and a measurement system which can detect the vertical position of the probe. When the tip is brought into close proximity to the sample surface it experiences van der Waals forces and the cantilever is deflected. The distance between the probe and the surface determines the direction of the force. In *contact mode* the tip is close enough to be repelled from the surface while in *non-contact* mode the separation is greater and the force is attractive. The forces are generally greater and therefore easier to measure in contact mode but the tip or the sample can be damaged if they are too great. A third mode of operation is intermittent contact or *tapping mode* where the cantilever is driven to vibrate at its resonant frequency and the tip is tapped across the surface. This is less likely to damage the surface than contact mode and is capable of resolving a greater range of surface topography than the non-contact mode [65].

The shape of the profile returned by the AFM is affected by the shape of the probe tip used as is shown in figure 2.10 [66].

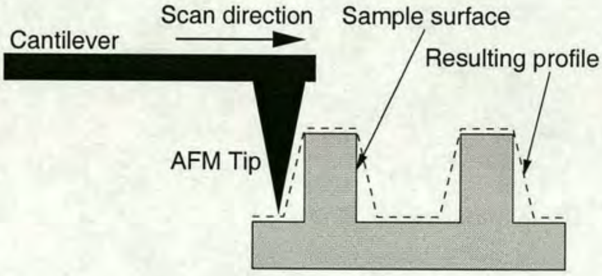
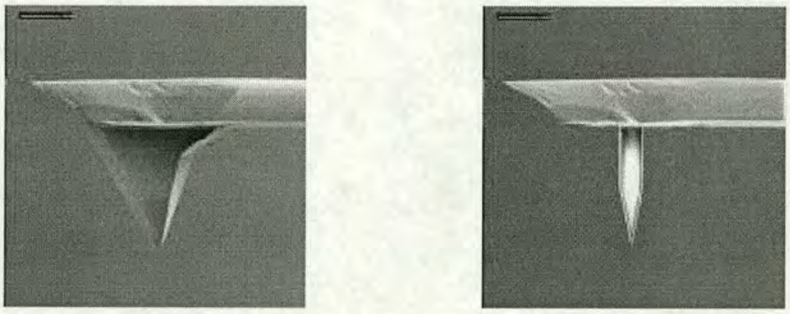


Figure 2.10: *Schematic diagram illustrating atomic force microscopy and showing the effect of probe shape on the profile which is produced.*

The use of an AFM for metrology of high aspect ratio, microfabricated features is made difficult by these interactions between tip and sample. The effect can be lessened by focused ion beam milling of a standard tip to produce a sharpened probe as in reference [67]. This sharpening will allow the imaging of high aspect ratio features but the shape of the probe will still affect the profile of feature edges and for that reason it is desirable to be able to measure the tip shape. Reference [68] describes the use of polysilicon features with undercut sidewalls to extract the tip shape. It was found that the same attractive forces which allow the non-contact AFM mode can cause a slender probe tip to bend towards the side of a feature affecting this measurement. Therefore the sharpened tip should quickly widen to a thicker, stiffer section. An example of focused ion beam sharpening of a silicon AFM probe tip can be seen in figure 2.11.



(a) Before sharpening. **(b)** After sharpening.

Figure 2.11: *SEM images of micromachined silicon AFM probe tips before and after focused ion beam sharpening.*

Although the resolution of an AFM system can reach the atomic scale with the right tip, performing a measurement is very slow. For this reason it is not a good choice in process control settings where large numbers of measurements are required.

2.2.3 CD-SEM

A scanning electron microscope uses a focused beam of electrons to produce an image of a sample surface [69]. The first stage in an SEM column is the electron gun which consists of an electron source (cathode) and a pair of electrodes (grid and anode) which extract and accelerate the electrons. The electron source was originally a thermionic cathode, like that found in a cathode ray tube display, but many modern SEM systems now use field emission arrays [70]. The beam then passes through one or two sets of electron lenses and apertures which condense the beam and control the incident beam current. In the final stage a set of scan coils deflect the beam to scan it in a raster pattern across the sample and a final objective electron lens focuses the electrons to a spot on the sample surface. The layout of a typical SEM column is shown in figure 2.12.

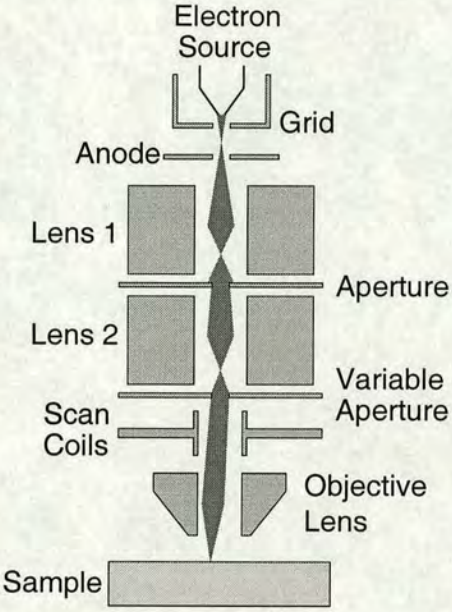


Figure 2.12: *Schematic cross section through a standard SEM column showing the important elements.*

When the beam hits the sample surface it produces secondary electrons (SE) and back scattered electrons (BSE). The low energy secondary electrons are detected by a collector in the side of the sample chamber while the high energy back scattered electrons require a group of detectors arranged around the objective aperture. These detectors produce separate signals proportionate to the amount of SE or BSE produced by the interaction between the electron beam and the sample. These signals, along the raster signal being used to drive the scan electrodes, are used to produce the image of the sample surface. A different image will be obtained depending on whether it is the SE or BSE signal that is used to produce it.

Linewidth measurement with an SEM is similar to the optical techniques previously discussed in that an intensity profile across the feature being measured is extracted from an image and this is analysed to provide a value of CD. However it is considerably more complicated because the SEM image contrast is not only dependent on the material being scanned - so that a metal line, for example, appears brighter than surrounding oxide - but also on the topography of the surface. Line edges show up brightly in an SE image and can lead to uncertainty in resolving the line edge. An example of this effect can be seen in figure 2.13 which shows a CD-SEM image of a chrome line on a quartz mask. Reference [71] describes the differences between SE and BSE images used for CD measurement. BSE measurements do not display the same peaks at the edge of the features and the linewidth returned is slightly lower than the SE results. In addition this paper suggests that the precision of BSE measurements is higher than those made on SE images. The extraction of linewidth from the intensity profiles is very similar to the optical methods where a threshold is applied to the measurement results.

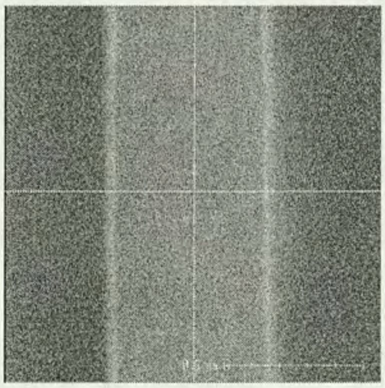


Figure 2.13: *SEM micrograph of a chrome track with a nominal width of 0.7μm showing increased brightness at line edges.*

There are a number of problems with SEM linewidth measurements. The electron beam scan can cause contamination of the sample, in particular causing carbon to be deposited over the area being imaged which can increase the effective linewidth. This is a particular problem in photomask metrology where it could have severe effects on the usefulness of the mask [72]. The second major problem with SEM metrology is charging of insulating samples which leads to problems with measurement repeatability [22]. It is possible however to lessen these effects through the use of a automated control system such as that described in reference [73]. This method served to reduce the 3σ repeatability to about 10nm over 20 repetitions of the measurement. Regardless of these problems CD-SEM metrology is typically the first choice for sub-micron, photolithographic process control because it can be used to measure developed photoresist before any further processing occurs [74].

2.2.4 Electrical Linewidth Measurement

Electrical measurement of linewidth differs fundamentally from the other measurement techniques described above in that the attribute being measured is the conducting width of the feature rather than the physical width. Hence, this method is limited to the measurement of conducting features but if it is being used for interconnect metrology the effective electrical width of the track is the most important parameter. The standard method for the measurement of Electrical CD (ECD) uses a test structure known as the cross-bridge sheet resistor which is a combination of a Greek or box cross and a four-terminal bridge resistor [45, 46, 75–80]. A schematic diagram of such a structure is shown in figure 2.14.

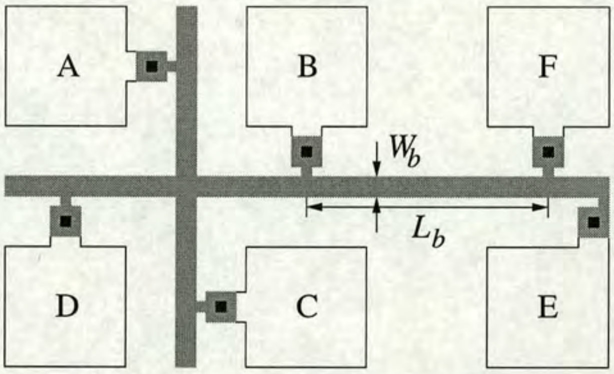


Figure 2.14: *Schematic diagram of a cross-bridge electrical linewidth test structure*

The electrical width W_b of the bridge resistor section between terminals B and F is

$$W_b = \frac{R_S L_b}{R_b} \tag{2.20}$$

where L_b is the length of the bridge in figure 2.14 and R_S is the sheet resistance of the material which is extracted using the Greek cross section as in section 2.1.4. In order to measure the bridge resistance R_b a current I_{DE} is forced between terminals D and E and the voltage V_{BF} measured between terminals B and F. As with the cross measurements described previously, the measurement is repeated with the current reversed and the average resistance calculated using

$$R_b = \frac{[V_{BF} + V_{FB}]}{[I_{ED} + I_{DE}]} \tag{2.21}$$

The resulting value of W_b from equation (2.20) is the average value of the conductive width of the bridge section.

There are a number of assumptions made in these calculations. First of all it is assumed that the value of sheet resistance extracted from the Greek cross applies to the whole of the structure. It should be noted that any error in the sheet resistance (R_S) in equation (2.20) will be directly translated into an error in the linewidth. In other words the accuracy of the sheet resistance measurements must be the same or better than that required from the linewidth measurement. This may be limited by the resolution of the voltmeter used in the Greek cross measurement [43]. In addition to these problems certain processes such as copper damascene interconnect fabrication can lead to non-uniformities in the thickness, and therefore the sheet resistance, of the features leading to errors in the measurements [81].

The second assumption is that the length of the bridge section L_b is the designed length between the centres of the voltage taps. However this is complicated by the effect of the taps which effectively widen the bridge and lead to an over-estimation of the value of linewidth [82–84]. The effect of this tap induced error can be minimised, so that no correction is required, by following design rules for the dimensions of the structure [39, 40]. The design rules are as follows:

$$\begin{aligned} L_b &> 150\mu\text{m} \\ L_b &> 20W_b \\ W_b &\geq W_t \end{aligned}$$

where L_b,W_b and W_t are the important bridge dimensions shown in figure 2.15

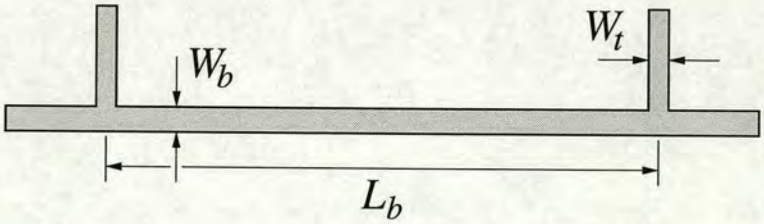


Figure 2.15: *Schematic diagram of a bridge resistor showing the important dimensions.*

2.2.4.1 Accounting for Finite Tap Width Effects

In certain processes the design constraints on the structure layout given above may be undesirable. For example, if the uniformity of the sheet resistance cannot be guaranteed then the length of the bridge may have to be shorter than the design rules. Reference [83] describes a modified test structure which can measure the effect of the voltage taps and correct for them in the measurement of a short bridge section. Figure 2.16 shows the layout of such a structure.

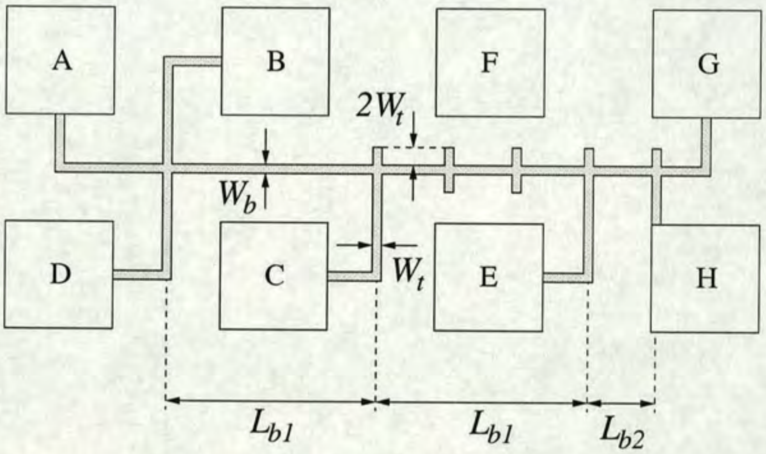


Figure 2.16: *Linewidth test structure which allows the extraction of the effect of the voltage taps on the measurement of the bridge section L_{b2}.*

The bridge sections of length L_{b1} can be used to extract the effective change in the length of the line (δL) caused by a voltage tap. The effective length of the short bridge section is then $L_e = L_{b2} - \delta L$ and the equation for linewidth becomes

$$W_{b2} = \frac{R_S L_e}{R_{b2}} \tag{2.22}$$

2.2.4.2 Proximity Effects

The proximity of features in a lithographic process has a significant effect on the printed size of those features. Cross-bridge linewidth structures with arrays of dummy features surrounding the measured bridge section can be used to show that the ECD increases as the separation of the dummy tracks decreases [22]. A similar structure intended for use in the characterisation of proximity effects in electron beam lithography can be seen in figure 2.17 [85].

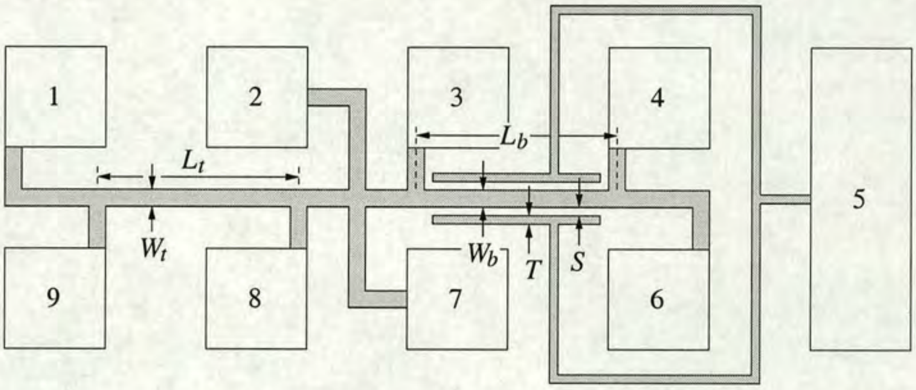


Figure 2.17: *Layout of a test structure used to investigate proximity effects on linewidth.*

The sheet resistance of the material is measured using the Greek cross at the centre of the structure. The widths of the simple bridge structure (W_t) and the structure with the dummy bars (W_b) can then be measured as in the standard cross-bridge and the proximity induced change in linewidth ΔW is calculated using

$$\Delta W = W_b - W_t \tag{2.23}$$

The results obtained from this structure showed that ΔW varied from 0.11 to 0.58 μm as the dummy bar spacing S was decreased from 3 to 1.5 μm. Other test structures for the measurement of proximity using a modified cross-bridge can be found in references [85–88]

2.2.4.3 Line Spacing and Pitch Measurement

Another of the many possible variations on the cross-bridge linewidth structure is the split-cross-bridge resistor which can be used to measure the spacing between narrow lines in addition to measuring sheet resistance and linewidth. The layout of such a structure can be seen in figure 2.18 [82].

This structure has two bridge sections of length L_b and L_s, the first of these has the width $W_b = 2W + S$. The second bridge is split into two channels of width W and the effective conducting width is $W_s = 2W$. Once both sections have been measured electrically the spacing S between the lines in the split bridge can be calculated as $S = W_b - W_s$. Finally the pitch of the split bridge tracks can be calculated as $P = W + S$. This

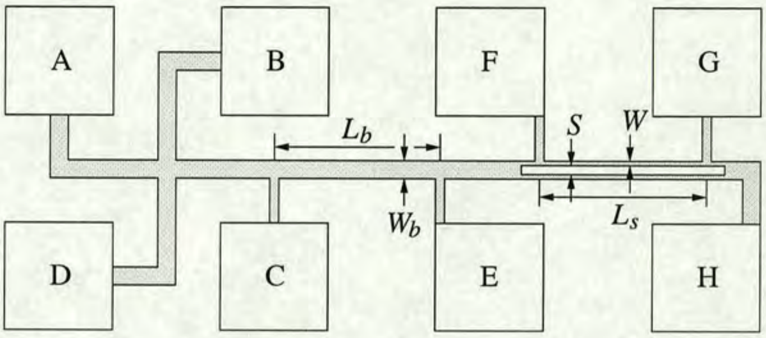


Figure 2.18: *Split-cross-bridge test structure which can be used to measure R_S, W_b, W and S.*

can then be compared with the drawn pitch from the mask used to print the structure. These figures should be identical (taking the magnification of the lithography system into account) and so this can be used to confirm the electrical measurements.

2.2.5 Comparison of CD Measurement Techniques

It is interesting to compare the different measurement techniques used to extract linewidth and there are a number of sources in the literature which do this. Reference [89] compares the results obtained by measuring the same structures in three different way: by optical metrology, by extracting the ECD and using a CD-SEM system. The optical system used the slit scan technique and was found to have a measurement uncertainty of about 65 nm which is more than 15% of the narrowest feature size measured (0.4μm). The ECD measurements have a very good repeatability with the standard deviation of a set of measurements made on a single structure being less than 1nm. However, the total uncertainty must take into account possible errors in R_S and the bridge length as described above. This means that the electrical linewidth results have a possible error of about 0.007μm on a 0.5μm line. This paper did not present an estimation of the uncertainty in the SEM measurements but the precision of the system is about 5nm at a magnification of 100,000×. This paper also compares the differences in linewidth extracted from each system. The results from the optical and SEM measurements agree very well and show a difference of about 10-12 nm. There are significant differences between the optical/SEM results and those extracted electrically. The differences here are about 80-90nm. This is to be expected as the electrical technique does not measure the physical width of the feature. Instead it extracts the average conducting width of the track. This concept is examined in more detail in chapter 4 which looks at the use of standards to calibrate dimensional measurements.

Reference [90] also compares optical and electrical measurements and finds an offset of 65-90nm depending on the structure material. Reference [91] emphasises the short term repeatability and long term stability of ECD measurements and demonstrates the high level of correlation between them and results obtained from a CD-SEM. Reference [44] looks at measurements made on single crystal silicon test structures (which again are covered in chapter 4) using electrical, SEM and AFM metrology. In this case it was found that there was an offset in the opposite direction where the electrical results showed the structures to be wider than the physical measurements. However, the authors suggest that this may be due to an error in the extraction of sheet resistance.

2.3 Other Resistive Electrical Test Structures

There are a number of test structure types which are either based on the four terminal resistive structures examined in this section or are measured in a similar way. This section will briefly describe some of these structures and explain their use.

2.3.1 The Fallon Ladder

The Fallon ladder structure is an alternative way to measure the minimum printable dimensions in a photolithographic process. It has advantages over the cross bridge linewidth structure because it does not need high resolution test equipment to make the measurement [92]. The layout of a Fallon ladder structure is illustrated in figure 2.19.

The minimum value of resolved linewidth can be extracted either by optical examination of the structure or through electrical measurement of the structure. The resistance of the structure is measured by forcing a current in one end of the ladder and out the other end as in the figure. The voltages (V_1 and V_2) at either end of the structure are measured and the total resistance calculated. The value of the resistance

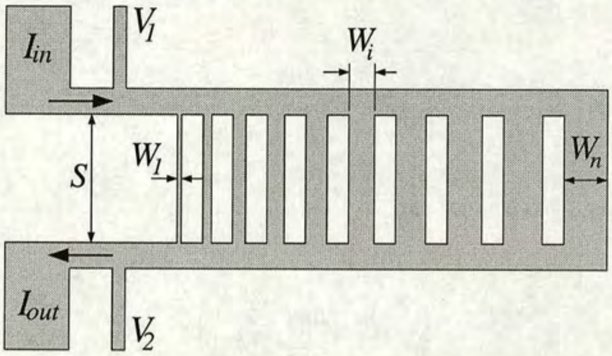


Figure 2.19: *Schematic layout of a Fallon ladder structure.*

will depend on how many of the rungs of the ladder have been successfully printed. The addition or removal of a rung of the ladder will cause an incremental change in the resistance of the ladder. The results presented in reference [92] showed that it could be used to extract the minimum resolvable linewidth in terms of the stepper focus used to print the structures. The results were confirmed by examination of the ladder in an SEM.

2.3.2 Alignment Test Structures

There are a number of test structures which can be used to measure errors in the alignment between successive layers in a process. Figure 2.20 shows an eight terminal structure based on the van der Pauw sheet resistance structure which can be used to simultaneously extract misregistration in X and in Y between two masking layers [93, 94].

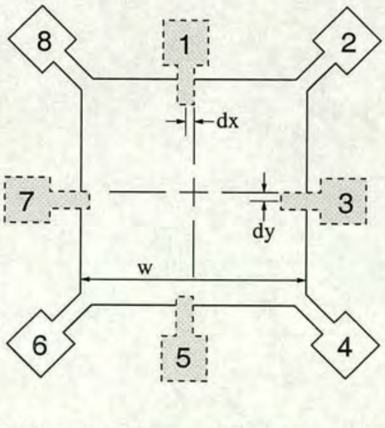


Figure 2.20: *Schematic layout of an eight terminal alignment test structure.*

The first mask is used to print the square body of the structure and the arms numbered 2,4,6 and 8. In the original paper this was a window etched into oxide over a silicon wafer. The second mask opens up similar windows to form the other 4 contacts to the structure (contacts 1,3,5 and 7). The result is an opening through oxide representing the combination of the two masks and this can be ion implanted to create a conducting test structure. Finally the arms will have metal pads deposited over them to make probeable contacts. The misalignment between the two masks in X is d_x and in Y is d_y. Through electrical measurement of the structure these figures can be extracted using [66]

$$d_x = 0.316w\arcsin(\gamma_x); \quad \gamma_x = \tfrac{V_{65}/I_{82} - V_{54}/I_{82}}{V_{65}/I_{82} + V_{54}/I_{82}} \tag{2.24}$$

$$d_y = 0.316w\arcsin(\gamma_y); \quad \gamma_y = \tfrac{V_{43}/I_{68} - V_{32}/I_{68}}{V_{43}/I_{68} + V_{32}/I_{68}} \tag{2.25}$$

where w is the width of the box section of the structure. The original paper states that the accuracy of the measurements made with this method is $\pm 0.1\mu$m. It is also possible that this structure could be used to measure misalignment between an implant or diffusion and the first layer of metallisation in a process. The first mask would be used to open the area for doping and the second would define the areas of metal. Reference [95] describes the application of this structure to the measurement of misalignment between different layers in a standard MOS process. It shows that the measurement error is about 10% when extracting a misalignment of 0.1μm. The conclusion of this paper is that the structure is capable of providing accurate mask registration measurements in a VLSI process.

There are a wide range of other structures which can be used to measure feature placement through electrical measurements. The differential linewidth bridge structure is fabricated in a single layer of conducting film and measures the overlay between two photomasks. The final structure is illustrated in figure 2.21 along with the two mask layouts used to print it [48, 77, 96].

This structure can be used to find the alignment error ΔW by calculating the difference between the widths (W_1 and W_2) of the two bridge structures. The measurements are performed in the same way as for a bridge linewidth structure by forcing a current between the terminals at either end and measuring the voltages at the other two

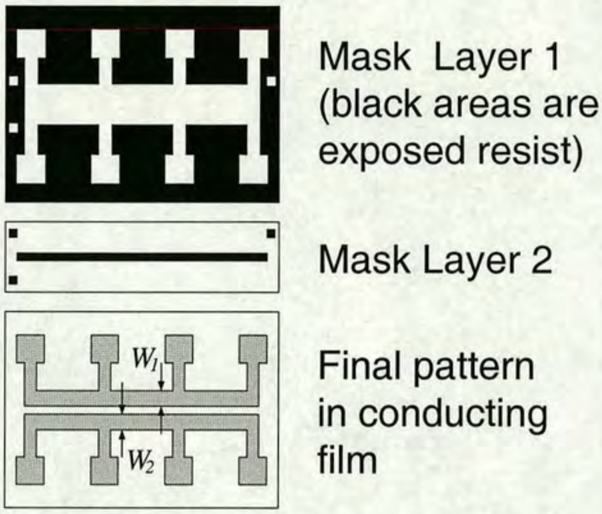


Figure 2.21: *Differential linewidth bridge test structure printed as a combination of two mask layouts.*

terminals to get R_1 and R_2. Then ΔW is calculated using

$$\Delta W = \frac{(W_1 - W_2)}{2} = R_S L \frac{1}{2}\left(\frac{R_2 - R_1}{R_1 R_2}\right) \tag{2.26}$$

The differential bridge requires a sheet resistance test structure close by to extract R_S and is subject to all the design rules applied to the bridge section of the cross-bridge linewidth structure. As with the original work on the eight terminal structure discussed above, this structure cannot be used to measure mask misalignment in a standard process because it is fabricated in a single layer of material. However, a variation on this structure can be used to measure misalignment between gate polysilicon and active area diffusions in a self-aligned MOS transistor process [97, 98]. In this structure the first mask will define the active area opening through the field oxide while the second will define the gate. The active area is doped by diffusion or implantation and the complete structure is illustrated in figure 2.22.

The voltage-dividing potentiometer and its derivatives are the most widely used test structures for the measurement of alignment [96, 99–105]. The basic operation of this structure is illustrated in figure 2.23.

The position of the centre voltage tap P3 is found by forcing a current along the conducting bridge and measuring the voltages $V1$ and $V2$. The offset x of the probe

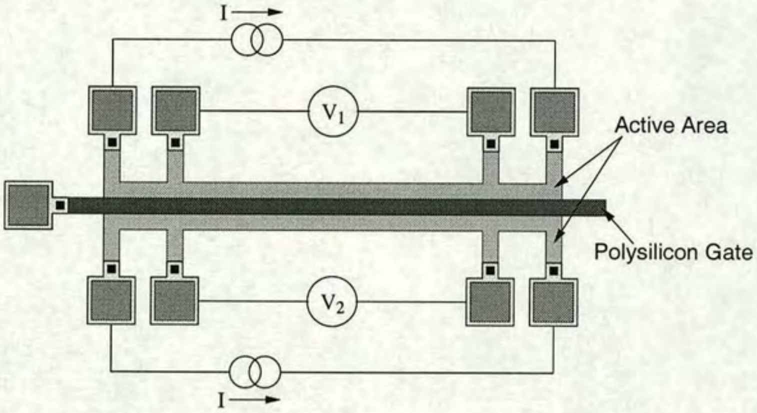


Figure 2.22: *Layout of differential bridge structure for poly to active area alignment measurement.*

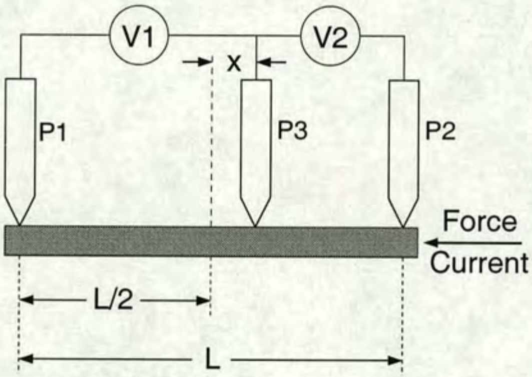


Figure 2.23: *Schematic illustration of the measurement of a voltage-dividing potentiometer.*

from the central position can be calculated using

$$x = \left(\frac{V_1 - V_2}{V_1 + V_2}\right)\left(\frac{L}{2}\right) \tag{2.27}$$

The accuracy of this structure will depend on the length of the bridge between the end voltage taps. It can be improved by reducing L as this increases the difference between V_1 and V_2 and reduces the effect of the uncertainty present in these measurements. The problem with scaling the bridge length in this way is that the effects of finite tap dimensions become important as with the bridge linewidth structure. The solution to this is to extract the linewidth shortening parameter δL with a structure similar to figure 2.16. An example of a test structure which can be used in this way is shown in figure 2.24.

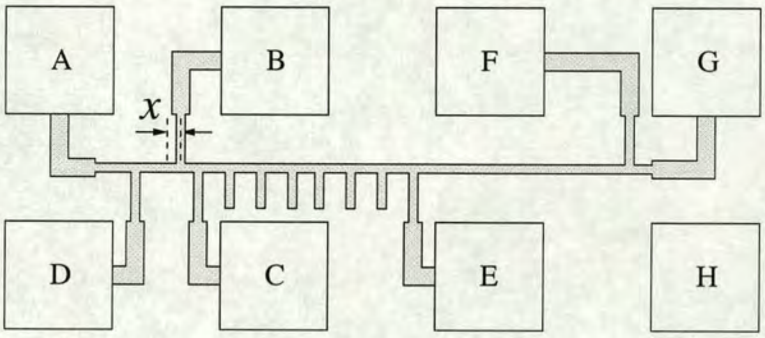


Figure 2.24: *Layout of test structure used to measure the tap offset x.*

It was found that there was a systematic error between the drawn and measured values of x [100], the source of which was identified as the asymmetrical layout of the voltage taps (the central tap (pad B) is connected to the opposite side of the structure from the end voltage taps (pads C and D)). The solution is to make the structure more symmetrical as has been demonstrated through computer simulation in reference [101]. The modified structure has an alignment bridge with all three taps on the same side and these taps extend on both sides of the bridge section by at least twice the tap width. This is illustrated in figure 2.25.

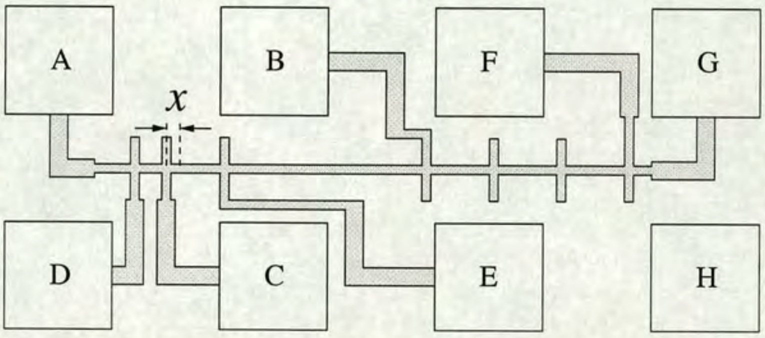


Figure 2.25: *Enhanced misalignment test structure with symmetrical voltage taps.*

Test structures with a similar layout were printed with fixed values of x and were accurately measured with an error of less than 10nm [96, 105]. Reference [103] describes the fabrication of similar misalignment test structures which were printed in polysilicon using two masks. The first mask defines the basic test structure while the second defines the position of the central voltage tap in a similar way to the structures pictured in figures 2.20 and 2.21. The residual errors in the final results obtained in this study were less than 11nm.

There are a wide range of other test structures which can be used to measure misalignment. These include; the triangular transistor [106, 107], passive and active digital alignment verniers [108–111] and the modified wheatstone bridge structure [112]. In addition to these electrical methods a technique using laser illumination of computer generated holograms has shown that misalignments in a single layer of metal can be measured with a resolution of about 0.1μm in a 1μm process [113–115]. The use of this technique for interlayer alignment metrology is theoretically possible but would require extremely accurate knowledge of interlayer dielectric thicknesses [62].

2.4 Conclusions

There are a number of methods available for the extraction of the sheet resistance of thin conducting layers. The four-point probe is useful for unpatterned films as this simplifies the calculations but other sample and probe geometries need to be analysed carefully to find the right correction factor.

The four-terminal van der Pauw method can be used to extract the sheet resistance of small, arbitrarily shaped, samples of uniform thickness and resistivity but requires point contacts for accurate measurement. The Greek cross is a special case of the van der Pauw structure with finite contacts and a scalable geometry which makes it ideal for use as a microelectronic test structure. Very small geometry Greek cross structures can be strongly affected by short range variations in the material resistivity caused by the grain structure of metal or polysilicon. Such structures can be used to quantify this variation but in most applications it is undesirable. In such cases a box cross structure can be used to extract a mean value of the sheet resistance as the measurement occurs over a larger area.

Measurement of linewidth is very important for the characterisation and control of lithographic or pattern transfer processes. The most widely used methods are optical and CD-SEM metrology as they can be used to measure developed photoresist before any further processing is performed. Both of these methods require a subjective decision about the position of the line edge which can lead to inaccurate results. AFM metrology is extremely sensitive but requires careful analysis of the tip shape for accurate measurement. In addition the measurements are too slow for use in process control and the equipment is very expensive.

Electrical linewidth measurement is typically performed using a four-terminal Kelvin bridge resistor in combination with a cross type sheet resistance structure. It is extremely repeatable as well as being relatively cheap and quick but can obviously only be used on conducting features. Design rules for this structure require a bridge which is much longer than it is wide but in some situations this is undesirable. The solution is to add features which can be used to extract the effect of the voltage taps on the measurement. This allows the use of short bridge sections without loss of accuracy. The basic cross bridge test structure has been adapted to measure many different parameters such as pitch and line spacing or lithographic proximity effects.

The Fallon ladder is an alternative to the cross-bridge linewidth structure which does not require high resolution test equipment. It can be used to extract the minimum resolution of a lithographic system and can be measured electrically or by optical or SEM inspection.

This chapter has also covered a range of different test structures used to measure the overlay between successive lithographic steps in a microfabrication process. The first of these is based on the van der Pauw resistor and can be used to measure X and Y misalignments as small as 0.1μm with an error of about 10%. The differential bridge structure consists of two four-terminal bridge resistors. The misalignment in this case is the difference between the bridge widths. A variation of this structure can be used to measure misalignment between the active area and polysilicon gate layers in a self aligned MOS process.

The final, and most widely used, alignment structure examined in this chapter was the voltage-dividing potentiometer. This is again based on the Kelvin bridge resistor but, unlike the differential bridge, does not require a value of sheet resistance for the measurement. The accuracy of measurements made with this type of structure can be increased by reducing the length of the bridge section and adding features which will allow the line shortening effects of the voltage taps to be measured.

Chapter 3
Sheet Resistance and Electrical Linewidth Measurement of Copper Damascene Interconnect

3.1 Introduction

The effects of the barrier layer and dishing in copper interconnect lead to extra difficulties in measuring sheet resistance (R_S) and linewidth when compared with equivalent measurements on non-damascene tracks. This chapter examines these issues and presents results which quantify the effects of diffusion barrier layers and dishing on the extraction of R_S from cross type test structures and the effect this has on linewidth measurement.

3.1.1 The Chemical Mechanical Planarisation (CMP) process

Advanced interconnect technologies are an essential part of the roadmap for improving the performance of integrated circuits [13]. As a result copper is rapidly replacing aluminium as the first choice for IC interconnect. Copper has a bulk resistivity of about $1.7\mu\Omega$-cm compared to $2.7\mu\Omega$-cm for Al [116]. The lower resistivity of copper, when combined with the introduction of low-k dielectrics, reduces RC time delays and power consumption [117]. Unlike aluminium, copper cannot be easily patterned using a subtractive process such as reactive ion etching and so a damascene metal process with CMP is used instead. A disadvantage of copper is that it will diffuse quickly into silicon and SiO_2 and can damage devices if it reaches the substrate. Consequently a protective barrier layer, consisting of a metal such as tantalum, must be employed. A typical copper interconnect process is illustrated in figure 3.1 [118, 119].

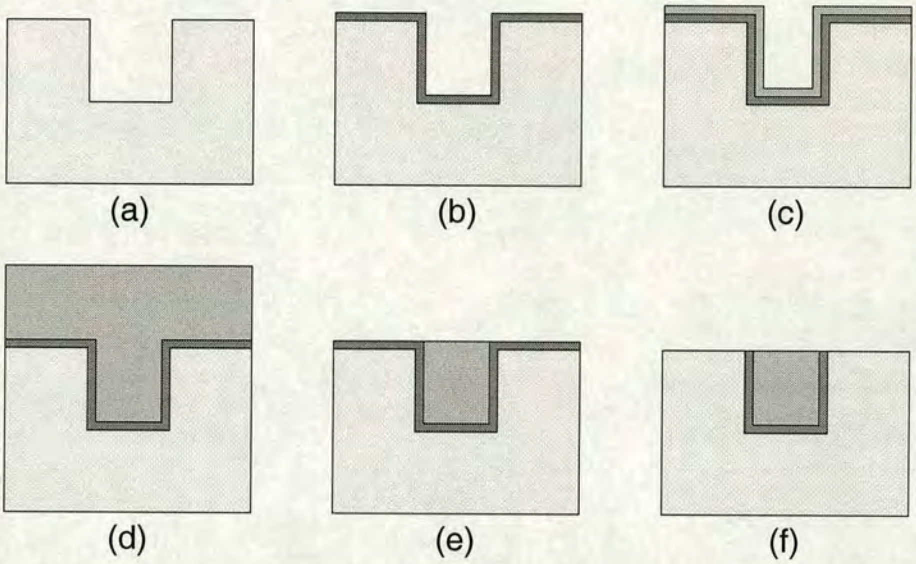


Figure 3.1: *Typical copper damascene process: (a) Etch tracks in inter-layer dielectric; (b) Deposit barrier layer Ta-PVD; (c) Deposit copper seed layer by PVD/CVD; (d) Copper deposited by electro-plating; (e) 1st CMP polish - selective towards Cu, stops on barrier layer; (f) 2nd CMP polish - removes Cu and Ta at same speed, removes barrier layer.*

3.1.2 Copper Damascene and Test Structures

Resistive electrical test structures used to measure the linewidth of conducting tracks assume a homogeneous layer of conducting material. This is not the case for copper damascene interconnect because of the requirement to use barrier layers. Figure 3.2 shows a schematic cross-section through two copper tracks with barrier layers and it is clear that as the width of the copper track decreases the percentage contribution of the barrier layer to the sheet resistance increases. For example, a tantalum diffusion barrier has a higher resistivity than copper ($\rho_{Ta} \approx 13\mu\Omega$-cm [116]) and a simple calculation based on the cross-sectional area can be used to calculate the resistance of a track [53].

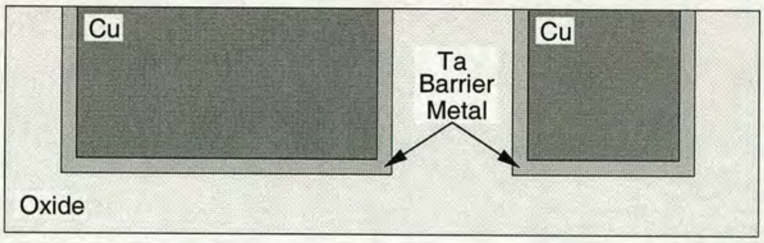


Figure 3.2: *Cross-section of copper damascene tracks of different widths. As the width of the copper line decreases the relative contribution of the sidewall barriers to the track resistance will increase.*

Another effect of the damascene process which can affect the resistance of a copper track is dishing. This occurs because the copper is softer than the surrounding dielectric and is removed more quickly. The CMP polishing pad deforms into the recess and removes more copper from the track making it thinner in the centre as is illustrated in figure 3.3.

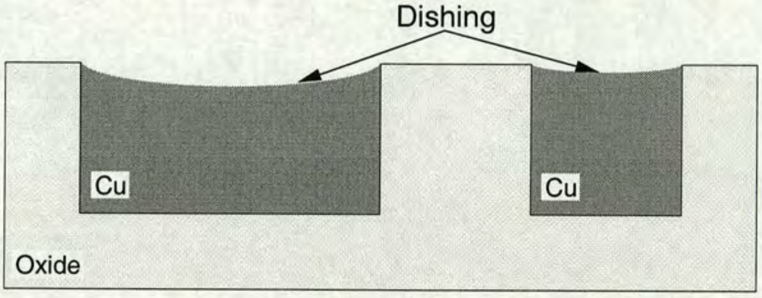


Figure 3.3: *Schematic cross section through two metal damascene lines which have been dished by the CMP process*

The amount of copper which is removed is a function of the track width [120, 121]. Figure 3.4 shows the results of Atomic Force Microscope (AFM) profile measurements which were made on copper damascene lines and demonstrates that the level of dishing increases as the feature becomes wider.

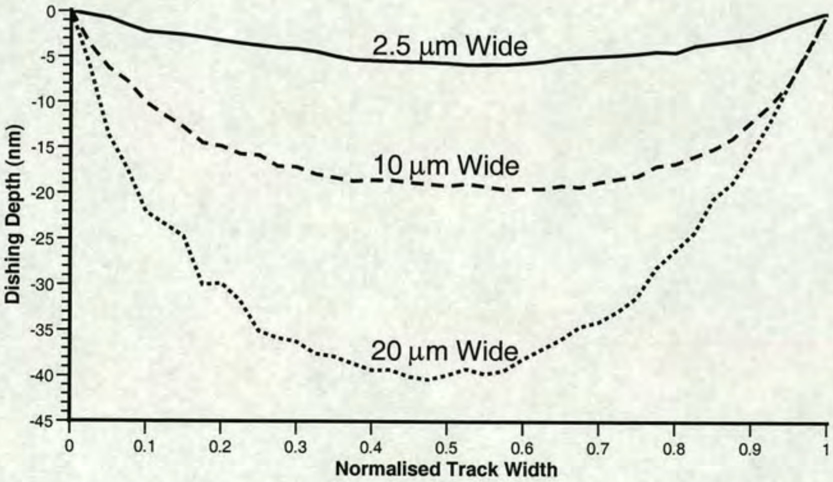


Figure 3.4: *AFM profiles of the surface of three copper tracks with linewidths of 2.5μm, 10μm and 20μm. The widths have been normalised in order to aid comparison.*

Any reduction in the cross sectional area of a track will increase its resistance. In order to electrically measure the linewidth of a conducting track the *effective* sheet resistance of the material must first be determined. This parameter is normally measured using either a Greek or box cross like those shown in figure 3.5. The method used to extract sheet resistance from such structures is described in section 2.1.4.

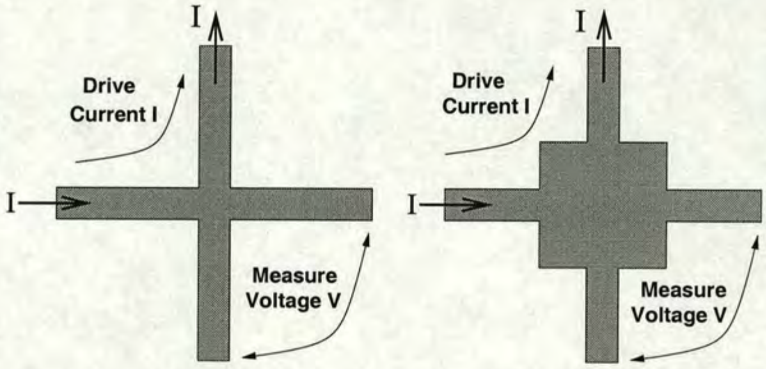


Figure 3.5: *Schematic plan views of Greek and box cross structures used for R_S extraction.*

These test structures are commonly used because no dimensional information is required in the measurement of sheet resistance. However, Greek and box crosses will be affected by the diffusion barrier layer and the pattern dependent effects of dishing. Any error in the value of R_S extracted using a cross sheet resistor will directly translate into an error in the value of linewidth calculated using that sheet resistance. Reference [53] discusses many of the issues associated with characterising copper interconnect using electrical test structures. The purpose of the work presented in this chapter is to quantify some of these effects through simulation.

3.2 The Effects of Barrier Layers and Dishing on the Measurement of Sheet Resistance and Electrical Linewidth

This section examines each of the damascene process issues in turn and describes the simulations that have been performed to determine their effect on the performance of sheet resistance test structures. This information is then used to investigate how errors in the extraction of sheet resistance affect electrical linewidth measurement. Finally, simulations of test structures which model the effects of both diffusion barrier layers and dishing together are described and the results presented.

3.2.1 Barrier Layer Effects on R_S Measurement

The first question that needs to be answered is the exact effect that the barrier layer has on the extracted value of R_S. The structure of the Greek cross used to perform this task is shown in figure 3.6. In this case the thickness of the tantalum barrier layer on the bottom and sidewalls of the trench was set to 50nm.

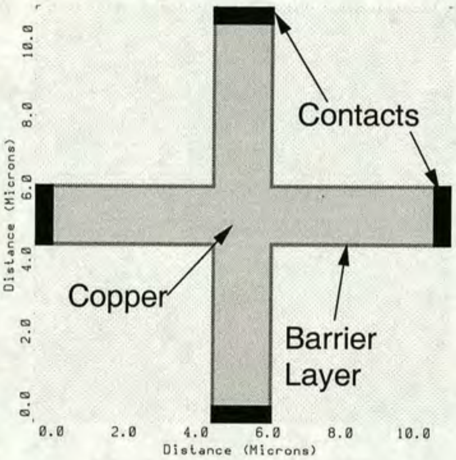


Figure 3.6: *Plan view of a Greek cross test structure for simulation of barrier layer effects.*

The 3-D interconnect simulator Raphael (see section A.3.2) was used for the following analyses with the material resistivities set to $1.7\mu\Omega$-cm for the copper core and $13\mu\Omega$-cm for the barriers. Figure 3.7 shows a schematic cross section through a copper track which indicates the important dimensions associated with the barrier layers.

For the following simulations the horizontal barrier width W_{bh} is 50nm and the copper thickness T_{Cu} is $0.45\mu m$ giving a total line thickness T_L of $0.5\mu m$. These values are same for all of the test structure simulations so a sheet resistance for the central part of the track, without the sidewall barrier layers, can be calculated. Using the values for ρ_{Cu} and ρ_{Ta} given previously the sheet resistance of the copper core in combination with the horizontal barrier layer ($R_{S(Cu+bh)}$) was calculated to be $0.037\Omega/\Box$.

Greek cross test structures were simulated for a range of different sidewall barrier widths (W_{bv}) from 25nm to 100nm and for linewidths (W_L) from $0.3\mu m$ to $5\mu m$. Box cross test structures where the box side was $10\mu m$ were also simulated with a sidewall

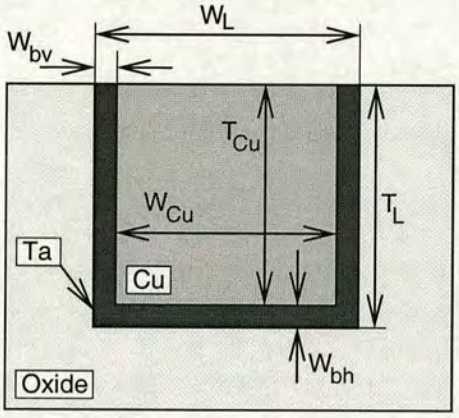


Figure 3.7: *Schematic cross section through a copper track with barrier layers showing the important dimensions.*

barrier thickness of 50nm. The width of the voltage taps in the box crosses varied over the same range of linewidths used for the Greek cross simulations. The grids for these simulations were set to have 1.5 million nodes but the software controlled grid generation resulted in the actual figures being lower, usually in the range of 1-1.4 million grid points. In each simulation two adjacent terminals are designated as the contacts through which the current will be forced. One of these contacts is grounded and the other has a voltage applied to it so that a current will then flow between them. The voltage, with respect to ground, is then measured at the other two terminals. The potential difference between these two measurements (V) is then used, along with the forced current (I), in equation (2.18) with $R = V/I$, to calculate the sheet resistance. Each simulation takes about two hours to run on a Sun Ultra 10 workstation and the results are presented in figure 3.8.

For large values of W_L the sheet resistance extracted from the simulated structures is close to the value of $R_{S(Cu+bh)}$. This indicates that the the effect of the sidewall barriers on the measurement is minimal and that the majority of the current flowing is in the highly conductive central region of the cross. The sheet resistance which is extracted is that of the copper core and the horizontal barrier layer. As the linewidth is reduced the difference between $R_{S(Cu+bh)}$ and the sheet resistance extracted from the cross structure increases. This is because more of the current is beginning to flow in the vertical barrier layers. As would be expected the onset of this condition will depend on the value of the sidewall barrier thickness and the resistivity of the barrier material.

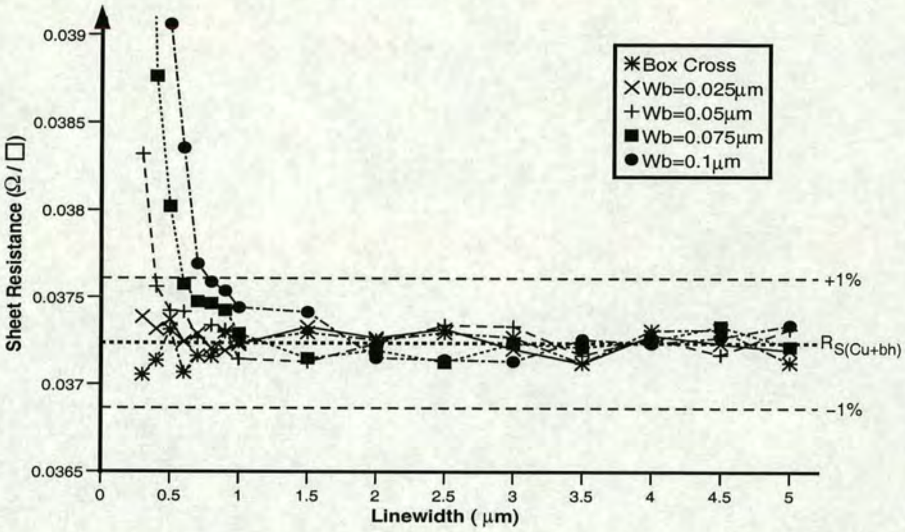


Figure 3.8: *Extracted sheet resistance versus linewidth for simulated Greek and box cross structures with barrier layers.*

If a sheet resistance error of more than 1% is considered to be significant then the minimum linewidth for each value of W_{bv} can be determined. These figures are presented in table 3.1. Note that the "Error" is the percentage difference between the extracted sheet resistance and the specified value of $R_{S(Cu+bh)}$.

W_{bv} (μm)	W_L (μm)	Error
0.025	0.3	0.4%
0.05	0.4	0.87%
0.075	0.6	0.91%
0.1	0.8	0.94%

Table 3.1: *Minimum value of cross arm width W_L where the error in the extracted sheet resistance is less than 1% for each of the sidewall barrier widths W_{bv} simulated.*

Even at the minimum linewidth of $0.3\mu m$ the error in R_S is less than 1% for the Greek cross simulations with $W_{bv} = 25$nm. From the other results it can be determined that the error will be less than 1% provided that $W_L > 8W_{bv}$ and the resistivities of the copper core and the barrier layers are the same as those used in the simulations. By taking into account the ratio of these resistivities a more general expression can be developed:

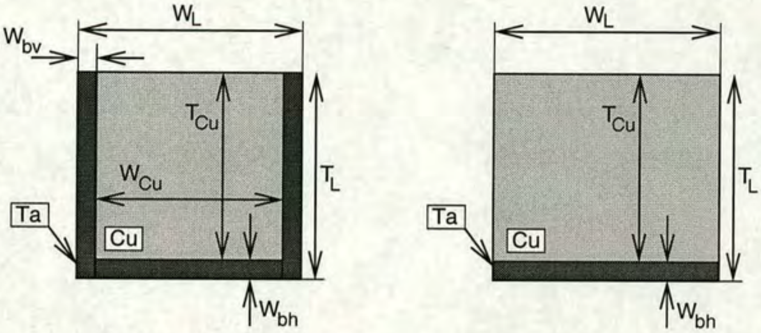
$$W_L > 61.2\frac{\rho_{Cu}}{\rho_b}W_{bv} \tag{3.1}$$

where ρ_b is the resistivity of the barrier material. The sheet resistances extracted from the box cross structures were all within 1% of $R_{S(Cu+bh)}$. This was expected because only the width of the voltage taps was varied. From these results it is clear that to accurately measure the sheet resistance of copper over an underlying barrier layer, either a box cross structure or a Greek cross which meets the condition given in equation (3.1) should be used.

3.2.2 Barrier Layer Effects on Linewidth Measurement

Electrical Critical Dimension (ECD) or linewidth is usually measured using a bridge type, four-terminal test structure [39]. This involves the measurement of the resistance R_L of a line of known length L. For the purposes of the work described here the value of R_L has been calculated by considering the cross section through a damascene copper track as represented in figure 3.7. The length of the line was set to be $100\mu m$ when calculating the resistance. The sheet resistance R_S is found from a cross type test structure and the electrical linewidth W_L is calculated using equation (2.20). It was shown in section 3.2.1 that the sheet resistance of copper over a horizontal barrier layer ($R_{S(Cu+bh)}$) can be extracted accurately from a box cross structure or a Greek cross with wide arms. If the metal line being measured has the same sheet resistance then it is possible to extract the linewidth with a similar accuracy. Unfortunately the presence of sidewall barrier layers means that the sheet resistance is not uniform across the width of the track. In order to achieve an accurate measurement of linewidth from a damascene track with sidewall barriers a method for determining the equivalent line resistance of a track with the same width but a constant sheet resistance $R_{S(Cu+bh)}$ has been developed. The effect of this procedure is illustrated in Fig. 3.9 which shows vertical cross sections through tracks with and without sidewall barriers. The resistances of the tracks are R_L and R_{eq} respectively.

The resistance difference between the original track and the equivalent uniform line is the resistance of the two sidewall barriers plus the effect of reducing the central core of the track by $2W_{bv}$. It is possible to define a modification factor R_{SW} which will allow the calculation of R_{eq} by subtracting it from the line resistance. R_{SW} is the difference between the resistance of the track with sidewall barriers and that of the equivalent



Resistance = R_L
(a)

Resistance = R_{eq}
(b)

Figure 3.9: *(a) Cross section through a copper damascene track. (b) Equivalent cross section for a track with a uniform sheet resistance.*

track with a uniform sheet resistance

$$R_{SW} = \left(\frac{1}{R_L} - \frac{1}{R_{eq}}\right)^{-1} \tag{3.2}$$

and because $R_L > R_{eq}$ it will have a negative value.

The value of R_{SW} will depend upon the sidewall barrier width W_{bv} which was defined as a constant in the simulations described in section 3.2.1. This assumption is reasonable for the barrier widths and feature sizes considered here but does not hold for narrower lines where a shadowing effect can reduce the barrier thickness [53]. This being the case R_{SW} does not vary with linewidth and it is therefore possible to calculate its value using

$$R_{SW} = \frac{R_{W_1} R_{W_2}}{2R_{W_2} - R_{W_1}} \tag{3.3}$$

where R_{W_1} and R_{W_2} are the resistances of copper damascene lines with widths W_1 and W_2 where $W_2 = 2W_1$. For example, if $W_{bv} = 0.05\mu m$ and $T_L = 0.5\mu m$ then the resistance of a $1\mu m$ wide line is $R_{W_1} = 4.072\Omega$ and the resistance of a $2\mu m$ track is $R_{W_2} = 1.945\Omega$, where length $L = 100\mu m$. This results in R_{SW} having the value -43.461Ω.

R_{SW} can now be used to calculate R_{eq} by rearranging equation (3.2) to give

$$R_{eq} = \left(\frac{1}{R_L} - \frac{1}{R_{SW}}\right)^{-1} \tag{3.4}$$

For example, the sheet resistance extracted from the Greek cross simulation with W_L equal to $1\mu m$ was $0.037\Omega/\square$ and if this is used in equation (2.20) with $R_L = R_{W_1}$ the electrical linewidth (W_L) will be $0.9121\mu m$ which is in error by more than 8%. If the line resistance is modified using equation (3.4) then a new value of linewidth can be calculated. In this case $W_{L(eq)} = 0.9975\mu m$ which reduces the error to 0.25%. Similar calculations have been performed using the results of the test structure simulations described in section 3.2.1 and the linewidth error results are presented in figure 3.10.

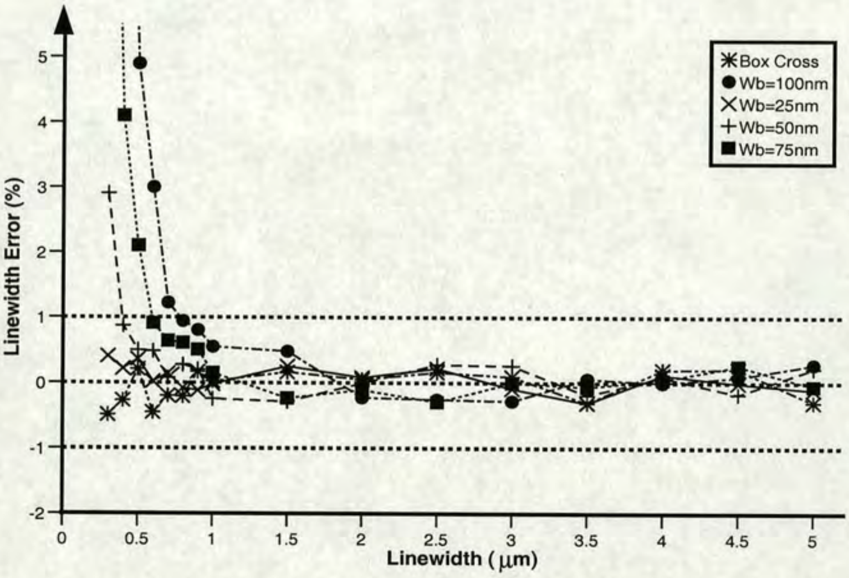


Figure 3.10: *Electrical linewidth measurement error versus actual linewidth for test structures with diffusion barrier layers of different widths.*

This shows the same trends seen in figure 3.8 which is to be expected. It can be observed that as the barrier width increases, the errors at low values of linewidth also increase. It should be noted that the box cross is insensitive to the actual linewidth and, provided there is no dishing, should be used in preference to a Greek cross.

3.2.3 Dishing Effects on R_S Measurement

Equation (3.1) gives the conditions that are required to extract the copper over barrier layer sheet resistance using a Greek cross where the damascene metal is assumed to have a rectangular vertical cross section. Unfortunately, the CMP process also affects the sheet resistance of conducting tracks through dishing and it is important to quantify the effect of this on the extraction of R_S. Figure 3.11 is a schematic cross section through a dished track and indicates the important variables used in the model described in reference [122].

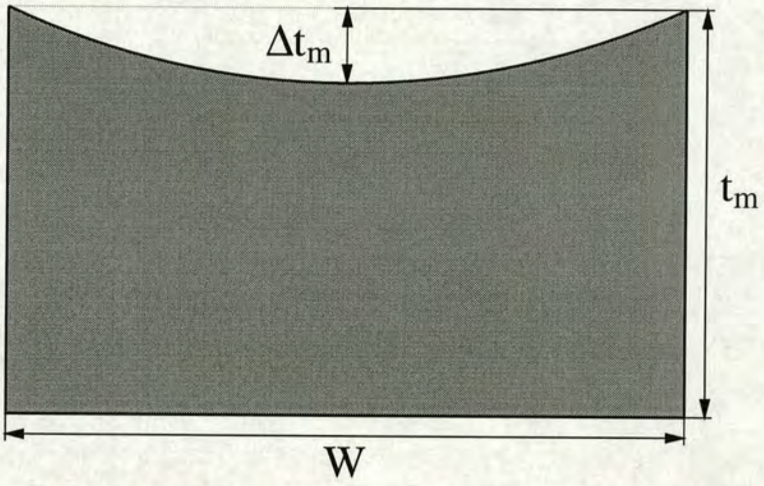


Figure 3.11: *Schematic cross section through a dished damascene track.*

The model defines the cross sectional area of such a copper track as

$$A = t_m W \left(\frac{1 + 2\alpha}{3} \right) \tag{3.5}$$

The variable α is the ratio of the metal thickness at the centre of the dished line to the ideal thickness, t_m.

$$\alpha = \frac{t_m - \Delta t_m}{t_m} \tag{3.6}$$

The dishing model also provides equations for α in terms of the feature width W at two different CMP endpoint conditions. These are, for a nominal polishing time

$$\alpha = 0.32e^{-0.008W} + 0.65 \tag{3.7}$$

and for a 25% overpolish:

$$\alpha = 0.68e^{-0.008W} + 0.22 \tag{3.8}$$

In the simulations that follow dishing has been approximated with a stepped cross section, as shown in figure 3.12, rather than a smooth curved surface.

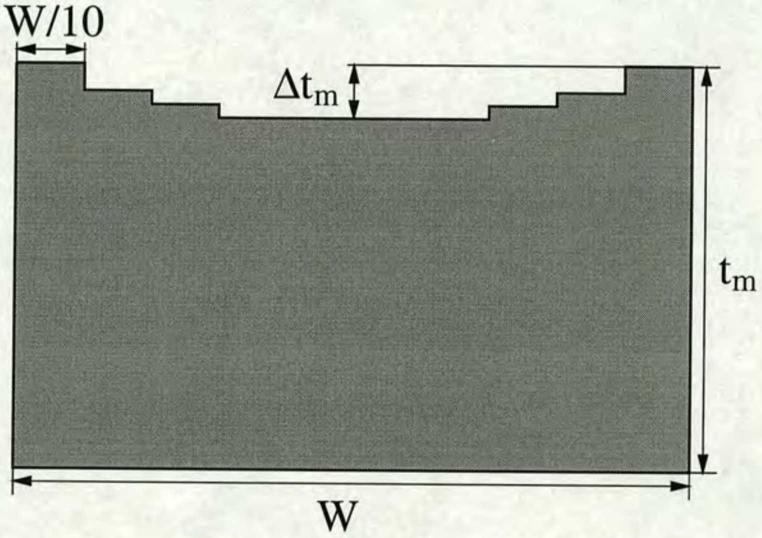


Figure 3.12: *Schematic cross section through a dished damascene track showing the stepped approximation of dishing used in the simulations.*

The first set of simulations which were performed using this model of dishing were Greek and box cross test structures modelled in two dimensions. With no vertical (z) dimension the change in the thickness of the conducting material due to dishing is approximated as a change in the sheet resistance. This results in the middle of the damascene structure, where the copper is thinnest, having a higher sheet resistance than the edge. Figure 3.13 shows a plan view of a Greek cross structure demonstrating the way that the sheet resistance changes across the structure to model the effect of dishing.

Greek and box cross test structures with voltage tap widths ranging from $1\mu m$ to $5\mu m$ have been simulated and sheet resistances extracted using the method described in section 2.1.4. Only structures using the 25% overpolish condition have been simulated in 2-D. The grids used for these simulations were set to have 0.5 million nodes though the actual number varied depending on the structure. The results of the simulations are shown in figure 3.14.

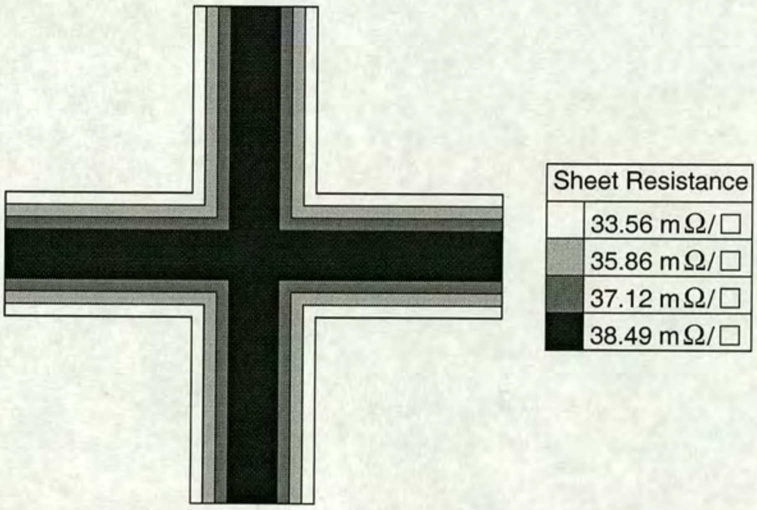


Figure 3.13: *Schematic plan view of a Greek cross with a linewidth of* $5\mu m$ *simulated in 2-D. The sheet resistance of each part of the cross depends on the amount of dishing in that area.*

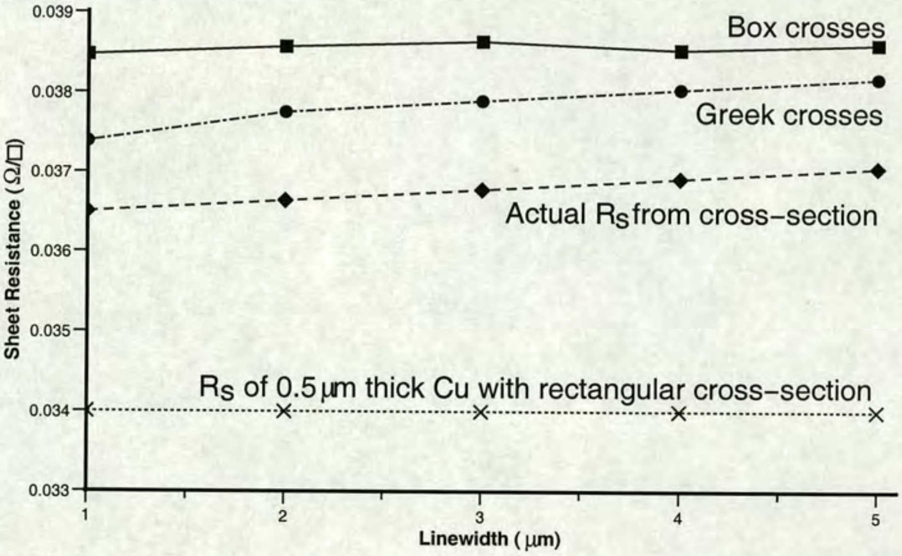


Figure 3.14: *Sheet resistance against linewidth for 2-D simulations of copper damascene test structures with 25% overpolish.*

The actual sheet resistance of a dished line of a given linewidth can be calculated by determining its cross sectional area using equations (3.5) and (3.8). This has been performed for each of the linewidths simulated and the results plotted in figure 3.14

along with the sheet resistance of $0.5\mu m$ thick copper with no dishing ($0.034\Omega/\square$). It can be observed that there is an offset of about 3% between the sheet resistance extracted from the Greek cross structures and that derived from the cross section of the line. The values of R_S extracted from the box cross do not increase with the width of the voltage taps because the dishing of the box is constant. The difference between the sheet resistance extracted from the box cross structure and the equivalent sheet resistance of the dished lines is greater (4% - 5%) simply because the larger dimensions of the box cross lead to more severe dishing.

However, it is possible that this 2-D approximation does not necessarily reflect the actual current flow that would occur in a real, three-dimensional, test structure. It is also likely that the dishing in the center of a Greek cross structure will be different to that in the arms. The depth of the dishing depends upon the width of the metal feature and the diagonal width across the center of a cross is greater than across the the voltage taps by a factor of $\sqrt{2}$. In order to investigate this effect a small number of AFM scans of copper damascene test structures have been performed. Figure 3.15 shows one scan of the centre of a Greek cross.

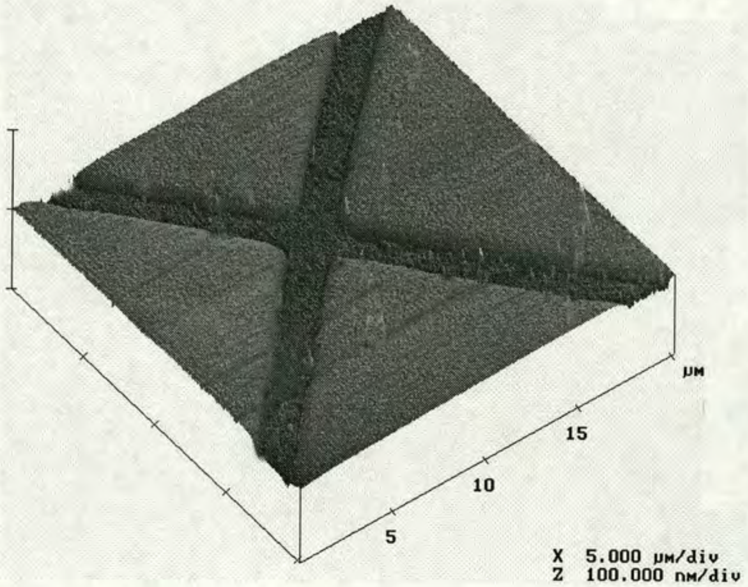


Figure 3.15: *$20 \times 20\mu m$ AFM scan of a copper damascene Greek cross test structure. The arms of the cross are $1\mu m$ wide.*

The CMP process used to produce this structure is a two stage process where the first polish slurry etches copper much faster than the barrier material (in this case the barrier is tantalum nitride) so that the process stops on the barrier layer. The second polish step uses a slurry that removes the copper and TaN at the same rate and is used to remove the excess barrier material. It was found that the amount of dielectric erosion along the edges of copper features after the second polish was so great that the dishing of the copper was not visible in AFM profiles. Because of this all of the AFM results described here were obtained from structures where the process was stopped after the first polish. The problem with using AFM profiles taken at this stage is that the slurry used in the first stage tends to etch the copper surface even when the wafer being polished is at rest. This means that the copper features usually end up being lower than the surrounding barrier material but with a surface profile that is quite different than that suggested by the dishing model. Instead of a smooth curved surface like that shown in figure 3.11 where the copper is thinner in the middle of the feature the slurry will etch the copper evenly across the track giving a flat surface. The surface will also show some roughness due to the aggressive slurry etching the copper faster at grain boundaries. This can be seen in figure 3.16 which shows profile lines extracted from the AFM scan of the copper Greek cross.

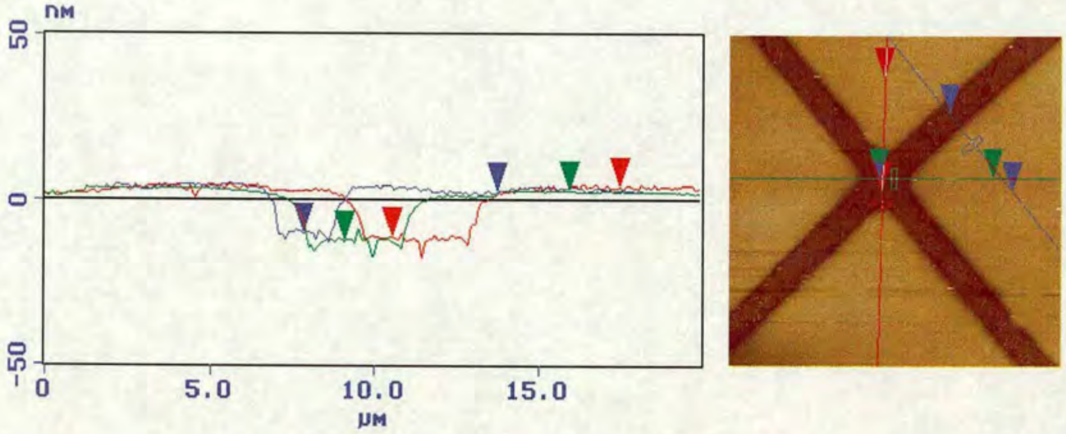


Figure 3.16: *On the left is a set of three AFM surface profiles from a copper damascene structure. On the right is a* 256 × 256 *AFM scan showing where the profiles have been taken from.*

Figure 3.16 also shows that the depth of the copper recess in the centre of the Greek cross is 2-3 nm greater than that measured in the arm of the cross. For this reason it was decided that a change should be made to the simulated structures in order to model increased dishing in the centre of a damascene Greek cross.

A new set of three-dimensional structures with this more complicated dishing arrangement have been simulated. The first step was to calculate a new depth of dishing in the centre of the cross. The value of linewidth (W) used in equations (3.7) and (3.8) is the diagonal width of the cross measured between opposite internal corners. In order to achieve the correct profile across the centre of the cross in the simulated structure, cylindrical sections of the conducting track were removed as illustrated in figure 3.17.

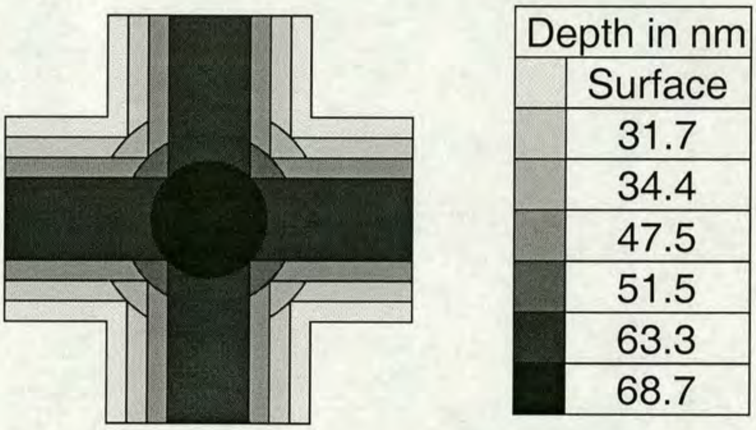


Figure 3.17: *Schematic plan view of the centre of a* $5\mu m$ *Greek cross which shows how dishing has been modelled in three dimensions in this part of the simulated structure.*

Both the nominal and 25% overpolish endpoint conditions have been used in the three-dimensional simulations and the results of extracting R_S from these structures are presented in figure 3.18. By using equation (3.5) to get the cross sectional area it is possible to calculate an actual sheet resistance for a dished line. This has been performed for the two different endpoints and for each of the linewidths simulated and the results are plotted alongside the simulation results. For reference, figure 3.18 also shows the nominal value of sheet resistance for $0.5\mu m$ thick copper with no dishing.

The results for the 3-D simulations with 25% overpolish compare well with the 2-D results indicating that the assumptions of the 2-D model approximating the dishing effect are reasonably valid. From figure 3.18 it can be observed that the offset between the sheet resistances extracted from the Greek cross structures and those calculated for a dished line is approximately 0.7% for the nominal polish conditions and 3% for the structures with 25% overpolish. This indicates that the error in the extracted sheet

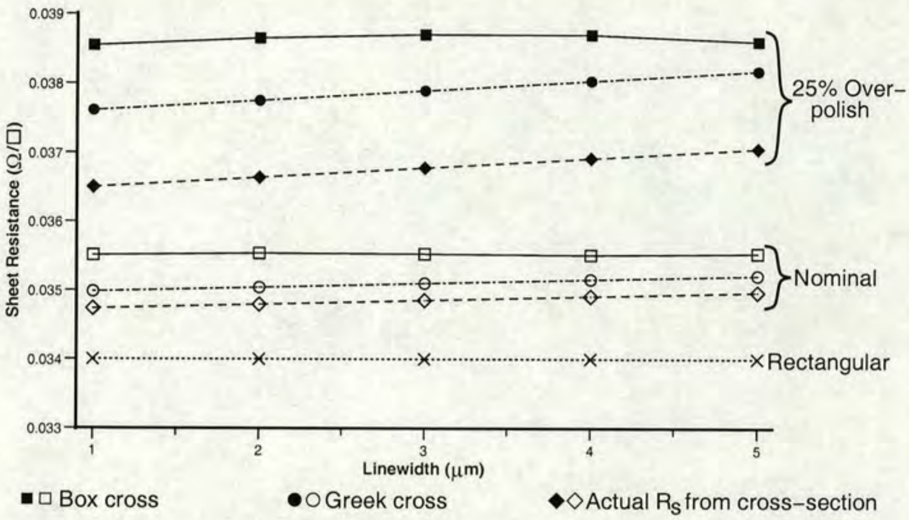


Figure 3.18: *Sheet resistance versus linewidth for 3-D simulations of the effects of dishing on Greek and box crosses.*

resistance increases with the amount of overpolish and therefore the level of dishing.

One important thing to note is that as the linewidth increases, the extracted R_S from the Greek cross structures increases at the same rate as the actual sheet resistance calculated from the cross sectional area. This is not the case for the simulated box cross structures where the sheet resistance extracted is independent of the width of the voltage taps. The variation in the 25% overpolish box cross results is probably due to small variations in the number of nodes in the automatically generated simulation grid.

3.2.4 Dishing Effects on Linewidth Measurement

The next step is to investigate the effect of dishing on the measurement of electrical linewidth. Equation (3.5), which gives the cross sectional area of a dished track, can be used to calculate the resistance for a certain length of copper line. This calculation has been performed for each of the linewidths used in the test structure simulations and for both endpoint conditions.

The electrical linewidth can then be found by using the line resistance and the extracted sheet resistances in equation (2.20). If these results are then compared to the actual widths the linewidth measurement errors due to dishing can be calculated. This process has been followed using the sheet resistances extracted from the 3-D simulations and the results are presented in figure 3.19.

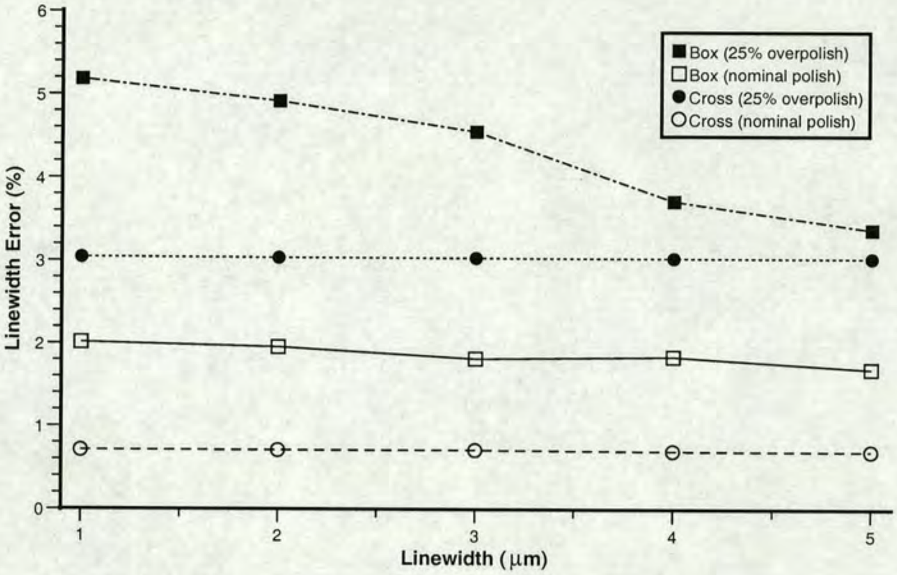


Figure 3.19: *Electrical linewidth error versus the actual linewidth for structures with dishing.*

The linewidth errors for the Greek crosses do not vary with tap width staying at about 3% for the 25% overpolish condition and at about 0.7% for the nominal polish. This should be expected because of the way that the sheet resistance extracted from the Greek crosses increases at the same rate as that calculated from the dished cross section. This can be seen for both of the endpoint conditions in figure 3.18. The box cross results are different because the amount of dishing in the box does not change with the voltage tap width. This means that the errors decrease with increased linewidth but are still higher than for the Greek cross structures. These results indicate that, provided the condition in equation (3.1) is not violated and instrumentation resolution and joule heating are not issues [53], sheet resistance measurements should be made using Greek cross structures with arm widths the same as the linewidth structures being tested.

The effects of diffusion barrier layers and dishing have been investigated separately so far but in a real copper test structure both will be present. The next step is to simulate structures which include both effects.

3.2.5 Combining Barrier Layers and Dishing

A vertical cross section through a copper damascene line which features both diffusion barrier layers and the stepped model of dishing can be seen in figure 3.20. The depth of the dishing for the simulation structures described in this section was calculated using the copper width W_{Cu} as the linewidth W in the equations for α.

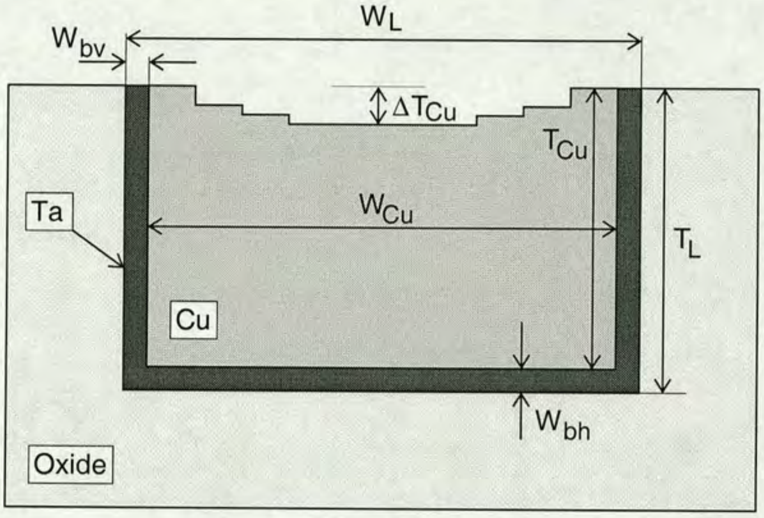


Figure 3.20: *Schematic cross section through a dished damascene track with diffusion barrier layers.*

Six Greek crosses and the same number of box crosses were simulated with voltage tap widths (W_L) varying from $0.3\mu m$ to $5\mu m$. All of the structures use the 25% overpolish endpoint condition (equation (3.8)) to determine the depth of dishing and have barrier layers 50nm thick. As in the previous simulations the size of the box in the box cross structures stays constant with only the width of voltage taps changing. The results of extracting sheet resistances from the simulated structures can be seen in figure 3.21. The effect of dishing dominates the results from the Greek cross for arm widths of $1\mu m$ and above and so the sheet resistance increases with width. As would be expected from the results in section 3.2.1 the sheet resistance extracted from the smallest Greek cross structure ($W = 0.3\mu m$) is greater than the other results due to the effect of the sidewall barriers. The results from the box cross simulations also agree with the results in the previous sections showing that such structures are insensitive to changes in the width of the voltage taps.

Figure 3.21 also shows sheet resistance values obtained by calculating the resistance of

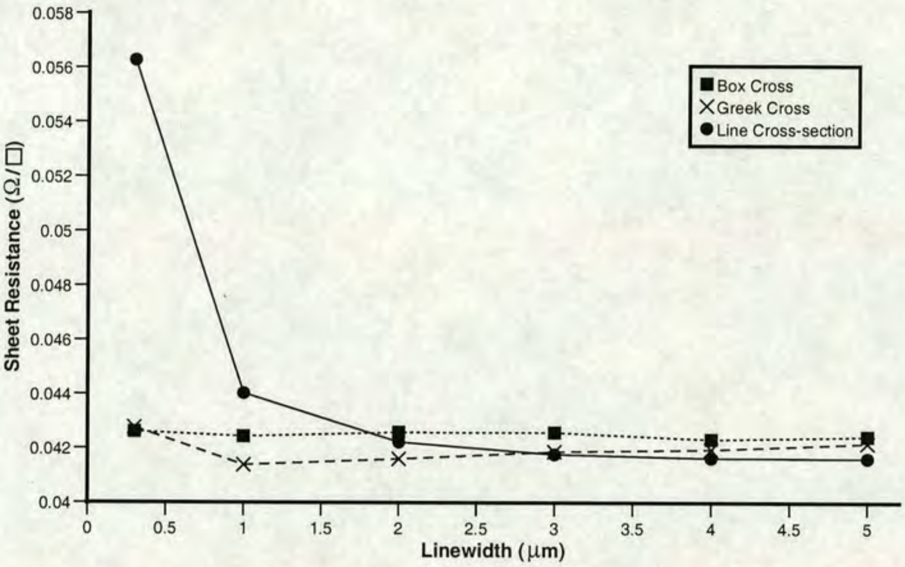


Figure 3.21: *Sheet resistance versus linewidth for sheet resistance test structures with both barrier layers and dishing.*

a copper track with a cross section like that shown in figure 3.20. It is clear that for low values of linewidth the equivalent sheet resistance calculated for the line is much higher than the value extracted from the test structures. This is because the contribution of the sidewall barriers to the total resistance starts to become more dominant. However, it should be possible to calculate the effect of the sidewall barriers on the line resistance and subtract it as was demonstrated in section 3.2.2. The problem with that method in this case is that dishing introduces an error which cannot easily be accounted for. To lessen this effect the resistance modification factor R_{SW} should be determined using the narrowest possible tracks which in this case means linewidths of $0.3\mu m$ and $0.6\mu m$. It should be remembered that this approach assumes that the sidewall barrier layer thickness is not a function of linewidth [53]. The resistances were calculated to be 18.759Ω for the $0.3\mu m$ track and 7.817Ω for the $0.6\mu m$ track, with the line length equal to $100\mu m$. When these values were substituted into equation (3.3) R_{SW} was found to be -46.936Ω. The next step is to subtract this from the calculated line resistances with equation (3.4) and use the results to calculate new equivalent sheet resistances. Table 3.2 shows the equivalent sheet resistances both before and after modification of the line resistance as well as the difference between these values and those extracted from the Greek cross simulations.

$W_L(\mu m)$	$R_{S(Line)}(\Omega/\Box)$	$Error_{Line}(\%)$	$R_{S(modified)}(\Omega/\Box)$	$Error_{modified}(\%)$
0.3	0.05628	-24.01	0.04021	6.36
1	0.04403	-6.01	0.04025	2.8
2	0.04222	-1.47	0.04041	2.96
3	0.04177	0.23	0.04057	3.21
4	0.04164	0.76	0.04073	2.99
5	0.04162	1.33	0.0409	3.13

Table 3.2: *Results of modifying the resistance of a dished copper track with barrier layers to remove the effect of the sidewall barriers. Note that "Error" is the difference between the value of R_S and that extracted from a simulated Greek cross with the same linewidth.*

The error between the modified R_S calculated for the line and that extracted from the simulated structures is constant at about 3% for widths of $1\mu m$ and above. This is similar to the results presented in section 3.2.3 indicating that this offset is due to dishing. The error, at a linewidth of $0.3\mu m$, of just over 6% is about 3% higher than the error seen for the structures with no dishing in section 3.2.1. This should be expected as the error is a combination of the effects of the sidewall barriers and dishing on the Greek cross.

The line resistances calculated previously to obtain the results in table 3.2 and the sheet resistances extracted from the simulated structures can be used to obtain electrical linewidth results in the same way as in section 3.2.2. Figure 3.22 shows the results of calculating linewidth error using the modified line resistances.

The results obtained using the sheet resistances extracted from the box cross simulations are quite similar to those presented in section 3.2.3 for structures with no diffusion barrier layers. The error decreases as the width of the track increases towards the actual size, and therefore level of dishing, of the box section of the structure. The errors seen when using the results from the Greek cross simulations to calculate linewidth are the same as the sheet resistance errors presented in the $Error_{modified}$ column of table 3.2. This is because any error in R_S translates directly into an error in linewidth. The error of about 3% observed for linewidths of $1\mu m$ or above is the same as that seen in figure 3.19 for Greek crosses using the 25% overpolish condition. The increased error observed for a width of $0.3\mu m$ should be expected because the structure does not meet the condition given in equation (3.1) for the minimum width.

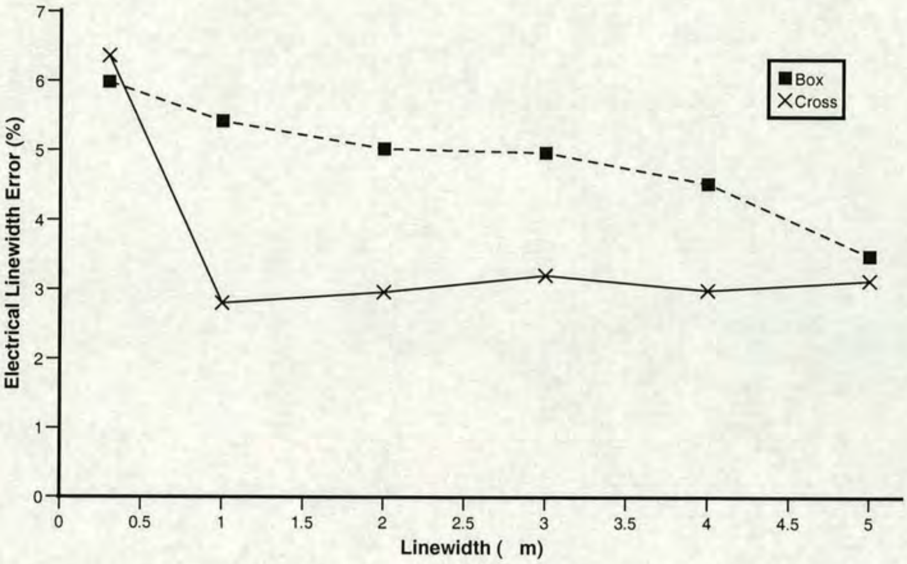


Figure 3.22: *Electrical Linewidth error versus actual linewidth for structures with both dishing and diffusion barriers.*

The results for structures with both barrier layers and dishing are close to those predicted by combining the results from the previous sections. This suggests that it is possible to study each of the damascene effects in isolation from other process issues and still obtain useful results.

3.3 Conclusions

This chapter has quantified the effects of diffusion barrier layers and dishing on the measurement of the sheet resistance and electrical linewidth of copper damascene interconnect. Section 3.2.1 showed that a Greek cross test structure can be used to measure the sheet resistance of copper and an underlying barrier layer with an error of less than 1% provided that the condition given in equation (3.1) is satisfied. It was also found that the values of R_S extracted from box cross sheet resistance structures were always within 1% of the correct value because the box structures are insensitive to the voltage tap width.

The results of the test structure simulations were then used to evaluate the effect of diffusion barrier layers on the electrical measurement of linewidth. It is clear that the effect of the sidewall barriers on the total line resistance becomes more dominant as the width of the line being measured is reduced. This potentially leads to very large errors in the linewidth measurement but fortunately it is possible to calculate the sidewall contribution and subtract it. The modified line resistances can then be used, along with sheet resistances extracted from the simulated structures, to calculate the electrical linewidth using equation (2.20). The only error in the resulting linewidth will be due to the effect of the sidewall barriers on the cross structure used to extract R_S. This method assumes that the sidewall barrier width (W_{bv}) does not vary with the total width of the line which will normally be the case for the feature sizes considered in this work [53].

The simulations of the effects of barrier layers assume that the metal track has a rectangular cross section but in most damascene processes some dishing will occur. Some exceptions to this might be advanced polishing processes with well developed endpoint control to reduce dishing or processes which use low-k dielectrics that are softer than copper [123]. The model of dishing which was used to create the simulated Greek and box cross test structures had two possible polishing endpoint conditions. The difference between the sheet resistances extracted from the Greek cross structures and equivalent sheet resistances for copper lines with the same amount of dishing was found to be less than 1% using the nominal polish condition and about 3% with a 25% overpolish. Although the amount of dishing is a function of linewidth this difference stays constant with width. This contrasts with the results from the box cross structures where the difference is greater and changes with the width of the voltage taps. These differences translate directly into linewidth errors when the extracted sheet resistances are used to measure electrical CD.

These results can be used to predict how a combination of dishing and barrier layers would affect the performance of sheet resistance test structures. These predictions are as follows:

- Errors in the sheet resistance, extracted from Greek cross test structures meeting the condition given in equation (3.1), will be dominated by the effects of dishing. R_S will increase as the arm width, and therefore the dishing, increases.
- The errors from Greek crosses which do not meet the condition of equation (3.1) will be dominated by the effects of the sidewall barrier layers and the sheet

resistance will increase as the arm width decreases.

- The sheet resistance extracted from box cross structures will not depend upon the width of the voltage taps but it will be affected by dishing in the large area of the box section.

The results of the simulations described in section 3.2.5 confirm these predictions. The value of R_S extracted from the smallest Greek cross structure is greater than all the other results because this structure is affected by the sidewall barrier layers. The other Greek cross structures meet the condition in equation (3.1) but are affected by dishing which means that R_S increases with arm width. The results of the box cross simulations are also as predicted with the sheet resistance staying reasonably constant at approximately $0.0425\Omega/\Box$ for all the different voltage tap widths simulated. When these results were used to calculate errors in linewidth measurement it was found that using a Greek cross which meets the width condition gives the minimum value of linewidth error. Therefore it can concluded that in order to achieve the most accurate measurement of the linewidth of a copper damascene track affected by both dishing and diffusion barriers the sheet resistance should be measured using a Greek cross which has arms the same width as the track.

Chapter 4
Test Structures for Use as Linewidth Measurement Standards

4.1 Introduction

This chapter begins by examining the motivation behind the development of electrical test structures for use as linewidth reference artifacts for Critical Dimension (CD) instrument calibration. One method of achieving this aim is to use cross-bridge linewidth structures fabricated in mono-crystalline silicon and this chapter will go on to review the previous work in this area. Three dimensional simulations of mono-crystalline silicon test structures have been performed in order to investigate the effects of production and testing parameters on their performance. The main part of this chapter will describe these simulations and present the results.

4.2 Motivation for the Development of Electrical CD Standards

The International Technology Roadmap for Semiconductors (ITRS) states that there is a need for reference materials for Critical Dimension (CD) measurement instrument design and calibration which meet the demands of deep sub-micron lithography [13]. Electrical CD measurements show the required level of repeatability[1] and directly relate to electrical functionality which is important for interconnect metrology. However, ECD measurements can only be made on conducting features and most metrology is performed on patterns in photoresist. This means that optical, CD-SEM (CD-Scanning Electron Microscope), surface profiler and AFM (Atomic Force Microscope) measurements are more common choices for linewidth measurement in a process control situation. In order to meet ITRS sub-micron metrology tolerances these

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[1] Typical repeatability is better than 1 nm (2σ) for lines with a nominal width of 1μm [124].

physical measurement techniques would require calibration with reference materials, which are traceable to nanometer level uncertainties.

Reference artifacts for measurement tool calibration should not display methods divergence, which is a systematic difference between measurement results depending on the instrument being used. References [89] and [90] describe comparisons between CD measurements made electrically and measurements of the same structures made using optical and CD-SEM techniques. These show that methods divergence can cause systematic differences which can make up a significant proportion of the linewidth. This effect occurs because each instrument is measuring the parameter known as linewidth in a slightly different way. The largest differences are seen when comparing electrical measurements with any other technique because the width of the conducting part of the line may not be the same as the physical width. For example, if an electrical linewidth structure has regions of low conductance along the edges of the track or large sidewall angles then the ECD is likely to be lower than the result obtained from an optical measurement. The roughness of the sidewalls is also a factor as this will tend to reduce the conducting width of the line for electrical measurements while at the same time making it necessary to take the average of a number of optical measurements. Figure 4.1 illustrates the differences between a typical real conducting track and an idealised line.

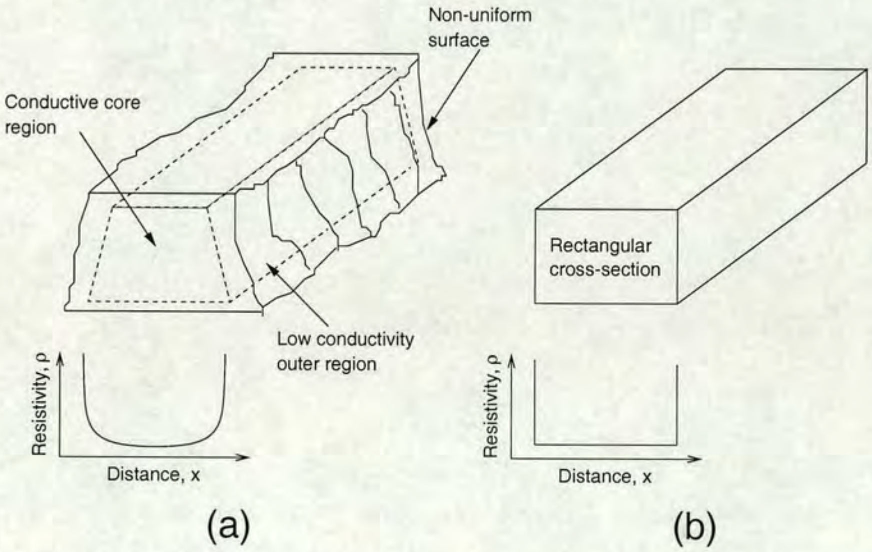


Figure 4.1: *(a) Schematic cross section through a conducting track with a trapezoid cross section with graph showing the effective resistivity across the width [90]. (b) Cross section through an ideal track with uniform resistivity and a rectangular cross section.*

The idealised line shown in figure 4.1 would not show significant methods divergence between electrical results and measurements made with any other instrument. This would make such a structure ideal for use as a reference artifact for the calibration of linewidth measurement systems.

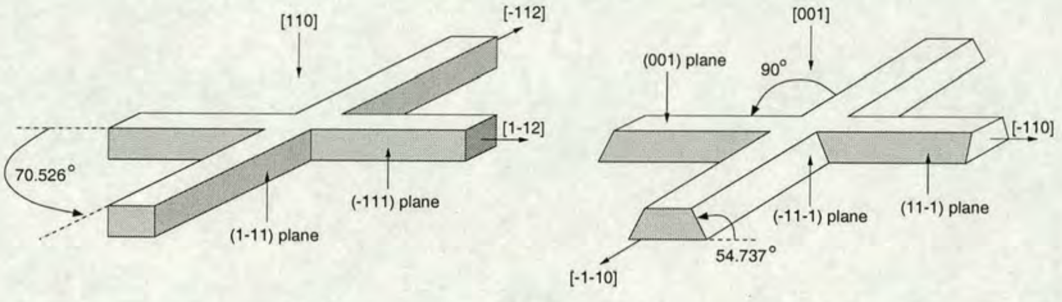
4.3 Mono-Crystalline Silicon Test Structures

The ideal linewidth reference artifact would have the following properties:

- Planar sidewalls.
- Uniform composition.
- Structure measurable by all common techniques (including electrical methods).
- Uniform geometry along feature length i.e., no sidewall roughness.

The National Institute of Standards in Technology (NIST) has developed a technology utilising lattice orientation specific, chemical etching of monocrystalline Silicon-On-Insulator (SOI) material which can provide structures which meet the conditions above [44, 80, 84, 124–130]. A wet etch consisting of a aqueous solution of KOH is commonly used in MicroElectroMechanical System (MEMS) fabrication to define structures in silicon which have {111}-planar surfaces. The etchant removes silicon with a {111}-orientated surface much more slowly than other crystal planes and so only these surfaces and those that are protected by a hard mask will be left after etching. This fabrication technique was chosen because the surfaces that remain have known orientations and are planar down to the level of the crystal lattice. Silicon-on-insulator starting material is used so that the electrically conducting features are isolated from each other.

The lattice orientation of the starting material limits the possible geometry of the structures that can be produced. If silicon with a (110) planar surface is used then structures patterned into the material will have {111} sidewalls which are at right angles to the surface. The resulting features will have a rectangular cross section similar to the idealised track in figure 4.1. However the intersection between two such lines would not be orthogonal because the {111} planes will be orientated to vectors which intersect at an angle $\phi = 70.526^\circ$. It is possible to make tracks which intersect at right angles by using silicon with a (100) planar surface but in this case the $\{111\}$ planar sidewalls will have a slope of 54.737° relative to the surface of the substrate. These two different implementations are illustrated in figure 4.2 [124].



(a) (b)

Figure 4.2: *(a) Schematic diagram showing the intersection of two lines fabricated in silicon where the surface is in the (110) crystal plane. (b) Schematic showing the intersection between two lines fabricated in silicon with a (100) surface orientation.*

The (110) implementation was preferred over the other type because the vertical sidewalls mean there can be little ambiguity in the position of the line edge when measurements are being made by optical methods or with a CD-SEM. Resistive electrical structures for the measurement of linewidth can be fabricated in this material but they will have an unusual geometry due to the wet etching process. The standard cross-bridge structure used to measure ECD consists of a four-terminal van der Pauw sheet resistance test structure in combination with a Kelvin bridge resistor [33, 34, 39, 40]. The most common type of van der Pauw structure used is the Greek cross [38], which is measured using the method described in section 2.1.4. The structures fabricated in (110) silicon have an asymmetrical geometry which complicates the measurement of R_S [44, 52]. In addition to this, facets with a $\{111\}$-planar surface are formed in the acute internal corners, as illustrated in figure 4.3.

The facet is a non-planarity in the structure which causes an error in the extracted sheet resistance. References [44] and [52] describe computer simulations of similar cross structures. The simulation results were used to develop an algorithm which will allow a more accurate value of R_S to be extracted.

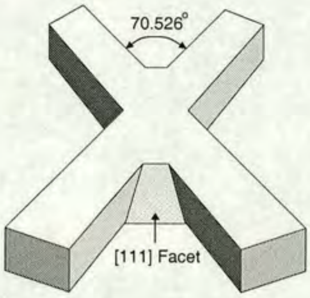


Figure 4.3: *Schematic diagram showing the facet which forms in internal corners of structures patterned into silicon with a (110) surface.*

Once the sheet resistance is known the electrical linewidth can be found using a four-terminal bridge structure. The method for the measurement of ECD with this structure is described in section 2.2.4. Bridge structures fabricated in (110) silicon have a number of attributes which complicate the linewidth extraction. Firstly the facets in the acute angles mean that the line shortening effect of the voltage taps is increased. However, it should be possible to extract a value for this effect and correct for it by using a test structure with dummy taps as described in section 2.2.4.1. The second issue peculiar to these structures is that the surfaces of the silicon tracks will be covered with a thin native oxide. Charge accumulates at the Si-SiO$_2$ interface during processing and can cause a depletion region on all sides of the track which reduces the conducting width. This issue will be examined later in the chapter where the effects of the oxide and the trapped charge on resistance measurements will be simulated. The final problem is a reduction in the width of the track caused by misalignment between the pattern printed in the photoresist and the silicon crystal lattice. This effect has more recently been turned into a useful method of fabricating silicon lines that are much narrower than the actual minimum critical dimension and this is described in reference [130]. References [80] and [127] describe an algorithm developed at NIST which allows the extraction of the linewidth and the line shortening effect from the sheet resistance and the results of measuring the resistance of a number of bridge structures of different lengths.

The most recent development of these monocrystalline structures is the use of a high resolution Transmission Electron Microscope (TEM) to measure the linewidth [131–133]. This is done by counting the number of lattice plane fringes visible in a phase contrast image taken across the track. The measurement uncertainty was calculated to be 2.5nm for a track with a nominal linewidth of 600nm. A combination of electrical and TEM measurements will allow the calibration of linewidth reference features down to this level of uncertainty.

It was mentioned previously in this section that oxide on the silicon surfaces can trap charge and lead to a depletion region which can reduce the electrical width of a track. There was a concern at NIST because significant methods divergences were still being observed between electrical and physical measurements. The width of the depletion region, and therefore the change in the linewidth, depends on the doping of the silicon and the temperature [126]. This chapter takes this work further and quantifies the effects of geometry, doping, temperature, measurement voltage and surface charge (Q_f) on the conductivity of a simulated mono-crystalline silicon track. The results can then be used to determine how these factors affect the extracted value of electrical linewidth.

4.4 Simulation of Mono-Crystalline Silicon Track

The Avant! three-dimensional device simulator Davinci (see section A.3.3) was used, in conjunction with TWB (see section A.3.1), to model current flow along an n-type, uniformly doped silicon track. The simulated track was surrounded by silicon dioxide which allowed the surface interface charge, Q_f, to be specified. Electrodes were positioned at the ends of the track and and different voltages were applied. The track resistance was calculated from the applied voltage and the resulting current. The specifications of the structure used in these simulations are given in table 4.1.

Factor	Value
Length	9.0μm
Width	3.0μm
Height	3.0μm
Q_f	10^{10}cm^{-2}
Doping Conc.	10^{14}cm^{-3}
Temperature	300K
Voltage	1.0V

Table 4.1: *Reference track simulation parameters.*

Figure 4.4 is a cross section through the simulated track showing the electron concentration. It can be observed that the surface charge Q_f results in a variation of the concentration of charge carriers and a non-uniform resistivity.

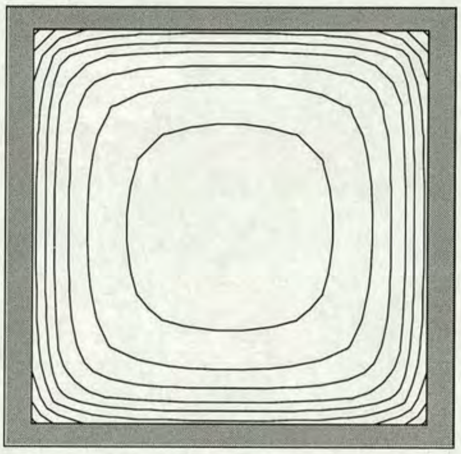


Figure 4.4: *Variation in electron concentration for a cross-section through the middle of the track (contours plotted $10^{14}cm^{-3}$ to $10^{15}cm^{-3}$, in steps of $10^{14}cm^{-3}$).*

The effects of changing the parameters given in table 4.1 have been investigated through a series of simulations. Firstly the effects of changing the length and width of the silicon bar were examined and the results can be seen in figures 4.5 and 4.6. The resistance of the track varies linearly with the length, as would be expected, but this is not the case where the width is changed. The equivalent sheet resistance of the silicon goes down as the width is reduced because the resistivity is non-uniform across the width of the bar. Figure 4.6 includes a straight line which is a linear fit to the results of the simulations of the widest tracks where $W \geq 3\mu$m.

The second attribute that was investigated was the temperature. The results of simulations where the material temperature was varied from 200 to 500K can be seen in figure 4.7. As would be expected the resistance stays constant for low temperatures but as it increases above 400K intrinsic carriers begin to increase the carrier concentration and the resistance falls.

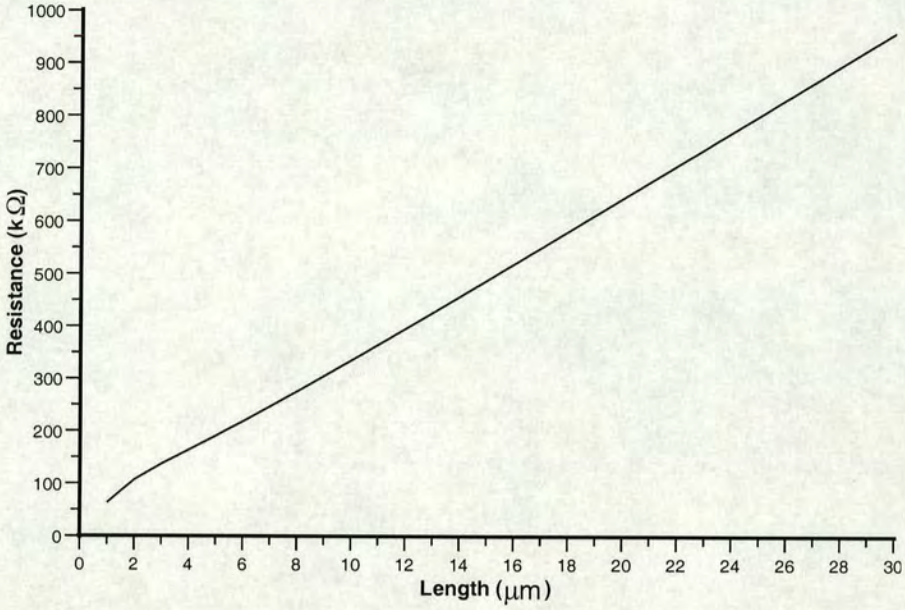


Figure 4.5: *Resistance versus silicon track length.*

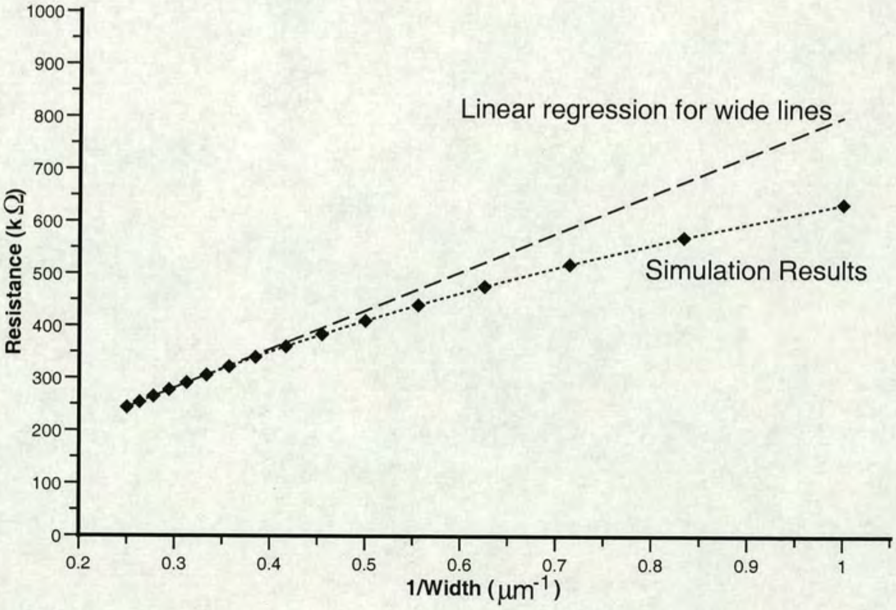


Figure 4.6: *Resistance versus the reciprocal of silicon track width.*

In the next set of simulations the surface charge Q_f was varied from 0 to 10^{11}cm^{-2} for two different levels of doping concentration, 10^{14}cm^{-3} and 10^{19}cm^{-3}. The results can be seen in figure 4.8 and they indicate that the effects of the fixed charge Q_f can be minimised by using starting material which is heavily doped. It should be

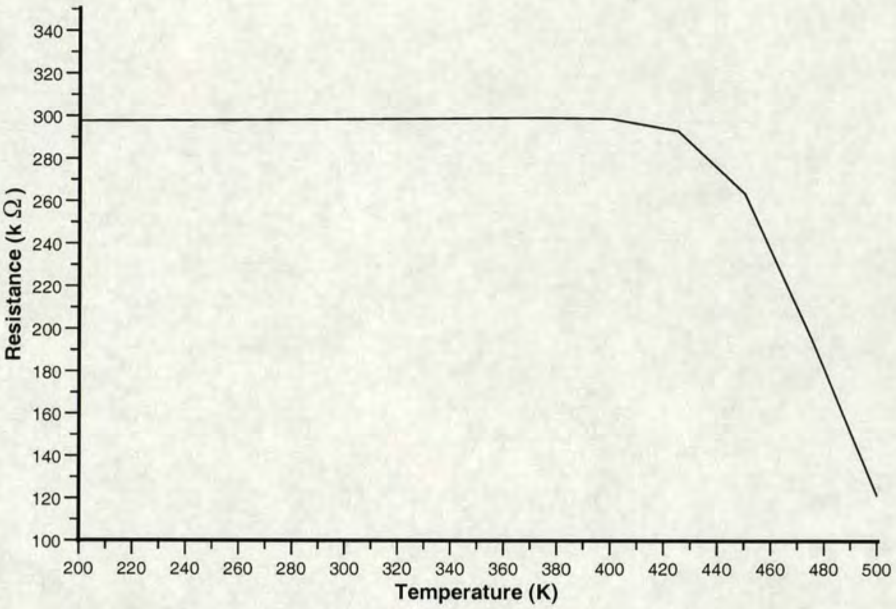
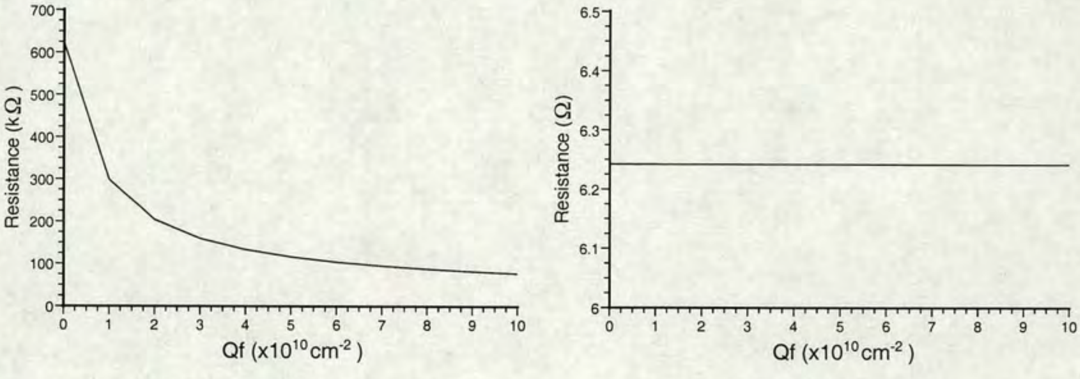


Figure 4.7: *Resistance versus temperature.*

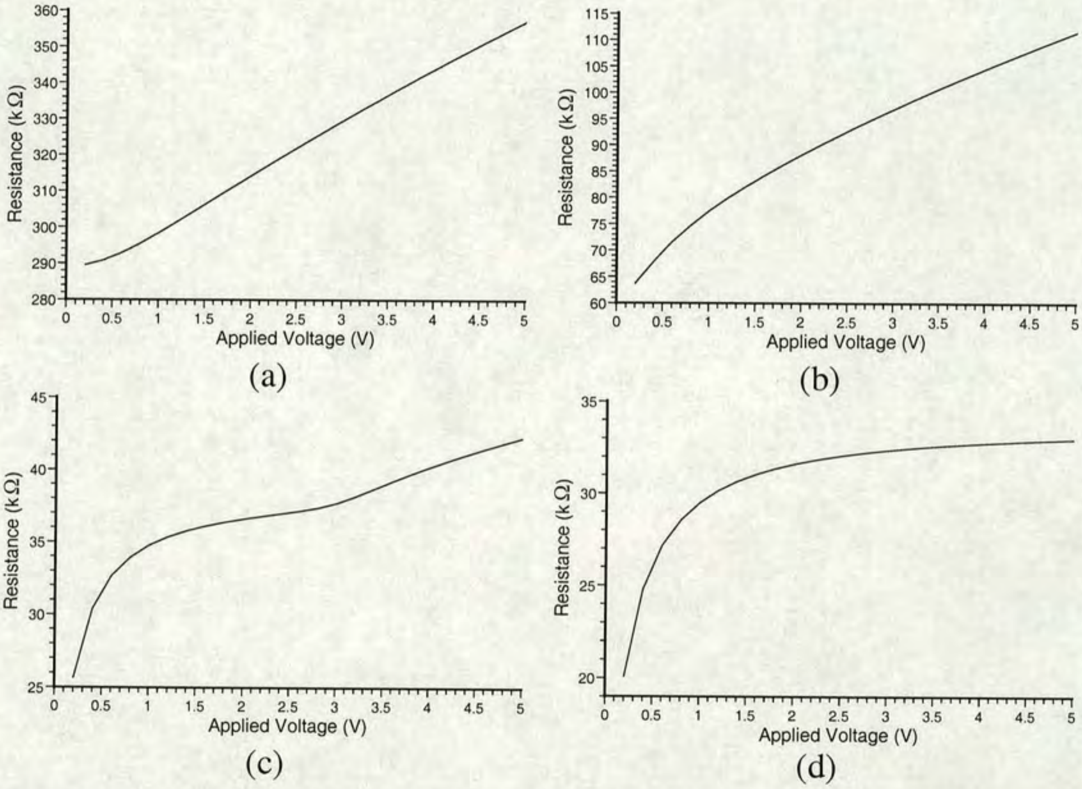
noted that if low resistivity material is used the voltage measurements must be made with high resolution instruments. This will be more of a problem for sheet resistance measurements on SOI structures because the asymmetry of a Greek cross made in this material and the presence of the facet mean that the voltage measurements in the acute orientation are already very small [52].



(a) (b)

Figure 4.8: *(a) Track resistance against Q_f for a silicon bar with a doping concentration of $10^{14}cm^{-3}$. (b) Track resistance against Q_f for a silicon bar with a doping concentration of $10^{19}cm^{-3}$.*

The final set of simulations which were performed investigated the effect of changing the measurement voltage used to extract the resistance. If the material resistivity is unaffected by the voltage the resistance should not change but the results presented in figure 4.9 show that this is not the case. The effect of the voltage is strongly dependent on the level of fixed charge and four sets of simulations have been performed with Q_f varying from 10^{10}cm^{-2} to 10^{13}cm^{-2}.



(a) (b)

(c) (d)

Figure 4.9: *Simulated resistance against applied voltage for silicon bars with the following values of* Q_f*: (a)* $10^{10}cm^{-2}$*; (b)* $10^{11}cm^{-2}$*; (c)* $10^{12}cm^{-2}$*; (d)* $10^{13}cm^{-2}$.

The effects of changing the measurement voltage can be minimised in the same way as the effects of Q_f by increasing the dopant concentration of the material. This is very important because in a typical measurement setup it is the force current which is set and the measurement voltage will depend on the resistance. Figure 4.10 shows the results of a simulation where the doping concentration was set to 10^{19}cm^{-3} ($Q_f = 10^{13}\text{cm}^{-2}$) and the applied voltage was swept from 0.2 to 5V.

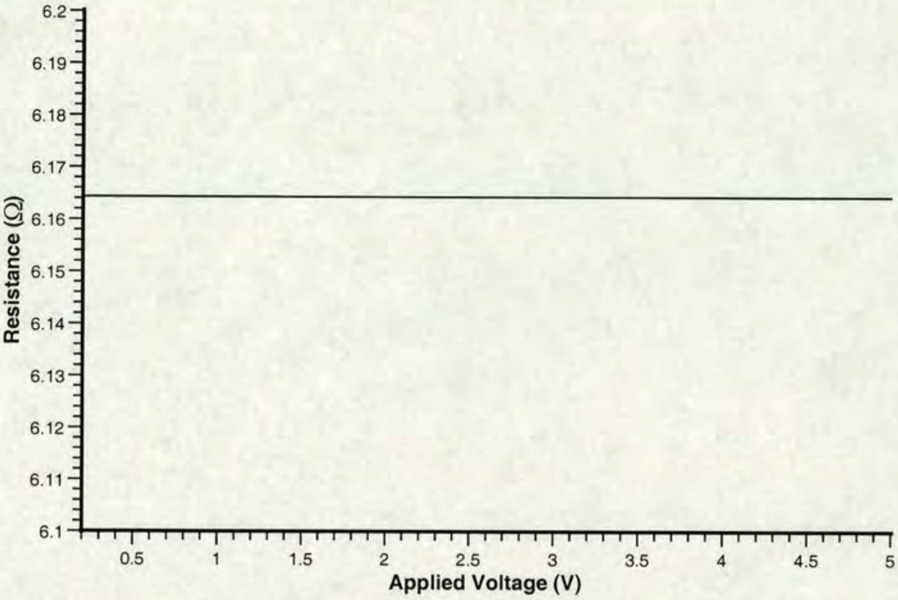


Figure 4.10: *Simulated resistance versus applied voltage for silicon bar with high doping concentration.*

4.5 Simulation of (110) Silicon Greek Cross

Davinci and TWB were used again to model current flow in three dimensions in a Greek cross with similar geometry to the monocrystalline silicon structures described in section 4.3. Figure 4.11 shows the top surface (XY plane) of the 3D structure, which measures approximately $14 \times 15\mu$m. The thickness of the cross structure being simulated is 1μm in the Z direction, with a 0.2μm layer of oxide underneath. On the bottom, covering the entire back of the structure, is a gate electrode which can be biased as required.

The grid generated for this structure has a total of 23,611 nodes and as the maximum number of nodes available within the Davinci simulator is 30,000 this gave little opportunity to significantly increase the mesh density. The mesh available for 3D simulations in Davinci is limited to an array of right angled triangular prismatic elements. This means that obtaining a 70° angle between the arms of the cross puts a further limit on exactly how the grid can be constructed and modified. The 70° angle was achieved by setting the ratio between the X and Y grid pitches to X= 0.1μm and Y= 0.275μm resulting in an angle of approximately $70.017°$. The node spacing in the Z direction was set to 0.2μm making 5 grid layers in the silicon cross plus one for the

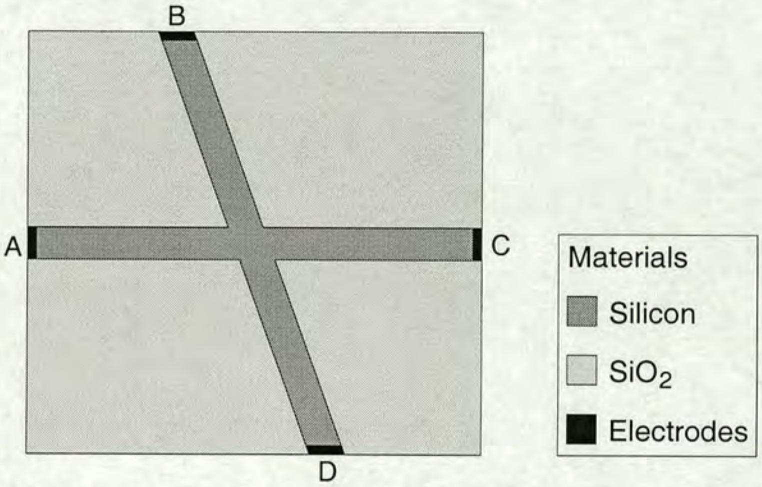


Figure 4.11: *Plan view of the simulated Greek cross without facets and with the arms at 70° to each other.*

layer of oxide mentioned above.

As well as this basic cross structure, a cross with facets in the acute angles was also simulated. Due to limitations imposed by the grid elements available in Davinci it is not possible to construct a facet with a smooth surface. As a result it has been approximated by a series of 5 stepped levels, as can be seen in figure 4.12. This also shows that that the edge of each layer of the facet has to be stepped to fit the grid in the XY plane.

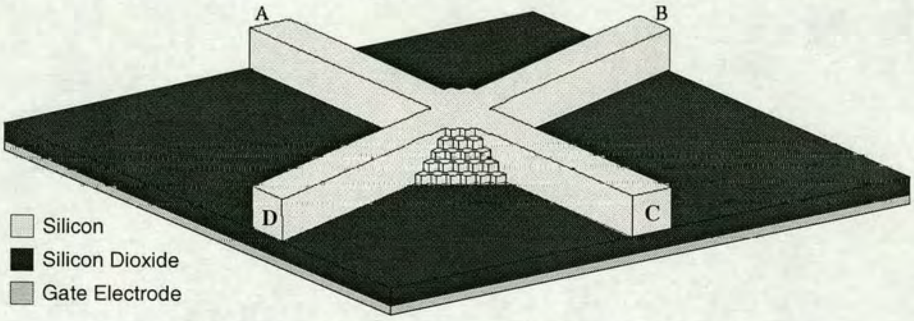


Figure 4.12: *Schematic 3D view of the Greek cross structure with facets in the acute angles between the arms.*

The method of extracting the sheet resistance from a four-terminal resistor requires four Kelvin measurements made at different orientations [37]. In each case a current I is forced between two adjacent terminals while the voltage drop V between the other two terminals is measured. The sheet resistance can then be calculated using the methods described in section 2.1.4 and, in particular, equation (2.15). It is clear that the unique geometry of these structures means they do not have 90° symmetry and that correction will have to be applied to the raw results.

The original paper published on this subject presented the results of simulations using Greek cross structures with a uniform doping concentration of $6.244 \times 10^{14}\text{cm}^{-3}$ (see reference [134]). This very low level of doping led to problems with the simulations. The most apparent of these being that the measurements with forward and backward force current direction were not equal, i.e. $R(+0^\circ) \neq R(-0^\circ)$. Further simulations, using higher doping concentrations, have been performed since the paper was published and the results obtained from these form the basis of this section.

The first new set of simulations were performed using the same cross structures described above but without a gate electrode. The sheet resistance extracted from a cross structure without the stepped facets was $12.93\text{k}\Omega/\Box$ compared with $22.42\text{k}\Omega/\Box$ for a cross with facets. The conducting material had been set up as N-type silicon with a uniform doping concentration of $6.244 \times 10^{15}\text{cm}^{-3}$. Simulations of simple silicon bars similar to those described in section 4.4 have shown that this level of doping gives a sheet resistance of $10\text{k}\Omega/\Box$ for a thickness of $1\mu\text{m}$. The extracted values of R_S given above are strongly affected by the asymmetry of these structures, especially in the case of the cross with the facets in the acute corners. Reference [37] defines the asymmetry factor F_A and suggests that no correction of the sheet resistance is required if $F_A \leq 0.1074$. The structure without facets has $F_A = 1.48$ while it is even greater for the cross with facets where $F_A = 1.93$. If a value of the correction factor f is calculated for each set of results, corrected sheet resistances can be obtained. These are R_S(no facet)$= 9.95\text{k}\Omega/\Box$ and R_S(facet)$= 10.13\text{k}\Omega/\Box$. These results illustrate the error introduced by the facets. The next step is to simulate the same structures with different biases placed on the gate electrode. The results are presented separately for each of the cross structures.

4.5.1 SOI Greek Cross Without {111} Facet

Twenty one different gate electrode bias points ranging from -5 to +5 volt were used in these simulations. Measurements were made at each gate bias point with a measurement force current of 1μA. The results of extracting sheet resistances from the simulated measurement data can be seen in figure 4.13. In addition to the sheet resistance results which have had the asymmetry correction factor f applied to them this graph also includes the raw, uncorrected results.

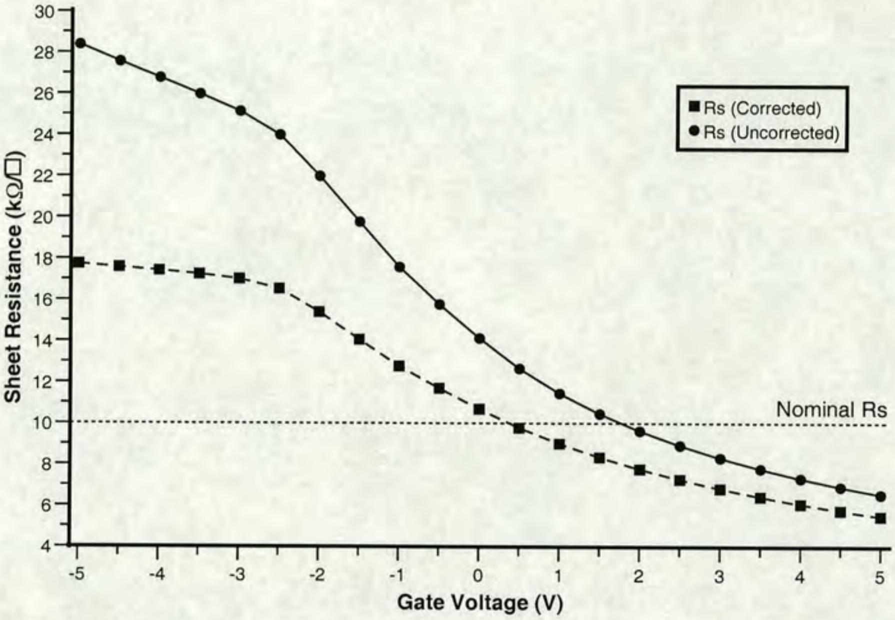
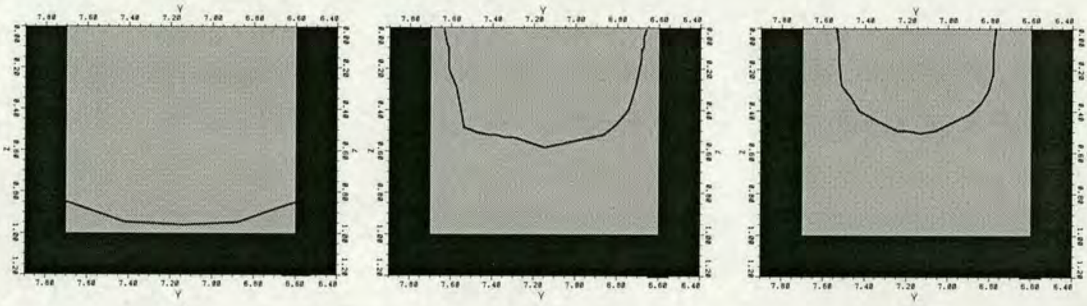


Figure 4.13: *Extracted sheet resistance against gate electrode voltage.*

Applying a positive voltage to the gate electrode causes accumulation under the gate, which lowers the resistivity of the silicon. This is similar to the effect illustrated for the silicon bar in figure 4.8(a) where the resistance decreases as the amount of surface charge increases. It should be remembered that, in addition to the voltage on the gate, a voltage is also applied to one of the terminals in order to force the measurement current. For example, in order to measure $R(+0°)$ terminal B (see figure 4.12) is grounded while there is a positive voltage, which varies from 61 to 247mV depending on the gate bias, on terminal A. This means that the voltage across the oxide, and therefore the accumulation charge, will vary with position. When the gate voltage is 0V there will be some depletion of the silicon around terminal A where the voltage drop across the oxide is negative with respect to the gate electrode. This is the reason why the sheet resistance is higher for this gate bias than the value extracted using the simulated structure without a gate electrode.

As the gate bias is decreased the sheet resistance increases more and more steeply until the gate voltage reaches -2.5V. This is the point at which the depletion region in the silicon structure reaches its maximum depth. At higher negative voltages the silicon closest to the gate electrode becomes inverted but this inverted region has no connection to the terminals and plays no part in current flow. High electrical fields at the edges of the cross arms cause the depletion region to extend towards the surface narrowing the tracks. Figure 4.14 shows how the boundary of the depletion region changes as the gate bias is made more negative.



(a) (b) (c)

Figure 4.14: *Cross sections through one arm of the simulated Greek cross showing the boundary of the depletion region caused by a gate bias of: (a) 0V; (b) -2.5V; (c) -5V.*

This change in the depletion region also changes the shape of the central part of the cross and because it is here that the resistance is effectively being measured this leads to some interesting results. Figure 4.15 shows the extent of the depletion region with a gate voltage of -5V, while figure 4.16 gives the results of the individual Kelvin measurements at the acute and obtuse orientations with negative gate voltages.

As the gate voltage is reduced from 0v to -2.5V the depth of the depletion region is increasing and this effect dominates the results so both the acute and obtuse measurements increase steadily. At -2.5V the depletion region reaches its maximum depth but as figures 4.14 and 4.15 show the shape of the conducting part of the cross changes. Effectively the acute angle becomes more acute which is why the values of V/I measured at this orientation are reduced. The opposite effect is observed with the obtuse measurements where the resistance measured continues to increase. The obtuse results are between 10 and 20 times larger than the acute results. This means they dominate the sheet resistance calculated from the average of the four measurements and this is clear from the "Uncorrected" values in figure 4.13. If these results are

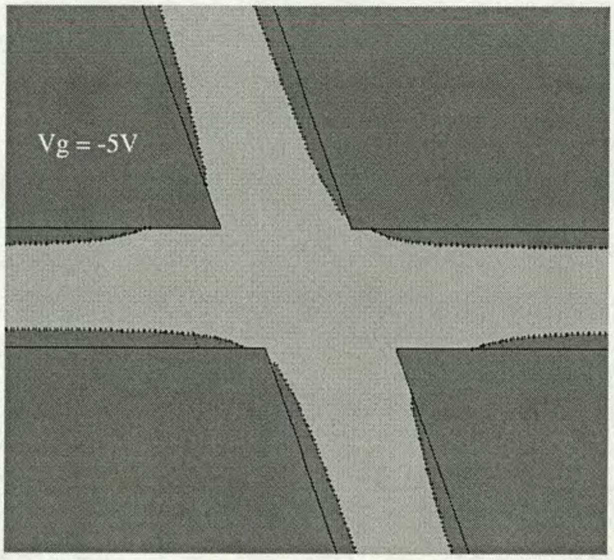
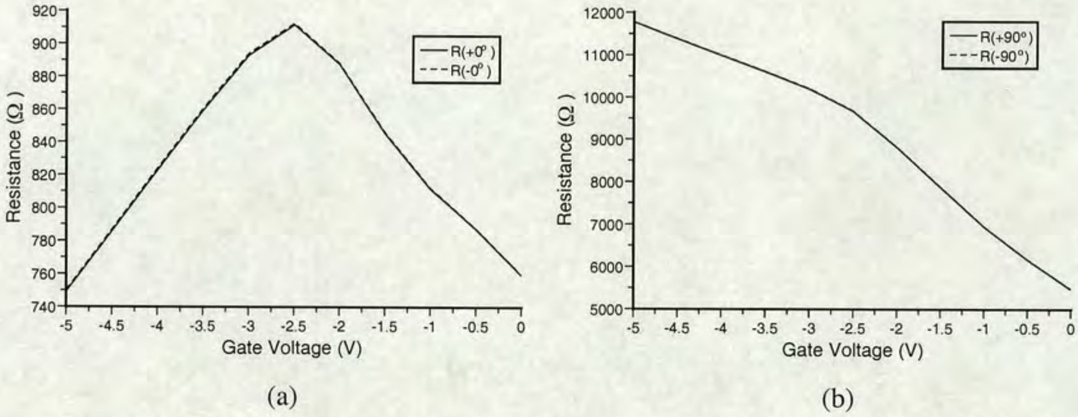


Figure 4.15: *Plan view of a simulated silicon Greek cross showing how depletion changes the effective geometry of the structure.*

corrected for the asymmetry of the structure then it is clear that once the depletion region reaches a maximum depth the sheet resistance also reaches a maximum value.



(a) (b)

Figure 4.16: *(a) Resistance against gate voltage showing the results of the simulations using the acute measurement orientations. (b) Resistance against gate voltage showing the results of the simulations using the obtuse orientations.*

4.5.2 SOI Greek Cross With {111} Facet

The next step was to perform similar simulations using the structure with the stepped facets in the acute corners of the cross. The results of extracting sheet resistance from this simulated Greek cross can be seen in figure 4.17.

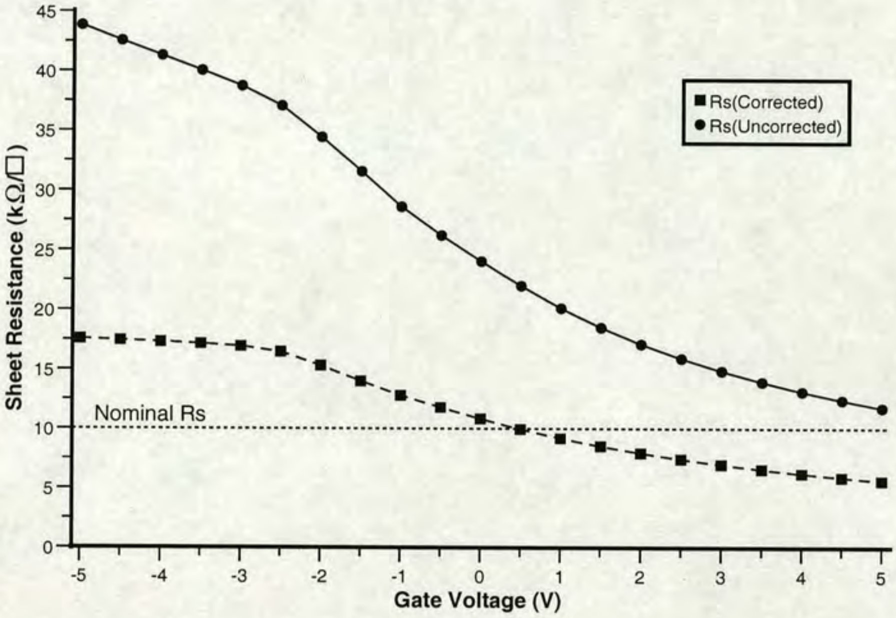


Figure 4.17: *Extracted sheet resistance against gate electrode voltage.*

The addition of the facet to the structure increases the asymmetry factor which means that the uncorrected results are much higher for this structure. However if these results are corrected then they are much closer to the results from the structure without a facet. The difference in the apparent sheet resistance also depends upon the bias on the gate electrode because the geometry of the cross is affected by the depletion region. The maximum difference between the two sets of results is 2% which could lead to a similar error in the linewidth measured using this value of sheet resistance. The increase in the asymmetry of the Greek cross due to the facet means that the resistances measured at the acute orientations are lower than for the structure with no facet while the obtuse measurements are greater. However, the results obtained at negative gate voltages follow similar trends, with a discontinuity at a voltage of -2.5V where the depletion region under the gate electrode reaches a maximum depth, as can be seen in figure 4.18

4.5.3 Effects of Fixed Charge and Structures with Highly Doped Silicon

The Greek cross structures which have been simulated so far do not include fixed charge on the silicon boundaries. This should have a similar effect on the measured sheet

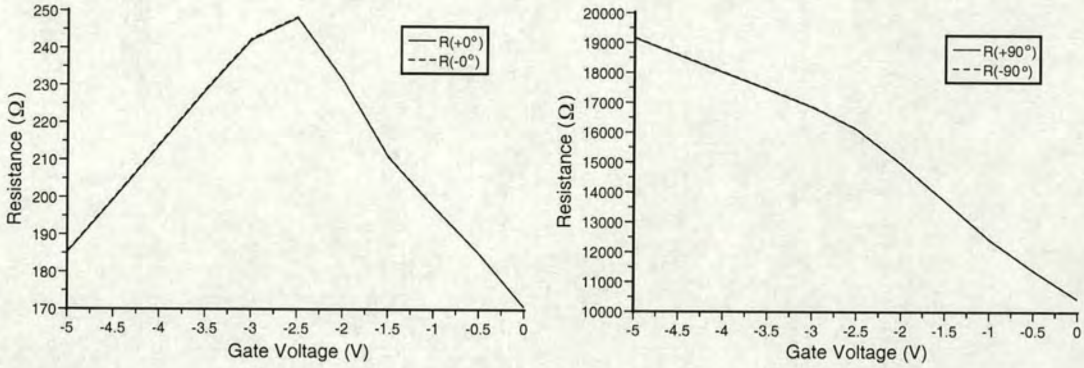


Figure 4.18: *(a) Resistance against gate voltage showing the results of the simulations using the acute measurement orientations. (b) Resistance against gate voltage showing the results of the simulations using the obtuse orientations.*

resistance as changing the voltage on the gate electrode. Simulations were performed using structures with a uniform donor concentration of $6.242 \times 10^{15}\text{cm}^{-3}$ and fixed charges ranging from 0 to 10^{12}cm^{-3}. The results can be seen in figure 4.19.

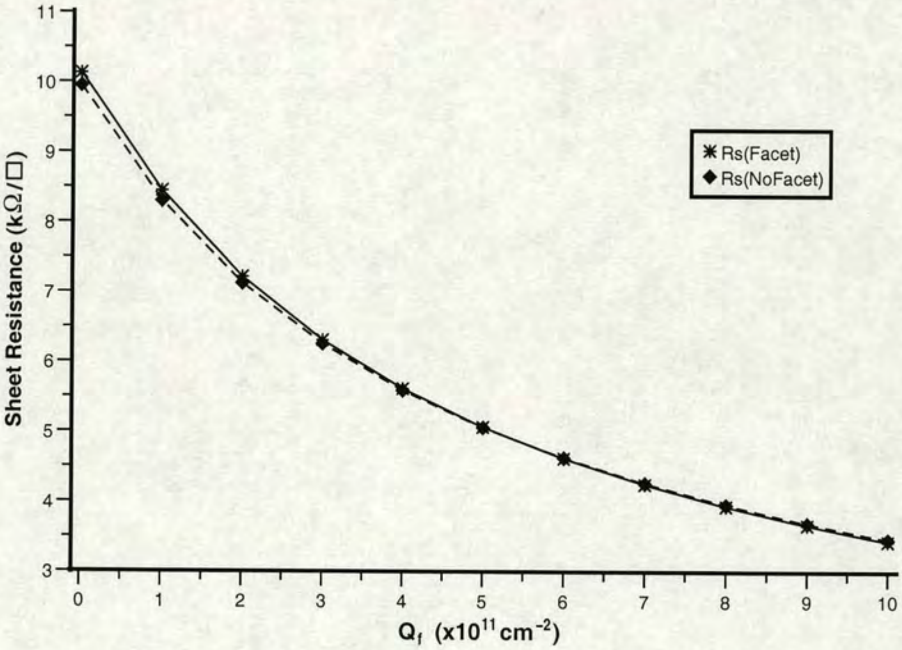


Figure 4.19: *Extracted sheet resistance against fixed charge. The results have been corrected for the asymmetry of the test structures.*

The results are similar to those observed for positive gate voltages in sections 4.5.1 and 4.5.2. The positive charge on the boundary between the silicon and the oxide on the underside of the cross and between the silicon and air on the sides of the features lowers the resistance. If the sheet resistance measured from such a structure was then used in the calculation of the linewidth of a bridge resistor it is likely that there would be significant errors.

The simulations of a silicon bar presented in section 4.4 indicate that the effects of fixed charge can be reduced by heavily doping the silicon. This should also reduce the effects of biasing the gate electrode on these Greek cross structures. Further simulations of structures with doping concentrations of $6.242 \times 10^{17}\text{cm}^{-3}$ and $6.242 \times 10^{19}\text{cm}^{-3}$ have been performed. These levels of doping give nominal sheet resistances of $100\Omega/\Box$ and $1\Omega/\Box$ respectively. The results, which have been corrected for asymmetry, can be seen in figure 4.20.

In the less highly doped structures described in previous sections the sheet resistance varies by about 120% of the nominal value as the gate voltage is swept from -5V to +5V. This compares with a variation of 1.7% for the structures with a doping concentration of $6.242 \times 10^{17}\text{cm}^{-3}$ and 0.017% for the more highly doped crosses. In the previous section it was stated that the difference between the results from the faceted and non-faceted structures with light doping varied with the bias on the gate. This is not observed for these more heavily doped structures where the difference is almost constant at about 1.7 - 1.8%. This is the systematic error introduced by the facet and is similar to that described in reference [44].

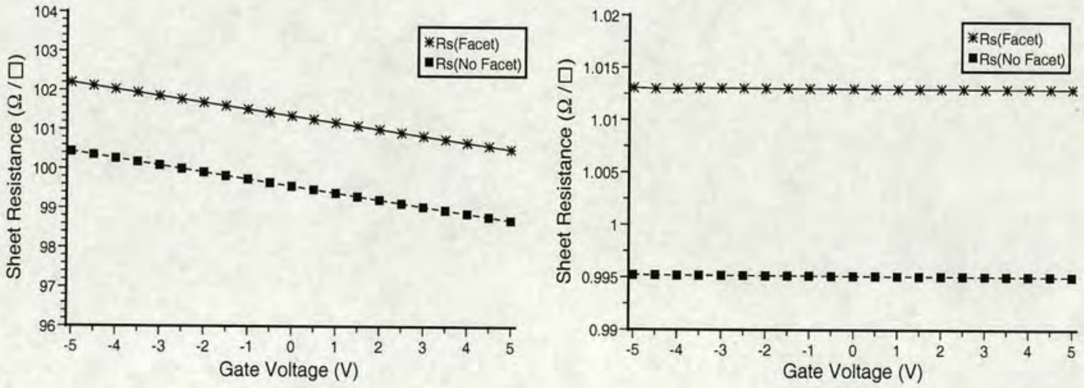


Figure 4.20: *Corrected sheet resistance against gate voltage for silicon crosses with n-type doping concentrations of (a)* $6.242 \times 10^{17}cm^{-3}$ *and (b)* $6.242 \times 10^{19}cm^{-3}$.

4.6 Conclusions

Section 4.4 described simulations which demonstrated how charge on the surface of mono-crystalline silicon tracks can affect the measurement of electrical critical dimension. The surface charge Q_f has an effect on the variation of the resistance of the track with width or measurement voltage as can be seen from figures 4.6 and 4.9. The variation of the resistance associated with the surface charge can help to explain divergence between physical and electrical measurement methods used with these structures [127]. It was found that heavily doping the silicon starting material will reduce the effect of the surface charge on the measurements.

Simulations were also performed using structures designed to model the operation of the Greek cross sheet resistors fabricated in (110) silicon by NIST. The simulation grids include a gate electrode separated from the silicon cross by a thin layer of insulation. This electrode allows the effect of biasing the substrate of an SOI wafer on the electrical performance of the test structures to be examined. As the bias on the gate electrode is made more negative the silicon under the gate is depleted and the sheet resistance increases. At a certain bias, -2.5V for this doping level, the depletion region reaches its maximum depth and the sheet resistance should reach a maximum value. This is what happens to the corrected value of R_S as can be seen in figures 4.13 and 4.17. However looking more closely at the individual figures of $R(\pm 0°)$ and $R(\pm 90°)$ it is clear that something more complicated is occurring around the centre of the cross. Once the maximum depletion thickness is reached, the depletion region tends to narrow the arms while changing the shape of the centre of the cross. The results from the obtuse measurement orientation continue to increase as the gate bias becomes more negative while the acute measurement results begin to decrease. This suggests that depletion of the silicon alters the effective shape of the cross making it more asymmetrical.

The results of simulations of Greek crosses without gate electrodes have revealed that the non-linearity introduced by the facet in the acute corners leads to a difference of about 1.8% in the extracted sheet resistance. The effect of the facet can be reduced by using SOI starting material with a thinner silicon conducting layer on top. The structures which result will have smaller facets but will be more difficult to measure by SEM or other methods [128]. Another possibility is the use of the measurement algorithm mentioned in section 4.3 which should return an accurate value of R_S taking the facet into account [52].

Further simulations have shown that surface charge at the interface between the silicon and the oxide has a similar effect to changing the bias on the gate electrode. Both of these experiments show that these relatively high resistance, low doped structures are strongly affected by processing and measurement conditions. The results from the simulations of the silicon bar have shown that increasing the doping of the silicon will decrease the effect of charging or measurement bias on the resistivity of the material. Simulations using structures with higher doping concentrations were performed and the results showed that the extracted sheet resistance was far less dependent on the gate voltage. The variation in R_S for a structure with an n-type doping level of $6.242 \times 10^{19}\mathrm{cm}^{-3}$ was only 0.017% for a gate bias ranging from -5 to +5V. The only possible problem with this option is that lowering the resistivity will also mean that the measurement accuracy needs to increase. For example, the lowest V/I measurement from these simulations was 0.016Ω measured in the acute orientation of a structure with a facet. The current forced was 1μA so the differential voltage between the two measurement terminals is only 0.016μV. Therefore, measurements of real structures with similar resistivities would require voltmeters with sub-μV resolution. The measurement current could be increased but this can lead to joule heating and current crowding which will affect the measurement accuracy.

The results presented in this chapter have shown that the adverse effects of surface interface charge and substrate bias on the operation of single crystal silicon test structures can be avoided or ameliorated through the careful choice of doping level. This has led to a change at NIST in the starting material used to fabricate these structures. The most recently published results were obtained from structures fabricated in silicon with a p-type (Boron) doping concentration of around $2 \times 10^{19}\mathrm{cm}^{-3}$ [133] whereas initial samples had lower doping levels. For example, in reference [126] the starting material had a doping level of approximately $5 \times 10^{17}\mathrm{cm}^{-3}$.

Chapter 5

Electrical Linewidth Test Structures for Advanced Lithography

5.1 Introduction

Economic considerations mean that optical lithography is still the first choice for high volume production of Ultra Large-Scale Integrated (ULSI) circuits. As the drive towards smaller and smaller feature sizes continues, techniques which allow the printing of features much smaller than the wavelength of the exposure light have become very important [135]. The resolution of a photolithographic system can be enhanced by the use of techniques such as off-axis illumination and Phase Shifting Masks (PSM) to allow the imaging of sub-wavelength features [136]. However, optical proximity effects which distort the final pattern become more pronounced in this region of operation and this can require the use of Optical Proximity Correction (OPC) to achieve a working circuit [137].

Masks which utilise OPC and phase shifting techniques are more complex to manufacture than conventional masks and so the ability to test and characterise the mask is very important. Most schemes for mask metrology require either optical testing [58] or, as geometries reduce, measurement with a Critical Dimension Scanning Electron Microscope (CD-SEM) system [72]. Both of these techniques are expensive in terms of equipment and testing costs. A less costly option would be to use electrical test structures such as the cross bridge linewidth structure. Although methods divergence exists between ECD measurements and other metrology techniques, electrical measurements tend to have superior repeatability [124]. Chapter 4 describes the use of electrical linewidth structures as CD calibration reference materials in more detail.

This chapter begins by examining the use of resistive electrical test structures for alternating phase shifting mask metrology. Then, in the second half of the chapter, simulation results are presented from a study of the effects of OPC on the function of cross-bridge linewidth structures.

5.2 Test Structures for Alternating Aperture Phase Shifting Masks

5.2.1 Introduction to Phase Shifting Masks

The Alternating aperture Phase Shifting Mask (AltPSM) is one of the earliest resolution enhancing techniques and was first described by Levenson et al. [138]. Figure 5.1(a) illustrates the problems encountered when trying to print small features with a binary or transmission mask. For the images of the two apertures to be resolved the light intensity at the wafer surface must fall between the two main peaks. Diffraction means that the light passing through each aperture spreads and constructive interference between the two images leads to a significant peak in an area which should be dark. Figure 5.1(b) illustrates the results of using a phase shifting mask to print features of the same dimensions as the binary mask. The 180° phase shifting elements are created by etching the mask substrate to a depth equivalent to half the wavelength λ of the light source being used in the projection tool. The result is that there is destructive interference between the two apertures which minimises the intensity in this region and allows the features to be successfully resolved.

Binary and phase shift masks have previously been used to print Electrical Critical Dimension (ECD) test structures as described in reference [139]. This study was concerned with using the printed structures to characterise the photolithographic process and examine exposure latitude, depth of focus and proximity effects in different PSM schemes. The work presented in this section takes the concept a step further by placing test structures on the mask so they can be measured electrically as in reference [100]. This will provide information about the mask making process capability and will highlight issues such as proximity induced errors. The results from the on-mask test structures can also be compared with measurements made on similar structures which will be printed using the photomask. This will provide information

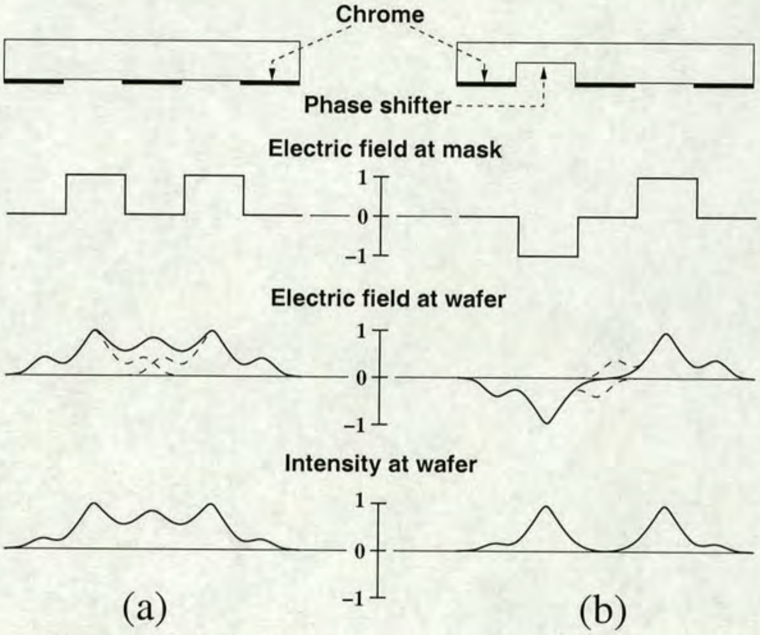


Figure 5.1: *Comparison of the results of image projection from (a) a binary photomask and (b) a similar mask where a* 180° *phase shifter has been etched in one aperture [138].*

about the Mask Error Enhancement Factor (MEEF) which is defined as [140]

$$MEEF = M\frac{\Delta W_{resist}}{\Delta W_{mask}} \tag{5.1}$$

Where M is the magnification of the projection system, ΔW_{mask} is the deviation of the mask dimension away from a nominal value and ΔW_{resist} is the resultant error in the resist CD when the mask is printed. If $MEEF = 1$ then the dimensional errors on the mask will simply be divided by the magnification of the exposure tool. Unfortunately this is not the case when printing sub-wavelength feature sizes as the MEEF is typically greater than unity [140, 141]. If $MEEF > 1$ then CD errors will be proportionately larger on the wafer than on the mask.

5.2.2 PSM Test Structures

The standard test structure used to measure the electrical critical dimension of a conducting track is the cross-bridge linewidth structure [45]. The cross-bridge structure consists of two different sections. The first is a Greek cross [38] which is a type of van der Pauw, sheet resistance test structure [33, 34]. The second part is a bridge resistor which is used, in conjunction with the value of R_S obtained from the Greek cross, to extract the electrical linewidth [39]. See chapter 2 for the methods used to measure R_S and ECD with these test structures.

Cross-bridge test structures which were developed to investigate metal damascene interconnect processes have been adapted for use with alternating phase shifting masks. In the "dense" test structures the electrically measured line is surrounded by floating lines and phase shifting regions in a similar way to the AltPSM test sites described in reference [139]. This is illustrated in figure 5.2.

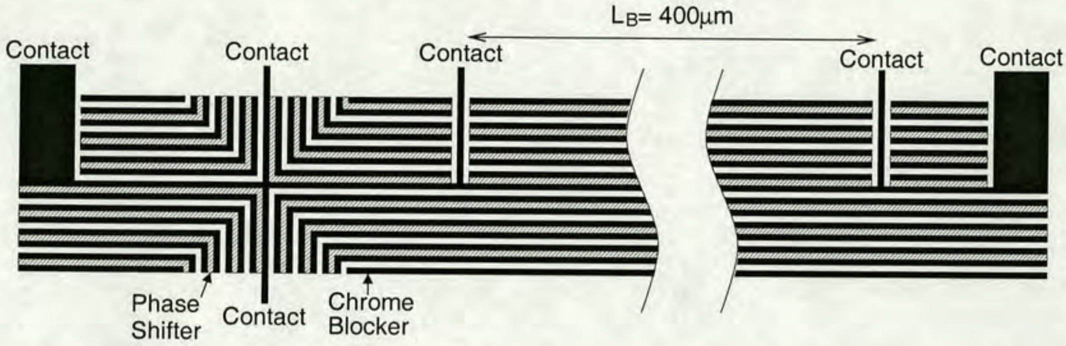


Figure 5.2: *Section of PSM test structure layout. The black areas are the chrome blockers while the shaded areas are regions of* $180°$ *phase shift. This is a structure with a linewidth of* $1.5\mu m$ *and a line to space ratio of 1:1.*

The test structure layout contains test structures with on mask linewidths of 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2 and 1.5μm. Bridge structures with line to space ratios of 1:1, 1:1.5, 1:2, 1:3, 1:5 and 1:10 were designed for each of these feature sizes. There are two sets of dense structures with different arrangements of the dummy lines around the Greek cross. The first set resemble figure 5.2, where the floating lines follow the shape of the cross, and these will be referred to as "L-Type" structures. In the second set the unmeasured lines run up to the vertical contact arms of the cross and stop short as they do in the bridge section of the structure. This set will be referred to as "I-Type" test structures. The full layout is a 14×10 array of test structures with probe pads which can be probed on-mask using a standard 2×n probe card. This includes two "isolated" linewidth structures, with no dummy features, at each feature size. A second layout has also been designed where the probe pads are scaled so that when the structures are printed using a $4\times$ exposure tool the pads will be the same size as those designed for on-mask measurement. Figure 5.3 shows lines with a CD of 91nm which were printed in photoresist using the 0.4μm features on the photomask.

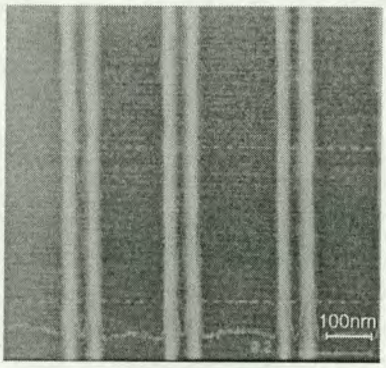


Figure 5.3: *SEM image of 91nm wide lines printed using a S202 scanner (0.6NA) and the phase shifting mask used in this study.*

The layout with the large pads has been repeated three times on the mask, once with the phase shifting elements removed to give binary structures. The version with the small pads for on-mask testing is repeated 24 times in three blocks of 8 on the mask where one set of 8 contains binary structures. A picture of the mask can be seen in figure 5.4 along with a closeup of the layout for on-mask probing.

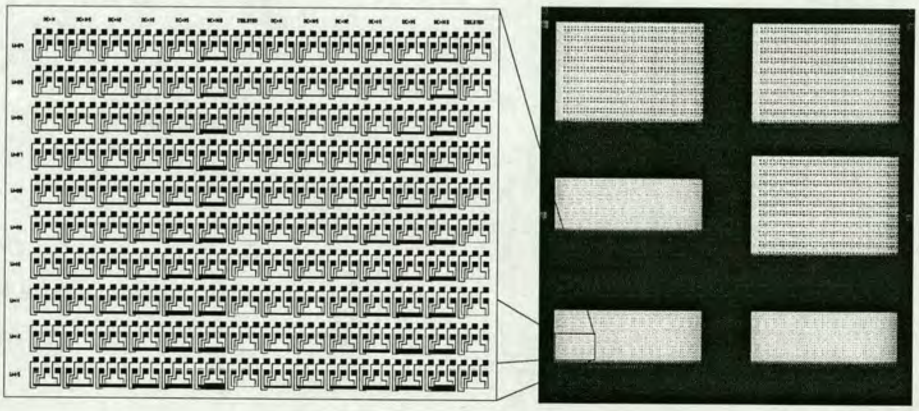


Figure 5.4: *Photograph of the actual phase shifting mask with a close up view of the layout of one of the sets of on-mask test structures.*

5.2.3 Sheet Resistance Measurements

The Anti-Reflective (AR) coating of chromium oxide over the chromium features on the mask presents a challenge when electrically probing the structures [142]. Initial attempts to use a standard 2×4 probe card designed to probe aluminium pads were unable to make reliable electrical contact because the AR coating was too hard for the probe tips to penetrate. However, it was found that steerable probes on a manual probe station were able to contact the chromium. It should be noted that considerable force was required to make contact but no scratching of the pads was observed. Sheet resistance measurements were made on the Greek cross section of one of the isolated binary 1.5μm structures. The measurements were very noisy partly because the potentials were being measured using an HP4156B parameter analyser (see section A.2.3) which did not have a high enough voltage resolution for low current measurements. The repeatability was significantly improved by using higher currents as can be seen in figure 5.5.

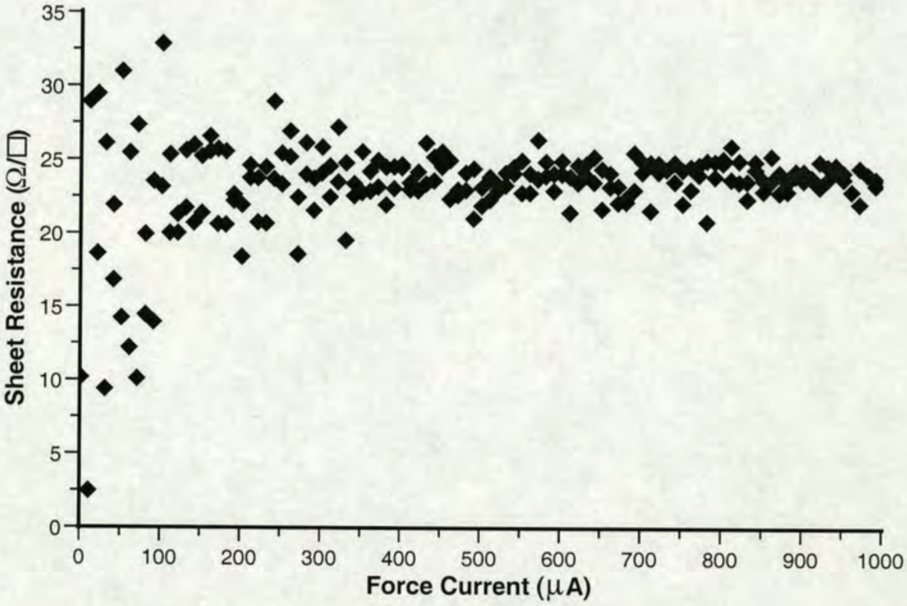


Figure 5.5: *Results of Kelvin measurements made on a chrome Greek cross structure as the force current was swept from 1μA to 1mA.*

One interesting result was that although the repeatability at low currents was quite poor, a large number of measurements at a set force current typically resulted in almost the same mean value. Sets of 200 measurements were made over a short space of time at five force currents ranging from 10μA to 1mA. The mean value of V/I and the standard deviation calculated for each current setting is plotted in figure 5.6.

The results indicate that although the repeatability of the measurement improves with higher force currents these high currents do not appear to cause joule heating which

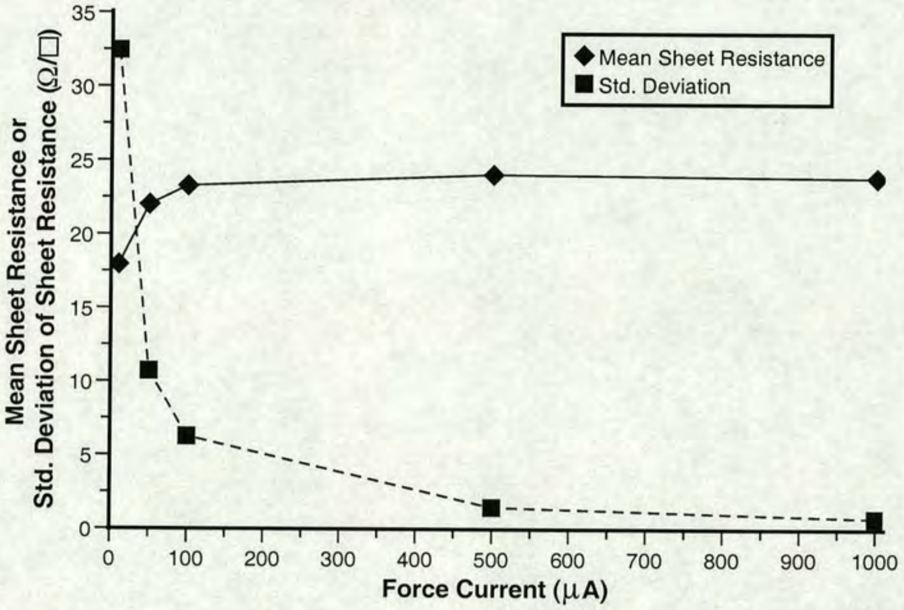


Figure 5.6: *Mean values and standard deviation of V/I versus force current for a chrome Greek cross structure.*

would result in a change in resistance. As the repeatability of the measurement is almost the same at 500μA and 1mA it was decided that the lower current should be used for any further measurements as a precaution against damaging the structure under test.

The Greek cross section of the test structure was measured 200 times at four different orientations with a force current of 500μA. The results are presented in table 5.1.

Orientation	Mean V/I (Ω)	$\sigma_{(V/I)}$ (Ω)	R_S (Ω/□)
+0°	5.30249	1.078	24.0328
−0°	5.36345	0.102	24.3091
+90°	5.23089	1.061	23.7083
−90°	5.40126	0.108	24.4804
Average	5.3245	-	24.1326

Table 5.1: *Results of Kelvin measurements made on a Greek cross test structure with a force current of* 500μ*A.*

The measured sheet resistance of 24.13Ω/□ is similar to a reported value of 19.4Ω/□ for chrome without an AR coating [100]. The measurements in table 5.1 show a factor of ten difference between the standard deviations measured with forward and reverse currents. The reason for the difference in variability is not clear but it may be related to probe contact problems. However, it does seem that contact resistance significantly affects the measurement as the values of mean V/I obtained are lower for the orientations with a larger standard deviation.

The chromium oxide coating was removed by a very short etch in an aqueous solution of ceric ammonium nitrate and acetic acid which left bare metal features. This meant that a test system using a probe card and semi-automatic probe station could then be used. Electrical measurements were performed using an HP4062B parametric tester (see section A.2.1) and a high resolution Solartron voltmeter (see section A.2.2) which provided more repeatable and precise measurements. However, isolated 1.5μm structures from one of the binary and one of the phase shifted layouts were tested first using the manual probe station and HP4156B to obtain further information about the effect of the measurement current on the results. Figure 5.7 shows the mean sheet resistance plotted against the force current while figure 5.8 shows the standard deviation.

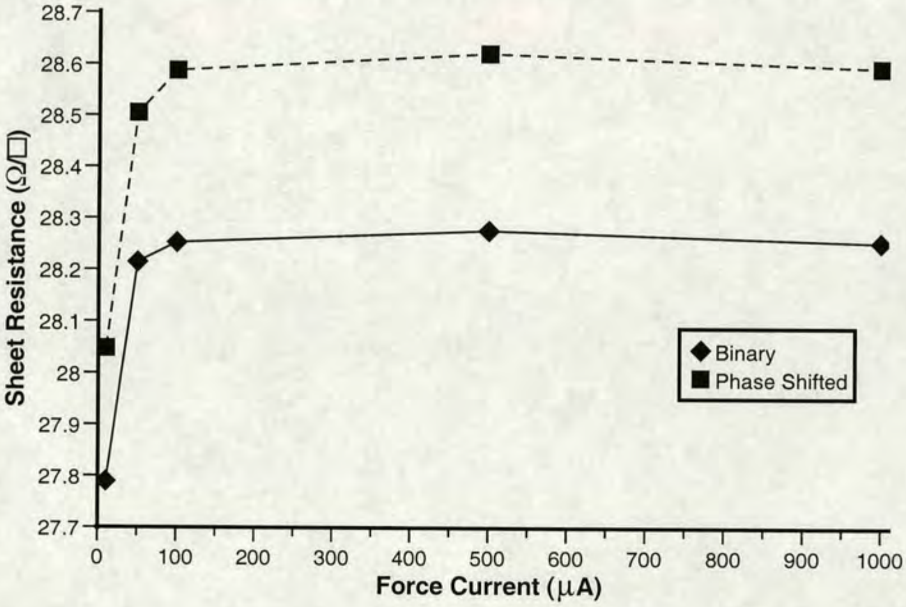


Figure 5.7: *Mean values of R_S against force current for chrome Greek cross structures.*

There are a number of conclusions that can be drawn from these results. Firstly the shapes of the curves are very similar to those in Fig. 5.6 indicating that the previous choice of a force current of 500μA is still applicable. However, the values of standard deviation are significantly lower than the previous results which suggests that most of the variability in the measurements made on the unetched structures was probably due

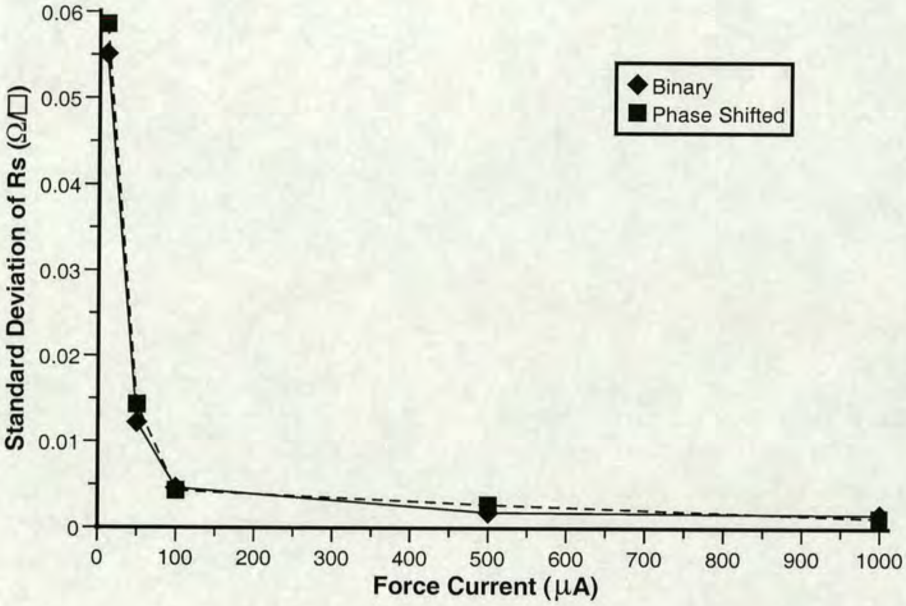


Figure 5.8: *Standard deviation of R_S against force current for chrome Greek cross structures.*

to noise introduced by poor probe contacts. Secondly there is an offset of ~0.34Ω/□ (1.2%) between the average sheet resistances obtained from the two structures with a force current of 500μA. Although the results are labelled "Binary" or "Phase Shifted" in Fig. 5.7 the isolated structures have no phase shifting elements around the measured structure. Therefore the offset between the structures is most likely due to variation of the chrome sheet resistance across the mask. The sheet resistances measured after the chromium oxide was removed were typically ~4.5Ω/□ higher than before which indicates there was some overetching of the chrome features.

Next, one complete set of structures (see Fig. 5.4) from the binary section and one from the phase shifted region were measured using the higher resolution system and the semi-automatic probe station. The sheet resistance results obtained from the dense I and L-type test structures have been averaged together for each feature size and are presented in Fig. 5.9.

Ideally R_S should be insensitive to feature size and the variation for structures with a nominal width of more than 0.7μm is small. For example, the difference between the mean sheet resistance extracted from the phase shifted I-type structures with a cross arm width of 0.7μm and those that are 1.5μm wide is ~0.25Ω/□ which is less

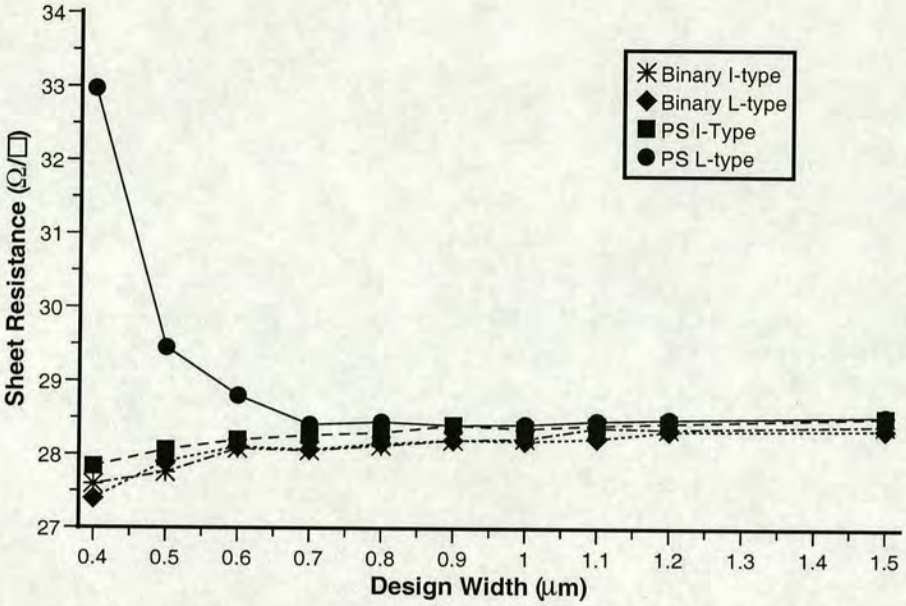


Figure 5.9: *Mean values of R_S against feature size for chrome Greek cross structures.*

than 1%. The narrower structures show much more variation with size, in particular the sheet resistances extracted from the phase shifted L-type structures show a sharp increase as dimensions reduce. At present the reason for this is not clear but it is only in the L-type structures that the phase shifting elements surround the centre of the Greek cross as can be seen in Fig. 5.2. The fabrication of the phase shifters may be affecting the geometry of the cross leading to problems with the measurements. Fig. 5.10 shows the average asymmetry factor F_A plotted against feature size. F_A is a figure representing the difference between measurements made on a cross structure at different orientations and is used to calculate a correction factor which is applied to the calculated sheet resistance to correct for asymmetry [37].

Provided that $F_A \leq 10.74\%$ the correction factor approaches unity and does not need to be used. Fig. 5.10 shows that F_A is negligible for binary and I-type phase shifted cross structures with cross arms wider than 0.7μm. Even the narrowest of these structures only requires correction of about 0.3% to the value of R_S. The results from the L-Type phase shifted structures confirm that these structures are not symmetrical and that correction factors should be applied. The sheet resistance results for these structures (see figure 5.9) have been corrected according to the method described in reference [37] and this has been effective for the structures wider than 0.7μm.

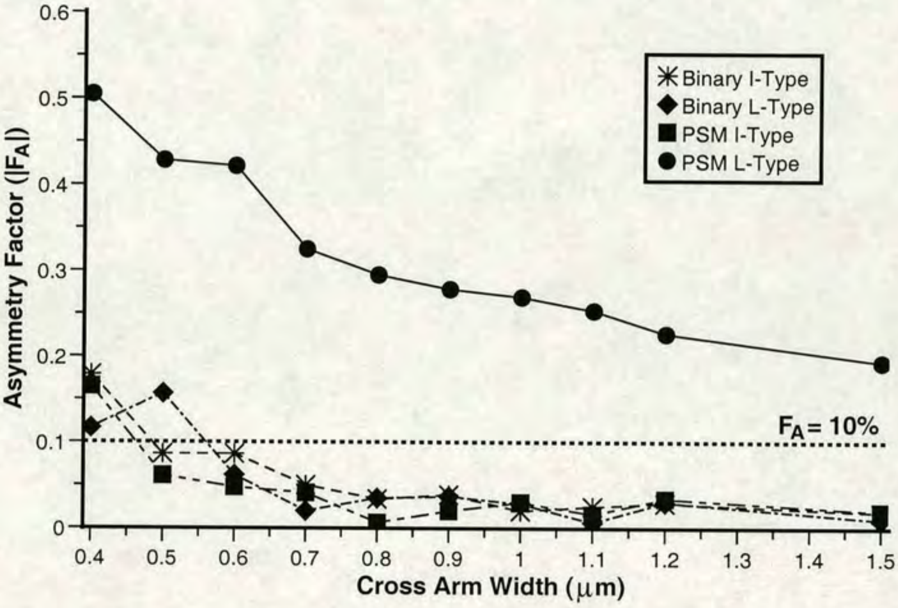


Figure 5.10: *Average Greek cross asymmetry factor F_A versus feature size for chrome structures.*

However, asymmetry correction cannot account for the high values of sheet resistance encountered in the narrower crosses. The effect of the phase shifting elements on these structures may lead to current crowding and joule heating in the narrow tracks during measurement. Alternatively, these crosses may have ceased to meet the conditions required for a van der Pauw structure (see sections 2.1.3 and 2.1.4).

In addition to the calculation of mean sheet resistance for all the structures with the same nominal feature size, as shown in Fig. 5.9, it is possible to investigate the variability of the measurements across the range of different mark to space ratios by taking the standard deviation. The results of these calculations are presented in Fig. 5.11.

It should be expected that the variation of the sheet resistance between different structures of the same size would reduce as the cross arm width is increased. Reference [41] shows that larger Greek cross structures are less sensitive to short range non-uniformity in the resistivity of the conducting film being measured. Large structures effectively extract the average sheet resistance for the material.

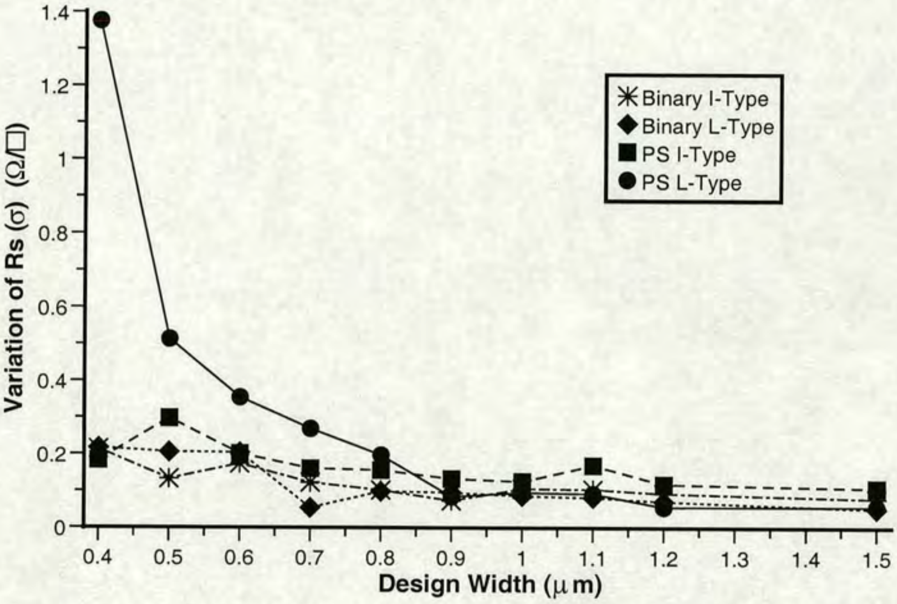


Figure 5.11: *Standard deviation of R_S against feature size for chrome Greek cross structures.*

5.2.4 Linewidth Measurements

Initial measurements of the resistance of a nominal 1.5μm wide track were performed using the manual probing system before the chromium oxide was removed and the results are presented in table 5.2.

Force Direction	Mean Resistance (Ω)	σ_R (Ω)
Forward	6730.22	2.4537
Reverse	6729.34	2.2709
Average	6729.78	-

Table 5.2: *Results of Kelvin measurements made on a bridge linewidth structure with a force current of $500\mu A$.*

The standard deviations observed when making the bridge measurements are proportionally much smaller (~0.035%) than for the R_S measurements where σ was almost 20% in some cases. This is probably because the voltages being measured are much higher for the bridge structures than for the crosses. Taking the average bridge resistance from table 5.2 and using it in equation (2.20), along with the average sheet resistance from table 5.1, gives an electrical linewidth (W_L) of 1.434μm. The nominal value of linewidth was 1.5μm so the electrical width is about 4.4% less than this.

If the individual values of R_S from each orientation are used to calculate linewidth figures using the average bridge resistance it can be seen that the measurements which showed the best repeatability provide values of ECD closest to the nominal linewidth. The linewidth results and the standard deviations of the sheet resistances can be seen in table 5.3.

Orientation	Mean R_S ($\Omega/\Box$)	σ_{R_S} ($\Omega/\Box$)	W_L (μm)
+0°	24.0328	4.886	1.428
−0°	24.3091	0.462	1.445
+90°	23.7083	4.809	1.409
−90°	24.4804	0.489	1.455

Table 5.3: *Sheet resistance, standard deviation of R_S and linewidths for each Greek cross measurement orientation.*

There are two main sources for variability in electrical CD measurements, firstly the measurement of the resistance of the bridge itself and secondly the value of sheet resistance used in the linewidth calculation. The first can be minimised through the choice of measurement current and, as is clear from the results in table 5.2, makes up a very small proportion of the measured resistance. The sheet resistance variability is more of a problem. It was shown in section 5.2.3 that the value of R_S extracted from the cross structures was a function of the feature size and it was also found that the repeatability of the measurements improved as the nominal cross arm width was increased. For this reason it was decided that the average of the sheet resistances extracted from the 1.5μm structures should be used in the calculation of electrical CD. These values are $28.5\Omega/\Box$ for the phase shifted structures and $28.4\Omega/\Box$ for the binary structures.

In addition to the electrical measurements of linewidth, the mask has been measured using a CD-SEM. The results obtained from the isolated structures are shown in figure 5.12. It is clear from these that there is an offset between the measured and designed width and it seems to be larger than the difference seen above for the measurements made before the oxide was removed. This suggests that there was some lateral etching of the chrome during oxide removal. There is also an offset between the results obtained by electrical measurements and those from the CD-SEM. This is to expected as systematic differences of a similar size are common between electrical linewidth measurements and other CD metrology techniques [89, 90]. Plotting the data in this way makes it difficult to visualise the offset because of the large range of widths. Fig. 5.13 shows the results of subtracting each of the measured CD values from the nominal drawn width for that structure.

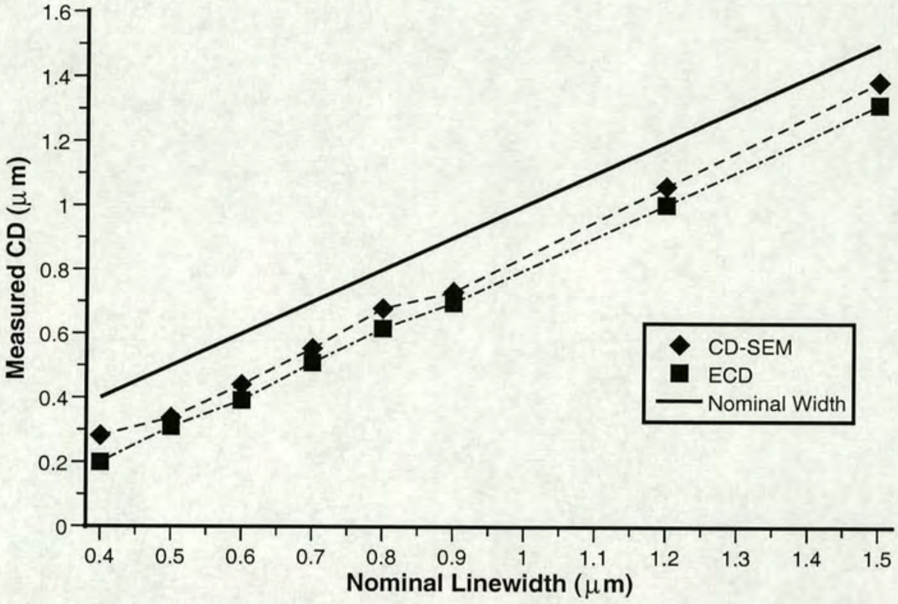


Figure 5.12: *Measured linewidth versus the designed CD for isolated bridge structures.*

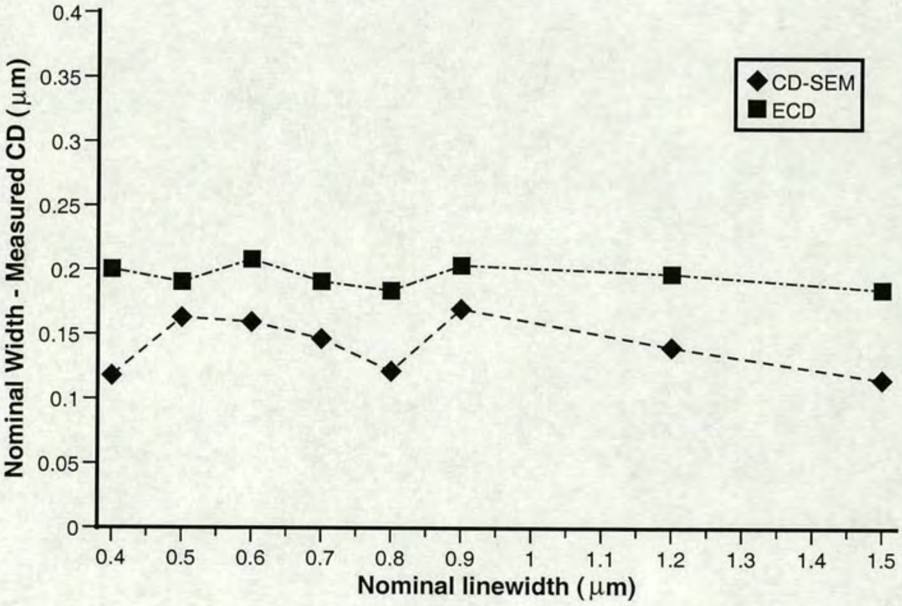


Figure 5.13: *Designed linewidth minus the measured CD plotted against the designed width for isolated bridge structures.*

This identifies the offset between the electrical and SEM measurements which varies from a maximum of $\sim 0.08\mu$m down to a minimum of $\sim 0.02\mu$m. However, there is no obvious trend with feature size. The same operation has been performed with the CD measurements of the dense linewidth structures with a mark to space ratio of 1:2 and the results are presented in figure 5.14.

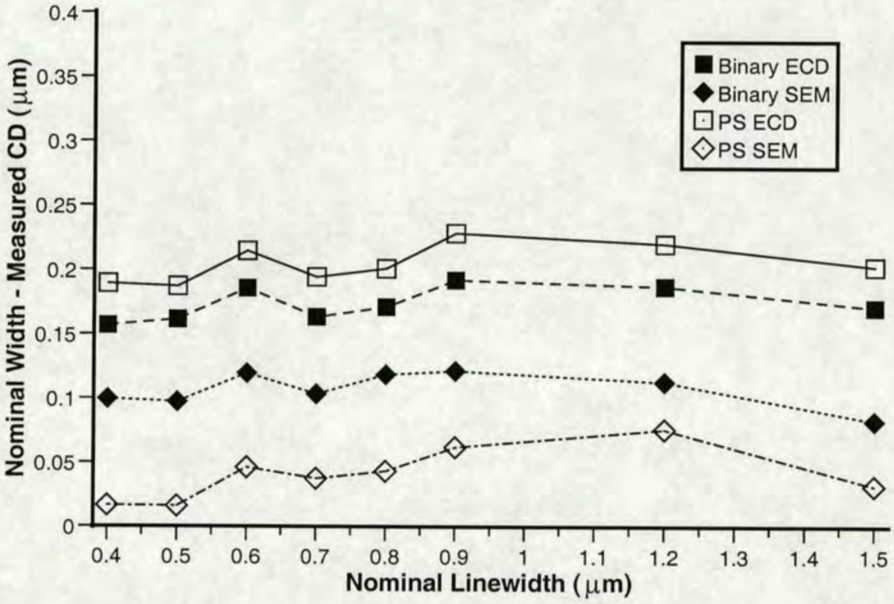


Figure 5.14: *Designed linewidth minus the measured CD plotted against the designed width for 1:2 dense bridge structures.*

The most important point to notice here is the offset between the electrical and SEM results for the phase shifted structure which is about twice that observed for the binary structures. For CD-SEM linewidth measurement the threshold selected to define the edge of the feature has a systematic effect on the extracted width. It is possible that the presence of the alternating phase shifting elements affect the SEM image so that the tracks appear significantly wider than expected. It is also clear that the electrical results track each other very well with an almost constant offset. The CD-SEM results from the binary structures also show a similar pattern but this is not the case for the phase shifted results. There seems to be an additional uncertainty about these SEM measurements which supports the case for the use of electrical on-mask metrology.

Unfortunately no SEM images are available of the phase shifted structures but figure 5.15 shows a typical image obtained from the binary section of the mask.

Charging of the mask in the SEM chamber meant that the images obtained had poor contrast which is undesirable when attempting to make accurate CD measurements. Imaging the mask for 10 minutes led to an almost total loss of contrast. The sample then had to be removed from the chamber for at least 20 minutes before measurements could continue. Only 7 measurements could be completed in this time which does not does not compare well with the electrical tests where automation can allow the measurement of hundreds of structures in 30 minutes.

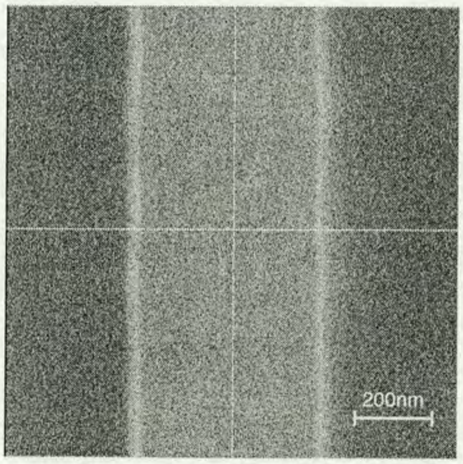


Figure 5.15: *SEM image of a nominally* $0.7\mu m$ *wide binary feature.*

The results presented in figures 5.13 and 5.14 suggest that the difference between the measured and designed width is not a function of the linewidth. However, if the results from the dense structures are plotted as a function of the mark to space ratio for a certain linewidth it becomes clear that there is a significant proximity effect on the width of the bridge resistor. Figure 5.16 shows the electrical and SEM CD results for dense 0.4μm structures. The difference between the designed and measured widths increases as the mark to space ratio becomes smaller. In other words, the measured width of the line decreases as the spacing between it and the surrounding dummy tracks increases.

5.2.5 Conclusions and Further Work

The preliminary measurements indicated that it is possible to probe test structures on chrome masks with anti-reflective coatings. However, suspected probe related problems make the measurements less repeatable than when probing the etched chrome pads.

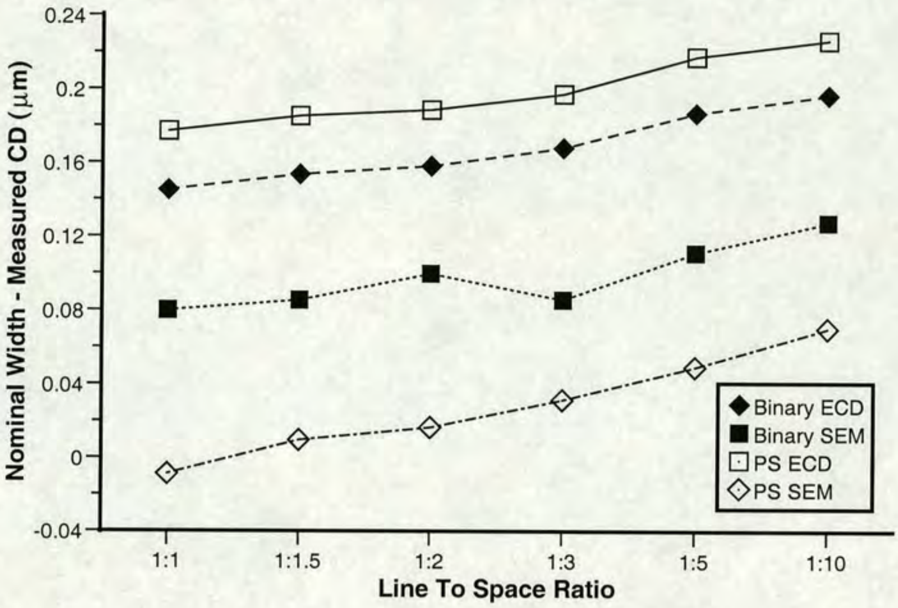


Figure 5.16: *Designed linewidth minus the measured CD plotted against mark to space ratio for* $0.4\mu m$ *dense bridge structures.*

The measurements made on Greek cross structures show that the variability of the extracted sheet resistance is reduced by increasing the size of the cross. It is clear that the etching of the phase shifting elements has a strong effect on the geometry of the L-type cross structures. This leads to large errors in the very narrow crosses which cannot be removed through the use of the correction factor f. Further work will include the use of an Atomic Force Microscope (AFM) to investigate these structures in an attempt to fully explain the results. Future on-mask test structure layouts should use very large Greek crosses, or possibly box crosses, for R_S extraction rather than following the minimum feature size of the bridge section. In addition these should be isolated structures as there is no need to use phase shifting elements which can affect the geometry of the cross in order to print relatively large features.

The electrical linewidth measurements show that the tracks are significantly narrower than the designed width and this may be partly due to the etching process used to remove the anti-reflective coating. There is also a systematic offset between binary and phase shifted dense tracks. Finally, there is a proximity effect in the dense structures which means that the width of the measured line increases as the spacing of the dummy tracks decreases.

Differences have been demonstrated between CD-SEM and electrical measurements. As expected there is a systematic offset between the ECD and SEM results obtained from the binary structures. What was unexpected was that the phase shifted lines, which appeared to be electrically narrower than the binary structures, were measured on the CD-SEM system as being significantly wider. This may be due to the phase shifting elements causing confusion about the position of the line edge. Charging of the mask in the SEM chamber also affects the measurement of linewidth leading to poor contrast and long testing times. This makes the possibility of using electrical test structures for mask metrology even more desirable.

Further work will include using the mask to print test structures which can be measured electrically and with a CD-SEM system. The results will be compared with those made on the on-mask structures in order to extract information about the MEEF of the exposure system being used. On-mask linewidth structures will also be imaged using an AFM in order to investigate the offsets observed between phase shifted and binary structures.

5.3 Optical Proximity Correction

5.3.1 Background

The introduction to this chapter stated that resolution enhancing schemes such as PSM can be used to image features with critical dimensions lower than the wavelength used in the exposure tool. The problem with printing sub-wavelength features is that the pattern becomes distorted because of optical or process proximity effects [135, 143–146]. Figure 5.17(a) shows some of the effects observed with sub-wavelength features such as shortening of lines and rounding of corners.

OPC is an attempt to make the final printed feature more closely match the desired layout by adding serifs to external corners and end lines, and removing opaque material at internal corners. The amount of material that is removed or added is a function of the surrounding pattern. A typical mask with OPC features and the corrected printed feature can be seen in figure 5.17(b).

There is another effect observed in sub-wavelength metrology which means there is

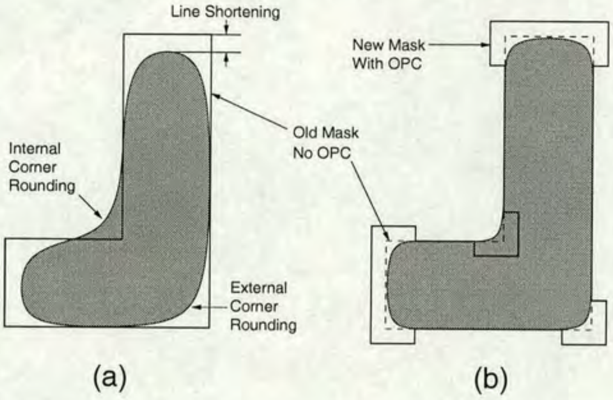


Figure 5.17: *(a)Schematic of mask layout without OPC and the resulting printed feature showing corner rounding and line shortening. (b)Schematic of mask layout with OPC and its printed feature which more closely fits the desired layout (dashed line).*

a critical dimension offset between densely packed and isolated lines. This is similar to the discrepancies observed with the PSM test structures in section 5.2. The effect is corrected either by adding sub-resolution assist features or by biasing the width of tracks depending upon their proximity to other features [137]. However, the work presented here focuses on linewidth test structures where the main interest is in examining the effect that OPC has on internal corners. For that reason proximity induced dimensional bias is not discussed.

5.3.2 Effects of OPC on Linewidth Measurement

Figure 5.18 shows a portion of a linewidth test structure illustrating the difference between the designed layout and the final mask geometry with OPC. It can be observed that the bridge section, which is to be measured, is narrowed near to the voltage taps in the version with OPC. It is therefore important to be sure that the correction that is applied to the design does not cause necking on the fabricated test structure leading to CD measurement errors.

For simple structures such as that shown in Figure 5.18 OPC can be performed manually on a trial and error basis. In this work the OPC module within Depict (see section A.3.4) was used to generate mask designs with different degrees of OPC aggressiveness. The next step is to use these to calculate “aerial images”, which represent the light intensity profiles in the image plane of the simulated stepper. The exposure wavelength used was

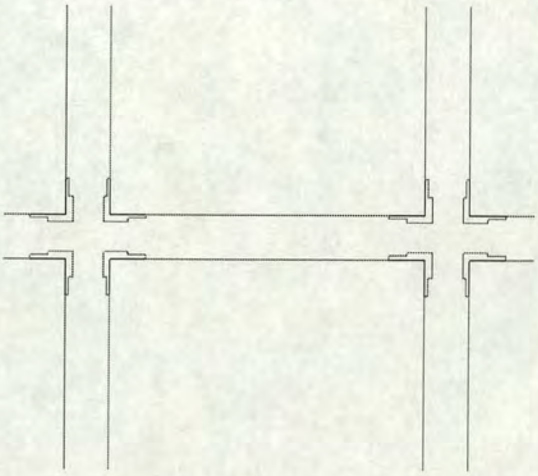


Figure 5.18: *An example of a portion of a linewidth test structure showing the original CAD layout and the mask geometry with OPC. The feature size is* $0.25\mu m$.

248nm with a numerical aperture (NA) of 0.48 and partial coherence (σ) of 0.7. These images were then used to simulate the exposure and development of the photoresist. An example of the resulting three-dimensional resist pattern can be seen in figure 5.19. It is clear that proximity effects lead to rounding of the internal corners of the structure but the effect of the OPC reduces this, as can be seen in figure 5.20.

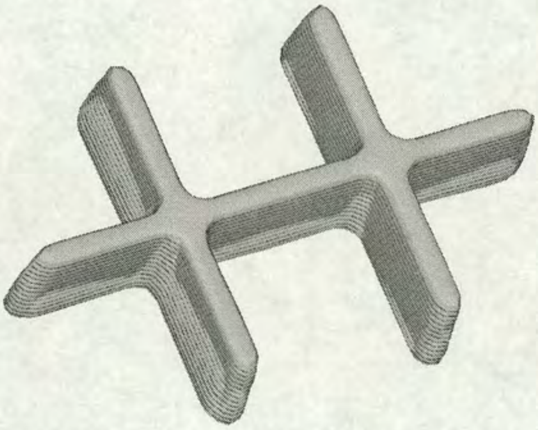


Figure 5.19: *3-D plot of the pattern transferred into the photoresist after exposure and development of a key portion of a linewidth test structure.*

It can be observed that the proximity correction caused no reduction in the width of the measured track, except in the case with the maximum amount of OPC where the bridge was narrowed along the whole length. The resulting photoresist images were

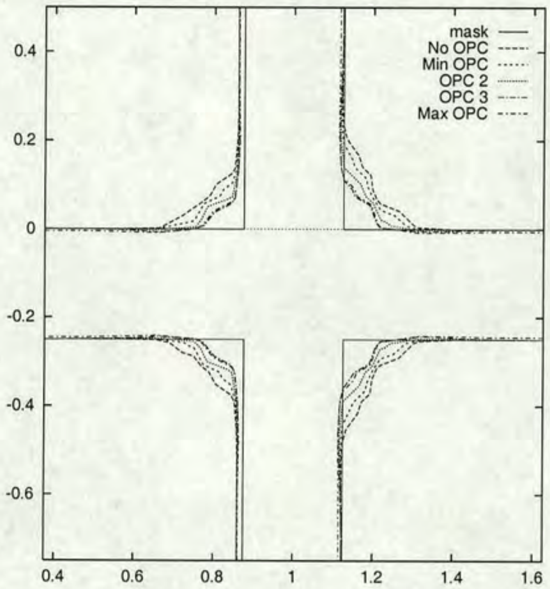


Figure 5.20: *Illustration of the way in which the image transferred to the photoresist is affected by the degree of OPC applied.*

then used to determine the exact geometries of test structures. Boundary information was extracted by taking a slice through the simulated photoresist pattern at a particular height. This data was used to generate grids in the Michelangelo visualisation and editing tool (see section A.3.5) for each level of OPC. These grids can then be used to simulate the electrical performance of the test structures using the Medici device simulator (see section A.3.6).

The initial simulations examined the resistance of a single voltage tap in the linewidth structure. This is very important for electrical CD measurements because the effect of the voltage tap is to make the line appear shorter [100]. This means that the linewidth will be underestimated unless the length of the bridge section is significantly larger than the tap width [39, 40]. Reference [83] describes a test structure which allows the measurement of the tap induced, line shortening figure, δL, by using bridge sections which include dummy voltage taps. This allows the use of much shorter bridge sections which may be important in some processes where the uniformity of the conducting material is uncertain.

One of the simulated tap sections, including the voltage contours, is shown in figure 5.21. The resistance of this structure can be used to calculate a value of δL

for each level of OPC. The simulated resistance results are plotted in figure 5.22(a) while the calculated δL values can be seen in figure 5.22(b). It is clear that the most aggressive OPC mask correction for 248nm exposures can reduce the value of δL by 0.1μm. The simulation of the designed mask geometry provides the theoretical minimum of δL for this structure.

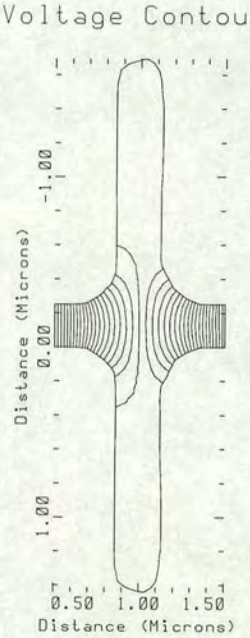
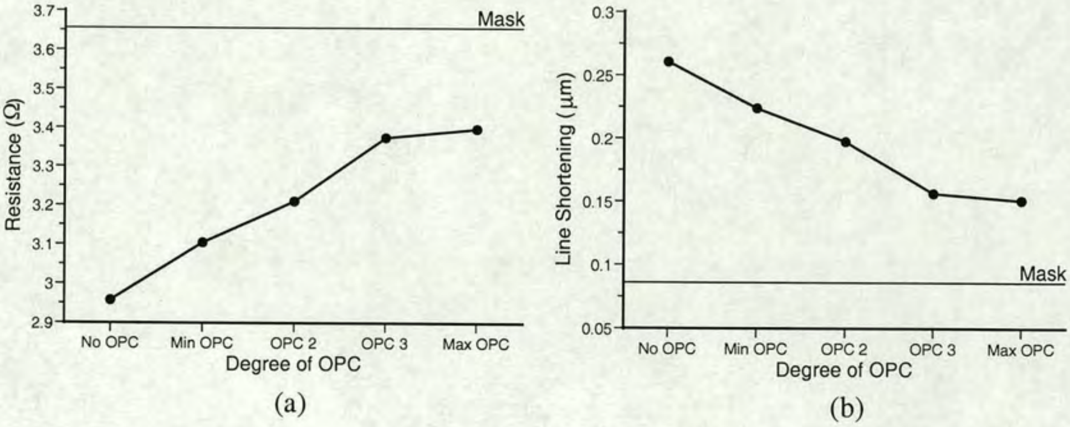


Figure 5.21: *Schematic plan view of simulated voltage tap showing contours of potential.*



(a) (b)

Figure 5.22: *(a) Simulated resistance of the voltage tap section for different degrees of OPC. The resistance obtained using the mask layout with no OPC is also indicated. (b) δL values calculated from the tap resistances in (a).*

In order to further investigate the effects of OPC on the functionality of this bridge resistor linewidth structure simulations were also performed using the whole structure. The electrical CD of the bridge section of the structures is calculated using equation (2.20). A schematic view of one of the simulated linewidth structures, including voltage contours, can be seen in figure 5.23.

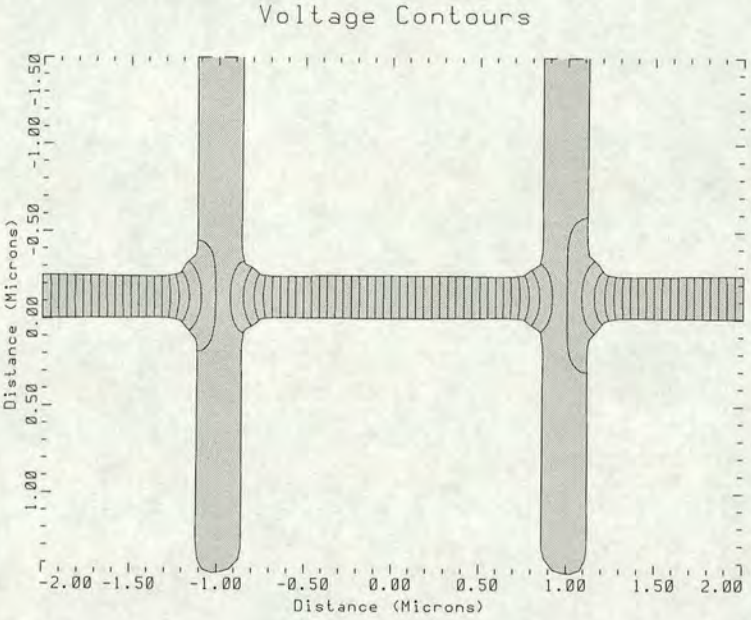
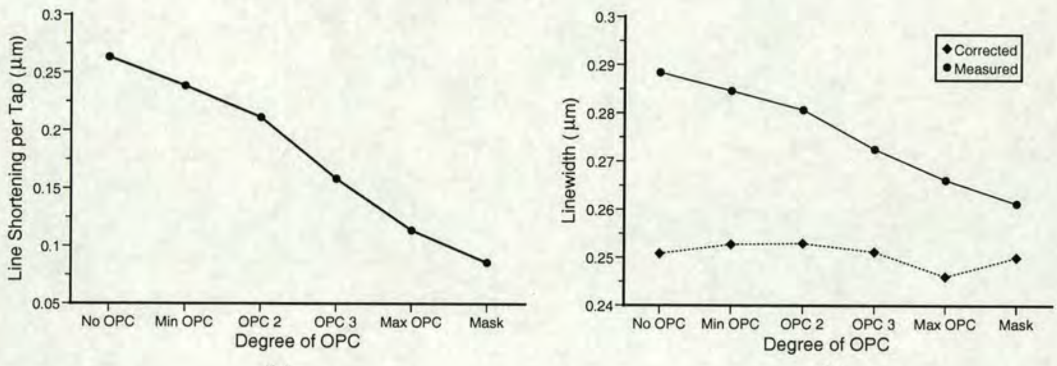


Figure 5.23: *Schematic plan view of a simulated bridge resistor linewidth structure showing typical voltage contours during testing.*

It is possible to calculate the tap induced, line shortening effect by measuring the resistance of the whole structure including the voltage taps. Current is forced between the terminals at either end of the structure and the voltage is measured to give the total resistance R_t. By assuming the linewidth is 0.25μm and knowing the value of R_S used in the simulation an apparent length for the structure can be calculated by rearranging equation (2.20). The line shortening effect of one voltage tap is simply given by half of the difference between the real (4μm) and the apparent length of the bridge. Figure 5.24(a) shows δL for this structure for different degrees of OPC.

For this full structure there is a greater δL at maximum OPC than for the previous simulations because part of the effect in this case comes from a thinning of the line between the voltage taps. For that reason it was decided that the δL values from figure 5.22(b) should be used to calculate corrected values of linewidth. Figure 5.24(b) shows the results of the linewidth measurement both with and without correction for line shortening, where $R_S = 1\Omega/\square$. The corrected values of linewidth are all within 1% of the nominal value of 0.25μm except for that obtained from the structure with the highest level of OPC. The proximity correction applied to this structure has actually narrowed the measured bridge section, as can be seen in figure 5.20.



(a) (b)

Figure 5.24: *(a) Line shortening derived from simulations of a full, bridge resistor, line-width test structure. (b) Results of linewidth extraction along with measurements corrected for the line shortening effects of the voltage taps.*

5.3.3 Effects of OPC on Sheet Resistance Measurements

From equation (2.20) it can be observed that any inaccuracy in the measurement of sheet resistance is directly transferred to the extracted value of linewidth [44, 51]. As geometries reduce, small asymmetries at the centre of the Greek cross, that were unimportant at larger dimensions, have the potential to significantly affect current flows. Figure 5.25 gives some examples of cross structures with severe asymmetries simulated in two-dimensions with Raphael (see section A.3.2).

The method for extracting sheet resistance from a Greek cross structure is described in section 2.1.4. If the structure has 90° rotational symmetry then sheet resistance can be found using equation (2.18) with the correction factor $f = 1$. However, this is not the case for asymmetrical structures such as those in figure 5.25. The simulation results for every possible measurement orientation of these structures are presented in table 5.4.

Obviously simulation results are not affected by any instrumentation problems and so reversing the current gives the same result, hence there are only four resistance columns. In addition, averaging together any pair of measurements which are at 90° to each other results in the same sheet resistance value. This is to be expected from the reciprocity relationship described in reference [37]. This reference also introduces

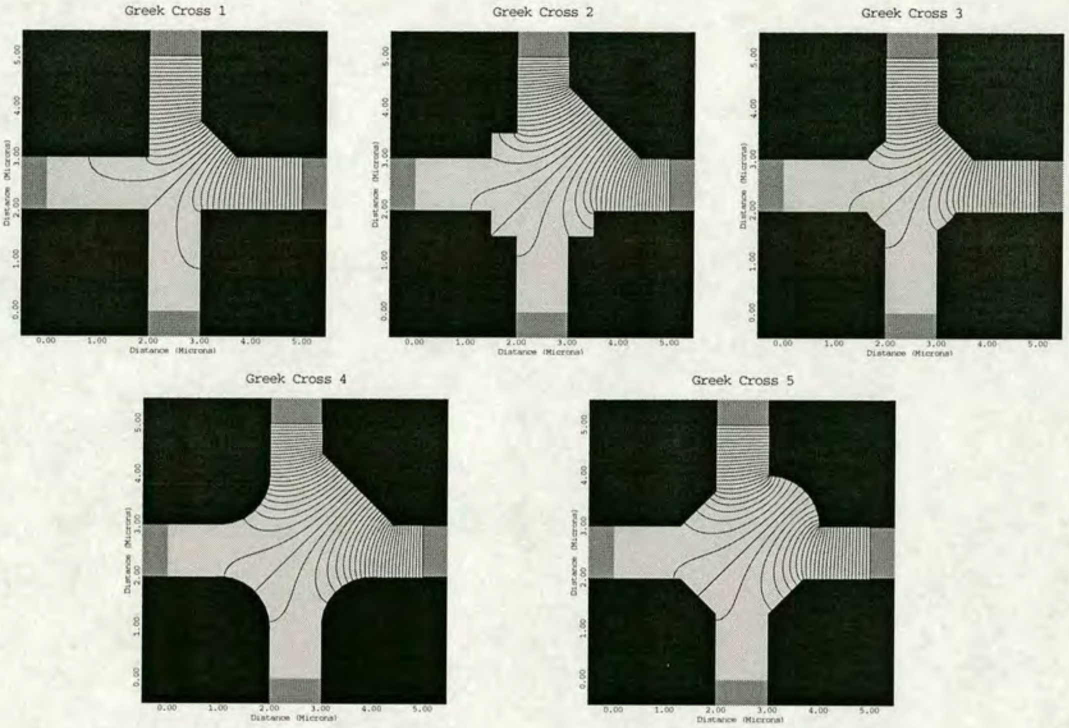


Figure 5.25: *Schematic plan views of five cross structures with large asymmetrical features showing the voltage contours observed during simulations*

the correction factor f which is combined with the sheet resistance to correct for the effects of asymmetry. A table of correction factors is provided in the appendix of this paper which covers values of asymmetry factor, F_A, up to 14%. Table 5.5 extends this for values of F_A over 70% using the simulation results in table 5.4

Structure	Orientation				R_{Avg}	Percentage Asymmetry	Correction Factor	Average Value	Corrected Value
	0°	90°	180°	270°					
	R_1&R_2	R_3&R_4	R_5&R_6	R_7&R_8		F_A(%)	f	R_S	fR_S
Greek 1	0.3023	0.1553	0.3023	0.1553	0.2288	64.294	0.9631	1.0369	0.9987
Greek 2	0.3230	0.1432	0.3230	0.1433	0.2331	77.135	0.9462	1.0565	0.9997
Greek 3	0.2585	0.1862	0.2585	0.1867	0.2225	32.513	0.9908	1.0079	0.9986
Greek 4	0.3146	0.1484	0.3146	0.1478	0.2313	71.807	0.9537	1.0492	1.0006
Greek 5	0.2785	0.1718	0.2785	0.1716	0.2251	47.395	0.9802	1.0205	1.0003

Table 5.4: *Simulated resistance values and the extracted sheet resistances for the structure shown in figure 5.25 (The value of sheet resistance in the simulations was* $1\Omega/\Box$*).*

F_A(%)	$1 - f$(%)	r
11.95	0.1195	1.1271
18.61	0.3006	1.2051
29.14	0.7396	1.3411
32.51	0.9223	1.3883
46.63	1.9116	1.6080
47.40	1.9762	1.6212
64.29	3.6858	1.9475
71.81	4.6322	2.1203
77.14	5.3766	2.2555

Table 5.5: *Relationship between geometrical asymmetry factor F_A and the sheet resistance correction factor f. r is the ratio between the values of V/I measured at the 0° and 90° orientations, as in section 2.1.4.*

The use of OPC on a Greek cross structure could introduce asymmetries into the geometry and it is clear from the results above that this can have a huge effect on very small crosses. The Medici structure boundaries generated using Depict have been used to create new sheet resisitance test structures for simulation. An example of one of these crosses can be seen in figure 5.26.

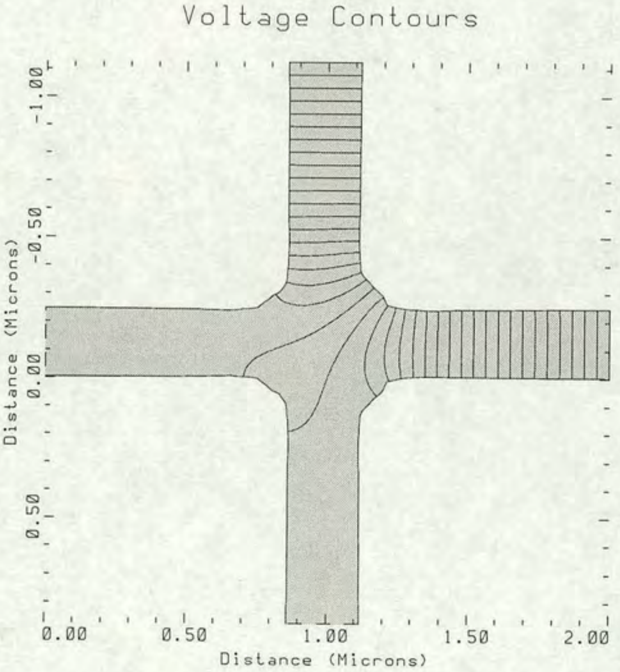


Figure 5.26: *Schematic plan view of a Greek cross structure with OPC generated by Depict. It shows equipotentials for the 0° orientation simulation.*

The five simulated photoresist images shown in figure 5.20, along with the mask layout without OPC, were used to create Greek cross structure boundaries for simulation. Table 5.6 presents the results of the simulations perfomed using these structures. Because the asymmetries in these devices were very small no values for the correction factor f ($f \approx 1$ in all cases) or for a corrected sheet resistance are given.

Simulation	$R(0°)(\Omega)$	$R(90°)(\Omega)$	$F_A(\%)$	$R_{Avg}(\Omega)$	$R_S(\Omega/\square)$
No OPC	0.22051	0.22083	-0.14588	0.22067	1.00016
Min OPC	0.22054	0.22110	-0.25225	0.22082	1.00083
OPC 2	0.22080	0.22053	0.12402	0.22066	1.00012
OPC 3	0.22060	0.22063	-0.01551	0.22061	0.99990
Max OPC	0.22052	0.22077	-0.11530	0.22064	1.00003
Mask	0.22086	0.22053	0.15186	0.22069	1.00027

Table 5.6: *Sheet resistance results for simulated Greek crosses derived from Depict aerial images. The results obtained from the uncorrected CAD layout are also included*

5.3.4 OPC Conclusions

This section has examined the effect of OPC on test structures designed to measure the electrical linewidth of tracks. It has been shown that OPC can reduce the value of voltage tap induced, line shortening for a 0.25μm wide track by between 0.1 and 0.15μm when using 248nm wavelength exposures. More importantly it has been shown that masks created by OPC software do not cause significant necking at the tap location and so can be safely applied to test structures.

In addition, the extraction of sheet resistance from asymmetrical Greek crosses has been investigated and the correction factors for values of F_A of over 77% have been presented. It has been shown that these correction factors can be used confidently, even with very large asymmetry values. While in theory only four measurements are required to extract the sheet resistance it is proposed that for best accuracy all eight possible measurement combinations should be made and a correction factor applied if necessary.

Finally, results for Greek cross structures exposed using OPC have been presented which, as expected, showed that OPC has no effect upon the value of sheet resistance extracted.

Chapter 6
Examples of Process Characterisation Using Resistive Test Structures

6.1 Introduction

This chapter presents two examples of the use of sheet resistance and electrical linewidth test structures to characterise semiconductor fabrication processes. These structures are ideally suited to this task because of the information that they can provide. Sheet resistance information can be used to characterise a deposition process by showing how the thickness changes with time. This could reveal whether or not the deposition rate is uniform. Sheet resistance structures could also be used to characterise an etch process where an increase in R_S would be observed when a conducting film is being thinned. Similarly, a linewidth structure would provide information about lateral etching of features. However, the most obvious use for an electrical linewidth structure is in the extraction of the minimum feature size capability of a photolithographic process.

The first example (section 6.2) of process characterisation described in this chapter is concerned with the effect of a bulk silicon wet etch on aluminium metallisation. Cross bridge test structures have been used to extract both sheet resistance and linewidth. The R_S data provides information about vertical etching of the aluminium while the ECD results indicate whether or not the metal features are becoming narrower due to exposure to the etchant.

The second example (section 6.3) describes test structures which have been used to characterise a Focused Ion Beam (FIB) induced platinum deposition process. Box cross type structures were used to extract the sheet resistance of the deposited platinum film. This data was then used to predict the resistances of Pt tracks fabricated using the same process. This section also includes details of computer simulations performed in order to find the ideal geometry for the cross structures.

6.2 Example 1: Characterisation of a Silicon Wet Etch Process

6.2.1 Introduction

Anisotropic wet etching of silicon is a central technology in Micro-Electro-Mechanical Systems (MEMS) fabrication. This is typically achieved using alkaline solutions such as sodium hydroxide (NaOH), potassium hydroxide (KOH) and tetramethyl ammonium hydroxide (TMAH). Unfortunately these etchants are incompatible with aluminium metallisation which makes the integration of MEMS elements with CMOS electronics problematic [147, 148]. References [149] and [150] describe the development of a TMAH based solution which has been shown to passivate aluminium metallisation while still giving a silicon etch rate of 1.1μm/min in the [110] direction. This is accomplished by adding sodium silicate solution, also known as water glass, to the TMAH. One additional problem encountered with such alkaline silicon etchants is hillock formation where pyramidal features form on the etched (100) Si surface [151, 152]. The addition of the strong oxidiser ammonium persulfate (APS) to the etch mixture prevents this effect and improves the quality of the surface [153]. The composition of the resultant etchant mixture can be found in table 6.1.

Chemical	**Concentration**
Tetramethyl Ammonium Hydroxide (TMAH)	5% by weight
Sodium Silicate Solution (Water Glass)	64g $SiO_2\ l^{-1}$
Ammonium Persulfate (APS)	5g l^{-1}
De-Ionised Water	To total volume of 0.8l

Table 6.1: *Composition of TMAH based anisotropic bulk silicon etchant which passivates aluminium and improves the quality of the etched Si surface [149].*

Initially the effect of the etch process on aluminium was characterised simply by observations using an optical microscope [149]. This is a purely qualitative measurement which does not provide information about the electrical properties of the remaining metal. In order to fully characterise this composition of etch solution the electrical and physical characteristics were measured and analysed. Electrical characterisation was performed with a standard cross-bridge test structure [45] measured using an HP4062B parametric test system and a Solartron voltmeter (see sections A.2.1 and A.2.2), while the physical analysis utilised a Scanning Electron Microscope (SEM). Initial results were published in reference [154] and this section will review that work and present the results of further experiments using the TMAH based etchant.

6.2.2 Test Structure Design

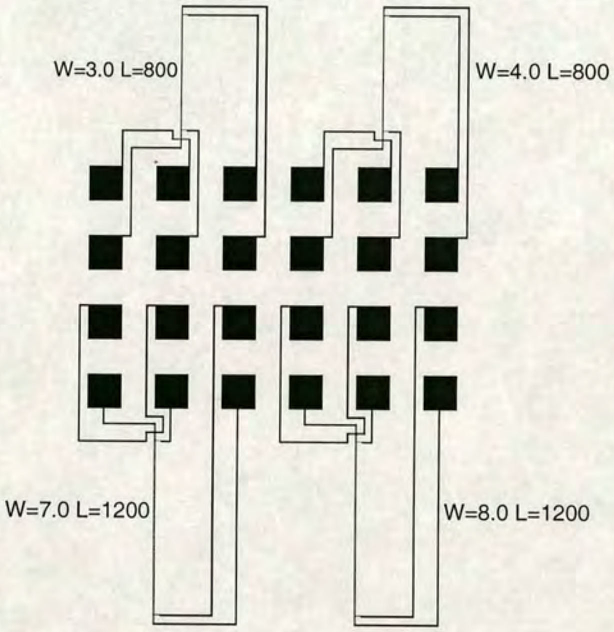


Figure 6.1: *Aluminium cross-bridge test structure layout.*

The test structures chosen for this investigation were part of a layout originally designed to characterise a damascene metallisation process and can be seen in figure 6.1 [50]. The tracks have nominal design widths of 3, 4, 7, and 8μm with measured bridge lengths of 800μm for the two narrower tracks, and 1200μm for the wider tracks. The pad configuration was designed to enable measurement using a standard 2×n probe card. Cross-bridge test structures were selected because they are able to measure both the sheet resistance and linewidth, and hence can help determine if the TMAH etch is thinning and/or narrowing the aluminium features.

Figure 6.2 illustrates three possible options for the fabrication of the test structures.

Each arrangement allows a different effect of the wet etch to be measured and requires a different fabrication technique. However, they all share the common layout design shown in figure 6.1. Type A structures are fabricated by using a Reactive Ion Etch (RIE) to remove the excess aluminium. This exposes three sides of the aluminium track to the wet etch which can then affect both the width and the thickness. Type B structures are fabricated using a CMP (Chemical Mechanical Planarisation) damascene process [121] where trenches are etched in the oxide followed by the deposition of aluminium to fill the trenches. Excess metal is then removed through CMP leaving the metal filled trenches. In this case only the top surface of the track is exposed to the etchant. Type C is a further option, similar to type A, with a protective layer of, for example, SiO_2 on top of the aluminium which would allow the sidewall etch rate to be evaluated. This type of structure has not been considered here.

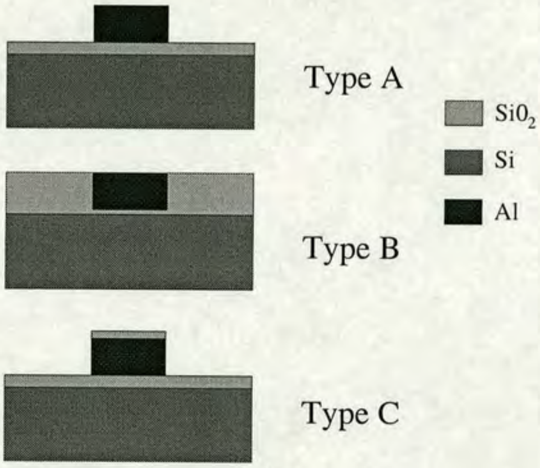


Figure 6.2: *Schematic cross sections through aluminium tracks showing possible test structure configurations.*

6.2.3 Type A Test Structures

The initial investigation described in [154] used type A structures to characterise the effect of the TMAH based etch. The test structures were fabricated on 3-inch (100) silicon wafers covered in 1μm thick, thermally grown, wet oxide. Half of the wafers were sputtered with 1μm of pure aluminium while the rest received the same thickness of Al/1%Si. The structures shown in figure 6.1 were printed using a 5× exposure tool, and the exposed metal reactively ion etched. It should be noted that these initial samples were not annealed.

The pure aluminium samples were initially etched in the TMAH based solution for one hour, and then at intervals of 30 minutes up to a total etch time of 3.5 hours. The etch was carried out in a 1l beaker with 0.8l of etch mixture. A reflux condenser was used to keep the concentration stable, and the temperature was kept at 80 ± 2°C using a temperature controlled hot plate. A 250 rev/min magnetic stirrer was used to keep the solution homogeneous both with respect to concentration and temperature. The setup is illustrated in figure 6.3.

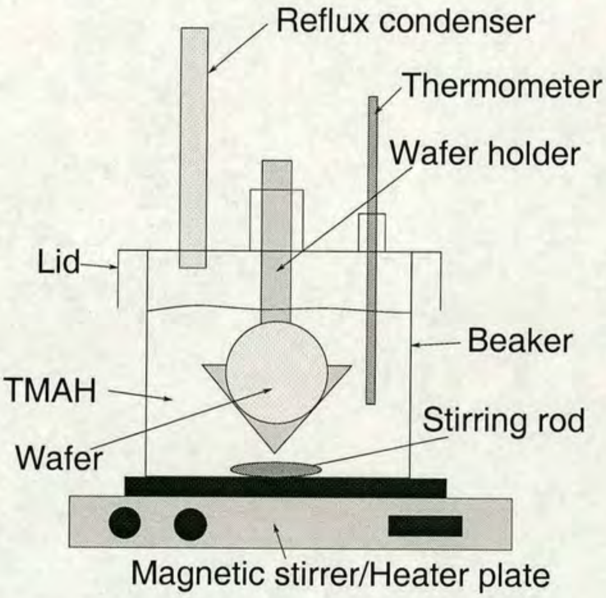
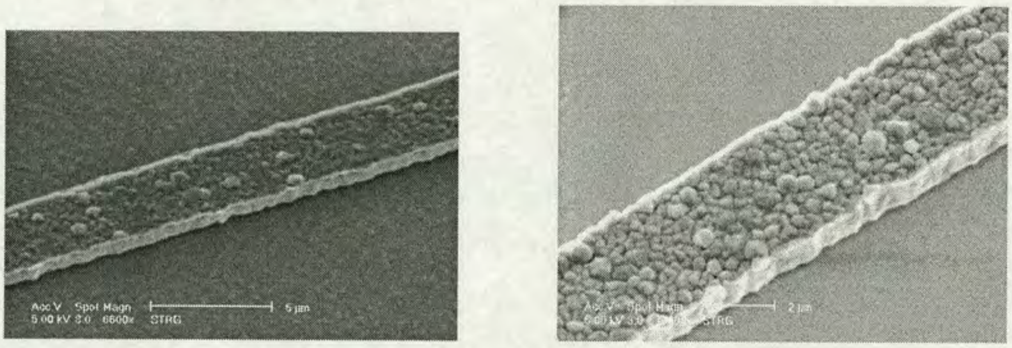


Figure 6.3: *Schematic diagram of the equipment used to perform the etching experiments.*

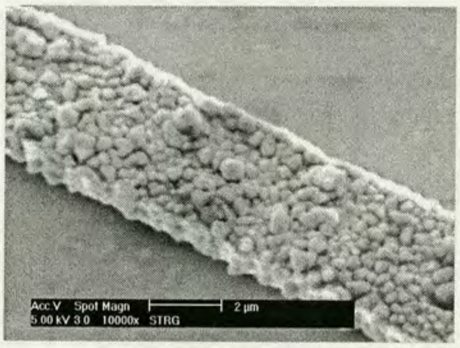
After each etch the wafer was rinsed and dried before both the electrical and physical effects on the aluminium lines (3, 4, and 7μm wide) were evaluated. SEM images of one of the pure aluminium tracks at various stages of the etch process can be seen in Figure 6.4. It can be observed that the roughness of the surface increases with etch time, and the grains can be easily identified.

The Greek cross sections of the test structures were measured in order to extract the sheet resistance and to reveal if the effective thickness of the metal is being reduced by the etch process. Initially, structures were measured on four different test die spread evenly over the wafer. The results from the structures with a nominal feature size of 3μm are presented in figure 6.5. There is significant variation in R_S from die to die,



(a) Before TMAH etch

(b) After 1 hour of TMAH etch



(c) After 3.5 hours of TMAH etch

Figure 6.4: *SEM micrographs of type A, pure aluminium tracks.*

which is caused by uneven aluminium deposition, but the trend of the data with etch time is similar for all four structures. The results indicate that sheet resistance increases linearly with etch time.

Any increase in sheet resistance suggests a decrease in the effective thickness of the track. The electrical measurements therefore indicate that the pure aluminium lines are monotonically becoming thinner throughout the etch time. The SEM images show that the top surface of the metal becomes rougher during the etch and that the grain structure becomes more defined. This suggests that the etching predominantly occurs along the grain boundaries leading to a non-uniform cross section similar to that illustrated in figure 6.6. The effect of this would be an increase in the measured sheet resistance, but this will vary depending on the initial grain size of the deposited material and the dimensions of the Greek cross. Reference [41] is an investigation of the effects

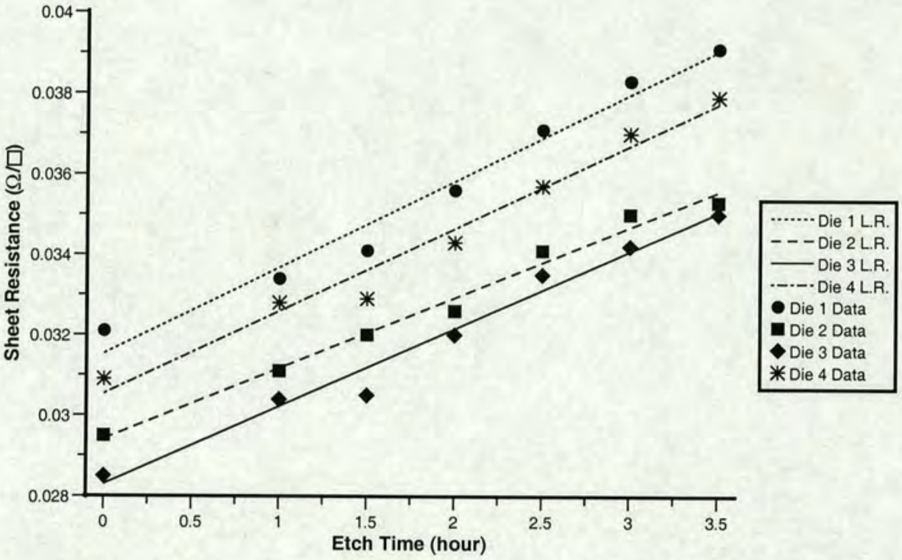


Figure 6.5: *Sheet resistance versus etch time for type A, pure aluminium structures. The straight lines are fitted to the measurement data by linear regression (L.R.).*

of non-uniform sheet resistance on the operation of four-terminal cross structures with different geometries. The conclusion of the paper is that Greek crosses with wide arms or some form of box cross should be used in such a situation to extract the mean value of sheet resistance.

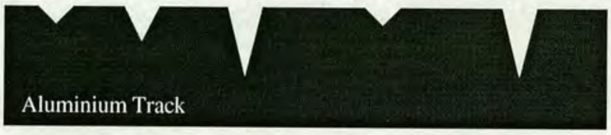


Figure 6.6: *Schematic cross section through an aluminium feature where etching has occurred along grain boundaries.*

The sheet resistance results were then used in the calculation of the width of the bridge section of each structure. The ECD results will indicate whether or not the etch solution is attacking the sides of the aluminium tracks and reducing the width. Figure 6.7 shows that the linewidth does not vary significantly over the 3.5 hours of etching. There are a number of possible reasons why the tracks are not attacked from the sides by the etchant. Firstly, as the nominal Al thickness is 1μm, the lines are between 3 to 8 times wider than they are thick, making the surface area available for etching smaller. In addition, the sidewalls do not have the same grain structure as the top surface. As the SEM micrographs show, the sidewalls are much smoother than the top surface and have no visible grain structure. This further reduces the surface area and therefore leads to slower etching.

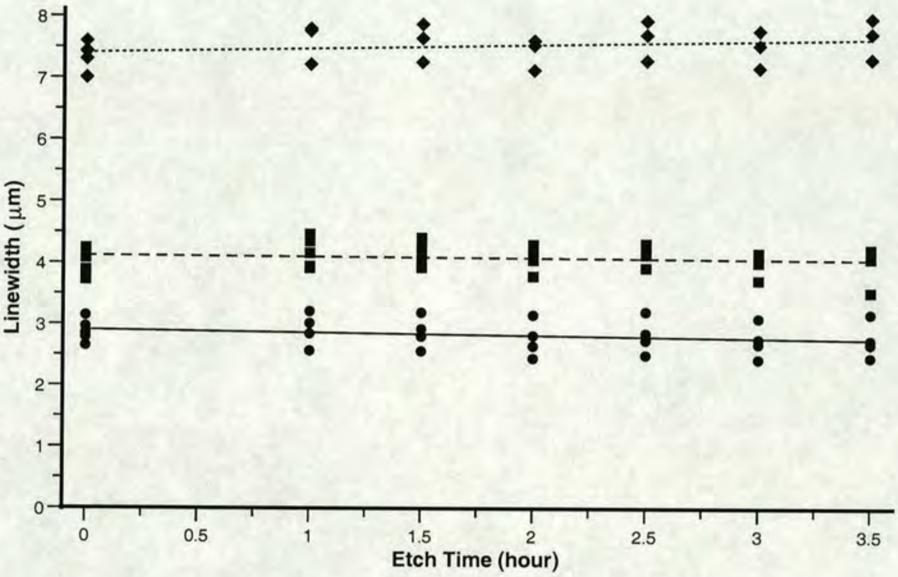
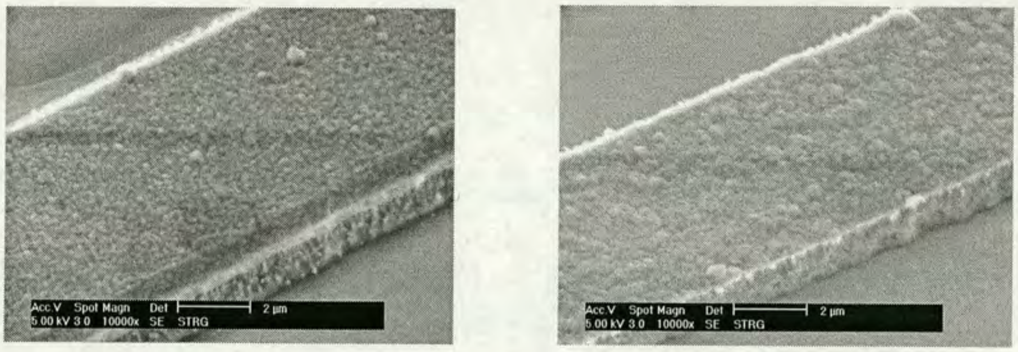


Figure 6.7: *Electrical linewidth versus etch time for type A, pure aluminium structures. The lines are linear fits to the data.*

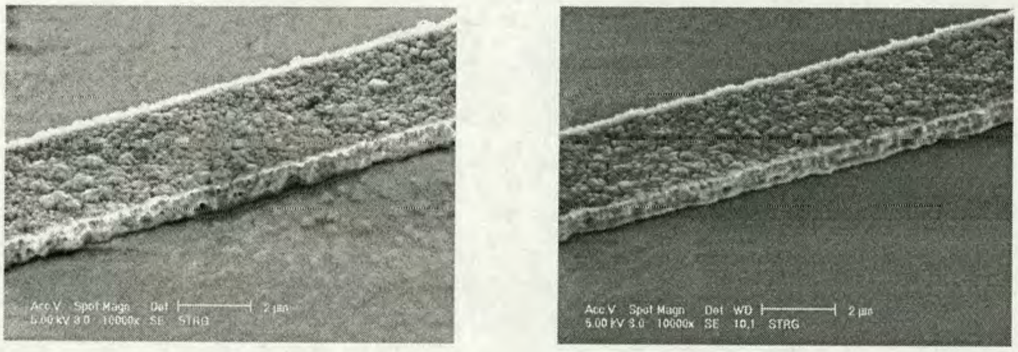
In order to provide more information about the initial period of etching, it was decided to monitor the Al/1%Si samples at 15 minute intervals during the first hour, and then at 30 minute intervals up to the total etch time of 3.5 hours. SEM images of a type-A Al/1%Si track at various stages during the wet etching process can be seen in figure 6.8.

It appears, from figures 6.8(a) to 6.8(c), that the surface roughness increases during the first 30 minutes of etching. However, comparison of figures 6.8(c) and 6.8(d) shows there is little additional etching after the initial 30 minutes. This suggests that the surface of the Al/1%Si is passivated after a certain length of exposure to the etch mixture. The electrical results appear to confirm this hypothesis as the sheet resistance increases during the initial period of etching, but remains approximately constant for the final 3 hours of etching. The results of R_S measurements are presented in figure 6.9(a) while figure 6.9(b) shows the measured electrical linewidths. The ECD results indicate that, as with the pure aluminium structures, there is little or no etching along the sides of the tracks and it is for this reason that type C structures were not investigated.



(a) Before TMAH etch

(b) After 15 minutes of TMAH etch



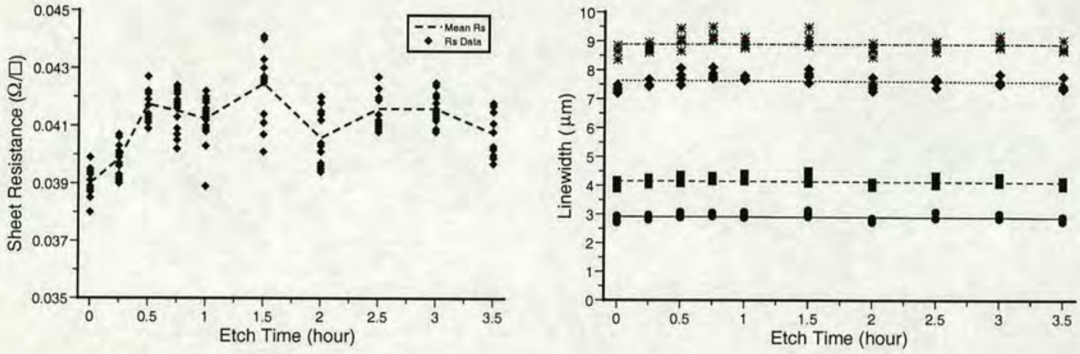
(c) After 30 minutes of TMAH etch

(d) After 3.5 hours of TMAH etch

Figure 6.8: *SEM micrographs of type A, Al/1%Si tracks*

6.2.4 Type B Test Structures

A number of type B structures were fabricated in order to extend the results presented in the initial study. The fabrication of the damascene metal samples begins with the growth of thermal oxide over the whole of the blank wafer. The thickness of the oxide was measured using a Nanospec optical metrology tool and was found to be $\sim 1.07\mu$m. The wafer was then patterned using a dark field (negative) version of the mask used to print the type A structures. This leaves the desired features exposed while the field oxide remains covered by photoresist. Next, the wafer undergoes a reactive ion etch which completely clears the oxide from the exposed trenches. A second thermal oxidation step follows the oxide etch and ensures that the metal features are isolated from the silicon substrate. The field oxide thickness after the second oxidation was $\sim 1.15\mu$m while the thickness at the bottom of the etched features was found to be $\sim$220nm. This makes the approximate depth of the trenches 930nm. The wafer was



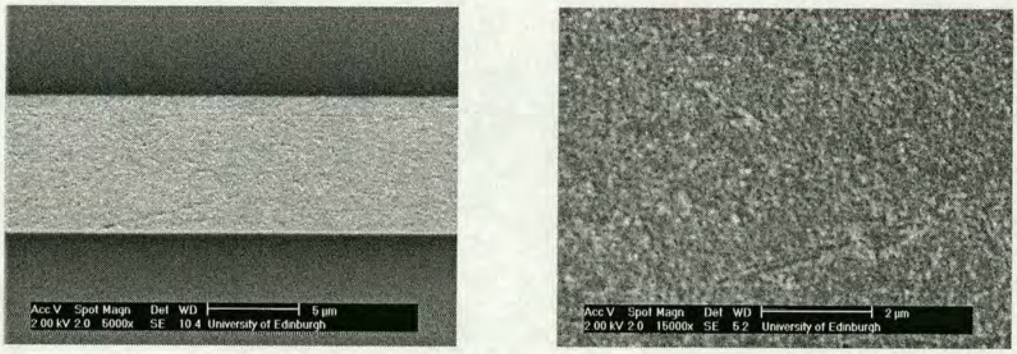
(a) (b)

Figure 6.9: *(a) Sheet resistance plotted against etch time for type A, Al/1%Si structures. The mean value of R_S for each etch time is also plotted (b) Electrical linewidth versus etch time for the same structures. The straight lines are linear fits to the data.*

then sputtered with approximately 1.4μm of Al/1%Si in order to fill the trenches and placed on a CMP polishing tool for damascene processing. After polishing for around 10 minutes the metal structures are cleared and ready for testing. SEM images of the damascene aluminium tracks at different stages of wet etching are presented in figure 6.10.

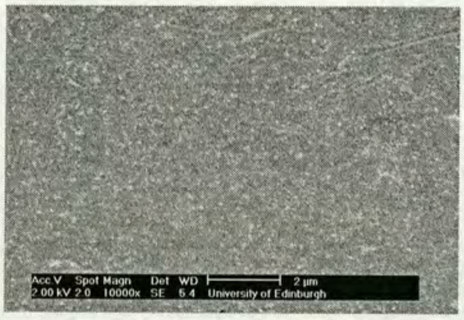
The first of the images (6.10(a)) shows a 7μm wide track before the first TMAH etch. The difference between the surface of the metal here and that shown in figures 6.4(a) and 6.8(a) is clearly evident. Instead of the clear grain structure observed with the type A lines the surface of the polished tracks appears to be reasonably smooth and uniform, apart from the occasional scratch mark caused by debris in the CMP slurry. The SEM images taken after the wet etching use a higher magnification but these again show a surface with a uniform roughness where there is no sign of the aluminium grain structure. Scratches caused during polishing can also still be seen on the metal surface after exposure to TMAH. The type-B structures were electrically tested before and after every 15 minutes of TMAH exposure up to a maximum of 1 hour. The sheet resistance and ECD results obtained are presented in figure 6.11

The first important issue with the sheet resistance results (figure 6.11(a)) is the variation with nominal linewidth where the sheet resistance increases with the feature size. This is likely to be an effect of CMP induced dishing which thins the metal in proportion to the width of the trench as described in chapter 3. The variation of the sheet resistance over the 60 minutes of wet etching is between 0.002-0.003Ω/□



(a) Before TMAH etch

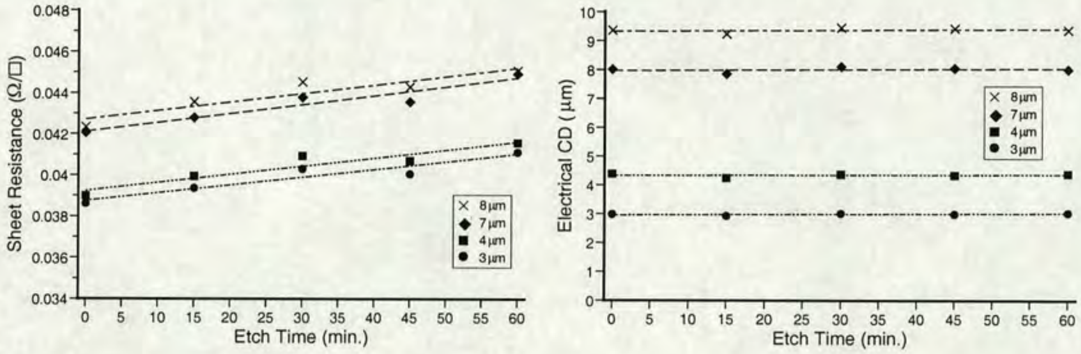
(b) After 30 minutes of TMAH etch



(c) After 1 hour of TMAH etch

Figure 6.10: *SEM micrographs of type B, Al/1%Si tracks.*

which is similar to the change in R_S observed during the first hour of etching with the type-A structures. Although there is no visible sign of etching occurring along grain boundaries, as is the case with the type-A structures, it is clear that there is a reduction in the conducting thickness of the aluminium. As the metal used was Al/1%Si it should be expected that the surface will become passivated and the sheet resistance become constant after the first hour of etching as in figure 6.9(a). Unfortunately, data from type-B structures which have been etched for longer than 60 minutes is not available so this cannot be confirmed. The electrical linewidth results (figure 6.11(b)) suggest there is little change in the width of the tracks with increasing TMAH etch time. This is to be expected because the sides of the damascene features are not exposed to the etchant.



(a) (b)

Figure 6.11: *(a) Mean Sheet resistance plotted against etch time for type B, Al/1%Si structures. (b) Mean ECD versus etch time for the same structures. The straight lines are linear fits to the data.*

6.2.5 Conclusions

The effect of a TMAH based, bulk silicon etch solution on aluminium metallisation has been investigated through the use of electrical sheet resistance and linewidth structures. The etchant was developed to passivate aluminium and prevent its removal while still providing a good [110] silicon etch rate and reducing hillock formation on etched Si surfaces. The initial experiments used type-A structures where both the top metal surface and sidewalls are exposed to the etchant. Electrical results from pure aluminium test structures showed that the sheet resistance increased linearly with etch time while the linewidth remained constant. SEM images of the tracks indicate that etching occurs primarily along the aluminium grain boundaries leading to increased surface roughness and a reduction in the average thickness.

A further set of type-A structures fabricated using Al/1%Si alloy were subjected to the same process and provided interesting results. The sheet resistance does not increase significantly after the first 30 minutes of etching so it appears that the etching of the metal ceases at this time. SEM images show that the surface roughness of the Al/1%Si tracks did not change significantly after the first 30 minutes which suggests that the aluminium surface is completely passivated.

The final experiment involved test structures fabricated using a damascene process which meant that only the top surface of the metallisation was exposed to the wet etch. There was no distinct grain structure visible at the surface of the polished tracks either before or after exposure to the TMAH. However it does appear that the tracks were being thinned as the sheet resistance increased with etch time at a similar rate to that observed with the type-A structures. As expected, the linewidths of the type-B structures were not affected by the wet etch.

6.3 Example 2: Characterisation of Platinum Deposited by Focused Ion Beam

6.3.1 Introduction

A focused ion beam system is similar to a Scanning Electron Microscope (SEM) but uses a beam of Ga ions produced by a Liquid Metal Ion Source (LMIS) rather than electrons from a field emission source. A schematic view of a typical FIB column can be seen in figure 6.12 [155]. It can be used to image surfaces in a similar manner to a SEM but its major application is the modification of integrated circuits by "cutting and strapping" [156].

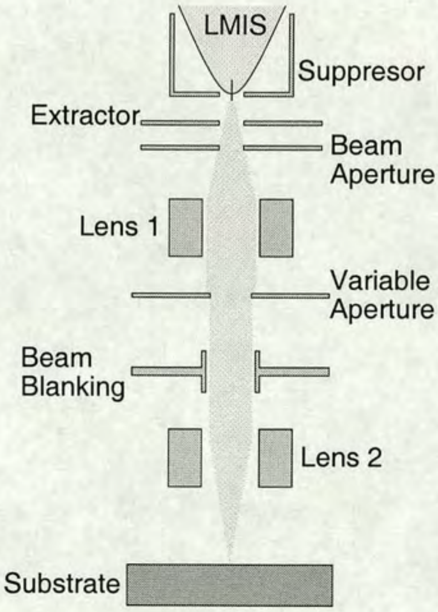


Figure 6.12: *Schematic cross section through a standard FIB column showing the important elements.*

The cutting operation is performed by using the ion beam to physically remove (sputter) atoms from the sample surface. This technique can be used to cut through passivation to the required level of metallisation in order to break a track or create a via. It is possible to obtain an enhanced etch rate with certain materials by adding iodine gas to the chamber. This increases selectivity between aluminium and silicon dioxide when cutting metal tracks and also prevents the redeposition of the etched aluminium.

A FIB system can also be used to selectively deposit metal on to the surface by ion beam induced deposition. Straps of metal deposited in this way can be used to create new connections between tracks once the FIB has cut vias through the passivation and the interlayer dielectric. This technique can be used to repair or modify an integrated circuit and can significantly reduce the time taken in debugging designs.

Platinum is the most common choice for use in integrated circuit repair and modification because it is inert in air and does not cause contamination of the circuit if deposited directly onto the silicon [157]. In order to deposit metal using the ion beam an organometallic precursor gas, (methylcyclopentadientyl)trimethyl platinum, is injected into the vacuum chamber through a needle close to the sample surface. This is adsorbed onto the surface and decomposes under the scanned ion beam to leave the deposited metal, as illustrated in figure 6.13. The FIB deposited platinum film can have a high concentration of contaminants such as carbon, which are also a product of the decomposition of the organometallic precursor. Typical resistivities for this material can range from $70\mu\Omega$-cm to over $1000\mu\Omega$-cm [157] whereas the bulk resistivity of pure platinum is approximately $10\mu\Omega$-cm [116].

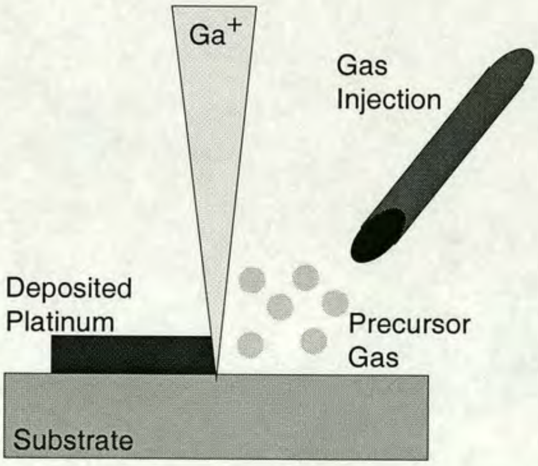


Figure 6.13: *Schematic illustration of ion beam induced platinum deposition.*

The quality of the film, its thickness, and therefore its sheet resistance, are functions of the ion beam current, the deposition time and the ion beam scan area. The deposition process needs to be characterised for each FIB system so that the basic electrical properties of a platinum strap can be predicted [156]. The typical requirement for a platinum strap is simply to have a low enough resistance to give a good electrical connection. The motivation for this study was to characterise the platinum deposition process so that resistive elements with a known value can be deposited.

6.3.2 Test Structures

The design of test structures for the characterisation of the platinum deposition process is complicated by the fact that it is only possible to deposit rectangular geometries. To fully characterise the platinum films the sheet resistance must be determined in terms of the deposition process variables. This information can then be used to predict the resistance of platinum tracks. The test chip also needed to include structures which can accurately measure the resistance of a conducting track so that the homogeneous nature and uniformity of the sheet resistance data could be confirmed.

6.3.2.1 Test Structure Design

There are many methods available for measuring the sheet resistance of the deposited platinum. The simplest technique is to deposit a very large area of metal and then use a four point probe technique [28]. The problem with this method is the relationship between the deposition rate, the beam current and the scan area. Large areas take a long time to deposit unless the beam current is increased proportionately. The manual for the FEI FIB 200 workstation used for this work recommends a beam current density in the range of 2-6pAμm^{-2} and a maximum of 2pAμm^{-2} for beam currents above 1nA [158]. Hence, a platinum square with a 50μm side requires a beam current of 5nA compared to the standard beam current of 150pA.

The alternative to the large deposition areas required by a four point probe technique is to use some version of the four-terminal van der Pauw [33, 34] sheet resistance structure such as a Greek [38] or a box cross [36]. The method of extracting the sheet resistance from these test structures is described in section 2.1.4. However, the fact that the FIB is limited to depositing rectangular geometries prevents the use of standard test structures. For example, a Greek cross would require at least three deposition regions connected together without any overlap which is completely impractical. The standard structures need to be adapted to meet the capabilities of the FIB system. The approach selected involved the design and fabrication of a set of aluminium features which form the basis of standard test structures. These are then completed by depositing a rectangular area of platinum. Figure 6.14 shows the aluminium layout for a box cross sheet resistance structure.

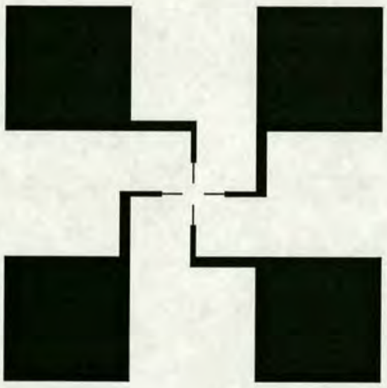


Figure 6.14: *Aluminium layout for a Pt box cross sheet resistor.*

The structure is completed by depositing a square area of platinum between the aluminium voltage taps at the centre resulting in a box cross. The full design includes a number of these structures with different spacings between the voltage taps to allow a number of box cross sizes to be fabricated. The ideal four-terminal van der Pauw sheet resistance structure is a homogeneous conducting film with an arbitrary shape and four point contacts on the boundary [33]. Real structures like Greek and box crosses can have finite contacts, and still provide accurate values of R_s, if they follow certain design rules [36, 40]. In the platinum box cross structures the contacts between the aluminium taps and the box can make up a significant proportion of the box area. This can be seen in figure 6.15 which shows the geometry used for the initial set of test structures which were fabricated.

It was decided that simulations of these structures should be performed to investigate any relationship between the size of the box and the accuracy of the measurements. In these simulations the width of the voltage taps (W_{tap}) was set to 1μm. Three sets

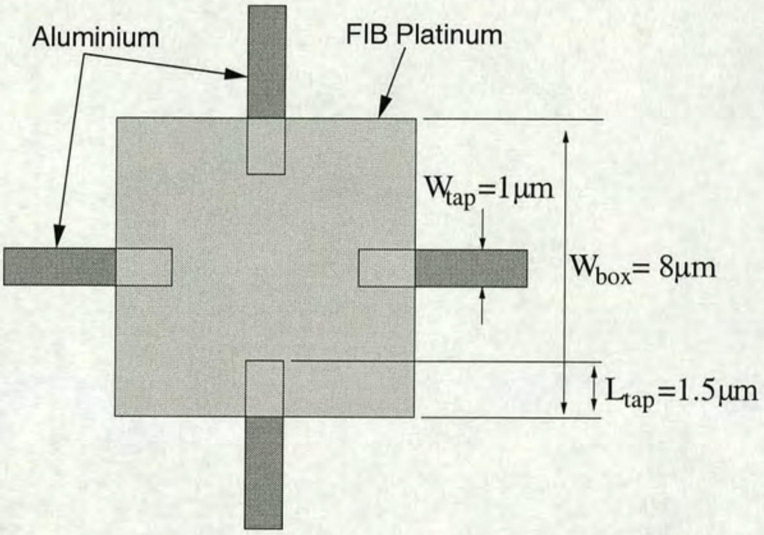


Figure 6.15: *Schematic plan view of the centre of an* $8 \times 8\mu m$ *box cross structure.*

of simulations were performed with different overlaps (L_{tap} = 1.5, 0.5 and 0.25μm) between the box and the aluminium taps. The sheet resistance of the box section was set to 1Ω/□ while its dimensions were were varied from $5 \times 5\mu$m up to $25 \times 25\mu$m. All of the simulations were performed in two dimensions using the Raphael package from Avant! and the results can be seen in figure 6.16.

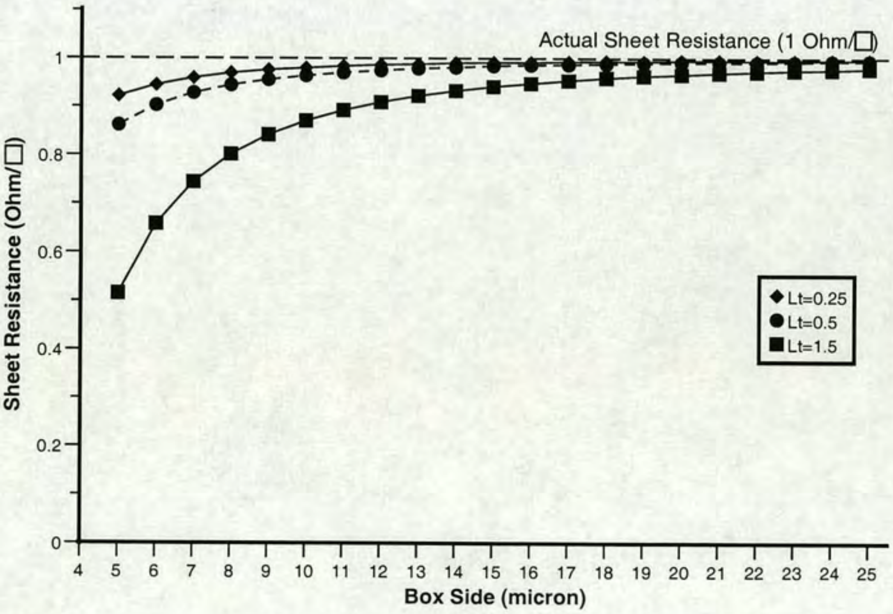


Figure 6.16: *Graph of sheet resistance against box dimensions for simulated platinum box cross structures with different voltage tap overlaps.*

The results show that the extracted sheet resistance approaches the actual value as the size of the box increases. The error observed for a box structure with $W_{box} = 5\mu\text{m}$ is almost 50% for a tap overlap of $1.5\mu\text{m}$. However, figure 6.16 indicates that this error can be significantly reduced by making L_{tap} smaller. Figure 6.16 also suggests that large box crosses should be used to increase the accuracy. The dilemma is that large deposition areas either require high beam currents or a long deposition time. The smaller structures also have areas closer to the dimensions of normal platinum straps. It was for this reason and also to ensure good contacts that the first set of box cross structures fabricated had the dimensions detailed in figure 6.15.

Asymmetries in van der Pauw structures can lead to errors in the extraction of sheet resistance. This would be the case if there was misalignment between the aluminium features and the platinum box. In order to investigate this a second set of simulations were performed which examined the effects of box misalignment. Box cross structures where W_{box} = 5, 10, 20 and $25\mu\text{m}$ were simulated in two dimensions with $L_{tap} = 1\mu\text{m}$ and misalignments ranging from $+0.9$ to $-0.9\mu\text{m}$ in X and Y. The box sheet resistance was again set to $1\Omega/\square$. Table 6.2 shows the results of the simulations with no misalignment and the results from structures with the maximum misalignment where $X_{offset} = Y_{offset} = \pm0.9\mu\text{m}$. The table also shows the percentage difference between the sheet resistances. The results show that the effect of misalignment is dependent on the size of the box cross with the smallest changes in measured R_s being observed with the largest boxes.

Box Size (μm)	$X_{offset} = 0\mu\text{m}$ $Y_{offset} = 0\mu\text{m}$ R_s ($\Omega/\square$)	$X_{offset} = 0.9\mu\text{m}$ $Y_{offset} = 0.9\mu\text{m}$ R_s ($\Omega/\square$)	Difference (%)
5	0.7137	0.7822	8.757
10	0.9243	0.9334	0.97
20	0.9811	0.9795	0.23
25	0.9874	0.9863	0.11

Table 6.2: *Results of simulating the effects of misalignment on different sizes of box cross structure.*

In addition to the sheet resistance measurement structures, the test chip also includes aluminium features which can be used to create a four-terminal bridge resistance structure. The aluminium layout for one such structure can be seen in figure 6.17.

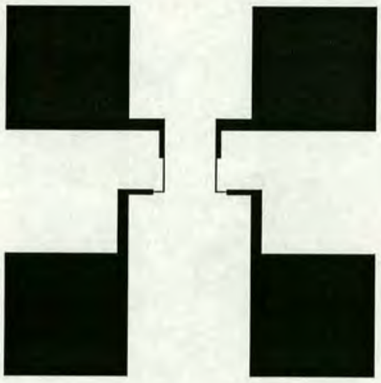


Figure 6.17: *Aluminium layout used to form Pt bridge resistance test structure.*

In this case the structure is completed by the deposition of a narrow strap of platinum between the aluminium taps to form the bridge resistor. The four-terminal bridge resistor is a Kelvin test structure which can be used to measure the resistance of a conducting track. Its main application is as part of a linewidth measurement test structure [45]. The full test chip layout contains a number of cross and bridge type structures with a range of possible platinum deposition sizes.

6.3.2.2 Test Structure Fabrication

The platinum test structure fabrication process begins with the aluminium layout which is patterned into 500nm thick Al deposited on a silicon wafer. The wafers used have a thin layer of thermally grown oxide which isolates the substrate from the aluminium structures. Once the desired deposition area is identified the tips of the aluminium tracks that will connect the platinum structure to the probe pads are cleaned. Aluminium oxide forms on any bare Al surface as soon as it comes into contact with air and must be removed in order to make a good contact. An additional problem was encountered with the initial set of samples where some sort of residue, possibly photoresist, was observed on the surface of the narrow voltage taps. The cleaning was performed by focusing the FIB closely on the end of the tap and imaging it until the residue appeared to have been removed. When the first platinum depositions were performed the oxide on the back side of the wafer led to charging of the surface causing the beam scan to shift after alignment. The result of this was that platinum was not deposited in the desired area. This was overcome by removing the oxide from the back of the wafer with a short wet etch in buffered HF solution.

As previously mentioned, the three main deposition process variables that affect the resistance of a platinum feature are the deposition area, the deposition time and the beam current. The deposition rate and the quality of the platinum film are dependent upon the beam current and the area which is being deposited. All of the structures fabricated so far for this study used a nominal ion beam current setting of 150pA as this is the same current used for strap deposition in normal operation. However, wear on the aperture in the FIB column gives an actual beam current which is typically between 190 and 200pA. If the beam scan area is also kept constant then the thickness of the film, and therefore its sheet resistance, should be solely controlled by the deposition time. As an initial experiment a set of twelve box cross structures were fabricated where the deposition area was $64\mu\text{m}^2$ ($8 \times 8\mu\text{m}$) as illustrated in figure 6.15. A very conservative overlap between the box and the Al taps was used ($L_{tap} = 1.5\mu\text{m}$) to ensure good contact but it should be possible to reduce this in future and improve the accuracy of the measurements.

The FIB system calculates a thickness for the deposited material based on the beam current, the deposition time and the area. Using this as a guideline the deposition times were set to give structures with nominal thicknesses from 500nm down to 60nm. The actual deposition times varied from about 330s for the thickest film down to 40s for the thinnest.

6.3.3 Initial Box Cross Results

The $8 \times 8\mu\text{m}$ box cross structures were tested electrically using the HP4062B/Solartron test system described in section A.2, and sheet resistance values were extracted. The simulation results in figure 6.16 reveal that an error of about 20% should be expected in the sheet resistance. The results of the R_s measurements are presented in figure 6.18. The graph also includes the result of adding 20% to each of the values and reciprocal functions which were fitted to each set of data.

The results indicate that the sheet resistance of the deposited platinum is inversely proportional to the nominal thickness or deposition time. As the deposition area and

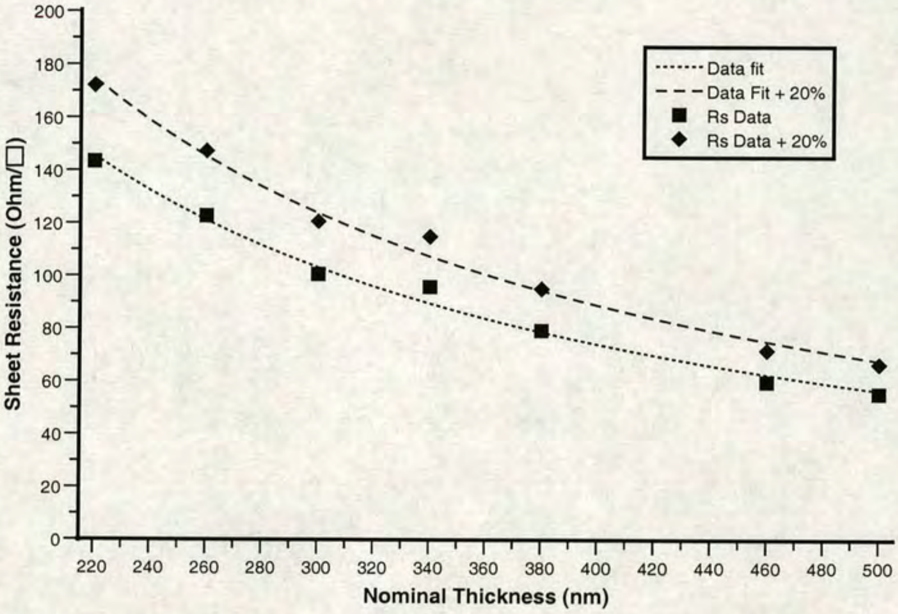


Figure 6.18: *Graph of sheet resistance against nominal thickness for* $8 \times 8\mu m$ *box cross test structures.*

beam current were the same for each structure then the deposition rate and material resistivity ρ should also be constant. Therefore, the thickness t will increase with time at a constant rate and as $R_s = \frac{\rho}{t}$ there should be an inverse relationship between the sheet resistance and the deposition time.

One of the box cross structures has been measured using an Atomic Force Microscope (AFM) and the resulting image can be seen in figure 6.19.

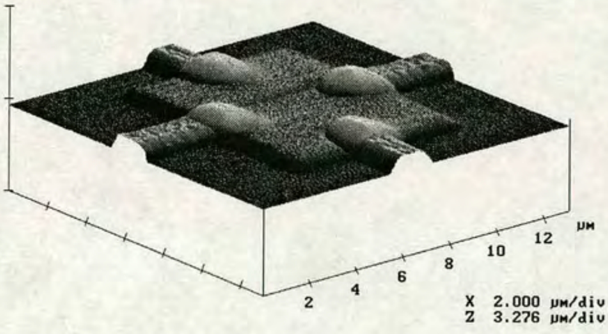


Figure 6.19: $13 \times 13\mu m$ *AFM scan of a FIB platinum box cross structure.*

A sectional analysis of the scan indicated that the platinum film thickness was between 320 and 335nm but the nominal thickness calculated by the FIB system for this structure was only 220nm. For this reason, the nominal thickness was ignored in subsequent experiments and the deposition time became the important variable.

6.3.4 Diagonal Box Cross Test Structures

The large errors associated with orthogonal box cross structures like that shown in figure 6.15 led to the consideration of other possible box cross geometries. Further simulations were performed using layouts where the box section of the structure is rotated through $45°$ as shown in figure 6.20. Structures were simulated with different tap spacings (S_{tap}) ranging from 5μm to 25μm and the results can be seen in figure 6.21. The sheet resistance of the box section of the structure is set to $1\Omega/\square$ and the tap width $W_{tap} = 1\mu$m as in the previous simulations. The dimensions of the box sections of the simulated structures were calculated using

$$W_{box} = \frac{\sqrt{2} + S_{tap}}{\sqrt{2}} \tag{6.1}$$

The result of using this equation is that the area of the tap overlap with the box is $0.25\mu\text{m}^2$. This is the same as an orthogonal box cross with $L_{tap} = 0.25\mu$m and figure 6.21 also includes the results of those simulations for comparison.

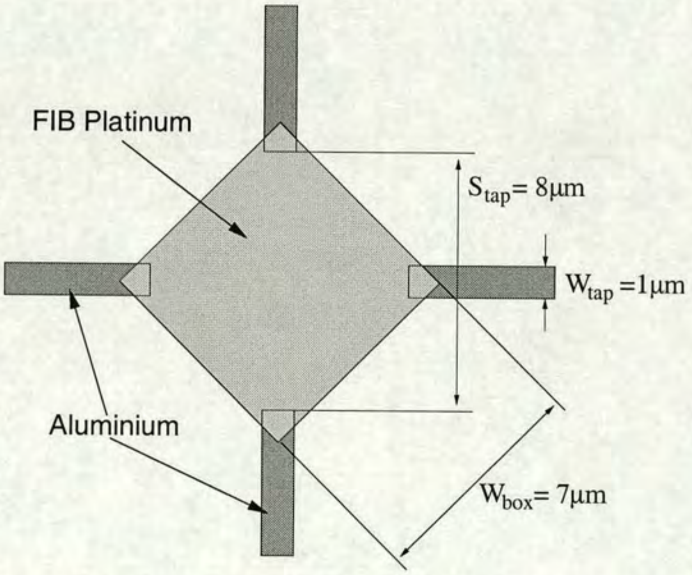


Figure 6.20: *Schematic plan view of the centre of a diagonal* $7 \times 7\mu m$ *box cross structure.*

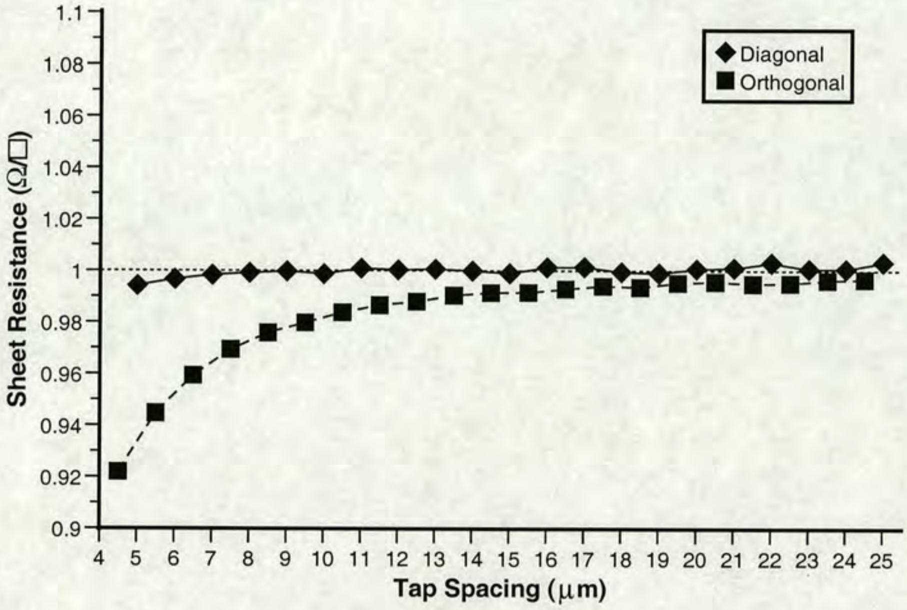


Figure 6.21: *Graph of sheet resistance against voltage tap spacing for simulated diagonal box cross test structures. The results from simulations of orthogonal structures with $L_{tap} = 0.25\mu m$ are also plotted.*

It is clear that a much more accurate value of sheet resistance can be extracted from the diagonal box cross structures. The error in R_S is less than 1% even for the smallest structure. The test chip includes a cross layout where the aluminium taps are 8μm apart. A diagonal box of FIB deposited platinum with sides of 7μm placed over these taps should give a sheet resistance error of about 0.1% according to the simulation results. A number of these structures have been fabricated with a beam current of about 200pA and deposition times varying from 30s to 250s. The results of extracting sheet resistance from these structures can be seen in figure 6.22.

The data indicates that, as expected, the sheet resistance is inversely proportional to the deposition time though there is some variation of the sheet resistance away from the linear regression curve fitted to the data. There was concern that this variation may have been caused by misalignment between the taps and the platinum square as was observed in the simulations of orthogonal box crosses. It is difficult to achieve perfect alignment between the aluminium and platinum and a resulting structure similar to that shown in Fig. 6.23 is more typical.

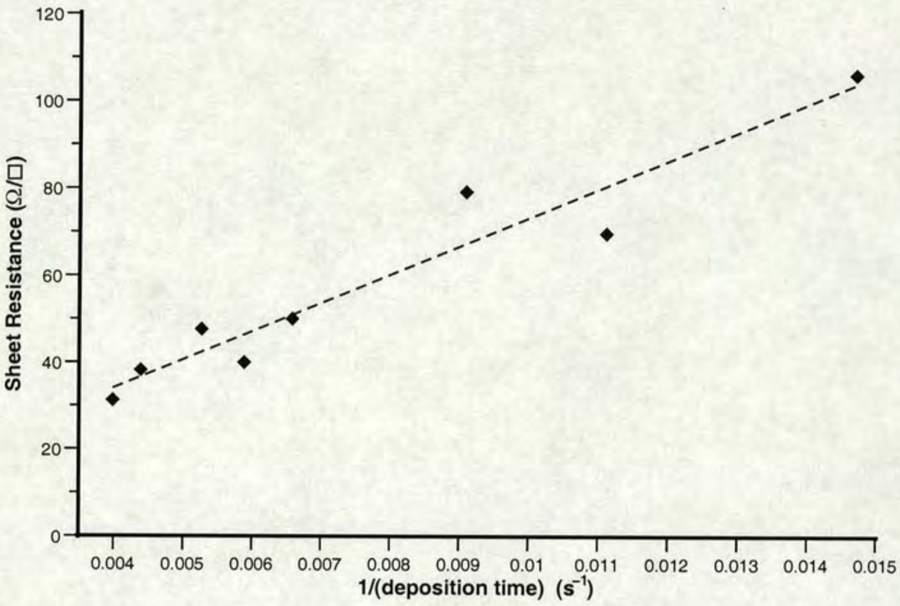


Figure 6.22: *Sheet resistance versus the reciprocal of deposition time for diagonal box cross test structures with $S_{tap} = 8\mu m$ and $W_{box} = 7\mu m$. The dotted line is a linear fit to the data.*

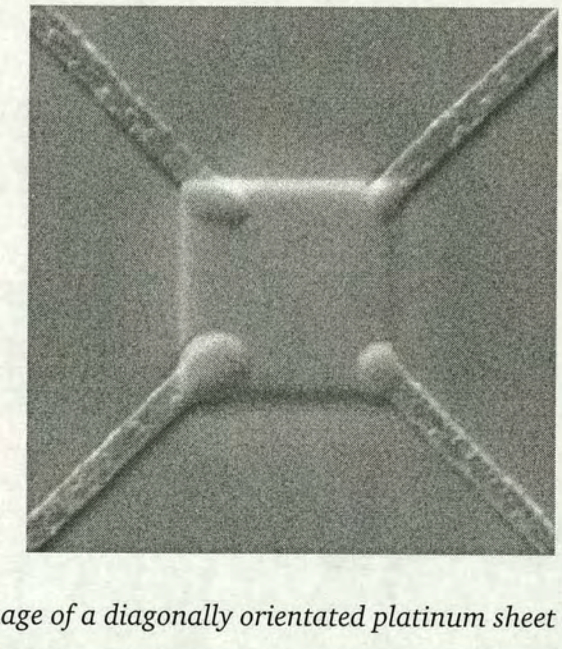


Figure 6.23: *FIB image of a diagonally orientated platinum sheet resistance test structure showing the misalignment between the aluminium taps and the FIB deposition*

In order to quantify the effect of misalignment a further set of simulations were performed using a diagonal box cross structure. The nominal dimensions of the box cross are the same as in Fig. 6.20 and the maximum offset in X or in Y was 0.5μm to ensure that all four taps still make contact to the box. The results of the simulations are presented in table 6.3 and these suggest that misalignment has a minimal effect on the measurement of sheet resistance from these structures.

X_{off} (μm)	Y_{off} (μm)	R_S ($\Omega/\Box$)	Error (%)
-0.5	-0.5	0.991	0.9
0.5	-0.5	0.991	0.9
0	0	0.992	0.8
-0.5	0.5	0.991	0.9
0.5	0.5	0.991	0.9

Table 6.3: *Results of simulating the effects of misalignment on a diagonal box cross structure.*

6.3.5 Bridge Test Structures

A small number of bridge resistor structures have been fabricated using the aluminium layout shown in figure 6.17. Figure 6.24 shows one of these structures.

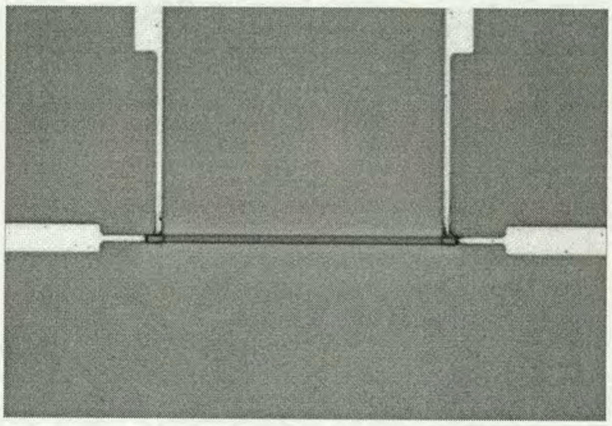


Figure 6.24: *Photomicrograph of a hybrid aluminium/platinum four-terminal bridge resistor test structure.*

This initial set of bridge resistors were fabricated with the same beam current and the same nominal thicknesses as the orthogonal box cross structures. However the strap deposition area was not the same being $55\mu\mathrm{m}^2$ rather than $64\mu\mathrm{m}^2$. Therefore, the sheet resistance information from the initial box cross structures should not be used to predict the resistance of these lines. The results of electrical measurements made on these bridge structures are presented in figure 6.25.

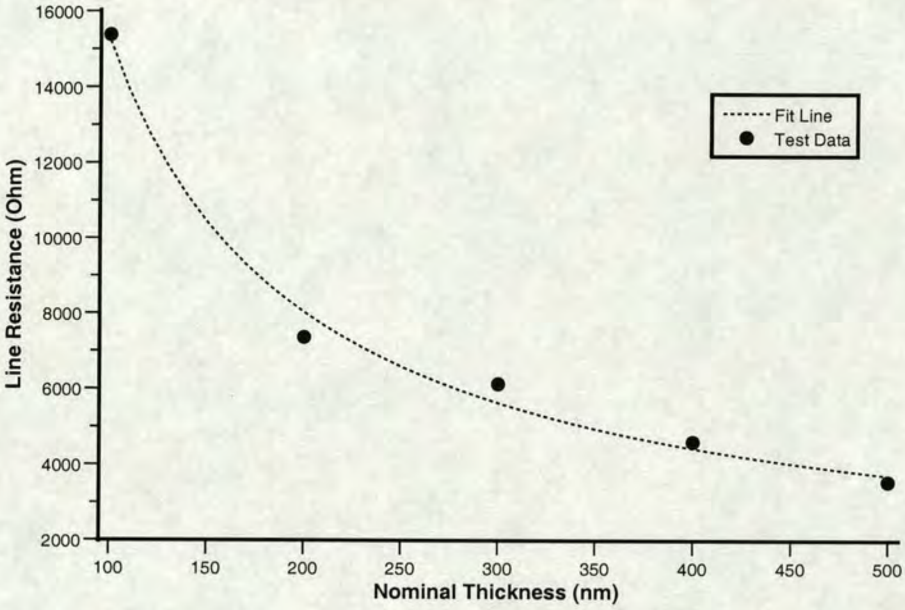


Figure 6.25: *Resistance against nominal thickness for four-terminal bridge resistor structures.*

As was expected, the results show that the resistance is inversely proportional to the material thickness. However, these bridge structures are not quite ideal because they do not allow true Kelvin measurements. The reason for this is that the current forcing terminals are connected to the voltage taps. Hence, the resistance measured with these structures may include some of the contact resistance between the platinum and the aluminium. In order to overcome this problem, the FIB system was used in enhanced etch ion milling mode to remove some of the aluminium and disconnect the force terminals from the voltage taps. Figure 6.26 shows the result of altering the aluminium layout.

The next step is to fabricate bridge resistors using these modified structures. The deposition area for the strap which will complete the structure was set to be the same as that used for the diagonal box crosses in section 6.3.4, i.e. $49\mu\text{m}^2$. The distance between the current forcing terminals is 72μm and so the strap length must be greater than this. The dimensions were chosen to be $0.5 \times 98\mu$m which gives the desired deposition area. An example of one of these Kelvin bridge resistors can be seen

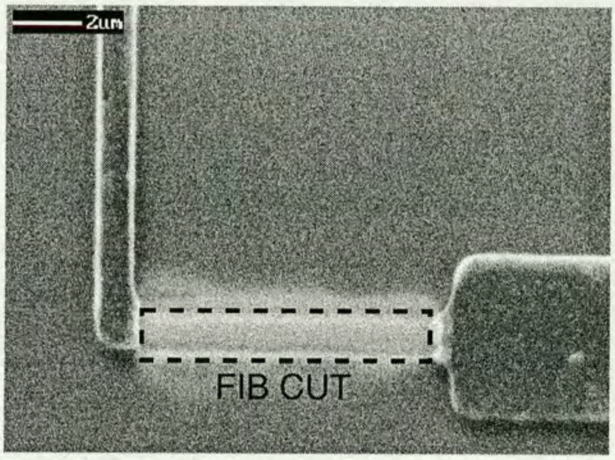


Figure 6.26: *FIB image of the alteration made to the aluminium test structure to allow Kelvin measurements.*

in figure 6.27. A number of these structures were fabricated with deposition times ranging from 60 to 240 seconds and the results of electrical measurements made on these resistors are presented in Fig. 6.28.

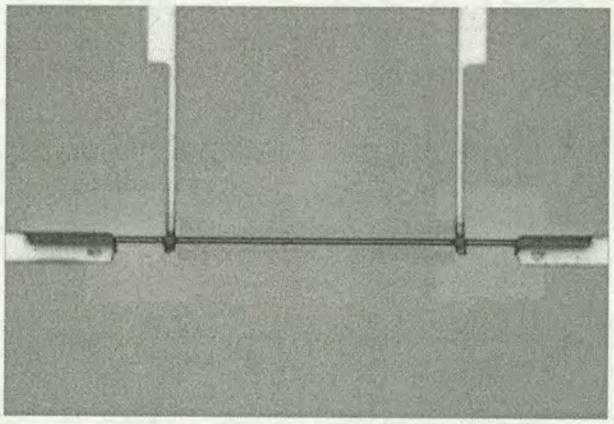


Figure 6.27: *Photomicrograph of a four-terminal Kelvin bridge resistor test structure. The dark strip is the platinum strap connecting the aluminium terminals.*

Figure 6.28 also shows the predicted line resistance determined from the linear fit to the sheet resistance date in figure 6.22. The measurement results are all within 10% of the predicted value except for those taken from the strap with the shortest deposition time. The thickness of the platinum tracks was measured using a Veeco Dektak surface profiler and the results are presented in figure 6.29(a). The film thickness data can then be used to calculate the resistivity of the conducting material assuming the linewidth is

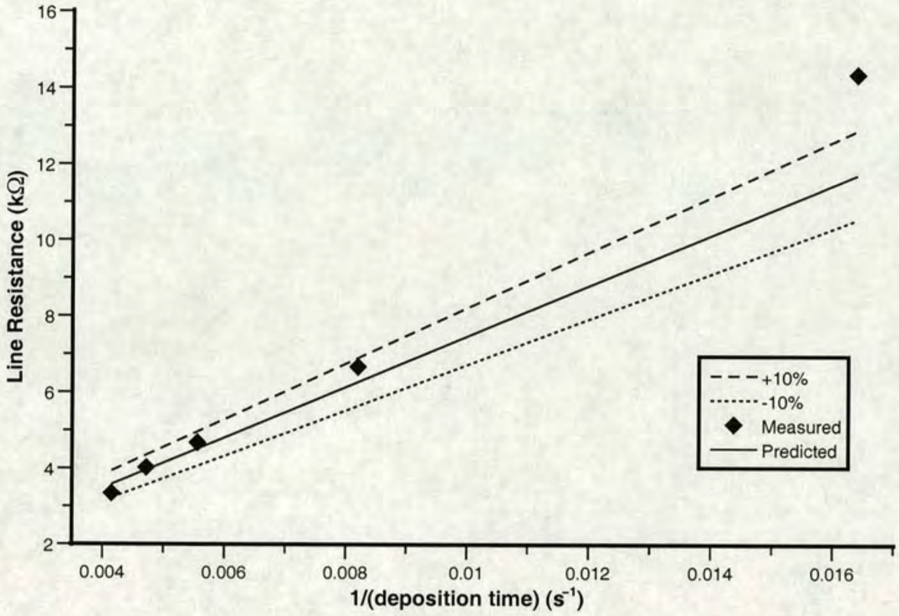
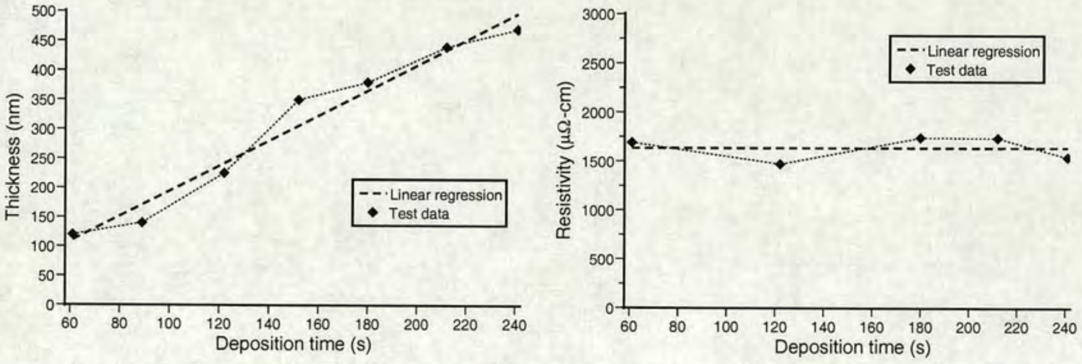


Figure 6.28: *Resistance versus the inverse of of deposition time for Kelvin bridge resistor structures including the predicted line resistance.*

0.5μm. These figures are plotted against deposition time in figure 6.29(b).

The resistivity should be a constant if the process parameters of deposition area and beam current are also constant. The results in figure 6.29(b) suggest that the resistivity is independent of the deposition time with $\rho_{mean} = 1630\mu\Omega$-cm and $\sigma_\rho = 123\mu\Omega$-cm.



(a) (b)

Figure 6.29: *(a) Film thickness of Kelvin bridge structures measured with Dektak against deposition time. (b) Resistivity of FIB platinum plotted against deposition time.*

6.3.6 Conclusions and Further Work

A methodology has been presented which allows the measurement of the sheet resistance of platinum films created by focused ion beam deposition. The geometry of the test structures can lead to errors in the extracted value of R_S and these have been quantified by simulations which showed that the errors reduce as the platinum box size increases. Further simulations which investigated the effects of misalignment on the measurement accuracy have also shown that the effects of alignment errors are minimised with larger structures.

An initial set of box cross test structures were fabricated with a platinum deposition area of $64\mu\text{m}^2$. The results indicated that the sheet resistance was, as expected, inversely proportional to the deposition time. This indicates that the deposition rate and material resistivity are constants for structures with the same area deposited using the same ion beam current.

Simulations of box cross structures fabricated with the wafer rotated through $45°$ indicate that accurate values of R_S can be extracted even when the dimensions of the box are much smaller than required with the original, orthogonal structures. Electrical measurements of diagonal box crosses again indicated that sheet resistance is inversely proportional to deposition time. The results of these measurements were used to estimate the resistance of platinum tracks deposited with the same process parameters.

A set of platinum Kelvin bridge resistor structures were fabricated with the same area and using the same beam current as the diagonal box cross structures. The results of electrical measurements have shown that it is possible to predict, with some accuracy, the resistance of the track from the sheet resistance data obtained from the diagonal box crosses. However, the deposition area of the strap must be the same as that of the box section of the cross and the same beam current setting must be used. Dektak profile measurements have confirmed that the thickness of the deposited material is, as expected, directly proportional to the deposition time and that the resistivity is a constant.

Further work will include the design and fabrication of a new mask for the aluminium layouts which takes into account the results presented in this section. For example, the layouts for box cross structures will not require the wafer to be rotated in the FIB chamber while the bridge structures will allow Kelvin measurements without the need for alteration of the aluminium layout.

Chapter 7
Conclusions and Future Work

This thesis has presented the results of investigations into a range of different applications for cross-type sheet resistance test structures and cross-bridge electrical linewidth structures. This chapter begins by briefly covering the important conclusions made in each of the preceding chapters. It will then go on to describe some areas for future investigation that have been suggested by this work.

7.1 Conclusions

7.1.1 Copper Damascene Interconnect

Computer simulation was used in Chapter 3 to investigate the effects of dishing and diffusion barrier layers on the measurement of sheet resistance and linewidth in a copper damascene metallisation process. Barrier layers are included to prevent the diffusion of copper into the dielectric but can have a significant effect on the resistance of interconnect as dimensions are reduced. The error due to the effect of barrier layers on the extraction of sheet resistance from a Greek cross was found to be less than 1% of the nominal value of R_S when the condition given by equation 3.1 is met. The box cross structure is insensitive to the effects of the barrier layers because the dimensions of the box section, where the voltage is sensed, do not vary as the arm width is changed.

The sheet resistance extracted from an appropriately designed cross is that of the copper in parallel with the underlying barrier. There is a problem with using this value in the calculation of electrical linewidth because the resistance of the bridge section also includes the sidewall barrier layers. However, if the width of the sidewall barriers is constant then this effect can be factored out through the measurement of two tracks of different widths.

Dishing, which thins the centre of a copper damascene track, occurs during CMP polishing and is a function of the width of the feature. A model of dishing was used to simulate cross-type test structures with different arm widths and different levels of overpolishing. The results showed that there was a constant offset between the sheet resistance extracted from a dished Greek cross and the effective sheet resistance of a copper track with the same minimum dimension. An even larger offset, which varied with feature size, was observed with the results from the simulated box cross structures. This was due to heavy dishing of the box section of the structure.

Further simulations were performed using structures with both barrier layers and dishing. The results showed that the effects of barrier layers dominate when the dimensions are small while dishing has more effect on Greek cross structures with wide arms. The sheet resistance extracted from box cross structures is not affected by the width of the cross arms. The final conclusion of this work was that accurate measurement of electrical linewidth in a copper damascene process requires cross-bridge test structures where the arms of the Greek cross are the same width as the bridge section while still meeting the condition for minimum width.

7.1.2 Linewidth Metrology Standards

Chapter 4 presented the motivation for the development of CD metrology standards and introduced the use of mono-crystalline silicon electrical linewidth test structures for this purpose. This chapter went on to describe computer simulations which modelled the effects of process and testing parameters on the extraction of sheet resistance and linewidth from such structures.

The initial simulations were of a simple silicon bar surrounded by silicon dioxide. The effect on the resistance of this silicon track of the dimensions, the surface charge at the Si/SiO_2 interface, the doping concentration, temperature and measurement voltage were investigated. It was found that the surface charge affects the variation of the resistance with width and measurement voltage. More importantly, it was demonstrated that the effects of the surface charge can be effectively eliminated by heavily doping the silicon.

Further simulations were performed using a Greek cross structure which mimics the geometry of the (110) mono-crystalline structures developed at NIST. The simulation structure included a "gate" electrode which enabled the effect of biasing the substrate of an SOI wafer to be investigated. A negative bias on this electrode causes depletion in the cross structure and the depletion depth reaches its maximum value for the doping level used at a bias of -2.5V. This leads to an alteration in the effective geometry of the cross making it appear more asymmetrical.

The effect of fixed charge at the silicon/SiO_2 boundary was also simulated and was found to have a similar effect to biasing the gate electrode. These effects arise during processing or testing and appear to have a strong influence on the measurements. The results from the bar simulations showed that these unwanted effects are dependent on the doping of the silicon and so further simulations of the cross structures were performed with higher carrier concentrations. These results showed a much lower variation in the extracted sheet resistance with gate bias but the value of R_S was also reduced to a level which would require the use of a voltmeter with sub-μV resolution to make the measurement. As a result of these studies, the doping concentrations used in the structures made at NIST have been increased in their more recent work.

7.1.3 Phase Shifting Mask Metrology

The use of electrical linewidth test structures for alternating phase shifting mask metrology was investigated in section 5.2. A state-of-the-art mask was fabricated featuring a large number of on-mask test structures with a range of different linewidths and mark to space ratios. Some of the structures were binary and some phase shifted. The mask is capable of being used to print test structures which can also be electrically tested. Initial electrical testing of the structures showed that the chromium oxide anti-reflective coating led to probing and repeatability problems. This layer was subsequently removed by a wet etch process.

Analysis of sheet resistance measurement results showed that the repeatability can be improved by the careful choice of force current and through the use of large cross structures. In addition, phase shifting elements were found to have an undesirable effect on the geometry of the L-type cross structures and so this arrangement should not be used in future.

The linewidths of one complete set of binary and one set of phase shifted structures were measured electrically and with a CD-SEM system. The electrical results show that there is a systematic offset between the designed width and the ECD. There is also an offset between the phase shifted and binary results which suggests that the fabrication of the phase shifting elements has some effect on the chrome features. Measurement of dense linewidth structures revealed a proximity effect in the mask making process which meant that the more closely spaced lines are wider than those that are widely spaced.

There is an offset between the results obtained with different methods, such that the tracks appear to be wider when measured with the SEM than when measured electrically. This is especially true for the phase shifted structures which the CD-SEM results show to be wider than the binary tracks. This is the exact opposite of the electrical results and suggests that the phase shifting elements affect the determination of the line edge position. In addition the SEM measurements were affected by charging of the mask which led to a loss of resolution and slow testing. The conclusion is that on-mask electrical linewidth measurements can be used for PSM metrology with confidence and indeed may be more useful than the standard CD-SEM technique which appears to be confused by the phase shifting elements.

7.1.4 Optical Proximity Correction

Section 5.3 examines the effects of applying optical proximity correction to electrical linewidth test structure layouts. Computer simulation of the photolithographic process was used to generate two-dimensional boundaries for electrical modelling of the printed structure. It was found that the OPC reduced the rounding in the internal corners of the structure and reduced the value of line shortening δL. The concern was that the OPC would lead to a reduction in the bridge width close to the voltage taps but this was not observed.

This section of the thesis also presented the results of simulations of Greek cross test structures with extremely large asymmetries. Sheet resistance correction factors for values of F_A over 70% were calculated and it was shown that these could be used with confidence. The suggestion is that all eight possible measurement orientations should be used to obtain the best accuracy.

Further simulations of the effects of OPC on a Greek cross structure were performed and in this case, where the original layout is symmetrical, it was found that the OPC does not have a significant effect on the symmetry of the resulting structure.

7.1.5 Characterisation of a Wet Etch Process

Chapter 6 presented two examples of the use of resistive test structures to characterise fabrication processes. The first of these examines the use of cross-bridge linewidth structures to evaluate the effects of a TMAH based, silicon bulk etch solution on aluminium metallisation.

A number of test wafers were prepared with test structures fabricated using different metallisation processes: RIE aluminium, RIE Al/1%Si and damascene Al/1%Si. The RIE, or "type A" structures were etched for a total of 210 minutes and were tested electrically at regular intervals during this time. The sheet resistance measurements of pure aluminium test structures showed a linear increase over the etch time. SEM imaging of these structures showed the grain structure becoming more distinct suggesting that the metal was being etched along the grain boundaries thus reducing the average thickness. The results from the Al/1%Si structures showed an increase in R_S during the first 30 minutes of etching but little change after that. The SEM showed the surface roughness increasing at first but there was no obvious difference between the picture taken after 30 minutes and the final image. Electrical linewidth measurements of the type A structures showed that there was very little lateral etching of the tracks. The exact reason for this is unclear but the surface area of the sidewalls is smaller than the top surface and there is no visible grain structure.

Results for the damascene or "type B" test structures are unfortunately only available for 60 minutes of etching but over this time the sheet resistance increases at a similar rate to that observed with the type A structures. SEM images of these structures showed no visible grain structure and no obvious change in the surface over the hour of wet etching. There was no change in the linewidth of these structures as the sidewalls are not exposed to the etch solution.

7.1.6 FIB Deposited Platinum Characterisation

The second example in chapter 6 presents a methodology for the characterisation of the sheet resistance of platinum deposited in a focused ion beam system. A mask layout has been developed for aluminium features which form the connections and probe pads of cross and bridge-type test structures. These test structures are completed by the deposition of rectangular areas of platinum between the aluminium taps.

Box cross structures were fabricated and tested. The results show that the sheet resistance of the platinum is inversely proportional to the deposition time if the other process parameters are kept constant. Simulation of the geometry of these initial structures showed that there are systematic errors which depend on the size of the box and the overlap of the aluminium taps. Further simulations of structures with the box section rotated so that the taps are at the corners showed much less sensitivity to the size and alignment of the platinum deposition. A number of these diagonal box cross structures were fabricated and the sheet resistance measured.

Bridge structures with a deposition area equal to the box section of the diagonal box cross structures were fabricated with the same beam current. The results of Kelvin measurements show that the resistance of a platinum strap can be predicted using the results from sheet resistance structures but the deposition areas must be the same. The thickness of each bridge deposition was measured using a surface profiler and it was shown to increase linearly with deposition time. The resistivity of the platinum was calculated from these results and was shown to be constant.

7.2 Future Work

A number of suggestions for further work in the area of microelectronic test structures have arisen from the work presented in this thesis. First of all, in chapter 3, simulation is used to investigate the measurement of linewidth in a copper interconnect process. There is plenty of scope for a further investigation examining these issues in a real process in an attempt to confirm that the methodology and conclusions drawn from the simulation results are valid.

Further work is required using the alternating phase shifting photomask from chapter 5.

Although on-mask measurements have been used to extract a great deal of information about the mask-making process and the viability of ECD metrology the usefulness of this for assessing the capability of the mask is not clear. The mask should be used to print structures which can either be measured electrically or by CD-SEM extraction from the final test structures or from photoresist images. These measurements should be compared with the on-mask results to provide information about the MEEF of the photolithographic process and the usefulness of the electrical results.

The on-mask electrical measurements revealed that the etching of the phase shifting elements affects the electrical width of the bridge resistor structures. This effect could be used to design a test structure which could electrically measure any errors in the alignment between the chrome features and the phase shifters. The structure would be based on the differential bridge structure described in section 2.3.2 and would be measured in the same way. A suggested layout for this structure can be seen in figure 7.1.

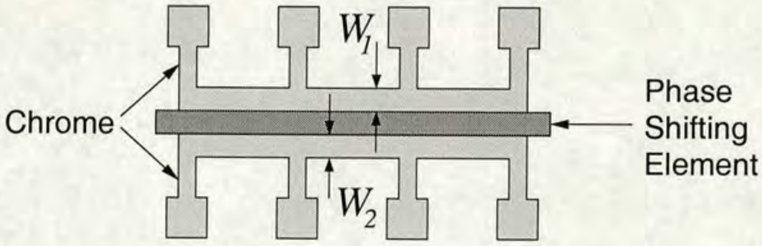


Figure 7.1: *Schematic diagram of a differential bridge test structure for phase shifting mask alignment metrology*

The work on platinum test structures fabricated by focused ion beam induced deposition has shown that the sheet resistance can be characterised accurately with box cross structures where the aluminium taps connect to the corners of the platinum deposition. The original aluminium test mask layout requires that the wafer be rotated through 45 degrees in the FIB chamber before deposition. A new test pattern should be designed which does not require this intervention. In addition, the revised layout should include structures which will allow the fabrication of four-terminal Kelvin bridge resistors without requiring an additional processing step in the FIB. The range of tap spacings included in the new mask should be chosen with reference to the results of the diagonal box cross simulations and consideration of the likely requirements for strap deposition areas in integrated circuit modification.

7.3 Final Conclusions

The work presented in this thesis has shown that sheet resistance and electrical linewidth test structures can be applied to a number of advanced microelectronic fabrication processes. Historically, bridge ECD structures have not been as widely used as the optical and CD-SEM techniques, mainly because they can only be fabricated in conducting layers. However, as this work has demonstrated, they do have the high repeatability required for metrology in the future. In addition, one of the most important applications for CD metrology is in interconnect characterisation and electrical measurement is more appropriate for this than the physical measurement techniques. The accurate measurement of sheet resistance has been shown to be essential for ECD extraction using the single bridge test structure, and this is strongly affected by non-uniformities introduced in advanced technologies such as copper interconnect. Although these test structures are some of the earliest to be developed they still have important applications today and will almost certainly remain as important in the future.

Future CD measurement techniques have to be capable of measuring linewidths of 25nm with an uncertainty of 2.5nm by 2007 [13]. This thesis has analysed and characterised test structures for the electrical measurement of linewidth, providing a greater insight into their operation. The results of this study will help to develop the appropriate metrology for future device technologies.

Appendix A
Supplementary Information

A.1 Resistance Measurements

The measurements made on the test structures investigated in this thesis are almost all resistance measurements. These are typically made, as in an ohmmeter, by forcing a known current I through the structure and measuring the resulting voltage V. The resistance is simply $R = V/I$. The simplest may to perform such a measurement is the two-wire method illustrated in figure A.1 [159].

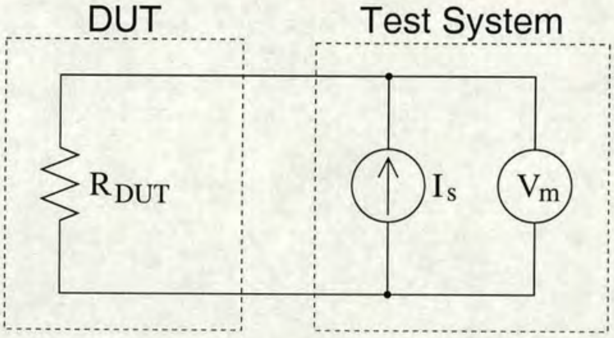


Figure A.1: *Two-wire resistance measurement. Force current I_s, measure voltage V_m.*

The problem with making the measurement in this way is that the voltmeter will sense the voltage drop caused by the Device Under Test (DUT) in series with the resistance of all the connections between the system and the DUT. If the resistance being measured is small (typically below 1Ω) then this will lead to a significant error in R_{DUT}. In such cases the four-wire or Kelvin measurement technique should be used. In this set up the voltmeter should be connected as close to the device as possible as in figure A.2.

If the resistance of the voltmeter is much greater than that of the DUT, i.e. $R_{VM} \gg R_{DUT}$, the current through the meter and the leads will be neglible and the measured voltage V_m will be the same as the voltage across the resistor. One other important consideration in resistance measurements is voltage offsets either in the test system

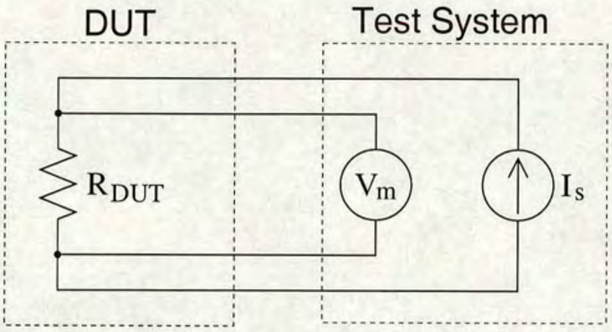


Figure A.2: *Kelvin resistance measurement. Force current I_s, measure voltage V_m.*

or thermal EMFs caused by the contact between different metals at the probe pads. These can generally be cancelled by repeating each measurement with the current flow reversed and averaging the two results. All of the electrical measurement results in this thesis have been obtained in this way.

A.2 Test Equipment

A.2.1 HP4062B Semiconductor Parametric Test System

The 4062B is a computer controlled test system made up of four main components: [160]

- 4084B Switching Matrix Controller
- 4085A Switching Matrix
- 4141B DC Source/Monitor
- 4280A Capacitance Meter/C-V Plotter

It is controlled using an HP 9000 Series 300 computer running HP BASIC 5.1 via a IEEE488 HPIB (Hewlett Packard Interface Bus). This is the main system used to make the resistive measurements presented in this thesis, however the 4280A was not used as no capacitive measurements were required.

The 4085A and 4084B are used to make the connection between the measurement instruments and the device being tested. The switching matrix has a total of 48 measurement pins available which are controlled electronically through a system of relays. Connection to a probe card on a wafer prober is made via an edge connecter and shielded leads from a test fixture on the 4085A. This allows any needle on the probe card to be connected to any part of the test system.

The 4141B has four Source/Monitor Units (SMUs) which can be used to force or measure voltages or currents. For DC resistive measurements they are typically used to force currents and measure voltages as in section A.1. It also includes two dedicated voltage sources (VSU), two voltage monitors (VMU) and a ground unit designed to be used as the ground connection in a measurement. The range of force currents available from one of the SMU runs from ±100mA to ±1000pA with a four digit resolution. The voltage resolution of the SMU is 1mV with a range of ±20V. A better voltage resolution of 0.1mV on a range of ±2V is provided by the VMUs.

A.2.2 Solartron Microvoltmeter

The voltage sensing resolution of the SMUs and VMUs in the 4062B system is not good enough for sheet resistance measurements made on van der Pauw cross-type test structures. For example, an aluminium cross structure was measured and found to have a sheet resistance of about $0.04\Omega/\square$. The measurement current used was 5mA and the resulting voltage measured was $\sim 44\mu$V. This required the use of a Solartron 7055 Microprocessor Voltmeter which has a sensitivity of 1μV on a range of ±10mV [161]. The Solartron can be controlled by the HP 9000 computer via an HPIB connection and so it is easily integrated into the measurement system.

A.2.3 HP4156B Precision Semiconductor Parameter Analyser

The 4156B is a electrical test system in a single unit with an LC display [162]. It can be controlled and programmed either from the front panel or from an external PC keyboard. In addition it can be controlled by a computer via an HPIB or LAN connection. The 4156B has four SMUs, 2 VMUs and 2 VSUs as in the 4141B DC Source Monitor described above. These SMUs have a higher resolution than those in the 4062B system, the voltage sensing resolution can be as good as 2μV with a range of ±2V using the longest possible measurement integration time [163]. The VMUs also have a similar voltage resolution and so the system has the capability of making sheet resistance measurements as described in section A.2.2. This system, along with a manual probestation, can be used to make rapid, multiple measurements and to perform sweeps of the forcing current when the high accuracy and precision of the 4062B is not required.

A.3 Simulation Software

Simulation software produced by Avant! (previously Technology Modelling Associates) was widely used in the work presented in this thesis. This section gives a brief description of the main features of each piece of software that was used. The simulations were performed on Sun Microsystems Ultra 10 workstations using the Solaris operating system.

A.3.1 TWB

TWB or Taurus WorkBench is not actually a simulator but provides a user interface for the integration of simulation and visualisation software [164]. It is typically used as a "virtual factory" environment where process simulators are used to model a process flow before device simulation software is used to extract the electrical characteristics. TWB can also be used to automate the design of experiments and the statistical analysis of the results. It was used in a similar manner for the work in this thesis as it allows many simulations to be run simultaneously across the network and speeds the extraction of results and visualistion of structures.

A.3.2 Raphael

Raphael is an interconnect simulator which can be used to analyse the electrical and thermal characteristics of two and three-dimensional structures [165]. There are five different solvers in the Raphael package but only two have been used in the course of this work, one 2-D and one 3-D. Both of these use the finite difference method and an automatically generated rectangluar grid to solve Poisson's equation for the simulated structure. The structures simulated for this work were typically resistive with

2-4 terminals. The simulator allows the resistivity of the conducting material to be set and voltages to be applied to the electrodes. The current flow around the structure is then calculated and potentials at any point in the simulation grid can be extracted.

A.3.3 Davinci

Davinci is a three-dimensional semiconductor device simulator [166] which can be used to model MOS and bipolar transistor behaviour. It solves the Poisson equation for the simulated structure and in addition the electron and hole carrier continuity equations. The user has a lot more control over the grid than in Raphael, and this allows the grid density to be concentrated on the areas of interest. Each region of the structure can be specified as a semiconductor, an insulator or an electrode. In addition, a number of default materials such as silicon, SiO_2 and silicon carbide have their important parameters pre-programmed into the simulator. The extrinsic carrier concentration can be set for each region of the structure defined as a semiconductor and new materials can be defined by changing the default parameters.

A.3.4 Depict

Depict is a suite of programs which can be used to simulate advanced photo-lithograpic processes [167]. The first, and most important part of Depict is the aerial image module which takes a mask layout and produces a profile of the light intensity at the image plane of the projection. This allows control of all the parameters of the stepper being simulated and can also be used to investigate advanced mask technologies such as phase shifters and sub-resolution assist features. The aerial image simulator also includes a module which will apply an optical proximity correction algorithm to a mask design in order to increase printability. The second section of the Depict suite allows the modelling, in three-dimensions, of the effect of the aerial image on photoresist. This includes simulation of the development process and the result is a 3-D representation of the photoresist surface.

A.3.5 Michelangelo

Michelangelo is a GUI based tool which allows the visualisation and editing of simulated device structures created with other TMA/Avant! software [168]. It can be used to interactively regrid structures created in the two-dimensional process and device simulators or to change the coping of regions. In addition Michelangelo can be used to plot the results of electrical simulations or any other data such as doping profiles.

A.3.6 Medici

Medici is a two-dimensional semiconductor device simulator similar to Davinci and it solves the Poisson and carrier continuity equations in a similar way [169]. Medici is typically used to simulate structures created through process simulation with TSUPREM-4 [170]. However, it can also be used to simulate a structure created with Michelangelo or from a text file giving the coordinates of points on the boundary of the structure.

Appendix B
Published Papers

The following are papers written by the author associated with this thesis which have been presented at an international conference or have been published in a peer reviewed journal.

S. Smith, I.A.B. Lindsay, A.J. Walton, M.W. Cresswell, L.W. Linholm, R.A. Allen, M. Fallon and A.M. Gundlach; "Analysis of Current Flow in Mono-Crystalline Electrical Linewidth Structures", International Conference on Microelectronic Test Structures, pp. 7-12, March 15-18 1999. *See figures B.1 to B.6.*

S. Smith, A.J. Walton and M. Fallon; "Investigation of Optical Proximity Correction (OPC) and Non-Uniformities on the Performance of Resistivity and Linewidth Measurements", International Conference on Microelectronic Test Structures, pp. 161-166, March 15-18 1999. *See figures B.7 to B.12.*

K. Lian, S. Smith, N.S. Rankin, A.J. Walton, A.M. Gundlach and J.T.M. Stevenson; "Characterisation of Aluminium Passivation for TMAH Based Anisotropic Etching for MEMS Applications", International Conference on Microelectronic Test Structures, pp. 210-214, March 13-16, 2000. *See figures B.13 to B.17.*

S.Smith, J.T.M. Stevenson, A.J. Walton, A.M.Gundlach, P. Christie and S.A. AbuGhazaleh; "Computer Generated Holograms for use as Microelectronic Test Structures", Second Conference on Postgraduate Research in Electronics, Photonics and Related Fields, PREP 2000, pp. 165-170, April 11-13, 2000. *See figures B.18 to B.23.*

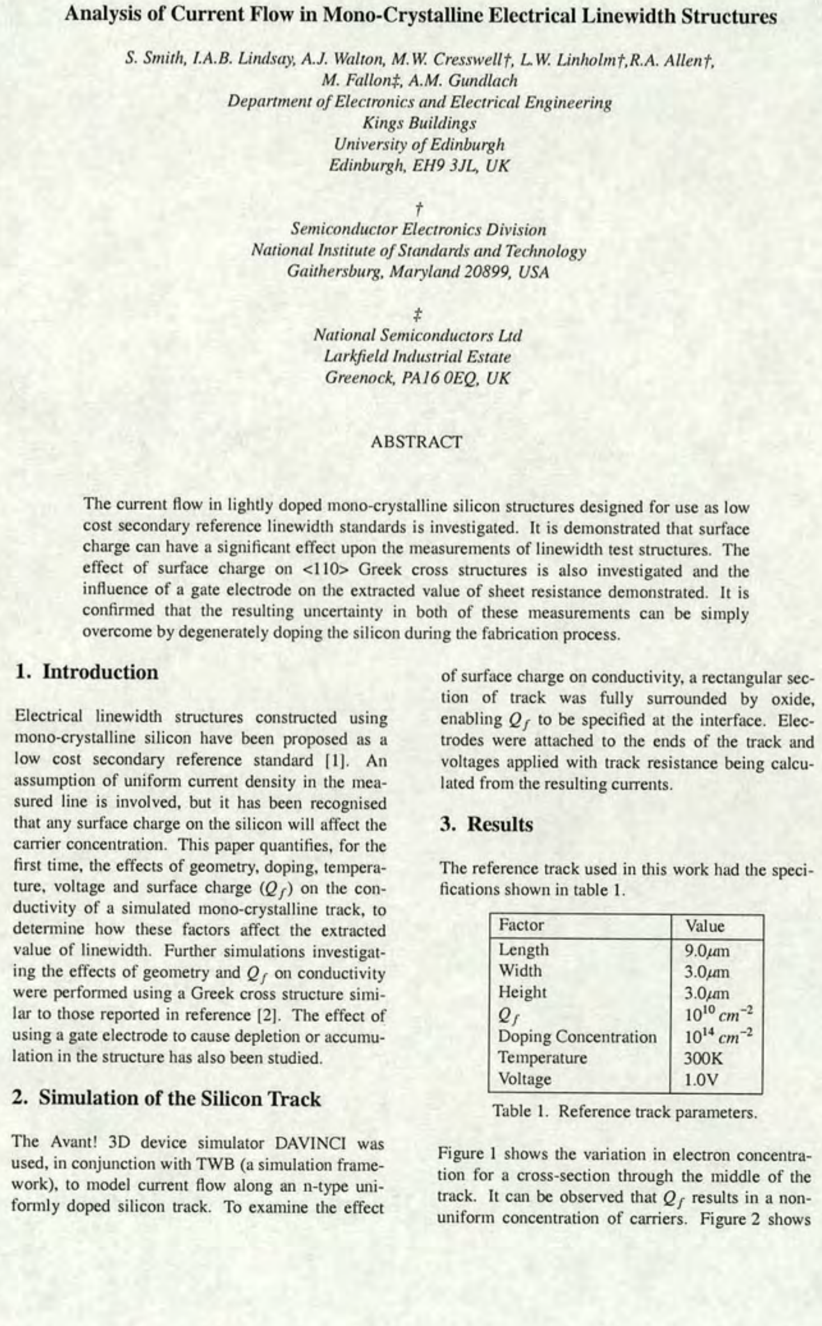
S.A. AbuGhazaleh, P. Christie, V. Agrawal, J.T.M. Stevenson, A.J. Walton, A.M. Gundlach and S.Smith; "Null Holographic Test Structures for the Measurement of Overlay and Its Statistical Variation", IEEE Transactions on Semiconductor Manufacturing, Vol. 13, No. 2, pp. 173-180, May 2000. *See figures B.24 to B.31.*

S.Smith, A.J. Walton, A.W.S. Ross, G.K.H. Bodammer and J.T.M. Stevenson; "Evaluation of the Issues Involved with Test Structures for the Measurement of Sheet Resistance and Linewidth of Copper Damascene Interconnect", International Conference on Microelectronic Test Structures, pp. 195-200, March 19-22 2001. *See figures B.32 to B.37.*

S. Smith, M. McCallum, A.J. Walton and J.T.M. Stevenson; "Electrical CD Characterisation of Binary and Alternating Aperture Phase Shifting Masks", International Conference on Microelectronic Test Structures, pp. 7-12, April 8-11 2002. *See figures B.38 to B.43.*

S. Smith, A.J. Walton, S. Bond, A.W.S. Ross, J.T.M Stevenson, A.M. Gundlach; "Test Structures for the Electrical Characterisation of Platinum Deposited by Focused Ion Beam", International Conference on Microelectronic Test Structures, pp. 157-162, April 8-11 2002. *See figures B.44 to B.49.*

S.Smith, A.J. Walton, A.W.S. Ross, G.K.H. Bodammer and J.T.M. Stevenson; "Evaluation of Sheet Resistance and Electrical Linewidth Measurement Techniques for Copper Damascene Interconnect", IEEE Transactions on Semiconductor Manufacturing, Vol. 15, No. 2, pp. 214-222, May 2002. *See figures B.50 to B.58.*



Analysis of Current Flow in Mono-Crystalline Electrical Linewidth Structures

S. Smith, I.A.B. Lindsay, A.J. Walton, M.W. Cresswell†, L.W. Linholm†, R.A. Allen†,
M. Fallon‡, A.M. Gundlach
Department of Electronics and Electrical Engineering
Kings Buildings
University of Edinburgh
Edinburgh, EH9 3JL, UK

†
Semiconductor Electronics Division
National Institute of Standards and Technology
Gaithersburg, Maryland 20899, USA

‡
National Semiconductors Ltd
Larkfield Industrial Estate
Greenock, PA16 0EQ, UK

ABSTRACT

The current flow in lightly doped mono-crystalline silicon structures designed for use as low cost secondary reference linewidth standards is investigated. It is demonstrated that surface charge can have a significant effect upon the measurements of linewidth test structures. The effect of surface charge on <110> Greek cross structures is also investigated and the influence of a gate electrode on the extracted value of sheet resistance demonstrated. It is confirmed that the resulting uncertainty in both of these measurements can be simply overcome by degenerately doping the silicon during the fabrication process.

1. Introduction

Electrical linewidth structures constructed using mono-crystalline silicon have been proposed as a low cost secondary reference standard [1]. An assumption of uniform current density in the measured line is involved, but it has been recognised that any surface charge on the silicon will affect the carrier concentration. This paper quantifies, for the first time, the effects of geometry, doping, temperature, voltage and surface charge (Q_f) on the conductivity of a simulated mono-crystalline track, to determine how these factors affect the extracted value of linewidth. Further simulations investigating the effects of geometry and Q_f on conductivity were performed using a Greek cross structure similar to those reported in reference [2]. The effect of using a gate electrode to cause depletion or accumulation in the structure has also been studied.

2. Simulation of the Silicon Track

The Avant! 3D device simulator DAVINCI was used, in conjunction with TWB (a simulation framework), to model current flow along an n-type uniformly doped silicon track. To examine the effect of surface charge on conductivity, a rectangular section of track was fully surrounded by oxide, enabling Q_f to be specified at the interface. Electrodes were attached to the ends of the track and voltages applied with track resistance being calculated from the resulting currents.

3. Results

The reference track used in this work had the specifications shown in table 1.

Factor	Value
Length	9.0μm
Width	3.0μm
Height	3.0μm
Q_f	$10^{10}\ cm^{-2}$
Doping Concentration	$10^{14}\ cm^{-2}$
Temperature	300K
Voltage	1.0V

Table 1. Reference track parameters.

Figure 1 shows the variation in electron concentration for a cross-section through the middle of the track. It can be observed that Q_f results in a non-uniform concentration of carriers. Figure 2 shows

Figure B.1: *Reprint of paper presented at ICMTS 1999, page 1.*

the variation of track resistance with length and, as would be expected, this is approximately linear. Figure 3 shows the effect of linewidth on resistivity. Figure 4 examines the effect that temperature has on resistivity and, as could be predicted, it can be observed that, while the intrinsic carrier concentration is well below doping levels, the structure is relatively insensitive to temperature variation.

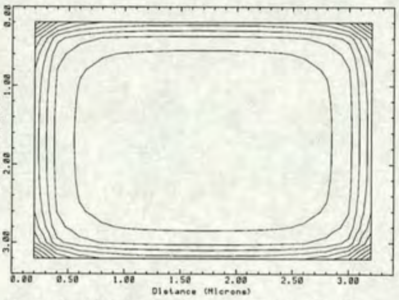


Figure 1. Variation in electron concentration for a cross-section through the middle of the track (Contours plotted 1.9×10^{14} to 1×10^{15} spacing=0.9×10^{14}).

In a real structure, it is difficult to be sure of the precise charge on the surface of the silicon. Figure 5 shows how the resistance of the track varies as a function of Q_f. This variation is not surprising, considering the effect that Q_f has upon carrier distribution, shown in figure 1. The measurement of linewidth is further complicated by the resistivity also being a function of the applied voltage, as shown in figure 6.

It is proposed that the sensitivity of resistance to both voltage and Q_f could minimised by heavily doping the track. Figure 7 shows the variation of track resistance with Q_f, providing confirmation.

4. Simulation of Greek Cross Resistors

DAVINCI and TWB were used again, to model the behaviour of the the diagonal cross structure fabricated in <110> silicon [1]. This cross has the arms at 70° (110°) to each other, rather than at the 90° of more conventional structures. Figure 8 shows the top surface (XY plane) of the 3D structure, which measures approximately $14\times15\mu m$. The thickness of the cross structure being simulated is $1\mu m$ in the Z direction, with a $0.2\mu m$ layer of oxide underneath. On the bottom, covering the entire back of the structure, is a gate electrode which can be biased as required.

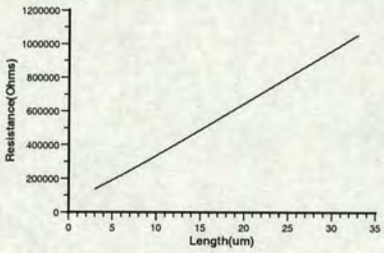


Figure 2. Variation of track resistance with length.

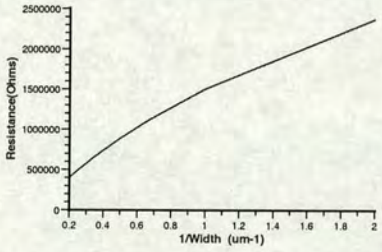


Figure 3. Variation of track resistance with linewidth.

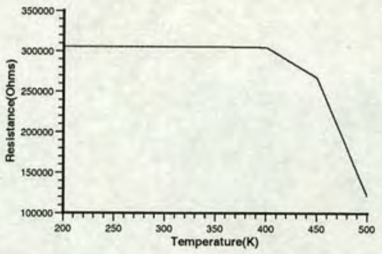


Figure 4. Variation of track resistance with temperature.

The grid generated for this structure has a total of 23,611 nodes and with the maximum number of nodes available within the DAVINCI simulator being 30,000 this gave little opportunity to to significantly increase the mesh density. The DAVINCI simulator only has available right angled triangular prismatic elements which means that obtaining a 70° angle between the arms of the cross puts a further limit on exactly how the grid can be constructed and modified. The 70° angle was achieved

Figure B.2: *Reprint of paper presented at ICMTS 1999, page 2.*

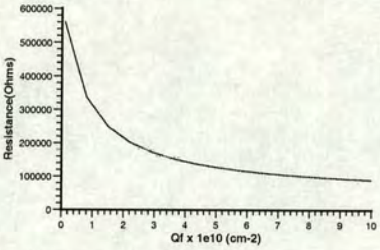


Figure 5. Variation of track resistance with Q_f.

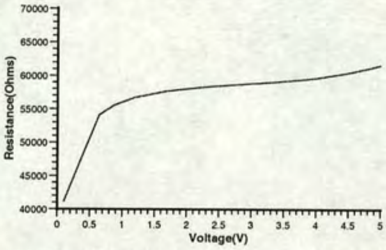


Figure 6. Variation of track resistance with applied voltage.

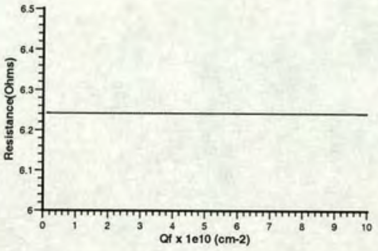


Figure 7. Variation of track resistance with Q_f for 1×10^{19} doped silicon.

by setting the ratio between the X and Y grid pitches to $X = 0.1\mu m$ and $Y = 0.275\mu m$ resulting in an angle of approximately 70.017°. The node spacing in the Z direction was set to $0.2\mu m$ making 5 layers in the silicon cross plus the layer of oxide mentioned above.

As well as this basic cross structure, a cross with facets in the acute angles was also simulated. Due to limitations imposed by the elements available in DAVINCI it is not possible to construct the elements to present a smooth facet. As a result it has been approximated to a series of 5 stepped levels, as can be seen in figure 9. It can also be observed that the edge of each layer of the facet also has to be stepped to fit the grid in the XY plane.

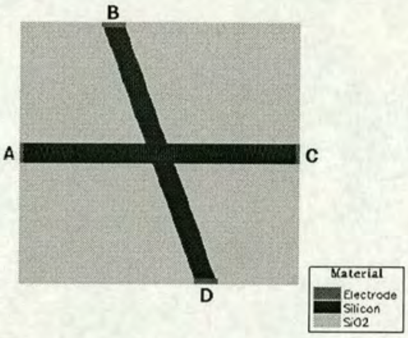


Figure 8. Plan view of the simulated Greek cross without facets and with asymmetric arms at 70° to each other.

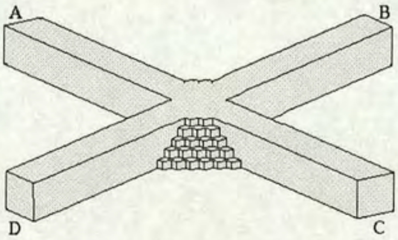


Figure 9. Schematic 3D view of the Greek cross structure with facets in the acute angles between the arms.

The method for extracting the sheet resistance from a 4 terminal resistor has been described by Buehler [3]. This requires four measurements at different orientations for the calculation of sheet resistance and table 2 shows the terminals used for forcing current and measuring voltage for each of the four orientations. The sheet resistance is then simply calculated using

Figure B.3: *Reprint of paper presented at ICMTS 1999, page 3.*

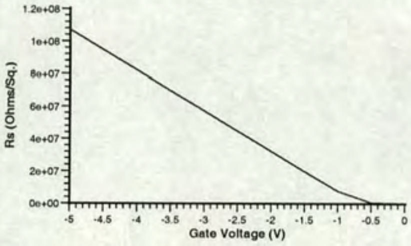


Figure 12. Variation of sheet resistance (R_s) with negative gate voltage for the structure without a facet, force current = 1nA.

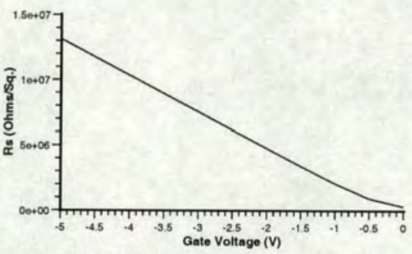


Figure 13. Variation of sheet resistance (R_s) with a negative gate voltage for the structure with a facet, force current = 0.1μA.

In both figures 12 and 13 the resistivity rises steadily as the depletion region grows and the effective thickness of the cross (Z direction) is reduced. The most interesting thing to note about these simulations is what happens to the individual resistances extracted at the four measurement orientations. Figures 14 and 15 show these individual resistances plotted against negative gate voltages. For the structure without the facet there are noticeable differences between R1 and R2, and R3 and R4. It is not believed that these differences are grid related as this effect was not observed when biasing in accumulation. However, it was not possible to confirm if any of this difference was attributable to the grid because of DAVINCI's node limitation. In figure 15 it is even more obvious that reciprocity is no longer obeyed. The complex interaction between the thinning of the cross due to depletion and the facet means that the structure effectively changes shape, as well as thickness, which may well be the cause of this non-linear effect.

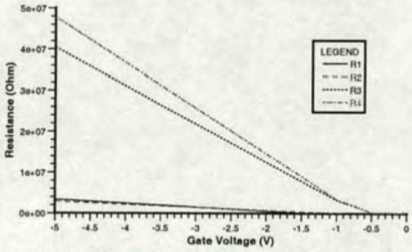


Figure 14. Resistances (R1-R4) measured for negative gate voltages on the structure without a facet.

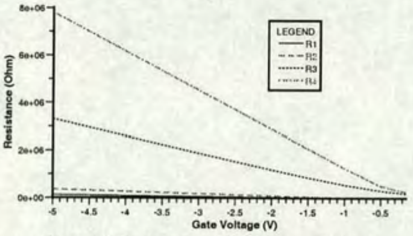


Figure 15. Resistances (R1-R4) measured for negative gate voltages on the structure with a facet.

Simulations to study effects of surface charge on the operation of the cross resistor were also performed. Note that in these simulations there was no Q_f on the top surface of the cross. Figures 16 and 17 show sheet resistance as a function of Q_f for both types of structure. It can be seen that changing Q_f on these crosses does not effect such a marked change in resistivity as that observed for the silicon track shown in figure 5. This is probably because the resistance being measured is effectively only in a small area in the middle of the cross, where the only large boundary with charge on it is at the bottom of the structure. Figure 18 shows the variation of R_s with positive gate voltage for both the structures with a Q_f of $5 \times 10^{10}\text{cm}^{-2}$. The effect of this charge is to reduce the maximum R_s value (at $V_g = 0V$) to less than half that for the simulations with no Q_f.

In order to make the structure insensitive to the effects of accumulation, depletion or surface charge the Greek cross structure can be highly doped. A simulation was performed on a cross with a uniform doping of $6.244 \times 10^{19}\text{cm}^{-3}$, which gave a nominal R_s of 1Ω/□ for $1\mu m$ thick silicon. As expected it was observed that changing the gate voltage no longer altered the extracted resistivity. This effect has been shown previously, for the silicon track in figure 7. The extracted sheet resistance for the cross with facets was found to be a constant 1.07Ω/□ for positive gate voltages between 0V and 5V.

Figure B.4: *Reprint of paper presented at ICMTS 1999, page 4.*

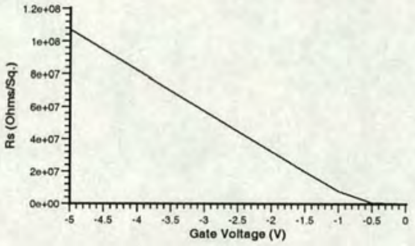


Figure 12. Variation of sheet resistance (R_s) with negative gate voltage for the structure without a facet, force current = 1nA.

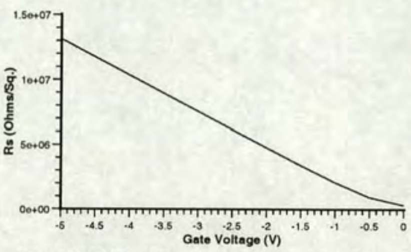


Figure 13. Variation of sheet resistance (R_s) with a negative gate voltage for the structure with a facet, force current = 0.1μA.

In both figures 12 and 13 the resistivity rises steadily as the depletion region grows and the effective thickness of the cross (Z direction) is reduced. The most interesting thing to note about these simulations is what happens to the individual resistances extracted at the four measurement orientations. Figures 14 and 15 show these individual resistances plotted against negative gate voltages. For the structure without the facet there are noticeable differences between R1 and R2, and R3 and R4. It is not believed that these differences are grid related as this effect was not observed when biasing in accumulation. However, it was not possible to confirm if any of this difference was attributable to the grid because of DAVINCI's node limitation. In figure 15 it is even more obvious that reciprocity is no longer obeyed. The complex interaction between the thinning of the cross due to depletion and the facet means that the structure effectively changes shape, as well as thickness, which may well be the cause of this non-linear effect.

Simulations to study effects of surface charge on the operation of the cross resistor were also performed. Note that in these simulations there was no Q_f on

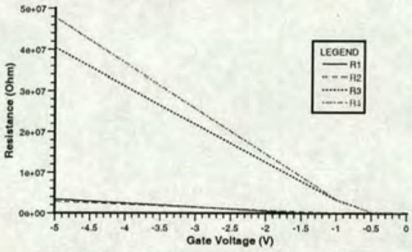


Figure 14. Resistances (R1-R4) measured for negative gate voltages on the structure without a facet.

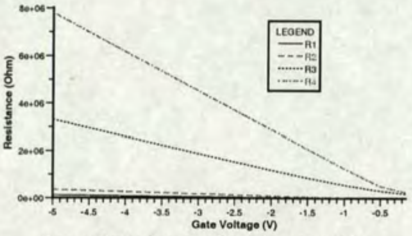


Figure 15. Resistances (R1-R4) measured for negative gate voltages on the structure with a facet.

the top surface of the cross. Figures 16 and 17 show sheet resistance as a function of Q_f for both types of structure. It can be seen that changing Q_f on these crosses does not effect such a marked change in resistivity as that observed for the silicon track shown in figure 5. This is probably because the resistance being measured is effectively only in a small area in the middle of the cross, where the only large boundary with charge on it is at the bottom of the structure. Figure 18 shows the variation of R_s with positive gate voltage for both the structures with a Q_f of $5 \times 10^{10}\text{cm}^{-2}$. The effect of this charge is to reduce the maximum R_s value (at $V_g = 0V$) to less than half that for the simulations with no Q_f.

In order to make the structure insensitive to the effects of accumulation, depletion or surface charge the Greek cross structure can be highly doped. A simulation was performed on a cross with a uniform doping of $6.244 \times 10^{19}\text{cm}^{-3}$, which gave a nominal R_s of $1\Omega/\square$ for $1\mu m$ thick silicon. As expected it was observed that changing the gate voltage no longer altered the extracted resistivity. This effect has been shown previously, for the silicon track in figure 7. The extracted sheet resistance for the cross with facets was found to be a constant $1.07\Omega/\square$ for positive gate voltages between 0V and 5V.

Figure B.5: *Reprint of paper presented at ICMTS 1999, page 5.*

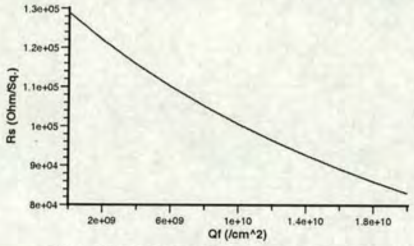


Figure 16. Variation of sheet resistance with surface charge Q_f for the structure without a facet.

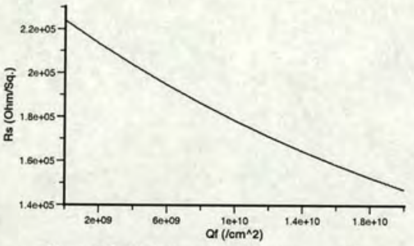


Figure 17. Variation of sheet resistance with surface charge Q_f for the structure with a facet.

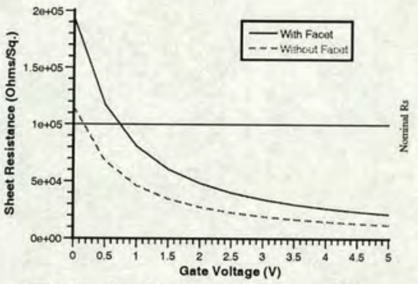


Figure 18. Variation of sheet resistance with gate voltage for both of the structures with $Q_f = 5 \times 10^{10}\text{cm}^{-2}$.

6. Conclusions

The results presented here have, for the first time, quantitatively demonstrated how charge on the surface of mono-crystalline silicon tracks can affect the value of electrically measured linewidths. This understanding helps to explain the divergence between SEM and electrical measurement methods [2]. We have also investigated the performance of the diagonal cross manufactured in <110> silicon and shown how the presence of Q_f can effect the value of R_s that is extracted. The structures that were simulated with the facets in the acute corners displayed non-reciprocity, indicating that non-linear effects are present.

This work helps to quantify this effect but the practical implementation of these results using calibration tables is limited, since any charge at the oxide-silicon interface is difficult to quantify. Obviously, the best approach to overcoming this problem is to determine the circumstances under which its effect can be minimised. To this end, the work has highlighted how heavily doping these mono-crystalline structures effectively removes the influence of Q_f on the measurement.

Acknowledgement

Staff at the University of Edinburgh would like to acknowledge the financial support of EPSRC (GR/L81000).

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3. M.G. Buehler and W.R. Thurber, "An experimental study of various cross sheet resistor test structures", *J. Electrochemical Soc - Solid State Technology*, vol. 125, no. 4, pp. 645-650, April 1978.

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Figure B.6: *Reprint of paper presented at ICMTS 1999, page 6.*

Investigation of Optical Proximity Correction (OPC) and Non-Uniformities on the Performance of Resistivity and Linewidth Measurements

S. Smith, A.J. Walton, M. Fallon†
Department of Electronics and Electrical Engineering
Kings Buildings
University of Edinburgh
Edinburgh, EH9 3JL, UK

†National Semiconductors Ltd
Larkfield Industrial Estate
GREENOCK, PA16 0EQ, UK

ABSTRACT

The effect of Optical Proximity Correction (OPC) on test structures is examined using DEPICT for the lithography simulation and MEDICI for the electrical calculations. It is concluded that OPC can be successfully used to reduce line shortening due to the voltage taps without causing necking effects on the track being measured. The effect of asymmetries (which may be introduced as a result of OPC) on the measurement of Greek crosses are also addressed and methods of accurately extracting sheet resistance from structures exhibiting these effects are discussed.

1. Introduction

As dimensions have reduced optical lithography systems have been pushed to their limit resulting in numerous technical innovations. The most major one has been the reduction in exposure wavelengths with 248nm now being common place. Deep submicron imaging has also required advances in mask technology with phase shift masks and and OPC being introduced. Electrical linewidth structures have been adapted to meet the measurement requirements [1] of smaller geometry processes but to the authors' knowledge there has been no investigation into the effect that OPC and non-uniformities may have upon their performance. Two key factors required for the accurate extraction of electrical linewidth are sheet resistance [2] and line shortening caused by voltage taps [3]. This paper investigates both parameters to ascertain the effect that different degrees of OPC have upon linewidth shortening and also the effect that non-symmetrical patterns have upon the performance of Greek cross structures.

2. The effect of OPC on tap geometry and line shortening (ΔL)

OPC works by adding serifs to external corners and removing opaque material at internal corners with the amount of material being removed or added a function of the surrounding pattern. For linewidth test structures we are mainly interested in examining the effect that OPC has on internal corners. Figure 1 shows an example of a portion of a linewidth test structure with the CAD layout and the mask geometry with OPC. It can be observed that the OPC mask narrows the mask track width in the region which is to be measured. It is therefore important to be sure that the OPC required to successfully fabricate the functional circuit does not cause necking on the fabricated test structure.

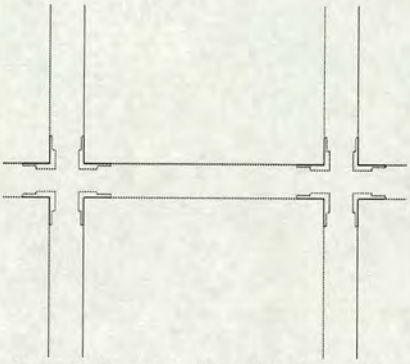

Figure 1. An example of a portion of a linewidth test structure with the CAD layout and the mask geometry with OPC.

While for simple structures such as this OPC can be performed manually on a trial and error basis we used the OPC module within DEPICT to generate

Figure B.7: *Reprint of paper presented at ICMTS 1999, page 1.*

mask designs with different degree of OPC aggressiveness. These masks were then used to calculate the aerial image and the photoresist developed. Figure 2 illustrates how the image transferred to the photoresist is affected by the degree of OPC applied.

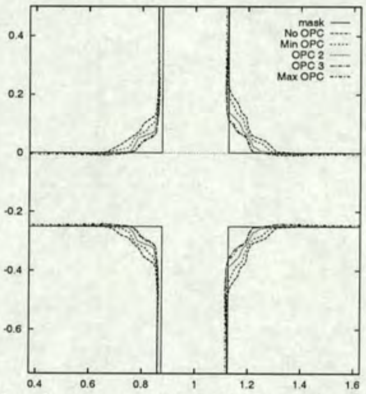

Figure 2. Illustration of how the image transferred to the photoresist is affected by the degree of OPC applied. The exposure wavelength was 248nm.

It can be observed that in the above cases OPC caused no necking of the track being measured. The resulting photoresist images, an example of which is shown in figure 3, were then used to determine the exact geometries of test structures. This provided boundary information for each of the structures which enabled the generation of grids so that the electrical performance could be simulated using MEDICI.

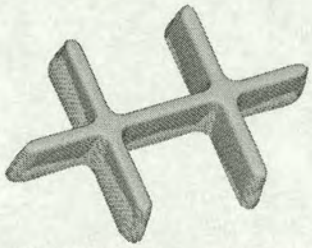

Figure 3. 3D plot of the pattern transferred into the photoresist after exposure and development of a key portion of a linewidth test structure.

The simulated resistance of the tap section of the track is shown in figure 4 for patterns obtained using masks with different levels of OPC processing. It also indicates the resistance which is extracted if the the mask geometry with no OPC is simulated.

Figure 5 gives the values of line shortening (ΔL) [4] for these cases and it can be observed that the most aggressive OPC mask correction for 248nm exposures can reduce the value of ΔL by 0.1μm. The simulation of the mask geometry provides the theoretical minimum of ΔL. Figure 6 shows the region simulated in MEDICI to obtain these results together with the voltage contours.

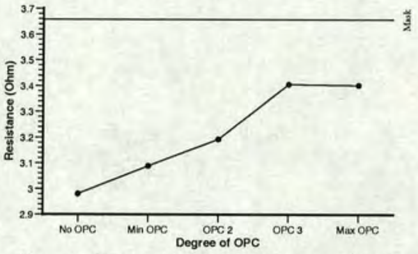

Figure 4. Simulated resistance of the tap section of the track shown in figure 2 for different degrees of OPC. The resistance extracted for the mask geometry with no OPC is also indicated.

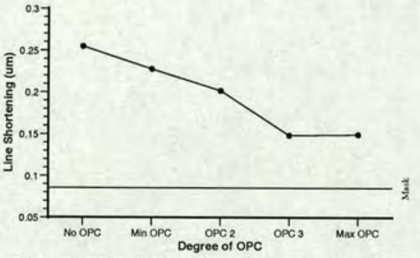

Figure 5. Simulated values of line shortening for the section of track shown in figure 2. The line shortening for the mask geometry with no OPC is also indicated.

In order to further investigate the effects of OPC on the functionality of this bridge resistor linewidth structure simulations were also performed using the whole structure. The linewidth of this structure is given by [5]

$$W = \frac{R_s L}{R} \qquad (1)$$

where R_s is the sheet resistance (Ω/□), R is the measured resistance between the taps and L is the

Figure B.8: *Reprint of paper presented at ICMTS 1999, page 2.*

distance between the centre of the taps.

Hence, both the "measured" line width and the line shortening effect [4] can be determined from simulation and figure 7 shows a typical example of the type of voltage contours obtained when simulating the operation of this linewidth structure.

To extract the line shortening effect of the voltage taps current is forced between the end terminals of the structure and the voltage between them extracted (note that the tap electrodes are left floating). This gives the track resistance, R. By assuming the linewidth is 0.25 μm and knowing the value of R_s used in the simulation an apparent length for the structure can be calculated using equation (1). The line shortening effect of one voltage tap is simply given by half of the difference between the real (4 μm) and the apparent length. Figure 8 shows ΔL for this structure for different degrees of OPC. For this full structure there is a greater ΔL at maximum OPC than for the previous simulations because part of the effect in this case comes from a thinning of the line between the voltage taps. Once the line shortening figures are known they can then be used to correct the extracted value of linewidth. Figure 9 shows the results of the linewidth measurement both with correction for line shortening and without it, assuming $R_s = 1\Omega/\square$.

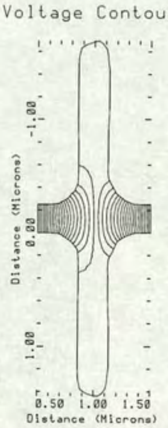

Figure 6. Contour plots of potential generated by MEDICI for one of the tap regions illustrated in figure 2.

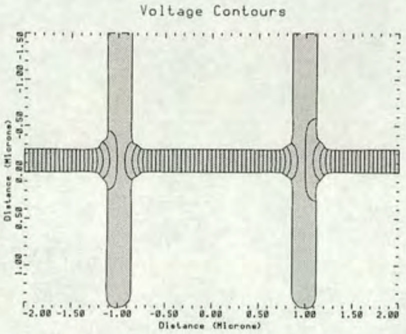

Figure 7. An example of the contour plots of potential generated by MEDICI for the whole of a linewidth test structure.

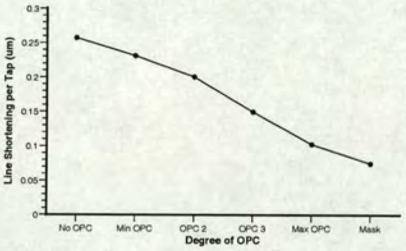

Figure 8. Line shortening derived from simulations using a full bridge resistor line-width test structure

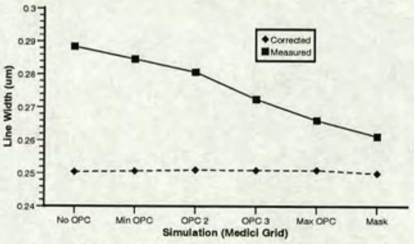

Figure 9. Results of linewidth extraction along with measurements corrected for the line shortening effects of the voltage taps.

Figure B.9: *Reprint of paper presented at ICMTS 1999, page 3.*

Structure	0°	90°	180°	270°	R_{TOT}	Percentage Asymmetry F_A (%)	Correction Factor f	Average Value R_s	Corrected Value fR_s
	$R_1 \& R_2$	$R_3 \& R_4$	$R_5 \& R_6$	$R_7 \& R_8$					
Greek 1	0.3023	0.1553	0.3023	0.1553	0.2288	64.294	0.9631	1.0369	0.9987
Greek 2	0.3230	0.1432	0.3230	0.1433	0.2331	77.135	0.9462	1.0565	0.9997
Greek 3	0.2585	0.1862	0.2585	0.1867	0.2225	32.513	0.9908	1.0079	0.9986
Greek 4	0.3146	0.1484	0.3146	0.1478	0.2313	71.807	0.9537	1.0492	1.0006
Greek 5	0.2785	0.1718	0.2785	0.1716	0.2251	47.395	0.9802	1.0205	1.0003

Table 1. Simulated resistance values and the extracted sheet resistances for the structure shown in figure 10 (The value of sheet resistance used in the simulations was 1Ω/□).

3. The effect of non-uniform pattern transfer on Greek cross sheet resistance measurements

From equation (1) it can be deduced that any inaccuracy in the measurement of sheet resistance is directly transferred in the the extracted value of linewidth [2, 6]. As geometries reduce small asymmetries at the centre of the Greek cross that were unimportant at larger dimensions have the potential to significantly affect current flows. Figure 10 gives some examples of severe asymmetries and how this affects the equipotentials of the structures.

The method for extracting sheet resistance from Greek cross structures is described by Buehler in reference [5]. Current is forced between two adjacent arms (eg north and east) and the voltage difference measured between the other two (south and west). The sheet resistance R_s is given by

$$R_s = \frac{\pi}{ln(2)} \frac{V}{I} \quad \Omega/\square \qquad (2)$$

The current direction is reversed and the measurement repeated. The current forcing terminals are moved by 90° (now south and east) and two measurements of voltage repeated as above. The sheet resistance is simply the average of these four measurements which will be identical assuming no instrumentation offsets, thermal heating etc and perfect symmetry along both the x and y axes. However, for the asymmetrical structures such as those in figure 10 this will not be the case.

The simulation results for every possible measurement combination of these structures is shown in table 1. Obviously these results do not have any instrumentation measurement problems and so reversing the current gives the same results which is why there are only four resistance columns. In addition using any pair of measurements which are at 90° results in the same sheet resistance value (reciprocity) [5]. When asymmetry is present then the sheet resistance should be combined with a correction factor to account for any asymmetries [5]. Reference [5] presented a table of correction factors for asymmetry factors (F_A) up to 14%. Table 2 extends this for values of F_A over 70%.

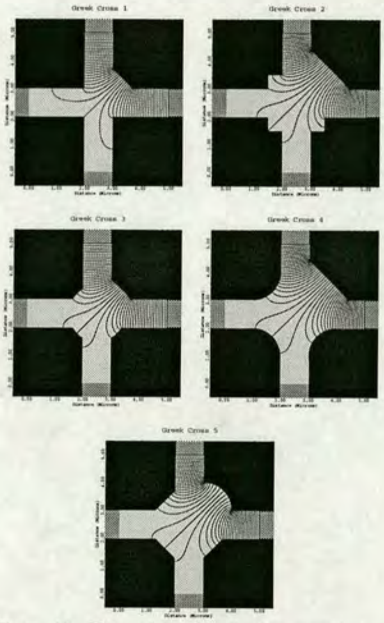

Figure 10. Plots of asymmetrical cross resistor structures used to obtain the simulation results in Table 1.

Cresswell [6] has suggested that using eight measurements for extremely asymmetrical structures improved the accuracy of measured sheet resistance. This work has confirmed once again that large asymmetries, such as those shown in figure 10 that may result from small geometry structures, can be accounted for by using a correction factor. The advantage of taking eight measurements is simply that their average provides a more repeatable result.

Figure B.10: *Reprint of paper presented at ICMTS 1999, page 4.*

Simulation	$R(0^o)$ (Ω)	$R(90^o)$ (Ω)	F_A (%)	R_{avg} (Ω)	R_s ($\Omega/\square$)
No OPC	0.22051	0.22083	-0.14588	0.22067	1.00016
Min OPC	0.22054	0.22110	-0.25225	0.22082	1.00083
OPC 2	0.22080	0.22053	0.12402	0.22066	1.00012
OPC 3	0.22060	0.22063	-0.01551	0.22061	0.99990
Max OPC	0.22052	0.22077	-0.11530	0.22064	1.00003
Mask	0.22086	0.22053	0.15186	0.22069	1.00027

Table 3. Greek cross sheet resistance extractions for the OPC corrected optical images and for the mask simulated in MEDICI.

F_A (%)	$1-f$ (%)	r
11.95	0.1195	1.1271
18.61	0.3006	1.2051
29.14	0.7396	1.3411
32.51	0.9223	1.3883
46.63	1.9116	1.6080
47.40	1.9762	1.6212
64.29	3.6858	1.9475
71.81	4.6322	2.1203
77.14	5.3766	2.2555

Table 2. Relationship between geometrical asymmetry factor and the correction factor

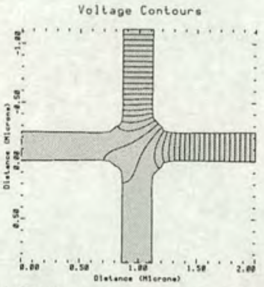

Figure 11 Greek cross structure generated using the OPC boundaries generated by DEPICT. It shows equipotentials for the 0° orientation simulation.

MEDICI simulations of Greek cross resistors were also performed using OPC boundaries previously generated by DEPICT for linewidth structures. Figure 11 gives an example of a plot from MEDICI showing the simulation area used for these resistance extractions.

Table 3 shows the simulation results for Greek cross resistance extractions performed on the five geometries shown in figure 2 and a grid generated directly from the mask file. Because the asymmetries in these devices were very small no values for the correction factor f ($f \approx 1$ in all cases) or for a corrected sheet resistance are given.

4. Conclusions

This paper has examined the effect of OPC on test structures designed to measure the electrical linewidth of tracks. It has been shown that OPC can reduce the effect of voltage tap linewidth shortening for a $0.25\mu m$ track by between 0.1 and $0.15\mu m$ when using 248nm wavelength exposures. More importantly it has been shown that masks created by OPC software do not cause significant necking at the tap location and so can be safely applied for test structures.

In addition the extraction of sheet resistance from asymmetrical Greek crosses has been investigated and the correction factors for asymmetry values up to and above 70% presented. It has been shown that these correction factors can be used with confidence with very large asymmetry values. While in theory only four measurements are required to extract the sheet resistance it is proposed that for best accuracy all eight measurement combinations should be made and correction factor applied.

Finally results for Greek cross structures exposed using OPC have been presented which, as expected, showed that OPC has no effect upon the value of sheet resistance extracted.

Acknowledgement

Staff at the University of Edinburgh would like to acknowledge the financial support of EPSRC (GR/L81000).

Figure B.11: *Reprint of paper presented at ICMTS 1999, page 5.*

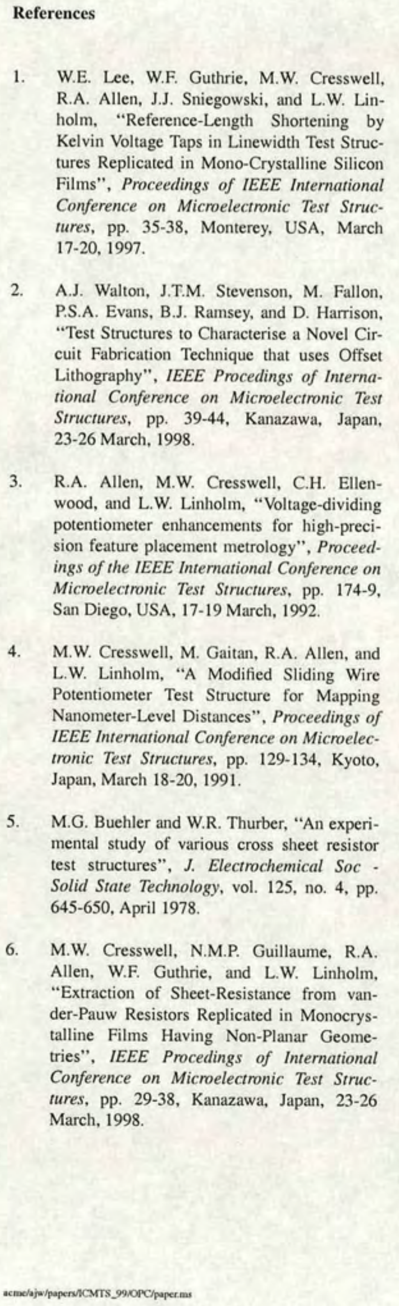

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Figure B.12: *Reprint of paper presented at ICMTS 1999, page 6.*

Characterisation of Aluminium Passivation for TMAH Based Anisotropic Etching for MEMS Applications

Knut Lian†, Stewart Smith, N. Rankin, A.J. Walton, Alan Gundlach, Tom Stevenson

Department of Electronics and Electrical Engineering
Kings Buildings, The University of Edinburgh
Edinburgh, EH9 3JL, UK

†SensoNor asa, PO Box 196
N-3192 Horten, Norway

Abstract

A cross-bridge linewidth test structure has been used to analyse, both electrically and physically, the effect of a new anisotropic silicon etch composition that has been designed to have an increased selectivity with aluminium. To characterise the effect of the etch on aluminium tracks, electrical measurements have been made to obtain sheet resistance and linewidth. These results are presented in combination with SEM micrographs to evaluate the surface quality of the exposed aluminium.

Introduction

The anisotropic etching of silicon using alkaline solutions such as tetramethyl ammonium hydroxide (TMAH), is a key technology in the production of microelectromechanical systems (MEMS). It has been shown [1] that the addition of $64gSiO_2/l$ sodium silicate solution (water glass) and 5g/l ammonium persulfate to 5wt% TMAH solution results in good anisotropic wet etching of silicon and good selectivity towards aluminium. To fully characterise this composition of etch solution the electrical and physical characteristics were measured and analysed. Electrical characterisation was performed using a standard cross-bridge line test structure [2] and the physical analysis was performed using a SEM.

Test Structure Layout

The layout of the test structures[3] is shown in fig. 1, where the aluminium tracks were designed to be 3, 4, 7, and $8\mu m$ wide. The line lengths were $800\mu m$ for the narrower tracks and $1200\mu m$ for the wider tracks. The pad configuration was designed to enable measurement using a standard 2×n probe card. The cross bridge test structure was selected because it is able to measure both the sheet resistance and linewidth, and can hence help determine if the TMAH etch is thinning and/or narrowing the aluminium track.

Test Structure Adaption Options

Fig. 2 shows a schematic of three test structures which can be used to measure different elements of the etch process. These are obviously manufactured using different techniques, but use a common mask layout. Type A is fabricated by reactively ion etching the exposed aluminium. This exposes three sides on the aluminium track to the wet etch which has an effect on both the width and thickness.

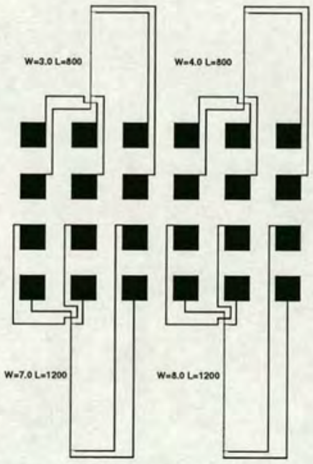


Fig. 1. Test structure layout.

Type B may be fabricated using a CMP (Chemical Mechanical Polishing) damascene process [3] where trenches are etched in the oxide followed by the deposition of aluminium to fill the trenches. Excess metal is then removed using CMP leaving the metal filled trenches. In this case only the top surface of the track is

Figure B.13: *Reprint of paper presented at ICMTS 2000, page 1.*

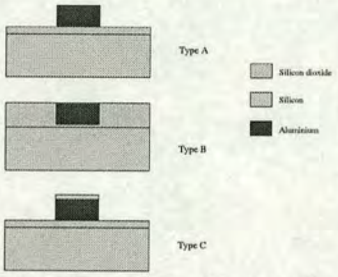


Fig. 2. Three different aluminium configurations to determine the etchants effect on the electrical properties of aluminium.

exposed to the etchant. Type C is another option, similar to type A, with a protective layer on top of the aluminium which allows the effect of the sidewall etch rate to be evaluated.

Experimental

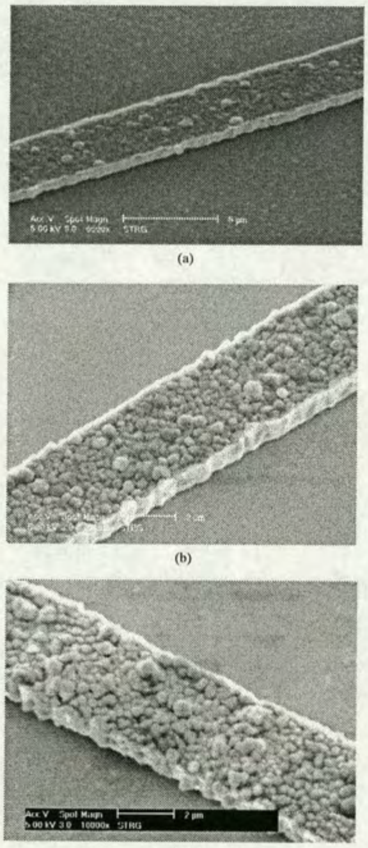
Test structures, of type A, were used to analyse the effect of the TMAH etch. The test structures were fabricated on 3-inch (1,0,0) silicon wafers by thermally growing $1\mu m$ of wet oxide followed by sputtering $1\mu m$ of either aluminium or Al1%Si. The structures shown in fig. 1 were lithographically defined using 5× wafer stepper technology, and the exposed aluminium reactively ion etched. It should be noted that samples reported were not annealed

The pure aluminium sample was initially etched in the TMAH based solution for one hour, and then at intervals of 30 minutes for a total etch time of 3.5 hours. The etch was carried out in a $1l$ beaker with $0.8l$ etch mixture. A reflux condenser was used to keep the concentration stable, and the temperature was kept at $80 \pm 2^{o}C$ using a temperature controlled hot plate. A $250 rev/min$ magnetic stirrer was used to keep the solution homogeneous both with respect to concentration and temperature. After each etch the wafer was rinsed and dried before both the electrical and physical effects on aluminium lines (3, 4, and $7\mu m$ wide) were evaluated.

Due to the effects observed on the pure aluminium, it was decided to monitor the Al1%Si samples at 15 minute intervals during the first hour, and then at 30 minute intervals for a total etch time of 3.5 hours. In addition, it was also decided to perform measurements on all four available linewidths.

Results

SEM images indicate that the pure aluminium tracks were severely attacked, as shown in fig. 3. It can be observed that the roughness of the surface increases with etch time, and the grains can be easily identified.



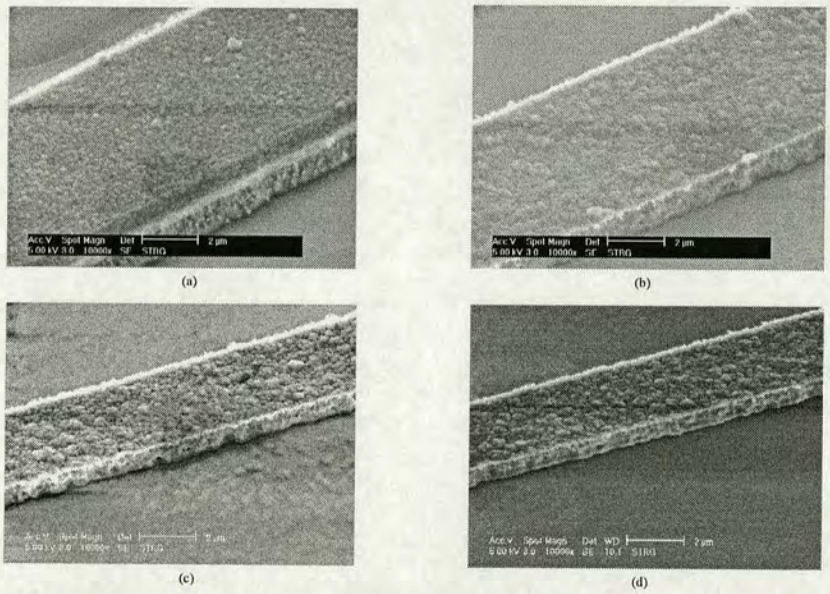
(a)

(b)

(c)

Fig. 3. SEM micrograph of pure aluminium track: (a) prior to TMAH etch, (b) after 1 hour TMAH etch, and (c) after 3.5 hours of TMAH etch.

Figure B.14: *Reprint of paper presented at ICMTS 2000, page 2.*



(a) (b)

(c) (d)

Fig. 4. SEM micrograph of Al1%Si track: (a) prior to TMAH etch, (b) after 15 minutes TMAH etch, (c) after 30 minutes of TMAH etch, and (d) after 3.5 hours of TMAH etch.

A range of images of Al1%Si tracks are shown in fig. 4. Visually it can be seen that surface roughness of these tracks increases for the first 30 minutes, and then stabilises. No noticeable change can be detected from 30 minutes to 3.5 hours. It appears that the aluminium grains become more detailed during the first period of the etching, and then the surface has a more or less constant texture for the remaining etch period.

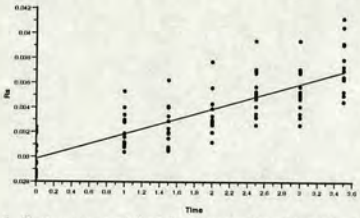


Fig. 5. Sheet resistance of aluminium lines varying with etch time.

Electrical measurements of the track sheet resistance can be used to show if indeed the effective thickness of the track was being thinned with increasing etch time. The graph in fig. 5 shows that the sheet resistance for aluminium lines increase linearly with etch time. Fig. 6 shows that the sheet resistance of Al1%Si lines initially increase for about one hour, and then remains approximately constant during the remaining 2.5 hours of etching. The linewidth showed no noticeable change with increasing etch time, as shown in fig. 7 and 8.

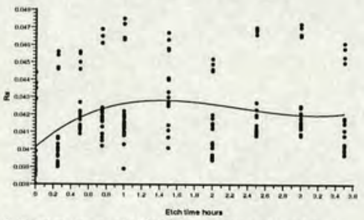


Fig. 6. Sheet resistance of Al1%Si lines varying with etch time.

Figure B.15: *Reprint of paper presented at ICMTS 2000, page 3.*

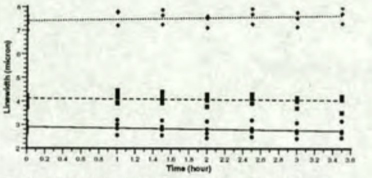


Fig. 7. Linewidth of aluminium lines varying with etch time.

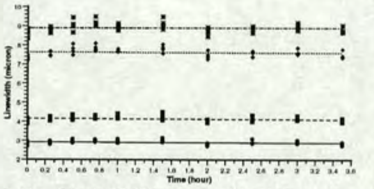


Fig. 8. Linewidth of Al1%Si lines varying with etch time.

Discussion

An increase in sheet resistance is equivalent to a decrease in the effective thickness of the aluminium track. The electrical measurements therefore indicate that the aluminium lines are monotonically becoming thinner throughout the etch time. However, the Al1%Si lines show an initial decrease in line thickness, and then a more stable phase after the first hour.

A similar effect is indicated in the SEM micrographs of the surface roughness. The aluminium lines clearly show an increase in roughness throughout the etch time, while the Al1%Si lines keep their texture fairly constant after the initial roughening during the first 30 minutes.

It is believed the reason why both the sheet resistance increases and the grains become more visible, is that the etch predominantly attacks the metal at the grain boundaries, as shown schematically in fig. 9.

Fig. 9. Etching of an aluminium line along grain boundaries.

There may be a number of reasons why the lines are not attacked from the sides. Firstly, the lines are from 3 to 8 times wider than they are thick, making the surface area available for attack smaller. In addition, the sidewalls do not have the same grain structure as the top surface. As the SEM micrographs shows, the sidewalls are much smoother than the top surface, which may make it more difficult for the etch to attack the metal.

Conclusions and Further Work

Interesting results have be obtained by using electrical test structures in conjunction with SEM analysis. The measurements clearly show that the proposed etch composition is potentially suitable for applications where Al1%Si is used as the metal conductor. Rather surprisingly, the silicon etch attacked Al1%Si alloy less than pure aluminium. Further work will include electromigration tests on both pure aluminium and Al1%Si that has been exposed to TMAH, to determine their reliability characteristics after etch. It is also proposed that the effect of annealing the aluminium be examined.

Acknowledgements

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Figure B.16: *Reprint of paper presented at ICMTS 2000, page 4.*

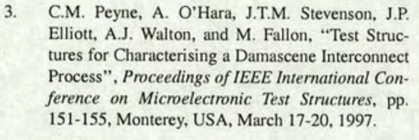

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Figure B.17: *Reprint of paper presented at ICMTS 2000, page 5.*

COMPUTER GENERATED HOLOGRAMS FOR USE AS MICROELECTRONIC TEST STRUCTURES

S. Smith* J.T.M. Stevenson* A.J. Walton* A.M. Gundlach* P. Christie† and S.A. AbuGhazaleh†

* Department of Electronics and Electrical Engineering, Kings Buildings,

† Department of Electrical and Computer Engineering, University of Delaware, Newark, DE 19716, U.S.A.

Abstract - The binary detour phase Wire Segment Hologram (WSH) is described and the previous work on its use as a test structure in a microelectronic fabrication process is reviewed. The extension of the use of the null WSH for measurement of misalignment in a two level metallisation process is examined and simulation results are presented. A new hologram image which allows measurement of feature size is also described and preliminary simulation results are presented.

1. Introduction

An optical hologram is normally produced by recording the interference pattern caused by an object wave and a reference wave [1]. The result is a diffraction grating from which the object wave can be reconstructed. This is done by imaging the hologram using a coherent light source similar to the reference wave used in recording. A typical setup for reconstructing the image from a reflection hologram is shown in figure 1.

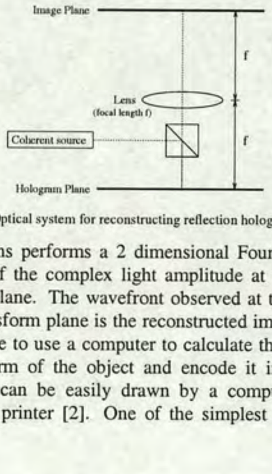

Fig. 1. Optical system for reconstructing reflection holograms.

The lens performs a 2 dimensional Fourier transform of the complex light amplitude at the hologram plane. The wavefront observed at the image or transform plane is the reconstructed image. It is possible to use a computer to calculate the Fourier transform of the object and encode it in a form which can be easily drawn by a computer controlled printer [2]. One of the simplest forms of Computer Generated Hologram (CGH) is the binary detour phase hologram [3-5]. To generate the hologram a 2-Dimensional Inverse Discrete Fourier Transform (2DIDFT) of the desired image is performed. This produces a matrix of complex values representing the hologram. The transform matrix is separated into amplitude and phase component matrices and encoded as a detour phase hologram. The encoding scheme is described in figure 2. This type of CGH was chosen as it can be easily fabricated as an array of metal lines to make a Wire Segment Hologram (WSH).

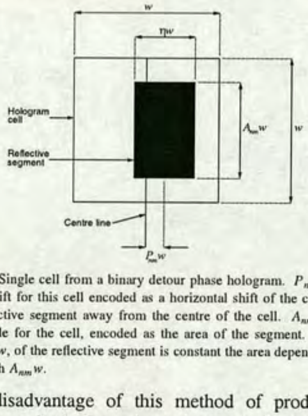

Fig. 2. Single cell from a binary detour phase hologram. P_{nm} is the phase shift for this cell encoded as a horizontal shift of the centre of the reflective segment away from the centre of the cell. A_{nm} is the magnitude for the cell, encoded as the area of the segment. As the width, ηw, of the reflective segment is constant the area depends upon the length $A_{nm}w$.

One disadvantage of this method of producing holograms is the large dynamic range of amplitude values in the transform matrix. This may lead to values of segment length $A_{nm}w$ lower than the minimum reproducible feature size. One way to avoid this is to use an technique such as that described by Fienup [6]. This method iteratively transfers amplitude information to the hologram phase matrix leading to a much smaller range of amplitude values and improving the WSH structures.

Figure B.18: *Reprint of paper presented at PREP 2000, page 1.*

2. Holograms as In-Line Test Structures.

The WSH has been developed in an attempt to provide a real-time in-line test structure for microfabrication processes. In practice each wafer being processed would have the hologram included in a metallisation layer. Each hologram would be illuminated by a laser on the production line and the reconstructed image captured. The quality of this image would show how well the hologram has been reproduced in the fabrication process so that errors in production can be detected. The first studies used simple hologram images and examined the effects of different exposures in the photolithography stage used to define the wire segments [7, 8]. The results of these studies indicated that the holographic test structure could discriminate differences in the dimensions of the wire segments as small as 1% of the designed feature size.

The next improvement in the WSH was the use of a null image hologram where light is diffracted away from some area of the image plane. The image used to design this hologram is shown in figure 3.

Fig. 3. Null hologram image produced from a raised cosine function.

The null image was used to generate holographic structures in order to investigate the effects of misregistration or alignment error [9]. Each of the hologram elements or cells was randomly selected to be in one of two groups as shown in figure 4. The two sets of hologram elements were printed separately and an alignment error could be introduced between them.

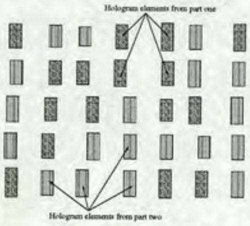

Fig. 4. Plan view of part of a hologram designed to allow measurement of alignment error

The effects of misalignment were investigated by analysing the reconstructed images obtained from holograms with different offsets between the two halves of the hologram. As the misalignment increases the degradation of the image leads to an increase in the intensity of light in the the null area. The Average Intensity Ratio (AIR) was introduced as a measurement of the image quality. To calculate the AIR the average intensity in the null area is divided by the average intensity in the rest of the image. The value of AIR rises as the misalignment increases. It was found that misalignments of 0.1 μm could be detected using holograms with a segment width of 2 μm. A Progressional Offset Technique (POT) was used as this does not require the measurements to be calibrated and will allow quantitative results to be obtained [10, 11]. In the progressional offset technique a set of holograms with a range of built in offsets is fabricated. Values of AIR are calculated from the reconstructed images and plotted against the built in misalignments as is illustrated in figure 5. By interpolating between the data points the actual misalignment introduced in the process can be determined.

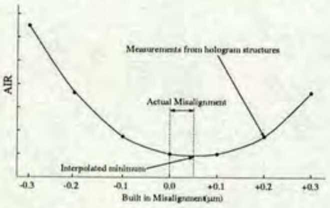

Fig. 5. Graph of AIR against built-in misalignment which shows how a POT can be used to extract the actual alignment error

The previous study used holograms fabricated in a single layer of metallisation but this cannot represent misalignments in a real process [9]. The next step is to investigate the performance of WSH structures where the two sets of wire segments are patterned on different levels of metal.

3. Two Level Metal Holograms

The production of a two level hologram is more complex than fabricating the single layer structures previously reported. The phase values of the hologram are encoded as a shift in the horizontal position of the wire segment. This means that a misalignment between the two sections of the hologram can be considered to be a phase shift added to one set of hologram elements. In a two level WSH there is a difference in height between the reflecting surfaces of the two levels of metal. This will introduce a further phase shift due to the optical path length difference. As both misalignment and layer thickness cause a phase shift their effects will be confounded thus making the actual misalignment difficult to extract.

Figure B.19: *Reprint of paper presented at PREP 2000, page 2.*

A cross section through part of a two level hologram is shown in figure 6.

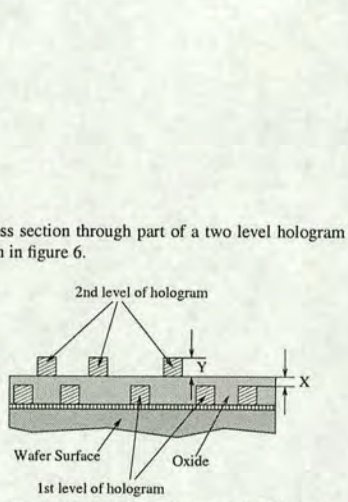

Fig. 6. Cross section through part of a two level WSH showing the important layer thicknesses for the hologram operation. X is the depth of oxide over first level metal and Y is the thickness of the second level metal.

The process required to fabricate such a structure begins in the same way as for a single level hologram with a layer of sputtered aluminium. This is patterned and etched with the first half of the WSH. The front of the wafer is then coated with a thick layer of deposited silicon dioxide which is polished flat. Finally, a second metallisation layer is added and the rest of the hologram is patterned into it.

The most important features to note from figure 6 are the layer thicknesses marked X and Y as these determine the phase difference between the two levels of the hologram. If the path length difference between the levels is equal to λ (or an integer multiple of λ) then the phase shift will be 2π (or 4π for 2λ etc.) which is equivalent to zero phase shift.

Simulations which show the effects of phase shifts due to layer thickness and misalignment have been performed using the GNU Octave software.* The process for simulating the reconstruction of a hologram is as follows:

1. Take 2DIDFT of the null image and perform Fienup iterations to get the hologram matrix. This is separated into amplitude and phase matrices.
2. Select half of the elements in the phase matrix at random and add phase shift. This is equivalent to a phase shift between the two levels of hologram elements in a real structure.
3. Recombine the amplitude matrix and the altered phase matrix to get a new hologram.
4. Take the 2DDFT of the hologram matrix to get the new image matrix. This can then be analysed to give an AIR value.

A set of hologram simulations have been performed with a range of phase shifts equivalent to different values of misalignment and layer thickness. The range of misalignments used runs from -0.5 μm to +0.5 μm. For the purposes of the simulation it is only the silicon dioxide thickness X which has been changed. The range of oxide thickness errors is from −1000Å to +1000Å, centred on a value of layer thickness which would give no phase shift. Figure 7 shows the array of hologram images produced by this simulation.

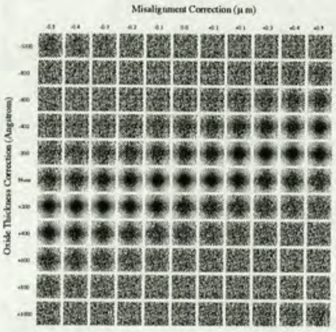

Fig. 7. Simulated null hologram images for a two level WSH. Each has a different phase shift due to misalignment or layer thickness.

This array is the equivalent of a 2 dimensional POT layout with correction for both alignment errors and layer thickness. It shows that good hologram reproduction does not just occur for the simulation with no offset or layer thickness error. Table 1 gives values of AIR for each of the simulated holograms.

Minimum values of AIR occur at two sets of phase shift values besides zero. Firstly for a thickness error of +200Å and a misalignment of $-0.3\mu m$. Then for a layer thickness error of −200Å and a misalignment of $+0.3\mu m$. This would make extraction of the misalignment in a real structure impossible without making other measurements.

4. Wire segment holograms for critical dimension measurement

The first two studies which used WSH structures examined the effects of exposure during the metal photolithography step of the fabrication [7, 8]. These showed that changing exposure times altered the size of the wire segments and therefore the intensity of the reconstructed image. It was also found that the exposure level could also affect the phase values in the hologram by causing some elements to merge or disappear. This would degrade the quality of the image and could cause unexpected results. For example the total image intensity may rise due to increased noise in the image even as the hologram element size decreases.

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* Octave is a Matlab compatible language which can be used to perform the matrix calculations needed to design WSH structures [12].

Figure B.20: *Reprint of paper presented at PREP 2000, page 3.*

Oxide Thickness	Alignment Error (μm)										
Error (Å)	-0.5	-0.4	-0.3	-0.2	-0.1	0.0	+0.1	+0.2	+0.3	+0.4	+0.5
-1000	0.8408	0.9115	0.9718	1.0204	1.0570	1.0814	1.0929	1.0918	1.0779	1.0514	1.0130
-800	1.0332	1.0661	1.0864	1.0939	1.0888	1.0709	1.0406	0.9986	0.9462	0.8842	0.8139
-600	1.0936	1.0846	1.0627	1.0285	0.9832	0.9277	0.8629	0.7903	0.7118	0.6294	0.5457
-400	1.0154	0.9668	0.9082	0.8408	0.7661	0.6861	0.6031	0.5197	0.4405	0.3688	0.3087
-200	0.8180	0.7414	0.6601	0.5767	0.4941	0.4170	0.3484	0.2930	0.2598	0.2680	0.3110
Zero	0.5503	0.4691	0.3943	0.3293	0.2793	0.2568	0.2788	0.3292	0.3973	0.4755	0.5587
+200	0.3116	0.2684	0.2595	0.2923	0.3493	0.4212	0.5013	0.5854	0.6704	0.7533	0.8324
+400	0.3080	0.3707	0.4458	0.5274	0.6123	0.6968	0.7788	0.8560	0.9247	0.9828	1.0288
+600	0.5540	0.6390	0.7229	0.8038	0.8787	0.9442	0.9986	1.0409	1.0713	1.0890	1.0938
+800	0.8282	0.9005	0.9626	1.0132	1.0517	1.0783	1.0919	1.0928	1.0811	1.0566	1.0202
+1000	1.0266	1.0614	1.0839	1.0936	1.0905	1.0748	1.0464	1.0063	0.9556	0.8951	0.8260

Table 1. Values of AIR for different alignment and layer thickness errors.

Simulations of size error effects have been performed using Octave. The first set of simulations used the null hologram. The hologram matrix was created and split into amplitude and phase matrices. In order to simulate the effect of a change in exposure time an offset was added to each element in the amplitude matrix.

The size of the offset depended on the value of the amplitude element and was equivalent to an increase or decrease in both the length and width of the wire segment. A graph of the results can be seen in figure 8.

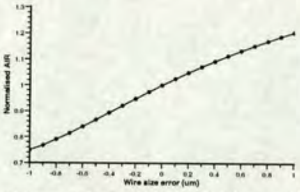

Fig. 8. AIR versus wire size error for a null hologram with a wire segment width of 2 μm. AIR values are normalised to the result of the simulation with no size error.

These results show that it would be difficult to get a quantitative measurement of the actual value of linewidth from one of these structures without calibrating the results against some other measurement. The objective is to be able to use a progressional offset technique where each hologram structure is compensated for a particular wire segment size error.

A second set of simulations was performed with a new hologram matrix created using an image which is the opposite of the null hologram. The new image is shown in figure 9 and the results are plotted in figure 10. The AIR increases with wire segment size for the null hologram and decreases with size error for the null hologram. It may be possible to use both types of holograms in a POT test layout and combine the measurements to determine the actual wire dimension. However this may also require refinement or calibration of the measurement techniques as the relative change in AIR was greater for the null hologram than for the simulated anti-null structures.

Fig. 9. Anti-null hologram image produced from a raised and shifted cosine function.

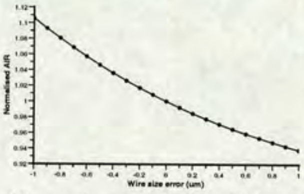

Fig. 10. AIR versus wire size error for anti-null hologram structure with 2 μm segment width.

In an attempt to find a solution to this problem a new hologram was created by adding the null and anti-null hologram matrices together. When the Fourier transform of this was taken the image shown in figure 11 was recovered. This hologram was used in a new set of simulations, the results of which can be seen in figure 12. Even more interesting results were found when a threshold was applied to the reconstructed images before the AIR was extracted. The thresholding involves first normalising each pixel to the maximum level in the image.

Figure B.21: *Reprint of paper presented at PREP 2000, page 4.*

Then each pixel with a value greater than the threshold is set to one while each that has a value less than the threshold is set to zero. Figure 13 gives the results using a threshold level of 0.5.

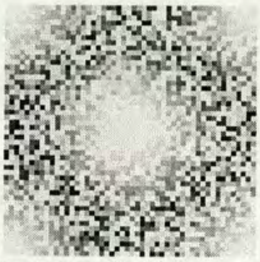

Fig. 11. Hologram image created by adding the null and anti-null hologram matrices

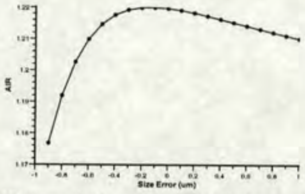

Fig. 12. AIR versus wire size error for combined hologram structure

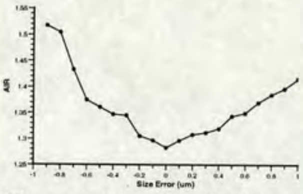

Fig. 13. AIR versus wire size error for combined hologram structure with a threshold of 0.5

The thresholding increases the sensitivity of the AIR measurement as well as reversing the trend of the graph. Further simulations for the region -0.2 μm to +0.2 μm have shown the percentage change in AIR with a threshold of 0.5 to be around 1% per 0.1 μm of wire size error.

5. Conclusions and Further Work

The previous work using WSH structures for process control testing has been reviewed. The method for using hologram test structures to allow in-line non-contact testing of metal interconnect patterning has been described. It now seems clear that although the null WSH can be used to measure misregistration quite accurately using a progressional offset technique it may not be possible to use it for this in a real process where the two parts of the hologram are defined in different metallisation levels. This is because the effects of alignment error and path length difference between the layers combine to determine the phase error added into the hologram. Simulations indicate that using a POT technique leads to ambiguous results with many possible values for the actual misalignment and layer thickness. Work is continuing on fabrication of a number of two level hologram structures. The test die will include other structures to allow measurement of the misalignment and layer thickness. This means the results from the optical measurements of the hologram can be correlated with more direct tests.

Results of simulations which looked at the effects of dimensional errors in the wire segments have been presented. The results have shown that the null and anti-null holograms can be used to measure critical dimension but the measurements will need to be calibrated for each process. A new hologram image made by combining the null and anti-null holograms in the transform plane has been described. Simulations using this hologram have indicated that it could be used to design a POT to measure wire segment dimension. WSH structures will be fabricated to allow confirmation of the simulation results for the combined image as well as for the null and anti-null holograms.

Acknowledgement

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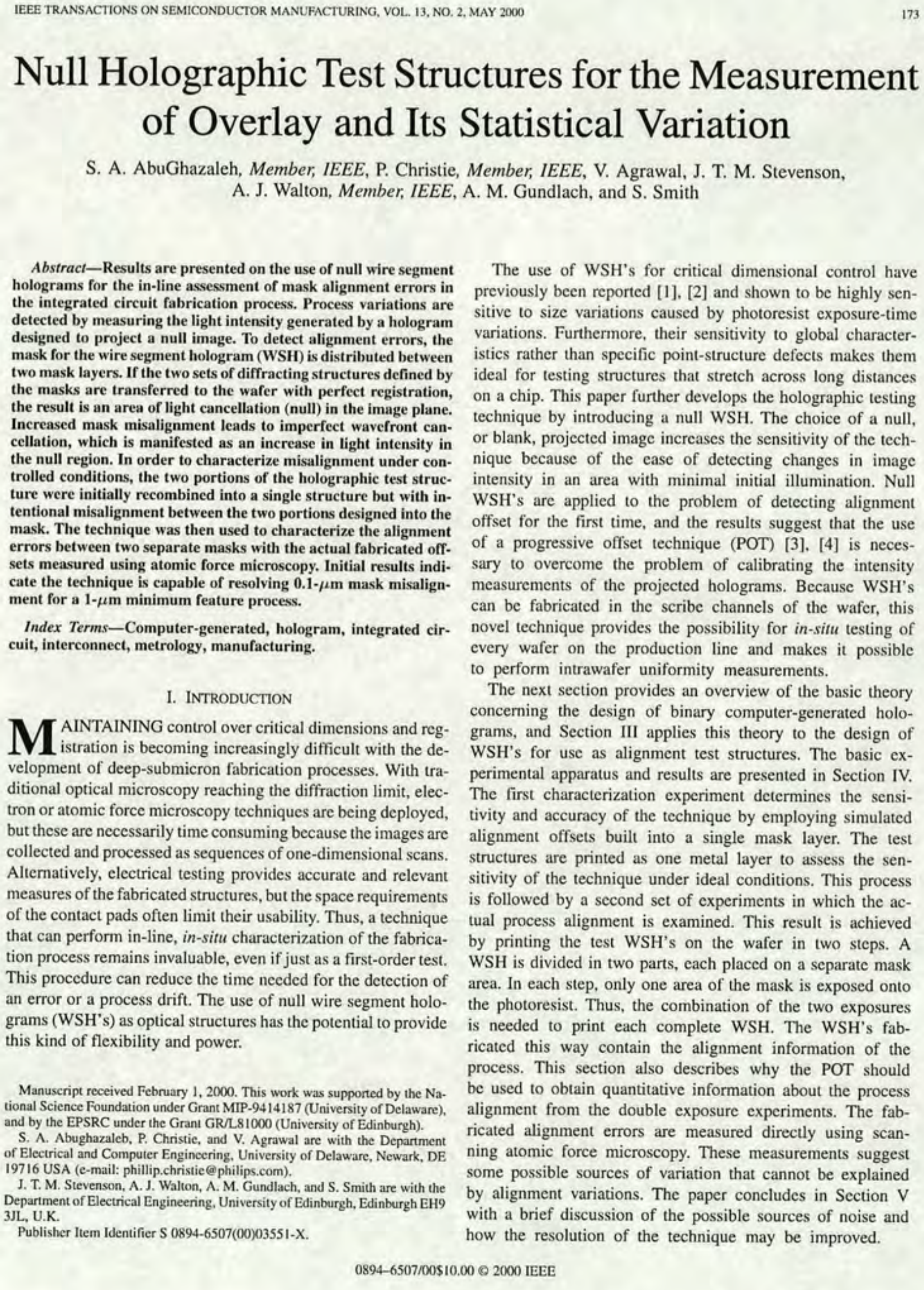
Figure B.23: *Reprint of paper presented at PREP 2000, page 6.*



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Null Holographic Test Structures for the Measurement of Overlay and Its Statistical Variation

S. A. AbuGhazaleh, *Member, IEEE*, P. Christie, *Member, IEEE*, V. Agrawal, J. T. M. Stevenson,
A. J. Walton, *Member, IEEE*, A. M. Gundlach, and S. Smith

***Abstract*—Results are presented on the use of null wire segment holograms for the in-line assessment of mask alignment errors in the integrated circuit fabrication process. Process variations are detected by measuring the light intensity generated by a hologram designed to project a null image. To detect alignment errors, the mask for the wire segment hologram (WSH) is distributed between two mask layers. If the two sets of diffracting structures defined by the masks are transferred to the wafer with perfect registration, the result is an area of light cancellation (null) in the image plane. Increased mask misalignment leads to imperfect wavefront cancellation, which is manifested as an increase in light intensity in the null region. In order to characterize misalignment under controlled conditions, the two portions of the holographic test structure were initially recombined into a single structure but with intentional misalignment between the two portions designed into the mask. The technique was then used to characterize the alignment errors between two separate masks with the actual fabricated offsets measured using atomic force microscopy. Initial results indicate the technique is capable of resolving 0.1-μm mask misalignment for a 1-μm minimum feature process.**

***Index Terms*—Computer-generated, hologram, integrated circuit, interconnect, metrology, manufacturing.**

I. INTRODUCTION

MAINTAINING control over critical dimensions and registration is becoming increasingly difficult with the development of deep-submicron fabrication processes. With traditional optical microscopy reaching the diffraction limit, electron or atomic force microscopy techniques are being deployed, but these are necessarily time consuming because the images are collected and processed as sequences of one-dimensional scans. Alternatively, electrical testing provides accurate and relevant measures of the fabricated structures, but the space requirements of the contact pads often limit their usability. Thus, a technique that can perform in-line, *in-situ* characterization of the fabrication process remains invaluable, even if just as a first-order test. This procedure can reduce the time needed for the detection of an error or a process drift. The use of null wire segment holograms (WSH's) as optical structures has the potential to provide this kind of flexibility and power.

The use of WSH's for critical dimensional control have previously been reported [1], [2] and shown to be highly sensitive to size variations caused by photoresist exposure-time variations. Furthermore, their sensitivity to global characteristics rather than specific point-structure defects makes them ideal for testing structures that stretch across long distances on a chip. This paper further develops the holographic testing technique by introducing a null WSH. The choice of a null, or blank, projected image increases the sensitivity of the technique because of the ease of detecting changes in image intensity in an area with minimal initial illumination. Null WSH's are applied to the problem of detecting alignment offset for the first time, and the results suggest that the use of a progressive offset technique (POT) [3], [4] is necessary to overcome the problem of calibrating the intensity measurements of the projected holograms. Because WSH's can be fabricated in the scribe channels of the wafer, this novel technique provides the possibility for *in-situ* testing of every wafer on the production line and makes it possible to perform intrawafer uniformity measurements.

The next section provides an overview of the basic theory concerning the design of binary computer-generated holograms, and Section III applies this theory to the design of WSH's for use as alignment test structures. The basic experimental apparatus and results are presented in Section IV. The first characterization experiment determines the sensitivity and accuracy of the technique by employing simulated alignment offsets built into a single mask layer. The test structures are printed as one metal layer to assess the sensitivity of the technique under ideal conditions. This process is followed by a second set of experiments in which the actual process alignment is examined. This result is achieved by printing the test WSH's on the wafer in two steps. A WSH is divided in two parts, each placed on a separate mask area. In each step, only one area of the mask is exposed onto the photoresist. Thus, the combination of the two exposures is needed to print each complete WSH. The WSH's fabricated this way contain the alignment information of the process. This section also describes why the POT should be used to obtain quantitative information about the process alignment from the double exposure experiments. The fabricated alignment errors are measured directly using scanning atomic force microscopy. These measurements suggest some possible sources of variation that cannot be explained by alignment variations. The paper concludes in Section V with a brief discussion of the possible sources of noise and how the resolution of the technique may be improved.

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S. A. Abughazaleb, P. Christie, and V. Agrawal are with the Department of Electrical and Computer Engineering, University of Delaware, Newark, DE 19716 USA (e-mail: phillip.christie@philips.com).

J. T. M. Stevenson, A. J. Walton, A. M. Gundlach, and S. Smith are with the Department of Electrical Engineering, University of Edinburgh, Edinburgh EH9 3JL, U.K.

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Figure B.24: *Reprint of paper published in IEEE Transactions on Semiconductor Maunfacturing, May 2000, page 1.*

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II. BASIC THEORY

A. Scalar Diffraction and the Fourier Transform

Using scalar diffraction theory, it may be shown that if the time-independent electric field within a diffracting aperture Σ is given by $E(x_a, y_a)$, the field in the observation plane is given by

$$E(x_o, y_o) = K_1 \iint_\Sigma E(x_a, y_a) e^{-j(2\pi/\lambda z)(x_a x_o + y_a y_o)}\, dx_a\, dy_a \quad (1)$$

where x_a, y_a and x_o, y_o are the coordinates in the diffraction and observation planes, respectively, z is the distance between the two planes, and K_1 is a (possibly complex) constant. The intent of this section is to generate a diffractive structure that will produce an $E(x_a, y_a)$ corresponding to a desired test image in the observation plane.

This expression is valid if certain limitations are placed on the size of the aperture and distance to the observation plane. The first requirement of scalar diffraction theory is that the aperture is much larger than the wavelength of the incident illumination. This assumption ensures that the field can be considered as a scalar quantity with the transmission or reflection function being defined in a plane in the near field of the diffracting object. Scalar diffraction theory ignores the field discontinuities that result at the boundaries and edges of the structure. It is possible to ignore field coupling when the extent of each aperture Σ is much larger than the wavelength λ, because the disturbance exists only in a very small region of the entire structure and uses a small fraction of the incident illuminating radiation. As the wavelength approaches the size of the grating, the discontinuities become more significant and their effect cannot be ignored. Prather *et al.* [5] use full vector solution and finite difference time-domain (FDTD) analysis to show that as the wavelength approaches the size of the grating, more power is coupled into the disturbances, which result in higher frequency evanescent waves. This power does not propagate and ends up contributing to a higher zeroth diffraction order intensity. As long as the wavelength is still smaller than the diffracting structure dimensions, the effect of violating this assumption is a reduction in the percentage of incident radiation diffracted into the desired image.

In practice, it is possible to fabricate wire segment holograms with individual segment sizes that are significantly smaller than that required by scalar diffraction theory. This approach reduces the quality of the diffracted image, lowering the diffraction efficiency of the hologram. It also increases the noise in the image and the intensity of the zeroth-order diffraction spot. Since the technique is based on relative comparison of the intensity, however, the absolute quality of each hologram is not necessarily a limiting factor.

The second assumption is that the observation is done far from the diffracting object. This procedure requires that a diffractive structure with an extent of 500 μm needs to be at least 2.5 m away from the observation plane. This large distance is difficult to achieve in a compact optical system. Observation of the pattern at a distance closer than the Fraunhofer distance leads to spherical aberrations in the image. For the application described in this paper, spherical aberrations do not present a problem. To simplify the application and take advantage of a smaller, less expensive charge-coupled device (CCD) array, however, a lens was added to the optical system and used in the collection of the final sets of data. The effect of the lens is to planarize the diffracted wavefront, which results in the Fourier plane being located at its focal length, which is significantly closer.

Because $(x_a/\lambda z) = u$ and $(y_a/\lambda z) = v$, where u and v are spatial frequencies, (1) can be rewritten as

$$E(x_o, y_o) = K_2 \iint_\Sigma E(u, v) e^{-j2\pi(u x_o + v y_o)}\, du\, dv. \quad (2)$$

The diffraction plane is defined to be where the hologram is placed, and the observation plane is defined as the position of the resultant diffraction image. Accordingly, notation is switched from a general observation-plane intensity field $E(x_o, y_o)$ to a specific image field $i(x, y)$ and $E(u, v)$ is replaced by the hologram transmission function $I(u, v)$. In addition, because $i(x, y)$ and $I(u, v)$ are continuous functions of space, their sampled values are defined as

$$i_{mn} = i(m, n) = i(m\Delta x, n\Delta y) \simeq i(x, y) \quad (3)$$

$$I_{mn} = I(m, n) = I(m\Delta x, n\Delta y) \simeq I(u, v) \quad (4)$$

where the sampling interval Δ is chosen appropriately to avoid aliasing. In the following sections, i_{mn} and I_{mn} will be interchanged rather freely, with the continuous spatial forms depending on whether the actual image or its sampled matrix representation are intended. This procedure is done because the discretized I_{mn} hologram projects a continuous spatial image $i(x, y)$. Inversely, $I(u, v)$, a function of space, is constructed from the sampled i_{mn}. Thus, an equation of the form

$$i(x, y) = \iint_\Sigma I_{mn} e^{-j2\pi(xm,\, yn)} dm\, dn \quad (5)$$

implies that the continuous image $i(x, y)$ is obtained from the hologram as represented by its sampled form I_{mn}. Although this may seem arbitrary, it simply means that the intermediate step of specifying the sampled version $i(m\Delta x, n\Delta y)$ is omitted.

With the new notation, (1) means that the desired image $i(x, y)$ is the Fourier transform of the hologram $I(u, v)$

$$i(x, y) = \iint_{-\infty}^{\infty} I(u, v) e^{-j2\pi(ux + vy)} du\, dv. \quad (6)$$

Inversely, the hologram $I(u, v)$ is obtained through the inverse Fourier transform of $i(x, y)$

$$I(u, v) = \iint_{-\infty}^{\infty} i(x, y) e^{j2\pi(ux + vy)} dx\, dy. \quad (7)$$

III. WIRE SEGMENT HOLOGRAM DESIGN

A. Wire Segment Layout

Most metallization processes restrict the geometry of the segment to right-angled shapes. As a result, the wire segments composing the hologram need to be rectangular in shape. The design

Figure B.25: *Reprint of paper published in IEEE Transactions on Semiconductor Maunfacturing, May 2000, page 2*

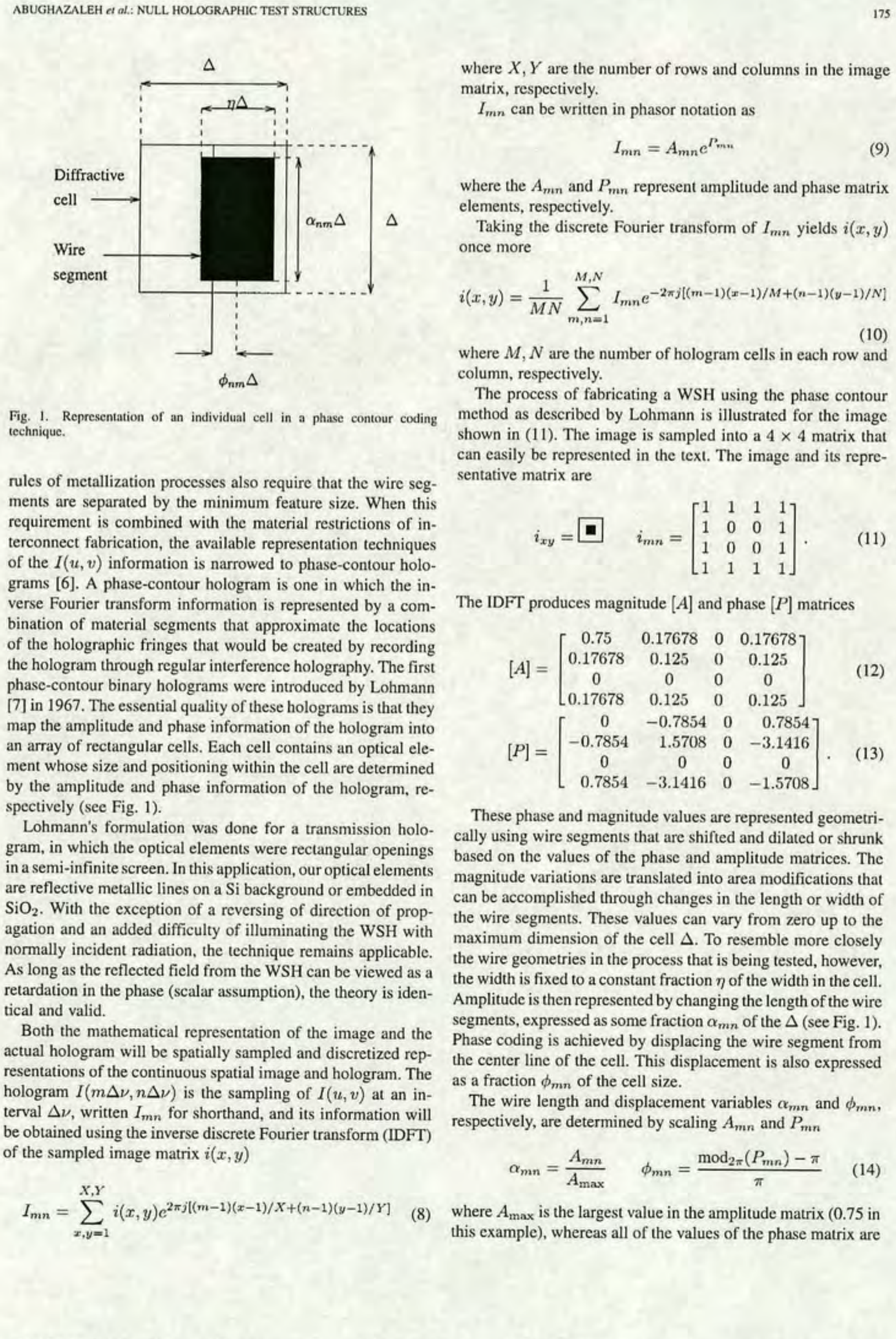

Fig. 1. Representation of an individual cell in a phase contour coding technique.

rules of metallization processes also require that the wire segments are separated by the minimum feature size. When this requirement is combined with the material restrictions of interconnect fabrication, the available representation techniques of the $I(u, v)$ information is narrowed to phase-contour holograms [6]. A phase-contour hologram is one in which the inverse Fourier transform information is represented by a combination of material segments that approximate the locations of the holographic fringes that would be created by recording the hologram through regular interference holography. The first phase-contour binary holograms were introduced by Lohmann [7] in 1967. The essential quality of these holograms is that they map the amplitude and phase information of the hologram into an array of rectangular cells. Each cell contains an optical element whose size and positioning within the cell are determined by the amplitude and phase information of the hologram, respectively (see Fig. 1).

Lohmann's formulation was done for a transmission hologram, in which the optical elements were rectangular openings in a semi-infinite screen. In this application, our optical elements are reflective metallic lines on a Si background or embedded in SiO_2. With the exception of a reversing of direction of propagation and an added difficulty of illuminating the WSH with normally incident radiation, the technique remains applicable. As long as the reflected field from the WSH can be viewed as a retardation in the phase (scalar assumption), the theory is identical and valid.

Both the mathematical representation of the image and the actual hologram will be spatially sampled and discretized representations of the continuous spatial image and hologram. The hologram $I(m\Delta\nu, n\Delta\nu)$ is the sampling of $I(u, v)$ at an interval $\Delta\nu$, written I_{mn} for shorthand, and its information will be obtained using the inverse discrete Fourier transform (IDFT) of the sampled image matrix $i(x, y)$

$$I_{mn} = \sum_{x,y=1}^{X,Y} i(x, y)e^{2\pi j[(m-1)(x-1)/X+(n-1)(y-1)/Y]} \quad (8)$$

where X, Y are the number of rows and columns in the image matrix, respectively.

I_{mn} can be written in phasor notation as

$$I_{mn} = A_{mn}e^{P_{mn}} \quad (9)$$

where the A_{mn} and P_{mn} represent amplitude and phase matrix elements, respectively.

Taking the discrete Fourier transform of I_{mn} yields $i(x, y)$ once more

$$i(x, y) = \frac{1}{MN} \sum_{m,n=1}^{M,N} I_{mn}e^{-2\pi j[(m-1)(x-1)/M+(n-1)(y-1)/N]} \quad (10)$$

where M, N are the number of hologram cells in each row and column, respectively.

The process of fabricating a WSH using the phase contour method as described by Lohmann is illustrated for the image shown in (11). The image is sampled into a 4 × 4 matrix that can easily be represented in the text. The image and its representative matrix are

$$i_{xy} = \boxed{\blacksquare} \qquad i_{mn} = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 1 \end{bmatrix}. \quad (11)$$

The IDFT produces magnitude $[A]$ and phase $[P]$ matrices

$$[A] = \begin{bmatrix} 0.75 & 0.17678 & 0 & 0.17678 \\ 0.17678 & 0.125 & 0 & 0.125 \\ 0 & 0 & 0 & 0 \\ 0.17678 & 0.125 & 0 & 0.125 \end{bmatrix} \quad (12)$$

$$[P] = \begin{bmatrix} 0 & -0.7854 & 0 & 0.7854 \\ -0.7854 & 1.5708 & 0 & -3.1416 \\ 0 & 0 & 0 & 0 \\ 0.7854 & -3.1416 & 0 & -1.5708 \end{bmatrix}. \quad (13)$$

These phase and magnitude values are represented geometrically using wire segments that are shifted and dilated or shrunk based on the values of the phase and amplitude matrices. The magnitude variations are translated into area modifications that can be accomplished through changes in the length or width of the wire segments. These values can vary from zero up to the maximum dimension of the cell Δ. To resemble more closely the wire geometries in the process that is being tested, however, the width is fixed to a constant fraction η of the width in the cell. Amplitude is then represented by changing the length of the wire segments, expressed as some fraction α_{mn} of the Δ (see Fig. 1). Phase coding is achieved by displacing the wire segment from the center line of the cell. This displacement is also expressed as a fraction ϕ_{mn} of the cell size.

The wire length and displacement variables α_{mn} and ϕ_{mn}, respectively, are determined by scaling A_{mn} and P_{mn}

$$\alpha_{mn} = \frac{A_{mn}}{A_{\max}} \qquad \phi_{mn} = \frac{\mathrm{mod}_{2\pi}(P_{mn}) - \pi}{\pi} \quad (14)$$

where $A_{\max}$ is the largest value in the amplitude matrix (0.75 in this example), whereas all of the values of the phase matrix are

Figure B.26: *Reprint of paper published in IEEE Transactions on Semiconductor Maunfacturing, May 2000, page 3*

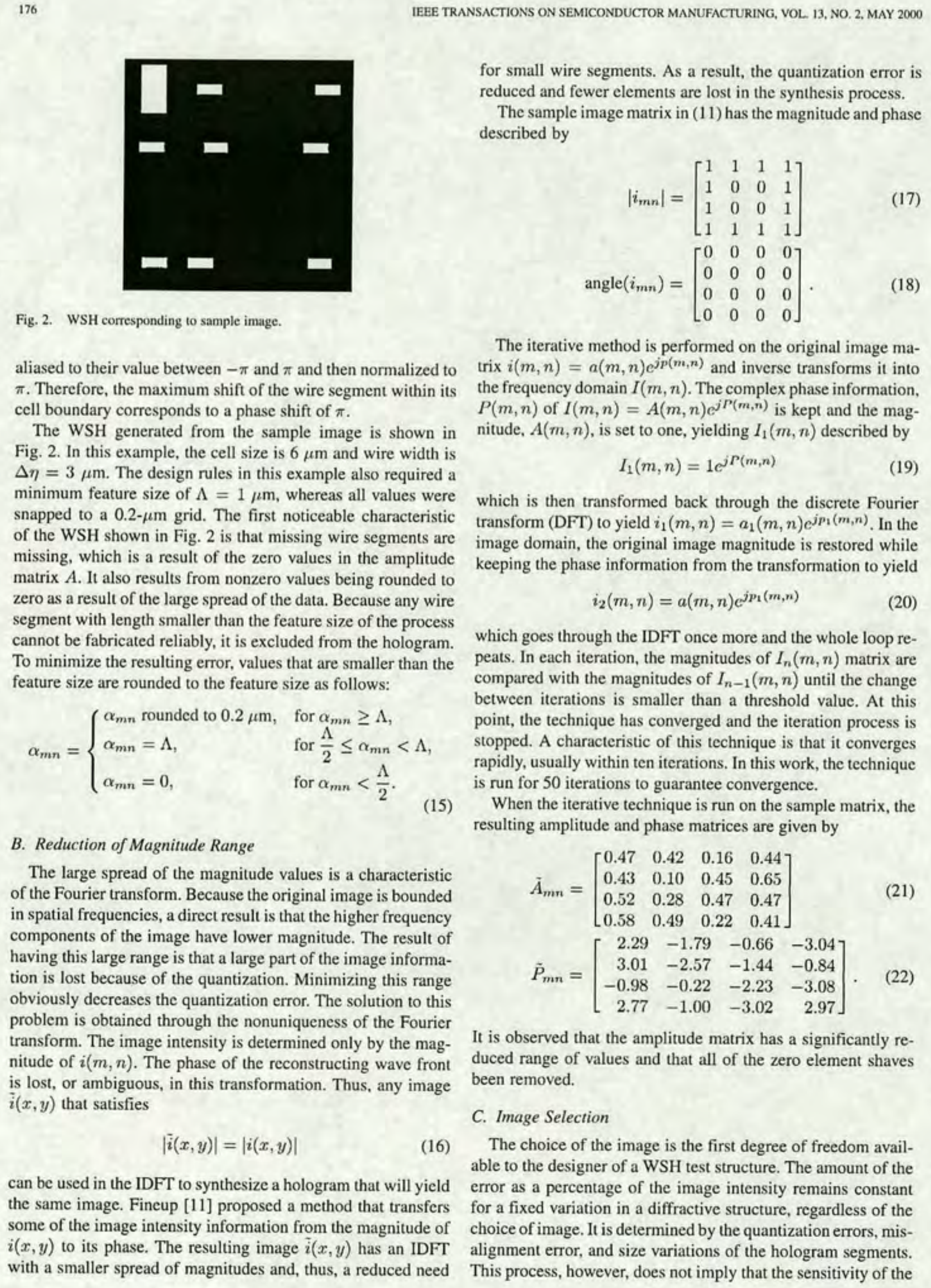

Fig. 2. WSH corresponding to sample image.

aliased to their value between $-\pi$ and π and then normalized to π. Therefore, the maximum shift of the wire segment within its cell boundary corresponds to a phase shift of π.

The WSH generated from the sample image is shown in Fig. 2. In this example, the cell size is 6 μm and wire width is $\Delta\eta = 3$ μm. The design rules in this example also required a minimum feature size of $\Lambda = 1$ μm, whereas all values were snapped to a 0.2-μm grid. The first noticeable characteristic of the WSH shown in Fig. 2 is that missing wire segments are missing, which is a result of the zero values in the amplitude matrix A. It also results from nonzero values being rounded to zero as a result of the large spread of the data. Because any wire segment with length smaller than the feature size of the process cannot be fabricated reliably, it is excluded from the hologram. To minimize the resulting error, values that are smaller than the feature size are rounded to the feature size as follows:

$$\alpha_{mn} = \begin{cases} \alpha_{mn} \text{ rounded to } 0.2\ \mu\text{m}, & \text{for } \alpha_{mn} \geq \Lambda, \\ \alpha_{mn} = \Lambda, & \text{for } \frac{\Lambda}{2} \leq \alpha_{mn} < \Lambda, \\ \alpha_{mn} = 0, & \text{for } \alpha_{mn} < \frac{\Lambda}{2}. \end{cases} \tag{15}$$

B. Reduction of Magnitude Range

The large spread of the magnitude values is a characteristic of the Fourier transform. Because the original image is bounded in spatial frequencies, a direct result is that the higher frequency components of the image have lower magnitude. The result of having this large range is that a large part of the image information is lost because of the quantization. Minimizing this range obviously decreases the quantization error. The solution to this problem is obtained through the nonuniqueness of the Fourier transform. The image intensity is determined only by the magnitude of $i(m,n)$. The phase of the reconstructing wave front is lost, or ambiguous, in this transformation. Thus, any image $\bar{i}(x,y)$ that satisfies

$$|\bar{i}(x,y)| = |i(x,y)| \tag{16}$$

can be used in the IDFT to synthesize a hologram that will yield the same image. Fineup [11] proposed a method that transfers some of the image intensity information from the magnitude of $i(x,y)$ to its phase. The resulting image $\bar{i}(x,y)$ has an IDFT with a smaller spread of magnitudes and, thus, a reduced need for small wire segments. As a result, the quantization error is reduced and fewer elements are lost in the synthesis process.

The sample image matrix in (11) has the magnitude and phase described by

$$|i_{mn}| = \begin{bmatrix} 1 & 1 & 1 & 1 \\ 1 & 0 & 0 & 1 \\ 1 & 0 & 0 & 1 \\ 1 & 1 & 1 & 1 \end{bmatrix} \tag{17}$$

$$\text{angle}(i_{mn}) = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}. \tag{18}$$

The iterative method is performed on the original image matrix $i(m,n) = a(m,n)e^{jp(m,n)}$ and inverse transforms it into the frequency domain $I(m,n)$. The complex phase information, $P(m,n)$ of $I(m,n) = A(m,n)e^{jP(m,n)}$ is kept and the magnitude, $A(m,n)$, is set to one, yielding $I_1(m,n)$ described by

$$I_1(m,n) = 1e^{jP(m,n)} \tag{19}$$

which is then transformed back through the discrete Fourier transform (DFT) to yield $i_1(m,n) = a_1(m,n)e^{jp_1(m,n)}$. In the image domain, the original image magnitude is restored while keeping the phase information from the transformation to yield

$$i_2(m,n) = a(m,n)e^{jp_1(m,n)} \tag{20}$$

which goes through the IDFT once more and the whole loop repeats. In each iteration, the magnitudes of $I_n(m,n)$ matrix are compared with the magnitudes of $I_{n-1}(m,n)$ until the change between iterations is smaller than a threshold value. At this point, the technique has converged and the iteration process is stopped. A characteristic of this technique is that it converges rapidly, usually within ten iterations. In this work, the technique is run for 50 iterations to guarantee convergence.

When the iterative technique is run on the sample matrix, the resulting amplitude and phase matrices are given by

$$\bar{A}_{mn} = \begin{bmatrix} 0.47 & 0.42 & 0.16 & 0.44 \\ 0.43 & 0.10 & 0.45 & 0.65 \\ 0.52 & 0.28 & 0.47 & 0.47 \\ 0.58 & 0.49 & 0.22 & 0.41 \end{bmatrix} \tag{21}$$

$$\bar{P}_{mn} = \begin{bmatrix} 2.29 & -1.79 & -0.66 & -3.04 \\ 3.01 & -2.57 & -1.44 & -0.84 \\ -0.98 & -0.22 & -2.23 & -3.08 \\ 2.77 & -1.00 & -3.02 & 2.97 \end{bmatrix}. \tag{22}$$

It is observed that the amplitude matrix has a significantly reduced range of values and that all of the zero element shaves been removed.

C. Image Selection

The choice of the image is the first degree of freedom available to the designer of a WSH test structure. The amount of the error as a percentage of the image intensity remains constant for a fixed variation in a diffractive structure, regardless of the choice of image. It is determined by the quantization errors, misalignment error, and size variations of the hologram segments. This process, however, does not imply that the sensitivity of the

Figure B.27: *Reprint of paper published in IEEE Transactions on Semiconductor Maunfacturing, May 2000, page 4*

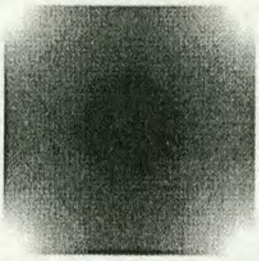

Fig. 3. Null image used in this work.

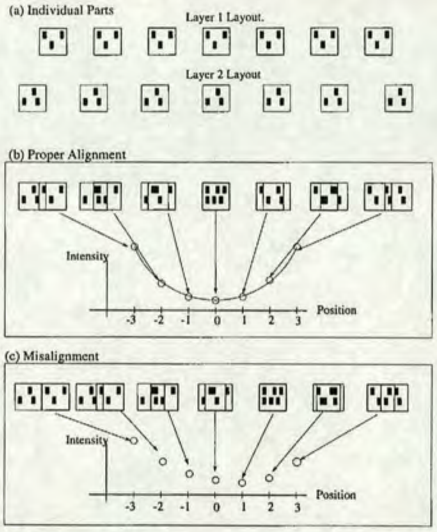

Fig. 4. Alignment POT Structure. (a) Layout of separated parts of WSH in their respective layers. Each square represents the position of the set of segments of the WSH. (b) Proper alignment results in the middle structure yielding the lowest null intensity. (c) Misalignment shifts the intensity minimum to a different position. The position of the new minimum points to the amount of misalignment.

technique does not depend on the choice of the image. The limited dynamic range and sensitivity of optical detectors make it necessary to choose an image that takes full advantage of the performance of the detector. An image should be chosen so that it uses the full dynamic range of the detector without saturating it. The maximum image intensity should be low enough so that variations in the intensity are detectable. Detectors have a finite number of quantization levels. If the changes in the image that result from process variations are smaller than the quantization step of the detector, the technique will fail.

Fig. 3 shows the image used in this work. The image is designed to have a central null region surrounded by annular region of high signal intensity. In order to reduce the effects of aliasing a raised-cosine function was selected to produce the central null because this is characterized by a narrow spatial bandwidth. If errors are introduced into the fabricated wire segments, the light intensity measured over the area of the central null region will increase, whereas the light intensity measured over the area of the bright outer region will decrease. We have therefore found it convenient to use ratio of the light detected in the central null to the light detected in the bright outer region, as a measure of the average error in the WSH. This quantity is referred to as the average intensity ratio (AIR).

D. Mask Generation

In the ideal case, no illumination is expected in the null region. Quantization errors inherent in the design process allow for the fabrication of these hologram (minimum feature and step sizes). These errors, along with reflections from the optical system, cause an imperfect null. Furthermore, process variations in metal height and profile obviously have an effect on the absolute value of the intensity of the image, which makes it more difficult to use the absolute sum of intensity as the measure for the degree of misalignment. To avoid the need for calibration, the use of POT is proposed [3], [4].

Testing for alignment offset involves moving a subset of the WSH elements with respect to each other. A number of the wire segments are randomly selected and designated as one part of the WSH, whereas the remaining segments constitute the other part. Each of these parts can be moved with respect to the other independently or completely separated into a different mask or layer. Several methods for identifying the element subsets were tried (e.g., alternate elements), and it was found that the random separation of wire segments into their respective parts provided the highest sensitivity of the null image to alignment variations.

The first part of the hologram is printed several times in array with constant separation, as shown in Fig. 4(a). The second part is arranged with increasing separation further from the center. When printed on top of the first layer, only one WSH in the array will have the proper alignment. When illuminated, this structure will give the best null image. Thus, it is possible to determine the alignment of the process directly by examining which section of the POT array is associated with the detected minimum in the AIR [3], [4].

IV. EXPERIMENTAL METHOD AND RESULTS

The null image was sampled using a 50×50 pixel matrix resulting in a 2DIDFT matrix containing 50×50 complex matrix elements. Because each element of this matrix corresponds to a wire segment in the WSH, the resulting WSH is an array of 50×50 wire segments. This WSH was tiled in a 2×2 grid to ensure that the available laser beam diameter is smaller than the extent of the WSH structure, as assumed by scalar diffraction theory. Each wire segment had a nominal width of $2\ \mu\text{m}$ and a height that varied between 1 and $5\ \mu\text{m}$, depending on the relative magnitude of the 2DIDFT matrix at the corresponding location. Each segment is placed within the boundaries of its own area $(6\ \mu\text{m})^2$. The final WSH structure is a 100×100 array of wire segments covering an area of $(600\ \mu\text{m})^2$.

Figure B.28: *Reprint of paper published in IEEE Transactions on Semiconductor Maunfacturing, May 2000, page 5*

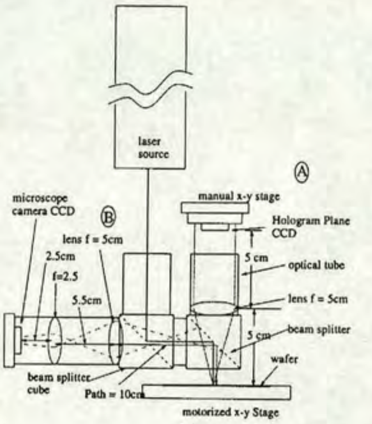

Fig. 5. Optical measurement system.

Fig. 5 illustrates the main configuration of the optical setup. The $2f$ optical system is labeled **A** in the figure. It consists of the stage that holds the wafer, a lens with a focal length $f \approx 50$ mm, and a CCD array placed in the Fourier plane of the lens. The x-y stage is fixed in a position relative to the direction of beam travel. The remainder of the setup is connected to a vertical stage so that it can be repositioned relative to the stage. This process allows the testing of several samples with varying thicknesses. The CCD array is also placed on a manual x-y-z stage that can move independently relative to the lens and sample. This feature makes it possible to move around the image plane to select the desired image order. This movement is necessary because of the limited size of the CCD array relative to the holographic image plane. The microscope camera setup is used to view the structures on the wafer. It is also used to position the laser beam in the desired area on the wafer, which allows for the correct correspondence between the structure and the image.

A. Simulated Alignment Offset

Characterizing the sensitivity of the WSH's to alignment variations was the focus of the first set of experimental structures. For this purpose, the offset between the parts of the hologram had to be known in advance, which was accomplished by fabricating an array of WSH's with simulated x-alignment offsets between the two parts of 0.0, 0.1, 0.2, 0.3, and 0.5 μm designed into the mask. The mask was printed using a 10× g-line stepper. Each structure was tested by illuminating it with a Green He–Ne laser with $\lambda = 543.6$ nm and capturing the projected image using a CCD array placed at the focal length of a Fourier lens [2], [7]. Fig. 6 shows the degradation of the null in the center of the image as alignment error is introduced (because of limitations in the printing process, the degradation of the image on the page is not as pronounced as the actual degradation of the projected image).

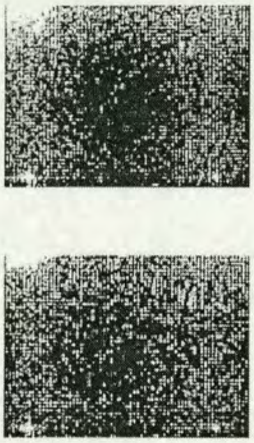

Fig. 6. The degradation in the image as alignment offset is introduced. Top image is designed with 0 μm alignment offset, and bottom image has 0.5 μm alignment offset between the two parts of the WSH.

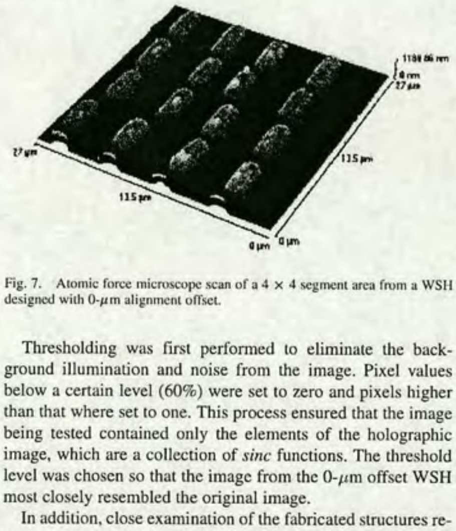

Fig. 7. Atomic force microscope scan of a 4 × 4 segment area from a WSH designed with 0-μm alignment offset.

Thresholding was first performed to eliminate the background illumination and noise from the image. Pixel values below a certain level (60%) were set to zero and pixels higher than that where set to one. This process ensured that the image being tested contained only the elements of the holographic image, which are a collection of *sinc* functions. The threshold level was chosen so that the image from the 0-μm offset WSH most closely resembled the original image.

In addition, close examination of the fabricated structures revealed variations in metal height and edge profile between structures (see Fig. 7). Previous work has shown these type of variations to affect overall intensity of the image but not the relative contrast between its parts. Thus, the ratio of the average intensity within the null region radius to that of the average intensity per pixel in the area of twice the radius surrounding it is used as the measure of null quality. With no error present, this ratio is expected to be zero. With the quantization errors, however,

Figure B.29: *Reprint of paper published in IEEE Transactions on Semiconductor Maunfacturing, May 2000, page 6*

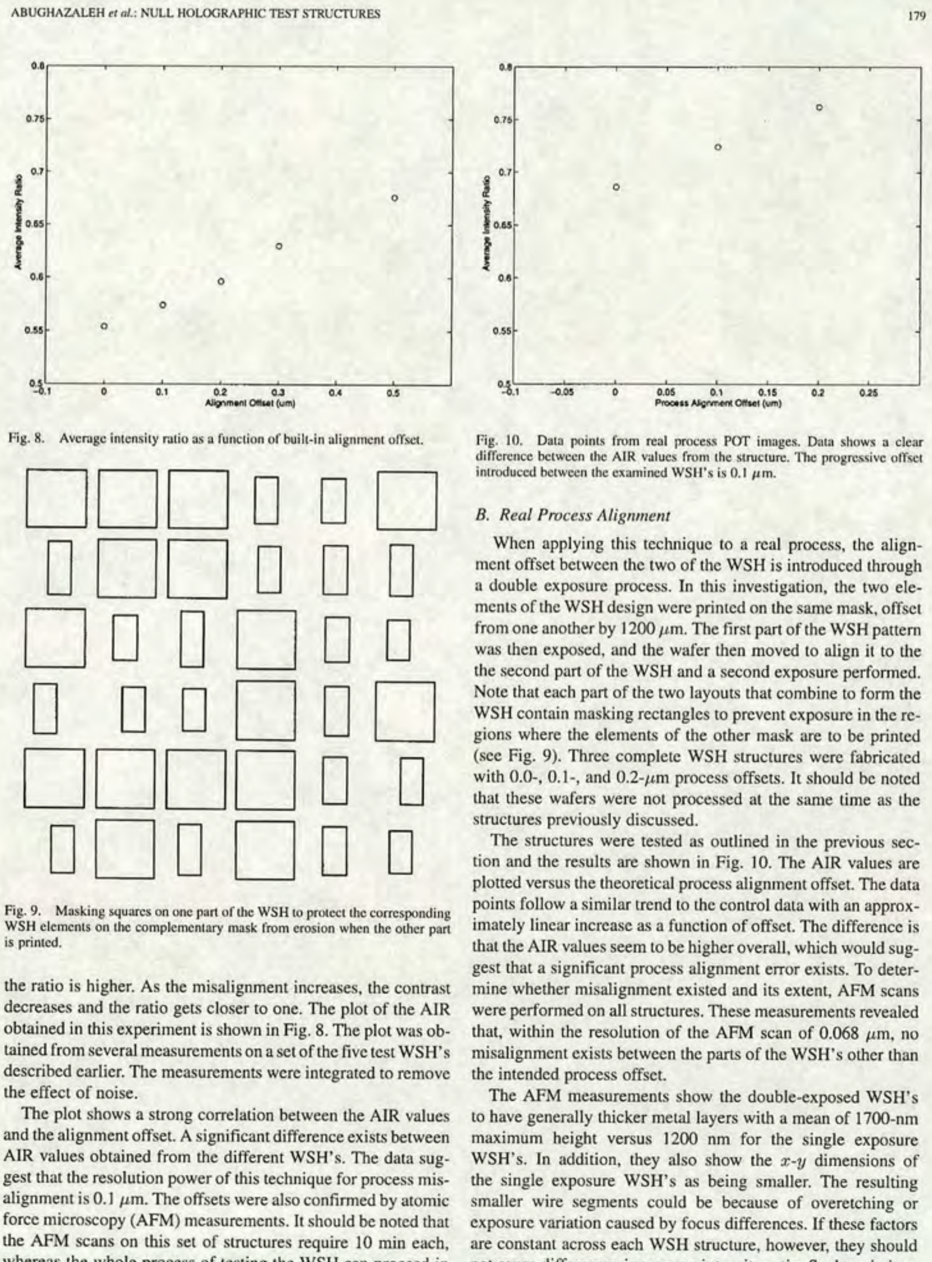

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Fig. 8. Average intensity ratio as a function of built-in alignment offset.

Fig. 9. Masking squares on one part of the WSH to protect the corresponding WSH elements on the complementary mask from erosion when the other part is printed.

the ratio is higher. As the misalignment increases, the contrast decreases and the ratio gets closer to one. The plot of the AIR obtained in this experiment is shown in Fig. 8. The plot was obtained from several measurements on a set of the five test WSH's described earlier. The measurements were integrated to remove the effect of noise.

The plot shows a strong correlation between the AIR values and the alignment offset. A significant difference exists between AIR values obtained from the different WSH's. The data suggest that the resolution power of this technique for process misalignment is 0.1 μm. The offsets were also confirmed by atomic force microscopy (AFM) measurements. It should be noted that the AFM scans on this set of structures require 10 min each, whereas the whole process of testing the WSH can proceed in close to real time when automated.

Fig. 10. Data points from real process POT images. Data shows a clear difference between the AIR values from the structure. The progressive offset introduced between the examined WSH's is 0.1 μm.

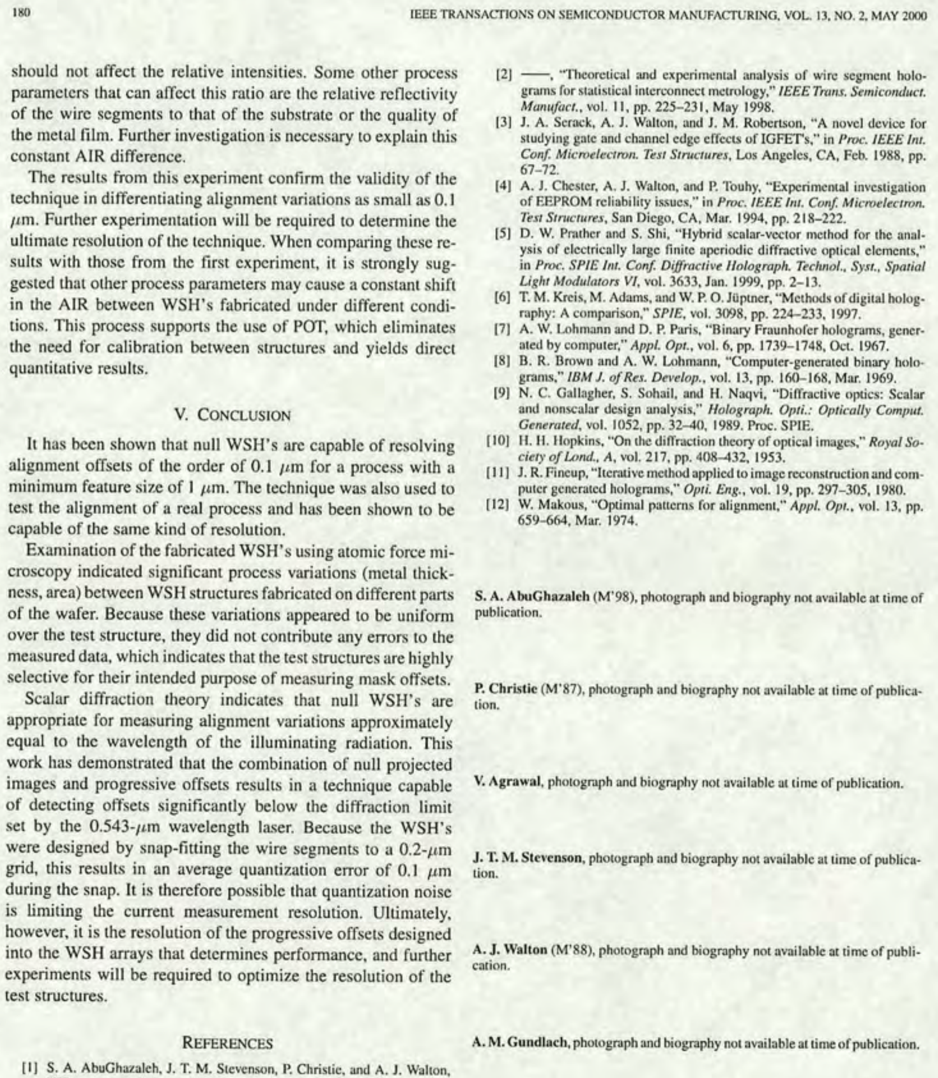
B. Real Process Alignment

When applying this technique to a real process, the alignment offset between the two of the WSH is introduced through a double exposure process. In this investigation, the two elements of the WSH design were printed on the same mask, offset from one another by 1200 μm. The first part of the WSH pattern was then exposed, and the wafer then moved to align it to the the second part of the WSH and a second exposure performed. Note that each part of the two layouts that combine to form the WSH contain masking rectangles to prevent exposure in the regions where the elements of the other mask are to be printed (see Fig. 9). Three complete WSH structures were fabricated with 0.0-, 0.1-, and 0.2-μm process offsets. It should be noted that these wafers were not processed at the same time as the structures previously discussed.

The structures were tested as outlined in the previous section and the results are shown in Fig. 10. The AIR values are plotted versus the theoretical process alignment offset. The data points follow a similar trend to the control data with an approximately linear increase as a function of offset. The difference is that the AIR values seem to be higher overall, which would suggest that a significant process alignment error exists. To determine whether misalignment existed and its extent, AFM scans were performed on all structures. These measurements revealed that, within the resolution of the AFM scan of 0.068 μm, no misalignment exists between the parts of the WSH's other than the intended process offset.

The AFM measurements show the double-exposed WSH's to have generally thicker metal layers with a mean of 1700-nm maximum height versus 1200 nm for the single exposure WSH's. In addition, they also show the x-y dimensions of the single exposure WSH's as being smaller. The resulting smaller wire segments could be because of overetching or exposure variation caused by focus differences. If these factors are constant across each WSH structure, however, they should not cause differences in average intensity ratio. Such variations can cause overall intensity changes in the image, but they

Figure B.30: *Reprint of paper published in IEEE Transactions on Semiconductor Maunfacturing, May 2000, page 7*



should not affect the relative intensities. Some other process parameters that can affect this ratio are the relative reflectivity of the wire segments to that of the substrate or the quality of the metal film. Further investigation is necessary to explain this constant AIR difference.

The results from this experiment confirm the validity of the technique in differentiating alignment variations as small as 0.1 μm. Further experimentation will be required to determine the ultimate resolution of the technique. When comparing these results with those from the first experiment, it is strongly suggested that other process parameters may cause a constant shift in the AIR between WSH's fabricated under different conditions. This process supports the use of POT, which eliminates the need for calibration between structures and yields direct quantitative results.

V. CONCLUSION

It has been shown that null WSH's are capable of resolving alignment offsets of the order of 0.1 μm for a process with a minimum feature size of 1 μm. The technique was also used to test the alignment of a real process and has been shown to be capable of the same kind of resolution.

Examination of the fabricated WSH's using atomic force microscopy indicated significant process variations (metal thickness, area) between WSH structures fabricated on different parts of the wafer. Because these variations appeared to be uniform over the test structure, they did not contribute any errors to the measured data, which indicates that the test structures are highly selective for their intended purpose of measuring mask offsets.

Scalar diffraction theory indicates that null WSH's are appropriate for measuring alignment variations approximately equal to the wavelength of the illuminating radiation. This work has demonstrated that the combination of null projected images and progressive offsets results in a technique capable of detecting offsets significantly below the diffraction limit set by the 0.543-μm wavelength laser. Because the WSH's were designed by snap-fitting the wire segments to a 0.2-μm grid, this results in an average quantization error of 0.1 μm during the snap. It is therefore possible that quantization noise is limiting the current measurement resolution. Ultimately, however, it is the resolution of the progressive offsets designed into the WSH arrays that determines performance, and further experiments will be required to optimize the resolution of the test structures.

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V. Agrawal, photograph and biography not available at time of publication.

J. T. M. Stevenson, photograph and biography not available at time of publication.

A. J. Walton (M'88), photograph and biography not available at time of publication.

A. M. Gundlach, photograph and biography not available at time of publication.

S. Smith, photograph and biography not available at time of publication.

Figure B.31: *Reprint of paper published in IEEE Transactions on Semiconductor Maunfacturing, May 2000, page 8*

Evaluation of the Issues Involved with Test Structures for the Measurement of Sheet Resistance and Linewidth of Copper Damascene Interconnect

S. Smith, A.J. Walton, A.W.S. Ross, G.K.H. Bodammer and J.T.M. Stevenson

Department of Electronics and Electrical Engineering
Scottish Microelectronics Centre
Kings Buildings, The University of Edinburgh
Edinburgh, EH9 3JF, UK

ABSTRACT

The effect of the barrier layer and dishing in copper interconnect causes extra difficulties in measuring sheet resistance and linewidth when compared with equivalent measurements on non-damascene processed tracks. This paper examines these issues and, for the first time, quantifies the effects of diffusion barrier layers and CMP dishing on the extraction of R_s from Greek cross type structures and the effect this has on linewidth measurement.

INTRODUCTION

Advanced interconnect technologies are an essential part of the roadmap for improving the performance of integrated circuits. As a result copper is set to rapidly replace aluminium because it has a lower resistivity which, when combined with the introduction of low-*k* dielectrics, reduces RC time delays and power consumption [1]. A damascene CMP process is typically used for fabricating copper interconnect, largely as a result of the difficulty associated with dry etching copper. Barrier layers are also required to prevent copper diffusing elsewhere which adds to the complexity of processing as well as complicating the measurement of sheet resistance.

Resistive electrical test structures used to measure the linewidth of conducting tracks assume a homogeneous layer of conducting material. This is not the case for copper damascene interconnect because of the requirement to use barrier layers. Figure 1 shows a cross-section through two copper tracks with barrier layers and it can be deduced that as the width of the copper track decreases the percentage contribution of the barrier layer to the sheet resistance increases. For example, a tantalum diffusion barrier has a higher sheet resistance than copper ($\rho_{Cu} \approx 1.678\mu\Omega$-cm, $\rho_{Ta} \approx 13\mu\Omega$-cm) and a simple calculation based on the cross-sectional area can be used to calculate the resistance of a track [2]. The resistance of damascene copper tracks is also affected by the polishing process, typically resulting in dishing which causes the track to be thinner in the centre. The degree of dishing is a function of the track width, increasing in magnitude for wider tracks as shown in in figure 2. The resulting reduction in the cross sectional area increases the resistance [3, 4]. To electrically measure the linewidth of a conducting track the *effective* sheet resistance of the material must first be determined. This parameter is normally measured using either a Greek or a box cross because no dimensional information is required (see figure 3) in the extraction of R_s [5, 6]. This insensitivity to CD variation has made these types of structures the industry standard for measuring sheet resistance of conducting layers.

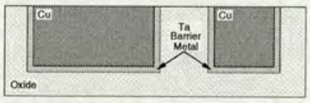


Figure 1. Cross-section of copper damascene tracks of different widths. As the width of the copper line decreases the relative contribution of the sidewall barrier layers to the track resistance becomes more important.

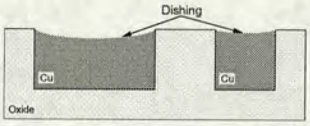
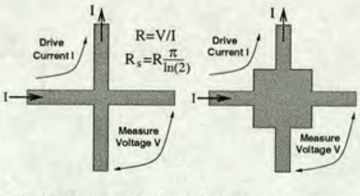


Figure 2. Schematic cross section through two metal damascene lines showing increased dishing with larger linewidths.



$R=V/I$

$R_s=R\frac{\pi}{\ln(2)}$

Figure 3. Greek cross and box cross sheet resistor structures used for extracting R_s.

However, both of these test structures will be affected by dishing and the diffusion barrier layer. Any error in the value of R_s will directly translate into an error in the value of linewidth extracted. Reference [2] discusses many of the issues associated with characterising copper interconnect and the purpose of this study is to, for the first time, quantify some of these effects.

Figure B.32: *Reprint of paper presented at ICMTS 2001, page 1.*

BARRIER LAYER EFFECTS

The first question that needs to be answered is the exact effect that the barrier layer has on the extracted value of R_s. The structure of the Greek cross used to perform this task is shown in figure 4. In this case the thickness of the tantalum barrier layer on the bottom and sidewalls of the trench was set to 50nm. A 2D simulator (Raphael) was used for the following simulations with the sheet resistance of the central region of the cross being equivalent to 500nm of copper over a 50nm thick barrier metal layer. The resistance of each sidewall barrier was set by assuming a layer of tantalum 550nm by the barrier layer thickness.

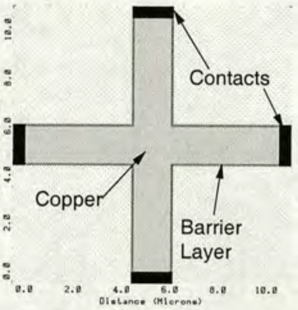


Figure 4. Greek cross test structure for simulation of barrier layer effects.

Simulations were performed for a range of linewidths with sidewall barrier layer thicknesses between 25 and 100nm. A 10 by 10μm box cross structure with a 50nm thick barrier layer was also simulated for a range of arm widths. The results of these simulations are presented in figure 5. For these simulations the sheet resistance of the copper over the thin barrier metal ($R_{s(Cu)}$) was set to 33. 132mΩ/□ and, as can be observed in figure 5, this is the sheet resistance extracted by the Greek crosses with large linewidths. For example, with a sidewall barrier layer thickness (W_b) of 100nm the extracted sheet resistance is within 1.3% of $R_{s(Cu)}$ for linewidths greater than 0.5μm. It can also be seen that as the barrier thickness is reduced the error in the extracted value of $R_{s(Cu)}$ associated with narrower tracks reduces e.g. with W_b = 25nm, R_s is always within 0.5% of $R_{s(Cu)}$. If an error in the measurement of sheet resistance of more than 1% is considered to be significant then further simulations must be made. From these it has been determined that for a copper track with a tantalum barrier layer the error in the sheet resistance will be less than 1% provided that $W_{Cu} > 5.6W_{Ta}$. Taking into account the ratio of resistivities of the copper and barrier layer a more general expression can be developed:

$$W_{Cu} > 43.4 \frac{R_{Cu}}{R_B} W_B \tag{1}$$

where R_B and W_B are the thickness and resistivity of the barrier layer. As would have been expected from the Greek cross results, figure 5 also shows that the tapwidth of the box cross structure does not affect the extraction of the copper over barrier layer sheet resistance.

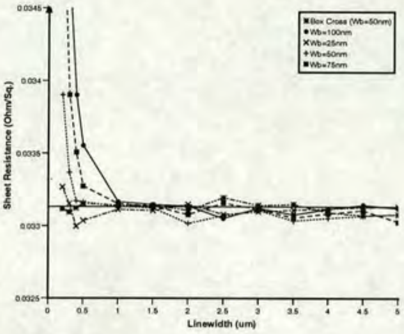


Figure 5. Extracted sheet resistance versus copper linewidth for simulated Greek cross structures with barrier layers.

The above results indicate that the majority of the current flows in the centre of the cross (i.e. copper) where the resistance is lowest. In the 2D simulations the resistivity specified in this region was the parallel combination of the the copper and the underlying barrier layer. This was the value of sheet resistance extracted but confirmation is required that the 2D approximation used is valid. Hence, simulations were also repeated in 3-dimensions using Raphael confirming that, for the conditions specified in equation (1), the extracted R_s is in fact that of the Cu in parallel with the underlying barrier layer. This is a useful observation which indicates that Greek cross structures can be used to measure the sheet resistance of copper and an underlying barrier layer.

DISHING EFFECTS

Equation (1) gives the conditions that are required to extract the copper over barrier layer sheet resistance but this assumes a track with a rectangular cross section. Unfortunately, the CMP process also affects the sheet resistance of conducting tracks through dishing and it is important to quantify the effect of this on the extraction of R_s. The dishing model used in this study is a function of the polishing time and parameters have been determined for two endpoint conditions [3]. These are for the nominal polishing time:

$$\alpha = 0.32e^{-0.008w} + 0.65 \tag{2}$$

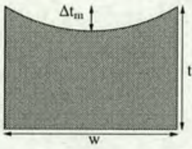
and for a 25% overpolish:

$$\alpha = 0.68e^{0.008w} + 0.22 \tag{3}$$

In these equations α is the the ratio of the metal thickness

Figure B.33: *Reprint of paper presented at ICMTS 2001, page 2.*

at the centre of the dished line to the ideal thickness and *w* is the linewidth as shown in figure 6.



$$A = t_m W\left(\frac{1+2\alpha}{3}\right)$$

$$\alpha = \frac{t_m - \Delta t_m}{t_m}$$

Figure 6. Cross section through a dished damascene track.

The following simulations approximate dishing as a stepped conducting track rather than a smooth curve, as illustrated in figure 7.

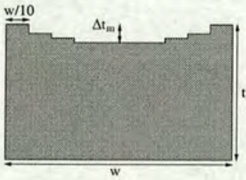


Figure 7. Cross section through a dished damascene track showing the stepped approximation of dishing used for the simulations.

This model was first simulated in two dimensions to determine the effect of dishing, for a 25% overpolish, on the extracted values of sheet resistance. The change in the metal thickness due to dishing is modelled in two dimensions as a change in the sheet resistance of the conducting area as is shown in Figure 8. The simulation results are presented in figure 9.

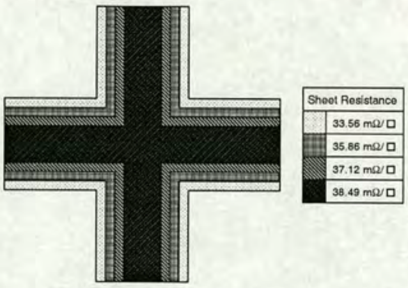


Figure 8. Plan view of a Greek cross with a linewidth of 5 μm showing how the dishing model is simulated in 2D. The sheet resistance of each part of the cross depends on the amount of dishing in that area.

For the 25% overpolish it can be observed that there is an offset of about 3% between the sheet resistance extracted from the Greek cross structures and that derived from the cross section of the line. The values of R_s extracted from the box cross do not increase with the width of the voltage taps because the dishing of the box is constant. The difference between the sheet resistance extracted from the box cross structure and the equivalent sheet resistance of the dished lines is greater (4% - 5%) simply because the larger dimensions of the box cross leads to more severe dishing.

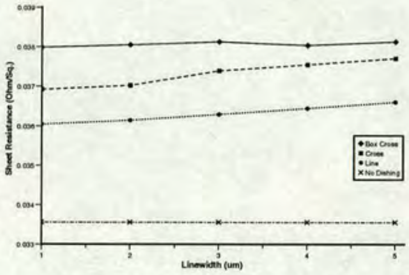


Figure 9. Sheet resistance against linewidth for 2D simulations of copper damascene Greek crosses with 25% overpolish. The values of R_s for the dished line were calculated using the equations for the cross sectional area given in figure 6.

However, this 2D approximation does not necessarily reflect the actual current flow in the test structures and so 3D simulations were also performed. The dishing model was changed slightly for the 3D simulations in order to achieve a more accurate model of dishing in the centre of the Greek cross. Because the amount of dishing is dependent on the linewidth it would be expected that the depth of copper removed in the centre would be more than in the arms of the cross. Using the model described above a new depth of dishing was calculated for the centre of the cross. The value of linewidth (*w*) used in equations (2) and (3) is the diagonal width of the cross measured between opposite internal corners. In order to achieve the correct profile across the centre of the cross in the simulated structure, cylindrical sections of the conducting track were removed. This is illustrated in Figure 10.

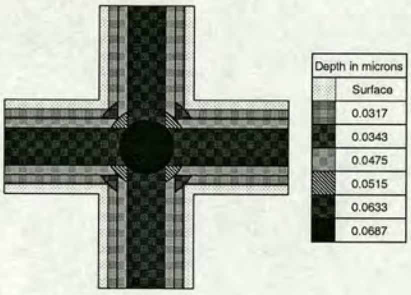


Figure 10. Plan view of a Greek cross with a linewidth of 5 μm showing the three dimensional dishing model.

Figure B.34: *Reprint of paper presented at ICMTS 2001, page 3.*

For these simulations both the nominal and the 25% polish endpoint models were used and the results are presented in figure 11.

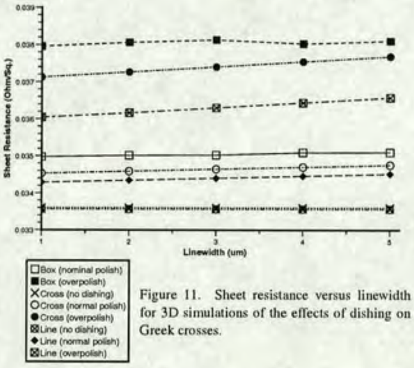


Figure 11. Sheet resistance versus linewidth for 3D simulations of the effects of dishing on Greek crosses.

The results for the 3D simulations with 25% overpolish compare well with the 2D results indicating that the assumptions of the 2D model approximating the dishing effect are reasonably valid for these structures. From figure 11 it can be observed that the offset between the line and cross sheet resistances is approximately 0.7% for the nominal polish conditions and 3% for the structures with 25% overpolish. The results indicate that the errors in extracted sheet resistance increase with the amount of dishing. However, the model for dishing in the centre of the Greek cross still may not reflect the true structure. In order to try and confirm the validity of the model AFM scans of real copper damascene structures have been performed and figure 12 shows the results of one scan of a Greek cross.

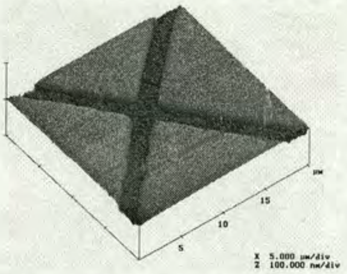


Figure 12. 20 × 20 μm AFM scan of a copper damascene Greek cross test structure. The arms of the cross are 1 μm wide.

It is not possible to tell from figure 12 if there is more dishing in the centre of the cross but figure 13 shows AFM profiles taken across the centre and arms of the same cross. The CMP process employed is a two stage process with the first polish stopping on the tantalum barrier layer. The sample tested here was stopped at that stage of the process to eliminate the effects of dielectric erosion which could swamp any dishing effects from the measurement. It can be seen that the results of the two profiles taken across the centre of the cross agree quite well. The average depth of the copper dishing in the centre of the cross is greater than the depth measured in the arm of the cross by between 2 and 3 nm. This difference in depth is similar to those modelled for the 3D simulations described above.

LINEWIDTH MEASUREMENTS

Any error in the measurement of the sheet resistance is directly translated into an error in the linewidth extracted. The previous discussions have indicated that this can come from either the barrier layer or from dishing.

Barrier layers

Provided equation (1) is satisfied and there is no dishing then the resistance of the measured layer is the parallel combination of the copper and the underlying barrier layer. However, the parameters associated with the contribution of the sidewall barriers to resistance are also required and reference [2] gives a methodology to obtain them. It should be noted that barrier sidewall thickness will be less than the thickness on a flat surface for narrow lines ($W_{Cu} < 4W_B$) due to a shadowing effect during deposition [2]. The narrower tracks will also have a higher resistance due to a reduction in copper grain size [7]. For the purposes of the simulations both copper sheet resistance and sidewall barrier thickness have been assumed to be constant. The resistances of 100 μm long copper damascene lines have been calculated with the same parameters as those used in the Greek cross simulations. The effects of the sidewall barrier layers have been subtracted and R_{line} used to calculate the linewidth using the sheet resistances obtained from simulations.

$$W_{line} = \frac{L \cdot R_s}{R_{line}} \tag{4}$$

The percentage errors between the extracted linewidths and the "drawn" linewidths were calculated and are presented in figure 14. It can be observed that as the barrier width increases, the errors at low values of drawn linewidth also increase. It should be noted that the box cross is insensitive to sidewall barrier layer thickness and, assuming there is no dishing, should be used in preference to a Greek cross.

Dishing

Dishing makes the extraction of sheet resistance using a Van der Pauw measurement problematic because the layer thickness is no longer constant. Figure 15 shows the linewidth error caused by dishing for the 3D Greek cross and 2D box cross structure. The linewidth errors for the Greek crosses do not vary with tap width staying at about

Figure B.35: *Reprint of paper presented at ICMTS 2001, page 4.*

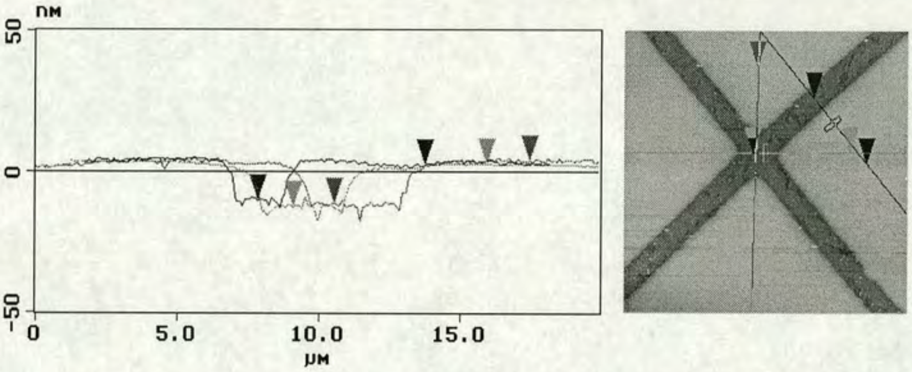


Figure 13. On the left is a set of three AFM surface profiles from a CMP copper structure. On the right is a 256 × 256 AFM scan showing where the profiles have been taken from.

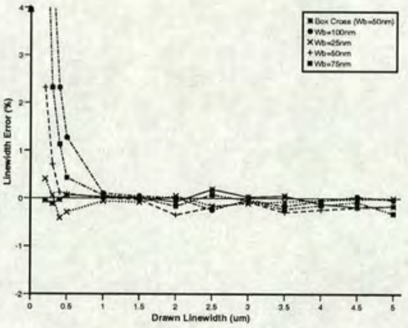


Figure 14. Linewidth error versus designed linewidth for the simulations of barrier layer effects.

3% for the 25% overpolish condition and about 0.7% for the nominal polish. The box cross results are different because the amount of dishing in the box does not change with the tapwidth. This means the error will depend upon the drawn width of the the line. These results indicate that, provided equation (1) is not violated and instrumentation and Joule heating are not issues [2] then sheet resistance measurements should be made on Greek cross structures with track widths the same as those used on the linewidth structures being tested.

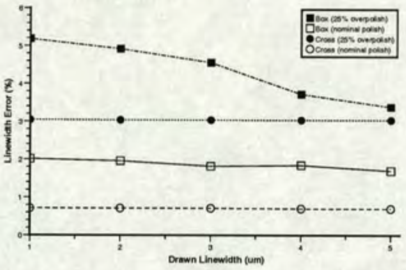


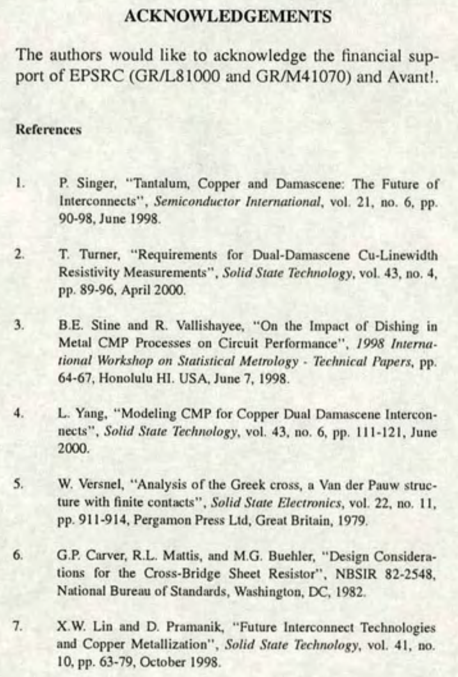
Figure 15. Linewidth error versus designed linewidth for the simulations of CMP dishing.

CONCLUSIONS AND FURTHER WORK

This work has quantified the effect of barrier layers and dishing on the measurement of the sheet resistance and linewidth of copper interconnect. A Greek cross structure can be used to measure the sheet resistance of the copper and underlying barrier with an error less than 1% provided $W_{Cu} > 43.4 \frac{R_{Cu}}{R_B} W_B$. The effect of dishing on the extraction of sheet resistance from Greek crosses has been evaluated and for a nominal dishing has been shown to contribute an error of less than 1%. For a 25% overpolish this rises to about 3%. Because of its larger dimensions the dishing associated with a box cross is considerably enhanced and hence a larger error in sheet resistance results. All of these errors are directly transferred into electrical based linewidth measurements.

Measurements of a copper CMP structure using an AFM appear to validate the 3D model of dishing in a Greek cross. Future work will involve fabricating more test structures with a range of different linewidths. These will be tested both electrically and with the AFM to further confirm the simulation results presented in this paper.

Figure B.36: *Reprint of paper presented at ICMTS 2001, page 5.*



ACKNOWLEDGEMENTS

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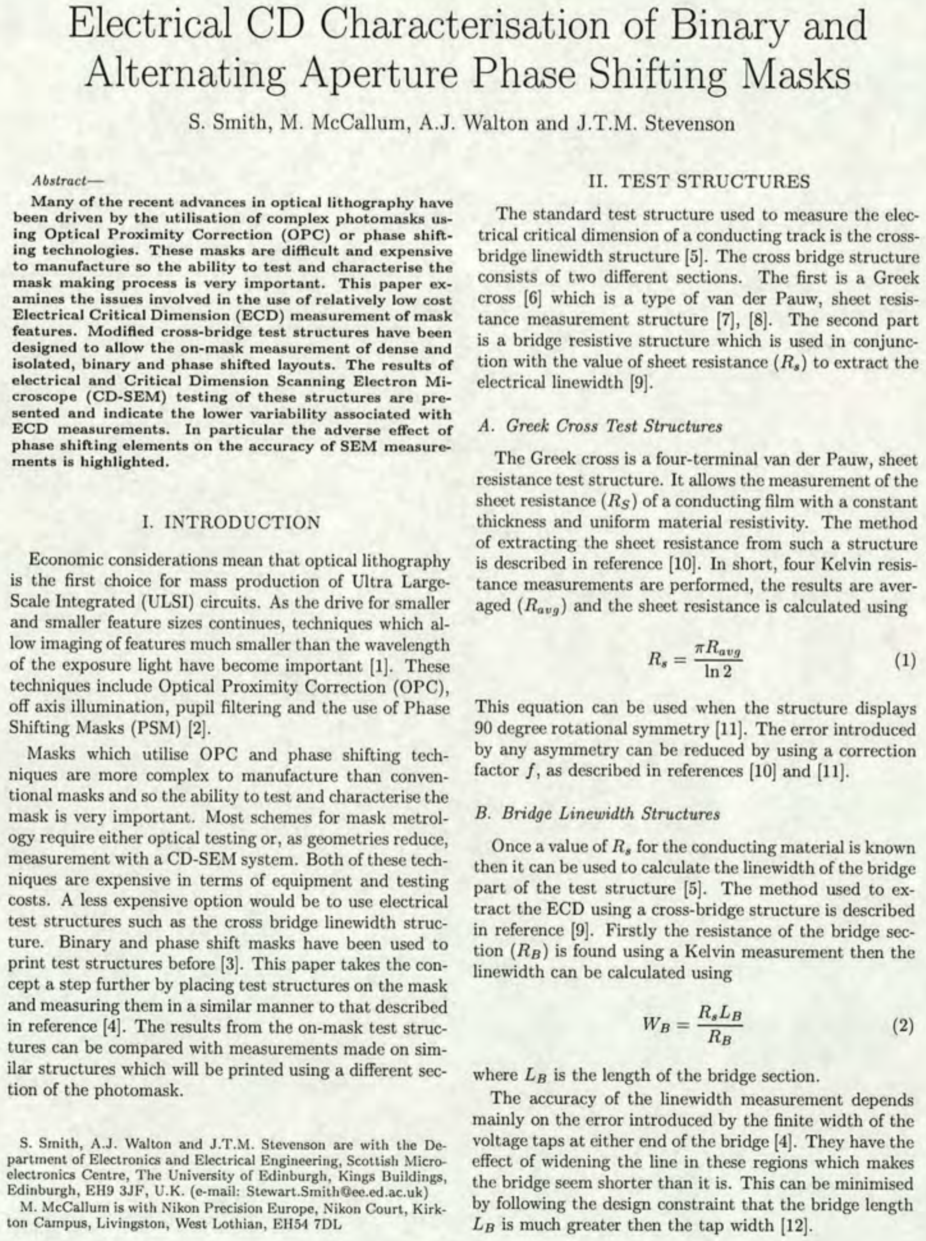
Figure B.37: *Reprint of paper presented at ICMTS 2001, page 6.*



Electrical CD Characterisation of Binary and Alternating Aperture Phase Shifting Masks

S. Smith, M. McCallum, A.J. Walton and J.T.M. Stevenson

Abstract—

Many of the recent advances in optical lithography have been driven by the utilisation of complex photomasks using Optical Proximity Correction (OPC) or phase shifting technologies. These masks are difficult and expensive to manufacture so the ability to test and characterise the mask making process is very important. This paper examines the issues involved in the use of relatively low cost Electrical Critical Dimension (ECD) measurement of mask features. Modified cross-bridge test structures have been designed to allow the on-mask measurement of dense and isolated, binary and phase shifted layouts. The results of electrical and Critical Dimension Scanning Electron Microscope (CD-SEM) testing of these structures are presented and indicate the lower variability associated with ECD measurements. In particular the adverse effect of phase shifting elements on the accuracy of SEM measurements is highlighted.

I. INTRODUCTION

Economic considerations mean that optical lithography is the first choice for mass production of Ultra Large-Scale Integrated (ULSI) circuits. As the drive for smaller and smaller feature sizes continues, techniques which allow imaging of features much smaller than the wavelength of the exposure light have become important [1]. These techniques include Optical Proximity Correction (OPC), off axis illumination, pupil filtering and the use of Phase Shifting Masks (PSM) [2].

Masks which utilise OPC and phase shifting techniques are more complex to manufacture than conventional masks and so the ability to test and characterise the mask is very important. Most schemes for mask metrology require either optical testing or, as geometries reduce, measurement with a CD-SEM system. Both of these techniques are expensive in terms of equipment and testing costs. A less expensive option would be to use electrical test structures such as the cross bridge linewidth structure. Binary and phase shift masks have been used to print test structures before [3]. This paper takes the concept a step further by placing test structures on the mask and measuring them in a similar manner to that described in reference [4]. The results from the on-mask test structures can be compared with measurements made on similar structures which will be printed using a different section of the photomask.

II. TEST STRUCTURES

The standard test structure used to measure the electrical critical dimension of a conducting track is the cross-bridge linewidth structure [5]. The cross bridge structure consists of two different sections. The first is a Greek cross [6] which is a type of van der Pauw, sheet resistance measurement structure [7], [8]. The second part is a bridge resistive structure which is used in conjunction with the value of sheet resistance (R_s) to extract the electrical linewidth [9].

A. Greek Cross Test Structures

The Greek cross is a four-terminal van der Pauw, sheet resistance test structure. It allows the measurement of the sheet resistance (R_S) of a conducting film with a constant thickness and uniform material resistivity. The method of extracting the sheet resistance from such a structure is described in reference [10]. In short, four Kelvin resistance measurements are performed, the results are averaged (R_{avg}) and the sheet resistance is calculated using

$$R_s = \frac{\pi R_{avg}}{\ln 2} \tag{1}$$

This equation can be used when the structure displays 90 degree rotational symmetry [11]. The error introduced by any asymmetry can be reduced by using a correction factor f, as described in references [10] and [11].

B. Bridge Linewidth Structures

Once a value of R_s for the conducting material is known then it can be used to calculate the linewidth of the bridge part of the test structure [5]. The method used to extract the ECD using a cross-bridge structure is described in reference [9]. Firstly the resistance of the bridge section (R_B) is found using a Kelvin measurement then the linewidth can be calculated using

$$W_B = \frac{R_s L_B}{R_B} \tag{2}$$

where L_B is the length of the bridge section.

The accuracy of the linewidth measurement depends mainly on the error introduced by the finite width of the voltage taps at either end of the bridge [4]. They have the effect of widening the line in these regions which makes the bridge seem shorter than it is. This can be minimised by following the design constraint that the bridge length L_B is much greater then the tap width [12].

S. Smith, A.J. Walton and J.T.M. Stevenson are with the Department of Electronics and Electrical Engineering, Scottish Microelectronics Centre, The University of Edinburgh, Kings Buildings, Edinburgh, EH9 3JF, U.K. (e-mail: Stewart.Smith@ee.ed.ac.uk)

M. McCallum is with Nikon Precision Europe, Nikon Court, Kirkton Campus, Livingston, West Lothian, EH54 7DL

Figure B.38: *Reprint of paper presented at ICMTS 2002, page 1.*

C. PSM Test Structures

Cross-bridge test structures which were developed to investigate metal damascene interconnect processes have been adapted for use with alternating phase shifting masks. In the "dense" test structures the electrically measured line is surrounded by floating lines and phase shifting regions in a similar way to the AltPSM test sites described in reference [3]. This is illustrated in figure 1.

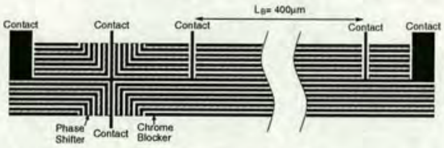


Fig. 1. Section of PSM test structure layout. The black areas are the chrome blockers while the shaded areas are regions of 180° phase shift. This is a structure with a linewidth of 1.5μm and a line to space ratio of 1:1.

The PSM layout contains test structures with on mask linewidths of 0.4, 0.5, 0.6, 0.7, 0.8, 0.9, 1.0, 1.1, 1.2 and 1.5μm. Bridge structures with line to space ratios of 1:1, 1:1.5, 1:2, 1:3, 1:5 and 1:10 were designed for each of the feature sizes. There are two sets of dense structures with different arrangements of the dummy lines around the Greek cross. The first set resemble figure 1, where the floating lines follow the shape of the cross, and these will be referred to as "L-Type" structures. In the second set the unmeasured lines run up to the vertical contact arms of the cross and stop short as they do in the bridge section of the structure. This set will be referred to as "I-Type" test structures. The full layout is a 14 × 10 array of test structures with probe pads which can be probed on-mask using a standard 2×n probe card. This includes two isolated linewidth structures for each feature size. A second layout has also been designed where the probe pads are scaled so that when the structures are printed using a 4× exposure tool the pads will be the same size as those designed for on-mask measurement. Figure 2 shows lines with a CD of 91nm which were printed in photoresist using the 0.4μm features on the photomask.

Fig. 2. SEM image of 91nm wide lines printed using a S202 scanner (0.6NA) and the phase shift mask used in this study.

The layout with the large pads has been repeated three times on the mask, once with the phase shifting elements removed to give binary structures. The version with the small pads for on-mask testing is repeated 24 times on the mask and again 8 of these are binary features. A picture of the mask can be seen in figure 3 along with a closeup of the layout for on-mask probing.

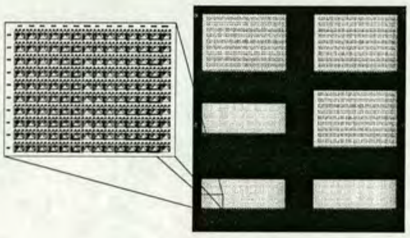


Fig. 3. Photograph of the actual phase shifting mask with a close up view of the layout of one of the sets of on-mask test structures.

III. Sheet Resistance Measurements

The Anti-Reflective (AR) coating of chromium oxide on the mask presents a challenge when electrically probing the devices [13]. Initial attempts to use a standard 2 × 4 probe card designed to probe aluminium pads were unable to make reliable electrical contact because the AR coating was too hard for the probe tips to penetrate. However, it was found that steerable probes on a manual probe station were able to contact the chromium. It should be noted that considerable force was required to make contact but no scratching of the pads was observed. Sheet resistance measurements were made on the Greek cross section of one of the isolated binary 1.5μm structures. The measurements were very noisy partly because the potentials were being measured using Source Monitor Units (SMUs) which did not have a high enough resolution for low voltages. The repeatability was significantly improved by using higher currents as can be seen in figure 4.

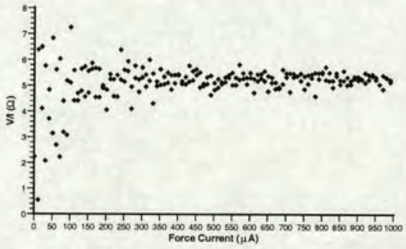


Fig. 4. Results of Kelvin measurements made on a chrome Greek cross structure as the force current was swept from 1μA to 1mA.

One interesting result was that although the repeatability at low currents was quite poor, a large number of measurements at a set force current typically resulted in almost the same mean value. Sets of 200 measurements were made over a short space of time at five force currents ranging from 10μA to 1mA. The mean value of V/I and the standard deviation calculated for each current setting is plotted in figure 5.

The results indicate that although the repeatability of the measurement improves with higher force currents

Figure B.39: *Reprint of paper presented at ICMTS 2002, page 2.*

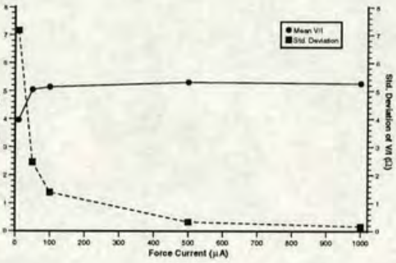


Fig. 5. Mean values and standard deviation of V/I versus force current for a chrome Greek cross structure.

these high currents do not appear to lead to joule heating and a change in resistance. As the repeatability of the measurement is almost the same at 500μA and 1mA it was decided that the lower current should be used for any further measurements as a precaution against damaging the structure under test.

The Greek cross part of the test structure was measured 200 times at four different orientations with a force current of 500μA and the results are presented in table I.

TABLE I

RESULTS OF KELVIN MEASUREMENTS MADE ON A GREEK CROSS TEST STRUCTURE WITH A FORCE CURRENT OF 500μA.

Orientation	Mean V/I (Ω)	$\sigma_{(V/I)}$ (Ω)	R_s ($\Omega/\Box$)
+0°	5.30249	1.078	24.0328
−0°	5.36345	0.102	24.3091
+90°	5.23089	1.061	23.7083
−90°	5.40126	0.108	24.4804
Average	5.3245	-	24.1326

The measured sheet resistance of $24.13\Omega/\Box$ is similar to a reported value of $19.4\Omega/\Box$ for chrome without an AR coating [4]. The measurements in table I show a factor of ten difference between the standard deviations measured with forward and reverse currents. The reason for the difference in variability is not clear but it may be related to probe contact problems. However, it does seem that contact resistance significantly affects the measurement as the values of mean V/I obtained are lower for the orientations with a larger standard deviation.

The chromium oxide coating was removed by a very short etch in an aqueous solution of ceric ammonium nitrate and acetic acid. This meant that a test system using a probe card and semi-automatic probe station could then be used. This system uses a voltmeter with a higher resolution which providing more repeatable and precise measurements. However, isolated 1.5μm structures from one of the binary and one of the phase shifted layouts were tested first using the manual probe station to obtain further information about the effect of the measurement current on the results. Figure 6 shows the mean sheet resistance plotted against the force current while figure 7 shows the standard deviation.

There are a number of conclusions that can be drawn

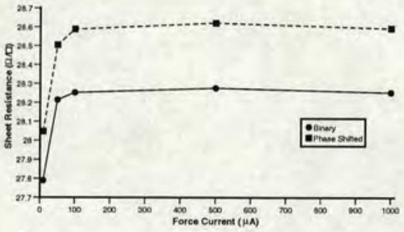


Fig. 6. Mean values of R_s against force current for chrome Greek cross structures.

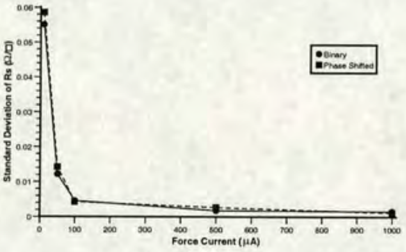


Fig. 7. Standard deviation of R_s against force current for chrome Greek cross structures.

from these results. Firstly the shapes of the curves are very similar to those in figure 5 indicating that a force current of 500μA could again be used to obtain repeatable results. However, the values of standard deviation are significantly lower than the previous results which suggests that most of the variability of the measurements made on the unetched structures was probably due to noise introduced by poor probe contacts. Secondly there is an offset of $0.344\Omega/\Box$ (roughly 1.2%) between the average sheet resistances from the phase shifted and binary structures when measured with a current of 500μA. This may have been due to variation of the sheet resistance across the mask plate. The sheet resistances measured after the chromium oxide was removed were typically $4\Omega/\Box$ higher than before which indicates there was some overetching of the chrome features.

Next, one complete set of structures (see figure 3) from the binary section and one from the phase shifted region were measured using the higher resolution system and the semi-automatic probe station. The sheet resistance measurements have been averaged together for each feature size (figure 8) and the standard deviation calculated (figure 9) to give some measure of the variation with pitch.

From figure 8 it can be seen that sheet resistance increases monotonically for designed feature sizes above 0.7μm. Similarly the variation of the sheet resistance decreases as the linewidth increases. The most interesting results are observed for the narrow, phase shifted, L-type structures. The mean sheet resistance increases as the feature size decreases as does the variation of R_s with

Figure B.40: *Reprint of paper presented at ICMTS 2002, page 3.*

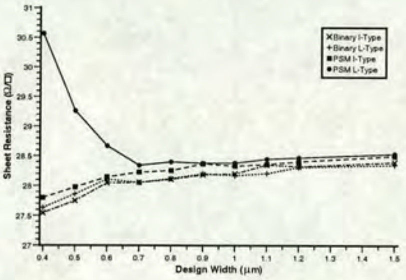


Fig. 8. Mean values of R_s against feature size for chrome Greek cross structures.

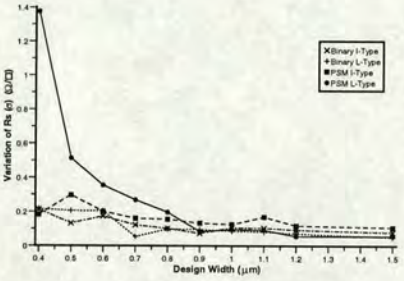


Fig. 9. Standard deviation of R_s against feature size for chrome Greek cross structures.

pitch. It is only on the L-type structures (see figure 1) that the phase shifting elements can significantly affect the extracted value of sheet resistance.

Figure 10 shows the average asymmetry factor F_A [10] plotted against the feature size. Provided F_A is less than 0.1, the correction factor f is insignificant and the sheet resistance can be calculated using equation (1). It is clear from figure 10 that there is no significant asymmetry in the binary and I-type phase shifted structures except for those with the smallest features. Even then the largest correction required to the value of R_S is only about 0.3%. The phase shifted L-type structures, however, show significant and systematic asymmetry. The maximum value of F_A is observed for the 0.4μm crosses and would require a 2.2% correction to the extracted sheet resistance. However, this effect cannot account for the high values of R_S measured with these structures. It is possible that the effect of etching the phase shifting elements on the geometry of these Greek crosses leads to current crowding and joule heating during measurement.

IV. ELECTRICAL LINEWIDTH MEASUREMENTS

Initial measurements of the resistance of a nominal 1.5μm wide track were performed using the manual probing system before the oxide was removed and the results are presented in table II.

It should be noticed that the standard deviations ob-

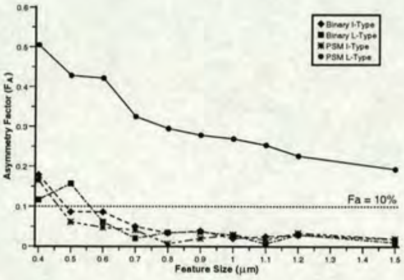


Fig. 10. Average Greek cross asymmetry factor F_A versus feature size for chrome structures.

TABLE II

RESULTS OF KELVIN MEASUREMENTS MADE ON A BRIDGE LINEWIDTH STRUCTURE WITH A FORCE CURRENT OF 500μA.

Force Direction	Mean Resistance (Ω)	σ_R (Ω)
Forward	6730.22	2.4537
Reverse	6729.34	2.2709
Average	6729.78	-

served when making the bridge measurements are proportionately much smaller ($\approx 0.035\%$) than for the R_s measurements where σ was almost 20% for some measurements. This is probably because the voltages being measured are much higher for the bridge structures than for the crosses. Taking the average bridge resistance from table II and using it in equation (2) along with the average sheet resistance from table I gives an electrical linewidth (W_L) of 1.434μ m. The nominal value of linewidth was 1.5μm so the electrical width is about 4.4% less than this. If the individual values of R_s from each measurement orientation are used to calculate linewidth figures using the average bridge resistance it can be seen that the measurements which showed the best repeatability provide values of ECD closest to the nominal linewidth. The linewidth results and the standard deviations of the sheet resistances can be seen in table III.

TABLE III

SHEET RESISTANCE, STANDARD DEVIATION OF R_s AND LINEWIDTHS FOR EACH GREEK CROSS MEASUREMENT ORIENTATION.

Orientation	Mean R_s ($\Omega/\Box$)	σ_{R_s} ($\Omega/\Box$)	W_L (μm)
+0°	24.0328	4.886	1.428
−0°	24.3091	0.462	1.445
+90°	23.7083	4.809	1.409
−90°	24.4804	0.489	1.455

There are two main sources for variability in electrical CD measurements, firstly the measurement of the resistance of the bridge itself and secondly the value of sheet resistance used in the linewidth calculation. The first can be minimised through the choice of measurement current and, as is clear from the results in table II, makes up a very small proportion of the measured resistance. The sheet resistance variability is more of a problem. The results presented in figures 8 and 9 indicate that the value

Figure B.41: *Reprint of paper presented at ICMTS 2002, page 4.*

of R_S extracted from the structures and the variability of the measurement with pitch is a function of feature size. This is particularly clear for the measurements made on phase shifted L-type crosses. For this reason it was decided that the average of the sheet resistances extracted from the 1.5μm structures should be used. The values are $28.5\Omega/\Box$ for the phase shifted structures and $28.4\Omega/\Box$ for the binary structures.

CD-SEM measurement of these structures has also been performed and figure 11 shows the electrical and SEM measurement results for the L-type, isolated structures.

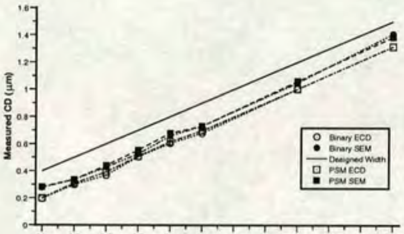


Fig. 11. Measured linewidth versus the designed CD for isolated bridge structures.

It is clear from these results that there is an offset between the electrical and SEM measurements. This is to expected as systematic differences of a similar size are common between electrical linewidth measurements and other CD metrology techniques [14], [15]. Plotting the data in this way makes it difficult to visualise the offset because of the large range of widths. Figure 12 shows the results of subtracting each of the measured widths from the drawn width.

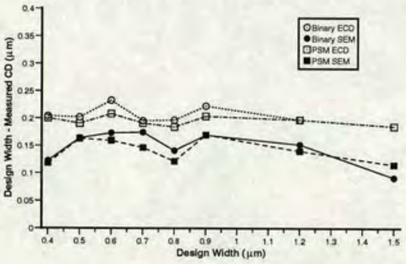


Fig. 12. Designed linewidth minus the measured CD plotted against the designed width for isolated bridge structures.

This identifies the offset between the electrical and SEM measurements which varies from a maximum of ~0.08μm down to a minimum of ~0.02μm. However, there is no obvious trend with feature size. The same operation has been performed with the CD measurements of the dense linewidth structures with a mark to space ratio of 1:2 and the results are presented in figure 13.

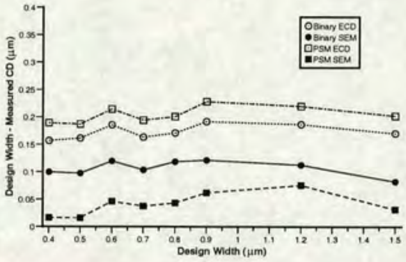


Fig. 13. Designed linewidth minus the measured CD plotted against the designed width for 1:2 dense bridge structures.

The most important point to notice here is the offset between the electrical and SEM results for the phase shifted structure which is about twice that observed for the binary structures. For CD-SEM linewidth measurement the threshold selected to define the edge of the feature has a systematic effect on the extracted width. It is possible that the presence of the alternating phase shifting elements affect the SEM image so that the tracks appear significantly wider than expected. Unfortunately no SEM images are available of the phase shifted structures but figure 14 shows a typical image obtained from the binary section of the mask. Charging of the mask in the SEM chamber meant that the images obtained had poor contrast which is undesirable when attempting to make accurate CD measurements.

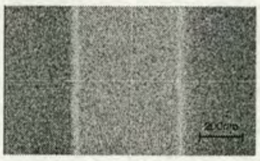


Fig. 14. SEM image of a nominally 0.7μm wide binary feature.

The results presented in figures 12 and 13 suggest that the difference between the measured and designed width is not a function of the linewidth. However, if the dense structure results are plotted as a function of the mark to space ratio for a certain linewidth it becomes clear that there is a significant proximity effect on the width of the bridge resistor. Figure 15 shows the electrical and SEM CD results for dense 0.4μm structures.

The difference between the designed and measured widths increases as the mark to space ratio becomes smaller. This means that the measured width of the line decreases as the spacing between it and the surrounding dummy tracks increases.

Figure B.42: *Reprint of paper presented at ICMTS 2002, page 5.*

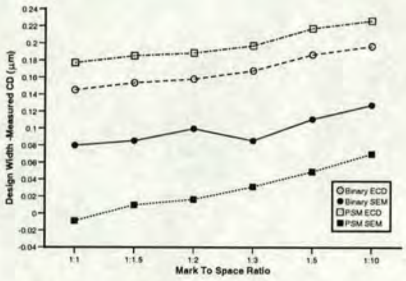


Fig. 15. Designed linewidth minus the measured CD plotted against mark to space ratio for $0.4\mu m$ dense bridge structures.

V. CONCLUSIONS

The preliminary measurements indicated that it is possible to probe test structures on chrome masks with anti-reflective coatings. However, suspected probe related problems make the measurements less repeatable than when probing the etched chrome pads.

The measurements made on Greek cross structures show that the variability of the extracted sheet resistance is reduced by increasing the size of the cross, as in reference [16]. Future on-mask test structure layouts should use very large Greek crosses, or possibly box crosses, for R_S extraction rather than following the minimum feature size of the bridge section.

It is clear that the etching of the phase shifting elements has a strong effect on the geometry of the L-type cross structures. This leads to large errors in the very narrow crosses which cannot be removed through the use of the correction factor f. Further work will include the use of an Atomic Force Microscope (AFM) to investigate these structures in an attempt to fully explain these results.

The electrical linewidth measurements show that the tracks are significantly narrower than the designed width and this may be partly due to the etching process used to remove the anti-reflective coating. There is also a systematic offset between binary and phase shifted dense tracks. Finally there is a proximity effect caused by the dummy tracks in the dense structures which makes the closely packed lines wider than those that are more generously spaced.

Differences have been demonstrated between CD-SEM and electrical measurements with the electrical results being more repeatable. As expected there is a systematic offset between the electrical and SEM results obtained from the binary structures. What was unexpected was that the phase shifted lines, which appeared to be electrically narrower than the binary structures, were measured on the CD-SEM system as being significantly wider. This may be due to the phase shifters causing confusion about the position of the line edge.

Future work will include AFM scans of these structures which should help identify the reasons for the differences between the electrical and SEM measurements. The mask will be used to print test structures which will also be measured electrically. These results will be compared with on-mask measurements to obtain information about the mask error factor (MEF).

ACKNOWLEDGEMENTS

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Figure B.43: *Reprint of paper presented at ICMTS 2002, page 6.*

Test Structures for the Electrical Characterisation of Platinum Deposited by Focused Ion Beam

S. Smith, A.J. Walton, S. Bond, A.W.S. Ross, J.T.M Stevenson, A.M. Gundlach

Abstract—

Focused Ion Beam (FIB) systems are commonly used to image, repair and modify integrated circuits by cutting holes in passivation to create vias or to selectively break metal tracks. The ion beam can also be used to deposit a metal, such as platinum, to create new connections. These techniques are very useful tools for debugging designs and testing possible changes to the circuit without the expense of new mask sets or silicon. This paper presents test structures to characterise a FIB platinum deposition process. Sheet resistance test structures have been fabricated using a FIB tool and the results of testing these structures are presented. This data will enable resistors with a known value to be fabricated in addition to conducting straps.

I. INTRODUCTION

A Focused Ion Beam (FIB) system is similar to a Scanning Electron Microscope (SEM) but uses a beam of Ga ions produced by a liquid metal ion source rather than electrons from a field emission source. It can be used to image surfaces in a similar manner to a SEM but the major application is the modification of integrated circuits by "cutting and strapping" [1]. The cutting operation is performed by using the ion beam to physically sputter the sample surface. It is possible to obtain an enhanced etch rate with certain materials by adding iodine to the chamber. This technique can be used to cut through passivation to the required level of metallisation in order to break a track or create a via. A FIB system can also be used to selectively deposit metal on to the surface by ion beam induced deposition. Straps of metal deposited in this way can be used to create new connections between tracks once the FIB has cut vias through the passivation and the interlayer dielectric. This technique can be used to repair or modify an integrated circuit and can significantly reduce the time taken in debugging designs.

Platinum is the most common choice for use in integrated circuit repair and modification because it is inert in air and does not cause contamination of the circuit if deposited directly onto the silicon [2]. In order to deposit a metal using the ion beam an organometallic precursor gas is injected into the vacuum chamber through a needle close to the sample surface. This is adsorbed onto the surface and then decomposes under the ion beam scan to leave the deposited metal. The FIB deposited platinum film can have a high concentration of contaminants such as carbon, which comes from the organometallic precursor. Typical resistivities for this material can range from $70\mu\Omega$-cm to over $1000\mu\Omega$-cm [2] while the bulk resistivity of pure platinum is approximately $10\mu\Omega$-cm [3].

The film quality, thickness and, therefore, the resistance of the material are functions of the ion beam current, the deposition time and the ion beam scan area. The deposition process needs to be characterised for each FIB system so that the basic electrical properties of a platinum strap can be predicted [1]. The typical requirement for a platinum strap is simply to have a low enough resistance to give a good electrical connection. The motivation for this study was to characterise the platinum deposition process so that resistive elements with a known value can be deposited.

II. TEST STRUCTURES

The design of test structures for characterising the platinum deposition process is complicated by the fact that it is only possible to deposit rectangular geometries. To fully characterise the platinum films the sheet resistance must be determined in terms of the deposition process variables. This information can then be used to predict the resistance of platinum tracks. The test chip also needs to include structures which can accurately measure the resistance of a conducting track so that the homogeneous nature and uniformity of the sheet resistance data can be confirmed.

A. Test Structure Design

There are many methods available for measuring the sheet resistance of the deposited platinum. The simplest technique is to deposit a large area of metal and then use a four point probe technique [4]. The problem with this method is the relationship between the deposition rate, the beam current and the scan area. Large areas take a long time to deposit unless the beam current is increased proportionately. The FEI manual for the FIB system recommends a beam current density in the range of $2\text{-}6\text{pA}\mu\text{m}^{-2}$ and a maximum of $2\text{pA}\mu\text{m}^{-2}$ for beam currents above 1nA. Hence, a platinum square with a 50μm side requires a beam current of 5nA compared to the standard beam current of 150pA.

The alternative to the large deposition areas required by a four point probe technique is to use some version of the four terminal van der Pauw [5], [6] sheet resistance structure such as a Greek [7] or a box cross [8] (The method of extracting the sheet resistance is given in references [9] and [10]). However, the fact that the FIB is limited to depositing rectangular geometries prevents the use of standard test structures. For example, a Greek cross requires at least three different deposition

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S. Smith, A.J. Walton, S. Bond, A.W.S. Ross, J.T.M Stevenson, A.M. Gundlach are with the Department of Electronics and Electrical Engineering, Scottish Microelectronics Centre, The University of Edinburgh, Kings Buildings, Edinburgh, EH9 3JF, U.K. (e-mail: Stewart.Smith@ee.ed.ac.uk)

Figure B.44: *Reprint of paper presented at ICMTS 2002, page 1.*

regions connected together and this is completely impractical. The standard structures need to be adapted to meet the capabilities of the FIB system. The approach selected involved the design and fabrication of a set of aluminium features which form the basis of standard structures with a rectangle of FIB deposited platinum completing the test structure. For example, figure 1 shows the aluminium layout for a box type test structure.

Fig. 1. Aluminium layout for a box cross sheet resistor fabricated in FIB deposited platinum.

The structure is completed by depositing a square area of platinum at the centre of the aluminium voltage taps to form a box cross. The full design includes a number of these structures with different spacings between the voltage taps to allow a number of box cross sizes to be fabricated. The ideal four terminal van der Pauw sheet resistance structure is a homogeneous conducting film with an arbitrary shape and four point contacts on the boundary [5]. Real structures like Greek and box crosses can have finite contacts, and still provide accurate values of R_s, if they follow certain design rules [8], [11]. In the platinum box cross structures the contacts between the aluminium taps and the box can make up a significant proportion of the box area. This can be seen in figure 2 which shows the geometry used for the initial set of test structures which were fabricated.

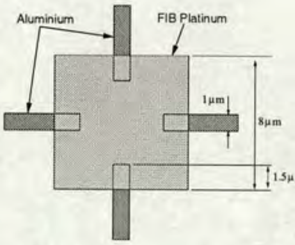

Fig. 2. Schematic plan view of the centre of an 8 × 8μm box cross structure.

It was decided that simulations of such structures should be performed to investigate any relationship between the size of the box and the accuracy of the measurements. In these simulations the width of the voltage taps was set to 1μm. Three sets of simulations were performed with different overlaps (L_t = 1.5, 0.5 and 0.25μm) between the box and the aluminium fingers. The dimensions of the box were varied from 5 × 5μm up to 25 × 25μm and the sheet resistance of the box material was set to 1Ω/□. All of the simulations were performed in two dimensions using the Raphael package from Avant!. The simulation results can be seen in figure 3.

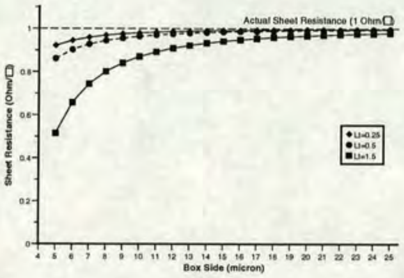

Fig. 3. Sheet resistance versus box dimensions for simulated platinum box cross structures with three different voltage tap overlaps (L_t).

These show that the extracted sheet resistance approaches the actual value as the size of the box increases. The error observed for a box structure with a 5μm dimension is almost 50% for a tap overlap of 1.5μm. However, figure 3 indicates that this error can be significantly reduced by making the tap overlap smaller. Figure 3 also suggests that large box crosses should be used to increase the accuracy. The dilemma is that large deposition areas either require high beam currents or a long deposition time. The smaller structures also have areas closer to the dimensions of normal platinum straps. It was for this reason and also to ensure good contacts that the first set of box cross structures fabricated had the dimensions detailed in figure 2.

Asymmetries in van der Pauw structures can lead to errors in the extraction of sheet resistance. This would be the case if there is misalignment between the aluminium features and the platinum box. In order to investigate this a second set of simulations were performed which examined the effects of box misalignment. Box cross structures with sides measuring 5, 10, 20 and 25μm were simulated in two dimensions with tap overlaps of 1μm and misalignments ranging from +0.9 to −0.9μm in x and y. The box sheet resistance was again set to 1Ω/□. Table I shows the results of the simulations with no misalignment and the results from structures with the maximum misalignment where $X_{offset} = Y_{offset} = \pm 0.9\mu m$. The table also shows the percentage difference between the sheet resistances. The results show that the effect of misalignment is dependent on the size of the box cross with the smallest errors in R_s observed for the largest boxes.

In addition to the sheet resistance measurement structures, the test chip also includes aluminium features which can be used to create a four terminal bridge resistance

Figure B.45: *Reprint of paper presented at ICMTS 2002, page 2.*

TABLE I

RESULTS OF SIMULATING THE EFFECTS OF MISALIGNMENT ON DIFFERENT SIZES OF BOX CROSS STRUCTURE.

Box Size (μm)	$X_{offset} = 0\mu$m $Y_{offset} = 0\mu$m R_s ($\Omega/\Box$)	$X_{offset} = 0.9\mu$m $Y_{offset} = 0.9\mu$m R_s ($\Omega/\Box$)	Difference (%)
5	0.7137	0.7822	8.757
10	0.9243	0.9334	0.97
20	0.9811	0.9795	0.23
25	0.9874	0.9863	0.11

structure. The aluminium layout for one such structure can be seen in figure 4.

Fig. 4. Aluminium layout for a FIB platinum bridge resistance test structure.

In this case the structure is completed by the deposition of a narrow strap of platinum between the aluminium taps to form the bridge resistor (see figure 10). The four terminal bridge resistor is a Kelvin test structure which can be used to measure the resistance of a conducting track. Its main application is as part of a linewidth measurement test structure [12]. The full test chip layout contains a number of cross type and bridge type structures with a range of possible platinum deposition sizes. It also includes structures which can be used to measure the contact resistance between the aluminium and the platinum but these have yet to be evaluated.

B. *Test Structure Fabrication*

The platinum structure fabrication process begins with the aluminium test layout which is patterned into 500nm thick Al deposited on a silicon wafer. The wafer has a thin layer of thermally grown oxide to isolate the substrate from the aluminium structures. Once the desired deposition area is identified then the tips of the aluminium tracks which will connect the platinum structure to the probe pads must be cleaned. Aluminium oxide forms on any bare Al surface as soon as it comes into contact with air and must be removed in order to make a good contact. In the samples that were used initially, some sort of residue, possibly photoresist, was also observed on the surface of the narrow voltage taps and was removed. The cleaning was performed by focusing the FIB closely on the end of the tap and imaging it until the residue appeared to have been sputtered away. When the first platinum depositions were performed the oxide on the back side of the wafer led to charging of the surface causing the beam scan to shift after alignment. The result of this is that platinum was not deposited in the desired area. This was overcome by removing the oxide with a short wet etch in buffered HF solution.

As previously mentioned the three main deposition process variables that affect the resistance of a platinum feature are the deposition area, the deposition time and the beam current. The deposition rate and the quality of the platinum film depend upon the beam current and the area that is being deposited. All of the structures fabricated so far for this study use a nominal ion beam current of 150pA as this is the same current used for strap deposition in normal operation. However, wear on the aperture in the FIB column gives an actual beam current typically between 190 and 200pA. If the beam scan area is also kept constant then the thickness of the film, and therefore its sheet resistance, should be solely controlled by the deposition time. As an initial experiment a set of twelve box cross structures were fabricated where the deposition area was $64\mu m^2$ ($8 \times 8\mu m$) as illustrated in figure 2. A very conservative overlap of the aluminium fingers was used ($1.5\mu m$) to ensure good contact. It should be possible to reduce this to $0.5\mu m$ or less for future depositions which will cause a reduction in the error due to the non-ideal geometry.

The FIB system calculates a thickness for the deposited material based on the beam current, the deposition time and the area. Using this as a guideline the deposition times were set to give structures with nominal thicknesses from 500nm down to 60nm. The actual deposition times varied from about 330s for the thickest film down to 40s.

III. INITIAL BOX CROSS RESULTS

The $8 \times 8\mu m$ box cross structures were tested electrically and sheet resistance values extracted. Looking back to the simulation results in figure 3 reveals that an error of about 20% should be expected in the sheet resistance measured. The results of the R_s measurements are presented in figure 5. The graph also includes the result of adding 20% to each of the values and reciprocal functions which were fitted to each set of data.

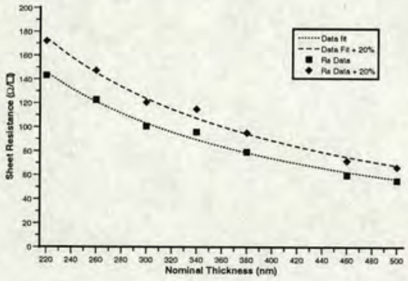

Fig. 5. Sheet resistance versus nominal thickness for $8 \times 8\mu m$ box cross test structures.

The results show that the sheet resistance for these structures is inversely proportional to the nominal thick-

Figure B.46: *Reprint of paper presented at ICMTS 2002, page 3.*

ness or deposition time. As the deposition area and beam current were the same for each structure then the deposition rate and material resistivity ρ should also be constant. Therefore, the thickness t will increase with time at a constant rate and as $R_s = \frac{\rho}{t}$ then there should be an inverse relationship between the sheet resistance and the deposition time.

One of the box cross structures has been measured using an Atomic Force Microscope (AFM) and the resulting image can be seen in figure 6.

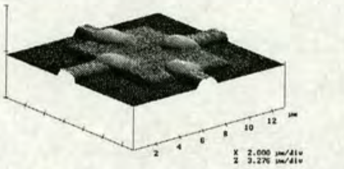

Fig. 6. 13 × 13μm AFM scan of a FIB platinum box cross structure.

A sectional analysis of the scan showed that the platinum film thickness was between 320 and 335nm but the nominal thickness calculated by the FIB system for this structure was only 220nm. For this reason, the nominal thickness will be ignored and the deposition time used instead for the next set of structures.

IV. Diagonal Box Cross Test Structures

As a consequence of the large errors associated with the orthogonal box cross structure of figure 2, further simulations were performed using layouts where the box section is rotated through 45° as shown in figure 7.

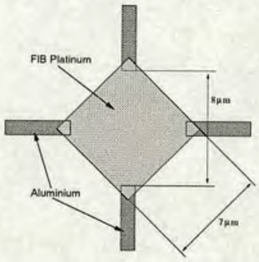

Fig. 7. Schematic plan view of the centre of a diagonal 7 × 7μm box cross structure.

Structures where the distance between the taps (8μm in figure 7) varies from 5μm to 25μm have been simulated, and the results are presented in figure 8. The sheet resistance of the box section of the structure is set to 1Ω/□ as in the previous simulations.

It is clear that a much more accurate value of sheet resistance can be extracted from the diagonal box cross structures. The error in R_S is less than 1% even with the smallest structure. The test chip includes a cross layout where the aluminium taps are 8μm apart. A diagonal box of FIB deposited platinum with sides of 7μm placed over these taps should give a sheet resistance error of about 0.1% according to the simulation results. A number of these structures have been fabricated with a beam current of about 200pA and deposition times varying from 70s to 250s. The results of extracting sheet resistance from these structures are presented in figure 9.

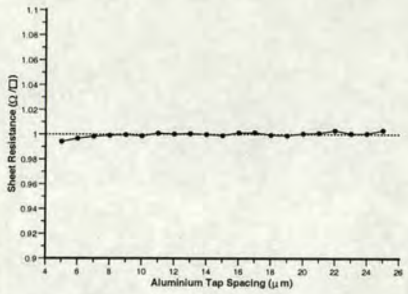

Fig. 8. Simulated sheet resistance versus voltage tap spacing for diagonal box cross test structures.

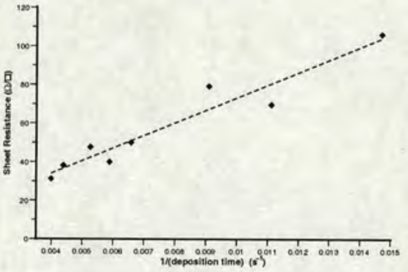

Fig. 9. Sheet resistance versus the inverse of deposition time for 7 × 7μm diagonal box cross test structures. The dotted line is a linear fit to the test data.

The data indicates that the sheet resistance is proportional to the reciprocal of the deposition time as expected. The linear fit to the sheet resistance data can now be used to estimate the resistance of platinum track fabricated in the FIB using the same process parameters.

V. Bridge Test Structures

A small number of bridge resistor structures have been fabricated using the aluminium layout shown in figure 4. Figure 10 shows one of these structures.

The beam current used in the fabrication of these structures was the same as that used for the initial box cross structures but the dimensions of the track mean that the

Figure B.47: *Reprint of paper presented at ICMTS 2002, page 4.*

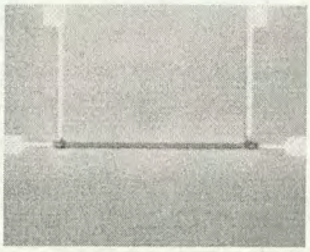

Fig. 10. Photomicrograph of a hybrid aluminium/platinum four terminal bridge resistor test structure

areas are different. This indicates that sheet resistances will not be the same as those measured before with structures with the same thickness. This problem could be rectified by making the line area fit the area of the box crosses measured earlier. In this case, for example, the distance between the taps is only $50\mu m$ and the width of the platinum strap is $1\mu m$. If the length of the strap is extended to $64\mu m$ the deposition areas should be the same. In that case the sheet resistance data from the box cross could be used along with the bridge resistance to extract the electrical linewidth of the platinum strap [12].

The results of measuring these bridge structures can be seen in figure 11.

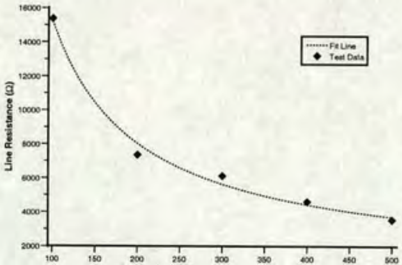

Fig. 11. Resistance against nominal thickness for four terminal bridge resistor structures

Again the results show that the resistance is inversely proportional to the material thickness as was expected. However, the bridge structures were not quite ideal because they did not allow true Kelvin measurements. The reason for this was that the current forcing terminals were connected to the voltage taps, hence the resistance measured may include some of the contact resistance between the platinum and the aluminium. In order to correct this the FIB system was used in ion milling mode to remove some of the aluminium and disconnect the force terminals from the voltage taps. Figure 12 shows the result of cutting through the aluminium track.

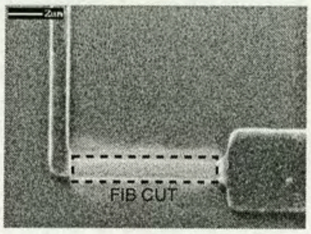

Fig. 12. FIB image of the alteration made to the aluminium test structure to allow Kelvin measurements.

The next step is to fabricate bridge resistors on these modified structures. The deposition area should be the same as the diagonally orientated box crosses in section IV which is $49\mu m^2$. The spacing of the voltage taps is $51\mu m$ which meant that the platinum deposition area had to be longer and so $0.5 \times 98\mu m$ was chosen. A set of test structures were fabricated with deposition times ranging from 60 to 240 seconds. The results of electrical measurements made on these resistors are presented in figure 13.

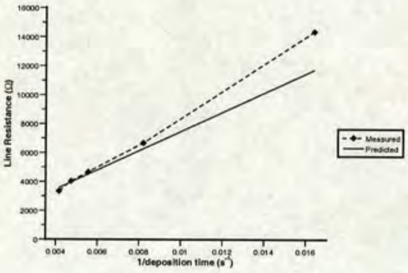

Fig. 13. Resistance versus the inverse of Pt deposition time for four terminal bridge resistor structures including the predicted line resistance.

Figure 13 also shows the predicted resistance of the track derived from the linear fit to the sheet resistance data in figure 9. The measurement results are all within 10% of the predicted value except for those taken from the track made with the shortest deposition time. The thickness of the platinum tracks was measured using a Dektak surface profiler and the results are presented in figure 14.

This thickness data can then be used to calculate the resistivity of the conducting material, assuming that the linewidth is $0.5\mu m$. These figures are plotted against the deposition time in figure 15

The resistivity should be a constant if the process parameters of area and beam current are constant. The results in figure 15 suggest that the resistivity is independent of the deposition time with $\rho_{mean} = 1630\mu\Omega$-cm and $\sigma_\rho = 123\mu\Omega$-cm.

Figure B.48: *Reprint of paper presented at ICMTS 2002, page 5.*

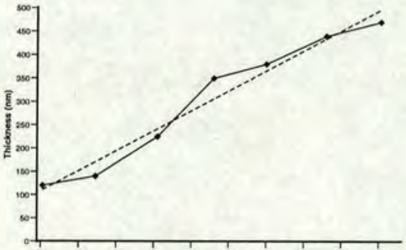

Fig. 14. Thickness of deposited platinum against deposition time. The dotted line is a linear fit to the data.

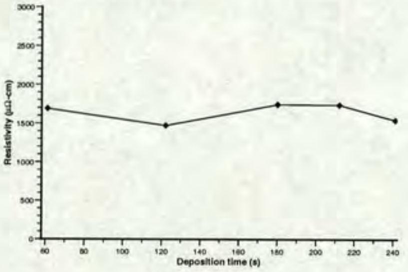

Fig. 15. Resistivity of deposited platinum against deposition time.

VI. CONCLUSIONS

A methodology has been presented for the measurement of the sheet resistance of platinum films created by focused ion beam deposition. The geometry of the test structures can lead to errors in the extracted value of R_s and these have been quantified by simulations which showed that the errors reduce as the platinum box size increases. Further simulations which investigated the effects of misalignment on the measurement accuracy have also shown that the effects of alignment errors are minimised with larger structures.

An initial set of box cross test structures were fabricated with a platinum deposition area of $64\mu\text{m}^2$. The results indicated that the sheet resistance was, as expected, inversely proportional to the deposition time, with the deposition rate and material resistivity remaining constant for structures with the same area deposited with the same beam current. Simulations of box cross structures fabricated with the wafer rotated in the FIB chamber by 45° indicate that accurate values of R_S can be extracted even when the dimensions of the box are much smaller than required with the original, orthogonal structures. Electrical measurements of these diagonal box crosses again indicated that sheet resistance is inversely proportional to deposition time and the results were used to estimate the resistance of platinum tracks deposited with the same process parameters and deposition area.

A set of platinum bridge resistor structures have been fabricated. The results of electrical measurements have shown that it is possible to predict with some accuracy the resistance of the track from the sheet resistance data obtained from box cross structures. Dektak measurements have confirmed that the thickness of the deposited platinum is, as expected, directly proportional to the deposition time.

Further work will include the fabrication of a new mask for the aluminium layouts which will be designed taking into account the results presented in this paper. For example the layouts for the box cross structures will not require the wafer to be rotated through 45 degrees in the FIB chamber while the bridge structures will be designed for Kelvin resistance measurements.

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Figure B.49: *Reprint of paper presented at ICMTS 2002, page 6.*

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Evaluation of Sheet Resistance and Electrical Linewidth Measurement Techniques for Copper Damascene Interconnect

Stewart Smith, Anthony J. Walton, *Member, IEEE*, Alan W. S. Ross, Georg K. H. Bodammer, and J. T. M. Stevenson

***Abstract*—The effects of the barrier layer and dishing in copper interconnect lead to extra difficulties in measuring sheet resistance (R_S) and linewidth when compared with equivalent measurements on nondamascene tracks. This paper examines these issues and presents the results of simulations that quantify the effects of diffusion barrier layers and dishing on the extraction of R_S from cross type test structures and the effect this has on linewidth measurement.**

***Index Terms*—Chemical mechanical polishing, CMP, copper, critical dimension, Cu, damascene, electrical CD metrology, interconnect, metrology, sheet resistance, simulation, test structures, van der Pauw method.**

I. INTRODUCTION

ADVANCED interconnect technologies are an essential part of the roadmap for improving the performance of integrated circuits [1]. As a result, copper is set to rapidly replace aluminum as the first choice for IC interconnect. Copper has a resistivity of about 1.7 $\mu\Omega$·cm compared to 2.7 $\mu\Omega$·cm for Al.[1] The lower resistivity of copper, when combined with the introduction of low-k dielectrics, reduces RC time delays and power consumption [3]. Unlike aluminum, copper cannot be easily patterned using a subtractive process such as reactive ion etching and so a damascene metal process with CMP is used instead. A disadvantage of copper is that it will diffuse quickly into silicon and SiO_2 and can damage devices if it reaches the substrate. Consequently, a protective barrier layer, consisting of a metal such as tantalum, must be included. A typical copper interconnect process is illustrated in Fig. 1, [4], [5].

II. COPPER DAMASCENE AND TEST STRUCTURES

Resistive electrical test structures used to measure the linewidth of conducting tracks assume a homogeneous layer of conducting material. This is not the case for copper damascene interconnect because of the requirement to use barrier layers. Fig. 2 shows a schematic cross section through two copper tracks with barrier layers and it is clear that as the width of the copper track decreases the percentage contribution of the barrier layer to the sheet resistance increases. For example, a tantalum diffusion barrier has a higher sheet resistance than copper ($\rho_{\mathrm{Ta}} \approx 13$ $\mu\Omega$·cm) and a simple calculation based on the cross-sectional area can be used to calculate the resistance of a track [6], [7].

Another effect of the damascene process that can affect the resistance of a copper track is dishing. This occurs because the copper is softer than the surrounding dielectric and is removed more quickly. The CMP polishing pad deforms into the recess and removes more copper from the track, making it thinner in the center as shown in Fig. 3.

The amount of copper that is removed is a function of the track width [8], [9]. Fig. 4 shows atomic force microscope (AFM) measurements we have made on copper damascene lines and demonstrates the increase in dishing as the trench becomes wider.

Any reduction in the cross-sectional area of a track will increase its resistance. In order to electrically measure the linewidth of a conducting track, the *effective* sheet resistance of the material must first be determined. This parameter is normally measured using either a Greek or box cross test structure like those shown in Fig. 5, [10], [11].

Fig. 6 shows an AFM scan of a copper Greek cross. In order to measure sheet resistance from such a structure, a known current I is forced between two adjacent terminals and the resulting voltage V is measured across the other two contacts. The sheet resistance R_S can then be calculated using the van der Pauw formula [12]

$$R_S = \left\{\frac{V}{I}\right\} \frac{\pi}{\ln(2)}. \quad (1)$$

The full extraction method, which takes into account possible asymmetries in the cross structure, is described in [11].

These test structures are commonly used to measure R_S because no dimensional information is required. However, both the Greek and box crosses will be affected by the diffusion barrier layer and the pattern-dependent effects of dishing. Any error in the value of R_S extracted using a cross sheet resistor will directly translate into an error in the value of linewidth calculated using that sheet resistance. Reference [6] discusses many of the issues associated with characterizing copper interconnect using electrical test structures. The purpose of the work presented in this paper is to quantify some of these effects.

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S. Smith, A. J. Walton, A. W. S. Ross, and J. T. M. Stevenson are with the Department of Electronics and Electrical Engineering, Scottish Microelectronics Centre, The University of Edinburgh, Edinburgh EH9 3JF, U.K. (e-mail: s.smith@ee.ed.ac.uk; a.j.walton@ee.ed.ac.uk; a.w.s.ross@ee.ed.ac.uk; j.t.m.stevenson@ee.ed.ac.uk).

G. K. H. Bodammer is with MicroEmissive Displays Ltd., Scottish Microelectronics Centre, Edinburgh EH9 3JF, U.K. (e-mail: georg.bodammer@microemissive.com).

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[1] All electrical resistivity data used in this paper is taken from [2].

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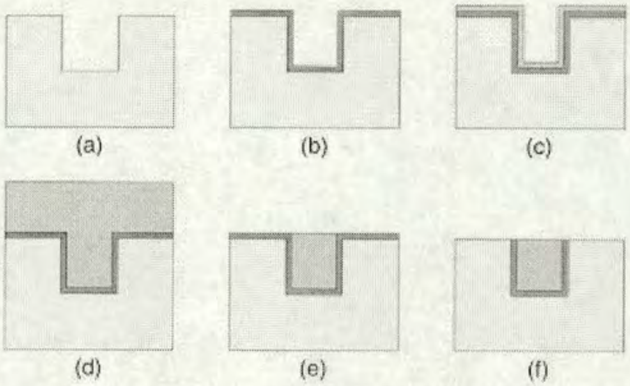

Fig. 1. Typical copper damascene process: (a) Etch tracks in inter-layer dielectric. (b) Deposit barrier layer Ta-PVD. (c) Deposit copper seed layer by PVD/CVD. (d) Copper deposited by electro-plating. (e) First CMP polish—selective toward Cu, stops on barrier layer. (f) Second CMP polish—removes Cu and Ta at same speed, removes barrier layer.

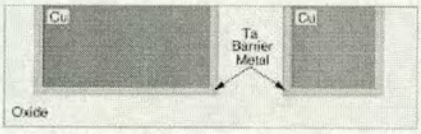

Fig. 2. Cross section of copper damascene tracks of different widths. As the width of the copper line decreases, the relative contribution of the sidewall barriers to the track resistance will increase.

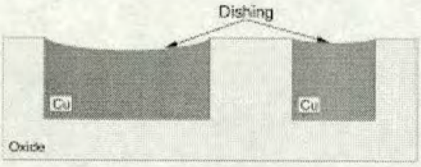

Fig. 3. Schematic cross section through two metal damascene lines which have been dished by the polishing process.

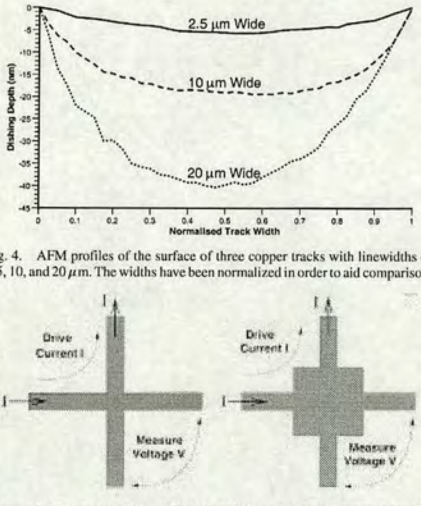

Fig. 4. AFM profiles of the surface of three copper tracks with linewidths of 2.5, 10, and 20 μm. The widths have been normalized in order to aid comparison.

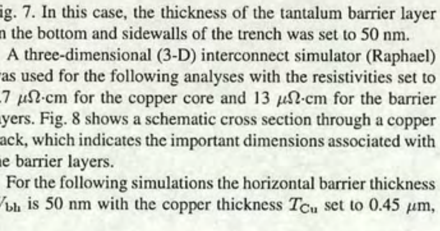

Fig. 5. Schematic plan views of Greek and box cross structures used for R_S extraction.

III. THE EFFECTS OF BARRIER LAYERS AND DISHING ON THE MEASUREMENT OF SHEET RESISTANCE AND ELECTRICAL LINEWIDTH

This section examines each of the damascene process issues in turn and describes the simulations that have been performed to determine their effect on the performance of sheet resistance test structures. This information is then used to investigate how errors in the extraction of sheet resistance affect electrical linewidth measurement.

A. Barrier Layer Effects on R_S Measurement

The first question that needs to be answered is the exact effect that the barrier layer has on the extracted value of R_S. The structure of a Greek cross used to perform this task is shown in Fig. 7. In this case, the thickness of the tantalum barrier layer on the bottom and sidewalls of the trench was set to 50 nm.

A three-dimensional (3-D) interconnect simulator (Raphael) was used for the following analyses with the resistivities set to 1.7 $\mu\Omega$·cm for the copper core and 13 $\mu\Omega$·cm for the barrier layers. Fig. 8 shows a schematic cross section through a copper track, which indicates the important dimensions associated with the barrier layers.

For the following simulations the horizontal barrier thickness $W_{\rm bh}$ is 50 nm with the copper thickness $T_{\rm Cu}$ set to 0.45 μm,

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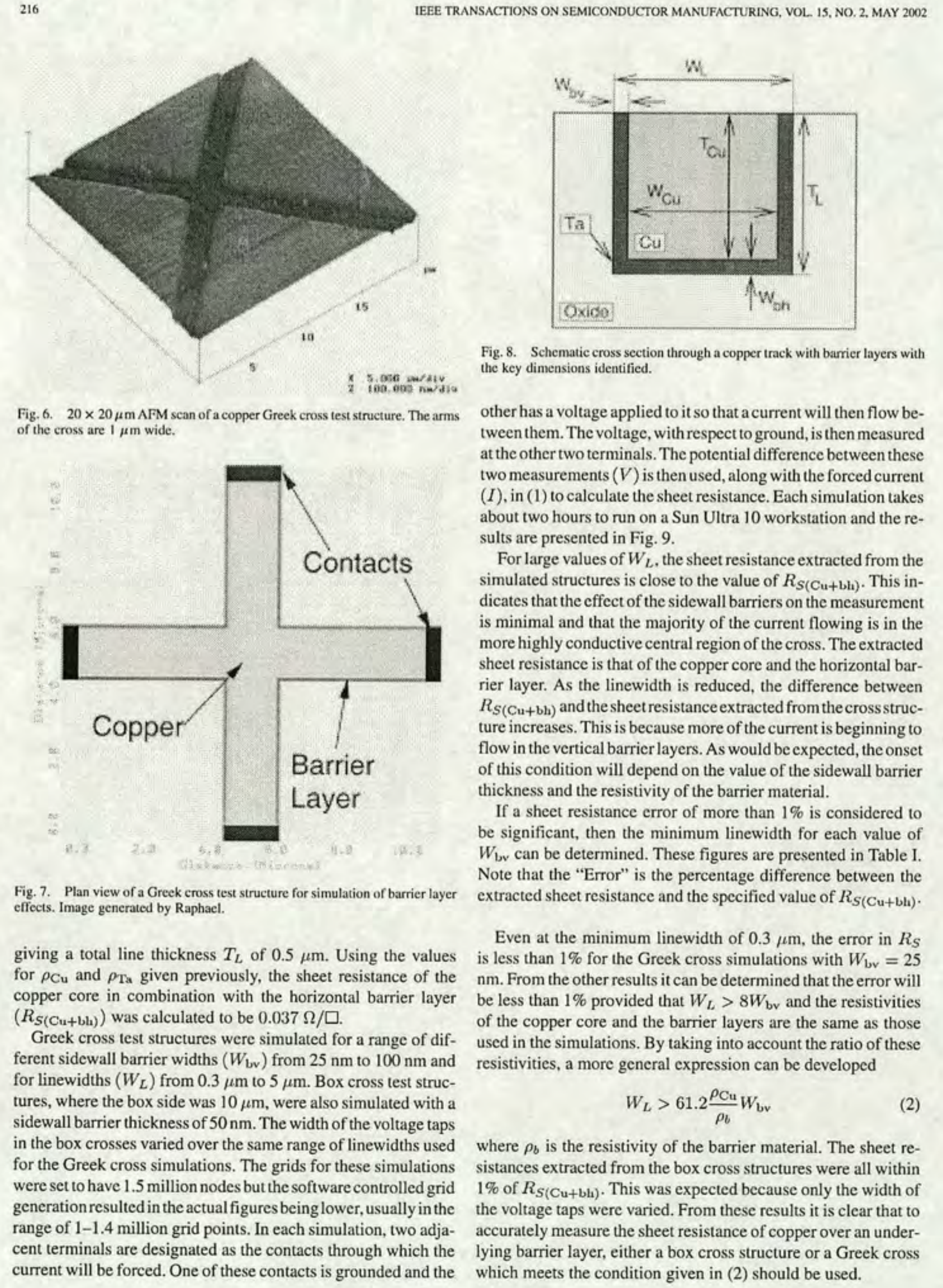

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Fig. 6. 20 × 20 μm AFM scan of a copper Greek cross test structure. The arms of the cross are 1 μm wide.

Fig. 7. Plan view of a Greek cross test structure for simulation of barrier layer effects. Image generated by Raphael.

giving a total line thickness T_L of 0.5 μm. Using the values for ρ_{Cu} and ρ_{Ta} given previously, the sheet resistance of the copper core in combination with the horizontal barrier layer ($R_{S(\mathrm{Cu+bh})}$) was calculated to be 0.037 $\Omega/\square$.

Greek cross test structures were simulated for a range of different sidewall barrier widths (W_{bv}) from 25 nm to 100 nm and for linewidths (W_L) from 0.3 μm to 5 μm. Box cross test structures, where the box side was 10 μm, were also simulated with a sidewall barrier thickness of 50 nm. The width of the voltage taps in the box crosses varied over the same range of linewidths used for the Greek cross simulations. The grids for these simulations were set to have 1.5 million nodes but the software controlled grid generation resulted in the actual figures being lower, usually in the range of 1–1.4 million grid points. In each simulation, two adjacent terminals are designated as the contacts through which the current will be forced. One of these contacts is grounded and the other has a voltage applied to it so that a current will then flow between them. The voltage, with respect to ground, is then measured at the other two terminals. The potential difference between these two measurements (V) is then used, along with the forced current (I), in (1) to calculate the sheet resistance. Each simulation takes about two hours to run on a Sun Ultra 10 workstation and the results are presented in Fig. 9.

Fig. 8. Schematic cross section through a copper track with barrier layers with the key dimensions identified.

For large values of W_L, the sheet resistance extracted from the simulated structures is close to the value of $R_{S(\mathrm{Cu+bh})}$. This indicates that the effect of the sidewall barriers on the measurement is minimal and that the majority of the current flowing is in the more highly conductive central region of the cross. The extracted sheet resistance is that of the copper core and the horizontal barrier layer. As the linewidth is reduced, the difference between $R_{S(\mathrm{Cu+bh})}$ and the sheet resistance extracted from the cross structure increases. This is because more of the current is beginning to flow in the vertical barrier layers. As would be expected, the onset of this condition will depend on the value of the sidewall barrier thickness and the resistivity of the barrier material.

If a sheet resistance error of more than 1% is considered to be significant, then the minimum linewidth for each value of W_{bv} can be determined. These figures are presented in Table I. Note that the "Error" is the percentage difference between the extracted sheet resistance and the specified value of $R_{S(\mathrm{Cu+bh})}$.

Even at the minimum linewidth of 0.3 μm, the error in R_S is less than 1% for the Greek cross simulations with $W_{\mathrm{bv}} = 25$ nm. From the other results it can be determined that the error will be less than 1% provided that $W_L > 8W_{\mathrm{bv}}$ and the resistivities of the copper core and the barrier layers are the same as those used in the simulations. By taking into account the ratio of these resistivities, a more general expression can be developed

$$W_L > 61.2\frac{\rho_{\mathrm{Cu}}}{\rho_b}W_{\mathrm{bv}} \qquad (2)$$

where ρ_b is the resistivity of the barrier material. The sheet resistances extracted from the box cross structures were all within 1% of $R_{S(\mathrm{Cu+bh})}$. This was expected because only the width of the voltage taps were varied. From these results it is clear that to accurately measure the sheet resistance of copper over an underlying barrier layer, either a box cross structure or a Greek cross which meets the condition given in (2) should be used.

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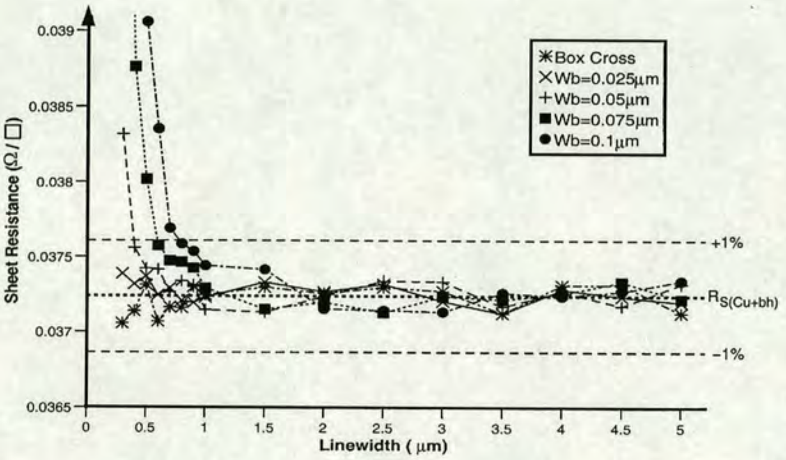

Fig. 9. Extracted sheet resistance versus linewidth for simulated Greek and box cross structures with barrier layers.

TABLE I
MINIMUM VALUE OF CROSS ARM WIDTH W_L WHERE THE ERROR IN THE EXTRACTED SHEET RESISTANCE IS LESS THAN 1% FOR EACH OF THE SIDEWALL BARRIER WIDTHS W_{bv} SIMULATED

W_{bv} (μm)	W_L (μm)	Error
0.025	0.3	0.4%
0.05	0.4	0.87%
0.075	0.6	0.91%
0.1	0.8	0.94%

B. Barrier Layer Effects on Linewidth Measurement

Electrical critical dimension (ECD) or linewidth is usually measured using a bridge type four terminal test structure [13]. This involves the measurement of the resistance R_L of a line of known length L. For the purposes of the work described here, the value of R_L has been calculated by considering the cross section through a damascene copper track as represented in Fig. 8. The length of the line was set to be 100 μm when calculating the resistance. The sheet resistance R_S is found from a cross type test structure and the electrical linewidth W_L calculated using

$$W_L = \frac{R_S L}{R_L}. \tag{3}$$

It was shown in Section III-A that the sheet resistance of copper over a horizontal barrier layer $(R_{S(\mathrm{Cu+bh})})$ can be extracted accurately from a box cross structure or a Greek cross with wide arms. If the metal line being measured has the same sheet resistance then it is possible to extract the linewidth with a similar accuracy. Unfortunately, the presence of sidewall barrier layers means that the resistivity is not uniform across the width of the track. Reference [14] describes a procedure that uses electrical measurements of four copper damascene bridge structures, with different widths, to determine physical parameters such as sidewall barrier width and copper linewidth. The following procedure only requires two structures for an accurate measurement of linewidth from damascene tracks with sidewall barriers. The technique makes it possible to take the resistance of a track with sidewall barriers and calculate an equivalent resistance for a line with the same width but a constant sheet resistance $R_{S(\mathrm{Cu+bh})}$. If this new line resistance is then used in (3), an accurate value of linewidth can be calculated. The effect of this procedure is illustrated in Fig. 10, which shows vertical cross sections through tracks with and without sidewall barriers. The resistances of the tracks are R_L and R_{eq}, respectively.

The resistance difference between the original track and the equivalent uniform line is the resistance of the two sidewall barriers plus the effect of reducing the width of the core of the track by $2W_{\mathrm{bv}}$. It is possible to define a modification factor R_{SW} that facilitates the calculation of R_{eq} by subtracting it from R_L. R_{SW} is the difference between the resistance of the track with sidewall barriers and that of the track with a uniform sheet resistance

$$R_{\mathrm{SW}} = \left(\frac{1}{R_L} - \frac{1}{R_{\mathrm{eq}}}\right)^{-1} \tag{4}$$

and because $R_L > R_{\mathrm{eq}}$, it has a negative value.

The value of R_{SW} will depend upon the sidewall barrier width W_{bv}, which was assumed to be constant in the simulations described in Section III-A. This assumption is reasonable for the barrier widths and feature sizes considered here but does not hold for narrower lines where a shadowing effect can reduce the barrier thickness [6]. Provided that R_{SW} does not vary with linewidth, it is possible to calculate its value using

$$R_{\mathrm{SW}} = \frac{R_{W_1} R_{W_2}}{2R_{W_2} - R_{W_1}} \tag{5}$$

where R_{W_1} and R_{W_2} are the resistances of copper damascene lines with widths W_1 and W_2 where $W_2 = 2W_1$. For example

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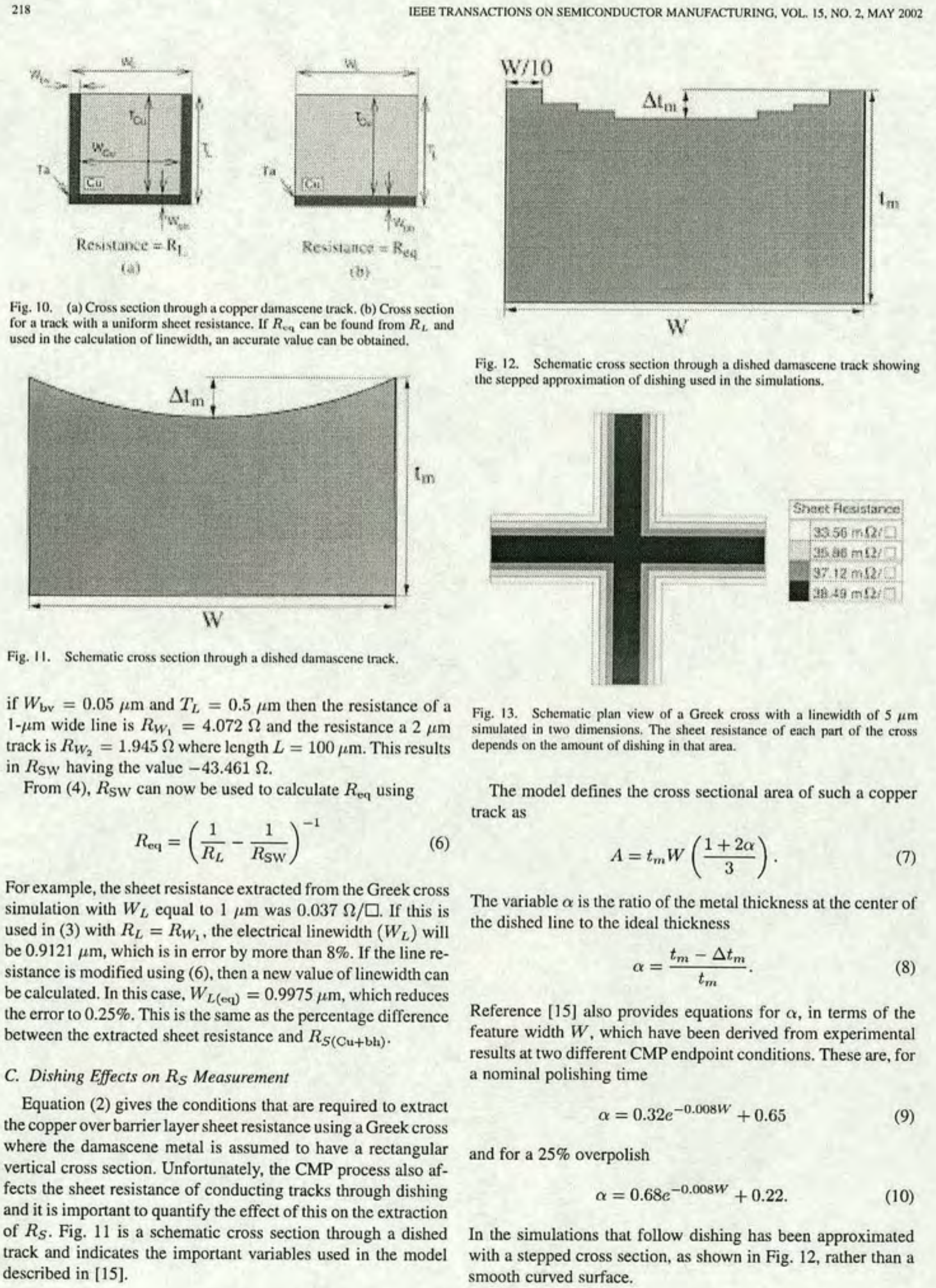

Fig. 10. (a) Cross section through a copper damascene track. (b) Cross section for a track with a uniform sheet resistance. If R_{eq} can be found from R_L and used in the calculation of linewidth, an accurate value can be obtained.

Fig. 11. Schematic cross section through a dished damascene track.

if $W_{bv} = 0.05\ \mu$m and $T_L = 0.5\ \mu$m then the resistance of a 1-μm wide line is $R_{W_1} = 4.072\ \Omega$ and the resistance a 2 μm track is $R_{W_2} = 1.945\ \Omega$ where length $L = 100\ \mu$m. This results in R_{SW} having the value $-43.461\ \Omega$.

From (4), R_{SW} can now be used to calculate R_{eq} using

$$R_{eq} = \left(\frac{1}{R_L} - \frac{1}{R_{SW}}\right)^{-1} \tag{6}$$

For example, the sheet resistance extracted from the Greek cross simulation with W_L equal to 1 μm was 0.037 $\Omega/\square$. If this is used in (3) with $R_L = R_{W_1}$, the electrical linewidth (W_L) will be 0.9121 μm, which is in error by more than 8%. If the line resistance is modified using (6), then a new value of linewidth can be calculated. In this case, $W_{L(eq)} = 0.9975\ \mu$m, which reduces the error to 0.25%. This is the same as the percentage difference between the extracted sheet resistance and $R_{S(\mathrm{Cu+bh})}$.

C. Dishing Effects on R_S Measurement

Equation (2) gives the conditions that are required to extract the copper over barrier layer sheet resistance using a Greek cross where the damascene metal is assumed to have a rectangular vertical cross section. Unfortunately, the CMP process also affects the sheet resistance of conducting tracks through dishing and it is important to quantify the effect of this on the extraction of R_S. Fig. 11 is a schematic cross section through a dished track and indicates the important variables used in the model described in [15].

Fig. 12. Schematic cross section through a dished damascene track showing the stepped approximation of dishing used in the simulations.

Fig. 13. Schematic plan view of a Greek cross with a linewidth of 5 μm simulated in two dimensions. The sheet resistance of each part of the cross depends on the amount of dishing in that area.

The model defines the cross sectional area of such a copper track as

$$A = t_m W \left(\frac{1 + 2\alpha}{3}\right). \tag{7}$$

The variable α is the ratio of the metal thickness at the center of the dished line to the ideal thickness

$$\alpha = \frac{t_m - \Delta t_m}{t_m}. \tag{8}$$

Reference [15] also provides equations for α, in terms of the feature width W, which have been derived from experimental results at two different CMP endpoint conditions. These are, for a nominal polishing time

$$\alpha = 0.32e^{-0.008W} + 0.65 \tag{9}$$

and for a 25% overpolish

$$\alpha = 0.68e^{-0.008W} + 0.22. \tag{10}$$

In the simulations that follow dishing has been approximated with a stepped cross section, as shown in Fig. 12, rather than a smooth curved surface.

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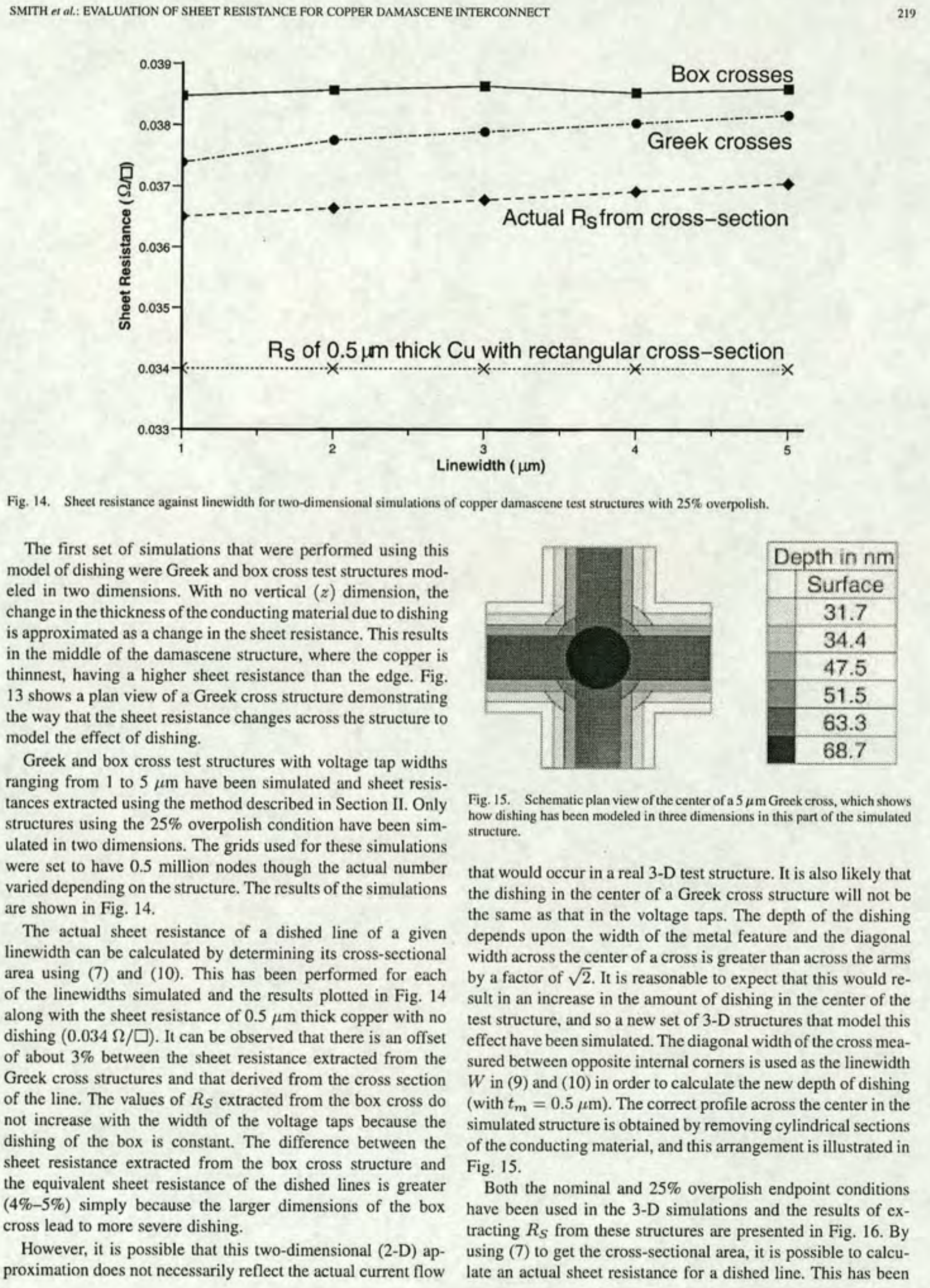

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Fig. 14. Sheet resistance against linewidth for two-dimensional simulations of copper damascene test structures with 25% overpolish.

The first set of simulations that were performed using this model of dishing were Greek and box cross test structures modeled in two dimensions. With no vertical (z) dimension, the change in the thickness of the conducting material due to dishing is approximated as a change in the sheet resistance. This results in the middle of the damascene structure, where the copper is thinnest, having a higher sheet resistance than the edge. Fig. 13 shows a plan view of a Greek cross structure demonstrating the way that the sheet resistance changes across the structure to model the effect of dishing.

Greek and box cross test structures with voltage tap widths ranging from 1 to 5 μm have been simulated and sheet resistances extracted using the method described in Section II. Only structures using the 25% overpolish condition have been simulated in two dimensions. The grids used for these simulations were set to have 0.5 million nodes though the actual number varied depending on the structure. The results of the simulations are shown in Fig. 14.

The actual sheet resistance of a dished line of a given linewidth can be calculated by determining its cross-sectional area using (7) and (10). This has been performed for each of the linewidths simulated and the results plotted in Fig. 14 along with the sheet resistance of 0.5 μm thick copper with no dishing (0.034 $\Omega/\Box$). It can be observed that there is an offset of about 3% between the sheet resistance extracted from the Greek cross structures and that derived from the cross section of the line. The values of R_S extracted from the box cross do not increase with the width of the voltage taps because the dishing of the box is constant. The difference between the sheet resistance extracted from the box cross structure and the equivalent sheet resistance of the dished lines is greater (4%–5%) simply because the larger dimensions of the box cross lead to more severe dishing.

However, it is possible that this two-dimensional (2-D) approximation does not necessarily reflect the actual current flow that would occur in a real 3-D test structure. It is also likely that the dishing in the center of a Greek cross structure will not be the same as that in the voltage taps. The depth of the dishing depends upon the width of the metal feature and the diagonal width across the center of a cross is greater than across the arms by a factor of $\sqrt{2}$. It is reasonable to expect that this would result in an increase in the amount of dishing in the center of the test structure, and so a new set of 3-D structures that model this effect have been simulated. The diagonal width of the cross measured between opposite internal corners is used as the linewidth W in (9) and (10) in order to calculate the new depth of dishing (with $t_m = 0.5\ \mu$m). The correct profile across the center in the simulated structure is obtained by removing cylindrical sections of the conducting material, and this arrangement is illustrated in Fig. 15.

Fig. 15. Schematic plan view of the center of a 5 μm Greek cross, which shows how dishing has been modeled in three dimensions in this part of the simulated structure.

Both the nominal and 25% overpolish endpoint conditions have been used in the 3-D simulations and the results of extracting R_S from these structures are presented in Fig. 16. By using (7) to get the cross-sectional area, it is possible to calculate an actual sheet resistance for a dished line. This has been

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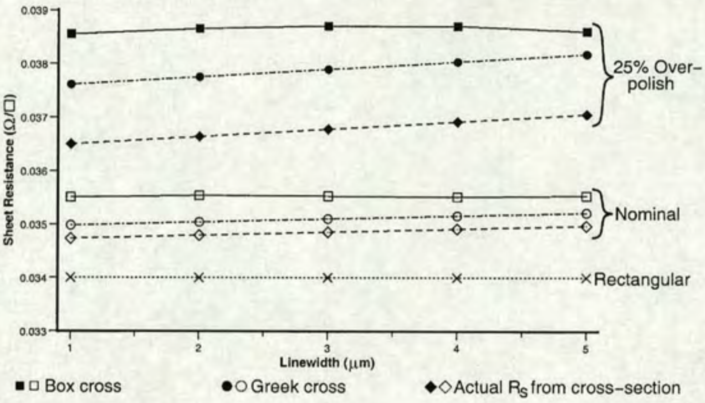

Fig. 16. 3-D simulations of the effects of dishing on the sheet resistance extracted from Greek and box crosses.

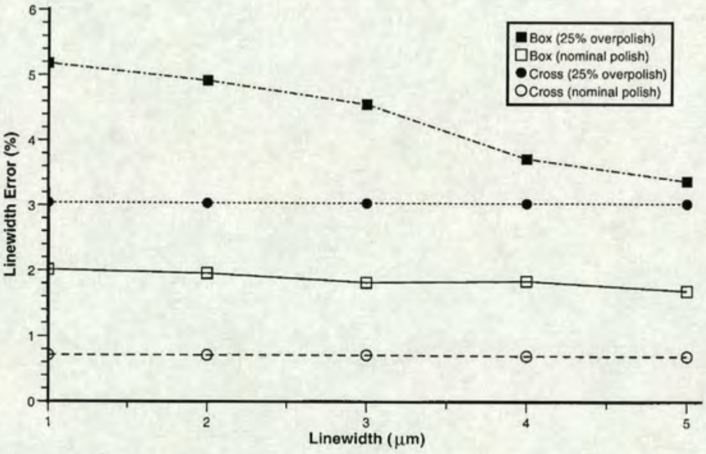

Fig. 17. Electrical linewidth error versus the actual linewidth for structures with dishing.

performed for the two different endpoints and for each of the linewidths simulated, and the results are plotted alongside the 3-D simulation results. For reference, Fig. 16 also shows the nominal value of sheet resistance for 0.5 μm thick copper with no dishing.

The results for the 3-D simulations with 25% overpolish compare well with the 2-D results indicating that the assumptions of the 2-D model approximating the dishing effect are reasonably valid. From Fig. 16, it can be observed that the offset between the sheet resistances extracted from the Greek cross structures and those calculated for a dished line is approximately 0.7% for the nominal polish conditions and 3% for the structures with 25% overpolish. This indicates that the error in the extracted sheet resistance increases with the amount of overpolish and, therefore, the level of dishing.

One important thing to note is that as the linewidth increases, the extracted R_S from the Greek cross structures increases at the same rate as the actual sheet resistance calculated from the cross-sectional area. This is not the case for the simulated box cross structures where the sheet resistance extracted is independent of the width of the voltage taps. The variation in the 25% overpolish box cross results is probably due to small variations in the number of nodes in the automatically generated simulation grid.

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D. Dishing Effects on Linewidth Measurement

The next step is to investigate the effect of dishing on the measurement of electrical linewidth. Equation (7), which gives the cross-sectional area of a dished track, can be used to calculate the resistance for a certain length of copper line. This calculation has been performed for each of the linewidths used in the test structure simulations and for both endpoint conditions.

The electrical linewidth can then be found by using the line resistance and the extracted sheet resistances in (3). If these results are then compared to the actual widths, the linewidth measurement errors due to dishing can be calculated. This process has been followed using the sheet resistances extracted from the 3-D simulations, and the results are presented in Fig. 17.

The linewidth errors for the Greek crosses do not vary with tap width staying at about 3% for the 25% overpolish condition and at about 0.7% for the nominal polish. This should be expected because of the way that the sheet resistance extracted from the Greek crosses increases at the same rate as that calculated from the dished cross section. This can be seen for both of the endpoint conditions in Fig. 16. The box cross results are different because the amount of dishing in the box does not change with the voltage tap width. This means that the errors decrease with increased linewidth but are still higher than for the Greek cross structures. These results indicate that, provided the condition in (2) is not violated and instrumentation resolution and joule heating are not issues [6], sheet resistance measurements should be made using Greek cross structures with arm widths the same as the linewidth structures being tested.

IV. CONCLUSION

Simulations have been used to quantify the effects of diffusion barrier layers and dishing on the measurement of the sheet resistance and electrical linewidth of copper damascene interconnect. Section III-A showed that a Greek cross test structure can be used to measure the sheet resistance of copper and an underlying barrier layer with an error of less than 1% provided that the condition given in (2) is satisfied. It was also found that the values of R_S extracted from box cross sheet resistance structures were always within 1% of the correct value because the box structures are insensitive to the voltage tap width.

The results of the test structure simulations were then used to evaluate the effect of diffusion barrier layers on the electrical measurement of linewidth. It is clear that the effect of the sidewall barriers on the total line resistance becomes more dominant as the width of the line being measured is reduced. This potentially leads to very large errors in the linewidth measurement but, fortunately, it is possible to calculate the sidewall contribution and subtract it. The modified line resistances can then be used, along with sheet resistances extracted from the simulated structures, to calculate the electrical linewidth using (3). The only error in the resulting linewidth is due to the effect of the sidewall barriers on the cross structure used to extract R_S. This method assumes that the sidewall barrier width (W_{bv}) does not vary with the total width of the line, which will normally be the case for the feature sizes considered in this work [6].

The simulations used to evaluate the effects of barrier layers have assumed that the metal track has a rectangular cross section but in most damascene processes some dishing will be present. Some exceptions to this might be advanced polishing processes with well-developed endpoint control to reduce dishing or processes which use low-k dielectrics that are softer than the copper [16]. The model of dishing that was used to create the simulated Greek and box cross test structures had two possible polishing endpoint conditions. The difference between the sheet resistances extracted from the Greek cross structures and equivalent sheet resistances for copper lines with the same amount of dishing was found to be less than 1% using the nominal polish condition and about 3% with a 25% overpolish.

The above results can be used to predict how a combination of dishing and barrier layers would affect the performance of sheet resistance structures and the measurement of linewidth. Sheet resistance measurements of box cross structures are not affected by the sidewall barrier layers but the large area of the box is more likely to experience a greater degree of dishing. In this case, the sheet resistance extracted from such a test structure may be significantly higher than for a narrow structure leading to an unacceptable error in the calculated value of electrical linewidth.

The effect of sidewall barriers on the sheet resistance measurement of Greek cross structures that meet the condition given by (2) is minimal. When dishing is the dominant effect, the extracted sheet resistance will increase as the width of the arms of the cross increase. If a Greek cross is to be used as part of a linewidth measurement, then the width of the cross arms should be the same as the nominal width of the bridge linewidth structure in order to minimize the effect of dishing.

However, if the Greek cross structure does not meet the condition of (2), then the effect of the sidewall barriers will dominate and the extracted sheet resistance will increase as the feature size decreases. This puts a limit on the minimum linewidth that can be measured accurately. If a larger Greek cross, which is unaffected by the sidewall barriers, is used, then another error is introduced because the dishing in the cross will be greater than in the bridge.

The conclusion is that in order to achieve the most accurate measurement of the electrical linewidth of a copper track affected by both diffusion barrier layers and dishing, the sheet resistance should be measured using a Greek cross that has arms the same width as the track and is large enough not to be affected by the sidewall barriers.

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Stewart Smith received the B.Eng. (hons.) degree in electronics and electrical engineering from the University of Edinburgh, U.K., in 1997. He is currently working toward the Ph.D. degree with the silicon technology research group at the University of Edinburgh.

His current research interests include the use of resistive electrical test structures for process development and for the characterization of advanced materials and fabrication techniques.

Anthony J. Walton (M'88) is professor of Microelectronic Manufacturing in the Department of Electrical and Electronic Engineering at the University of Edinburgh, U.K. He has been actively involved with the semiconductor industry in a number of areas including silicon processing (both IC technology and microsystems), microelectronic test structures, Yield improvement, Design for Manufacturability (DFM) and Technology Computer Aided Design (TCAD). His present interests also include the optimization of semiconductor processes through the integration of experimental design and TCAD simulation tools. He has published over 150 papers.

In 1990, Dr. Walton won the best paper award for the IEEE Transactions on Semiconductor Manufacturing. He also serves on the steering committee of the IEEE International and IEEE International Conference on Microelectronic Test Structures (ICMTS) and is an associate editor of the IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING and *The Journal of Electronics Manufacturing*.

Alan W. S. Ross was senior production engineer at Ferranti plc, Edinburgh, U.K., where he developed manufacturing methods for optical metrology products. In 1989, he transferred to the field of silicon technology research at The Edinburgh Microfabrication Facility, based at The University of Edinburgh. As a research fellow, his activities encompassed wafer metrology, X-ray lithography and semiconductor processing methods.

He next worked for Siemens Microelectronics in Dresden and North Tyneside, where he was closely involved in process transfer and start-up of the new 8-in wafer fab in the U.K. He was later invited to take up a research post in the Department of Physics and Astronomy at The University of Edinburgh, where he devised techniques for manufacturing low-cost adaptive optical devices. He is now part of the new Scottish Microelectronics Centre team, carrying out research into copper interconnect strategies for the new generation of silicon microchip devices.

Georg K. H. Bodammer studied physics as the Universities of Karlsruhe, Cambridge, and Edinburgh, U.K. He received the Ph.D. degree from the University of Edinburgh, U.K., in 1997.

In the following years, he held post-doctoral positions in various departments of the University of Edinburgh, and joined MicroEmissive Displays Ltd. as wafer processing engineer in early 2001.

J. T. M. Stevenson received the B.Sc. degree in physics in 1967, the M.Sc. degree in instrument design from the University of Aberdeen, U.K., in 1969, and the Ph.D. degree from the University of Edinburgh, U.K., in 1988.

He spent five years at Ferranti Ltd, Dalkeith, as a Development Engineer on moire measuring systems. In 1974, he joined the Wolfson Microelectronics Institute to work on the design of a pattern generator for the production of integrated circuits. In 1980, he was appointed to a research fellowship in the Edinburgh Microfabrication Facility, University of Edinburgh. His main research interests are in optical lithography and optical measurement techniques.

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