THE UNIVERSITY
of EDINBURGH

Power and Spectrally Efficient Integrated High-Speed LED drivers for Visible Light Communication

The University of Edinburgh

Aravind Venugopalan Nair Jalajakumari

October 23, 2017

Abstract

Recent trends in mobile broadband indicates that the available radio frequency (RF) spectrum will not be enough to support the data requirements of the immediate future. Visible light communication, which uses visible spectrum to transmit wirelessly could be a potential solution to the RF 'Spectrum Crunch'. Thus there is growing interest all over the world in this domain with support from both academia and industry. Visible light communication(VLC) systems make use of light emitting diodes (LEDs), which are semiconductor light sources to transmit information. A number of demonstrators at different data capacity and link distances has been reported in this area. One of the key problems holding this technology from taking off is the unavailability of power efficient, miniature LED drive schemes. Reported demonstrators, mostly using either off the shelf components or arbitrary waveform generators (AWGs) to drive the LEDs have only started to address this problem by adopting integrated drivers designed for driving lighting installations for communications. The voltage regulator based drive schemes provide high power efficiency (> 90 %) but it is difficult to realise the fast switching required to achieve the Mbps or Gbps data rates needed for modern wireless communication devices. In this work, we are exploiting CMOS technology to realise an integrated LED driver for VLC. Instead of using conventional drive schemes (digital to analogue converter (DAC) + power amplifier or voltage regulators), we realised a current steering DAC based LED driver operating at high currents and sampling rates whilst maintaining power efficiency. Compared to a commercial AWG or discrete LED driver, circuit realised utilisng complementary metal oxide semiconductor (CMOS) technology has resulted in area reduction ($29mm^2$).

We realised for the first time a multi-channel CMOS LED driver capable of operating up to a 500 MHz sample rate at an output current of 255 mA per channel and >70% power efficiency. We were able to demonstrate the flexibility of the driver by employing it to realise VLC links using micro LEDs and commercial LEDs. Data rates up to 1 Gbps were achieved using this system employing a multiple input, multiple output (MIMO) scheme. We also demonstrated the wavelength division multiplexing ability of the driver using a red/green/blue commercial LED. The first integrated digital to light converter

(DLC), where depending on the input code, a proportional number of LEDs are turned ON, realising a data converter in the optical domain, is also an output from this research. In addition, we propose a differential optical drive scheme where two output branches of a current DAC are used to drive two LEDs achieving higher link performance and power efficiency compared to single LED drive.

Declaration of originality

I hereby declare that:

- the thesis has been composed entirely by myself;
- the research recorded in this thesis (excluding the exceptions stated below) originated as a result of my work;
  - the UP-VLC demonstrator characterisation (in Chapter 5) were performed by Dr Sujan Rajbhandari at University of Oxford.
  - fabrication and characterisation of μLED (in Chapter 5) were carried out by Dr Jonathan McKendry and Dr Enyuan Xie at University of Strathclyde
- the work has not been submitted for any other degree or professional qualification

Aravind Venugopalan Nair Jalajakumari

Acknowledgement

I have had the pleasure of working with many highly skilled professionals throughout the duration of my research and to each of them I would like to attribute the success of this research. I would first like to thank my academic supervisor, Prof Robert K. Henderson, whose guidance and dedication has been invaluable and irreplaceable throughout this research. Special thanks must also go to Prof Harald Haas for providing me with valuable advice at the most crucial moments. I must also thank Dr. Katherine Cameron, for her valuable suggestions and reviewes. Special thanks to Dr Sujan Rajbhandari, from The University of Coventry for helping me with the measurements and PAM decoding. Many thanks to Dr Dobroslav Tsonav, for helping me with OFDM decoding firmware and innumerable discussions. Special thanks to Dr Stefen Videv, for assisting me with experimental setups and lab equipments. I must also thank Dr Jonathan Mckendry and Dr Enyan Xie from the University of Strathclyde, for assisting me with μLED measurements and characterization. Special thanks to Susan Kivlin, for PCB assembly. To my wonderful team mates from CMOS Sensors and Systems and Institute for Digital Communications at the University of Edinburgh group – thank you for your practical contributions, our many insightful discussions and most importantly your infectious enthusiasm for the research. This research and its findings would not have been possible without the Scholarship from School of Engineering, the University of Edinburgh. To all my friends; thank you for your patience during my long social hibernation, I look forward to spending more time with you all. I dedicate this work to; my mother for her relentless encouragement and support, my father - who I lost mid-journey for being a calming strength in my life and my daughter Iha- the gift I received mid- journey for her smiles and unconditional love; I promise to make up for our lost time. I must also thank my extended family in India for their words of encouragement. My deepest gratitude however must go to the person who has been my better half in every sense of the word throughout this journey – Aiswarya, thank you for teaching me persistence, for your love and for your complete faith in me; this success is as much yours as it is mine.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Light based Communication Systems

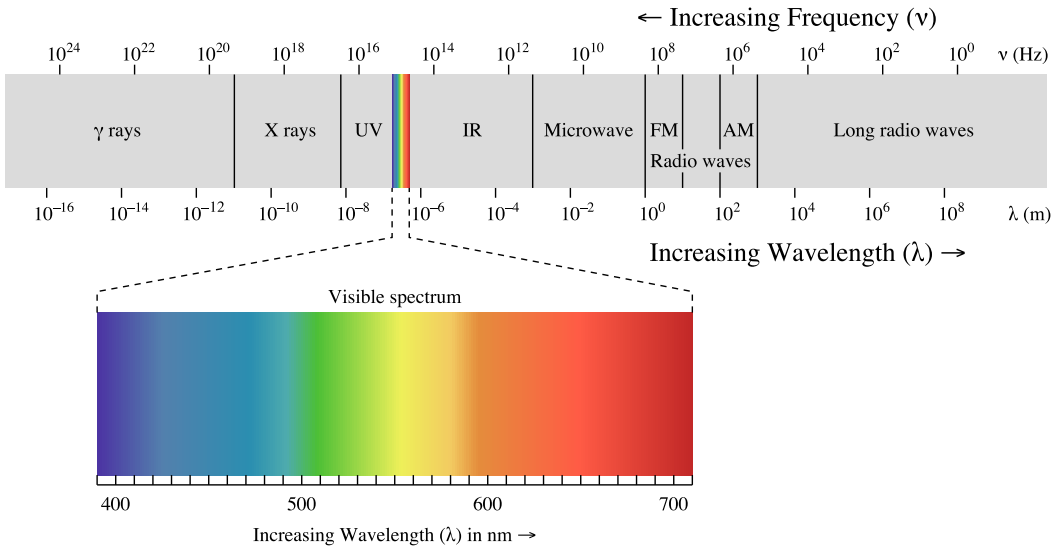


Figure 1.1: EM spectrum [1]

Light is a form of electro magnetic (EM) radiation produced by the oscillating electric and magnetic fields. It forms part of the EM spectrum which extends from gamma rays to radio waves (see Figure 1.1). Since it's a form of energy, it can be used to establish communication links to transfer information from one point to another. From early history, light has been used as a medium to send information over distances. For example, Greek historian Polybius devised an encoding mechanism for Greek alphabets known as the *Polybius Square* which could be communicated using fire torches [2]. Many ancient civilisations used smoke generated from fire to convey presence or special messages. The optical telegraph invented by Claude Chappe was another example which used high ris-

ing towers separated by tens of kilometres to transmit information [3]. Optical telegraph towers consist of wooden semaphores to transmit information and telescopes to receive information. During the late 18th century an extensive optical telegraph network was built through France, Germany, Italy, Netherlands e.t.c. Light based communication systems have evolved to become the backbone of the communication infrastructure due to their reliability and lower cost of implementation. They can be broadly classified into wired systems (FOC systems) and wireless systems (optical wireless communication (OWC) systems).

1.1.1 Wired systems: Fibre optic communication (FOC)

In FOC, data is transmitted between two points by encoding light pulses and sending them through optical fibres. Optical fibres are thin, transparent fibres made out of glass or plastic which can carry light signals through them over distances. They have a dense core layer and less dense outer cladding layer. Light injected into the transparent optical fibre does not escape to the outside, but traverses forward inside the optical fibre by the phenomenon of total internal reflection. This happens when the angle at which a light ray strikes the fibre is greater than the *critical angle*, causeing the ray to reflect internally and propagate instead of refracting.

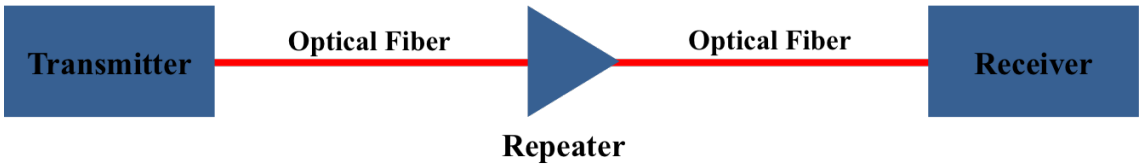


Figure 1.2: FOC link

A typical FOC system consists of a transmitter, optical fibre, repeater stages and a receiver as shown in Figure 1.2. The transmitter encodes the digital information into light pulses and sends them through the optical fibre to the receiver, which converts light pulses into electrical signals for further processing. Optical signals traversing through the link attenuate due to scattering, absorption leakage e.t.c which results in reduction of received signal power [4]. To compensate for the losses, repeater stages are required at different points in the link depending on the link distance. Fibre optic cables started to replace copper based wired communication links from 1970's owing to their superior capacity and reduction in operating costs. Over the last three decades, the installed capacity has increased by 10000 times owing to usage of newer transmission windows and application wavelength division multiplexing (WDM) techniques [5].

1.1.2 Wireless systems: Optical wireless communication (OWC)

Unlike FOC, which uses optical fibres as a medium to carry the light modulated with information, OWC systems transmit optical signals encoded with information into free space. VLC is a subset of OWC which uses the visible part of the EM spectrum (wavelengths 400 - 800 nm) for wireless communications. Outdoor long distance OWC links are also possible using high power laser diodes (LDs) as demonstrated in the 622 Mbps earth-moon communication link by National Aeronautics and Space Administration (NASA) [6]. A 1.25 Gbps OWC link from a flying aircraft to an earth station is presented in [7]. There are also other incarnations of OWC employing the infrared (IR) and ultraviolet (UV) regions of the EM spectrum. Work in this thesis is primarily targeting VLC systems therefore it will be introduced in this section and discussed in detail in Chapter 2. In modern times, it was Alexander Graham Bell who invented an apparatus that could transmit speech signals wirelessly using light. Named *Photophone* [8], the device was used to transmit the world's first wireless voice message on February 19, 1880. Even though Bell considered Photophone to be his greatest achievement, it did not become as popular as his other invention, the wired telephone. One possible reason for this could be the long distance cable lines laid across continents and oceans allowing long haul wired communications to become easily accessible and cost effective. The photophone could achieve wireless communication only over a range of a few hundred meters and there was no suitable electronics or artificial light sources available at that time to make this technology faster for other purposes such as data communication. After the Photophone, OWC did not gain momentum until 1970's. In 1979, Gfeller and Bapst showed that diffused IR radiation can be used to realise indoor OWC links [9]. They demonstrated free space links up to 125 Kbps. Recent VLC works are discussed in Section 2.3. Figure 1.3 shows

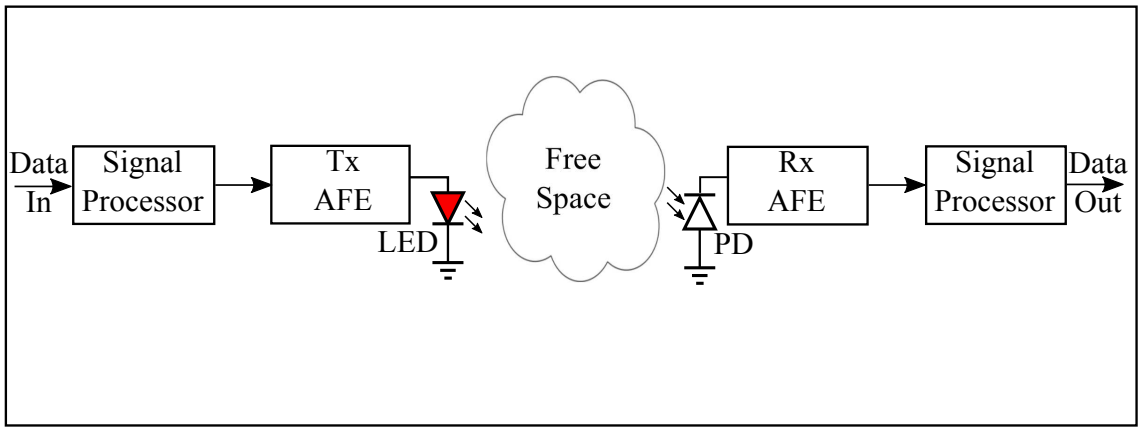


Figure 1.3: VLC system block diagram

a typical VLC system. It consists of a transmitter section, free space optical channel and a receiver section.

1.1.2.1 Transmitter

Incoming digital data is processed by a signal processor before transmission using visible light. Processing includes various steps such as error correction , digital modulation, pre-distortion etc. Error correction schemes (e.g. forward error correction (FEC)) encodes the message utilising an error correcting code (ECC) before modulation. This ensures redundancy in transmitted data and thereby easy recovery. The data to be transmitted is then modulated using any standard modulation scheme (e.g. OOK, OFDM and PAM). Modulation varies the properties of the digital information stream so that it can be now transmitted through an analogue channel utilising an appropriate front end. The transmitter analogue front end (AFE) generates an analogue signal from the modulated digital signal. This step involves digital to analogue conversion performed by a DAC and power amplification to increase the transmitted power. The generated analogue signal is used to drive the optical front end (LED, LD) whose output light intensity is modulated by this signal. Both voltage mode and current mode drive schemes are possible for driving LEDs. In a VLC system, the light generated from the LED propagates through free space. Free space light propagation causes the intensity of the light to reduce over distance, reflect back and forth, partial absorption or even completely by opaque barriers.

1.1.2.2 Receiver

A receiver element (e.g. photodetector (PD)) placed in the illumination field of the LED will convert the intensity variations into corresponding electrical signals (voltage or current). This is further processed in the analogue domain by the receiver analogue front end (AFE) (e.g. transimpedance amplfier (TIA)). Analogue processing involves amplification, filtering and analogue to digital conversion by an analogue to digital converter (ADC). The digital output from the ADC is demodulated and decoded by the signal processor block.

1.1.2.3 Advantages of a VLC system

Compared to other wireless data transmission technologies such as radio frequency (RF) communication systems, VLC systems has certain advantages such as,

Free and unregulated spectrum: The visible part of the EM spectrum is freely available to use for wireless communication purpose and it is not regulated by any agency unlike the RF spectrum which is tightly controlled by government agencies and very expensive to obtain.

Available bandwidth: Compared to RF spectrum (~3 Hz to 300 Ghz), the visible spectrum ranges from approximately 400 to 800 THz, which translates to a usable bandwidth of 400 THz (~1000 times more than RF).

Inherent security: Unlike RF transmission, light cannot penetrate opaque barriers such as walls thus making it secure compared to RF systems.

Safety: Light does not have adverse health effects like RF or IR systems. It can also be used in restricted environments such as hospitals, petroleum refineries and similar environments where RF emission is hazardous.

Energy efficiency: VLC systems use LEDs to transmit information. LEDs are already replacing conventional light sources [10] due to their energy efficiency and long life time. Therefore data transmission using LEDs comes at zero power penalty compared to RF systems which needs dedicated power to transmit information.

Infrastructure: Lighting infrastructure which is already present could have VLC capability by minor modifications.

No electro magnetic interference (EMI): Light does not cause EMI hence VLC systems can be used in scenarios susceptible to EMI.

1.1.2.4 Selected applications of VLC

VLC can support existing RF systems to increase capacity. Hybrid networks using both VLC and RF schemes has been studied [11]. Fully networked, bi-directional VLC links named Light Fidelity (Li-Fi) [12] could complement or replace existing indoor wireless networks. Like Wireless-Fidelity (Wi-Fi) links, Li-Fi links could also provide connectivity to multiple users simultaneously [12]. Vehicle to Vehicle communication is another area where VLC can be used. Increase in road traffic and accidents points to the need for intelligent vehicular and traffic control systems. VLC could be a potential solution to this problem and experiments demonstrating successful vehicular communications using VLC has been reported [13, 14]. Indoor positioning using VLC systems is an attractive proposition since satellite navigation signals does not work inside buildings [15]. Such systems will be useful especially in busy public areas such as airports, hospitals, museums e.t.c. Other application domains where VLC could be employed include under water communications, the internet of things (IoT) and communication systems for hazardous environments.

1.1.2.5 Significance of VLC

Recent trends in communications [16, 17] shows an exponential increase in the data usage. The Cisco visual networking index forecasts monthly mobile data traffic to reach 30.6 exabytes by 2020 [17]. RF systems, which dominate the wireless world may not be able to cope with the exponential data capacity requirements due to the unavailability of new bands in the RF spectrum [18, 19]. VLC using the unregulated ~400 THz visible spectrum (compared to ~300 GHz RF spectrum) could solve the spectrum crisis by augmenting or replacing RF technologies.

1.2 Research aims

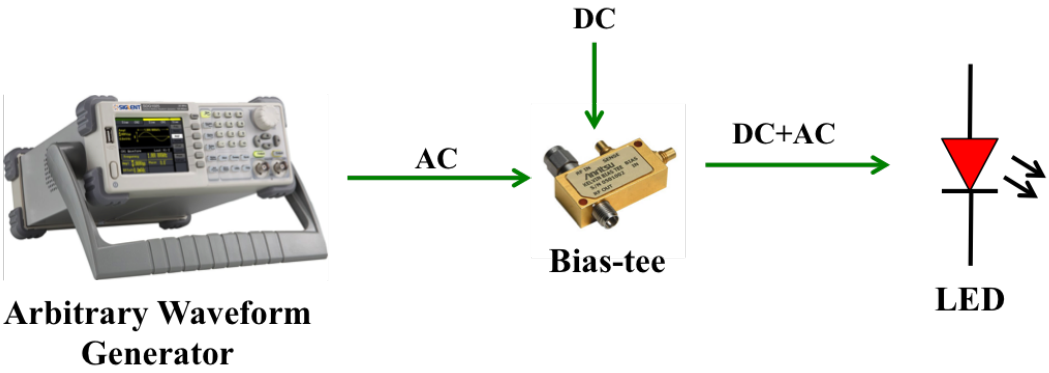


Figure 1.4: AWG based VLC transmitter

State of the art high speed VLC demonstrators (listing a few [20, 21, 22, 23, 24, 25, 26, 27]) use a commercially available AWG to generate the time varying modulation signal mixed with a DC bias using a bias tee. This scheme is shown in Figure 1.4. Other VLC demonstrators realised transmitter systems using discrete components to drive LEDs [28, 29]. The next step needed for the commercialisation and mass production of VLC transmitters is to reduce the size of the drive circuitry electronics. The primary aim of the research undertaken is to miniaturise the LED drive circuitry using CMOS technology, which should help to reduce the transmitter footprint, reduce the cost of the system and allow it to be easily added to portable electronics. The secondary aim is to investigate suitable drive schemes that can be integrated whilst providing high power efficiency, high speed operation and support multiple modulation schemes (OOK, PAM, OFDM). Even though the driver specifications were derived from UP-VLC project (Section 1.3), including the demonstrator requirement to use μLEDs, the tertiary aim of this research is to increase the output current levels to drive commercial OTS LEDs as well.

1.3 Project background

The work carried in this thesis is part of the UP-VLC project. UP-VLC is a £4.5 Million Engineering and Physical Sciences Research Council (EPSRC) funded project [30]. The UP-VLC project aims to develop high data density ($Tb/S/mm^2$) VLC systems utilising developments at the component and system level. These include developments in Gallium Nitride (GaN) μLEDs, CMOS LED drivers, CMOS APDs, communication system algorithms, organic materials for colour conversion etc. The penetration of LEDs into lighting markets have also spawned interest in utilising them to solve the RF spectrum crunch. Five academic institutions in the UK are partnered in this project namely the University of Strathclyde, University of Edinburgh, University of Oxford, University of St Andrews

and University of Cambridge. Each partner institution's expertise in areas mentioned earlier are leveraged to realise data dense VLC demonstrators. Industrial partners are also involved in providing useful feedback into the research in this project. Integrated CMOS electronics envisaged in the UP-VLC project include a LED driver and APD receiver chips. Research into this area is undertaken by the CMOS Sensors and Systems group at the University of Edinburgh where I started working on the integrated LED driver. The CMOS LED driver developed is to be part of a Gbps VLC demonstrator deliverable for the UP-VLC project.

1.4 Method of Execution

The work carried out as part of the thesis had many steps

- Survey the literature to understand different LED drive schemes suitable for VLC.
- Study the electrical and optical characteristics of different types of LEDs.
- Derive specifications for the integrated LED driver from system modelling done at University of Oxford and Edinburgh.
- Develop a drive scheme suitable for integration satisfying all specifications.
- Design of the integrated LED driver, including layout and simulations to verify the functionality.
- Prepare supporting hardware (PCBs) and firmware (personal computers (PCs), FPGAs and Matlab).
- Perform electrical characterisation and realise VLC links using the driver and study them.
- Support project partners to perform experiments using the CMOS LED driver.

1.5 Contribution to knowledge

For the first time a multi-channel CMOS integrated current steering DAC based LED driver is implemented for VLC. It has the highest power efficiency vs achievable data rate when compared to other integrated drive schemes reported so far. By circuit integration, we have reduced the foot print of the driver circuit to approximately 30 mm^2, which is key towards mass production and commercialisation of VLC systems. The driver is capable of operating up to a 500 MHz sample rate whilst delivering 255 mA of current for each channel, which is the highest output current reported for a current steering DAC so far. We

have also demonstrated that the driver is compatible with different modulation schemes such as OOK, PAM and OFDM. Study of the VLC links established with this driver has shown that the adjustable full scale current feature of the driver is beneficial to maintain the data rate when the link distance is changed. Usage of this scheme combined with the DC offset feature is shown to be useful to tune the frequency response of the transmitter to achieve better performance while employing μLEDs. Varying the bias current to adapt the data rate has also been shown to affect the correlated colour temperature (CCT) of the light emitted by the RGB LED and puts a constraint to the achievable data rate in a CCT constrained system. The integrated multi-channel current DAC drive scheme introduced in this work also supports various possible methods to improve performance of VLC links such as MIMO and WDM. An experiment where two LEDs were driven differentially by loading them on to the two output branches of a current DAC is performed and resulted in a link with improved signal to noise ratio (SNR) and optical output power when compared to conventional drive schemes. We have also realised the first integrated DLC by wire bonding a custom built μLED array on to the CMOS die. VLC links using both OFDM and PAM modulation schemes at high power efficiency were demonstrated. The DLC link demonstrated is suitable for high speed, short range wireless communications targeting applications like IoT.

The results from this work including electrical characterisation of the CMOS LED driver, OTS LED based VLC link, differential optical drive and power efficiency values were presented at the International Communication Conference (ICC) 2015 and are available in conference proceedings [31]. A photonics technology letters (PTL) paper was published collecting results from the integrated DLC experiments [32]. Collaborative work with project partners has resulted in other publications [33, 34, 35, 36]. UP-VLC MIMO work has been submitted to the Journal of Lightwave Technology (JLT) and is being reviewed at this time.

1.6 Thesis structure

Chapter 2 discusses VLC and recent research undertaken in this domain. LED properties and structure, modulation schemes, and associated electronic drive schemes are also discussed. Since this work is based on DACs, different types of DAC structures are presented.

Chapter 3 begins with the specifications of the driver chip and the CMOS technology used for fabricating the chip. Design details of each IC sub block is presented along with simulation results. Layout of the circuit blocks are also shown here along with optimisations. The circuit structure of the DLC scheme and integration details are presented in this chapter as well.

In Chapter 4, details of the characterisation bench are presented. Design details of PCBs designed to characterise the LED driver and used to realise various VLC demonstrators are given. Discussion of the firmware used in the PC and FPGA are presented. Results from electrical characterisation of the DAC are presented and discussed.

VLC experiments performed with the driver chip while driving μLEDs are presented in Chapter 5. The UP-VLC demonstrator utilising the multichannel capability of the CMOS LED driver to realise a Gbps MIMO link is presented along with results from link characterisation. The first integrated DLC system realised by integrating a unary CMOS DAC and a custom fabricated μLED array is characterised for static parameters. An OFDM based VLC link using the integrated DLC is created and characterised. The power efficiency of the DLC system is calculated based on measured voltage and current values at the output stage.

Owing to the output drive current and an open drain architecture, the driver chip can drive high power OTS LEDs. Chapter 6 presents the results from VLC links realised using OTS LEDs. Results from VLC SISO links realised using two different variants of OTS LEDs are presented. Correlation between different parameters such as link distance, bias current, sampling rate and QAM levels are studied in this chapter. A WDM VLC link is realised using an OTS RGB LED utilising the multi channel drive capability of the CMOS LED driver and the results are presented from this experiment. To utilise the power dissipated in the dummy branch of the current DACs in the CMOS LED driver and to increase the transmitted power, a differential optical drive is experimented with where both the branches are loaded with LEDs. This chapter also presents results from the differential optical drive experiment showing the improvement in link performance.

The thesis is concluded in Chapter 7. A summary of the results from experiments using the CMOS LED driver are presented along with a brief critical discussion. Possible research avenues further to this work are also discussed here.

Additional details related to this work such as driver chip pin out, bonding diagram, schematics of PCBs, Verilog and Matlab firmware are given in Appendix A. Appendix B lists down the publications that came out as a result of this work.

Chapter 2

Visible Light Communication

2.1 Overview

The aims of this work are threefold namely (1) miniaturisation of the LED driver circuit for VLC, (2) investigate power efficient drive schemes that do not compromise on data rates and (3) support different variants of LEDs. Recently interest in VLC has increased due to various factors such as the RF spectrum crunch, the penetration of solid state lighting and IoT. This chapter discuss VLC systems and subcomponents in detail. A literature review of VLC systems and LED drive schemes are presented. Like any other wireless communication system, VLC requires and supports data encoding or modulation formats. Simple modulation schemes like OOK and complex schemes such as OFDM, PAM etc have been successfully used to encode light signals transmitted wirelessly. The operation principles of the modulation schemes used for VLC are presented in this chapter. VLC uses semiconductor light sources such as LEDs or LDs. The electrical and optical properties of LEDs which affect the performance of a VLC system is analysed in this section of the thesis. LED technology is widely used for lighting purposes due to advantages such as long life time, lower cost and high power efficiency. Electronic control of these light sources is possible and many different types of circuit topologies exist, which could efficiently drive the LEDs in lighting applications. Conventional LED drive topologies for lighting applications are presented and their drawbacks, when used for VLC are analysed. An open-drain current steering DAC based drive scheme is introduced for VLC transmitters. Before presenting design details of the said driver, different DAC topologies are discussed.

2.2 Wireless Communication and Spectrum Crunch

Even though the world's first wireless communication experiment used visible light for signal transmission, named *Photophone* [8], RF based systems gained popularity and wide usage across various domains. In the late 19'th century and early 20'th century, many pioneers like David Edward Hughes (printing telegraph [37]), Guglielmo Marconi (radio [38]), Thomas Edison, Nikola Tesla, Jagadish Chandra Bose (radio research [39]) investigated and demonstrated wireless communication using radio waves. Radio communication systems gained wide popularity during the last century [40]. The radio spectrum, ranging from $3Hz$ to $300GHz$, is divided between many commercial and military applications [19]. This includes widely used ones like audio broadcasting, wireless telegraphy, telephony, data communication, device to device communication, local area networks to niche applications like military radars, radio astronomy amateur radio etc. Advancements in other technological areas such as electronics, computing, manufacturing and signal processing resulted in wider usage for radio communication. In the late 20'th century, developments in cellular telephony and the internet resulted in further penetration of radio communications. The RF spectrum is regulated by governments in all countries and this spectrum is divided into various bands based on the applications (the allocation in the UK can be found in [19]). The increase in applications using RF has resulted in non-availability of RF spectrum to satisfy ever growing need of wireless data [16, 17]. Trends in mobile data usage indicates that 30.6 exabytes will be the monthly mobile data traffic by 2020 and the per capita connected devices per person will be 1.5 by 2017 [17]. The Federal Communications Commission (FCC) termed this as the *Spectrum Crunch*. Various methods are proposed to solve the spectrum crunch such as freeing up unused spectrum including the millimetre band[41], TeraHertz band (0.1 THz - 10 THz) [42] and the visible spectrum. The visible light spectrum extends from approximately 400 to 800 THz. Compared to 300 GHz RF band , the visible spectrum has a bandwidth of 400 THz, wide which is approximately 1000 times more than RF. It also offers inherent security since light, unlike radio waves, cannot penetrate through walls or such obstacles.

2.3 VLC systems in literature

Light has been used a medium of communication since very old days. Optical wireless communication needs suitable light sources which could be modulated to transmit information and detectors to receive that information. Unavailability of such devices, the popularity of wired communication systems (early-mid 20'th century) and RF wireless communication systems (late 20'th century) has caused this area to be in hibernation. The invention of LEDs [43] and further developments in this area revolutionised the semiconductor lighting industry. LED performance has multiplied over decades of improvement

from semiconductor materials, manufacturing process and assembly methods[44]. Free space optical communications using IR LEDs is well studied by Gfeller and Bapst in [9]. In [9] an OOK modulation scheme was used and data rates up to 1 Mbps were achieved. Wireless IR communication was standardised by the Infrared Data Association (IrDA) in 1993 [45]. Data rates up to 100 Mbps are possible as of now and higher data rates are envisaged by IrDA. The visible light spectra (400 to 800 THz) could also be used for free space communication. The invention of the blue LED [46] and white light generation using them, resulted in the replacement of conventional light sources (incandescent and fluorescent) for ambient lighting due to their long life span and high power efficiency. In 1999, some VLC concepts were explored by Pang *et.al* from University of Hong Kong [47, 48, 49]. In these works, commercially available LEDs or LED displays were used for application scenarios like information transmission from traffic lights and wireless transmission of audio. Link distances of up to 20 m have been reported [48]. Research in free space optical communication using visible light started in Japan in 2000's lead by Nakagawa [50, 51, 52], where it was demonstrated that white LEDs used for ambient lighting could also be used for VLC. Usage of multiple white LEDs and their effects while using OOK and OFDM was explored in [50], whereas [51] studies the effect of multi path reflection of light on VLC. A home networking scenario is modelled and studied in [52]. These led to the formation of the Visible Light Communications Consortium (VLCC) and standardisation of VLC by 2003 in Japan. Modulation schemes play a key role in increasing achievable data rate within the available spectrum. They also determine the complexity of the communication system. Predominantly, OOK is the modulation scheme explored in the works mentioned so far. Using multi-level modulation schemes such as PAM or multi-carrier modulation schemes such as OFDM should increase the amount of information transmitted within the available bandwidth. Afgani *et.al* reported a VLC system using OFDM in [53]. OFDM based systems were also reported in [54, 55]. Even though OFDM offers superior spectral efficiency, it suffers due to high peak to average power ratio (PAPR) [56] which results in non-linear distortions such as clipping due to the limited dynamic range of the electronic driver front ends and LEDs. Comparison of single carrier schemes such as OOK, PAM and multi-carrier variants of OFDM (asymmetrically clipped optical OFDM (ACO-OFDM), direct-current-biased optical orthogonal frequency division multiplexing (DCO-OFDM)) indicates that the latter offers better spectral efficiency [57]. Practical demonstrations, system modelling and noise analysis of VLC systems using OFDM has been carried out in [58, 59]. Techniques such equalisation has been successfully applied to overcome the limited bandwidth of the commercially available LEDs [60, 61]. High modulation bandwidth [62, 63, 64] μLED developments has sparked interest to use these devices for VLC and multi-gigabit demonstrations had been reported [21, 65]. Transfer characteristics of LEDs are studied in [66], which shows that the optimum bias point selection is crucial to the operation of modula-

tion schemes such as OFDM. Interestingly it has also been shown that LEDs could also be used to sense external light intensity variations and there by replace photo detectors in VLC systems [67]. MIMO implementation [68], gigabit links have also been reported in [69]. VLC systems are maturing into user friendly, networked systems with clear specifications from the physical layer to the higher communication protocol layers, termed *LiFi* [12]. VLC demonstrators based on discrete multitone (DMT) modulation scheme, which is very similar to OFDM, have shown improved performance and been reported over years [70, 24, 25, 22]. Traction to commercialise VLC and associated technologies has resulted in both established players in lighting and semiconductor industries and also spin out companies taking greater participation and introducing new products and demonstrators. Table 2.1 lists published VLC demonstrators from 1999 to present. The achieved data rates in these demonstrators has increased from Mbps to tens of Gbps, which is due to the combined effect of high bandwidth luminaries and spectrally efficient modulation schemes at the transmitter and improved receiver characteristics which are not discussed here. However more than a two thirds of the demonstrators in the above table uses commercially available AWGs to drive the LEDs. This drive scheme is suitable for laboratory demonstrations, but for commercialisation and mass deployment of VLC technology it is not suitable due to the bulky equipment size, high power consumption and high cost of purchase and maintenance. A few of the demonstrators in the list have been realised using discrete components, but the circuit foot print is still higher for portable applications (mobile devices, where most of the wireless data transfer is going to happen [17]). Reported integrated drive schemes for VLC systems could be embedded in portable devices, but so far the achievable data rate is very low. The non-availability of high speed, high power efficient drive schemes for VLC is what we address in the project detailed in this thesis.

2.3.1 Modulation schemes for VLC

The capacity of any digital communication system was derived by Shannon as shown in equation 2.1.

$$C = Blog_2\left(1+\frac{S}{N}\right) \tag{2.1}$$

where C is the capacity of the channel in bps, B is the available bandwidth in Hz, S is the signal power and N is the noise power. From 2.1 it is clear that, to achieve a high data rate, the communication system should have either very high bandwidth or high SNR. Light received at a VLC receiver has gone through the free space optical channel, resulting in various losses including received optical power per area, multi path reflections and interference from other light sources. This results in signal quality degradation and there by reduction of SNR. It is not possible to increase the signal power of the VLC system without compromising eye safety or damaging the LEDs. All these factors limit the available transmit power from a VLC system. Similarly, the available bandwidth of a

Ref	Year	LED	Modulation	Driver	Data rate	Range
[47]	1999	Phosphor White	OOK	Discrete	100 Kbps	20 m
[71]	2007	Phosphor White	DMT	AWG	117.2 Mbps	1 cm
[72]	2008	Phosphor White	OOK	Discrete	40 Mbps	2 m
[73]	2008	Phosphor White	OOK	Discrete	80 Mbps	-
[74]	2009	Phosphor White	OOK	AWG	100 Mbps	-
[70]	2009	Phosphor White	DMT	AWG	230 Mbps	70 cm
[69]	2010	Infrared Laser	OOK	Discrete	1.25 Gbps	4 m
[24]	2010	Phosphor White	DMT	AWG	513 Mbps	30 cm
[25]	2011	RGB	DMT	AWG	803 Mbps	12 cm
[75]	2012	RGB	DMT	AWG	870 Mbps	1.5 m
[26]	2012	Phosphor White	DMT	AWG	1 Gbps	10 cm
[22]	2012	RGB	DMT	AWG	1.25 Gbps	10 cm
[76]	2012	μLED	OOK	Integrated	512 Mbps	-
[77]	2012	Phosphor White	CAP	AWG	1.1 Gbps	23 cm
[78]	2012	RGB	WDM - DMT	AWG	3.4 Gbps	30 cm
[79]	2013	Phosphor White	MIMO - OFDM	AWG	1 Gbps	1 m
[80]	2013	Phosphor White	OFDM	Discrete	48 Mbps	1 m
[27]	2013	RGB	WDM - CAP	AWG	3.22 Gbps	25 cm
[63]	2013	μLEDs	OOK	Integrated	1.5 Gbps	-
[63]	2013	Phosphor White	OOK	Discrete	300 Mbps	11 m
[81]	2014	Phosphor White	MIMO - OOK	-	50 MBPS	2 m
[23]	2014	RGBA	WDM - DMT	AWG	5.6 Gbps	1.5 m
[21]	2014	μLED	OFDM	AWG	3 Gbps	5 cm
[20]	2015	Phosphor White	OFDM	AWG	2 Gbps	1.5 m
[82]	2015	-	OOK	Integrated	266 Kbps	2 m
[83]	2015	μLED	WDM - OFDM	AWG	2.3 Gbps	-
[84]	2015	Blue Laser	OFDM	AWG	4 Gbps	50 cm
[85]	2015	RGBY	WDM - CAP	AWG	8 Gbps	1 m
[86]	2015	RGB - Laser	OFDM	AWG	14 Gbps	30 cm
[87]	2016	μLED	OFDM	AWG	5 Gbps	75 cm
[88]	2016	μLED	WDM - OFDM	AWG	11.28 Gbps	1.5 m

Table 2.1: Published VLC demonstrators

VLC system is limited by the modulation bandwidth of LEDs and other components. Any communication system has to utilise the available bandwidth efficiently for maximising data throughput. Modulation is the process of altering the characteristic of a carrier signal (a sinusoid) with the information to be transmitted. In RF communication, the properties of the carrier signal such as amplitude, phase, frequency or a combination of these are varied according to the information to be transmitted. For example in the amplitude modulation (AM) scheme, the amplitude of the carrier signal is varied in proportion to the information signal. Modulating the information into high frequency carrier signal ensures that the available spectrum is efficiently used, information is not lost by interference and also the physical dimension of the antennas used can be made reasonable since the size of the transmitting antenna is directly proportional to the wavelength of the signal being transmitted. RF wireless systems employ a coherent detection mechanism, where the carrier frequency is generated locally at the receiver to mix with the incoming signal to recover the information signal [89]. Both analogue (e.g. analogue audio or video) and digital (e.g. data) information can be modulated into high frequency carriers. Since VLC is a data communication technology for transferring data using visible light, the focus will be on digital modulation schemes. Unlike analogue modulation schemes where the modulating signal can have infinite values, a digital modulating signal will a only discrete set of values. Basic digital modulation schemes are amplitude shift keying (ASK), frequency shift keying (FSK) and phase shift keying (PSK). In ASK, the amplitude of the carrier signal is modulated based on the digital input. OOK is a special case of ASK, where for transmitting a digital 0, the carrier amplitude is 0. Different carrier frequencies are assigned for representing digital 1 and 0 in FSK. Similarly in PSK, the phase of the carrier is varied, which depends on the digital levels. Binary phase shift keying (BPSK) is a special case where, where the phase of the carrier is changed between 0°and 180°for transmitting binary 1 and 0. The simple modulation schemes (OOK, BPSK) described above transmits 1 bit per carrier frequency, thus having spectral efficiency of 1 bit/Hz. It is desired to achieve a higher spectral efficiency for transmitting more information within limited bandwidth. Complex variants of the modulation schemes mentioned here such as OFDM, PAM report increased spectral efficiencies. More about these schemes will be discussed in this section.

2.3.1.1 IM and Direct detection (DD)

Semiconductors light sources like LEDs or LDs [90, 91] are used for VLC. Due to their wide install base [10], low cost, long life time, high power efficiency and better eye safety characteristics compared to LDs, LEDs are more likely to be used for VLC. Unlike LDs, LEDs produce incoherent light, which means the emitted photons have random phase information. Another aspect to be considered is the frequency of the radiation emitted by LEDs, which goes into hundreds of THz. In RF communication where the frequency of

the radiation is much less (hundreds of GHz), it is possible to modulate the electric field of the carrier utilising suitable electronics [92], whereas electronic circuitry operating at frequencies of visible spectrum are not available at this time. Due to these reasons, intensity modulation (IM)/direct detection (DD) is suited for modulating information and reception. In IM, the intensity or power of the emitted radiation is varied. Variations in intensity depends on the incoming digital data and modulation scheme used. Figure

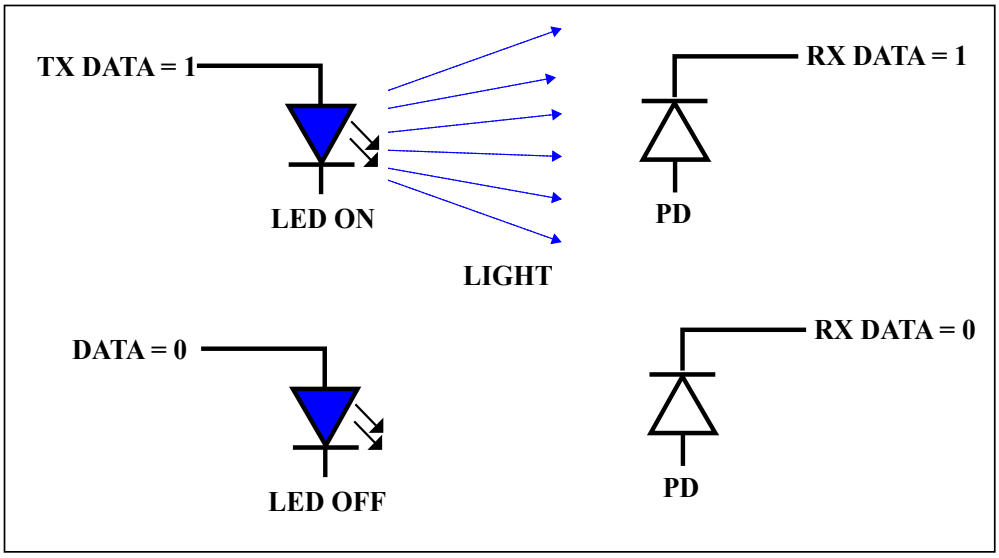


Figure 2.1: Basic principle of IM

2.1 shows the basic principle of IM, where binary 1 and 0 are transmitted by turning a LED ON and OFF respectively. The intensity of the light emitted from the LEDs can be changed by varying either the voltage across it or current through it. Since the intensity modulated signals carry no phase information, conventional heterodyne techniques used in RF reception cannot be used to detect the intensity modulated signals. Instead, the DD technique is employed, where intensity variations are detected by a photo sensitive device (PDs). Owing to the smaller wavelength of the visible light, physical dimensions of these receivers are small compared to receivers used in RF communication (antennae).

2.3.1.2 On-off keying (OOK)

OOK is a relatively simple digital modulation scheme. In this scheme, the incoming binary data stream is used to control the intensity of the LED by turning it ON to represent a binary one or turning it OFF to represent a binary zero. Since intensity modulation and direct detection (IM/DD) technique has to be used, the OOK signal amplitude has to be positive, which is implemented as uni-polar non-return-to-zero (NRZ) signalling. Each transmission symbol corresponds to a bit and therefore the symbol rate corresponds to the bit rate. Due to its relative simplicity OOK has been adopted for OWC early [93] in its modern history and widely [94, 50, 29, 28, 95, 71, 61, 96]. To achieve higher data rates,

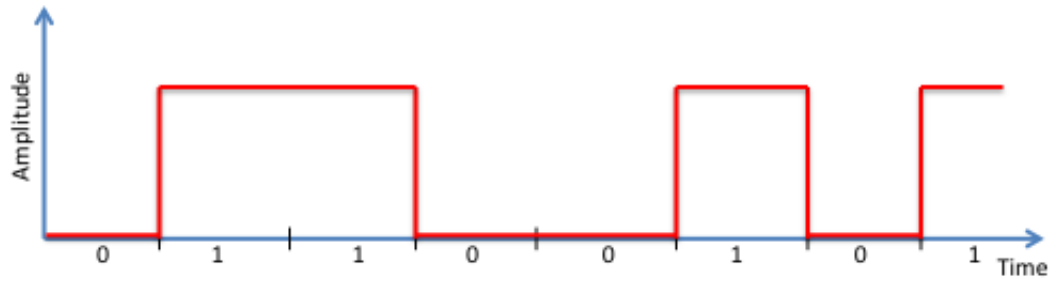


Figure 2.2: OOK modulation

the LEDs must be turned ON and OFF at faster rates. An ideal OOK modulated signal has pulse shapes as shown in figure 2.2 with fast rise and fall times. For a square pulse, the rise/fall times are an indicator of the bandwidth required. The widely used rule of thumb 2.2 relates the bandwidth and rise time of the square pulse.

$$BW = \frac{0.35}{\tau_r} \tag{2.2}$$

where BW is the bandwidth required for generating a square pulse with rise time of τ_r (assuming rise time equal to fall time). The life time of the minority carriers in the active region of the LEDs is a key factor in determining the modulation bandwidth. The rise time is fairly constant, whereas the fall time depends on the voltage applied across the LED [97]. Dependence of rise and fall times on the internal parasitic capacitances (diffusion and junction capacitance) and their voltage dependence puts a limit on the modulation bandwidth and thereby OOK performance. Techniques such as carrier flush out [98] to take away the remaining carriers during the OFF phase and the resultant faster fall times have caused an improvement in modulation bandwidth. Due to the spectral inefficiency of the OOK scheme, it is not suited for high data rate systems.

2.3.1.3 M-level pulse amplitude modulation (M-PAM)

M-level pulse amplitude modulation (M-PAM) is a single carrier digital modulation scheme, where information is encoded into M discrete amplitude levels of the carrier for transmission. For M-PAM the generated signal can be represented as in 2.3 [99]

$$S_m(t) = A_m p(t);\ 1 \leq \mathrm{m} \leq \mathrm{M} \tag{2.3}$$

where A_m represents a set of M amplitude levels and $p(t)$ is a pulse of duration T_s. M can be represented as, $M = 2^K$, where K is the number of bits represented by the symbol. If $R_s = \frac{1}{T_s}$ represents the symbol rate, then data rate can be calculated as $R_s \times log_2(M)$. For example, a 4-PAM system can generate four discrete output levels corresponding to four symbols and each level representing 2 bits. Compared to OOK, it offers better

spectral efficiency at same sampling rate since each symbol could represent more than 1 bit (which is the case of OOK). Transmitting multiple levels demands higher SNR in the communication system. Figure 2.3 shows 4-PAM and 8-PAM schemes. As M increases,

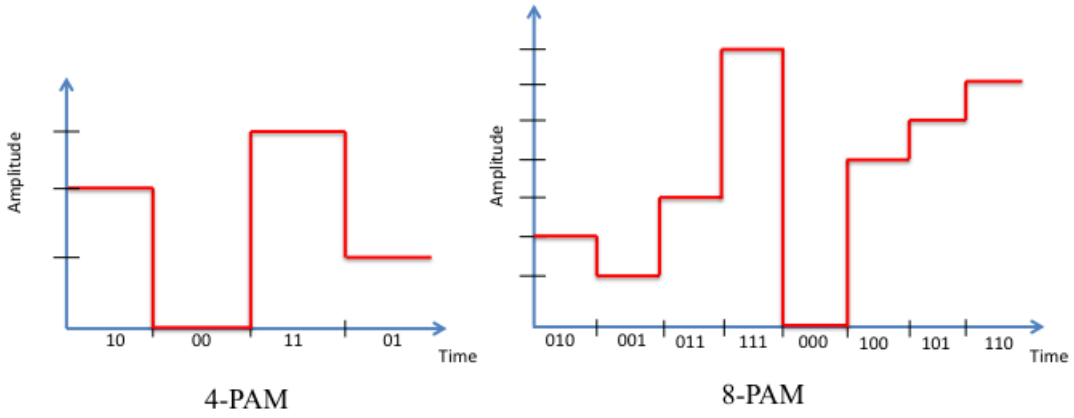


Figure 2.3: 4-PAM and 8-PAM

the system will be more vulnerable to noise since the spacing between each discrete level decreases. To mitigate this the discrete levels have to be spaced apart, which translates to the need for more transmit power and dynamic range. M-PAM is widely used for wired technologies like Mbps and Gbps Ethernet [100]. For VLC, M-PAM modulation scheme can be implemented by generating multiple intensity levels from the LED light source. A PAM scheme supports both unipolar and bipolar signalling, however VLC demands an unipolar scheme. The LED modulation bandwidth which translates to the rise and fall times of the generated optical pulses dictate the quality of the PAM modulated signal. The quality of the PAM transmission can be judged from the eye-diagrams of the received signals. A slower LED response will result in the amplitude level fidelity reducing making it difficult to detect them at the receiver. The non-linear characteristics of the LEDs translate to unequal amplitude spacings which increases error probability as M goes up. Bandwidth limitations can be minimised to an extent by using various equalisation techniques [101]. M-PAM has been well studied for VLC [102, 35, 103, 104, 105] and VLC demonstrators have been reported [106, 107].

2.3.1.4 Orthogonal frequency division multiplexing (OFDM)

The modulation schemes such as OOK and M-PAM discussed so far use a single carrier and manipulate the characteristics of this carrier to transmit the information. There are also other modulation schemes, which uses multiple carriers to transmit information over the same channel simultaneously. OFDM is one of such schemes, which offers high spectral efficiency and is widely used in RF communications and wired communication schemes such as asymmetric digital subscriber line (ADSL). Figure 2.4 compares the fre-

quency domain representation of a single carrier modulation scheme, FDM and OFDM. The carrier signal is modulated by the information signal of a certain bandwidth in single

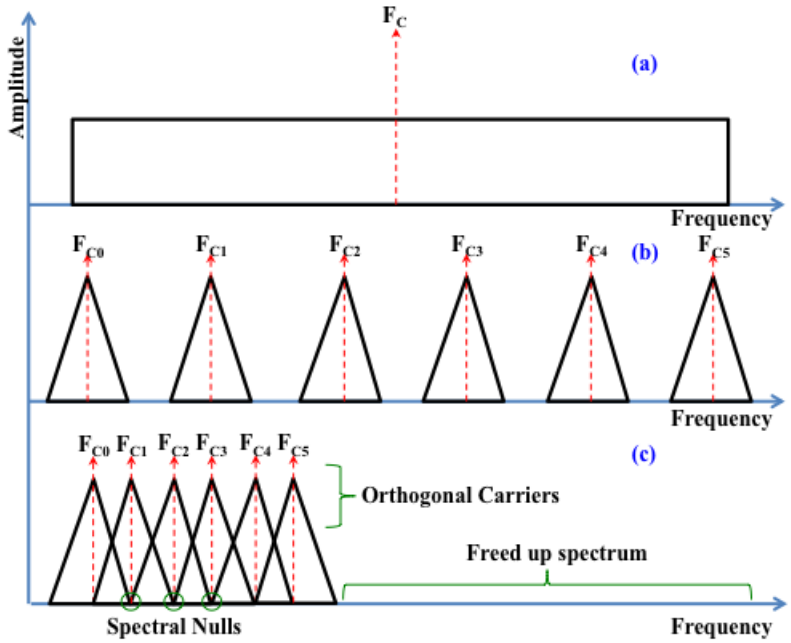


Figure 2.4: (a) Single carrier modulation; (b) FDM; (c) OFDM

carrier modulation. This scheme suffers from effects such as frequency selective fading and crosstalk from adjacent channels, which necessitates the need for guard bands between them. High data rate single carrier systems have a guard band period comparable to symbol periods and thereby spectrum wastage. Conventional FDM employs multiple carriers over the same bandwidth to achieve similar throughput, however carriers must be spaced apart to avoid inter symbol interference (ISI) which is not very spectrally efficient. In OFDM, the available bandwidth is divided into number of sub-carriers, however carriers satisfy orthogonality which means any carrier is not affected by adjacent carriers (no interference from adjacent carriers). From 2.4 it can be seen that for OFDM, the sub-carrier peaks are arranged in such a way that adjacent sub-carrier nulls occur in the same point, thus no cross talk. For orthogonality, an OFDM symbol period should have integer number of sub-carrier cycles.

Figure 2.5 is an OFDM system showing the various blocks involved in transmission and reception. Incoming digital data is split into blocks and each block is modulated with schemes such as PSK or M-QAM, N parallel streams are generated where N represents the number of sub-carriers to be transmitted. The modulated parallel data stream is fed into an inverse fast Fourier transform (IFFT) block, which generates the time domain signal. For each symbol, a cyclic prefix (CP) is added to combat ISI. Since CP samples are copied from the beginning or end of the OFDM symbol itself, adding this to the signal, either at the beginning or end of each symbol does not result in any additional distortion. Prior to transmission, the digital time domain signal has to be converted to the analogue domain.

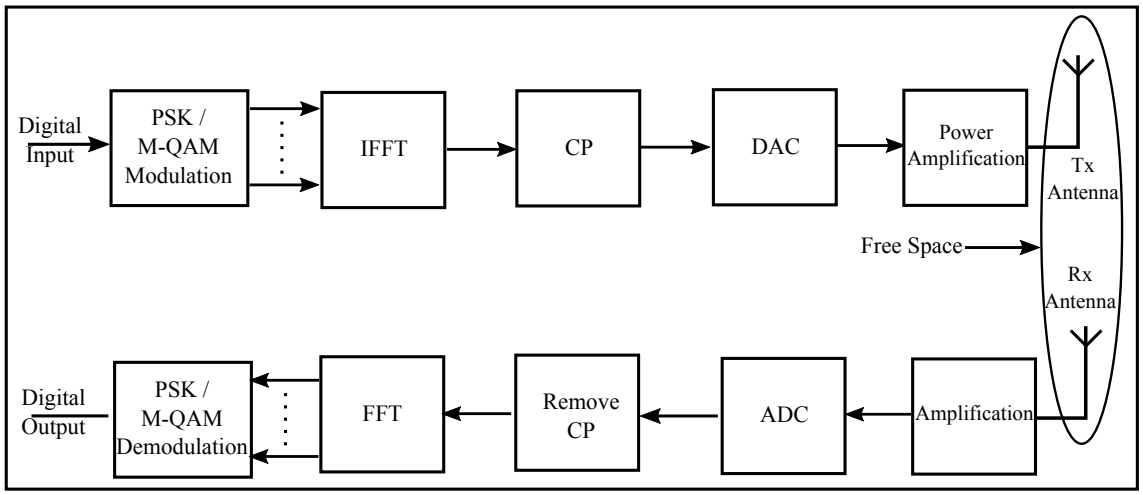


Figure 2.5: Block diagram of an OFDM system

A DAC is employed for this purpose. Characteristics of the DAC which are vital for such a system will be discussed in 2.5.4. The power level of the generated analogue signal is amplified by a power amplifier (PA) prior to transmission. The load to which the amplifier will be driving information depends on the type of communication system. For example, in a RF system, it will be an antenna and for VLC it will be an LED. The received signal is amplified and digitised by an ADC. The CP is removed and a fast Fourier transform (FFT) is performed to recover the PSK or M-QAM symbols, which are further demodulated to generate the original data stream.

IM/DD enforces a few constraints for the modulation schemes used in VLC such as, no usage of bandpass modulation (no frequency up-conversion) enforcing a base-band scheme and real valued unipolar signalling [108]. For a real valued IM/DD system this also reduces the spectral efficiency since only half the sub-carriers can be used to carry data (Hermitian symmetry). These constraints forces OFDM generated signals to be modified appropriately prior to transmission. For VLC, the two flavours of OFDM are DCO-OFDM and ACO-OFDM. DCO-OFDM scheme adds a DC bias to the time domain signal, thus making it suitable for IM/DD, whereas ACO-OFDM clips the negative valued time domain samples. DCO-OFDM is bandwidth efficient since it uses more sub-carriers compared to ACO-OFDM whereas the latter is power efficient since there is no additional power needed to step up the bias of the LED [109]. OFDM offers very high spectral efficiency as shown in 2.4 [21] and immunity to multi path fading.

$$\eta = \frac{\sum_{k=0}^{\frac{N_{fft}}{2}-1} sgn(M_k) log_2 M_k}{N_{fft} + N_{CP}} \quad bits/s/Hz \tag{2.4}$$

where N_{fft} is the FFT size, M_k is the size of the constellation at sub-carrier k, N_{CP} is the length of the CP appended to the OFDM frame and $sgn(.)$ is the sign function. The

bandwidth, B and data rate D of such a system can be calculated as follows [21].

$$B = \frac{1}{2T_S} \quad Hz \tag{2.5}$$

$$D = 2B\eta \quad bits/s \tag{2.6}$$

T_S is the sampling period. By learning the channel properties through channel estimation and there by SNR at different sub-carriers, it is possible adjust the power and modulation order of each sub-carrier increasing power efficiency to the system. Even though OFDM has the advantages mentioned so far, it requires circuitry with high dynamic range to cope with high PAPR of the OFDM stream. PAPR is defined as the ratio of peak power to the average power of time varying signal. The PAPR limitation could be overcome either by clipping the signal or by increasing the dynamic range of the circuitry dealing with the signal [56, 66]. From the perspective of a VLC system, this means increased power consumption while operating the LEDs at high dynamic range, which could also introduce additional distortions due to the non-linear transfer characteristics of the LEDs. Clipping and filtering techniques could reduce the dynamic range requirement in the system at the expense of an increased BER. It is also prone to the effects of frequency and phase offsets. Various VLC demonstrators utilising OFDM have been mentioned in 2.3. Table 2.2 summarises the discussion on the three modulation schemes discussed so far. OOK offers simplicity of implementation at the cost of achievable data rate, whereas OFDM systems are complex to implement but at the same time have high spectral efficiency.

	OOK	PAM	OFDM
Spectral Efficiency	+	+++	+++
Non-linearity immunity	+++	++	+
System complexity	+	++	+++
Multipath immunity	+	++	+++

Table 2.2: Comparison of modulation schemes for VLC

2.4 Light Emitting Diodes

LEDs are semiconductor devices capable of emitting EM radiation in the visible, ultraviolet and infra-red region of the EM spectrum. Although they are P type - N type (P-N) junction devices like silicon diodes, they emit light when forward biased and current passes through the junction. In this section, we will go through history of LEDs and physical phenomenon behind light generation in an LED.

2.4.1 History of Light Emitting Diodes

Light emitted from a semiconductor was first observed by the British engineer Henry Joseph in 1907, while working with Silicon Carbide crystals but the inner dynamics of this emission was not understood. Gallium Arsenide based IR and red emitting devices appeared during the early 1960's. During 1962, Holonyak and Bevacqua reported the first visible spectrum (red) LED [43]. Many companies started mass production of such LEDs intended for displays and other portable electronic devices [97]. Green LEDs based on a Gallium Phosphide semiconductor started to appear by the end of 1960's and early 1970's [97]. Even though blue LEDs based on a GaN semiconductor first appeared during the early 1970's, they were inefficient [97]. Discovery of more efficient doping methods resulted in efficient blue LEDs by the end of 1980's.

2.4.2 LED semiconductor physics

The electronics industry was revolutionised after the invention of semiconductor devices like transistors and diodes. They can be broadly classified into two types, elemental form (e.g. Group IV elements) or compound form (e.g. Group III-V compounds).
Semiconductor materials in the purest form do not conduct electricity as well as conductors like metals. The conductivity of semiconductor materials can be controlled by adding impurity elements into the lattice structure. These impurity elements are called *dopants*. The process of adding impurity elements to the semiconductor material is called doping. When a semiconductor material is doped with an impurity having excess electrons, then it is called a "N-type" semiconductor where negatively charged electrons are the majority carriers. If the dopant lacks electrons in the valence band, the doped semiconductor is called a "P-type" semiconductor where positively charged holes are the majority carriers. The term hole indicates absence of an electron. The basic building block of many semiconductor devices are the P-N junction or semiconductor diode. A P-N junction is formed in a single semiconductor substrate by selectively doping areas with P-type and N-type dopants. It has two terminals, anode (P) and cathode (N). When P-type and N-type mate-

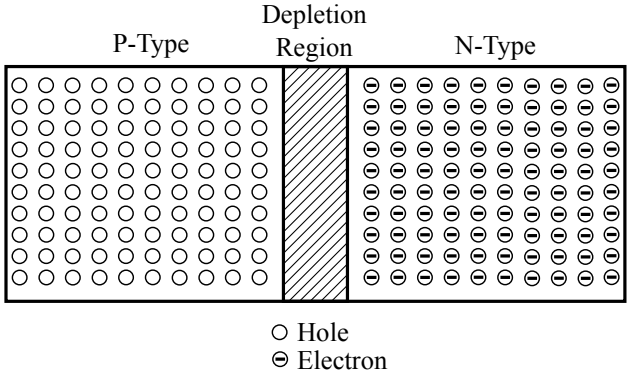


Figure 2.6: A P-N junction with depletion region

rials are joined, at the junction, electrons from N-type material will diffuse into P-region and holes from P-type material will diffuse into N-region, thus forming an area depleted of carriers called the depletion region. The depletion region or space charge region of a P-N junction develops a characteristic potential across it known as the built in potential. This potential can be represented as follows:

$$V_D = \frac{kT}{e} ln \frac{N_A N_D}{n_i^2} \tag{2.7}$$

where N_A and N_D are the acceptor and donor concentrations, n_i is the intrinsic carrier concentration, T is temperature in Kelvin, k is Boltzmann's constant and e is the charge of an electron. To enable current flow through the junction, the built potential must be overpowered. This can be achieved by application of an external voltage across the terminals of the P-N junction, termed biasing. A P-N junction is said to be forward biased when the anode is connected to positive terminal of a voltage source and cathode is connected to negative terminal of a voltage source and vice versa for reverse biased. When the forward bias voltage is greater than built in potential, carriers diffuse through the depletion region i.e. a current starts to flow and carriers recombine. Semiconductors materials can also be classified based on the energy gap between the conduction and valence band. If the conduction band energy minima and valence band energy maxima in the semiconductor have the same crystal momentum, they are said to be *direct band gap* semiconductors. For *indirect band gap* semiconductors, the crystal momentum is not same for the conduction band energy minima and valence band energy maxima.

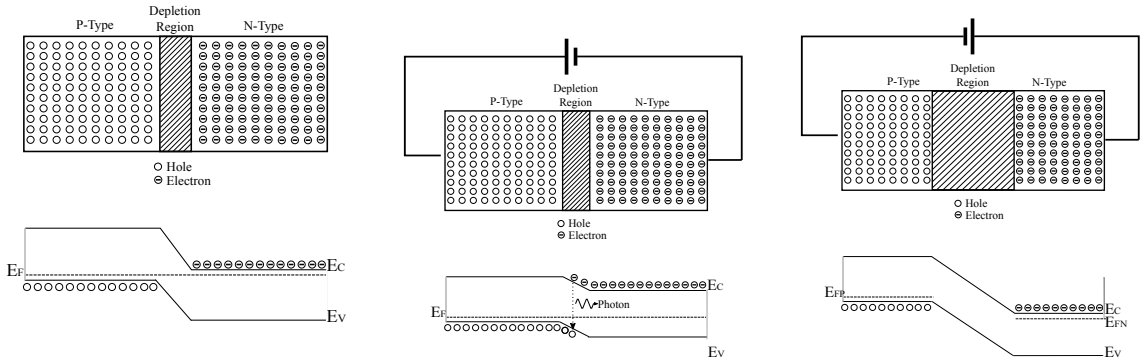


Figure 2.7: Energy bands of P-N junction with no bias, forward bias and reverse bias

2.4.2.1 Carrier generation and Recombination

Semiconductor materials at temperatures above absolute zero have free electrons in the conduction band and holes in the valence band. In equilibrium, they obey the law of mass action i.e. the product of electron and hole concentration is a constant at a fixed temperature, irrespective of the amount of impurities added. For a semiconductor material

with an equilibrium electron and hole concentration of n and p this can be represented mathematically as equation 2.8.

$$np = N_i^2 \tag{2.8}$$

where N_i^2 is the intrinsic carrier concentration [110]. The recombination of holes and electrons happens without external stimulus due to thermal energy. However in equilibrium the rate of carrier generation and re-combination are equal. An external stimulus like the application of voltage results in more carrier generation. As the concentration of carriers increases, the rate of recombination also increases, this can be explained using the bimolecular rate equation[97] given below (equation 2.9).

$$R = Bnp \tag{2.9}$$

where R is the rate of recombination, B is the bimolecular recombination coefficient, n and p are the total electron and hole concentration respectively. Electrons from the conduction band lose energy during recombination. The lost energy is expelled as photons in the case of *radiative recombination*. Radiative recombination is possible only if the semiconductor is direct band gap type. Generated photons will have energy proportional to the band gap, which means the wavelength of light generated will be proportional to the band gap energy difference. An electron in the conduction band of an indirect band gap semiconductor has to go through an intermediate state before recombining with a hole in valence band there by emitting phonons (lattice vibrations), which increases lattice temperature. This is *non-radiative recombination*. For LEDs to generate light, radiative recombination is required, however it is not possible to reduce non-radiative recombination to zero. Great effort is given in the LED design process to reduce non-radiative recombination mechanisms in the semiconductor.

2.4.3 Electrical and Optical characteristics

Since LEDs are P-N junction devices, they have similar electrical characteristics like other P-N junction devices. The electrical characteristics of P-N junction devices were first studied in detail in [111] by William Shockley. The Shockley equation (2.10) given below relates the applied voltage, V and generated current, I in a P-N junction device.

$$I = I_S(e^{(eV/kT)} - 1) \tag{2.10}$$

where I_S is reverse bias saturation current given by the following equation (equation 2.11)

$$I_S = eA\left(\sqrt{\frac{D_p}{\tau_p}}\frac{n_i^2}{N_D} + \sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_A}\right)e^{e(V-V_{TH})/kT} \tag{2.11}$$

where A is the P-N junction cross sectional area, D_p and D_n are hole and electron diffusion constants, τ_p and τ_n are hole and electron minority carrier life times. The voltage-current characteristics (I-V characteristics) of an LED when forward biased is shown in figure 2.8. A P-N junction device starts conducting when it is forward biased and the applied bias

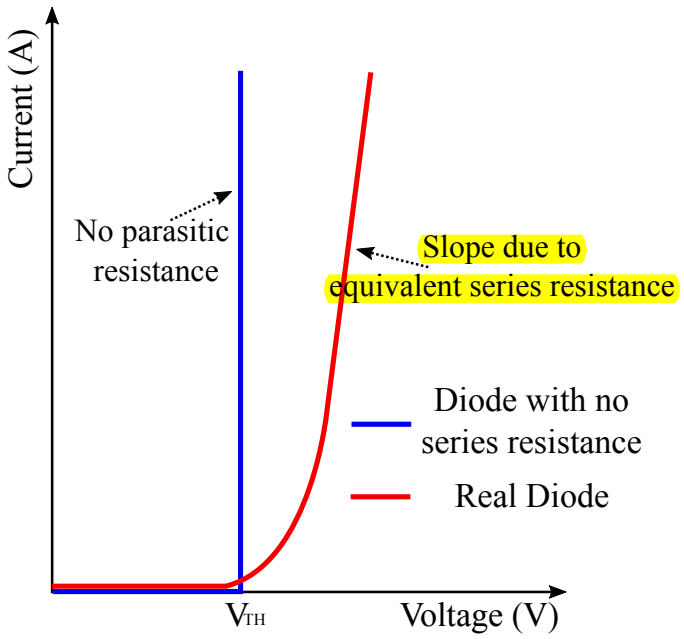
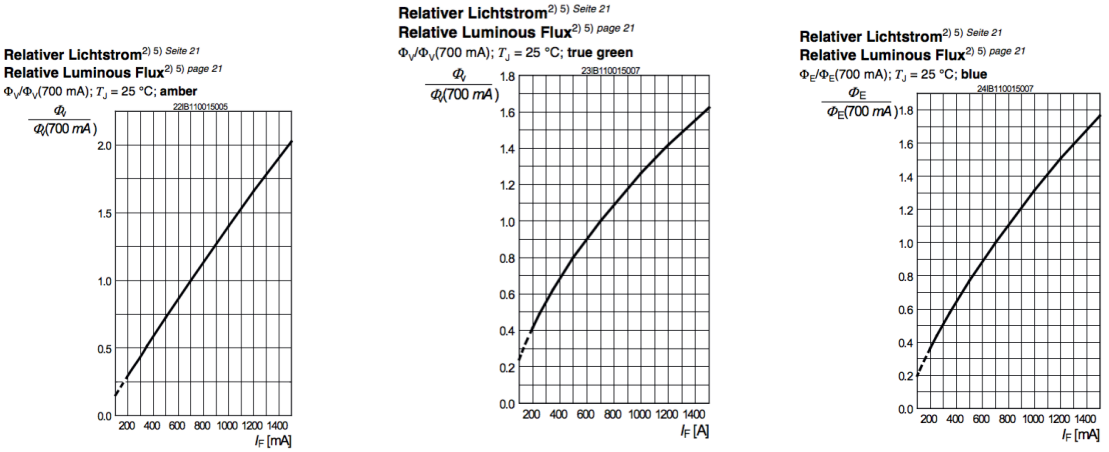


Figure 2.8: I-V curve of a an ideal diode and real diode

voltage exceeds the turn on voltage V_{TH}. The V_{TH} of the LED depends on the band gap of the semiconductor material used. The amount of photons coming out of the LED device is subject to various efficiencies associated with the device described below. External quantum efficiency (EQE) of an LED is the ratio of total number of photons emitted into the free space to the total number of electron-hole pairs injected into the device from the external source per second. EQE depends on two other efficiency factors namely internal quantum efficiency (IQE) and extraction efficiency [97]. IQE is the ratio of number of photons emitted from the active region of the LED to the total number of electron-hole pairs injected into the LED per second whereas extraction efficiency is the ratio of total number of photons emitted into the free space to the total number of photons emitted from the active region. A linear transfer characteristic from input current to output optical power is preferred for VLC to prevent distortions in transmitted signals. Even though electrical to optical conversion is often assumed to be linear [112], it is not always the case as shown by the current to optical power (I-L) output characteristics from a commercial LED in figure 2.9, where green and blue LEDs have a visible non-linear current to optical output.



(a) Red **(b)** Green **(c)** Blue

Figure 2.9: Current to Light output from Red, Green and Blue (OSRAM OSTAR LE-ATB-S2W)

2.4.3.1 LED parasitics

LEDs have parasitic components which alter their characteristics from the ideal behaviour. The prominent parasitics in the case of a P-N junction device are the equivalent series resistance (R_S), junction capacitance (C_J) and diffusion capacitance (C_D). The effect of equivalent series resistance (R_S) can be seen in the I-V characteristics (figure 2.8) as the gradual slope after turn on. Higher R_S translates to more electrical power being wasted in this resistor therefore less power is converted to optical energy. The junction capacitance (C_J) arises due to the minority carriers concentrated in the depletion region. This could be thought of as a capacitor with positive plate formed by P-type semiconductor, negative plate formed by N-type semiconductor and the depletion region acting as the dielectric of the capacitor. This component become more prominent as the P-N junction is reverse biased, thereby widening the junction. Thus the role of the junction capacitance is not prominent during the forward biased operation. Junction capacitance depends on the applied voltage across the LED and reduces as the applied voltage increases. When the P-N junction is forward biased the depletion width reduces as majority carriers cross over the junction to recombine. The concentration of carriers in the junction before recombination is equivalent to a capacitance, known as diffusion capacitance (C_D). Diffusion capacitance dictates the modulation bandwidth of the LED [97].

2.4.4 μLEDs

μLEDs are a type of LEDs whose physical dimensions and power output capabilities are less than OTS LEDs. Compared to the OTS LEDs they have a higher modulation bandwidth [113, 64] owing to the smaller size and higher current densities [113]. Some recent publications indicate they could reach modulation bandwidths close to 1 GHz [64].

2.5 LED Driver circuits

The global LED driver market targeting lighting applications is expected to reach $ 20 billion by 2021 [114]. There are also driver circuits available for driving LEDs coupled into optical fibre (OF)s for high speed wired optical communication. However at the time of this work, a driver dedicated for both VLC and ambient lighting was not present. To realise such a driver circuit system, various aspects of a VLC system should be understood in detail. The LED characteristics are the most important set of parameters to be analysed and understood before the circuit architecture and method of implementation is finalised.

2.5.1 Drive method: Voltage/Current

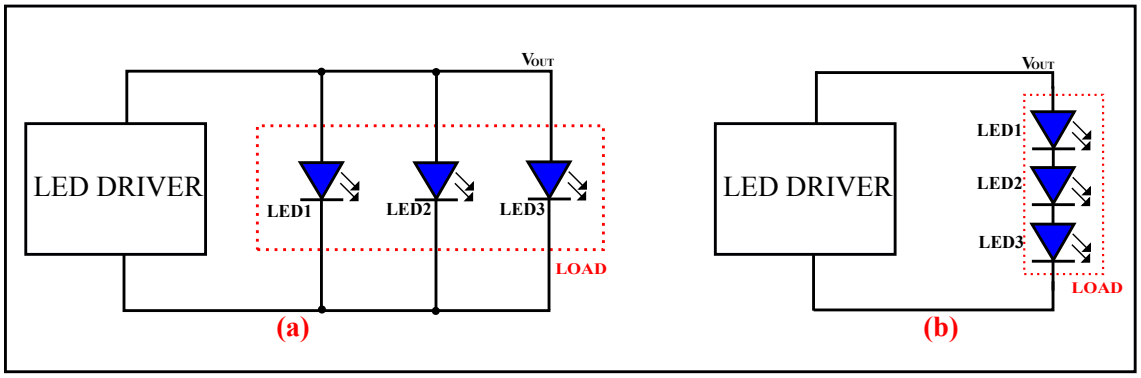


Figure 2.10: (a) Voltage mode drive (b) Current mode drive

LEDs drivers can be broadly classified into two types namely voltage mode drivers and current mode drivers as shown in figure 2.10.

2.5.1.1 Voltage mode drive

From 2.4.3 we have seen that LEDs have an exponential voltage to current relationship. After the turn on voltage, the output current rises exponentially for a change in the input voltage. For lighting applications, flicker-free constant light output is preferred. In constant voltage mode drive, the voltage across the LEDs is held constant, which in turn results in a fixed current through them and therefore a fixed output optical power. Usually lighting fixtures will have more than one LED to provide more ambient light. Even though the same LEDs are used in such fixtures, they do not have similar characteristics as their V-I and L-I curves will be mismatched across the various LED samples. This arises due to various reasons such as imperfections added while manufacturing, ageing due to operation and temperature. In voltage mode drive, even though all the LEDs have same voltage across them, mismatch in their characteristics results in variations in output optical power and wavelength. This is not desired. However this drive scheme also has

advantages such as to drive a number of LEDs connected in parallel, there is no need to increase the drive voltage, which relaxes driver circuit design.

2.5.1.2 Current mode drive

In current mode drive, LEDs are arranged in a series fashion as shown in figure 2.10. In this drive scheme, each LED has the same current flowing through it. The V-I characteristic mismatches can be avoided in this scheme. However, the mismatches in the I-L characteristics are still present. To drive a string of LEDs a higher voltage has to be generated by the drive circuit, depending on the number of LEDs in the string and the current needed to flow through them. If one element in the string malfunctions, the whole string will be rendered useless in this drive scheme. To avoid this, a number of strings can be used together in parallel, which is a hybrid scheme of voltage mode and current mode drive scheme. In both schemes, the current flowing through the LEDs is limited by passive circuitry (resistor) or active circuitry (current monitoring and feedback).

2.5.2 Driver topologies

Active circuit topologies proposed for driving LEDs include popular switched regulator variants from both the DC-DC and alternating current (AC)-DC domain. These include buck, boost, buck-boost and fly back converters. Dimming of lights is an added feature in ambient lighting, this can be achieved by reducing the average current flowing through the LED.

2.5.2.1 Buck converter driver

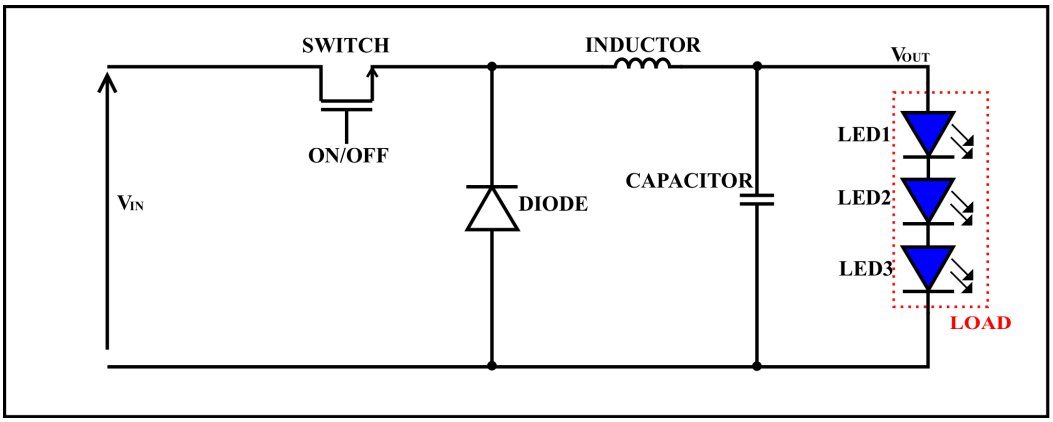


Figure 2.11: Basic circuit diagram of a buck converter.

A buck converter is a switching DC-DC converter whose output voltage is less than the input voltage. The maximum output current is normally higher than the input current thus keeping the power constant from input to output including the losses in the converter.

They have typical power conversion efficiencies > 90%. A basic diagram of a buck converter is shown in figure 2.11. It consists of a switching device (metal oxide semiconductor field effect transistor (MOSFET)) between the input and the inductor, a diode and a capacitor across the output node. The basic working principle is that, when the switch is turned on, it connects the input voltage to the rest of the circuit. The diode will be reverse biased hence all the current has to flow through the inductor to the capacitor and load. The inductor during this phase stores energy as a magnetic field. When the switch is open, the inductor is no longer connected to the input. To maintain the current through it, a reverse voltage is developed across it, which can be quantified by the equation 2.12

$$V = -L\frac{di}{dt} \tag{2.12}$$

The reverse voltage results in the diode becoming forward biased and the current path is kept closed. Even though the switch turn ON/OFF cycle results in a large voltage swing at the inductor input, the output voltage does not have this large voltage variation and it has only a minimal ripple voltage. The capacitor at the output node helps to reduce the ripple voltage, since it can source instantaneous current to the load whenever needed. The output voltage of the buck converter can be represented by the equation 2.13

$$V_{OUT} = V_{IN}\frac{T_{ON}}{T} \tag{2.13}$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, T_{ON} is the ON time of the switch and T is the switching period. T_{ON}/T represents the duty cycle of switching. By varying the duty cycle the output voltage can be controlled. It can be seen from this equation that the output voltage does not depend on the values of the components used such as inductance and capacitance. However the switching frequency dictates the size of these components. A precise control loop is usually implemented to sense the output voltage/current and vary the duty cycle of the switch as required. Usually pulse width modulation (PWM) is implemented to achieve this. A single LED or a string of LEDs could be connected at the output node of the buck regulator. The output current can be sensed using a resistor inserted into the current path. The dimming feature present in LED drivers samples the voltage across the resistor to generate the PWM signal to vary the duty cycle of the switch control signal and therefore output voltage and current.

2.5.2.2 Boost converter driver

In the boost type converter, the output voltage is higher than the input voltage but the output drive current is less than the input current levels to keep the power constant. Similar to buck converters, boost converters owing to the switching architecture have an efficiency > 90%. A circuit diagram of a boost converter is shown in figure 2.12. The circuit has

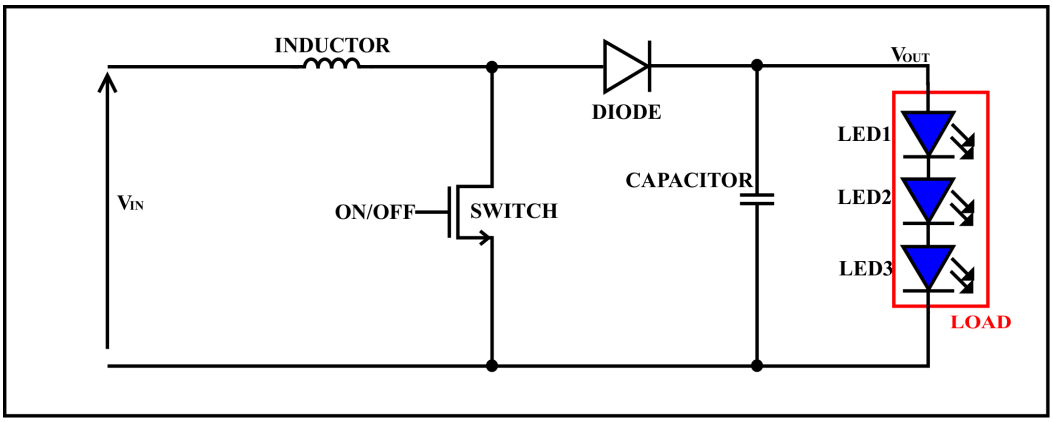


Figure 2.12: Basic circuit diagram of a boost converter.

similar components to a buck converter, however they are arranged differently. The inductor, diode and the switching transistor have changed positions. When the switch is turned ON for the first time, the inductor is placed across the input terminals causing a current to flow through it, which results in the inductor storing the energy. No input current flows through the load during this phase of operation. When the switch is turned off, the impedance seen by the inductor switches from a low impedance switch to the relatively high impedance output side (capacitor and load). This results in a drop in current, which triggers the inductor to generate a voltage of the reverse polarity according to 2.12. Now the voltage seen by the load and the capacitor is the sum of input voltage and the voltage across the inductor, assuming an ideal diode, which indicates that the output voltage is higher than the input voltage. The capacitor is charged to the higher voltage during each OFF cycle of the switch and inductor is charged during the ON cycle. In the next switch ON cycle, when input is isolated from the output, the capacitor will be able to source the load current. The output voltage of the boost converter can be defined by 2.14

$$V_{OUT} = \frac{V_{IN}}{1 - \frac{T_{ON}}{T}} \tag{2.14}$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, T_{ON} indicates the ON time of the switch and T indicates the switching period. Similar to the buck converter, the output voltage does not depend on component parameters. A control loop implemented to sense the output voltage/current is used to control the ON/OFF time of the switch and thereby achieving a closed loop system. Boost converters are suitable for driving LED strings due to their higher output voltage.

2.5.2.3 Buck-Boost converter driver

A buck boost converter driver can operate in the buck mode where the output voltage is less than the input or boost mode where output voltage can be higher than the input.

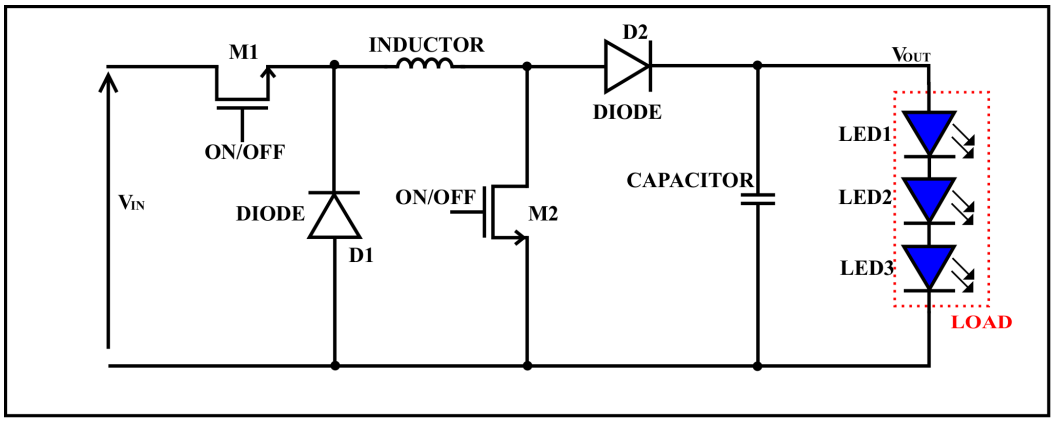


Figure 2.13: Basic circuit diagram of a buck-boost converter.

This type of switching regulator driver can thus operate at a wide voltage range. The circuit diagram of a basic buck-boost converter is shown in figure 2.13. It consists of two transistor switches (M1, M2), two diodes (D1, D2), an inductor and a capacitor. The switches are controlled by control logic not shown in this diagram. The control logic can decide whether the circuit is operated in buck mode or boost mode. Buck mode operation is dictated by M1, D1 and D2 and boost mode is defined by M1, M2 and D2. The inductor and capacitor are utilised in both modes. In buck mode, M1 is either ON or OFF and M2 is OFF. When M1 is ON, it energises the inductor, charges the capacitor and provides current to the load as well. When M1 is OFF, the inductor tries to keep the current constant by generating a reverse polarity voltage, which forward biases D1 enabling the return current path. The capacitor provides instantaneous current to the load thereby smoothing the output voltage. An additional diode drop is expected here since D2 is in the path during both the ON and OFF states of M1. In boost mode, M1 is ON all the time. Turning on M2 results in the inductor storing energy in the magnetic field. When M2 is turned OFF, the inductor action results in a higher voltage across the load and capacitor (sum of input voltage and voltage across inductor). Various commercial incarnations of the above said structures are widely available for lighting applications. Most of them also have the capability for dimming the LED lamps. PWM is the choice of dimming method for many of the commercially available LED drivers.

2.5.3 VLC LED drivers

Work has been done into the use of the topologies mentioned so far for enabling VLC alongside lighting. Electronic circuitry has been realised utilising both discrete components and integrated circuit technology. [115] implements a high efficiency buck LED driver with discrete components capable of VLC up to 2 Mbps. It supports dimming using PWM and uses variable pulse position modulation (VPPM) scheme for data transmission. A resonant LLC converter driver capable of VLC is presented in [116]. This

design utilises discrete components and it is capable of delivering 80W to the LEDs with the ability to adjust the average output current level for dimming. Data transmission up to 50 Kbps has been demonstrated. The drive schemes discussed so far uses discrete components to realise the LED driver. Realising the circuitry using discrete components requires a PCB are and therefore bulkier than integrated circuit solutions. Losses in such incarnations are more due to switching and conduction losses in various discrete components.

A boost converter based integrated LED driver capable of data transmission is discussed in [82]. Data rates up to 266 Kbps were achieved in this work with a peak power efficiency of 92%. The boost converter enables driving of a string of LEDs. It also supports multi-level dimming. The Institute of Electrical and Electronics Engineers (IEEE) 802.15.7 baseband logic is included in this chip, which enables either OOK or VPPM schemes for modulating the light intensity. A switching transistor is embedded in the chip, which reduces the external component count, however a few passive components are needed externally. The same group has also published an integrated driver for a LED micro-display capable of transmitting into free space [117]. μLED pixels are used to create an active display matrix of 400 x 240 pixels from a single GaN substrate. The integrated device is capable of transmitting data using OOK. Data rates up to 1.25 Mbps have been reported in this work. [76] discusses an integrated CMOS-GaN μLED driver capable of 512 Mbps using OOK. The bandwidth of commercial LEDs is a limiting factor in the performance of a VLC system. The bandwidth of these devices is dictated by the parasitic components such as the depletion capacitance of the LEDs. A slower extinguishing time of the LEDs can be linked to these parasitics. [98] proposes a driver structure where the junction capacitance is reduced by removing extra carriers present at the junction and therefore a faster turn-off time. This system reports a 38% increase in achievable data rate by sweeping out the carriers.

2.5.3.1 LED drivers: Limitations

Table 2.1 lists the key VLC demonstrators evolved over time. The generic trend that can be seen from the table is, most of the high speed VLC demonstrators generate the digital data to be transmitted in a computing platform and feed it into an AWG. Commercially available AWGs are used for this purpose and they have memory to hold the digital information stream, high speed DACs to convert the digital data to analogue, capable of operating at high speeds (Gsps). Usually the outputs of AWGs have fixed voltage swing and limited current capability. A power amplifier is used post AWGs to boost the signal power and appropriate DC bias is added to the signal before the LED. In [21], a 3 Gbps μLED VLC link was achieved by using a commercial AWG, N8241 [118], which supports sampling rates up to 1.25 Gbps and 15 bits resolution per channel. However the maximum output voltage specified for this device while driving a 50Ω impedance is 1 V (peak to peak), which translates to a maximum current drive of 20 mA. Comparing with the cur-

rent capability of LEDs (usually in hundreds of mA) this is low, which in this experiment is compensated by using a PA and separate DC biasing for the LED. [118] consumes up to 100 Watts during operation and thus a power inefficient scheme to drive an LED for VLC. Overall power efficiency of the similar schemes will be lower since it involves other components such as discrete PA, DC biasing etc. High power efficiency is critical since it is environmental friendly and reduces operating cost. Device footprint is another key factor crucial for a wireless communication technology like VLC. Since it is expected to augment RF based communication systems, which is widely used in consumer and other communication equipments which are portable, smaller device foot prints are preferred. Physical dimension of the AWG used in [21] is $422mm \times 213mm \times 89mm$ and it weighs $5.6Kg$, which clearly rules them out to be used for any consumer friendly wireless communication application. Capacity of VLC links could be improved by using techniques such as WDM which uses multiple LEDs as demonstrated in [83, 65] and many other similar demonstrators. Most of the WDM demonstrators use RGB type LEDs since they could also produce ambient white light at the same time transmitting three separate data streams. Such schemes were able to offer VLC links up to 14 Gbps (Table 2.1). To realise WDM schemes multiple drive channels are needed which means more AWG channels and thereby increased driver footprint. For technology demonstrators at laboratories aiming to experiment with different types of LEDs, modulation schemes, colour converters etc. such large drive circuitry is acceptable. However, circuit miniaturisation whilst maintaining power efficiency and modulation bandwidth is key for commercialisation of the VLC technology. Customised driver circuits using discrete electronic components can be used to realise LED drive circuitry capable of IM. Discrete incarnations of VLC drivers can be found in [69, 119, 29, 28]. [119] is able to achieve up to 80 Mbps using a commercial white LED and a discrete driver. An IR LD based system designed using discrete components is presented in [69], which uses a commercial laser driver and associated circuitry achieving 1.25 Gbps. Driver circuit foot print is smaller compared to using a commercial AWG while realising a Gbps OWC link. [29] realise a WDM VLC link with maximum data rate per channel up to 622 Mbps. The LED driver used in this circuit is a current mode logic driver realised using discrete component. Another publication [28] realise an LED driver capable of data rates up to 460 Mbps using discrete components. All the VLC demonstrators using discrete components discussed so far have smaller area footprint compared to the AWG based schemes mentioned earlier and some of these demonstrators were able to use simple passive circuit components to incorporate functions such as equalisation. However they were unable to utilise spectrally efficient modulation schemes such as OFDM or PAM since they did not utilise digital circuits to generate data and DAC to convert them to analogue domain. So far we saw that high speed VLC demonstrators use either AWGs or discrete components to realise LED drivers, where the former scheme offers high speed link at the expense of power and area and the latter offers better power

efficiency and area metrics. For many applications such as consumer electronics, IoT etc. further savings in area and power consumption is required whilst maintaining data rate and link distance. Many of the circuit functions (signal processing, DAC, etc.) required to realise a LED driver can be integrated into a single circuit by using circuit integration technologies such as CMOS. Since its inception, CMOS technology has become the most widely used technology for circuit miniaturisation due to low cost, high power efficiency, high operating speed and technology scaling. LED drivers for lighting have been realised using CMOS technology [120]. They are either not suitable for VLC or have lower data transmission performance compared to the high speed VLC implementations discussed in this section since they do not have the required additional circuitry to take high speed data and intensity modulate the LEDs. A few of the integrated solutions published so far [82, 76] are capable of using simple modulation schemes such as OOK or VPPM therefore resulting in under-utilisation of the available bandwidth.

Any digital communication system utilising multi-level or multi-carrier modulation uses digital circuitry such as a microprocessor or digital signal processing (DSP) to generate modulated digital signals. Transmission happens in the analogue domain, which points to the need for DACs. A typical wireless transmission system is shown in 2.14. The DAC converts the digital signal to the analogue domain for transmission. Power

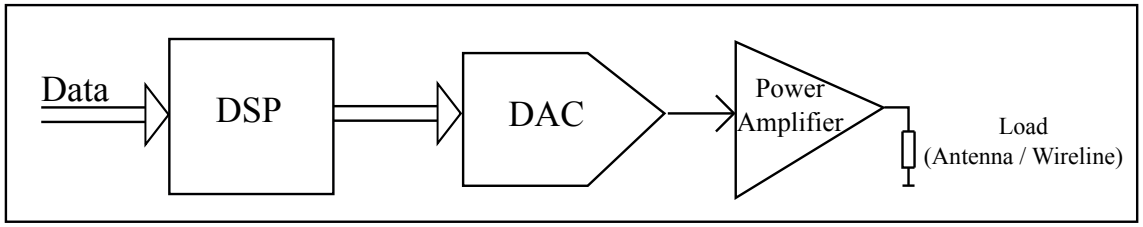


Figure 2.14: Circuit blocks in a digital communication system

amplification of the signal is needed prior to transmission since the DAC does not have enough output power to drive the antenna or a cable in the case of a wired transmission system. Such transmission systems are widely used for applications such as wireless local area network (WLAN), ADSL etc. These systems have been shown to reach transmission speeds from mbps to gbps [121, 122]. Similar system could be used for VLC as well. Unlike wired or RF communication links, in VLC the final stage has to drive LEDs, whose characteristics are different cables or antennae.

2.5.3.1.1 Limitations of power amplifiers (PAs) Both wired (eg. ADSL) and wireless (eg. RF) communication systems uses PAs [123, 124, 125] at the last stage of the electronic circuitry to deliver sufficient amount of electrical power to transmit the signal through cables or antennae. PAs stages are also used in audio systems to drive the loud speakers. Different types of PA stages are in use to satisfy the application needs. They can be broadly classified into continuous (Class A, B, AB, C) and switched (Class D, E, G, H)

types. However PAs have disadvantages which makes them not the primary candidates for drive stages in VLC systems. Major disadvantages are listed and explained below.

- **Power Efficiency**: A major draw back of the PAs is low power efficiency compared to the DC-DC converter type drive stages discussed in section 2.5. For example, a class-AB type power amplifier could only reach maximum efficiency of 24% and a class H could reach an ideal efficiency of 58% and practical efficiency of 27% [126, 125]. Power efficiency is key to an LED based OWC system which is expected to have wide install base.

- **Non-linearity and PAPR**: To increase the achievable data rates, spectrally efficient modulation schemes such as OFDM must be used. However, OFDM, since its a multi-carrier modulation scheme has non-uniform signal envelope levels and therefore high PAPR [56]. Non-linearity in the PAs results significant distortion while amplifying signals with non-uniform envelopes [127, 128]. High linearity of the amplification stage is also crucial to prevent occurrence of intermodulation distortion while passing a multi-carrier modulated signal.

These negative aspects of the PAs indicate that there is space for improvement in the driver circuit architecture while designing for VLC. From the discussion so far, it is evident that there exists highly power efficient, low speed, VLC compliant ambient LED drive schemes using switching regulator architectures. There also exists bulky and less power efficient but faster driver schemes using discrete components or laboratory bench equipment such as AWG. For wide spread acceptance and large scale deployment of VLC systems, the LED driver should have following characteristics

- **High datarate**
- **High power efficiency**
- **Support for multiple modulation formats**
- **Support multiple types of LEDs**
- **Realisable in popular integration technology such as CMOS**

The communication system shown in figure 2.14 can be modified to drive LEDs for VLC. We demonstrate that a DAC can be used to drive the LEDs, thereby removing the low power efficient PA stage. DACs have certain inherent advantages which make them suitable to drive LEDs. DACs have reported up to giga samples per second operating speeds [129, 130] whilst maintaining linear output range up to 12 bit resolution [131]. DACs have also been reported in CMOS technology to drive current output [132, 130] to the loads which can be faster compared to voltage output since it is easier to realise current

sources and switch the current paths in CMOS technology. LEDs have more linear current to light output relation (over wide range) than voltage, thus making current drive option better. Current mode drive also makes it easier to generate discrete light levels proportional to the input digital code. This type of drive scheme where a current DAC driving LED for VLC whilst maintaining linear range of operation over whole input range and bandwidth is new. Before discussing this scheme in detail, a short introduction to the different types of DAC circuit topologies, merits and performance criteria are discussed in next section.

2.5.4 Digital to Analogue Converters

DACs are a type of data converter circuit, which converts the discrete time and amplitude digital data into continuous time and amplitude analogue signals. The core of the electronic systems are digital in nature for error free information processing and easy data manipulation. DACs are an important part in any modern electronic system which has to represent information in natural quantities such as voltages or currents. For example, in a digital communication system, the DAC converts the incoming digital information into analogue representations which can be transmitted using an antenna or cable. In a digital video processing system, the DAC converts the digital video stream to an analogue voltage or current, so that it can be displayed.

2.5.5 Ideal DAC

Understanding the functioning of a DAC without any circuit or system non-ideality is an important step. Consider a DAC system show in figure 2.15. The DAC has a N-bit wide

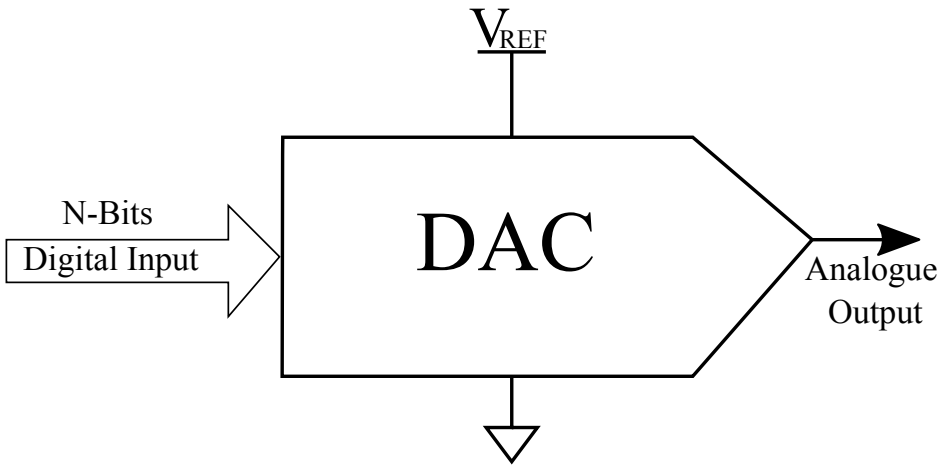


Figure 2.15: An ideal DAC with input and output

digital input word, which determines the *resolution* of the DAC. The higher the resolution, the more accurate is the DAC in representing the analogue signal. The output of the DAC

represents the analogue equivalent of the digital input word. The DAC generates the analogue output based on the applied analogue reference voltage V_{REF}. The accuracy of the reference voltage is an important factor affecting the performance of the DAC. The expression for the analogue output of the DAC can be written as below [133]

$$V_{OUT} = V_{REF}\left(b_1 2^{-1} + b_2 2^{-2} + ... + b_N 2^{-N}\right) \tag{2.15}$$

b_N is the least significant bit (LSB) and b_1 is the most significant bit (MSB) in the digital word. A change in LSB corresponds to smallest analogue output variation possible by the DAC. This voltage change is given by,

$$V_{LSB} = \frac{V_{REF}}{2^N} \tag{2.16}$$

Equation 2.15 can be represented graphically as shown in 2.16.

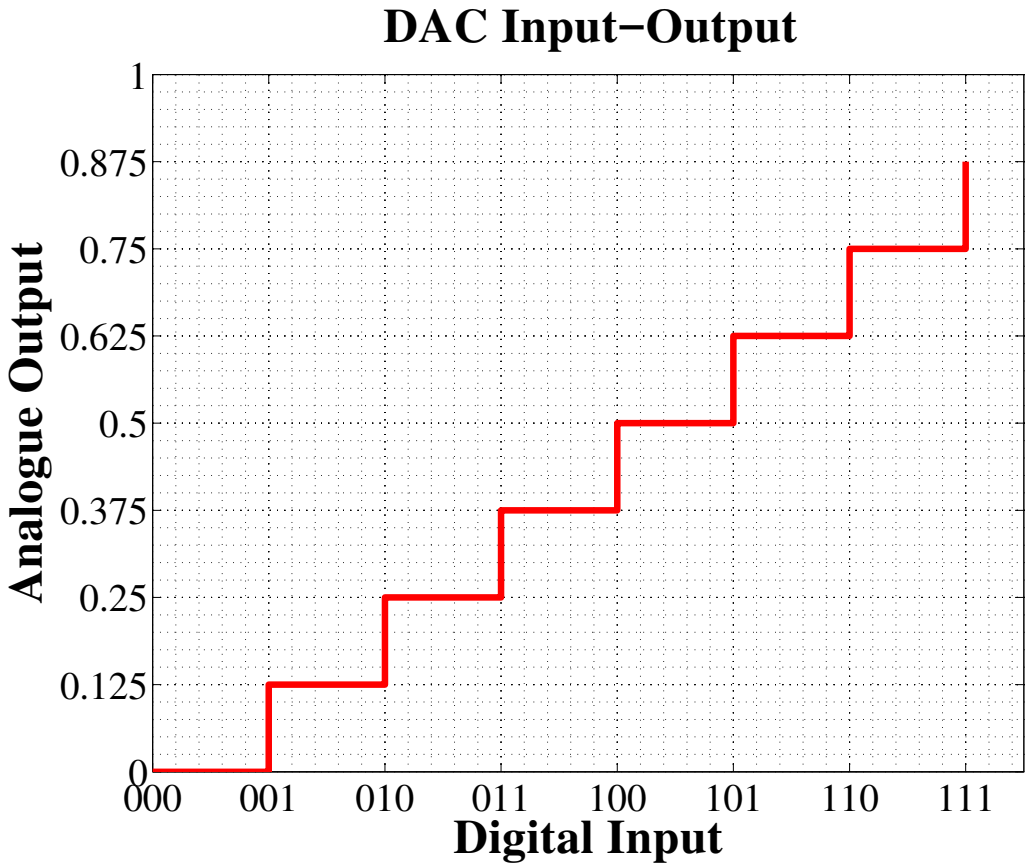


Figure 2.16: DAC Input Output characteristics

2.5.6 DAC Static Parameters

2.5.6.1 Resolution

The resolution of a DAC is defined as the number of distinct analogue levels (voltage or current) which correspond to the different digital words [133]. If the width of the input digital word is N bits, then the analogue output will have 2^N different values. A higher resolution could be interpreted as an indication of a more accurate representation of real world signal but it also increases circuit complexity at the same time. For a DAC used in communication system, higher the resolution, the more spectrally efficient system could be realised. For example, in an OFDM transmission scenario, this indicates better representation of the time domain waveform (less quantisation noise and distortion) and for a system transmitting in PAM, more levels could be represented there by increasing the spectral efficiency and data rate.

2.5.6.2 Full scale

The full scale of a DAC is defined as the difference between analogue output for the largest digital word and analogue output for the smallest digital word[134].

2.5.6.3 Conversion rate

The sampling rate or conversion rate (F_S) of the DAC is defined as the rate at which the digital input is converted to an analogue output. Obeying the Nyquist-Shannon sampling theorem [135],the usable bandwidth of the output analogue signal extends to $\frac{F_S}{2}$. The DAC circuitry will have a clock signal input which determines the conversion rate of the system. A higher sampling rate translates to increased bandwidth and thereby data rate for communication systems.

2.5.6.4 Offset Error

The offset error of a DAC is defined as the analogue output value corresponding to a digital input of 0. For an ideal DAC, the offset error should be 0, but circuit non-idealities may cause this value to be greater than or less than equal to 0. Offset error is measured in LSBs and can be represented by equation 2.17

$$E_{offset} = \left.\frac{V_{out}}{V_{LSB}}\right|_{Input=0} \tag{2.17}$$

This error can be calibrated out and it does not affect the linear operating range of the DAC.

2.5.6.5 Gain Error

The gain error of the DAC can be defined as the difference between the actual output and the ideal output at the full scale input after the offset error is corrected. Gain error is expressed in LSBs and can be expressed as shown in 2.18.

$$E_{gain} = \frac{V_{out}}{V_{LSB}}\bigg|_{Input=Fullscale} \tag{2.18}$$

It is possible to calibrate out both gain error and offset error of the DAC.

2.5.6.6 Differential and Integral non-linearity

The differential non-linearity (DNL) error represents the difference in output analogue step size from the ideal LSB output step. In an ideal DAC the output variation when the input is changed by one digital code corresponds to the ideal LSB step, whereas in real DACs the output step may not be equal to ideal LSB step due to circuit imperfections or temperature variations. DNL is represented in units of LSBs. Mathematically DNL can be represented as the expression given by 2.19.

$$DNL_{X_N} = \frac{V_{X_N} - V_{X_{N-1}} - V_{LSB}}{V_{LSB}} \tag{2.19}$$

where DNL_{X_N} is the DNL at digital input X_N and V_{LSB} is the ideal analogue output step change.

Integral non-linearity (INL) represents the deviation of the DAC output characteristics from a straight line characteristic or ideal characteristic after calibrating out the offset and gain errors. It can also be said that, the INL of a DAC at digital input X_N is the sum of the DNLs up to X_N. This can be expressed mathematically as 2.20.

$$INL_{X_N} = \sum_{i=0}^{N} DNL_i \tag{2.20}$$

where INL_{X_N} is the INL at digital input X_N and DNL_i is the DNL at digital input code X_i. Effect of DNL and INL in a DAC are studied using a simple model and this is described in section 2.5.8.

2.5.6.7 Monotonicity

Monotonicity implies that the DAC output increases when the DAC input code increases. Certain DAC architectures ensure monotonicity by design. If the DNL of the DAC is less than 1 LSB, then the DAC will be monotonic.

2.5.7 DAC Dynamic characteristics

The dynamic performance of the DAC is important for any communication system which utilises it.

2.5.7.1 SNR

The SNR of a DAC can be defined as the ratio of the power of the full scale fundamental tone to the power of the in band noise components.

2.5.7.2 Glitch performance

Glitches are unwanted signal transitions that happens at the output during input change. Glitches occur in the output of the DACs due to capacitive effects or switching imperfections. For DACs used in communication systems, glitches have a lesser effect in performance compared to other applications such as audio or video processing.

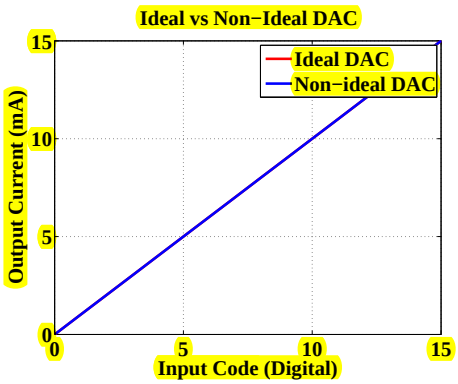
2.5.7.3 Spurious Free Dynamic Range

Spurious free dynamic range (SFDR) is the ratio of the root mean square (rms) value of the signal to the rms value of the worst spurious signal. The spur does not have to be a harmonic of the primary signal. Higher SFDR is required especially for modulation schemes such as OFDM, else individual subcarriers in the OFDM stream could be affected by the harmonics resulting in intermodulation distortion and there by increase in BER.

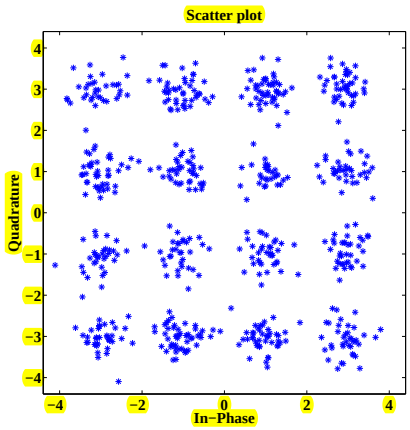
2.5.7.4 Multi-tone power ratio (MTPR)

A MTPR test is performed by feeding the DAC with a time domain waveform comprising of most of the frequency components in the band of interest except a few. The missing frequency components or tones will appear as notches in the frequency domain representation. A FFT of the DAC output will show the notches filling up due to intermodulation tone components generated by the DAC due to circuit non-linearity.

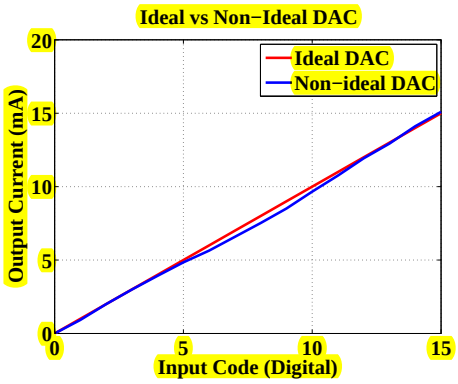
2.5.8 DAC modelling



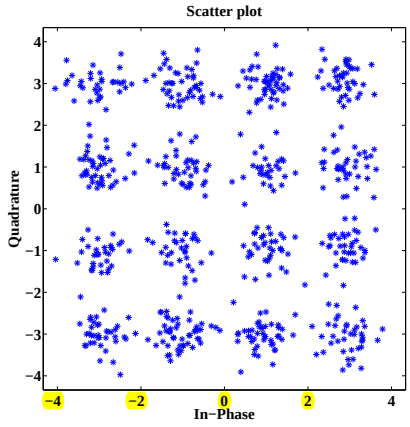
(a) DAC input-output (mismatch 0)



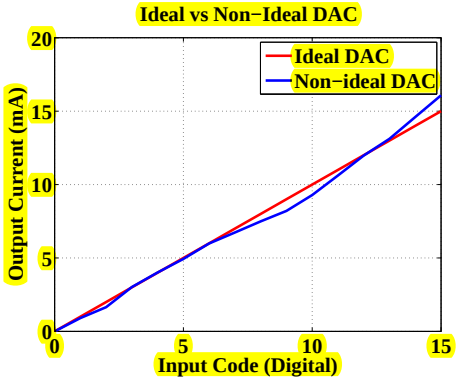
(b) 16-QAM constellation (mismatch 0)



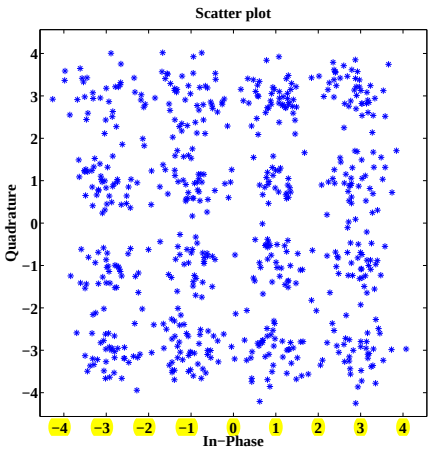
(c) DAC input-output (mismatch 0.5)



(d) 16-QAM constellation (mismatch 0.5)



(e) DAC input-output (mismatch 1)



(f) 16-QAM constellation (mismatch 1)

Figure 2.17: DAC model and constellations

Mismatch	DNL	INL	BER
0	0	0	0
0.3	+0.13/-0.14	+0.39/-0.08	0.0004
0.5	+0.18/-0.2	+0.11/-0.5	0.0008
0.7	+0.33/-0.32	0/-0.9	0.0024
1	+0.48/-0.3	+1.1/-0.8	0.008

Table 2.3: DAC mismatch vs (INL/DNL/BER)

To study the effect of DAC in an OFDM data stream, a Matlab model of the DAC is created where matching and resolution of the DAC elements can be varied. The model can be represented mathematically as shown in equation 2.21.

$$I_i = 1 + (m * rand) \tag{2.21}$$

Where I_i is the i^{th} element of an N-bit DAC and $1 < i < 2^N$, m is the mismatch factor and *rand* is an element in a set of normally distributed numbers between -0.5 and 0.5. Increasing m increases the mismatch between each elements thereby deteriorating DNL and INL. An $m = 1$ translates to a worst case element mismatch of 50%, where as $m = 0.1$ translates to a worst case element mismatch of 5%. Variation of the random mismatch also changes the INL and DNL of the DAC. The model consists of random digital bit stream which is converted to an OFDM signal. The OFDM signal (range -1 to 1) is scaled and quantised to suit the DAC input range (For 4-bit dac, 0 to 15). For the OFDM signal, various parameters such as number of sub-carriers, constellation levels etc. are configurable. A 4-bit DAC transmitting an OFDM signal (16-QAM, 128 sub-carriers, CP of 10) with different mismatch configurations is presented here as an example. Table 2.3 summarises the effect of random mismatch of DAC elements in a 4-bit configuration to INL, DNL and BER. As the mismatch increases, BER increases due to increase in DNL values and corresponding INL spread. Increasing mismatch results in the transfer characteristics of the DAC deviating from the ideal case, which results in increase of both DNL and INL. Figure 2.17 shows the transfer characteristics and output constellations for no mismatch, mismatch factor of 0.5 and mismatch factor of 1, which clearly shows the trend discussed in this section.

2.5.9 Types of DACs

Broadly DACs can be classified based on the type of output (voltage or current DACs), decoding scheme (Binary weighted, Fully decoded and Segmented) or sampling criteria (Nyquist or Oversampled DACs. We will examine a few DAC structures and relate them to the classifications mentioned above. DACs uses components like resistors, capacitors or current sources to generate their output. The output may or may not be buffered.

The output impedance of the DAC, which is a critical parameter, depends on the circuit structure and could be input digital code dependant or independent.

2.5.9.1 Resistor string DACs

A string of resistors in series are connected to a reference supply voltage V_{REF}. For an $N-bit$ DAC there are 2^N resistors. Figure 2.18 shows a 2 - bit resistor string DAC with

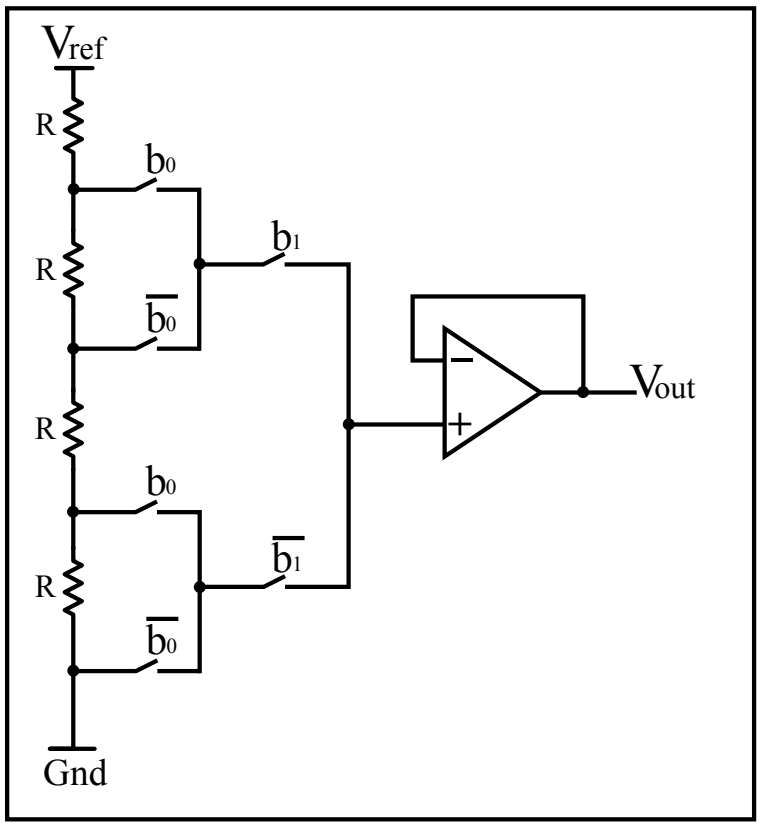


Figure 2.18: Resistor string DAC

4 resistors and associated switches controlled by bits b_0 and b_1 and an output buffer generating V_{out}, the output voltage. This is a voltage output DAC, where each intermediate node in the resistor string is connected to the output through a switch matrix depending on the input digital code [136]. Since each input code results in a different node in the resistor string being connected to the output, this DAC structure has code dependant output impedance. The output of the resistor string DAC could be buffered to alleviate this. In CMOS technology, the switch matrix could be implemented using transmission gates (low resistance at logic high or low gate inputs), NMOS switches (low resistance at logic high gate input) or P-channel MOSFET (PMOS) switches (low resistance at logic low gate input). Monotonicity of the output is inherently built into this converter, since each incremental node voltage will always be higher than the previous node. Resistor matching plays an important role in the precision of resistor string DACs. The number of switches and therefore the parasitic capacitance at switch nodes could be reduced if full decoding

of the binary inputs is performed. Increasing the digital logic as a result of this should not cost much since it is relatively easy to implement. Such an architecture is described in [137]. Folded architectures further reduce component count by implementing a memory like array of resistors and switches and row/column decoding [137]. Another variant of a resistor string DAC suitable for high resolution low power applications uses cascaded chains of resistor strings, where the first string (MSB string) selects an intermediate voltage which is further divided by the second string (LSB string) [138]. Additional buffering stages are required between the resistor strings. The accuracy of resistor string DACs depends on the matching of the resistors. Often laser trimming or averaging techniques are employed to increase the accuracy of each part. The different error compensation techniques mentioned in [139] improve the accuracy without trimming.

2.5.9.2 Binary weighted resistor DACs

Since the input to the DAC is in binary format, it is natural to assume that binary weighted structures could generate an analogue output. A string of binary weighted resistors as shown in 2.19 represents a binary weighted DAC. Although this method has the advantage

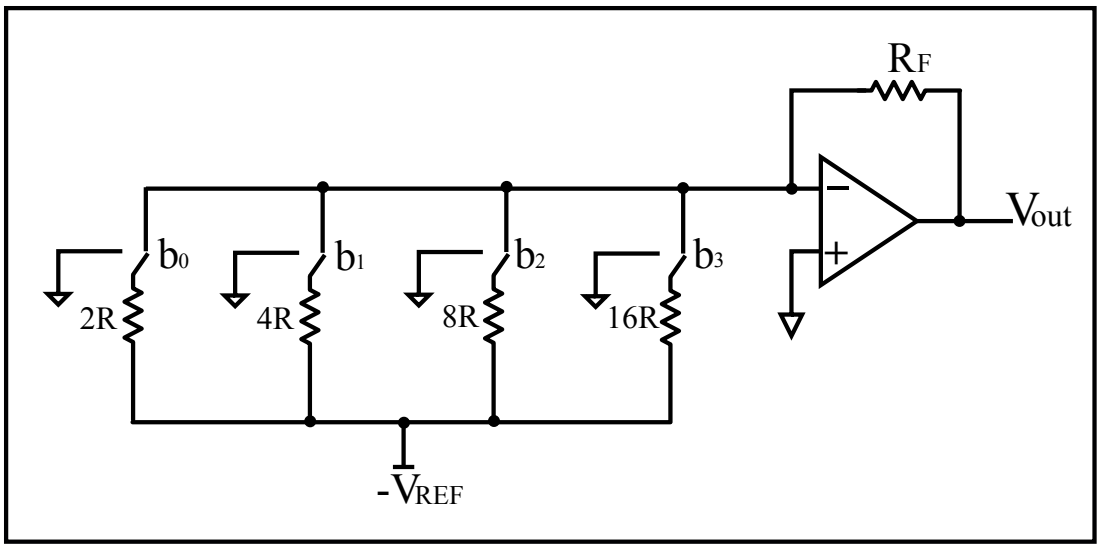


Figure 2.19: Binary weighted DAC

of utilising less circuit components (resistors and switches), the binary weighted nature of these components will results in large components sizes resulting in a slower response and more glitching. Monotonicity cannot be guaranteed in these type of structures. The output analogue voltage for the structure shown in 2.19 can be represented as 2.22 [133].

$$\begin{aligned} V_{OUT} &= -R_F V_{REF}\left(-\frac{b_0}{2R}-\frac{b_1}{4R}-\frac{b_2}{8R}\right) \\ &= \left(\frac{R_F}{R}V_{REF}\right)B_{IN} \end{aligned} \tag{2.22}$$

2.5.9.3 R-2R DACs

R-2R ladder DACs as are very popular due to their simplicity in structure, which aids in ease of design, matching and trimming. A current mode R-2R DAC is shown in 2.20. The

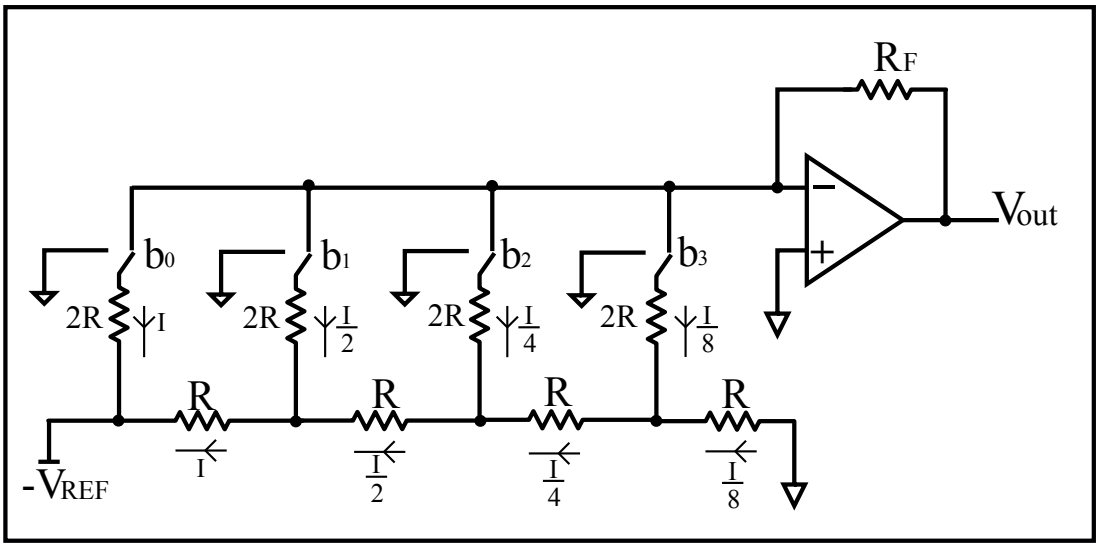


Figure 2.20: R-2R DAC

output node of the resistor network goes into the virtual ground of an operational amplifier (OPAMP). The current flowing into the virtual ground (flowing out into the feedback resistor R_F) is proportional to the digital input code. When a switch is connected to the output node, the current flowing through that switch will be a binary weighted multiple of the reference current. Only two resistance values are required to realise this DAC. Like resistors, generating binary weighted currents or voltages, it is also possible to realise DACs by distributing charge using capacitor networks.

2.5.9.4 Current steering DACs

Current steering DACs function by steering current into the output branch based on the digital input. Figure 2.21 shows the operating principle of a 2 bit current steering DAC. Current from the current sources are channelled either to the load resistor *R* or to a dummy node (GND) depending on the digital input. For a 2 bit DAC, code input 0 represents the lowest current and code input 3 represents the highest current. The voltage output is generated by the load resistor and further buffering or power amplification stages could be provided if needed. If current output is required for the application, the resistor could be replaced by an appropriate load. In current output schemes, sufficient voltage headroom must be provided to keep the current sources in the right mode of operation (e.g. saturation region for MOSFET based current sources.) Conventionally current source unit cells in the current steering DAC are realised using MOSFETs. The simplest implementation of the current steering DACs use binary weighted current sources, however as the resolution

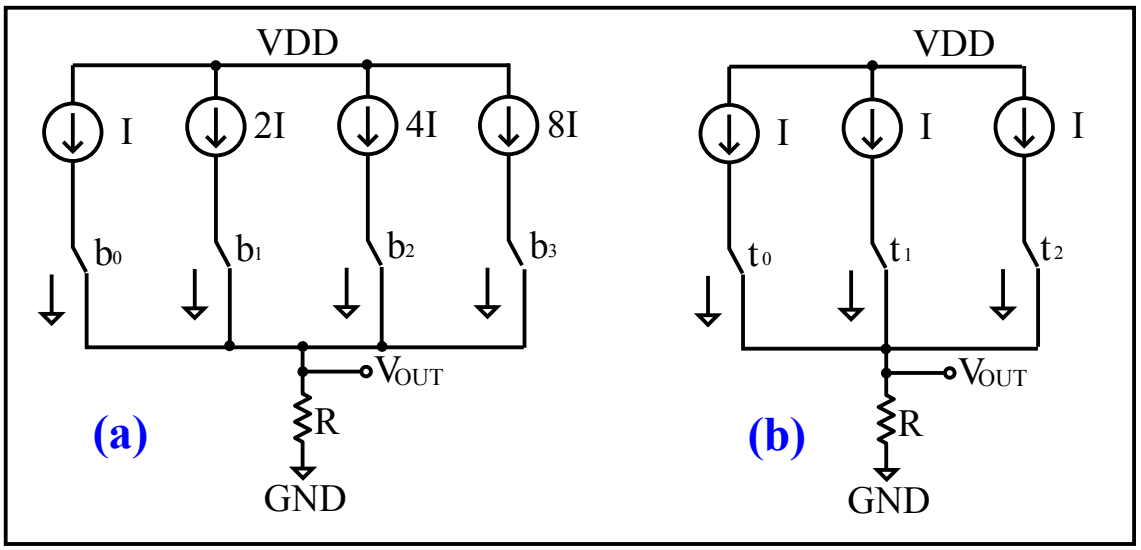


Figure 2.21: (a) Binary weighted and (b) Thermometer coded 2-bit current steering DAC

increases, the size of the MSB current source increases as well making them slower while switching. Binary weighted structures require fewer switch elements compared to other structures. For example, a 10-bit fully binary weighted DAC requires only 10 switching elements. Binary weighted structures suffer from increased glitching, non-monotonic characteristics arising due to poor current ratios and increased DNL and INL performance when compared to fully unary architectures[133]. If the current at MSB is less than the sum of all other currents, we can see that the DAC could become non-monotonic. As an example for a 3-bit DAC the transition from input binary code 011 to 100 will result in decrease of output current instead of an increase. This also indicates poor DNL performance at significant bit transitions. Increased glitches at the output arise due to the switching of larger current sources and switches and therefore large parasitic node capacitances. To solve these problems, a thermometer decoding scheme or unary decoding scheme can be used to decode the incoming digital inputs. Table 2.4 shows binary vs thermometer coding for 3-bit inputs. The thermometer code for an N-bit binary number has $2^N - 1$ bits. Ther-

Input	Binary Code	Thermometer Code
0	000	0000000
1	001	1000000
2	010	1100000
3	011	1110000
4	100	1111000
5	101	1111100
6	110	1111110
7	111	1111111

Table 2.4: Binary code vs Thermometer code

mometer coding demands complex digital logic, clock routing and layout constraints due

to the increase in the number of switches. As the resolution of the DAC increases, these requirements rise exponentially. For example a 12-bit binary weighted DAC requires 12 binary weighted current sources and associated circuitry whereas a 12-bit thermometer coded DAC requires 4095 unit current source elements and associated circuitry. This also increases the power consumed by the circuit. However, it guarantees monotonic performance over the entire code range, since each code input directly controls a single current source. Advantages of both binary weighted DACs and thermometer coded DAC could be combined in a hybrid structures such as a segmented current steering DAC. Figure 2.22 shows a 2-bit example. A segmented DAC, is constituteed of two or more sub DACs

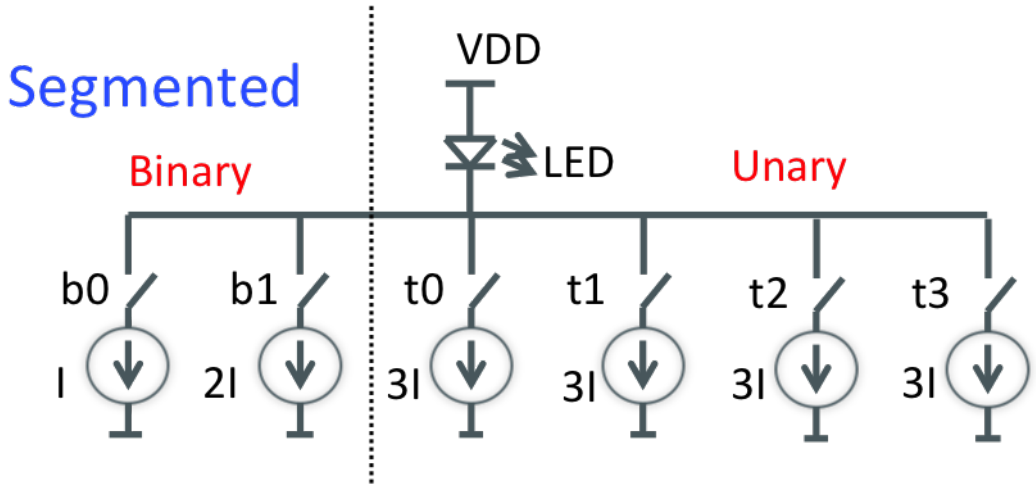


Figure 2.22: 2-bit Segmented DAC

where the MSBs are unary decoded and LSBs are binary decoded. In the simplest form a N-bit segmented DAC is constructed using a L-bit bit binary weighted structure for the LSBs and M-bit unary decoded structure for MSBs and $N = M + L$. The DACs has a monotonic performance, better INL and DNL performance and current steering DACs are reported to have high operating speeds [129, 130, 131]. Thus they are used for high speed applications such as broadband communications, video processing etc.

2.5.9.5 Oversampled DACs

The DACs discussed so far have sampling rates dictated by the Nyquist sampling rate (discussed in 2.5.6.3). It is possible to increase the sampling rate beyond twice the signal rate and gain performance improvements such as lower in band quantisation noise and thereby better SNR. By utilising techniques such as noise shaping using digital circuitry [140], further reduction of in band noise can be achieved and thereby a higher effective number of bits (ENOB). More details about oversampled DACs can be found in published literature [140, 141].

2.5.10 DAC based LED driver

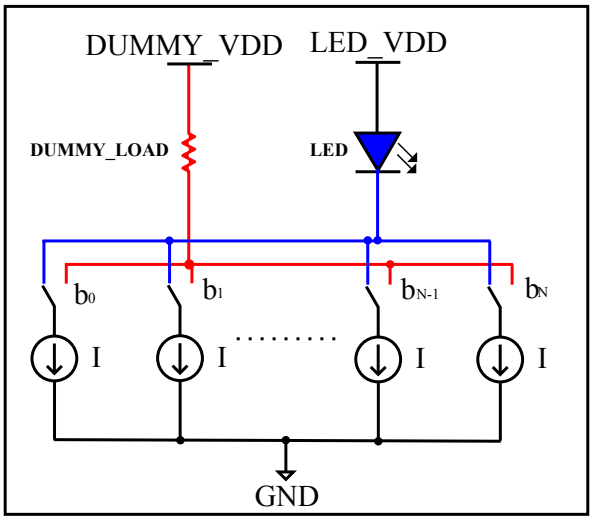


Figure 2.23: Current steering DAC based LED driver

Section 2.5.3.1 discussed the limitations of LED drivers from the perspective of VLC. A new drive scheme is proposed in this work based on the current steering DAC architecture. The high level concept of this scheme is shown in figure 2.23. Current sinks controlled by the digital inputs are connected to the cathode of the LED. When a current sink is activated by the input code, it sinks current from the LED, during the de-activated state, it sinks current through the dummy load, thereby maintaining constant current. The anode of the LED is connected to the external voltage source whose voltage is set based on the compliance required for the current sink and the voltage drop across the LED.

2.5.11 Digital to light converter (DLC)

Data conversion circuits in the electrical domain convert analogue information to the digital domain (ADC) and vice versa (DAC). For VLC digital to analogue conversion is required in the transmit signal chain to convert the digital data stream to the analogue current or voltage needed to drive the LEDs. In a typical VLC system, discrete electrical voltage or current levels for intensity modulation (IM) are generated by a single DAC, which is used to drive single or multiple LEDs after sufficient amplification. However, another way of realising an intensity modulated VLC link is by using multiple LEDs where IM is achieved by turning ON a number of LEDs based on the input code. This scheme can be called a digital to light converter (DLC), because the digital inputs dictate the number of LEDs turned ON and consequently direct conversion from the digital domain to optical domain. Figure 2.24 illustrates a 2-bit DLC system where the number of LEDs turned on is proportional to the input digital code. This method has been modelled and experimented in [142, 80, 143, 144]. The modelling and study of various factors

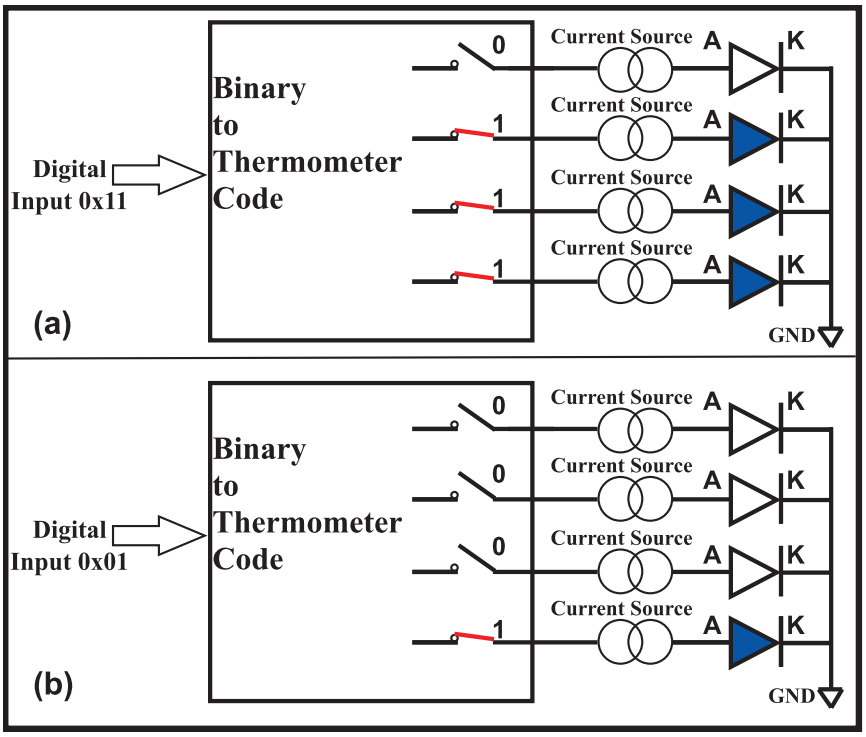


Figure 2.24: Illustration of DLC system operation; (a) With digital input of 3 (0x11) ; (b) With digital input of 1 (0x01)

that could affect such a system using μLED arrays such as mismatch between μLED elements, life expectancy of each μLED element are studied in [142]. Demonstrators based on this scheme are realised in [80, 144] using discrete and micro LEDs respectively. A discrete incarnation of this scheme is reported in [80] and demonstrates the ability of such a system to transmit an OFDM modulated signal where as the integrated system reported in [144] demonstrates the ability to transmit PAM symbols at rates up to 200 MS/s. For the first time an integrated DLC capable of complex modulation schemes such as OFDM is realised and characterised as part of the research carried out in this thesis. More details about this will be presented in section 3.4.3.

2.6 Summary

Utilisation of visible light for free space wireless communication known as VLC is becoming more relevant due to the RF spectrum crunch and wide spread adoption of semiconductor light sources such as LEDs. High speed VLC systems have been demonstrated in controlled environments (research laboratories). VLC system concepts are discussed in this chapter highlighting different modulation schemes such as OOK, PAM and OFDM. Some characteristics of the LEDs were analysed to understand their importance while modulating them. Performance of electronic drive circuitry is key to realising a power efficient , high speed VLC system. Common LED driver circuit topologies used for light-

ing applications are introduced and their drawbacks are discussed. VLC demonstrators in the literature use either discrete electronic components or complex laboratory equipment (AWGs) to modulate LEDs at high speed. These schemes are not suitable for widespread commercial installation of VLC systems. Circuit miniaturisation using CMOS technology and utilisation of current steering DAC scheme to drive different types of LEDs at high current (255 mA) and high speed (500 MHz) for VLC is proposed in this work. Different DAC architectures are also discussed in this chapter and further chapters present an insight into the design of the new LED driver and experimental results. A short introduction about DLC is presented and includes some of the listed published work in this area.

Chapter 3

Integrated Circuit Design

3.1 Overview

In this chapter, various aspects of the LED driver and its design process are detailed. Any IC design has to start from the specifications for the circuitry. Specification of the circuitry originates from the defined system level performance criteria. These criteria are derived from the system level simulations and calculations which are presented here. Selection of an appropriate fabrication technology is critical to achieving the required performance while at the same time, staying within the available budget. An Austria Micro Systems (AMS) 180 nm CMOS technology is selected for the IC fabrication, and details are also presented in this chapter. As discussed in 2.5.10 a current steering DAC structure is used to drive the LEDs. The circuit architecture of this driver is presented along with design details. Details include, circuit hierarchy, input-output details, power domains, biasing requirements and MOSFET sizing. Digital control of the driver chip through a serial interface is also detailed. The driver chip also has additional circuitry allowing direct digital to light conversion experiments by wire bonding GaN μLEDs to it. More information about this block is given in this chapter. The circuit layout of each block is presented along with optimisations to improve the overall performance of the LED driver.

3.2 Circuit specification

The CMOS LED driver design was carried out as a part of the UP-VLC project. This project is a "component to system level" design project to demonstrate high speed parallel VLC links utilising high bandwidth μLEDs. System modelling and simulations from other project groups generated the specification for the LED driver [35]. Even though the primary aim of the CMOS LED driver is to drive μLEDs, flexibility is built into the driver to drive OTS LEDs as well. Key aspects considered during the design of this driver

include operating bandwidth, power efficiency, multi channel operation and high current drive.

3.2.1 Bandwidth

The bandwidth requirement of the driver circuit is determined by considering the modulation bandwidth of the different types of LEDs to be used in the system and the overall system data rate requirements for the demonstrators envisaged. μLEDs have reported bandwidths up to 800 MHz as mentioned in section 2.4.4, whereas OTS LEDs have reported modulation bandwidths up to a few tens of MHz. Two types of μLEDs were fabricated for the demonstrators built in this project to be used for two different modes of operation namely single-input single-output (SISO) mode and multiple-input multiple-output (MIMO) mode. System parameters derived from the simulations indicate to achieve a 1 Gbps link at a distance of 1 m using these μLEDs, the driver should have a modulation bandwidth of 175 MHz for the SISO mode and 125 MHz for the MIMO mode. The bandwidth of the DAC depends on the sampling rate of the system as set by the Nyquist sampling theorem. The relationship between the analogue bandwidth and the sampling rate has been discussed in section 2.5.6.3. The driver chip has an input sampling rate and an output sample rate. The input sampling rate is the rate at which incoming data is sampled into the internal circuitry. Depending on the mode of operation, the output sample rate varies. In SISO mode, the input sampling rate and the output rate are the same, where as in MIMO mode, the output rate is less than the input sampling rate. The UP-VLC system demonstrator aims to achieve data rates up to 1 Gbps, from which the sampling rate of the DAC can be derived. Both M-PAM and OFDM schemes were analysed. For 4-PAM, which encodes 2 bits per symbol, to achieve 1 Gbps, the output sample rate must be at least 500 MHz without considering any error correction overhead, and similarly OFDM with 16-QAM could theoretically give 1 Gbps with a similar sampling rate, this rate was fixed for SISO mode. In the MIMO mode a fraction of 500 MHz could be used per channel.

3.2.2 Channels

System simulations using μLED models indicated that to achieve 1 Gbps at a link distance of 1 m, more than one μLED is needed since the maximum optical power emitted by the μLED is limited. This is by either increasing the transmitted power in SISO method by ganging more than one LED to transmit the same information or in the MIMO method by using multiple μLEDs to transmit parallel data streams. Both schemes point to the need for a multi channel driver with the ability to stream incoming data based on the mode of operation. Considering the silicon die area and drive current strength, the number of channels per driver is fixed to 4.

3.2.3 Drive current

Drive current needs for different LEDs are not the same. OTS LEDs are available in the market for drive currents up to 10 A [145]. Most of the high current LEDs are capable of carrying currents more than 1 A. The voltage to current characteristics of the red channel of an OTS RGB LED [**osram_ostar_lertdus2w**] is shown in figure 3.1.

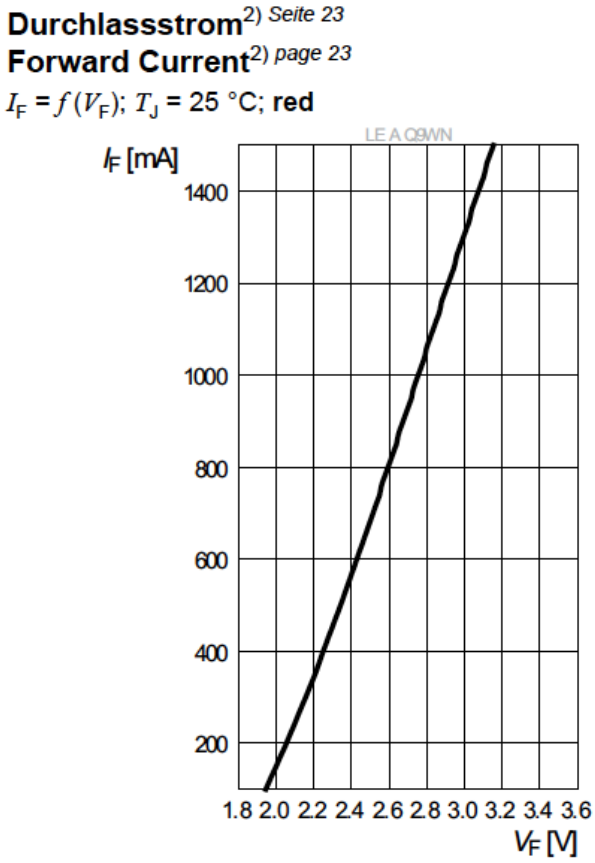


Figure 3.1: V-I characteristics of an OTS LED [146]

μLEDs due to their smaller dimensions have a lower current carrying capability compared to OTS LEDs. Figure 3.2 shows the current to voltage characteristics of various pixels in the MIMO μLED array.

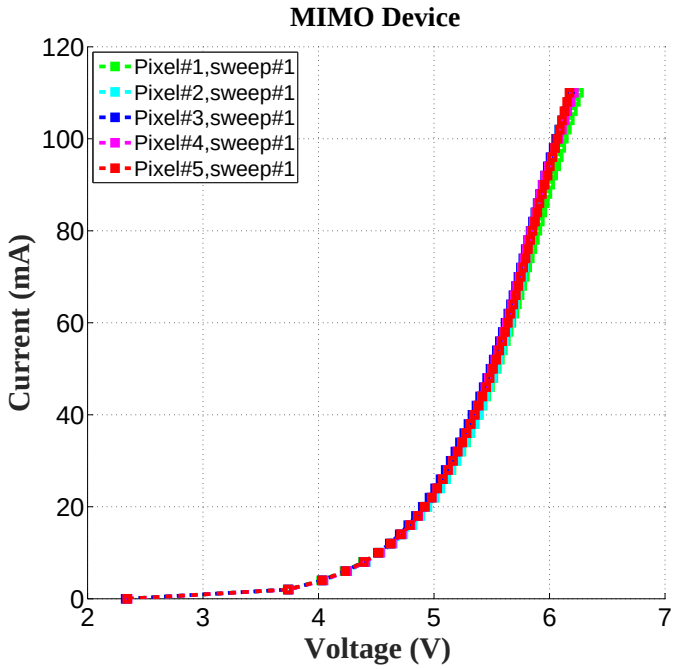


Figure 3.2: V-I characteristics of a μLED array fabricated for MIMO operation and characterised at the University of Strathclyde

It has been shown that the small signal bandwidth of the μLEDs increases with current density (applied current per unit area)[113]. Figure 3.3 shows the measured bandwidth of μLEDs of various dimensions.

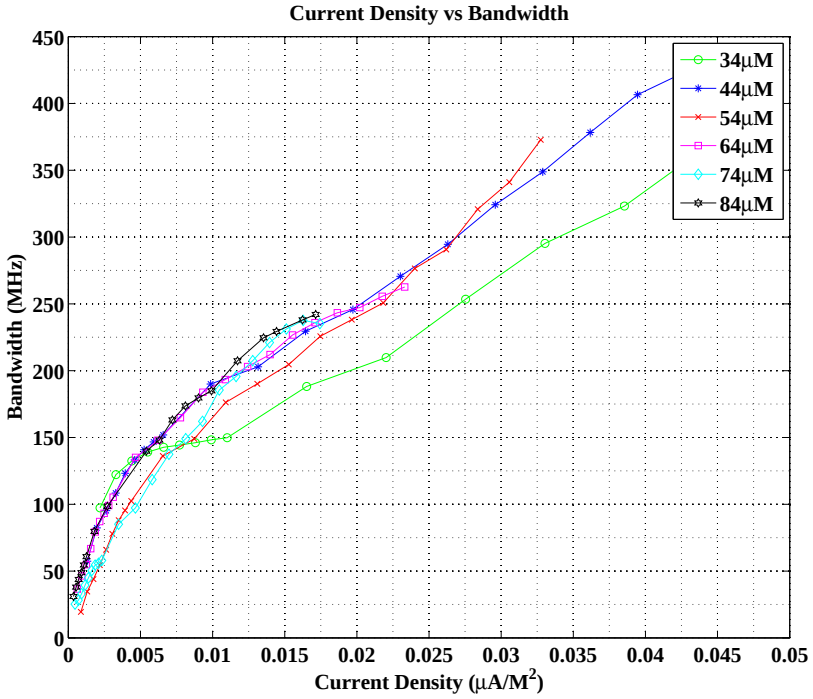


Figure 3.3: Current density .vs Bandwidth of μLEDs in different sizes provided by the University of Strathclyde

Increasing the drive current also increases the size of different circuit blocks inside the driver chip including the final drive stage transistors. Bigger transistors contribute more parasitic capacitances in circuit nodes and they are slower to be turned ON or OFF thus affecting the operating speed. Here is a trade off between the maximum current delivery capability of the driver and its switching speed. Considering these factors, a drive current rating of 255mA was chosen per channel, which should be able to drive the μLEDs and some OTS LEDs.

3.2.4 Power efficiency

High power efficiency is key to any technology which has the scope for mass production. From the electrical power received by the driver, the maximum possible should be delivered to the LED to convert to optical power. As seen in Table 2.1, the majority of the VLC demonstrators use AWGs or discrete components to achieve high data rates. Neither are power efficient schemes for driving LEDs compared to some of the integrated schemes reported for VLC (see Table 3.1) From figure 3.4 it is clear that, even though existing integrated driver architectures (listed in table 3.1) achieve high power efficiency, they do not deliver data rates comparable to AWG based drive schemes listed in table 2.1.

Index	Reference	Data rate	Power efficiency	Type	Application
1	[116]	50 Kbps	95%	Resonant converter	VLC
2	[82]	266 Kbps	92%	Boost converter	VLC
3	[115]	2 Mbps	90%	Buck converter	VLC
4	[147]	20 Mbps	85%	Buck converter	VLC
5	[148]	24 Mbps	42%	Self oscillating PA	ADSL

Table 3.1: Power efficiency of various integrated drive schemes from literature

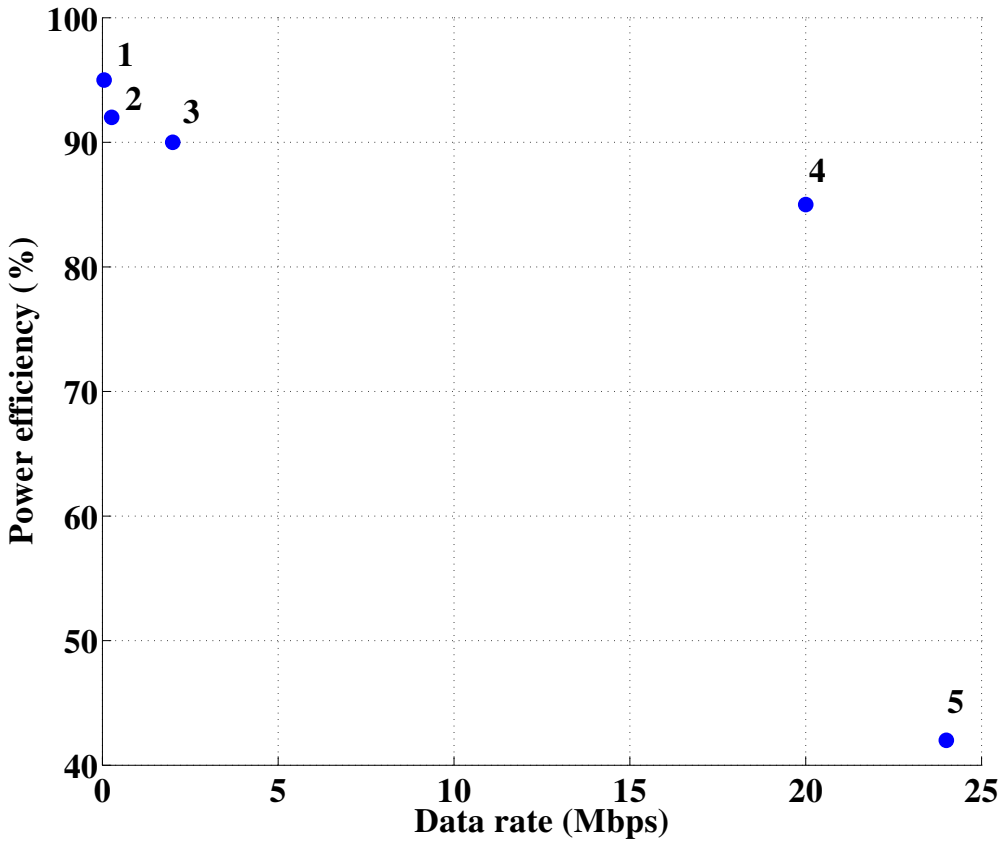


Figure 3.4: Data rate .vs Power efficiency of wired and wireless drive circuits realised as ICs.

Achieving data rates comparable to existing RF technologies such as Wi-Fi while maintaining the high power efficiency of switch mode converter based LED drivers for lighting is a challenge. A number specification was not derived for this parameter, but possible methods to increase the power efficiency of the drive stage of the current steering DAC has been explored in this work.

3.2.5 Resolution

The resolution of the DAC translates to the number of amplitude discrete current levels producible. For modulation schemes such as OFDM the non-linearities introduced by the DAC are not desirable and limit the quality of the analogue signal reproduced. However realising high resolution DACs (>10 bits) at high speed and specified load current to drive LEDs is difficult and might not be necessary to achieve the data rate required by the UP-VLC demonstrator. From 2.5.9.4 published architectures has the maximum output load current of 30 mA which is not enough to drive LEDs. It has been shown in [149] that for OFDM an optimum resolution can be decided upon on the modulation scheme's complexity. In the case of PAM, the system simulations indicated that going above 32-PAM

does not provide significant improvement in data rate, which indicates, a 5-bit system will be enough. Modelling of the DAC to study the effect of non-linearity in the I-L characteristics and the effect of pre-distorting the input has shown that the higher the resolution, the better linearity performance can be obtained from pre-distortion. 4-bit, 8-bit and 12-bit DAC models were built using Simulink along with a pre-distortion function and LED model. The 4-bit DAC is easiest to design, however the noise performance (quantisation and pre-distortion) is not good enough, whereas the 12-bit DAC offers better noise performance at the cost of design complexity. An 8-bit DAC offers good enough linearity (~48 dB) for an OFDM scheme and supports 32-PAM without the need to have the circuit design complexity and matching requirements of a 12-bit DAC. Table 3.2 summarises and compares the specifications and design complexities.

	4-Bit	8-Bit	12-Bit
Unit Cells	16	256	4096
Matching Requirements	Low	Medium	High
Unit Cell Current	16 mA	1 mA	62.5 uA
Layout Complexity	Low	Medium	High
Achievable Spectral Efficiency	Low	Medium	High
SQNR	24 dB	48 dB	72 dB

Table 3.2: Comparison of 4-Bit, 8-Bit and 12-Bit DACs

3.2.6 DAC architecture

3.2.7 System interface

Transferring of the digital input, sampling clock and control signals to the DAC is done digitally. Due to high speed operation (section 3.2.1), digital inputs and sampling clocks are chosen to be fed through an LVDS [150] interface, which is a differential signalling scheme used to transfer high speed digital data between components on PCBs. The sampling rate requirements of the DAC points out that the LVDS interface should be able to operate at least up to 500 MHz. A differential signalling scheme offers the added advantage of higher noise immunity and reduced crosstalk, which is critical in high speed communication systems. The LVDS interface will be used to deliver the data, clock and DAC select signals for the chip. The control and configuration of the driver chip needs a dedicated digital interface capable of receiving control signals from outside and storing these details internally. A low speed (10 MHz) serial interface is specified for this purpose.

3.2.8 Modes of operation

The DAC driver is envisaged to operate in modes listed below. Mode selection must be done through the control interface.

3.2.8.1 Single-input single-output (SISO) Mode

In SISO (Gang) mode, the received data is simultaneously transmitted through all channels. This mode enables overall transmit power to be increased by ganging the LEDs to transmit the same information. Incoming data must be routed to all output channels at the same rate.

3.2.8.2 Multiple-input multiple-output (MIMO) Mode

This mode enables multi stream MIMO transmission. In MIMO mode, the incoming data sample stream is split into 4 sub streams and one is sent to each channel. The output rate is less than input rate for MIMO mode operation.

3.2.8.3 Digital to Light Converter

An additional experimental DAC was added to the chip to study the direct digital to light conversion, where discrete optical levels for IM/DD are generated by turning ON/OFF individual elements in a μLEDs array bonded to the CMOS die.

3.3 Design and fabrication

A standard CMOS design methodology was followed to realise the circuit in Silicon. The various steps in this method are listed blow

- High level design and selection of suitable technology
- Schematic capture of the circuit
- Functional verification of the circuit
- Layout of the circuit
- Post layout verification
- Circuit fabrication

3.3.1 Technology

AMS C18 ($0.18\mu M$ CMOS) technology was used for designing and fabricating the driver chip. This technology supports various flavours of $5V$ and $1.8V$ MOSFETs [151]. It has 6 metal layers available for interconnection including a low resistance top metal layer. AMS also provides a digital standard cell library as part of the process design kit (PDK). Europractice™ provides access to AMS foundry service through their multi-project wafer (MPW) run.

3.3.2 IC design and simulation tools

Software tools from Cadence™ and Mentor Graphics™ were used to design, simulate and verify the driver chip. The Cadence IC suite, which consists of Virtuoso version 6 was used for analogue and custom digital circuit design. The Virtuoso package consists of schematic capture and layout utilities. Design rule check (DRC) and layout versus schematics (LVS) checks are performed using Calibre™ from Mentor Graphics corporation. Schematic level and post layout extracted netlist simulations were performed using Spectre™ from Cadence systems.

3.4 Chip architecture

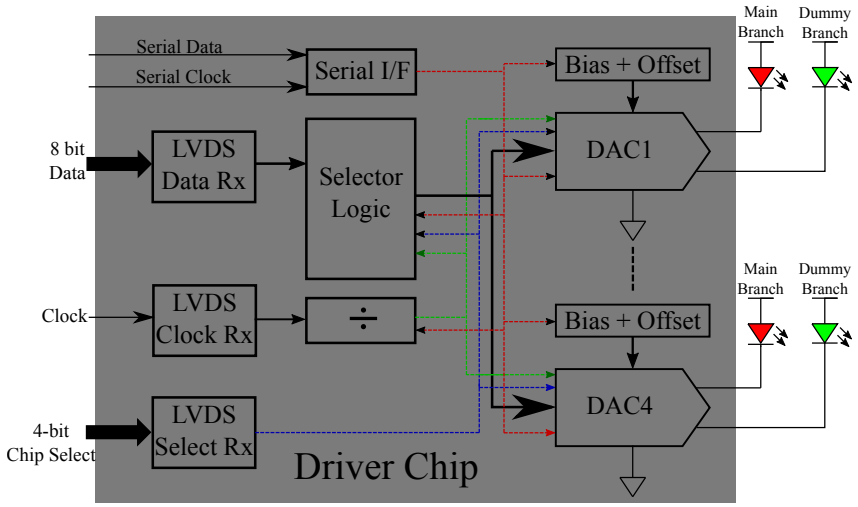


Figure 3.5: Block diagram of the driver chip depicting major functions

The block diagram of the driver chip is shown in figure 3.5. The main sub blocks inside the chip are listed below

- Current steering DACs
- LVDS receiver

- Digital logic
- Configuration register
- DAC for digital to light conversion

The CMOS driver chip is powered from both 1.8V and 5V external supplies. It also has different bias current inputs for biasing various parts of the circuitry. Other than power supplies and biasing inputs, the chip has 2 sets of digital inputs, high speed LVDS inputs for receiving data, clock and DAC select signals and a low speed serial bus for configuration clock, data and latch in signal. The high speed digital inputs from outside are wired into the LVDS receiver block, which generates single ended signals to be propagated inside the chip. The low speed serial bus is interfaced to shift register logic , which acts the register bank where chip configuration is stored. Digital logic controls the data path based on the mode of operation configured through the serial interface. It also generates the required clock based on the mode of operation. Each DAC receives its own data, clock, bias settings and enable signal. The total silicon area of the driver chip is $29mm^2$. For prototyping, a ceramic pin grid array (CPGA) package is used to house the silicon die. Design details of each of these blocks are presented below

3.4.1 Main DAC

Hierarchical design methodology is normally followed during any complex CMOS design. A top - bottom analysis of the main DAC hierarchy is presented in this section.

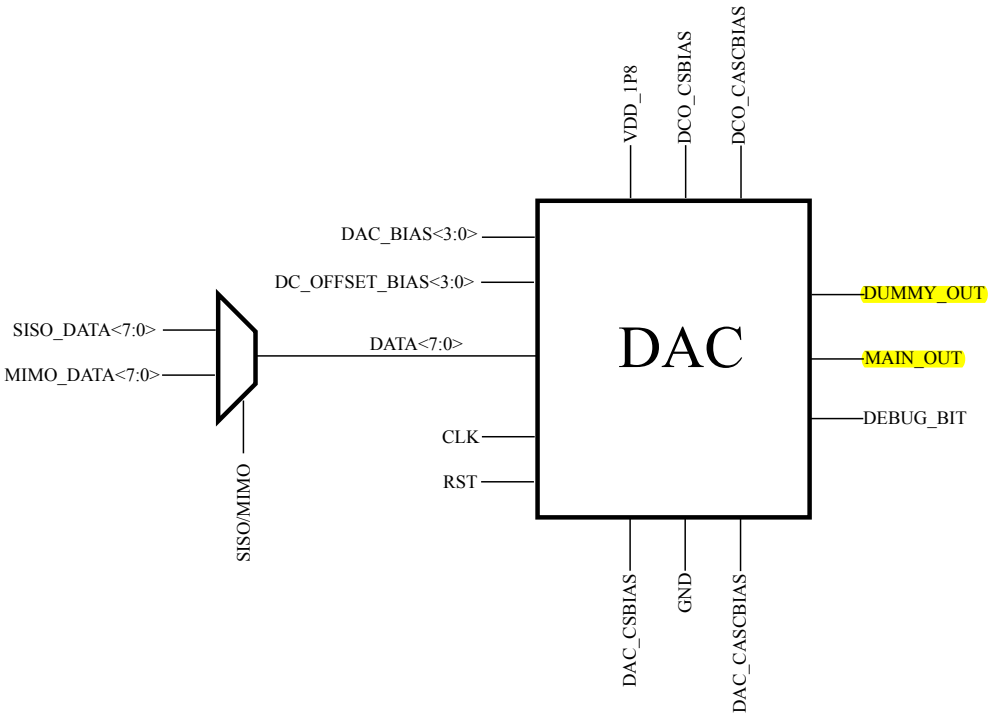


Figure 3.6: DAC cell top level

Figure 3.6 shows the top level of the DAC. Inputs to the DAC can be classified into analogue inputs and digital inputs. Analogue inputs include the power supply rail and bias currents. The DAC is powered by a 1.8V rail which is part of the analogue power domain in the chip. External bias currents for the current cells in the DAC are DAC_CSBIAS and DAC_CASCBIAS and for the DC-offset generator block DCO_CSBIAS and DCO_CASCBIAS. The digital inputs include data, clock, control signals and reset. Based on the mode of operation (SISO/MIMO), the 8-bit data from the digital logic is fed to the DAC through a multiplexer. SISO_DATA<7:0> is selected for SISO mode of operation and MIMO_DATA<7:0> selected for MIMO mode. The control signal for the multiplexer, SISO/MIMO is generated by the digital logic based on the configuration register value. The clock input, CLK, to the DAC comes from the clock divider in the digital logic. The frequency of this clock depends on the mode of operation. The bias current required for the DAC can be controlled digitally through DAC_BIAS<3:0>, thus enabling LSB current level selection. DC_OFFSET_BIAS<3:0> enables the digital control of the DC-offset bias. The DAC and sub-cells can be reset through the active high reset pin. All digital signals going to the DAC block are referenced to 1.8 V. The DAC has 2 analogue outputs namely main branch and dummy branch. Both dummy branch and main branch have similar architecture as they are part of the same current cell (Current cell is described in section 3.4.1.2). When the current cell is activated by a digital input, the current source is connected to the main branch and when the current cell is deactivated, the current source is connected to the dummy branch. This arrangement ensures that the current cell can always sink current irrespective of the input state and thereby preventing voltage glitches at the output of the current source which could happen if the current path is disconnected. Current cells steer current through either of these branches based on the state of the input. These outputs are wired to chip pads, where LEDs can be connected to either or both of these.

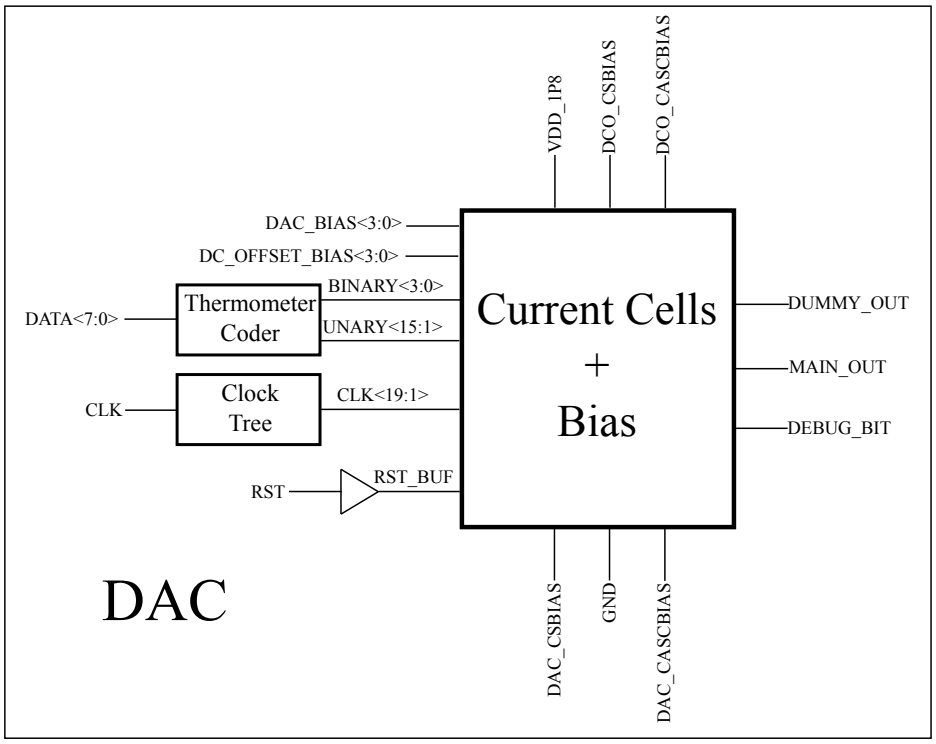


Figure 3.7: DAC cell intermediate level

Figure 3.7 descends into the next level of the DAC. Digital inputs are further processed at this level. Section 2.5.9.4 discussed different types of current steering DAC structures and their merits and de-merits. For this work, a segmented architecture is selected comprising of two sub DACs, a unary DAC and a binary weighted DAC. This structure provides monotonic performance at high speeds while maintaining linearity. The incoming 8-bits are split in a 50-50 ratio for the sub DACs, the 4 MSBs for the unary DAC and the 4 LSBs for the binary weighted DAC. The segmentation scheme is shown in figure 3.8. The upper half or MSB 4-bits (DATA<7:4>) are unary decoded by the thermometer decoder to generate 15 unary decoded outputs (UNARY<15:1>) to drive the MSB current cells. Table 3.3 shows the binary inputs to the thermometer decoder and unary outputs.

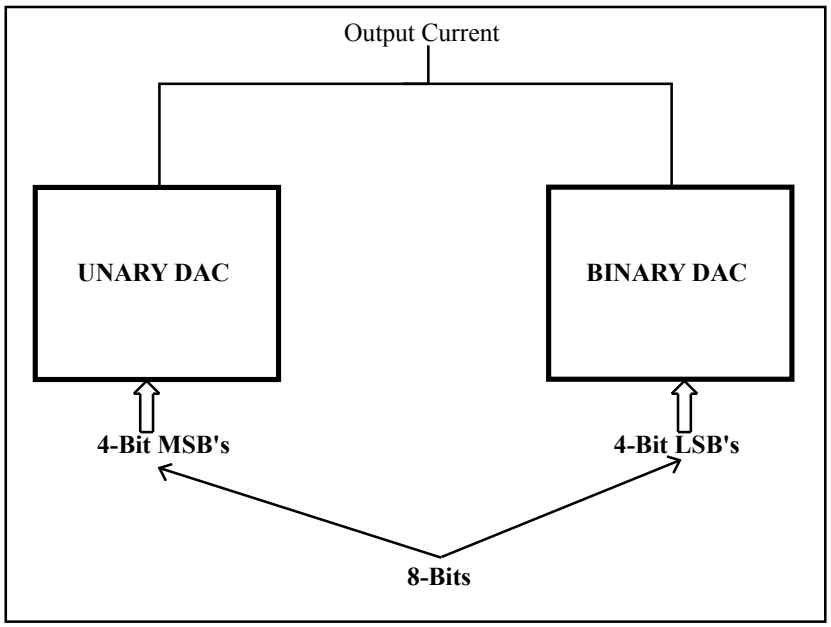


Figure 3.8: Segmentation scheme for the current DAC

Binary				Thermometer Code															
B_3	B_2	B_1	B_0	T_{15}	T_{14}	T_{13}	T_{12}	T_{11}	T_{10}	T_9	T_8	T_7	T_6	T_5	T_4	T_3	T_2	T_1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 3.3: Unary decoding inputs and outputs

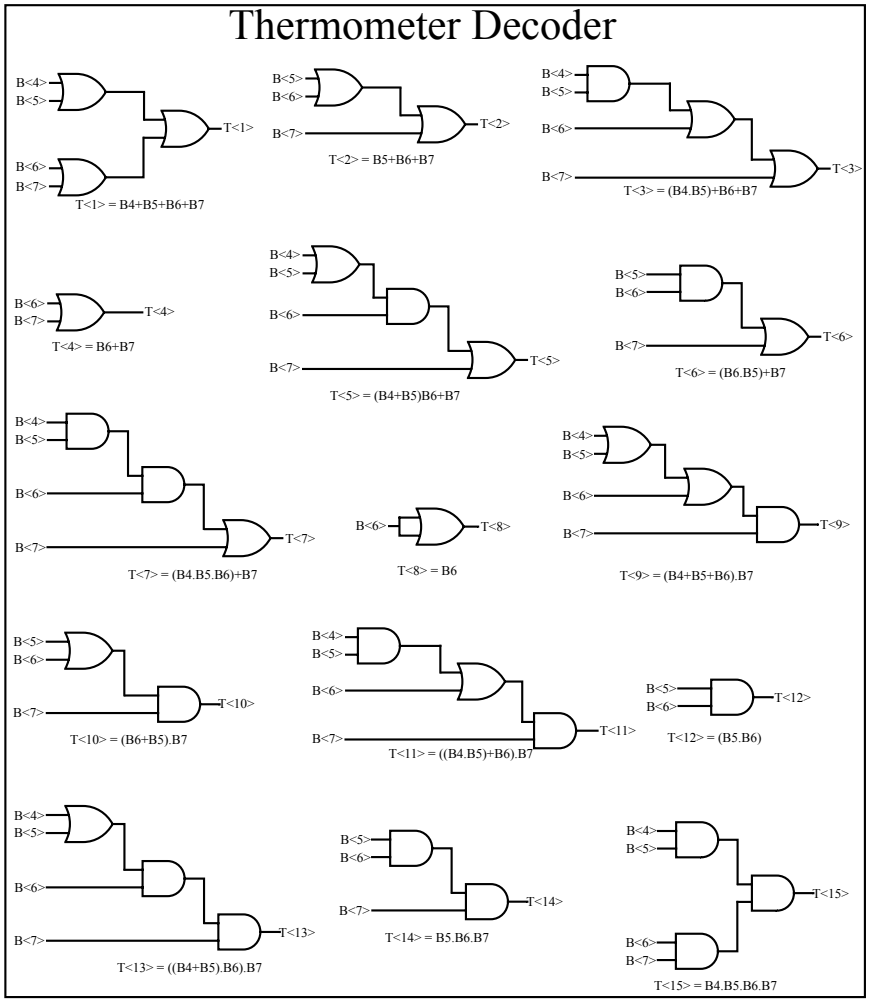


Figure 3.9: Thermometer decoding logic

Decoding logic generates the unary output based on the boolean expressions derived from the table 3.3. Figure 3.9 shows the decoding logic and boolean expressions. The lower half or LSB 4-bits (DATA<3:0>) are not decoded and they will control the binary weighted current cells. The lower bits are delay equalised with the unary decoded outputs by adding two inverter stages and passed to the current cells (BINARY<3:0>). This will ensure that all current cells are synchronously enabled or disabled which is critical for the error performance of the DAC. Bit 0 from this block is wired to an input-output (I/O) pad and accessible externally for debug purposes. Current cells should be enabled or disabled synchronously. To ensure this, the clock is split and routed to each current cell. A clock tree is implemented, which receives a clock input from the clock divider and generates 19 delay equalised clocks. These clocks are routed symmetrically to each current cell. The clock tree network is shown in figure 3.10.

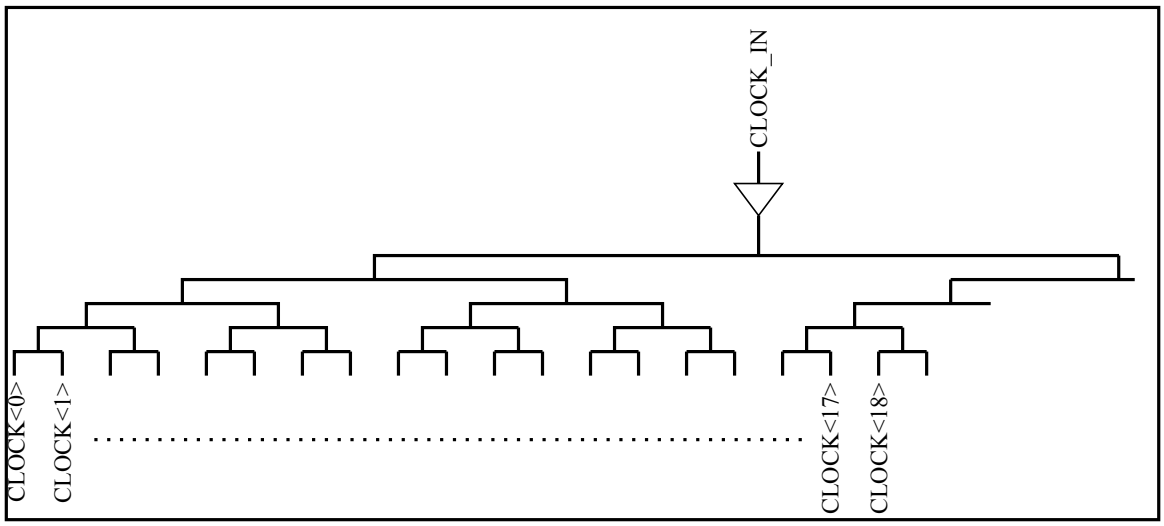


Figure 3.10: Clock distribution network

The clock tree is implemented with a network of clock buffers from the standard cell library. 5 levels of buffering is required to generate 19 clocks. The drive strength of the clock buffers reduces as the clock propagates deep into the tree. The incoming reset signal, RST is buffered and routed to sub blocks.

An array of current cells are needed to realise the 8-bit DAC. A fully decoded DAC would need $2^8 = 256$ unit current cells, where as a binary weighted structure needs only 8 current cells with current weights as (1,24,8,16,32,64,128). As seen in section 2.5.9.4, both schemes has merits and demerits. A segmented scheme, with 50-50 segmentation is implemented here. The LSB current cells, controlled by data bits DATA<3:0>, are binary weighted and the maximum current weightage per bit is in the order 1 mA, 2 mA, 4 mA and 8 mA. 15 MSB current cells capable of carrying 16 mA each are controlled by thermometer coded outputs <15:1>. The total current from all the cells is routed to the output nodes and can be calculated as in 3.1.

$$\begin{aligned} I_{max} &= I_{binary} + I_{unary} \\ &= (1+2+4+8)mA + (15 \times 16mA) \\ &= 255mA \end{aligned} \tag{3.1}$$

The arrangement of the current cells, biasing block and DC offset block is shown in figure 3.11. Each current cell receives the control bit, sampling clock, bias voltages and reset signal. The output nodes from all current cells where currents are steered (main and dummy nodes) are wired up to output pads of the chip at top level. The DC offset block incorporated into each DAC, provides an adjustable DC offset current to the main output node of the DAC. The DC offset current level can be configured through the serial interface. Inside each current cell, there is a digital logic block and the differential current steering block with biasing circuitry. Figure 3.12 shows the current cell organisation.

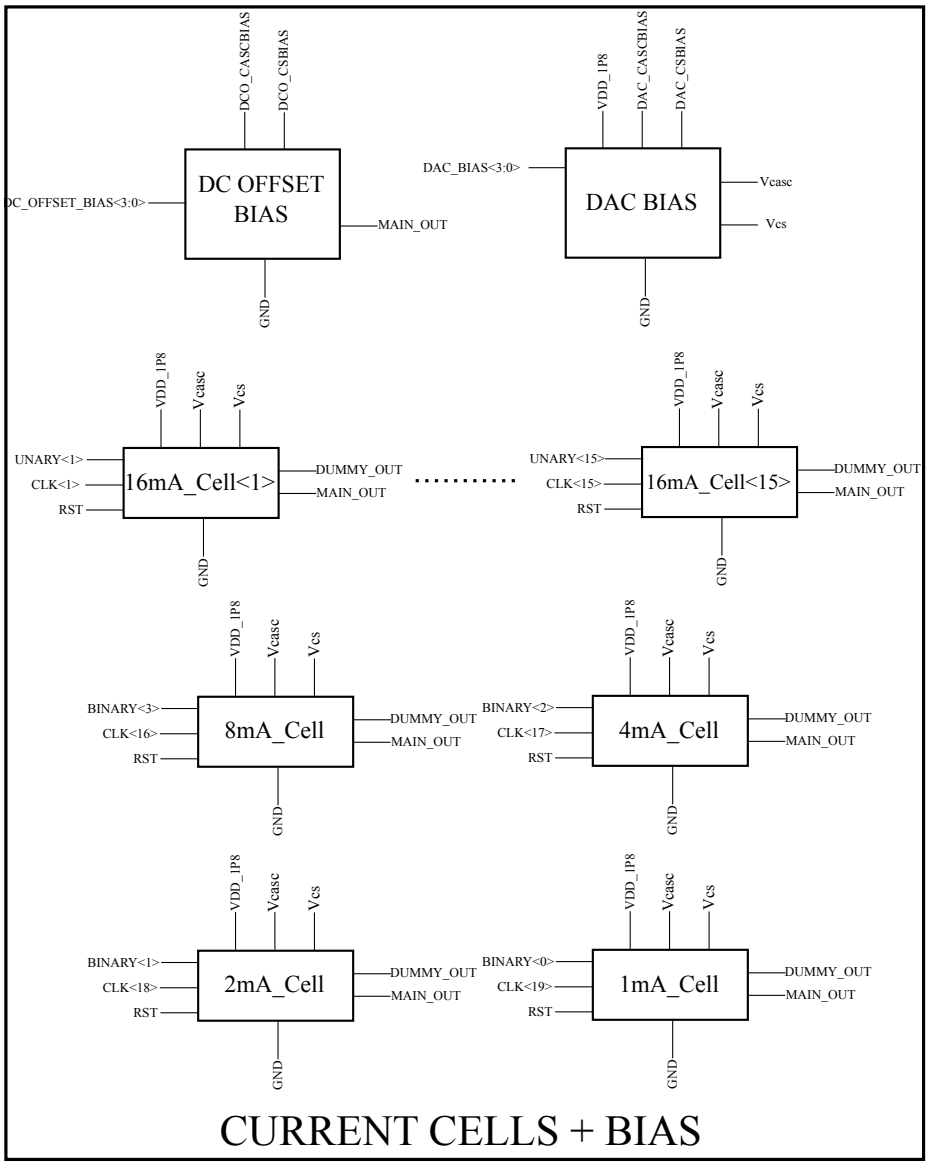


Figure 3.11: Current cells, DAC biasing and DC offset

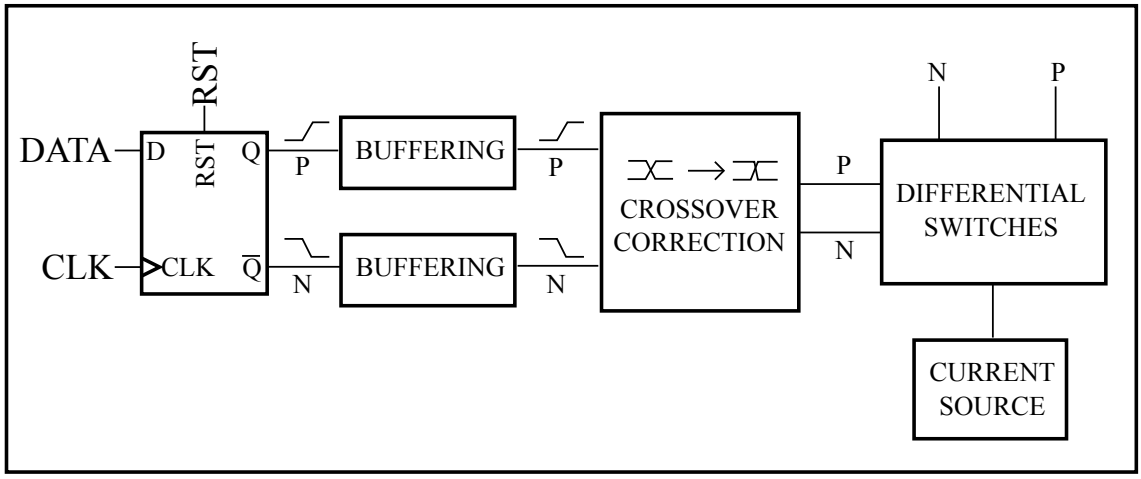


Figure 3.12: Current cell logic

The digital logic in the current cell has an input D-type flip flop which re-samples the incoming data. Global reset is wired to the flip flop reset pin to keep the flip flop and thereby the current cell in reset if needed. D-type flip flops have complimentary outputs Q and $\overline{Q}$. Each current cell, due to the differential current steering structure requires these complimentary outputs. The outputs of the flip flop are buffered through 5 inverter stages and edge corrected before being passed on to the differential switches. Inverter sizing is performed based on the transistor size of the next stage. The current sources in the DAC should always be conducting to ensure the linearity of the DAC, otherwise, they will move out of saturation and into the tlinear region. A differential current steering scheme is implemented to achieve this. However, while switching the current from one branch to the other using complimentary switch control signals, both switches will not be conducting enough for a brief period of time and the current sources will be pushed into the triode region. To prevent this, the complementary switch signals are conditioned so that, the cross over happens not at half level of the switch signal, but at a higher level, ensuring a seamless switching of current from one branch to other. This is realised using the crossover correction latch circuitry shown in figure 3.13. By adjusting the aspect ratios of PMOS and NMOS transistors the rising and falling edges of the signals can be varied and thereby the crossover point.

3.4.1.1 Structure

A 50-50 segmented cascoded current steering structure with 8 bit resolution is implemented. An 8 bit DAC has a granularity of 256 different analogue output levels. The drive current requirement of 255 mA translates to a LSB current level of 1 mA. The block level representation of the circuitry is shown in 3.11. The main sub blocks in this circuitry are the following

- Current cells

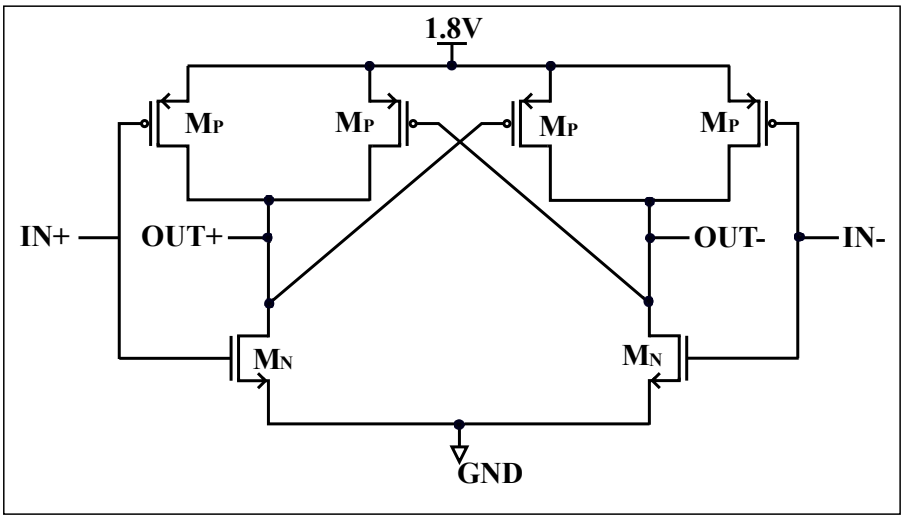


Figure 3.13: Crossover correction latch

- Biasing PMOS DAC
- DC Offset NMOS DAC

3.4.1.2 Current cells

Current cells consists of a current sink, constantly drawing fixed current through the load. To avoid glitches occurring at circuit nodes, and thereby affecting the load current itself, the current source must be conducting constant current all the time. Figure 3.14 shows the structure of a single current cell. The current cell is made of NMOS transistors.

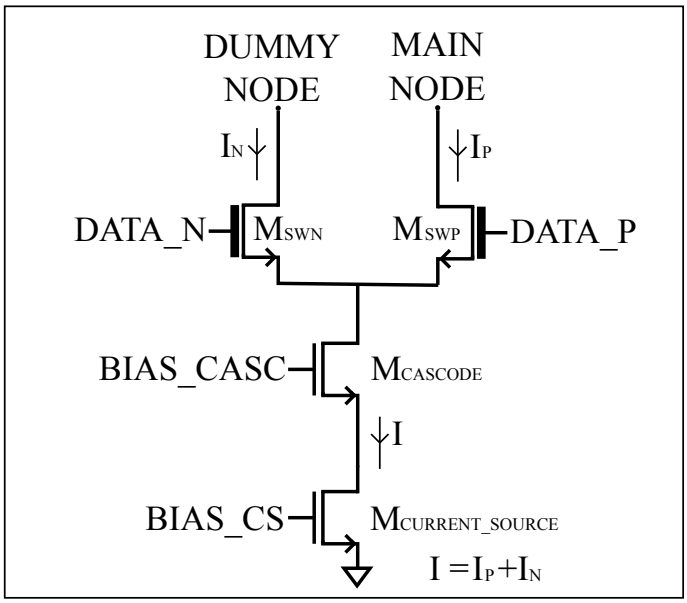


Figure 3.14: Single current cell structure

$M_{CURRENT\_SOURCE}$ is the current sink transistor, which constantly sinks drain current I. $M_{CASCODE}$ is the cascode transistor, which ensures that the V_{DS} variation of the current

source transistor is minimal, thereby keeping the current I constant. Using a cascode transistor also increases the output impedance of the current sink which is desirable. The current cell consists of a current sink drawing constant current through the load. They are made of NMOS transistors. The majority carrier in NMOS transistors are electrons which have a mobility approximately 2.5 times that of holes, the majority carriers in PMOS devices. This led to NMOS transistors being used as they have an inherent speed advantage over PMOS transistors. The increased mobility also means that, to carry a specific amount of current, NMOS transistors can be smaller in dimension compared to PMOS. The output impedance(r_o) of the current cell is an important factor determining the performance of the DAC. During the operation of the DAC, depending on the input codes, different current cells will be connected and disconnected from the output nodes which makes the output impedance of the DAC, input code dependant. For good performance, the output impedance of the DAC should be as high as possible to prevent output current variations over voltage range. This can be achieved if the individual current cells themselves have very high output impedance. For an ideal current source, the output impedance is infinity, .i.e. the current source could change its node voltage to whatever it is needed to keep the constant current flowing. Figure 3.15 shows an ideal current source and its voltage - current characteristics, which shows the current is constant over voltage variation, indicating infinite impedance. Both NMOS and PMOS transistors biased in the saturation region can be used to realise practical current sources. Practical current sources have limitations such as a limited operating voltage range and limited output impedance. NMOS or PMOS devices are said to be in saturation when the conditions 3.2 are met.

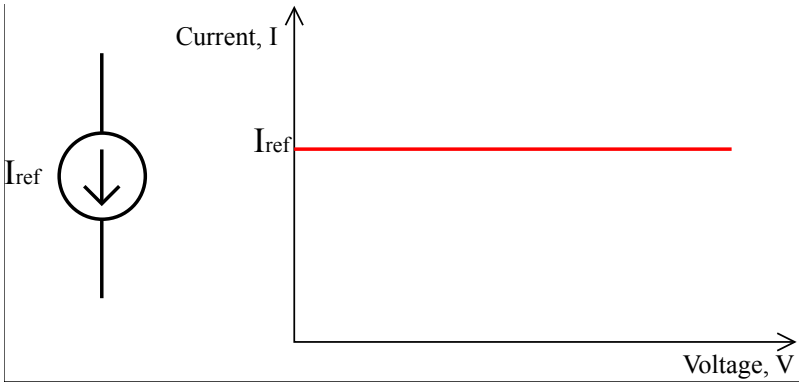


Figure 3.15: Ideal current source and its characteristics

$$\begin{aligned} |V_{GS}| &> |V_{TH}| \\ |V_{DS}| &> |V_{GS}| - |V_{TH}| \end{aligned} \tag{3.2}$$

where V_{GS} is the voltage between the gate and source terminals, V_{DS} is the voltage between drain and source terminals and V_{TH} is the threshold voltage of the MOSFET.

The drain current (I_{DS}) through an NMOS current source can be defined by the equa-

tion 3.3. This equation is a close approximation of the drain current which can be used for quick calculations. More accurate representation of the drain current can be obtained through computer simulations using simulators such as *SPICE* and complex transistor models.

$$I_{DS} = \frac{\mu_n C_{OX}}{2} \frac{W}{L} (V_{GS} - V_{THN})^2 (1 + \lambda V_{DS}) \tag{3.3}$$

μ_n is the mobility of electrons, majority carrier in NMOS devices, C_{OX} is the gate capacitance per unit area, W is the width of the gate, L is the effective gate length of the NMOS transistor. λ is the channel length modulation parameter, which is a short channel effect indicating the reduction of the channel length of the MOSFET in saturation with increase in drain to source voltage. Channel length modulation results in increase of drain current with increase in drain to source voltage, showing a finite drain to source resistance r_{DS}. μ_n, C_{OX} and V_{TH} are CMOS fabrication process related parameters obtained from documentation provided by the foundry or extracted from simulations using models provided by the foundry.

An NMOS transistor as current source is shown in figure 3.16 and its various voltage to current characteristics are shown in figure 3.17.

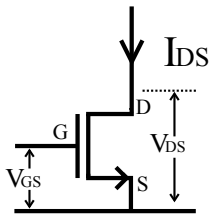
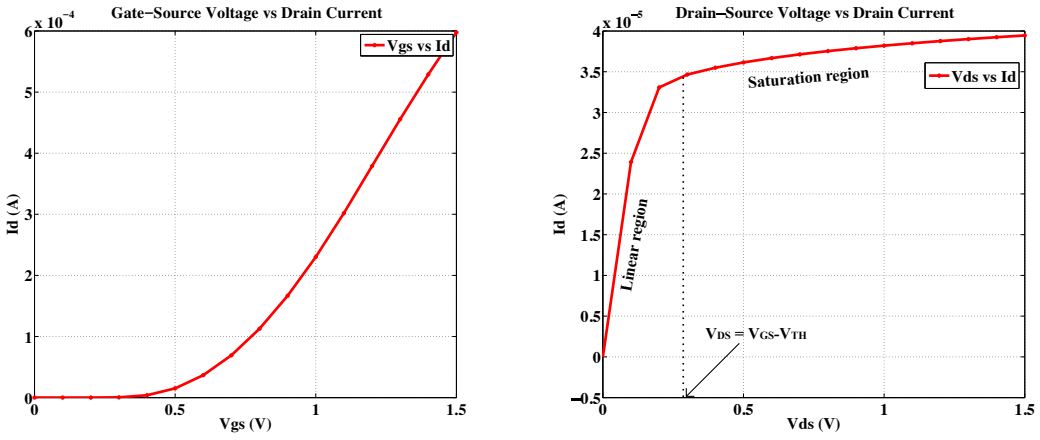


Figure 3.16: NMOS current source



(a) **(b)**

Figure 3.17: NMOS current source V-I characteristics (a) Vgs-Id and (b)Vds-Id

From the figure 3.17b, the NMOS transistor approximates a current source (ignoring channel length modulation and finite output impedance) source for V_{DS} greater than

($V_{GS} - V_{TH}$). When V_{DS} is less than ($V_{GS} - V_{TH}$), MOSFET is in the linear region and acts a resistor. The dependence of the output current on the drain to source voltage limits the performance of the MOSFET as good current source.

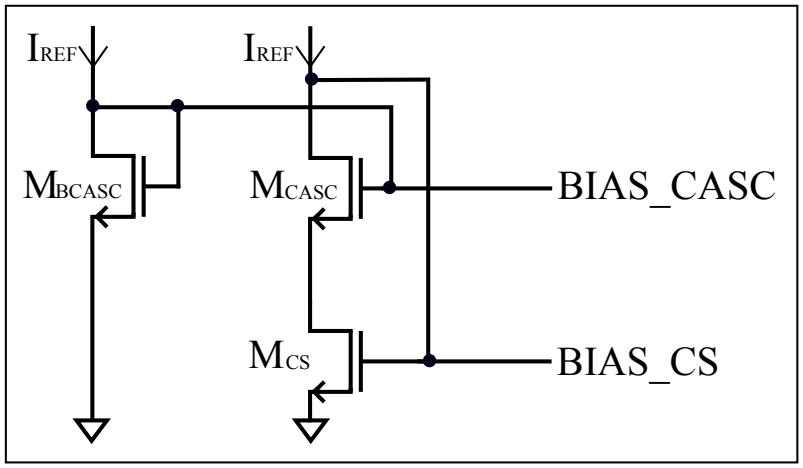


Figure 3.18: Cascode current mirror

3.4.1.2.1 Unit Current cell The circuit diagram of the NMOS based unit current cell is shown in 3.14. Unit current cell is a differential current steering structure which consists of the current source transistor ($M_{CURRENT\_SOURCE}$), cascode transistor ($M_{CASCODE}$), differential current steering switches (M_{SWN}, M_{SWP}) and the cascode current mirror circuit to generate the required bias voltages (*BIAS_CS*, *BIAS_CASC*) shown in figure 3.18. Differential current steering ensures that the current source (sink in this case) will always be able to sink the current from the supply through the load. If there is no current through the current source, the V_{DS} of $M_{CURRENT\_SOURCE}$ will reduce and reach 0 volts, pushing the MOSFET into the linear mode of operation. This is not desirable, since the MOSFET has to be in the saturation region to be a current source/sink. When the current path is established, V_{DS} increases and the MOSFET moves into saturation. This indicates that the operating region of the current source changes between linear and saturation mode if no continuous current path is provided which will introduce distortions in the output current. Providing a constant current also keeps the drain voltage of $M_{CASCODE}$ constant and thereby avoiding parasitic capacitances at that node from charging and discharging, which could add spikes to the current. The sizing of each of the transistors in the unit current cell is explained in the following text.

Section 3.4.1 defines the different current ratios required to realise the 50-50 segmented DAC structure. The maximum drain current I_{Dmax} to be carried through the unit cell is $1mA$. The design strategy for this cell is to get the device sizing for the transistors in the bias generator first (figure 3.18) and then use the same for $M_{CURRENT\_SOURCE}$ and $M_{CASCODE}$ in figure 3.14. Once the unit cell is designed, all other higher currents can be realised in the different DAC cells by multiplying the current source width by the ratio

of higher current to the unit cell current. Equation 3.4, which is a simplified version of 3.3 ignoring channel length modulation can be used to estimate initial values of NMOS transistor width and length. Th values obtained from the equation is fed to the circuit simulator and adjusted based on simulation results.

$$I_{DS} = \frac{\mu_n C_{OX}}{2} \frac{W}{L} (V_{GS} - V_{THN})^2 \tag{3.4}$$

For $M_{CURRENT\_SOURCE}$, it is assumed that the drain current I_{Dmax} is $1mA$ and V_{DSAT} is $300mV$. Since $M_{CURRENT\_SOURCE}$ is part of a current mirror a higher V_{DSAT} is chosen as it is critical for matching. The product of μ_n and C_{OX}, two process dependant parameters are provided by the foundry as gain factor KP_N for NMOS transistors and KP_P for the PMOS transistors. Process parameters for the 1.8V thin oxide devices used in the current cell are obtained from [151].

Using the process related parameters from [151] in equation 3.4 gives the aspect ratio ($\frac{W}{L}$) of $M_{CURRENT\_SOURCE}$ and also M_{CS} in the bias network to be 81.

3.4.1.2.2 Current matching requirements Multiple current cells are used in the DAC to generate the outputs. The matching of currents generated from these current sources is critical to achieving 8-bit linearity. Poor matching results in degradation of the DNL performance of the DAC [152]. A segmented scheme offers relaxed matching requirements compared to a fully binary weighted scheme. To ensure a monotonic linear characteristic the DNL of the DAC should be within $\pm$ 1 LSB and INL within $\pm$ 0.5 LSB. Worst case DNL for this DAC happens at mid-code transition, .i.e when the input code changes from $(2^{N/2} - 1)$ to $2^{N/2}$, where N is the resolution of the DAC. For the 8-bit DAC in this work, this translates to input code transition from 127 to 128. Any code transition results in the some current sources receiving current through the main branch and some through the dummy branch. The current outputs of these current sources, when realised in CMOS technology, can be considered as uncorrelated random variables [152, 153] with mean current I and standard deviation σ_I. Since the output currents are random variables, the DNL of the DAC is also a random variable with a standard deviation of $\sqrt{127}\sigma_I$. For 3σ yield (99.97%), which is common in semiconductor industry we can formulate that,

$$\begin{aligned} 3\sqrt{127}\sigma_I &= \frac{1}{2} I \\ \frac{\sigma_I}{I} &= \frac{1}{6\sqrt{127}} I \end{aligned} \tag{3.5}$$

where I is the LSB current, which is 1 mA for the full scale operation of the DAC in this work. Substituting values and calculating gives σ_I/I to be 0.01. [153] models mismatch

in a CMOS technology and formulates the drain standard deviation using 3.6.

$$\frac{\sigma_I^2}{I^2} \approx \frac{4\sigma_{V_T}^2}{(V_{GS}-V_T)^2} \tag{3.6}$$

where $\sigma_{V_T}^2$ is the variance of V_T which can be equated to A_{VT}^2/WL, where A_{VT}^2 is the V_T matching parameter from foundry, W is the width and L is the length of the current source transistor. A_{VT}^2 for this technology is 10×10^{-9} for the NMOS field effect transistor (FET) transistor used to realise the current source. Substituting the values in equation 3.6 results in WL to be $44.4\mu M^2$ for a $(V_{GS}-V_T)$ of 0.3V.

3.4.1.2.3 Current cell MOSFET sizing From previous sections, the aspect ration W/L and area WL for the current source are respectively 81 and $44.4\mu M^2$, using this information, W for the unit current source is chosen to be $81\mu M$ and L to be $1\mu M$. The width of the cascode is increased from the unit current cell dimensions to reduce the V_{DSAT} and thereby reducing voltage required to maintain both cascode and current source in saturation and thereby lower power consumption. Minimum length devices are not used in current sources for better matching whereas for cascode devices a small length is used. Dimensions of all devices in figure 3.18 are shown in table 3.4. Higher current cells are

Device	W (μM)	L (μM)
M_CS	81	1
M_CASC	248	0.36
M_BCASC	32	1

Table 3.4: Device size of unit current cell and biasing

generated by multiplying the width of unit cell devices with the current ratio.

3.4.1.2.4 Differential switch sizing Current steering action in the DAC is performed by differential switches M_{SWN} and M_{SWP} as shown in figure 3.12. Switches are connected to either LEDs or resistive loads depending on DAC configuration. Midoxide devices, which have thicker gate oxide and therefore capable of withstanding higher voltage than thin oxide devices are used as switches to protect the rest of the circuitry from the large voltage swings expected during operation due to the characteristics of μLEDs used and fixed supply voltage. Complimentary control signals for the switches are generated by the crossover correction latch (figure 3.13). The control signal swings from 0 to 1.8V to turn a switch ON and vice versa for OFF. Realised switch sizes for various currents are given in table 3.5.

Current	W (μM)	L (μM)
1 mA	25	0.7
2 mA	50	0.7
4 mA	100	0.7
8 mA	200	0.7
16 mA	400	0.7

Table 3.5: Switch sizing for different currents.

3.4.1.3 Bias current generation

A biasing strategy is required for the DAC. It is designed to generate the bias currents needed centrally by a smaller binary weighted PMOS DAC, BIAS_DAC and distribute the current to each current cell. As seen in the previous section, each current cell, receives current at the BIAS_DAC input and generates the bias voltages required using the cascode current mirror (figure 3.18). Since bias voltage generation and distribution happens locally in each current cell, parasitic voltage drops can be minimised, thereby minimising errors in the output current. The bias current generated by BIAS_DAC is configurable through the serial interface and can provision the full scale range of the DAC. Circuit diagram of the BIAS_DAC is shown in figure 3.19.

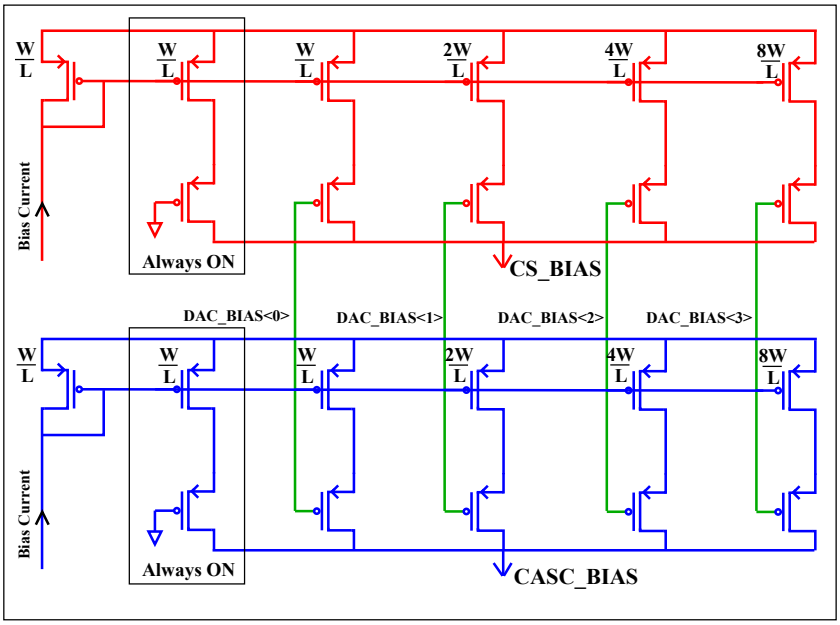


Figure 3.19: BIAS_DAC schematics

The cascode current mirror described in section 3.4.1.2.1 requires two bias currents, thus BIAS_DAC has two outputs BIAS_CS and BIAS_CASC. Each of the outputs are generated by a 4-bit DAC, which receives an external bias current and mirrors it using a binary weighted PMOS current mirror. Binary weighted currents from each branch are gated using PMOS switches which are controlled by the digital bus DAC_BIAS<3:0>.

Since PMOS switches are used, maximum current flows through the output for an input of 0 and minimum current for an input of 15. The outputs when an external bias of 1 mA is applied are shown in table 3.6.

DAC_BIAS				Output currents (mA)	
$< 3 >$	$< 2 >$	$< 1 >$	$< 0 >$	CS_BIAS	CASC_BIAS
0	0	0	0	16	16
0	0	0	1	15	15
0	0	1	0	14	14
0	0	1	1	13	13
0	1	0	0	12	12
0	1	0	1	11	11
0	1	1	0	10	10
0	1	1	1	9	9
1	0	0	0	8	8
1	0	0	1	7	7
1	0	1	0	6	6
1	0	1	1	5	5
1	1	0	0	4	4
1	1	0	1	3	3
1	1	1	0	2	2
1	1	1	1	1	1

Table 3.6: Expected BIAS_DAC outputs

The external bias current can be adjusted to generate a wide range of bias currents inside the DAC using BIAS_DAC.

3.4.1.4 DC Offset current

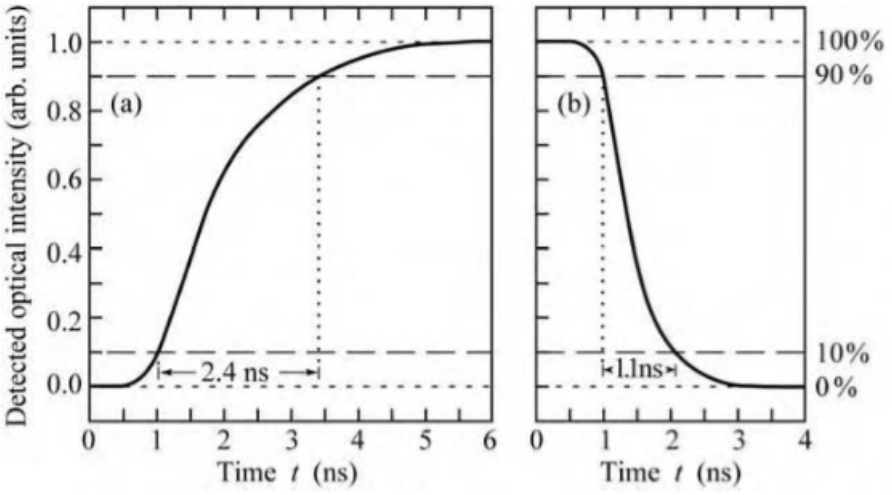


Figure 3.20: Rise and fall time of an LED [97]

[97] discusses the rise and fall times associated with LEDs (Figure 3.20). Rise times of the LEDs could be attributed to either junction or diffusion capacitance where as fall time could be attributed to the voltage dependant carrier sweep out. Limited rise and fall times indicate limited switching speed and thereby limited modulation bandwidth. Rise time can be increased by not letting the LED to turn OFF completely when the DAC is driven with a digital code of 0. To achieve this an DC offset current generator is added to the driver stage.

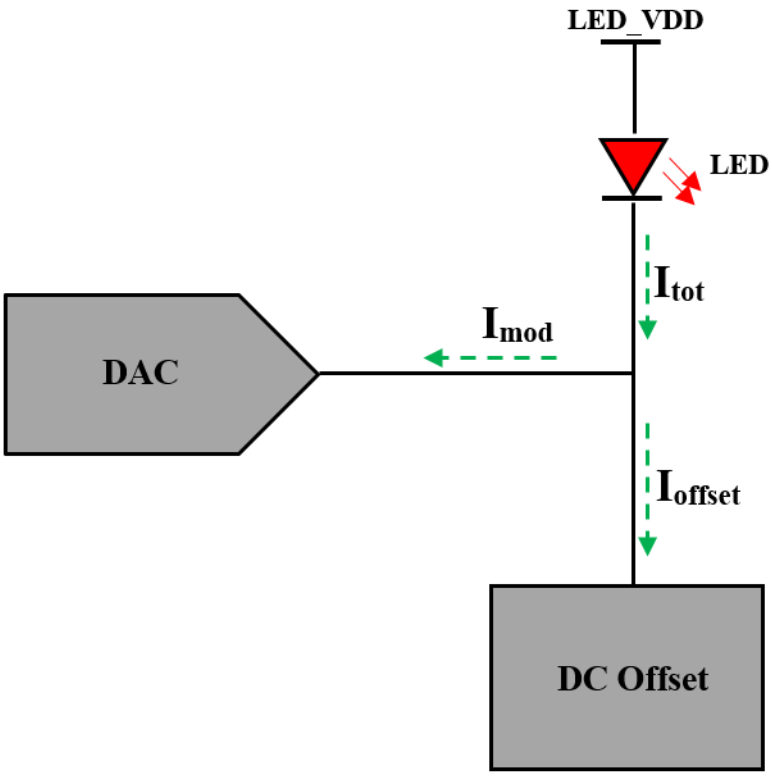


Figure 3.21: DC offset concept

High level wiring diagram of the DC offset generator circuit is shown in figure 3.21. In the figure, I_{tot} is the total current through the LED at any instant which is the sum of I_{offset}, the constant current drawn by the DC offset block and I_{mod}, the modulated current from the DAC driver. The constant current drawn by the DC offset block will act as a base current level for the modulation current from the DAC. If there is no modulation current from the DAC, the light emitted by the LED will be proportional to the DC offset current. The bias point of the LED can be conveniently adjusted.

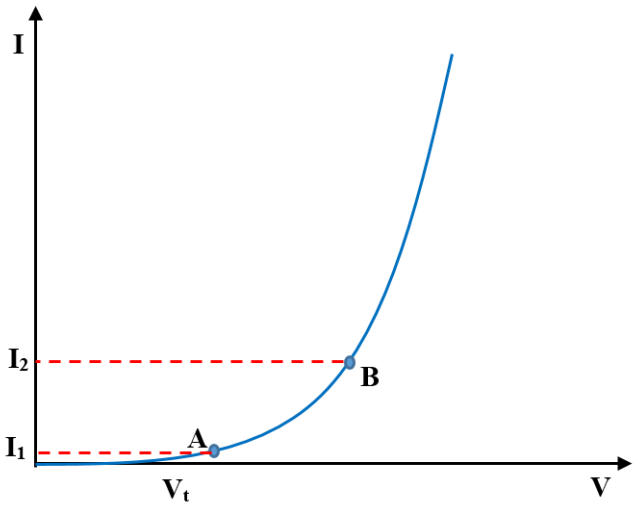


Figure 3.22: Example of DC offset levels

Figure 3.22 shows the I-V characteristics of an LED with two DC offset points, A and B, turn ON voltage V_t. Configuring the driver with an offset A ensures that the LED is not fully turned OFF if there is no modulation current from the DAC, which means the turn ON time can be faster (compared to turn ON from a fully OFF LED) [97]. Data transmission results discussed in section 5.3.4.3 and 5.3.4.5 compares the system performance with and without DC offset and it is clear that, turn ON time is lesser at higher speeds (NMOS drive scheme and DC offset) compared to turn OFF time (no active turn OFF mechanism). This conflicts with the measurement results in figure 3.20 since a voltage mode pulse generator is used to drive the LED, which has an active turn OFF mechanism [154]. The LED will be turned ON and emitting some light if its configured for the offset point B. This configuration is useful to adjust the average lighting level if required.

DC offset setting also protects the MOSFETs in the differential current steering cell inside the DAC by ensuring that most of the voltage is dropped across the μLEDs (they have a higher resistance and therefore a higher voltage is required to draw the same current compared to OTS LEDs) and the V_{DSmax} requirement is not violated. When the DAC is configured for a low bias current, the dynamic range is reduced and brought close to the knee of the transfer characteristics which is not very linear. The DC offset DAC provides the option to move the operating point across the transfer characteristics of the LED thereby achieving a linear mode of operation. The circuit diagram of the DC offset generator is shown in figure 3.23.

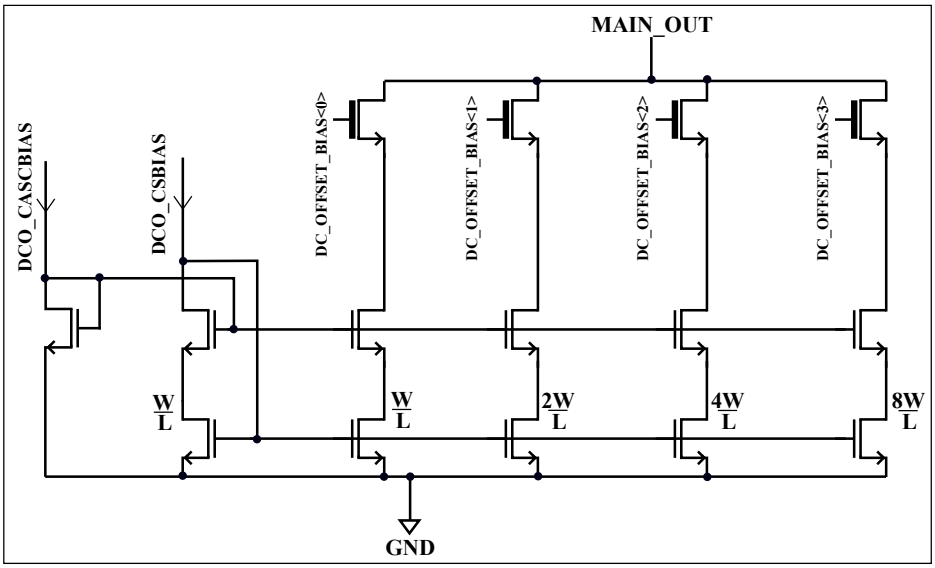


Figure 3.23: DC offset generator

The DC offset is generated by a binary weighted 4-bit NMOS DAC whose output is connected to the main output branch of the DAC. The architecture is similar to the unit current cell discussed in section 3.4.1.2.1, however there is no differential current

steering. The DC offset generator can be configured through the serial interface. The configuration bits (DC_OFFSET_BIAS<3:0>) control the midoxide switches inside the block, which gates the current from main branch to the current sink transistors in this block. An external bias is required to generate the bias voltage for this block. The output configuration for an external bias of 16 mA is shown in table 3.7.

DC_OFFSET_BIAS				
$< 3 >$	$< 2 >$	$< 1 >$	$< 0 >$	Output Current(mA)
0	0	0	0	0
0	0	0	1	8
0	0	1	0	16
0	0	1	1	24
0	1	0	0	32
0	1	0	1	40
0	1	1	0	48
0	1	1	1	56
1	0	0	0	64
1	0	0	1	72
1	0	1	0	80
1	0	1	1	88
1	1	0	0	96
1	1	0	1	104
1	1	1	0	112
1	1	1	1	120

Table 3.7: Expected DC offset generator outputs

3.4.1.5 Chip layout

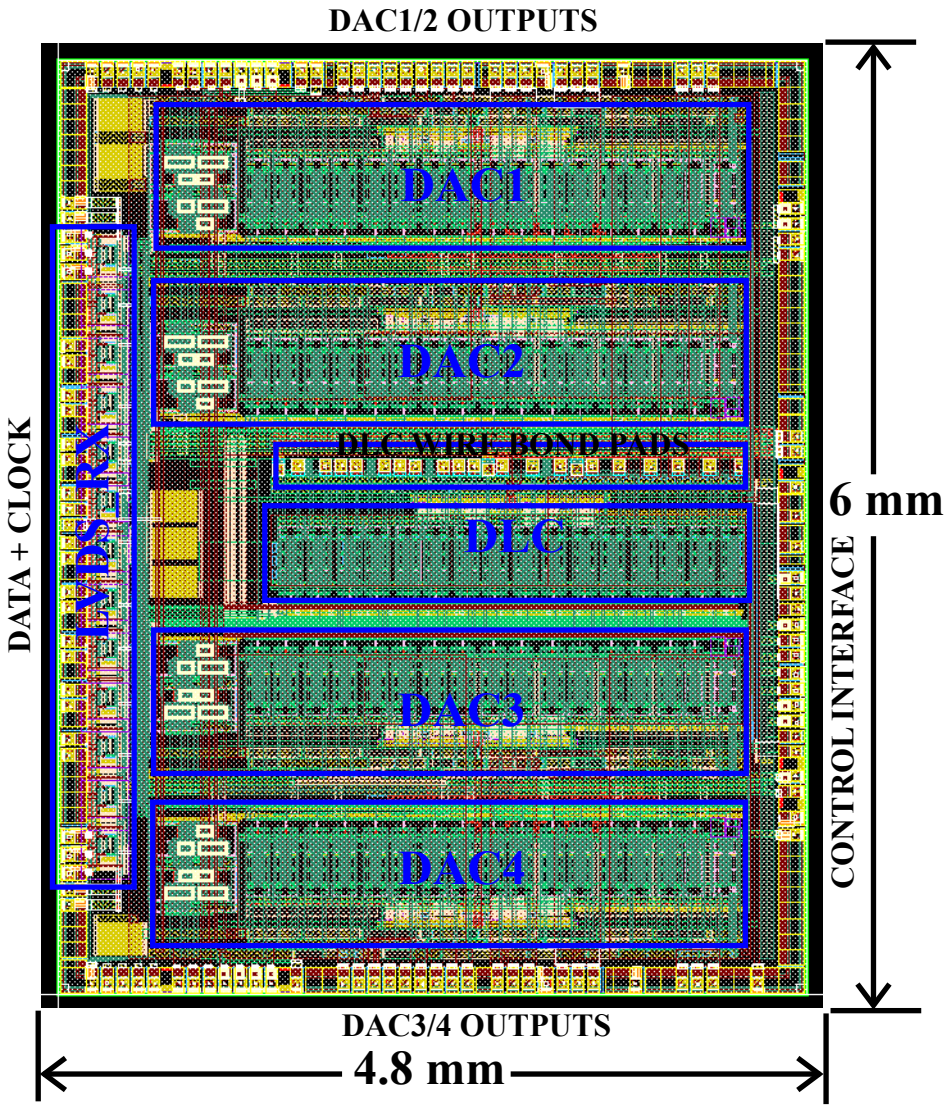


Figure 3.24: Layout of driver chip with major blocks illustrated

The top level layout is illustrated in figure 3.24. The total die area is approximately 29 mm^2. Supply and I/O pads are placed around the periphery of the chip.

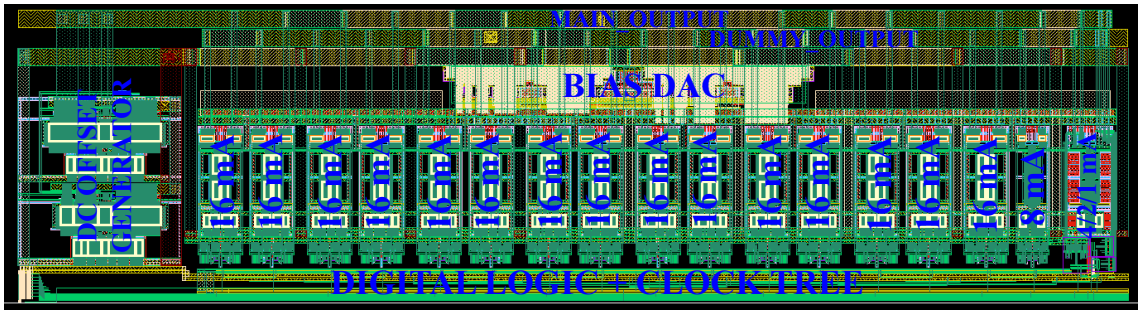


Figure 3.25: Layout of main DAC

Current cells are arranged in a linear fashion as shown in figure 3.25. The bias DAC is placed on top of the current cells, and generates the bias currents for all the current cells. The clock tree and digital logic associated with each DAC are placed beneath the current cells.

3.4.1.5.1 Layout optimisation In the CMOS technology used, the top most metal layer has the least resistance across the chip (0.007 Ω). This layer is used to route the ground net, which is also connected to the source terminals of the current source transistors in the current cells. Any variation in ground resistance will result in mismatch in V_{GS} for the current sources across the chip and thereby mismatch in the current. This results in uneven output characteristics and thereby inferior performance. However for the 5 unary weighted current cells, it was not possible to provide low resistance top layer ground routing due to layout constraints. For these blocks, multiple metal lower metal layers are used to provide the ground path increasing net resistance to 0.2 Ω. The layout of an individual current cell is shown in figure 3.26.

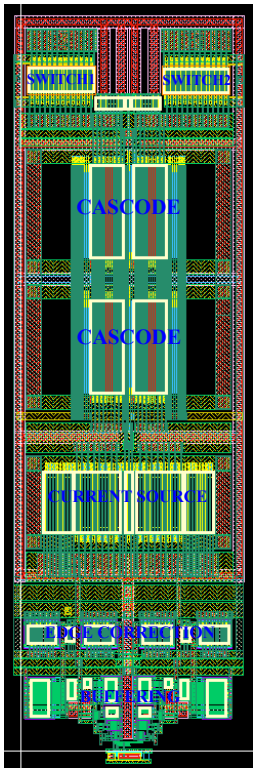


Figure 3.26: Layout of a current cell

3.4.2 Simulation results

3.4.2.1 Current cells: V_{DS} sweep

A constant bias of 1 mA is supplied to the cascode current mirror and V_{DS} is swept. The plots for the different current sources are shown in figure 3.27.

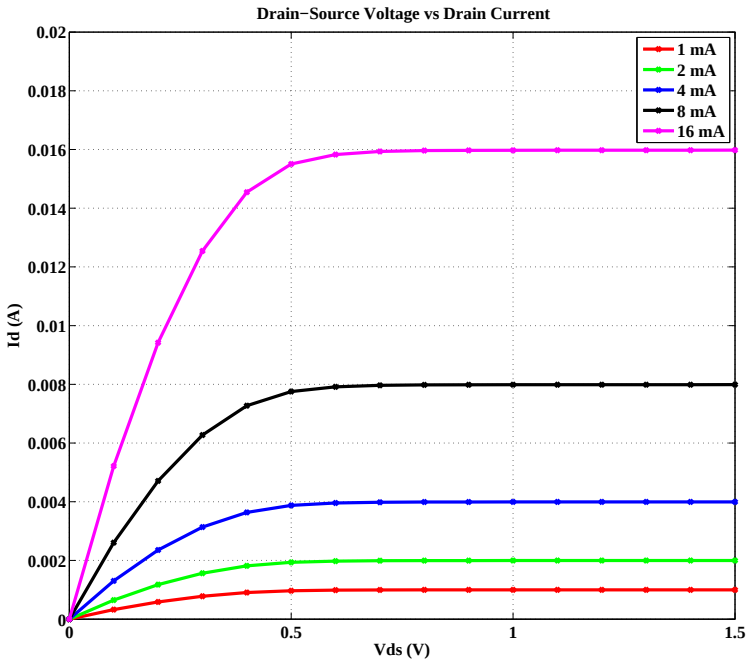


Figure 3.27: V_{DS} sweep of current cells at unit current bias of 1 mA

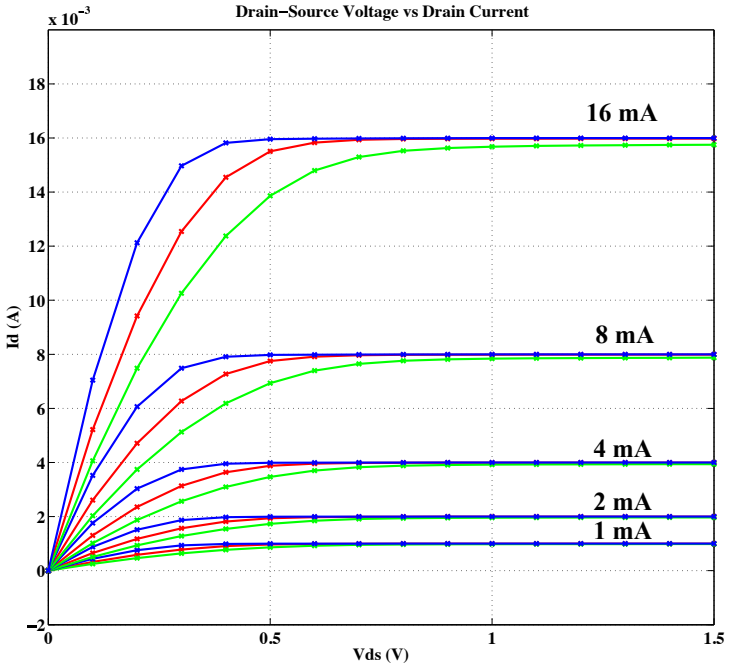


Figure 3.28: V_{DS} sweep of current cells over corners

Results from simulations over two process-temperature corners namely worst power (WP) and worst speed (WS) are shown in figure 3.28 and the current values with variation from the nominal values are summarised in table 3.8. WP corner is has the highest supply voltage (1.98 V) and lowest operating temperature (-40 °C) translating to the highest

power consumption corner whereas WS corner has the lowest supply voltage (1.62 V) and highest operating temperature (85 °C).

Output	WS variation	WS (A)	Nominal (A)	WP (A)	WP variation
1 mA	-1.95%	0.0009788	0.0009983	0.0009997	0.14%
2 mA	-1.90%	0.001959	0.001997	0.001999	0.10%
4 mA	-1.83%	0.00392	0.003993	0.003999	0.15%
8 mA	-1.85%	0.007839	0.007987	0.007997	0.13%
16 mA	-1.82%	0.01568	0.01597	0.01599	0.13%

Table 3.8: Current cell variations over corners at 1 mA unit current and 1 V across driver

3.4.2.2 Current cells: pulsing at 500 MHz

Pulsing of current each current cell at 500 MHz sampling rate is shown in figure 3.29.

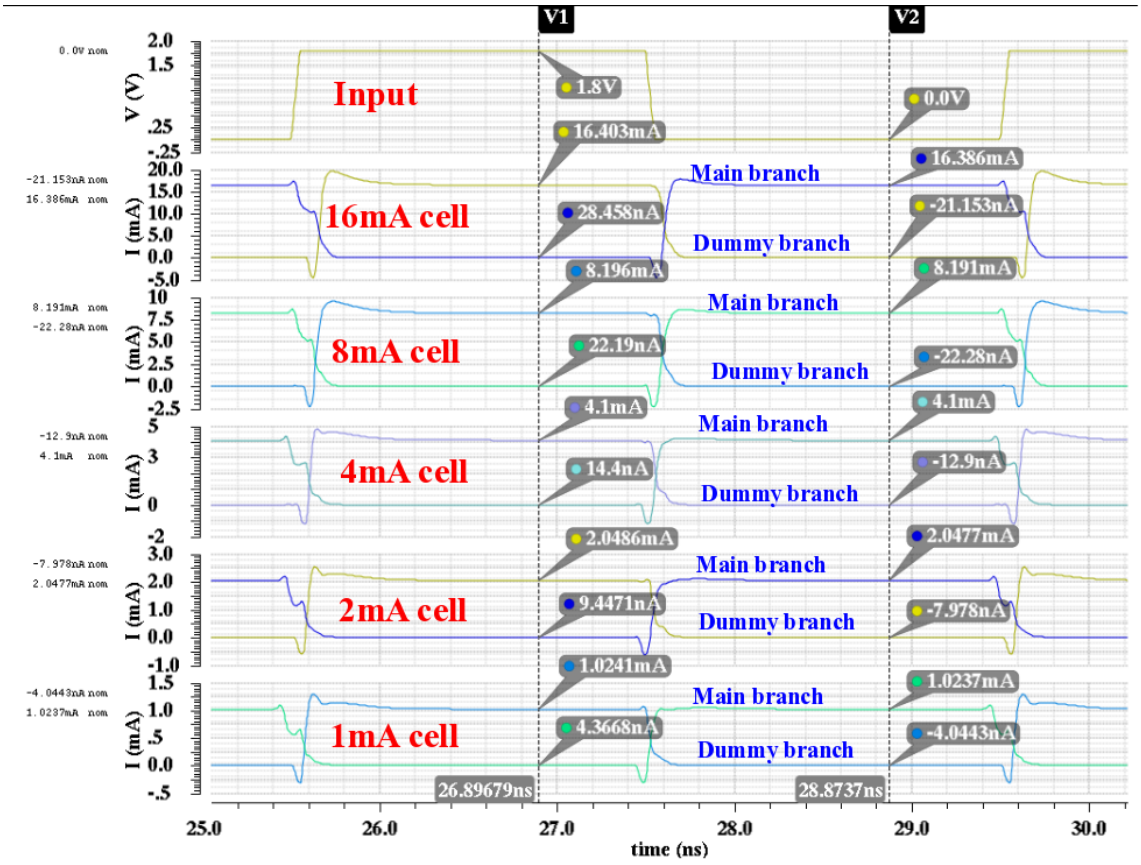


Figure 3.29: Pulsing of different current cells at 500 MHz

The quality of the pulses is affected by the overshoots and undershoots at the rising and falling edges of the current pulses as seen in figure 3.30. However, due to the low pass characteristics of the LEDs being driven, these pulses will be filtered out since they are happens at frequencies greater than 1 GHz.

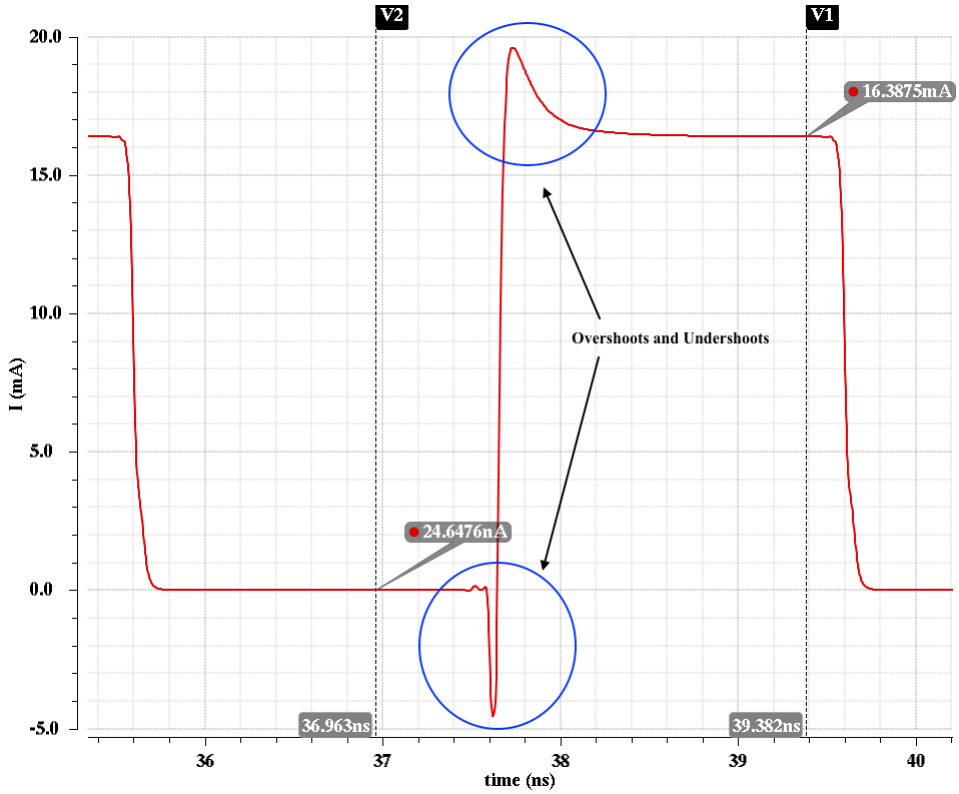


Figure 3.30: Quality of 16 mA current pulse at 500 MHz

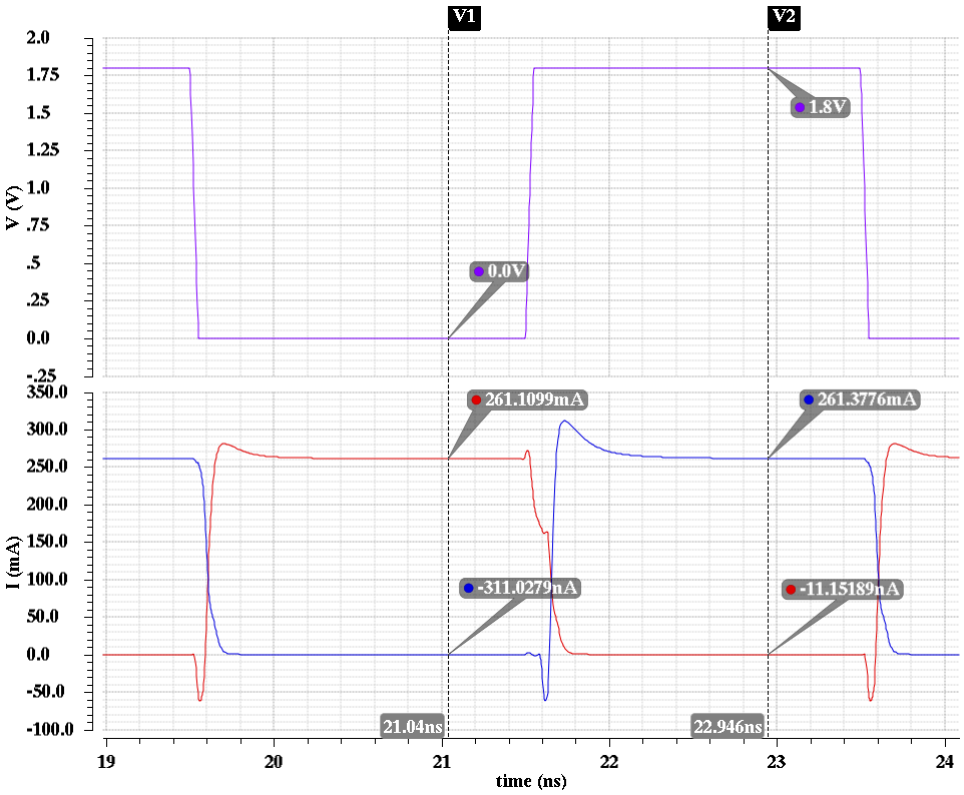


Figure 3.31: Full scale pulsing at 500 MHz sample rate

All current cells combine their output currents to generate the DAC output pulse,

which can be see in figure 3.31.

3.4.3 Digital to light converter (DLC)

The design details for the DLC mentioned in section 2.5.11 are presented here. A 4-bit digital to light converter (DLC) circuit is implemented in the driver chip along with the main DACs for studying the concept and characterising the circuit using a custom built μLED array. The ability to realise a VLC link is also tested. While operating the driver chip in DLC mode, the 4 LSBs from the incoming 8-bit data is decoded into 15 thermometer coded outputs. These thermometer coded outputs are used to drive the current cells. Each current cell can sink a maximum of 16 mA from an LED. The circuit blocks described in previous sections have been re-used in this block, these include the current cell discussed in section 3.4.1.2.1, the bias current generation circuit mentioned in section 3.4.1.3 which adjusts the current through each cell if needed, the clock tree (figure 3.10) and the reset buffering. Since the current cells have two outputs namely main branch and dummy branch, there are 30 outputs, 15 main branch outputs and 15 dummy outputs. The main branch outputs are connected to a customised bond pad array (15x1) placed in the centre of the CMOS die right on top of the DLC block. The μLED array is wire bonded to the CMOS die to establish the electrical connection whereas all the dummy branch outputs are shorted to three custom bond pads. Three more bond pads were provided in the middle of the CMOS die to wire bond the anode connection of the μLED array to an external supply voltage. The supply bond pads are connected to two bond pads at the periphery of the chip and are bonded to the package to connect to the external voltage. The data path and μLED wiring in the DLC are shown in figure 3.32

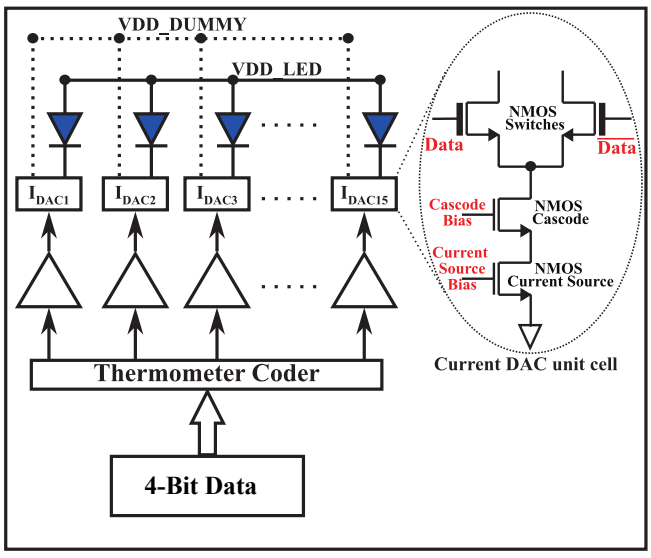


Figure 3.32: DLC data path and μLED array connection

3.4.3.1 μLED array

For the DLC, an Indium Gallium Nitride (InGaN)-GaN μLED array with 16 μLEDs arranged in a linear fashion was fabricated by the University of Strathclyde in a common anode process. Since the LED driver is based on NMOS transistors, the individual cathode connections are required which translates to 16 cathode pads, whereas the anodes are shorted together in the μLED array die itself and connected to three pads for bonding to the CMOS die. Three arrays were fabricated with different metallisation schemes (Pd, Ni/Au, Ni/Au[MI7])at the University of Strathclyde. More details about these arrays and their characteristics can be found in Section 5.4.1. The μLED array is glued on top of the CMOS die for wire bonding as shown in figure 3.34. Modified bond pads ($60\mu m$) are provided at the centre of the CMOS LED driver die to attach wire bonds from the μLED array.

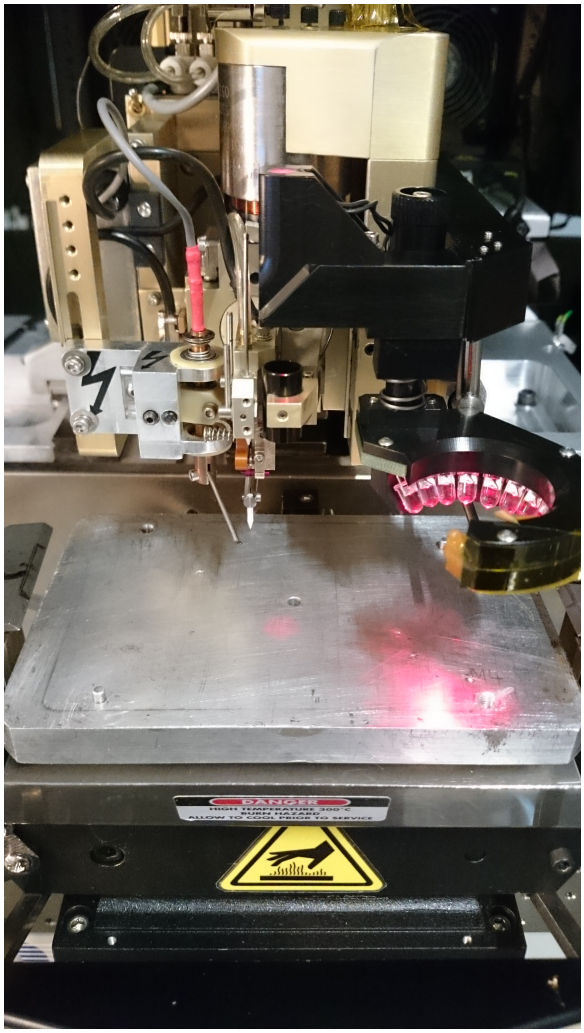


Figure 3.33: Palomar 8000 bonding head

A high speed thermosonic bonding machine (Palomar 8000) shown in FigureBonding was carried out by Optocap Inc. The bonded CMOS-μLED stack is packaged into a 120

pin CPGA package with a transparent lid to aid light extraction. A photograph of the bonded DLC chip is shown in Figure 3.34.

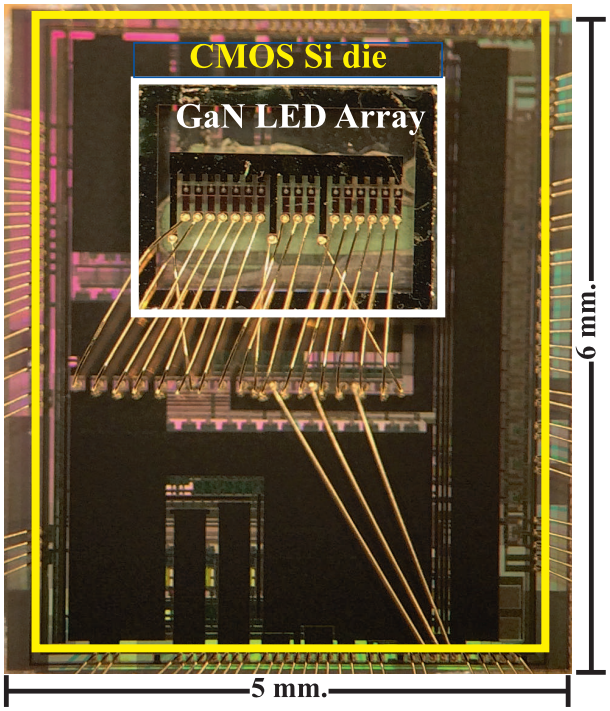


Figure 3.34: DLC wire bonding

3.4.4 LVDS Receiver

An array of low voltage differential signalling (LVDS) receivers are used at the input of the driver chip to sample data, clock and select signals to the chip.

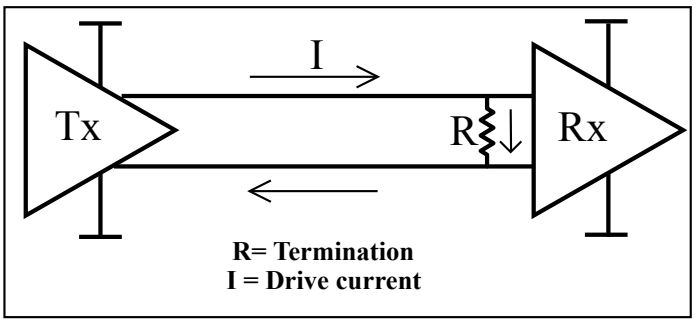


Figure 3.35: LVDS transmission scheme

A LVDS interface is a high speed differential interface which steers fixed current from the transmitter through a transmission line which is terminated with a fixed termination resistance near the receiver (see figure 3.35). The voltage across the termination resistance is the input to a differential amplifier in the receiver and processed to generate a single ended rail-rail signal inside the driver chip. The transmitter changes the current direction, which generate opposite polarity voltages at the termination indicating logic 0 and 1. A

differential scheme has advantages such as noise immunity, common-mode rejection and low voltage swing compared to single ended schemes. A LVDS interface is typically used for inter-chip communication in PCBs and also for inter-PCB communication. Typically a drive current of 3.5 mA is used in the interface with a common mode voltage of 1.2V. A 100 Ω termination resistance generates 350 mV across the input terminals of the differential amplifier at the receiver. The LVDS receiver block used in this work is adapted from [150]. The input differential amplifier in the LVDS receiver is powered from 5V supply and the next stage comparator from 1.8V. An external bias resistor is required to bias this block.

3.4.5 Rest of the Logic circuitry

The logic circuits associated with some of the analogue circuit blocks have been discussed in previous sections. In this section, the rest of the logic circuitry in the driver chip is detailed.

3.4.5.1 Serial interface

A digital configuration interface is provided to configure the driver chip in the right mode of operation. The serial interface consists of a clock (CLK), data (DATA) and sample (RESAMPLE) inputs connected to digital I/O pads in the chip. These inputs are wired to an internal shift register circuit shown in figure 3.36.

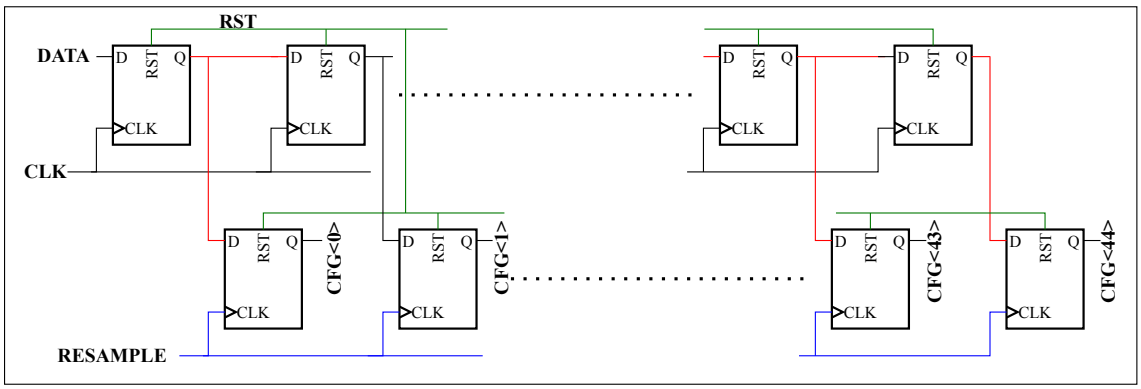


Figure 3.36: Shift register arrangement for internal configuration

The different circuit configurations envisaged requires a total of 45 control bits, which is the number of register blocks in the shift register. 45 bits transmitted serially from an external source is sampled in by the clock, which is also generated externally. 45 clock cycles are required to push in all the bits to the chain of D-type registers. After all the bits are clocked in, a rising edge on the RESAMPLE line samples the output of each D-type to the internal register bank whose outputs are connected to the associated circuit blocks. The operation speed of this interface is not critical to the performance of the VLC

system, however speeds of tens of MHz are possible. The shift register circuit requires 1.8V transistor-transistor logic (TTL) compliant inputs.

3.4.5.2 Clock network

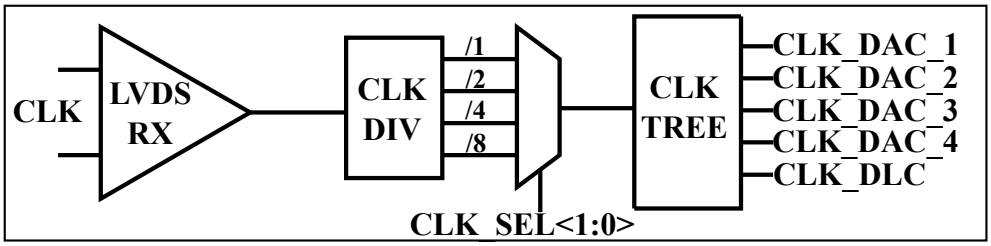


Figure 3.37: Clock networking

The differential clock network is received by the LVDS receiver and converted to a single ended clock to be routed inside the driver chip. Divided versions of the clock are generated which are required for the MIMO mode of operation. Selection of the appropriate clock is done through the configuration bits CLK_SEL<1:0> controlling the clock multiplexer. The selected system clock is fed to the appropriate DACs by a clock tree. A diagrammatic representation of the network is shown in figure 3.37.

3.4.5.3 Data path

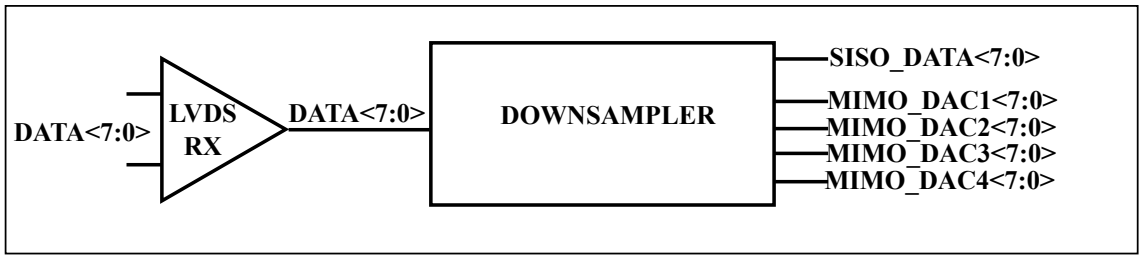


Figure 3.38: Data path

The 8-bit data received through the LVDS receivers is passed on to a down sampling block (figure 4.4). This block copies the incoming data to all DACs for SISO operation and also generates a down sampled version for each DAC in MIMO mode. Operation of the down sampler is shown in figure 3.39.

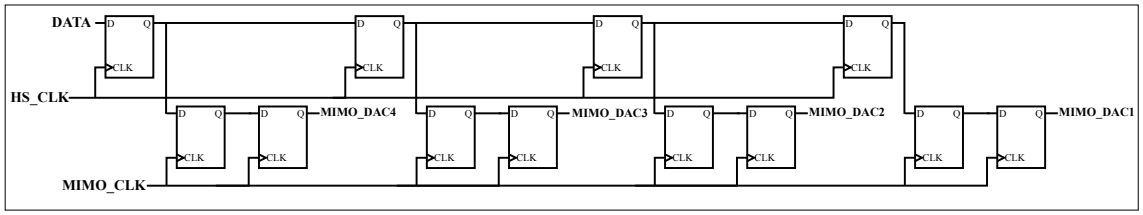


Figure 3.39: Down sampler

3.4.6 Packaging

(b)

(a)

Figure 3.40: (a) CMOS die and (b) Packaged chip

The fabricated CMOS die (figure 3.40a) is packaged in CPGA 120 package (figure 3.40b).

3.5 Summary

In this chapter design details of the LED driver are presented. System level modelling and simulations carried out by Oxford University at the beginning of UP-VLC project provided key specifications for the driver such as bandwidth, the number of drive channels, modes of operation and output current levels. The resolution of the DAC was estimated based on the complexity of pre-distortion required to compensate the non-linear L-I characteristics of the LED. The drive stage design is optimised to reduce power consumption by the driver, thereby increasing the electrical power transferred to the LEDs. The circuit structure is explained in detail following a top down architecture. Each DAC in the driver chip has many sub blocks such as current cells for sinking the current from the LEDs, a biasing network for generation of bias currents, DC offset generator, thermometer decoder and clock tree. The sizing of current cell transistors is carried out based on the unit current requirement and matching criteria for 8-bit linearity. The circuit and configuration details of the bias network and DC offset generator included in each DAC is presented. The layout strategy of the chip is shown from top level to a current cell inside the DAC. An experimental DLC block re-uses the current cells from main DAC, however

bond pads were customised and placed at the centre of the chip for bonding a μLED array fabricated at the University of Strathclyde. DC and transient simulations were performed at current cell level and DAC level to ascertain the performance. The data and clocking interface in the driver chip uses a LVDS standard receiver interface to connect to external devices. The clock network includes a clock divider for generating clocks based on the mode of operation. Similarly in the data path a down sampler is included to split the data to different DACs.

Chapter 4

Characterisation Bench and Results

4.1 Overview

A characterisation platform is required for the electrical characterisation of the driver chip and the visible light communication (VLC) experiments performed using the driver chip. This chapter presents the details of the characterisation platform along with results from the electrical characterisation of the driver chip performed using the platform. The characterisation platform consists of four printed circuit board (PCB)s and associated firmware/software. The CMOS driver chip is mounted on a mother board (MB) PCB which has multiple voltage rails wired to the driver chip. It also provides the different bias currents needed for the DACs and the low voltage differential signalling (LVDS) receiver in the driver chip. In addition to the driver chip, the MB PCB also has connection mechanisms to interface to an external field programmable gate array (FPGA) card and a range of daughter cards for connection to LEDs. A FPGA card from Opal Kelly (OK) can be inserted into the connector base provided in the MB for controlling the driver chip. The high speed clock, 8-bit data samples and enable signals for the DACs, available through the LVDS interface in the driver chip, are connected to the OK board along with the single ended serial configuration signals. Resistors are used to load the DACs for electrical characterisation and the MB has an option to mount these resistors and sample the voltage across them for calculations. Since different types of LEDs (micro light emitting diode (μLED) and off-the-shelf (OTS) LED) can be driven by the driver chip for different VLC experiments, the MB provided options to connect all these LED variants to the driver chip. Subminature version-A (SMA) connectors wired to the DAC outputs are used to interface to the μLED array boards, whereas for OTS LEDs separate daughter cards are required. These can be interfaced to the DACs through the connectors provided. For digital to light converter (DLC) characterisation, the same bench can be used with the wire bonded μLED - CMOS driver chip. To control all the electronics mentioned so far, software is

written at various levels. FPGA logic is realised using the Verilog hardware description language (HDL). Since OK board has a Xilinx Spartan series FPGA, the development environment from Xilinx is used to synthesise and verify the logic developed using Verilog. Data processing, modulation and demodulation are performed using Matlab for VLC experiments. Modulation and demodulation algorithms for OFDM and PAM modulation schemes were provided by ultra-parallel visible light communication (UP-VLC) project partners. Custom Matlab code was developed including the modulation/demodulation algorithms to generate samples for the DACs and process the received data from them. The OK board has to be interfaced to the PC to send and receive data to the FPGA. This is realised using a custom Python interface developed, which can communicate to the OK board using the interfacing software library provided by OK. Before performing VLC experiments, the CMOS driver chip is characterised electrically to understand the various static and dynamic performance metrics. Results of these characterisations are also presented in this chapter.

4.2 Publication List

Electrical characterisation results of the CMOS LED driver discussed in Section 4.4 have been presented at the International Communication Conference, 2015 and published in the conference proceedings [31].

4.3 Characterisation Bench

The functionality of the CMOS LED driver chip designed and fabricated in this work is verified in different stages. This includes basic electrical functional verification, electrical characterisation of the CMOS LED driver to ascertain the performance metrics of the DACs mentioned in Section 2.5.4 and communication or data transmission experiments using different LEDs in order to realise a VLC link. The supporting platform including the electronic circuitry required to interface to the CMOS LED driver, FPGA firmware and software for signal processing and PC interfacing is needed to perform the wide range of experiments mentioned. Instead of realising different experimental setups, a modular approach is followed, where depending on the experiment, components can be interchanged to realise the experiment setup. A characterisation bench was designed and implemented to verify the functionalities of the CMOS LED driver chip in each of the different configurations. The main components of the characterisation bench are listed below.

- **Hardware**
  - Mother board (MB)

  - Opal Kelly (OK) PCB
  - LED daughter board

- **Software**
  - FPGA firmware
  - Matlab firmware
  - Python scripts

Each item in list 4.3 will be discussed in detail in the following sections.

4.3.1 Mother board (MB)

The MB is a multi-layer PCB designed and fabricated to house the CMOS LED driver chip and associated circuitry. The main functions of this PCB are to interface the CMOS LED driver to the digital controller (FPGA), provide power and bias currents and to interface various LEDs to the CMOS LED driver. Circuit schematics for this PCB is created using Mentor Graphics Expedition suite, whereas the layout task was sub-contracted. Full schematics of the MB can be found in Appendix A. Since the MB has multiple power domains with both analogue and high speed digital signals, multi-layer (6-layers) PCB design and fabrication is chosen so that different power domains can be separated and impedance control and length matching could be implemented for high speed digital interfaces such as LVDS. Flame retardant type 4 (FR4) glass based epoxy resin is used to fabricate the 1.6 mm thick PCB which has an area of 203 x 127 mm^2. Layer stack for the

Layer	Type	Notes
1	Signal	Impedance matched
2	Ground	AGND
3	Signal	Impedance matched
4	Power	5 V ,1.8 V
5	Power/Ground	3.3 V, 1.8 V, AGND, DGND
6	Signal	Impedance matched

Table 4.1: PCB layer stack

MB is given in Table 4.1. Signal layers are impedance controlled (100Ω), to satisfy the LVDS impedance matching requirements [155].

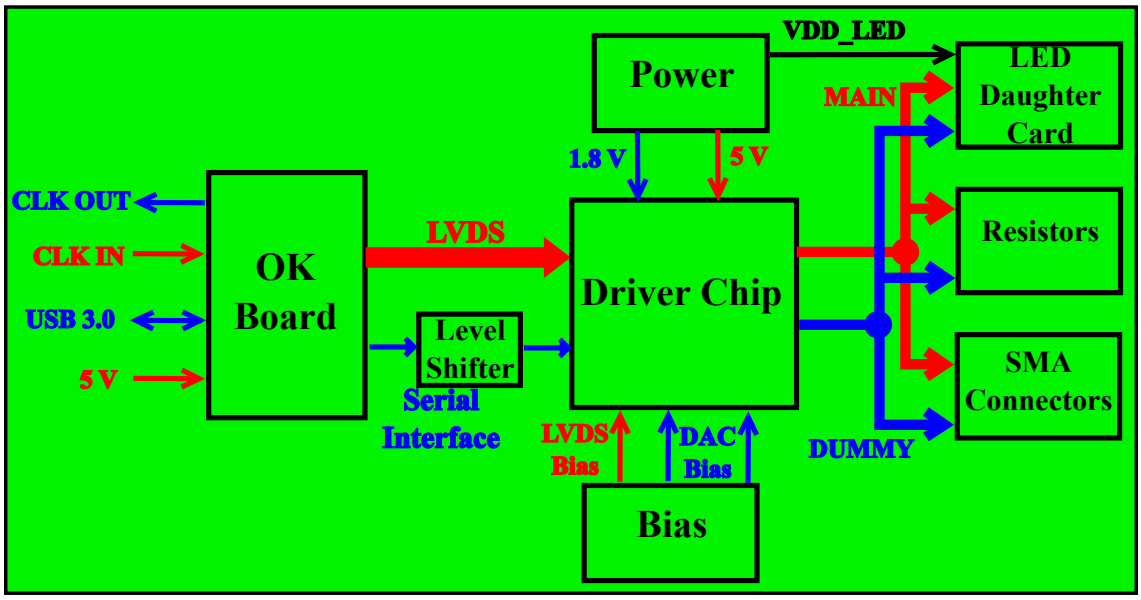


Figure 4.1: Block diagram of the MB PCB.

Figure 4.1 shows the major circuit blocks in the MB. A zero insertion force (ZIF) socket [156] is provided in the MB to install the CMOS LED driver, which allows the IC to be replaced whenever required. Multiple voltage rails are required for various components in the MB. The CMOS LED driver requires 1.8 V and 5 V supplies, and a 3.3 V supply is needed for the logic level translator. Additional voltage rails are required for wiring the LED and dummy loads to the CMOS LED driver. The voltages required can either be locally generated through a number of linear voltage regulators provided on board the MB or can be brought in through a terminal block connected to an external bench supply. Adjustable bias currents to the CMOS LED driver chip are generated in the MB for the DAC biasing, DC offset and LVDS receiver. Potentiometers on board the MB can be used to adjust the bias currents to different blocks in the CMOS LED driver. As discussed in Section 3.4.1, the CMOS LED driver chip has high speed LVDS interface capable of operating up to 500 MHz switching speeds for transferring 8-bit digital data, clock and select signals from an external digital controller. The LVDS traces are length matched in the PCB layout to minimise any timing errors between individual data lanes and clock lanes. For the LVDS interface, a 100Ω termination resistance is required, to generate a voltage drop, which can be detected by the circuitry inside the CMOS LED driver chip. Termination resistors for each LVDS lane are placed in close proximity to the CMOS LED driver chip. Configuration of the CMOS LED driver is performed over the serial interface provided in the chip. Both the LVDS and the serial interface to the CMOS LED driver are wired to an OTS FPGA board (Opal Kelly (OK)) through the connectors provided in the MB. More details about the FPGA card will be presented in Section 4.3.1.2. The FPGA in the OK board generates a single ended serial interface signal at a logic level of 3.3 V, which means a level translator is required in the MB to translate it to the 1.8 V level which

is acceptable for the CMOS LED driver. Serial interface signals (Serial clock, Serial data, Serial latch) and the global reset signal for the CMOS LED driver are level shifted to the 1.8 V logic level. Each CMOS LED driver can drive up to a maximum of 4 LEDs owing to the 4 current steering DACs, however for VLC systems requiring more than 4 channels, it is possible to use more than one MB. To facilitate timing synchronisation, the MB has a clock out and clock in port capable of either supplying a synchronisation clock to another MB / group of MBs or receiving a synchronisation clock from another board or external clock generator. Both clock in and out ports are wired to the FPGA, whose internal circuitry handles the clock management.

The different experiments envisaged require multiple wiring options to different types of loads. To electrically characterise the performance of the CMOS LED driver, resistors are used to load different channels. The MB has mounting options for surface mount technology (SMT) resistors which can be connected to both the main and dummy branches of each channels. Results from electrical characterisation of the DACs are measured using resistors loaded into the MB. The UP-VLC demonstrator system uses μLEDs arrays of different sizes to realise VLC links. The CMOS LED driver outputs needs to be wired to the μLEDs for this purpose. Since the μLEDs are mounted on a separate PCB with their cathodes wired to subminature version-A (SMA) connectors, the MB has a set of eight SMA connectors, wired to both the main and dummy branches of the four channels in the CMOS LED driver. OTS LEDs can be driven by mounting them on a custom designed daughter card (see Section 4.3.1.1) which can be attached to the MB through the daughter card connectors provided. The outputs of the CMOS led driver are wired into the daughter card connector along with the LED voltage rail. It is possible to switch the output of the DACs to any of the outputs mentioned so far dependent on the experiment requirements.

4.3.1.1 OTS LED daughter card

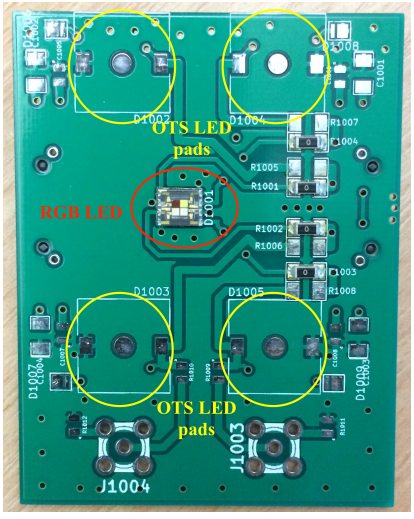


Figure 4.2: Fabricated LED card with options

Figure 4.2 shows the fabricated LED daughter card which can be attached to the MB. It has mounting option for the two OTS LED variants [146, 157] used in the experiments described in Chapter 6.

4.3.1.2 Opal Kelly Board

The CMOS LED driver has digital inputs, both differential LVDS and single ended TTL standard. The LVDS inputs consists of an 8-bit port for data, one clock input and 4-bit select signals. The single ended inputs are the serial clock, serial data, serial select and reset signals. All the digital inputs are interfaced to an OTS FPGA board XEM6310-LX150 [158]. Using an OTS FPGA board reduces the prototyping time considerably due to the availability of pre-designed hardware that can be integrated into our own platform (MB) and the availability of pre-built interfacing firmware/software for quick application development. A functional block diagram of the OK XEM6310 is extracted from the user manual of the board and shown in figure 4.3. The XEM6310 consists of a *Xilinx*

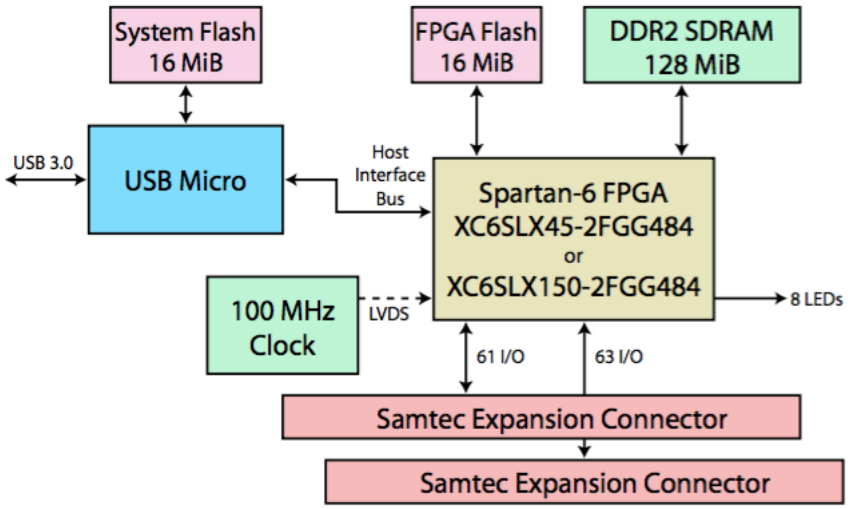


Figure 4.3: Block diagram of the OK daughter card [158]

SPARTAN 6 FPGA and associated circuitry. PC connectivity for the characterisation platform is through the universal serial bus (USB) 3.0 interface on the OK board. The I/O ports of the Spartan 6 FPGA are connected to the expansion headers in the OK board. These I/O ports can be configured as single-ended or differential (LVDS). The clock for the driver chip is generated by the FPGA using the 100 MHz oscillator on the OK board. Based on the configuration, the FPGA can either transfer the data pattern stored in its memory to the DAC or generate standard test signals for the DAC.

4.3.2 Data and Control path

Figure 4.4 shows the control and data path architecture of the characterisation bench. This bench is used to perform all the experiments in further chapters. A PC is used to generate

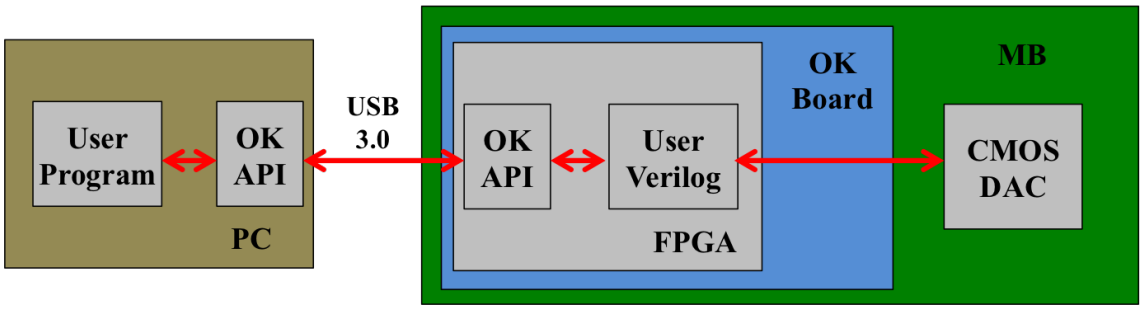


Figure 4.4: Data and control path in the characterisation bench

the data and control sequence for the DAC. The physical link between the PC and the OK board is through a USB 3.0 interface. A user program in the PC (written in Python) is used to communicate with the OK board through the application programming interface (API) provided by *Opal Kelly*. The functionality of this program is presented in Section 4.3.2.2. The FPGA in the OK board had custom firmware developed for it which controls the sending of data, control and clock signals to the DAC based on the commands from the PC (see Section 4.3.2.1).

4.3.2.1 FPGA Firmware

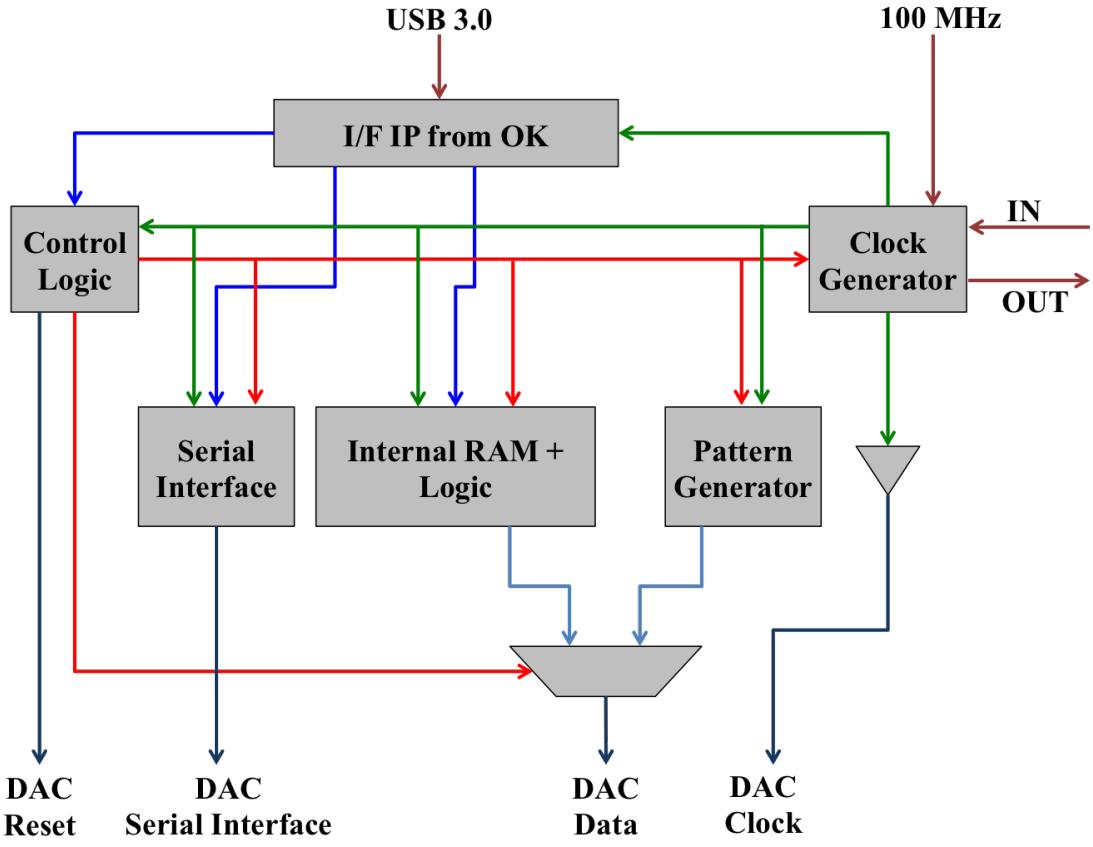


Figure 4.5: FPGA Logic

The FPGA firmware required for the project is developed using the Verilog hardware description language (HDL). *Opal Kelly* provides supporting logic to connect the Verilog modules to the outside world through the USB 3.0 interface. The *Xilinx* ISE™development suite, version 14.4, was used for compiling the Verilog firmware and generating the required binary files, which can be programmed into the FPGA. The main functions of the FPGA are listed below.

- Receive data and commands from PC
- Process received commands as needed
- Re-format data so that it is suitable for the driver chip
- Generate standard signal pattern for the DAC
- Generate control and clock signals for the DAC

A block level representation of the firmware functionality is given in Figure 4.5. The control logic is responsible for decoding the incoming command from the PC and generating the appropriate internal control signals for the logic inside the FPGA or external CMOS DAC. The serial interface blocks receive the commands from the PC (set of registers) and converts them into a serial format suitable for the DAC. It also generates the sampling clock and latch signal for the DAC serial interface. The 8-bit LVDS data for the DAC is either generated locally in the FPGA by the pattern generator or received from the PC and stored in the internal memory of the FPGA. The pattern generator can generate standard functions such as sinusoid, triangle, ramp and square waveforms. Through the PC, the user can select the appropriate signal source in the FPGA. The clock generator block in the FPGA generates and distributes clock signals for internal blocks and external circuits. An oscillator on the OK board generates a 100 MHz clock, which is received by the clock generator and used to generate all internal and external clocks. It also has the option to receive an external clock to be used for synchronisation if multiple MBs are used in an experiment. In such multiple driver experiments, one board will be generating the master clock which will be distributed to other boards. To facilitate this a clock output option is also provided. A single ended to differential buffer is used to generate the LVDS clocks for the DAC.

4.3.2.2 Python program

To interface a PC to the OK and through it the driver chip, a computer program was developed in the Python programming language (*www.python.org*). The program is able to do the functions listed below in the sequence,

- Setup the communication link to the OK board through the USB 3.0 interface.

- Program the FPGA on the OK board.
- Reset the FPGA logic and driver chip.
- Send the configuration bits for control registers in the driver chip.
- Select the appropriate output data stream for the driver chip.
- Issue commands to the driver chip to start driving the data stream to its output.

Sample code is available at Appendix A.

4.3.2.3 Matlab firmware

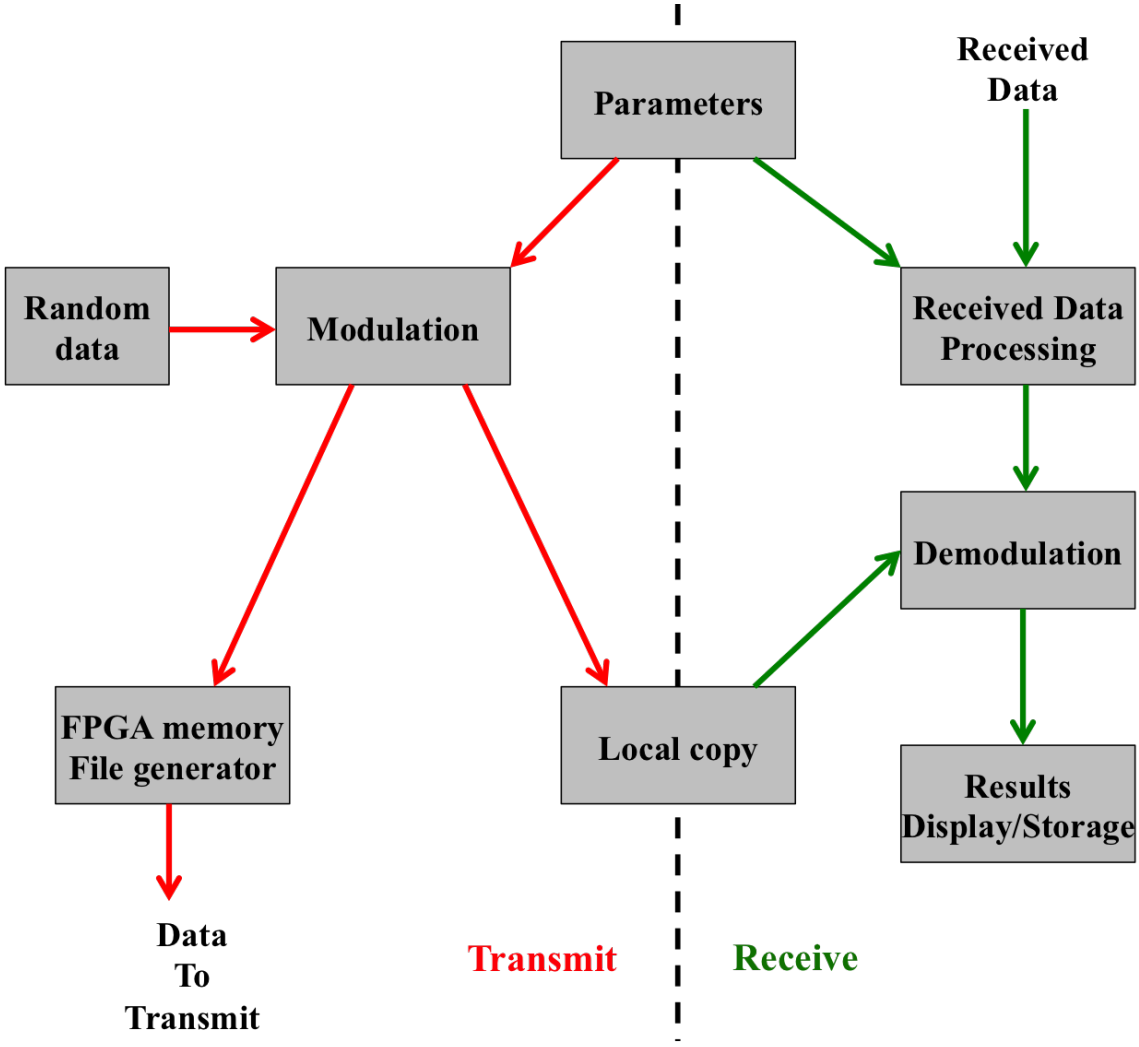


Figure 4.6: Matlab firmware flowchart

Matlab is used to generate the data stream to be transmitted through the driver chip. A set of parameters are used to modulate the data to be transmitted and demodulate the received data. The parameters depend on the modulation scheme used. For example, in

the case of OFDM modulation, the parameters would include the number of sub carriers, QAM levels, Sampling rate e.t.c. OFDM modulation firmware was provided by Institute for Digital Communication at the University of Edinburgh and PAM modulation firmware was provided by Communication research group at the University of Oxford. The modulated data stream is quantised and scaled for the DAC and arranged in the memory file format required for the FPGA compilation software. A local copy of the data is stored for BER calculation. Received samples are processed by the demodulator function. This calculates the BER and estimates other parameters such as SNR and eye diagrams.

4.4 Electrical Characterisation of Main DACs

The functionality of the CMOS LED driver was verified using the characterisation bench. Each block is checked to be functional before performing the DAC characterisation and VLC experiments. Functional checks include the verification of the serial interface, LVDS interface, DAC outputs, bias current and DC offset check. After establishing the functionality of individual blocks, the DACs are characterised to ascertain their performance. The INL/glsdnl of each DACs is checked (see Section 2.5.6.6 for definition of these parameters). SFDR is also characterised to understand the dynamic performance of the DAC.

4.4.1 Experimental Setups

4.4.1.1 Static characteristics measurement setup

For measuring static characteristics, the DACs in the driver chip are loaded with 8.2Ω resistors in both the main and dummy branches. The voltage drop across this resistor while drawing maximum current through a DAC in the driver chip is $256\ mA \times 8.2\ \Omega\ = 2.1\ V$. At least 1.2 V is needed across the current source transistors stack in the output stage of DAC to ensure they remain in the saturation region thereby preserving the linearity of the DAC while driving AC signals from the OK FPGA. Therefore, the total voltage needed across the stack of load and DAC in the driver chip would be at least $1.2\ V + 2.1\ V = 3.3\ V$. A Keithley source meter 2400[159] was used to supply the required voltage needed for the LEDs and DACs. A block level illustration of this setup is shown in Figure 4.7. Measurements are controlled using a modified version of the Python program mentioned in Section 4.3.2.2. It controls the source meter as well as the OK board. The script is capable of configuring the source meter and the DAC bias settings, the input to the DAC,the reading of source meter outputs and doing the necessary calculations on the measured values and then storing the results in PC. The DAC input codes are swept by the program and it reads the voltage across the terminals of the source meter to calculate DNL and INL. This is repeated for each bias setting of the DAC.

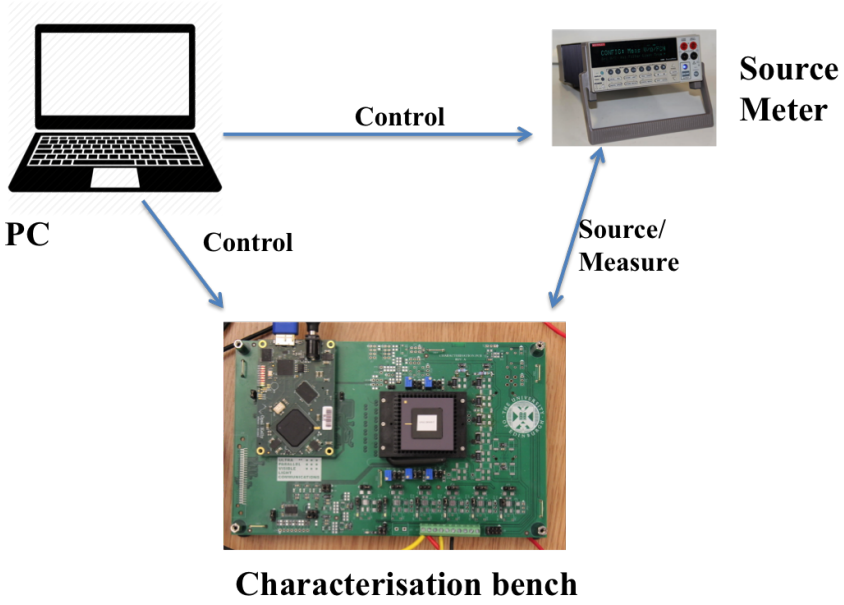


Figure 4.7: Static characterisation bench

4.4.1.2 Dynamic characteristics measurement setup

The measurement of the dynamic characteristics of the DAC involves generating data streams in Matlab and driving it through the DAC. The voltage across the load resistor connected to the DAC is captured using a digital storage oscilloscope (DSO). The captured data is post-processed using Matlab to calculate the dynamic characteristics. SFDR measurements are performed for each bias setting of the DAC.

4.4.2 DNL

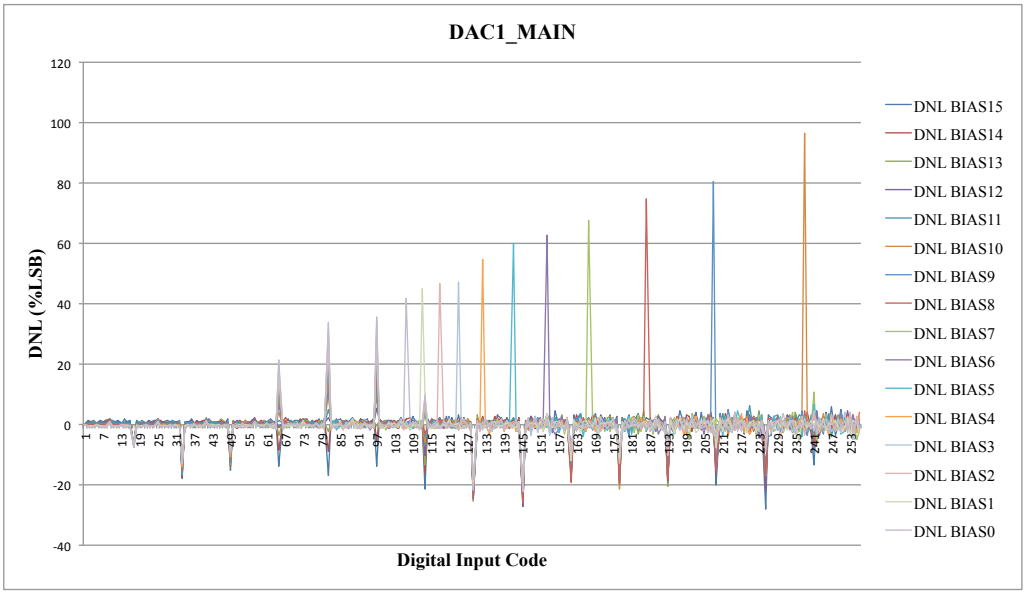


Figure 4.8: DNL measurements at various currents of main branch in DAC 1

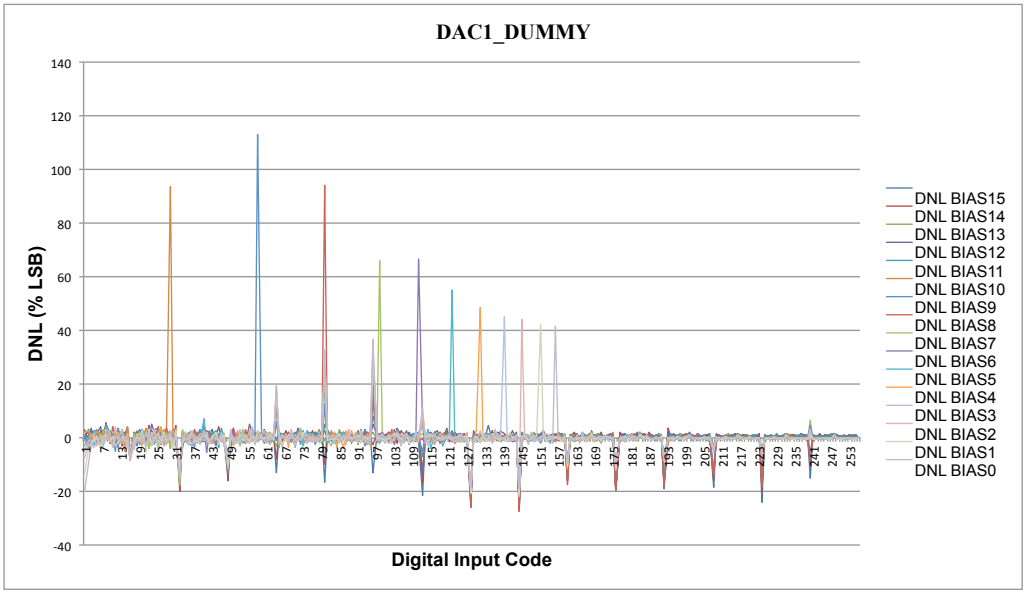


Figure 4.9: DNL measurements at various currents of dummy branch in DAC 1

Section 2.5.6.6 discussed Differential non-linearity (DNL) and its importance in the performance of the DAC. DNL measurements at all bias current settings of the DAC were performed for both the main and dummy branches.

Figure 4.8 and 4.9 shows the DNL measurements from the dummy and main branches of DAC 1. For both the dummy and main branch the measured DNL is close to +90% LSB. This confirms that the DAC is monotonic. From the figures it can also be seen that for every unary cell switching after code 64 the DNL performance deteriorates indicating a poor matching between the unary current levels across the array. In the layout, there is a gap in the ground routing for all cells starting from the fourth unary weighted cell which could cause ground voltage shifts and thereby current mismatch for all the subsequent cells. A similar but reversed pattern can be observed in the dummy branch since the current values are complimentary to the main branch.

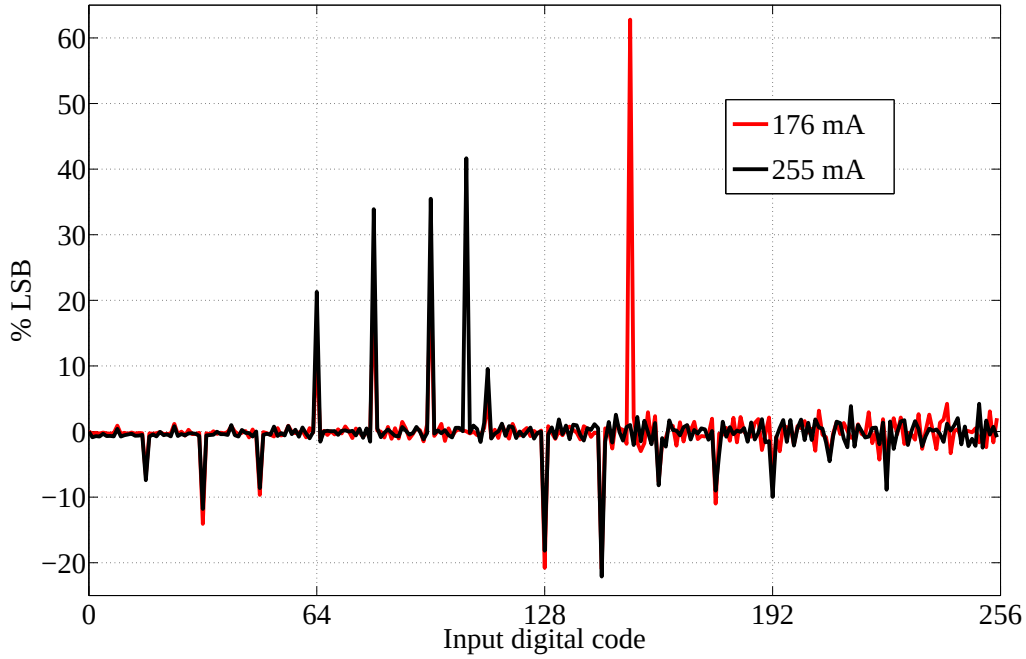


Figure 4.10: DNL measurements at various currents

Figure 4.10 shows a DNL performance of +0.6/-0.2 LSB for full scale currents up to 176 mA. For a full scale current of 255 mA , a DNL of +0.4 and -0.2 is measured. DNL results from the other DACs are similar to the first DAC and can be found in Appendix A.

4.4.3 INL

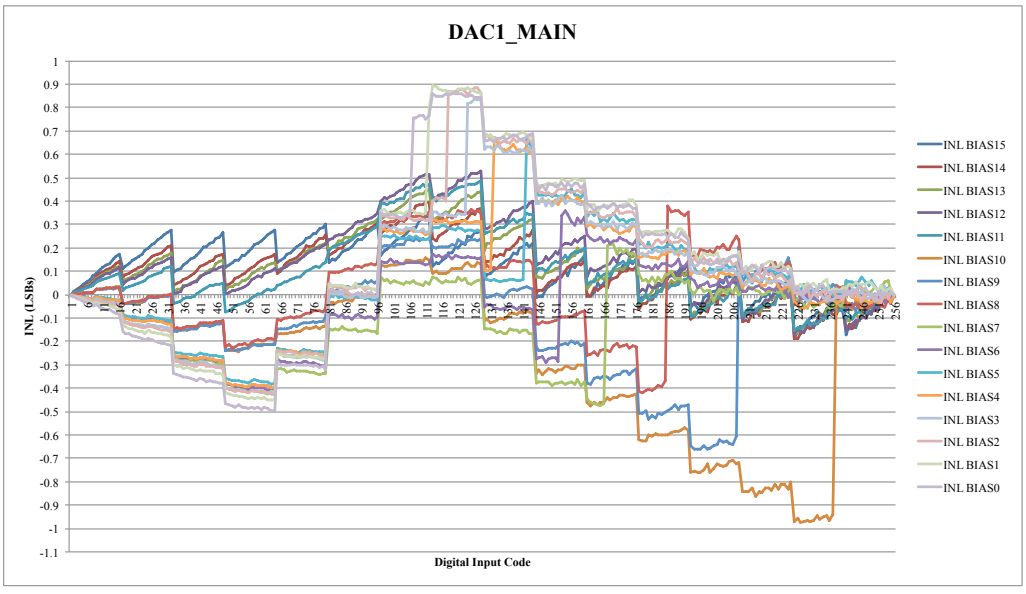


Figure 4.11: INL measurements at various currents of main branch in DAC 1

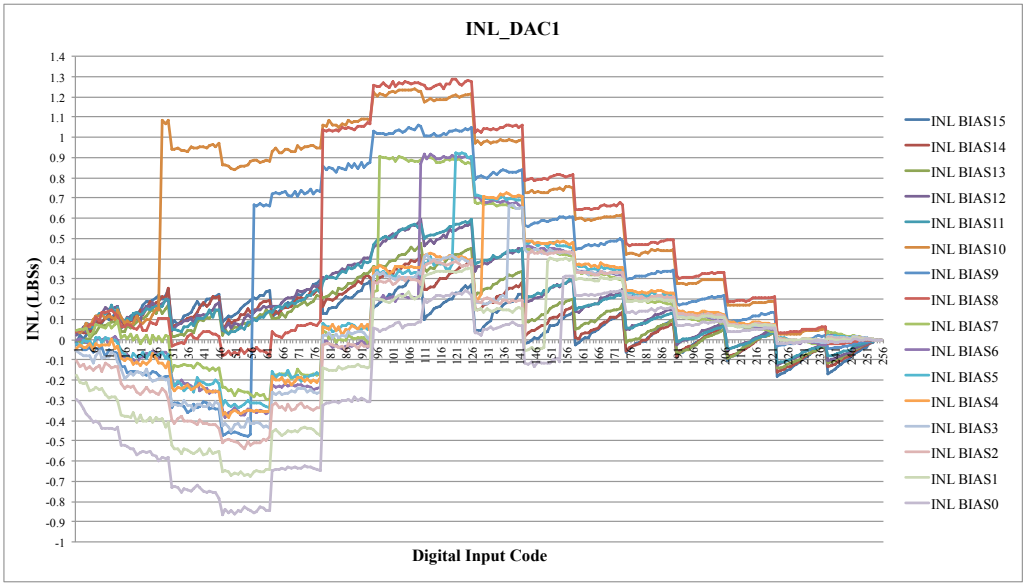


Figure 4.12: INL measurements at various currents of dummy branch in DAC 1

Figures 4.11 and 4.12 shows the INL measurements over the full scale currents of from 16 mA to 255 mA. For higher bias currents the INL performance is greater that 0.5 LSB which means the DAC does not confirm to 8-bit linearity.

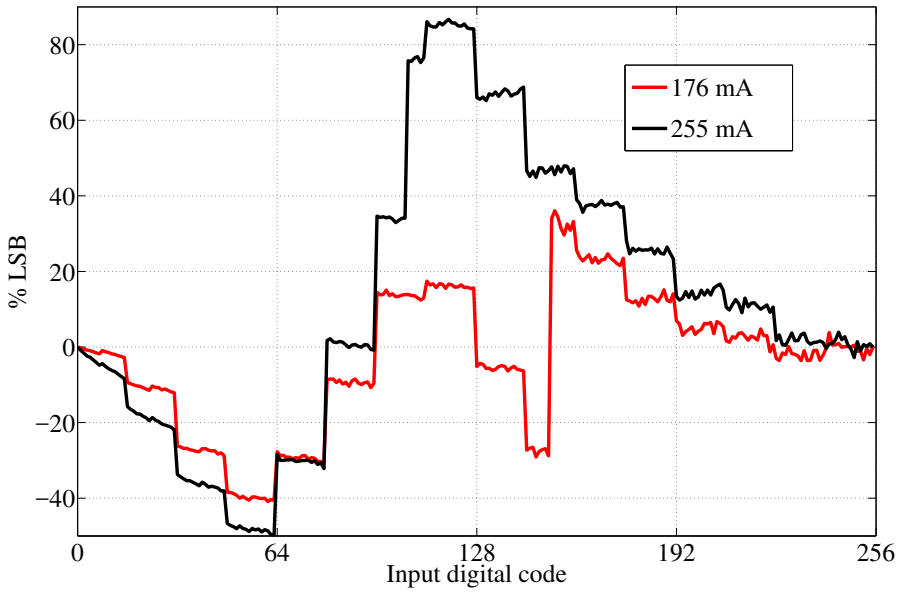


Figure 4.13: INL measurements at various currents

Figure 4.13 indicates that for a 176 mA full scale current, DAC 1 is 8-bit, while at 255 mA the linearity drops.

4.4.4 SFDR

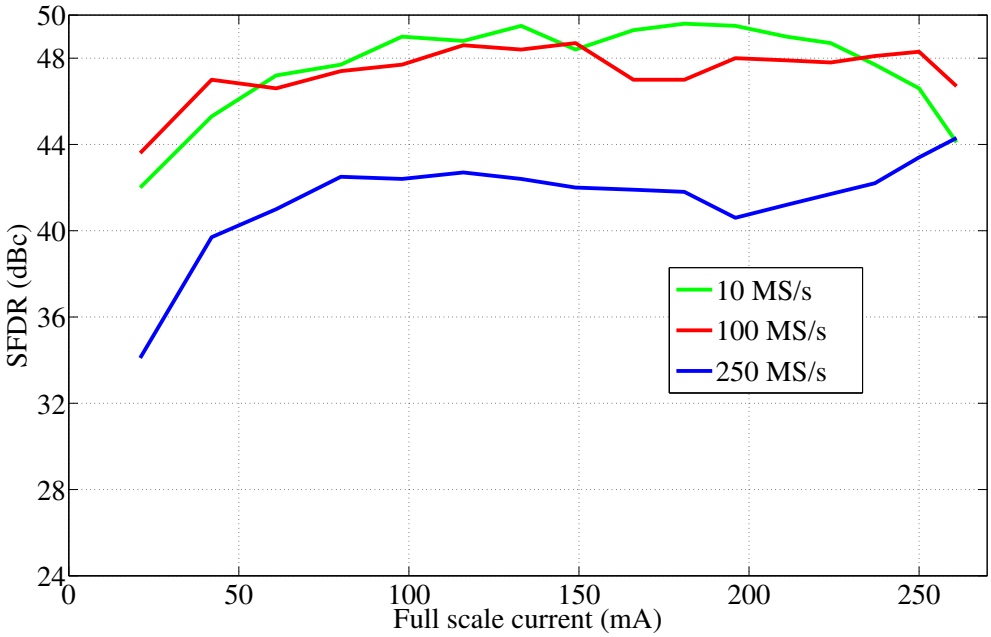


Figure 4.14: SFDR measurements at various currents

Figure 4.14 shows SFDR results from single tone measurements for different sampling rates, from 10 MS/s to 250 MS/s and different bias currents up to the 255 mA. A SFDR of 48 dB is achieved at sampling rates up to 100 MS/s. At the highest sampling rate (250 MS/s), 44 dB SFDR is achieved. At low full-scale currents, the SFDR is lower. This can be attributed to increased mismatch at lower bias currents. Glitch performance, linearity of the DAC and coupled digital noise in the MB ground net influence the SFDR performance. SFDR reduction at higher sampling rates is explained by degraded glitch performance and MB ground net variations due to digital noise coupling. This means at 100 MHz sample rate, the DAC linearity is close to 8-bit where as at 250 MHs, it drops to 6 bits. Reduction in linearity translates to an increase in BER while using modulation schemes such as OFDM.

4.4.5 Data transmission

The data rate achievable using the driver chip is measured while using the resistive load. An OFDM modulated stream is used to drive the DAC which results in proportional current variations at the output and thereby voltage variations across the load resistors sampled by the DSO. For OFDM transmission, the channel is estimated using a sequence

Sampling Rate (MS/s)	QAM levels	Bitrate (Mbps)	BER
100	16	200	$< 10^{-4}$
250	16	500	$< 10^{-4}$

Table 4.2: Electrical data rate measurements.

of pilot frames: pre- determined OFDM frames, which are known at the receiver. The OFDM demodulator estimates the noise power and signal power of the received data to calculate the SNR of the system. Table **??** summarises the electrical data rate measurement results in differential mode from DAC-1. The number of bits transmitted (32000) limits the BER estimation accuracy. Figure 4.15 shows the constellation diagram for 250 MS/s 16-QAM. Electrical data rate measurements were performed differentially where the difference voltage across the dummy branch and main branch resistor is demodulated; this cancels out the common mode ground noise induced in the MB. Up to 500 Mbps were achieved using the DAC and was limited by the clock output from the FPGA.

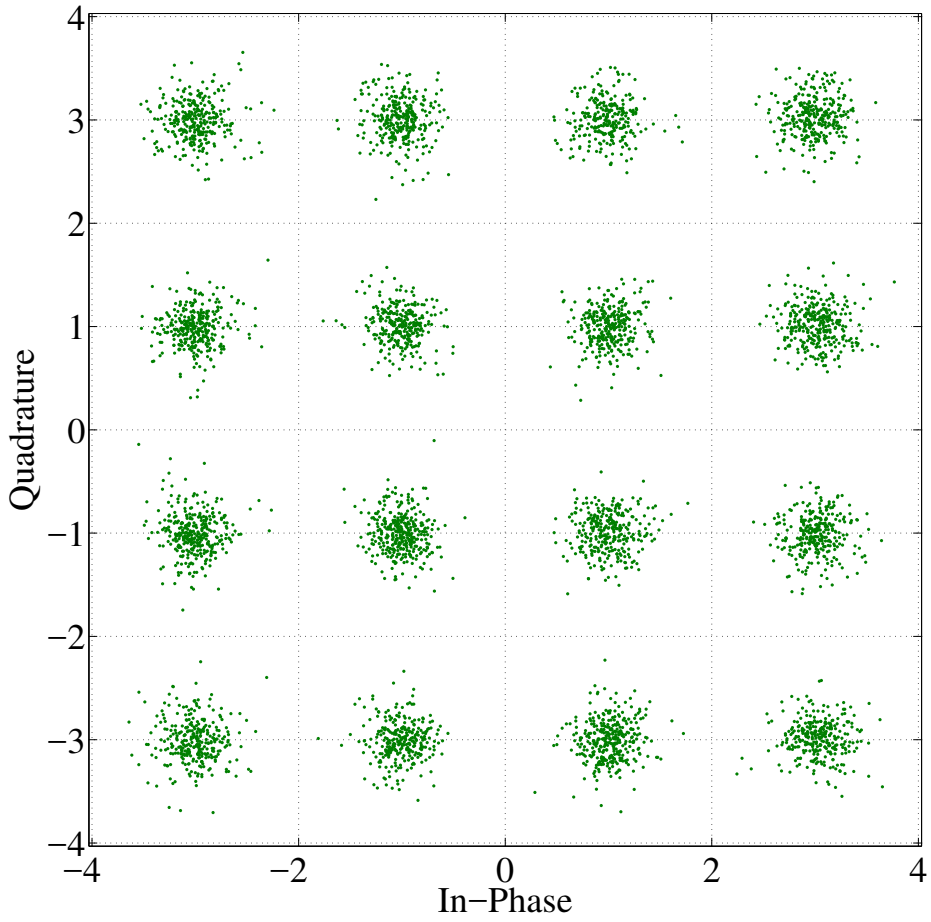


Figure 4.15: 16QAM at 250 Msps electrical

4.4.6 Voltage compliance

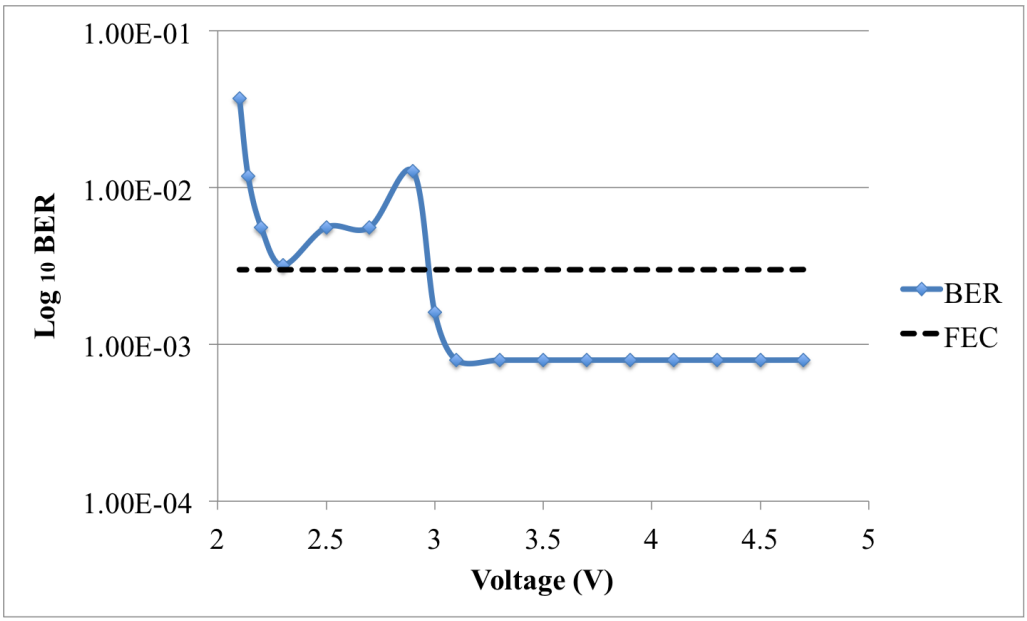


Figure 4.16: Supply voltage vs BER

Voltage compliance of the DAC is measured by using an OTS LED load. The turn on voltage for the LED used is 1.95 V. While transmitting an OFDM modulated signal, the supply voltage is gradually reduced to see at what voltage point the BER goes above the FEC limits. From Figure 4.16 it is seen that at approximately 3 V, the BER goes above the FEC limit. This means the voltage across the DAC at this time is $3V - 1.95V = 1.025V$. This shows that even at 1.02 V, the DAC is able to sustain data transfer and this value is lower than our initial estimate of 1.2 V. Even though this is an optical experiment, the results are more suitable for the electrical characterisation section and hence here.

4.5 Summary

This chapter described the details of the characterisation bench designed and fabricated to test the CMOS LED driver. The bench consists of a MB and associated daughter cards. The MB houses the CMOS LED driver chip and at the same time provides the required voltages and bias currents. It also interfaces to an OTS FPGA card for data streaming, PC interfacing and DAC control. To drive OTS LEDs, a daughter card is fabricated which can house different types of OTS LEDs. For μLED wiring, suitable SMA connects are provided. Sanity checks were performed to ensure full functionality of the CMOS LED driver chip before doing full electrical characterisation including data transmission. DNL characteristics indicated that the DAC is fully monotonic but that linearity drops at higher full scale currents. Dynamic measurements indicated that the performance of the system

deteriorates at higher sampling rates.

Chapter 5

μLED based experiments

5.1 Overview

This chapter presents the results from μLED based VLC experiments performed with the CMOS LED driver chip discussed in Chapter 3. In addition to the components and firmware 5described in chapter 4, suitable receiver circuitry (APD and associated circuitry based on a custom CMOS APD [36, 35] array or OTS components [160]) were required for testing. μLEDs, owing to their higher modulation bandwidth are well suited to high speed optical communications as discussed in Section 2.4.4. The UP-VLC demonstrator specifications resulted in the realisation of two different types of μLED arrays for SISO and MIMO schemes. Details of these arrays fabricated using GaN in a common anode process are presented in this chapter. Unlike, previous incarnations of CMOS drivers for μLEDs that used PMOS transistors, an NMOS based drive scheme is implemented in this work to achieve a higher speed of operation. To facilitate the NMOS drive scheme, a common anode fabrication method is used for μLEDs. Electrical and optical characterisation results from these arrays along with their construction details are presented in this chapter. Even though VLC links have been reported operating at Gbps speeds using μLEDs, several limitations could be observed in those systems such as incompatibility with complex modulation formats [63], limited link distance [21] or use of bulky laboratory equipment to drive the μLEDs [83, 65]. The UP-VLC demonstrator aims to achieve a Gbps VLC link using μLED arrays and the custom built integrated CMOS transmitter mentioned in Chapter 3 at a link distance of 1 m. Various experiments were performed to ascertain the performance of the demonstrator in different combinations of DAC settings, modulation formats and μLED array combinations. A commercial AWG was also used to drive the μLED array to compare the performance of the integrated CMOS LED driver and understand shortcomings if any. The integration of CMOS driver chip and μLED array into a single package is a key step towards realising miniature VLC enabled light

sources with many possible applications including IoT. Details of the new custom 16x1 μLED array fabricated in common anode process is given. As part of this work, an experimental circuit block in the driver chip (see section 3.4.3) was wire bonded to a custom built μLED array to realise a DLC. Experimental results obtained from this integrated CMOS - GaN package is presented in this chapter.

5.2 Publication List

This chapter presents UP-VLC system demonstrator whose design aspects are published in [35]. Characterisation results from UP-VLC system demonstrator including CMOS LED driver are published in [161]. Digital to light converter (DLC) system and characterisation results are published in [32],

5.3 UP-VLC System Demonstrator

One of the primary aims of the UP-VLC project is to realise a VLC demonstrator with high data capacity utilising μLED arrays and integrated electronics. Usage of integrated components and low area profile μLEDs provides a path towards miniature, power-efficient and mass producible VLC systems that could be used in portable devices with limited power availability. High data rates are always desirable in any wireless system including VLC to satisfy the growing demand. Different techniques can be employed at different stages of the VLC system to improve data rate performance. The limited modulation bandwidth of OTS LEDs can be overcome by using equalisation schemes or by using high bandwidth μLEDs at the cost of reduced transmit power. Flavours of complex modulation schemes capable of transmitting more bits per Hz such as OFDM or L-PAM can be used to increase the data rate of a VLC system. But these schemes depend on SNR possible with the system, limited by factors such as transmit power, link distance, receiver area etc. Another approach to increase the bandwidth of the VLC system is to use MIMO method, which is popular in the RF domain [162]. In a MIMO scheme, multiple transmitter and receivers are used to simultaneously transmit information increasing data rate by efficient spectral utilisation. Since multiple LED luminaries are present in a real lighting scenario, a MIMO scheme can be used in VLC systems to enhance data rates. [163] demonstrated a 4 x 4 MIMO VLC system using OTS electronic circuit components at a link distance of 2 m achieving a data rate of 50 Mbps (12.5 Mbps per channel). Compared to other non-MIMO VLC implementations [164, 24] the data rate is less, however 175 mW of optical power emission resulted in increased illumination levels. In [163] an OOK modulation scheme is experimented, which limits the achievable data rate. A Gbps MIMO demonstrator in [79] uses OTS LEDs to realise a 4 x 9 MIMO system, however a commercial AWG along with a bias-T is used to generate the modulated signal to

drive the LEDs, which makes the driver side electronics size unrealistic for portable and power conservative applications. The UP-VLC demonstrator built and characterised in this work addresses some of the key issues seen in other VLC implementations such as miniaturisation of circuit components and high power efficiency.

5.3.1 Specification

Parameters		Values	
		Ganging	MIMO
Data rate (Gpbs)		>1	>1
Link Length (m)		>1	>1
Number of parallel channel		1	4
µLEDs	Array size	6×6	6×6
	Wavelength (nm)	450	450
	Diameter (µm)	24	39
	Transmitted optical power (mW)	2	3
	Bandwidth (MHz)	175	125
	Pitch size (mm)	0.3	1.5
Transmitter optics	Divergence angle (full)	10°	7.5°
Receiver Optics	FOV (full angle)	10°	5°
	Gain (maximum)	296	1182
Photodetector (APD)	Array size	5×5	5×5
	Width (µm)	200	200
	Pitch length (µm)	240	240
	Responsivity @ 450 nm (A/W)	2.41	2.41
	Bandwidth (MHz)	175	>125

Figure 5.1: UP-VLC demonstrator specifications [35]

A demonstrator was specified, designed and built as part of the UP-VLC project to showcase the technological advancements needed to realise a data dense VLC system leveraging expertise in various related domains including CMOS electronics, μLED fabrication and communication algorithms and modulation schemes [35]. The demonstrator system consists of a transmitter subsystem and receiver subsystem. The transmitter and receiver, kept 1 m apart, realises a multi-channel VLC system capable of achieving 1 Gbps. Experiments were carried out in various combinations of driver chip configurations (SISO and MIMO) and μLEDs to find out the most suitable setup to achieve the target data rate and link distance. A PC is used to process the data before transmission and after reception. Block level representation of the system is shown in figure 5.2. Details of the transmitter and receiver subsection are given below.

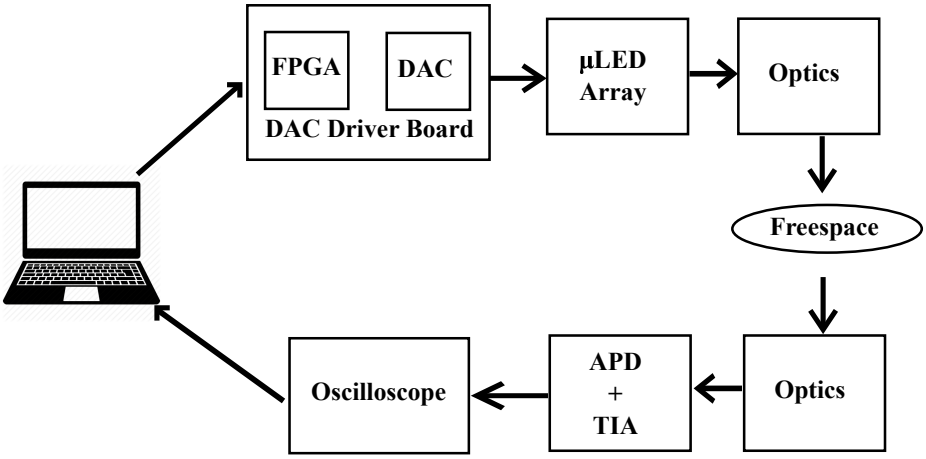


Figure 5.2: Block diagram of UP-VLC demonstrator

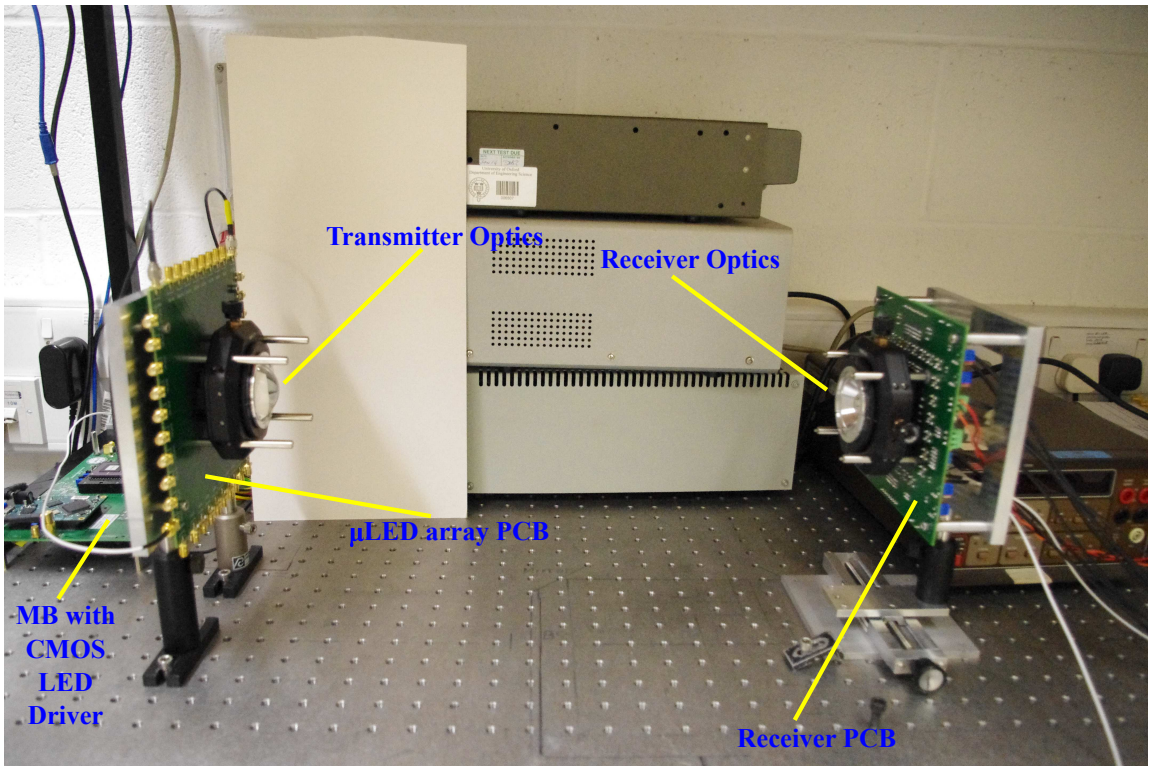


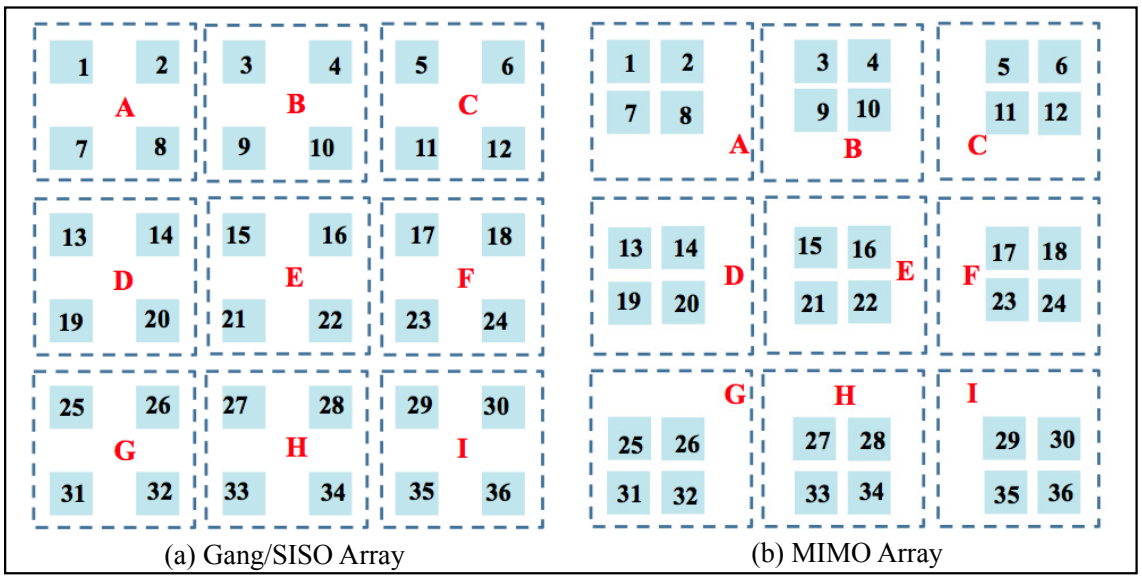
Figure 5.3: UP-VLC demonstrator system

The CMOS APD receiver chip housing different CMOS APDs and associated circuitry has a bandwidth of approximately 100 MHz [36, 35]. A commercial DSO (Tektronix MSO7104B) with a maximum sampling rate of 4 GS/s was used to sample the data from the APD receiver chip. Before performing VLC data transmission, component level characterisation is performed and details of these results are presented in the following sections.

5.3.2 UP-VLC demonstrator: Transmitter

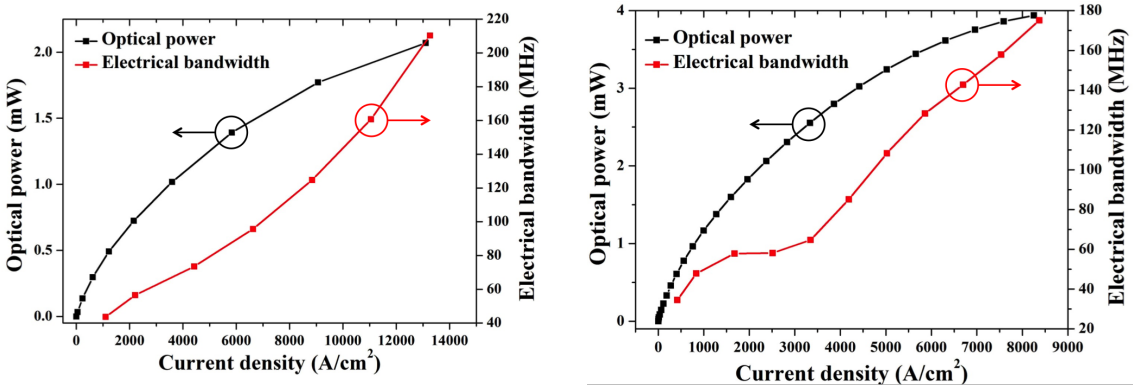
The transmitter consists of the electronic components (Opal Kelly (OK) and Mother board (MB) PCB along with the CMOS LED driver chip) which are described in section 4.3, the μLED array subsystem (μLED array and its PCB), transmitter optics and a mounting mechanism for the μLED and optics. The CMOS LED driver is designed to operate up to 500 MS/s which translates to a usable bandwidth of 250 MHz. The OK board FPGA limits the rate of the sampling clock to 375 MHz which means the maximum sampling rate per channel in MIMO mode operation will be limited to $375/4 = 93.75MHz$ when using all the four channels and $375/2 = 187.5MHz$ when using just two channels. See section 3.4 for more details about the design and configuration of the driver chip. The specified data rate is achieved by setting the sampling rate to the maximum (375 MHz) and using two driver chips to with each chip configured to use two out of the four channels available. This means the maximum per channel data rate could be 375 Mbps while using 4=PAM and 1.5 Gbps aggregate (4 channels). The modular approach in the bench design makes this possible, since multiple MBs can be used in the system to increase the number of available channels. Synchronisation of the data paths of both driver chips and MBs are essential in this configuration to prevent timing errors in the receiver side. One MB should act as the master board in this system capable of generating a synchronisation clock for the slave MB. Section 4.3.1 discuss the details of the clock output and input ports available on MB. These ports can be used to send out a synchronisation clock from the master MB to the slave MB. The 100 MHz clock from the oscillator on board the master MB is used to generate a 10MHz synchronisation clock. The synchronisation clock is used to generate the sampling clock for the driver chip in the FPGA and also fed through to the clock output LVDS interface which in turn is wired through an SMA connector to the slave MB. Slave MB receives this clock through the clock input SMA connector wired to the LVDS receiver in the FPGA and generates the required sampling clock for the driver chip.

5.3.2.1 μLEDs Arrays



(a) Gang/SISO Array (b) MIMO Array

Figure 5.4: SISO and MIMO μLED arrays

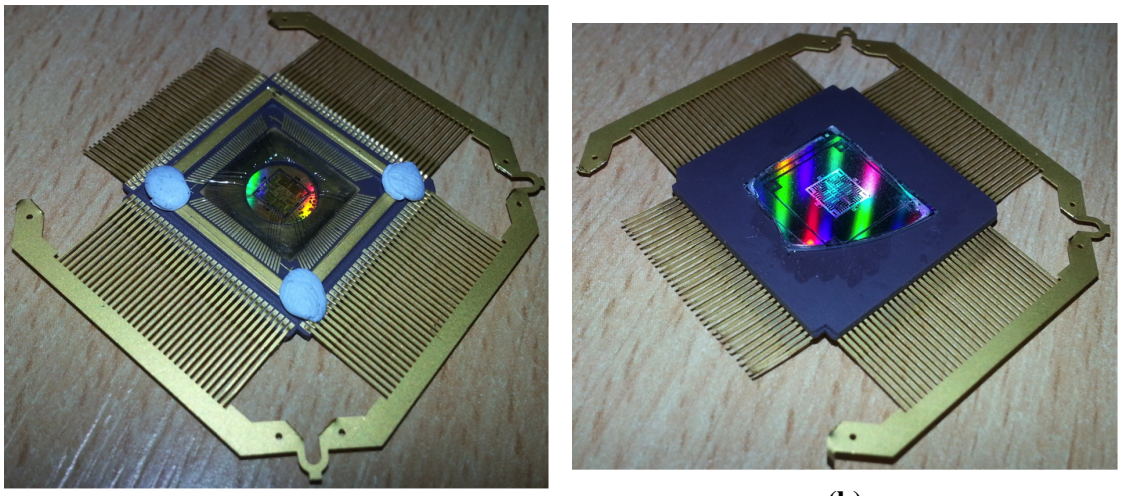


(a) SISO pixel **(b)** MIMO pixel

Figure 5.5: Power-Bandwidth-Current density relation in μLED pixels.

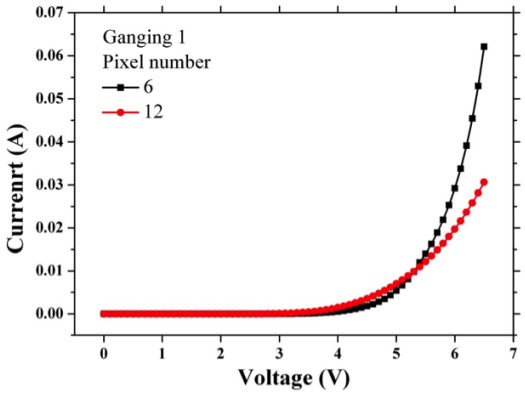
As seen from Figure 5.5, the μLEDs active area has to be reduced to increase the modulation bandwidth which results in reduced optical output power. However the UP-VLC demonstrator aims for Gbps data transmission at a distance of 1 m, where both output power and bandwidth are critical. Output power can be increased by using more than one μLED, without compromising the bandwidth [35]. A square array having 36 μLEDs is fabricated by the University of Strathclyde based on the specifications shown in Figure 5.1. For the SISO array, simulations predict that the optical power required is at least $2mV$, which can be achieved from a μLED of $24\mu m$ diameter. μLED pixels are arranged as shown in Figure 5.4 (a) with a pixel pitch of $300\mu m$. To achieve $3mV$ optical power for the MIMO operation, the μLED pixel size has to be increased to $39\mu m$. To reduce

cross talk between optical channels for the MIMO scheme, imaging optics at the receiver are used. In addition, the pitch of the receiver elements and transmitter elements (μLED pixels) should match. Thus, as shown in Figure 5.4 (b), μLED pixels in the array are grouped into sub-units of 2 x 2 elements. This scheme also offers the possibility of running the system in a hybrid mode, where each sub-unit could act as one single μLED and the whole array as a 3 x 3 μLED array. Both SISO and MIMO arrays were constructed in InGaN/GaN wafers grown on c-plane (0001) sapphire substrate resulting in an emission wavelength of 450*nm* (Blue) with 20*nm* full width at half maximum (FWHM). μLEDs arrays are fabricated with individual access to the cathodes of each pixel. Connections are through Ti/Au metal contacts to the NMOS based CMOS LED driver. The anodes of the all the pixels in the array are shorted together and accessible allowing connection to a supply voltage through a Pd layer. Fabricated arrays are bonded on to the rear side of a 132-pin ceramic package as shown in Figure 5.6. Heat sinks are glued to the package to improve I-V and I-L performance and ageing characteristics.

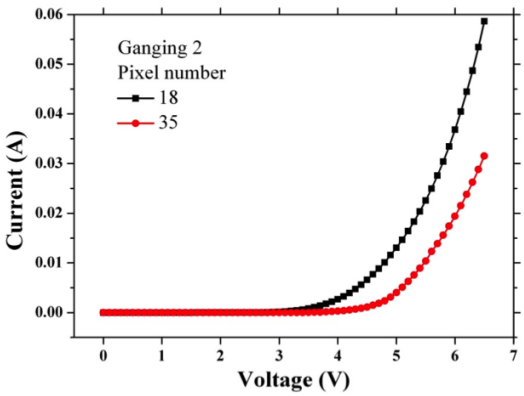


(a) **(b)**

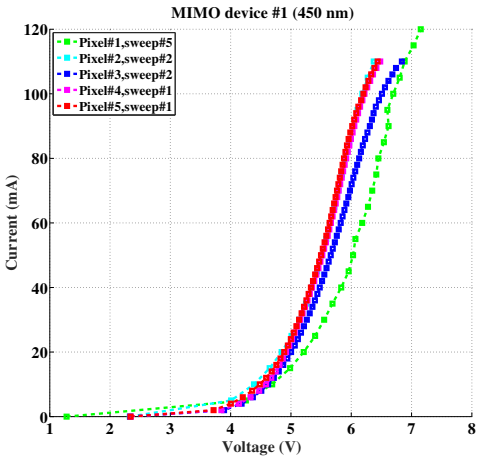
Figure 5.6: Top and Bottom view of packaging for SISO array



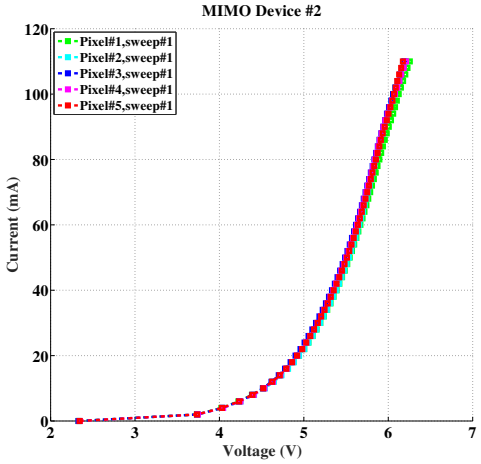
(a) SISO array 1



(b) SISO array 2



(c) MIMO array 1



(d) MIMO array 2

Figure 5.7: Measure I-V characteristics of two SISO and MIMO arrays

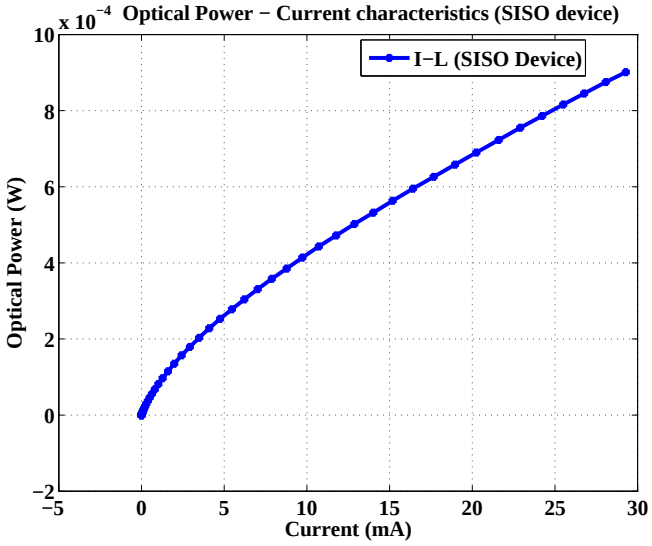
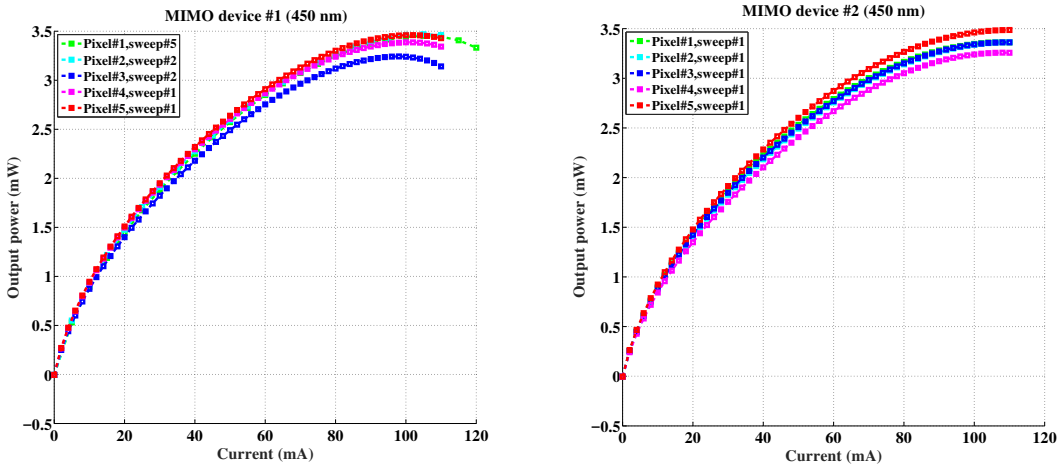


Figure 5.8: Measured I-L characteristics of SISO array pixels



(a) MIMO array 1 **(b)** MIMO array 2

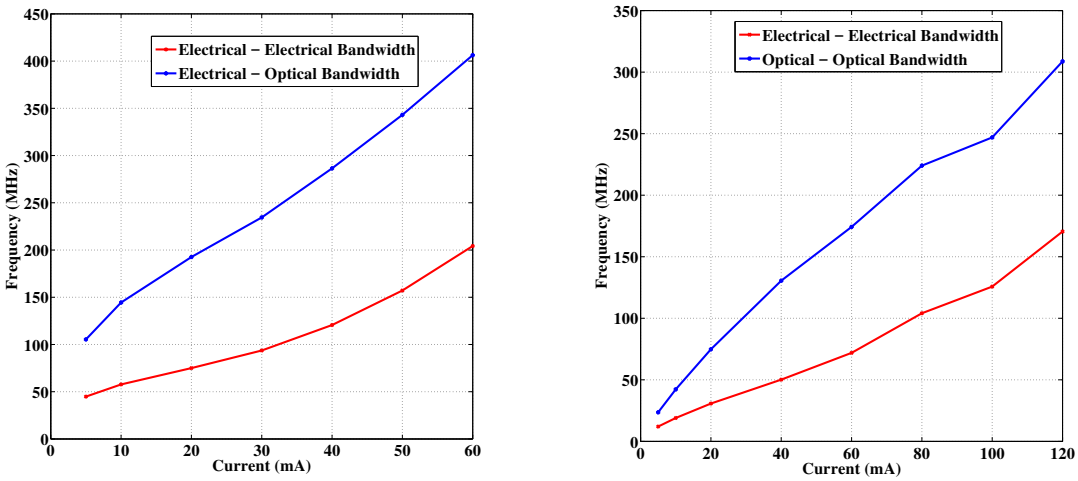
Figure 5.9: Measure I-L characteristics of two MIMO arrays

5.3.2.1.1 μLED characteristics Before demonstrator experiments, μLED arrays are characterised to ascertain characteristics such as voltage - current, current - optical power and modulation bandwidth. The voltage-Current and Current - Light output power characteristics of few pixels from two variants each of SISO and MIMO array are shown in Figure 5.7, 5.8 and 5.9 respectively. The turn ON voltage for all the pixels used in the arrays is approximately 3.5V, which is proportional to the band gap energy [97] of GaN/InGaN type semiconductor used in the P-N junction. Compared to the I-V characteristic of the OTS LED shown in Figure 3.1, where the parasitic series resistance can be estimated to be approximately 0.8Ω (a voltage swing of 0.2V results in a current variation of 225 mA) both SISO and MIMO arrays have considerable parasitic series resistance which affects their performance. For the SISO arrays, the series resistance is approximately 40Ω and 42Ω for variant 1 and 2 and for MIMO arrays it is approximately 16Ω and 10Ω (estimated from the I-V curves). Higher series resistance requires an increased supply voltage across the μLED and thereby increased power consumption compared to an OTS LED. Even though the pixels have the same dimensions and are fabricated in a single GaN die, the characteristics do not match well within different pixels in both the MIMO and SISO arrays (both I-V and I-L). Individual metal tracks connecting the μLEDs to the bond pad and the bonding contact resistance are not uniform, this mismatch in resistance also adds up to the difference in characteristics observed between different pixels in the same array. Table 5.1 lists the individual metal track resistance from different pixels from cathode of the μLED to the cathode bonding site in the array. Track resistance optimisation is limited due to the spacing requirements that needs to be satisfied for the μLED arrays. Mismatch in I-V characteristic can be nullified by providing adequate supply voltage and configuring the current DACs to sink equal current through all the μLEDs. The output power requirements for the demonstrator in both SISO and MIMO schemes were listed

SISO Array		MIMO Array	
Pixel	Resistance (Ω)	Pixel	Resistance (Ω)
1	0.84	1	1.21
2	0.91	2	1.22
3	0.8	3	0.82
7	0.82	7	1.2
8	1.82	8	1.34
9	1.83	9	0.95
13	0.63	13	0.74
14	1.5	14	0.88
15	1.74	15	1.29

Table 5.1: Cathode track resistance variation in μLED arrays

in Figure 5.1. For the MIMO array, the required specification of 3 mW optical power per pixel can be achieved at a bias current of approximately 70 mA for both variants. The optical output characteristics of both the arrays have non-linear characteristics which could affect modulation schemes such as OFDM [66]. Non-linearity effects can be mitigated by liming the signal swing across the DC bias point by adding appropriate DC offset and adjusting the bias current through each DAC. Mismatch in the I-L characteristic will affect the performance of the system since the individual channels will generate different light output levels for same input current which in turn results in a reduced SNR performance for those channels with poor characteristics and thereby a reduced modulation order. This can be mitigated either by adjusting the DAC input code for each pixel or by adjusting the bias current for each DAC.



(a) SISO pixel

(b) MIMO pixel

Figure 5.10: Electrical-Optical-Electrical bandwidth of a SISO nd MIMO pixel

Small signal bandwidth characterisation on pixels from the SISO and MIMO arrays are performed and results from a pixel is shown in Figure 5.10. Both electrical to optical and electrical to electrical bandwidths (the square-law detection by the PD) at various bias currents indicates that for high speed operation, a higher bias current is required. It can be seen that as the bias current increases, the bandwidth also increases, which translates to a proportional relation between current density and bandwidth [76]. The SISO pixel bandwidth requirement of 175 MHz and the MIMO pixel bandwidth requirement of 125 MHz based on specifications in Figure 5.1 is possible with the fabricated arrays at a bias current of 55 mA and 100 mA respectively.

5.3.3 UP-VLC demonstrator: Receiver

The receiver used in the UP-VLC demonstrator consists of the custom built CMOS APD array with embedded TIAs and an associated PCB providing power, bias settings, control signals and an output interface to the CMOS APD array. The CMOS APD array was designed and fabricated as part of the UP-VLC project in 0.18μm fabrication process from AMS (see section 3.3.1).

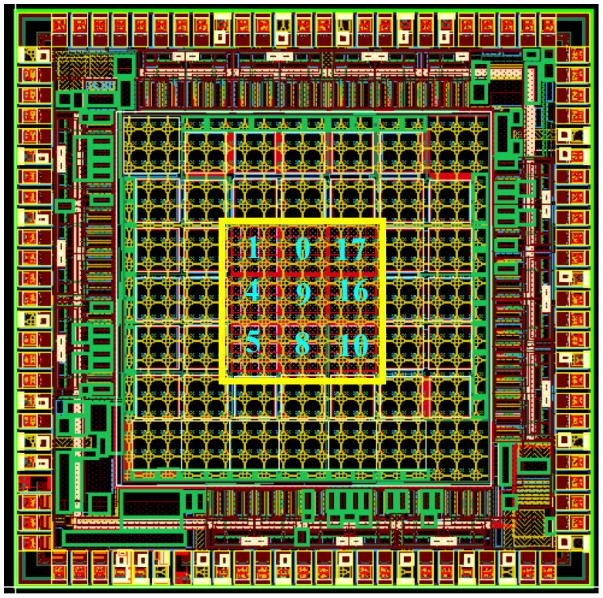


Figure 5.11: Layout of CMOS APD chip

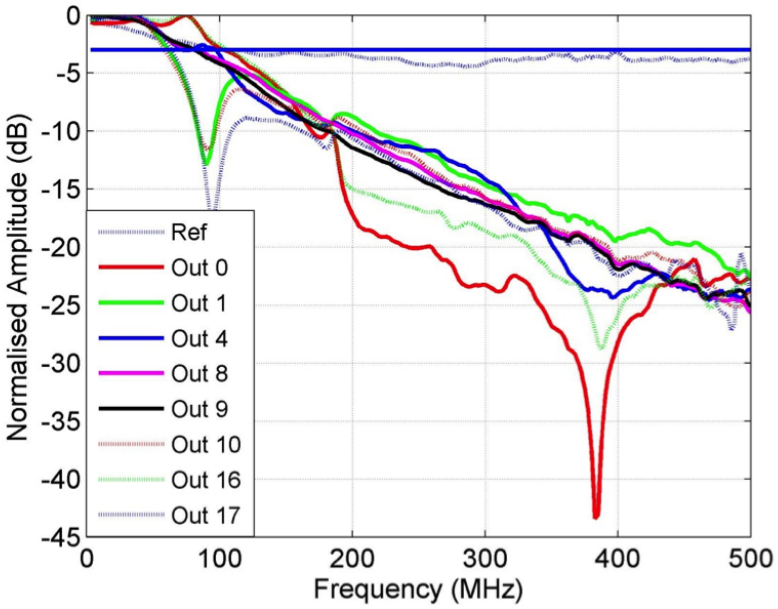


Figure 5.12: Frequency response of 3 x 3 sub array

The APD array consists of 49 APDs arranged in an array of 7 x 7, where the central 3 x 3 sub array (Figure 5.11) consists of APDs designated for the UP-VLC demonstrator, whereas rest of the APDs are test structures. Each APD in the central array has an area of $200 \times 200 \mu m^2$ and a responsivity of 2.61 A/W when reverse biased at 12.75 V (at 450 nm)[35, 34]. The APD chip has integrated TIAs for each detector and the output of the TIA is accessible outside for further processing. Due to the low noise performance, a shunt feedback topology is selected for the TIA since noise performance of the receiver is critical [35]. The frequency response of all the detector elements in the 3 x 3 sub-array is measured by the University of Oxford and shown in Figure 5.12. Bandwidth of the measuring equipment used for this experiment was 300 MHz. We can see that the losses at 300 MHz is approximately -25 dB, and measurement points beyond 300 MHz are ignored since they are not reliable. The bandwidth of the detector array varies from 60 MHz to 100 MHz for different detector elements. Even though the detector elements have same physical structure, the electrical connectivity from the detector to the corresponding TIA and then to the output pads is not well matched considering the parasitic RC components, which results in the difference in measured bandwidth across the array. The CMOS APD array is housed in the custom built PCB. The associated receiver optics are placed in front of the receiver chip to focus transmitted light into the detector array. The output from the APD array is sampled using a DSO and transferred to a PC for further processing.

5.3.4 UP-VLC demonstrator: Characterisation results

5.3.4.1 Tonal quality

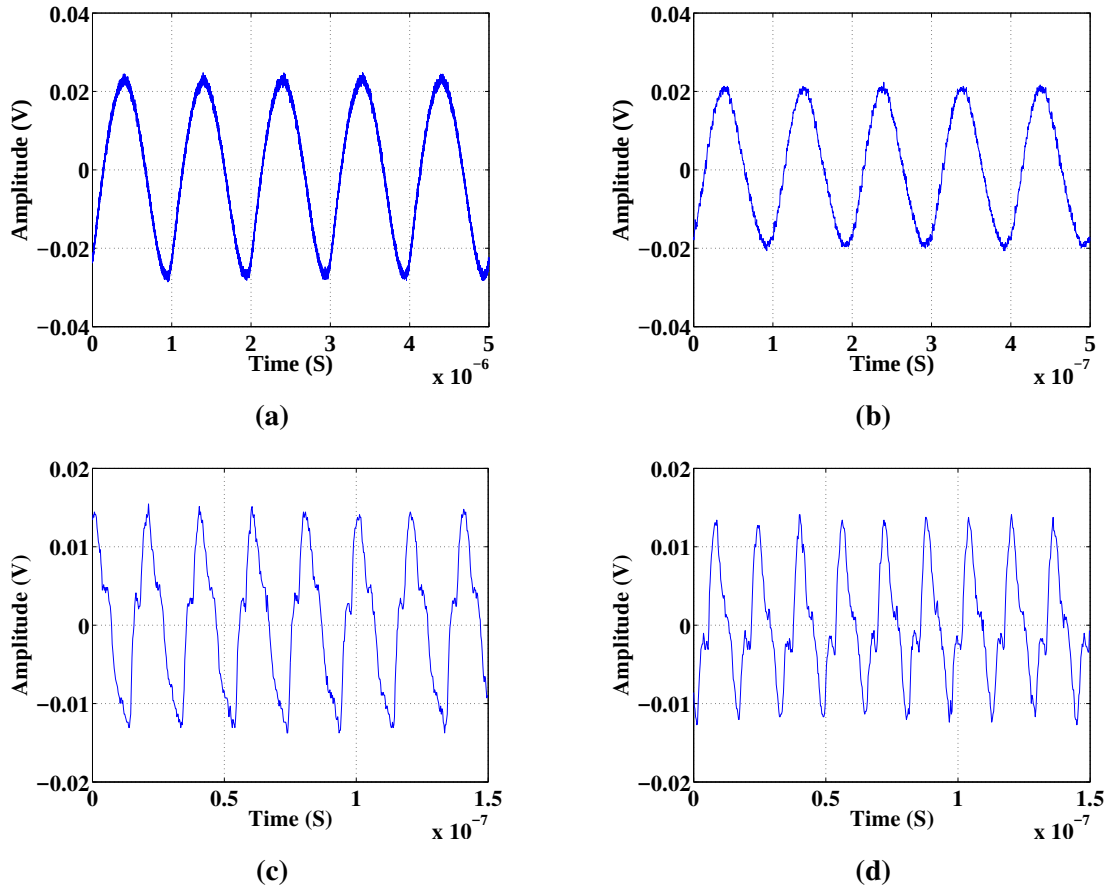


Figure 5.13: Sinusoid outputs (a)1 MHz (b)10 MHz (c)50 MHz (d)62.5 MHz

Different sinusoidal inputs frequencies fed into the DAC at a sampling rate of 250 MHz are plotted in Figure 5.13. As the input frequency increases the quality of the reconstructed signal degrades due to factors such as the limited number of samples per cycle, μLED and receiver bandwidths and channel characteristics.

5.3.4.2 System frequency response

The frequency response of the UP-VLC demonstrator system is measured, which is an indicator to the maximum data loading capacity of the system. Since the system includes various components, such as the driver circuit, μLEDs, transmit and receive optics, transmission channel and receiver circuitry, any of the components could be a bottleneck and thereby affect the performance of the system. Figure 5.10 is the bare die bandwidth measured from the μLED arrays, however these measurements are performed in the small signal domain, where a very small voltage swing is introduced across the μLED (0.2 V or

less) which results in a small variation in the optical power generated by the μLED element. Even though the small signal bandwidth is an indicator of the system performance, it does not indicate the actual transmission capability of the UP-VLC system, since the small signal swing is not enough to generate sufficient optical power variations detectable at the required link distance of 1 m. Therefore a larger current swing and thereby wider variation in generated optical power is required. The large signal frequency response of the μLEDs will not be same as the small signal one due to factors such as the asymmetric rise/fall times of the μLEDs [97]. This affects the frequency response of the system. Figure 5.14 is the frequency response from a single channel in the DAC at different bias and offset configurations. The measured frequency response indicates that the highest operating bandwidth of the system is achieved at a bias setting of 13 (average DC current of 48 mA through the μLED) and DC offset configuration of 2 (16 mA offset current). As the bias current is reduced, the bandwidth drops (current density in the μLED reduces and also received optical power reduces), increasing the bias setting beyond 13 will reduce the dynamic range of the system due to optical power saturation observed in the L-I characteristics (see Figure 5.9)

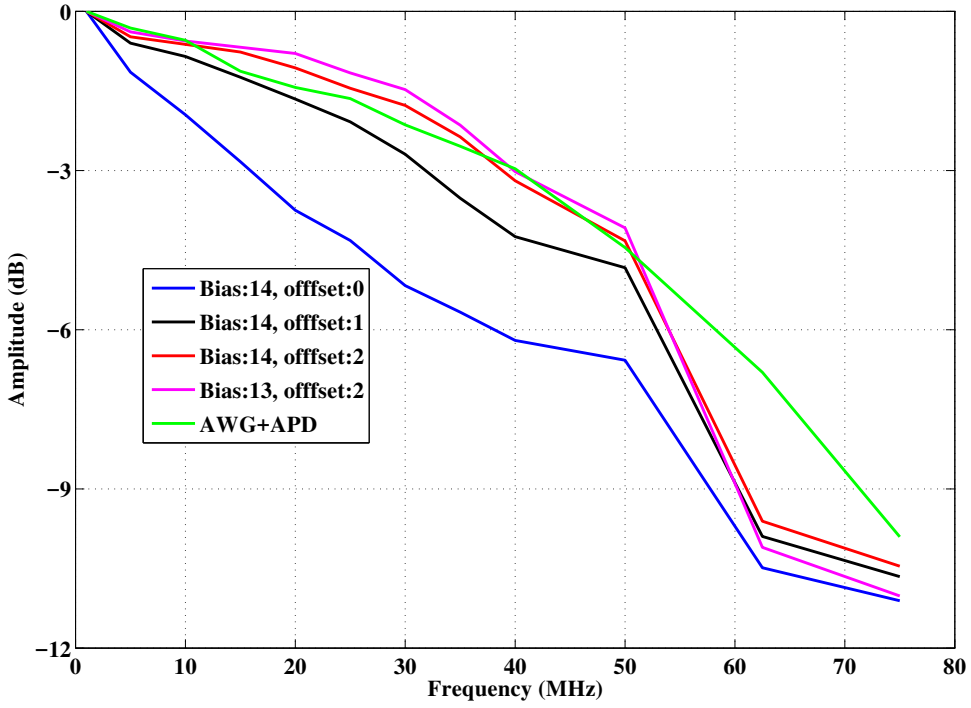


Figure 5.14: Frequency response of the system at different bias currents

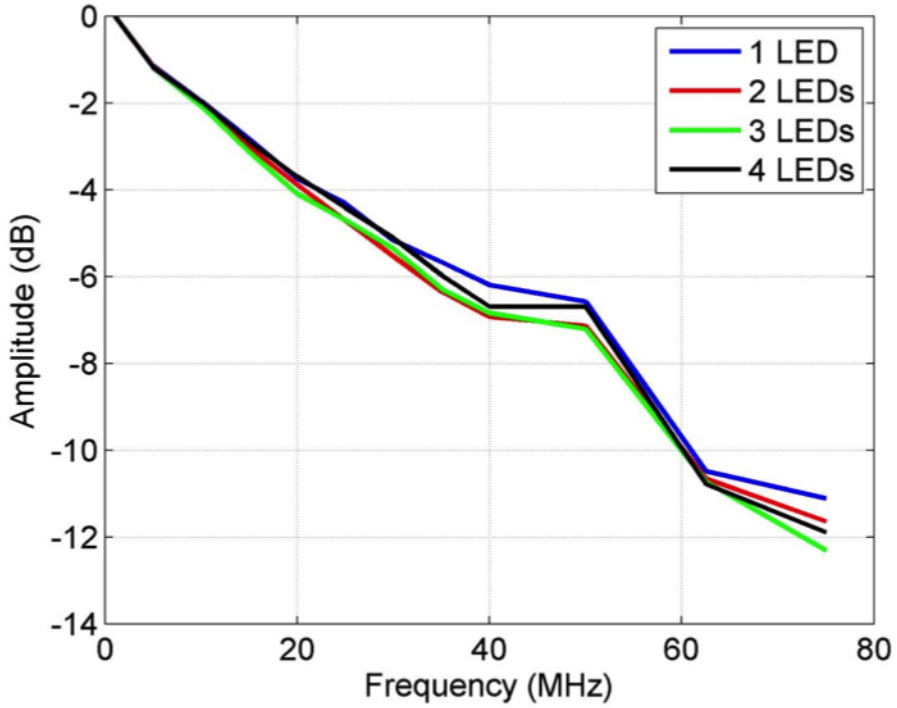
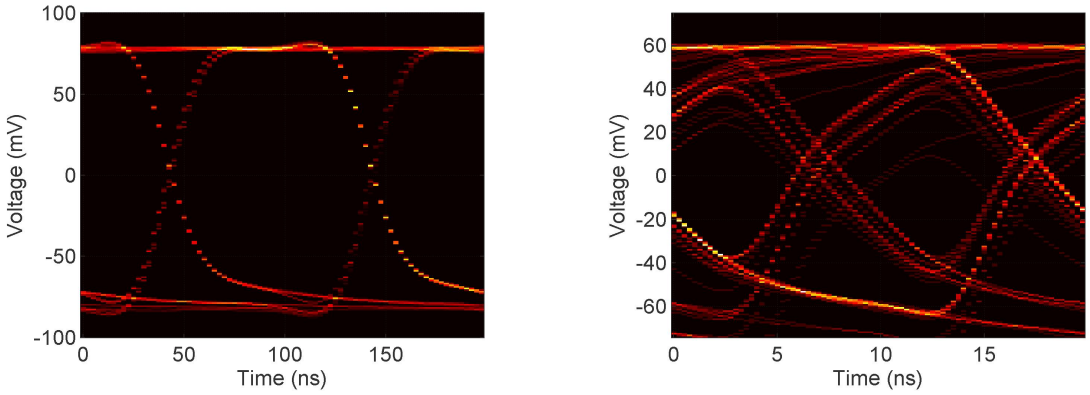


Figure 5.15: Frequency response of the system when all DACs enabled

In MIMO operation, multiple channels will be activated and transmitting different data streams thus bandwidth characterisation of the system was performed by turning on each channel and is shown in Figure 5.15. The same -3 dB bandwidth is measured when operating a single channel or all channels together. The frequency response plots (Figure 5.14 and 5.15) are plotted in linear frequency scale which resulted in an almost linear frequency vs. amplitude relation especially for second plot.

5.3.4.3 Data transmission: OOK

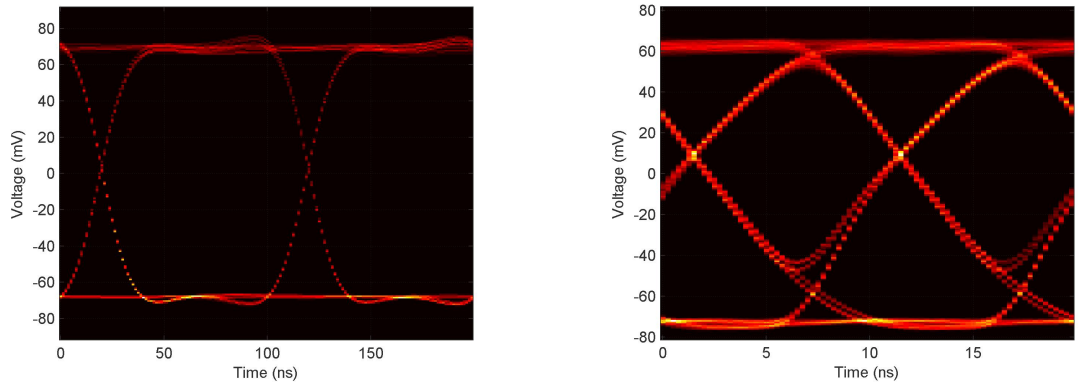
OOK is the simplest modulation scheme for IM/DD, where binary information is represented by two discrete optical intensity levels. Since the number of bits representing a symbol is 1 for OOK, the bit rate is same as symbol rate. Section 2.3.1.2 discussed the OOK scheme in more detail. OOK transmission is attempted using pixels in the MIMO array and within the UP-VLC demonstrator setup at different bias and offset settings.



(a) 10 Mbps **(b)** 100 Mbps

Figure 5.16: Eye diagrams of OOK transmission at bias setting 14 and no offset

A bias setting of 14 means a full scale current of 32 mA through the μLED. Eye diagrams at a sampling clock rate of 10 MHz and 100 MHz can be seen in Figures 5.16a and 5.16b respectively. A clear eye opening is visible at 10 MHz, whereas at 100 MHz, the vertical and horizontal opening windows are reduced, which means decision making at the receiver will be more difficult. It can also be seen that the jitter performance has worsened at the higher operating speed. The NMOS DAC based LED drive scheme implemented in this work turns the LED ON by sinking a current through the LED, whereas to turn it OFF, the current is re-routed to the dummy branch of the DAC. Parasitic capacitances (see Section 2.4.3.1) during the forward biased operation of the LEDs will be charged. To turn OFF the LED completely, these capacitances should be discharged. If no active turn OFF mechanism is provided, charge accumulated in the junction will leak slowly resulting in slower turn OFF characteristics. The effect of this passive turn OFF results in the eye opening being reduced.



(a) 10 Mbps **(b)** 100 Mbps

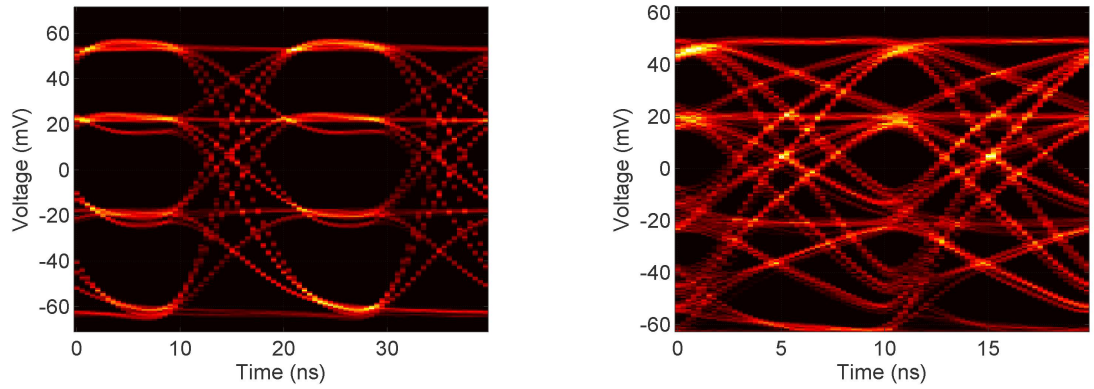
Figure 5.17: Eye diagrams of OOK transmission at bias setting 13 and no offset 2

Adding a DC offset of 16 mA (offset setting of 2) and increasing the full scale current

to 48 mA (bias setting of 13) results in better transmission characteristics for both 10 MHz and 100MHz sampling rates as seen in Figures 5.17a and 5.17b respectively. Increasing the bias setting to 13 results in increased transmit power and thereby increased received power and SNR, which is evident from the wider eye opening. Providing a DC offset results in the μLED pixel being turned ON even when there is no data transmission, thus the passive turn OFF issue is mitigated. However, additional power is consumed which reduces the power efficiency of the scheme. The power penalty due to the DC offset in this experiment can be quantified as follows. Assuming an equal distribution of zeroes and ones in the incoming digital bit stream, for the scheme with setting bias 14 and 0 DC offset (scheme 1),the average current through the μLED will be 16 mA. For a bias setting of 13 and a DC offset of 2 (scheme 2), assuming the same digital bit pattern, the total average current is the sum of the constant DC offset (16 mA) and the average of the dynamic current (24 mA) which is 40 mA. For the same supply voltage, an increase in current consumption by a factor of 2.5 ($40mA/16mA$) results in increased power consumption by the same factor.

5.3.4.4 Data transmission: 4-PAM

Higher data rates could be achieved by increasing the number of discrete PAM levels at the expense of higher SNR and thereby transmission power requirement. From the OOK experiments, the bias setting of 13 and DC offset setting of 2 gave better results, thus for the same configuration, 4-PAM data transmission is performed.



(a) 50 Msps **(b)** 100 Msps

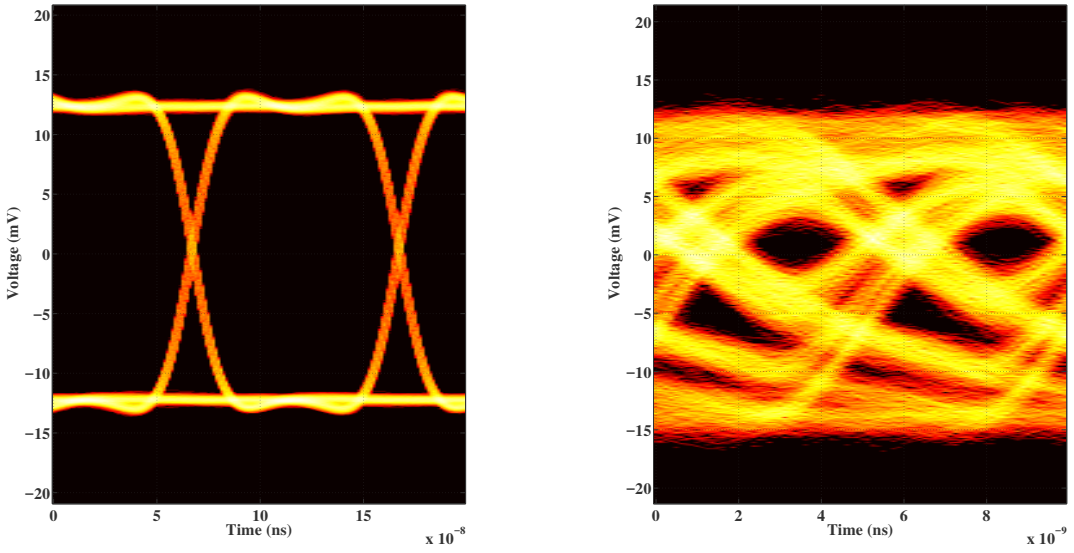
Figure 5.18: Eye diagrams of 4-PAM transmission at bias setting 13 and no offset 2

From the eye diagrams in Figure 5.18 it can be seen that for 4-PAM transmission eye opening at 100 MHz sampling clock, which translates to 200 Mbps has a reduced eye opening compared to 50 MHz (100 Mbps) transmission. The jitter performance of the DAC combined with DAC non-linearity and asymmetric rise/fall times resulted in worse eye openings at 100MHz. The carrier flush out mechanisms implemented in [98] could

be a solution to the problem of the passive turn OFF mechanism while driving LEDs. In this method, carriers are removed by an active drive scheme.

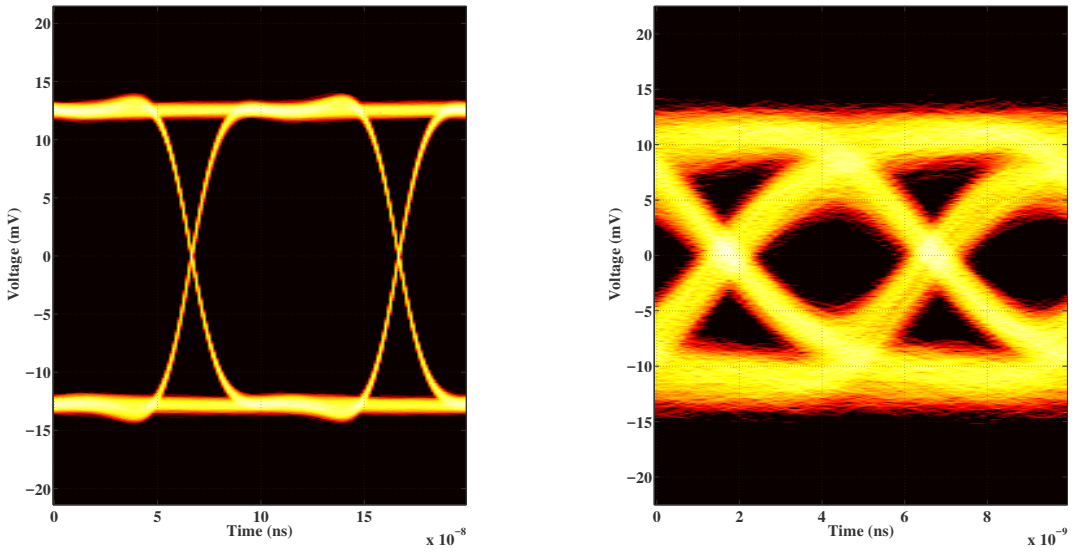
5.3.4.5 Comparison: CMOS DAC and AWG

Performance of the CMOS DAC is compared with that of a commercial AWG (Agilent 81150A) in the UP-VLC demonstrator. The AWG is a voltage mode driver with output resolution of 14 bits and a sample rate of 2 GS/s [165] compared to the current mode CMOS DAC driver with 8 bits output resolution and a sample rate of 500 MS/s (in the demonstrator, the sample rate of the DAC was limited by the FPGA used). The output settings of both the DAC and AWG are adjusted so that the received optical intensity is equal at the APD for a fair comparison. For the DAC based drive scheme, the supply voltage is set to 7.5V across the stack of μLED and DAC with a bias setting of 12 and offset setting of 1, resulting in an average current of 46 mA and the received signal having a peak-peak amplitude of approximately 33 mV at 10 MHz OOK. When using the AWG, a similar signal is received at the APD when the AWG is configured for a DC voltage of 3.85V and a peak-peak pulsing voltage of 3.3V.



(a) 10 Mbps **(b)** 200 Mbps

Figure 5.19: Eye diagrams of 2-PAM transmission from DAC



(a) 10 Mbps **(b)** 200 Mbps

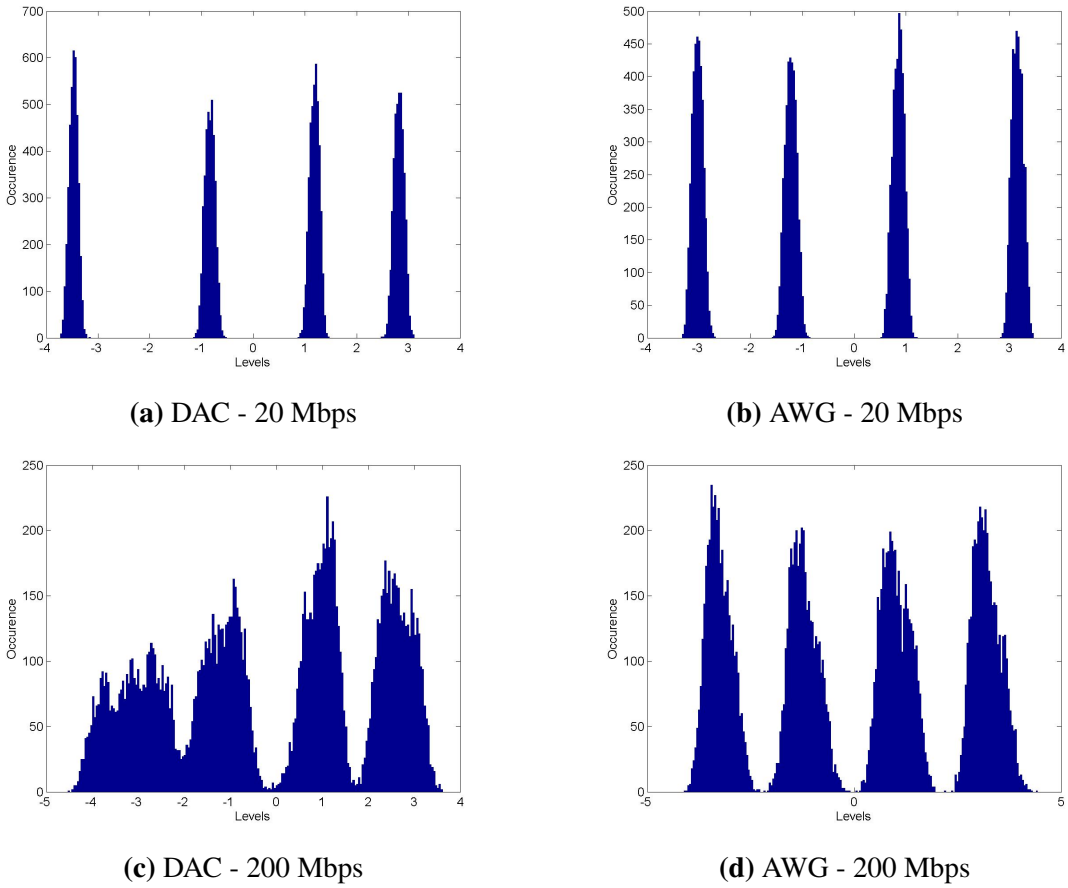
Figure 5.20: Eye diagrams of 2-PAM transmission from AWG

Limited bandwidth, absence of an active turn OFF mechanism discussed in section 5.3.4.3 and the limited sampling rate in the DAC driver results in the performance degradation while transmitting PAM signals at higher clock rates compared to an AWG based drive scheme. Figure 5.19 and 5.20 shows the eye diagrams from 2-PAM or OOK transmission using the DAC and AWG respectively. At 10 Mbps the performance is comparable, with the same rise/fall times, equal vertical and horizontal eye openings and jitter performance (Figures 5.19a and 5.20a). As the sampling rate increases, the DAC based drive scheme falls short in the performance metrics listed above which is evident from the 200 Mbps eye diagrams plotted above. Beyond 200 Mbps, the eyes were completely closed for the DAC drive scheme and thus not usable in realising a reliable communication link. The superior performance from the AWG based scheme can be attributed to the higher sampling rate and an increased resolution for the reproduction of the analogue output. Table 5.2 compares the various eye diagram metrics of 2-PAM transmission at

Parameter	DAC	AWG	DAC	AWG
	10 Mbps		200 Mbps	
Rms Jitter (ps)	1490	505	818	331
Rise Time (ns)	23.6	24.8	2.87	3.39
Fall Time (ns)	23.9	26.1	3.53	3.59
Eye SNR	53	37.5	2.24	4.01

Table 5.2: Eye diagram metrics: DAC and AWG

different sample rates.



(a) DAC - 20 Mbps

(b) AWG - 20 Mbps

(c) DAC - 200 Mbps

(d) AWG - 200 Mbps

Figure 5.21: 4-PAM histogram comparison at different data rates (DAC and AWG)

Figure 5.21 shows the histogram of received samples at different clock rates while transmitting 4-PAM. Four distinct levels can be easily recovered in the case of 10 MHz operation for both DAC (Figure 5.21a) and AWG (Figure **??**). At a 100 MHz sample rate, the lower levels of the DAC merge, making it difficult for the receiver to distinguish discrete levels and thereby causing an increased error rate.

5.3.5 Gbps MIMO VLC link

A MIMO Gbps 1 m VLC link is realised using multiple CMOS LED driver chips, the MIMO μLED array and the CMOS APD receiver chip with suitable optics at the transmitter and receiver. As mentioned in Section 5.3.2, two MBs are used in master-slave configuration, where the master board provides the system clock for the slave board. The DACs in both the master and slave boards are configured to be in 2 channel MIMO mode where channel 1 and channel 2 in each DAC will be transmitting a demultiplexed incoming bit stream at a sample rate of half the input clock to the chip. A single PC will provide data and control signals for both the MBs. Both the outputs from each DAC are connected to 4 μLEDs in the MIMO μLED array board. The dummy branches were not connected

to a load, and this did not deteriorate the performance of the link. From the 6 x 6 μLED array four pixels for transmission are chosen in such a way that the beam pattern at the receiver is a close match to the simulated beam pattern [35]. The transmitter-receiver alignment is optimised to receive the highest peak-peak signal in all the four channels thereby highest SNR. The output from selected four channels of the CMOS APD receiver are sampled by a DSO (Agilent MSO7104B) and transferred to the computer for processing. A 4-PAM modulation scheme with decision feedback equaliser (DFE) is used, which resulted in achieving approximately 330 Mbps per channel and an aggregate data rate of 1.3 Gbps as seen in 5.22.

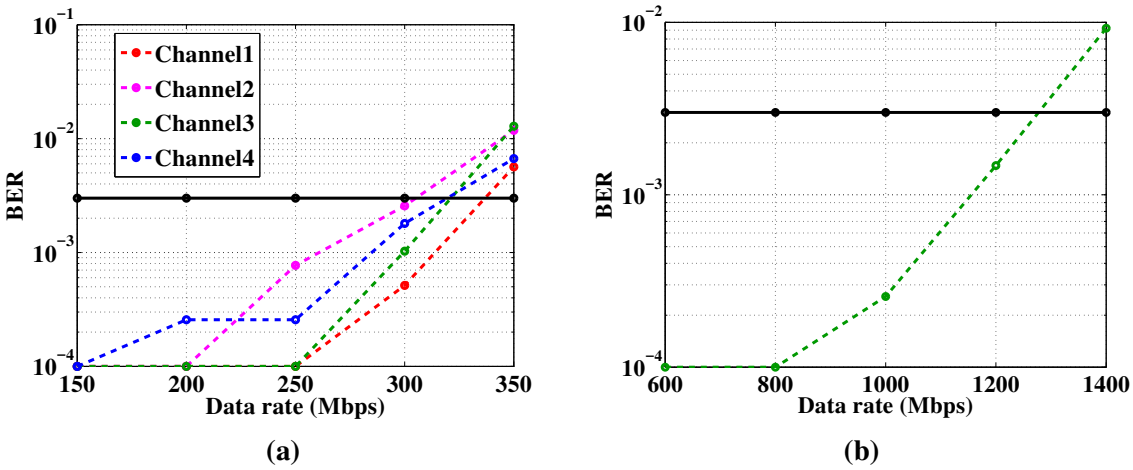


Figure 5.22: BER performance of UP-VLC demonstrator (a)Channels (b) Aggregate

5.3.6 Power efficiency of CMOS LED driver in UP-VLC system

For the UP-VLC demonstrator, the total supply voltage used for the experiments is 8 V, out of which 1.2 V is meant to keep the DAC in saturation. The average current through the μLED is 46 mA. This means the total power consumed by the system is 0.38 W, out of which the μLED consumed 0.31 W, which translates to an average power efficiency of the drive stage to be 85%. This power efficiency figure does not include power consumed by the rest of the circuit including digital logic. Therefore a de-rating factor of 0.85 is applied to incorporate aforementioned losses and make the power efficiency figure more realistic. Power efficiency of the driver after de-rating is 72%.

5.4 Integrated Digital to Light Converter

The concept of DLC was discussed in Section 2.5.11 and the design of an integrated DLC transmitter was presented in Section 3.4.3. In this section, results from the characterisation of the DLC system is presented. Since the DLC is a data converter which converts digital information to the optical domain, static and dynamic performance metrics used to

benchmark conventional data converters, such as DNL INL, SFDR, can be used for DLC as well.

5.4.1 μLED array variants

Three variants of DLC were built using the CMOS LED driver and three variants of the μLED array. Similarly to the μLED arrays fabricated for the UP-VLC demonstrator mentioned in Section 5.3.2.1, a common anode, individual cathode fabrication method is followed since the CMOS DLC circuit is based on NMOS transistors. The semiconductor material used for fabricating these devices is a commercial 450 nm InGaN/GaN wafer grown on a sapphire substrate with a surface orientation of c-plane (0001). Each array has 16 μLEDs of $24\mu m$ diameter arranged in a linear fashion with metal bonding sites for both individual n-contacts and shared p-contacts. Cathode metallisation is realised by sputtering Ti/Au (50/200 nm) and insulation/protection provided by a SiO_2 layer deposited by chemical vapour deposition (CVD). Three different metallisation schemes were experimented for anode metallisation by e-beam evaporation and thermal annealing which as mentioned below. For the device 1, also known as SEG1, 15/30 nm Nickel/Gold(Ni/Au) is used whereas for device 2, also known as (SEG2) 10/20 nm Nickel/Gold(Ni/Au) is used and annealed at 500 °C in air ambient and for device 3, also known as (SEG3), 20 nm Palladium(Pd) is used and annealing at 300 °C in Nitrogen ambient. Bare die V-I characteristics of each die are measured by probing the n and p contacts of each pixel separately using a programmable power supply (Yokogawa GS610), which can vary the current and measure the voltage across the pixel. At the same time a silicon power sensor (Thorlabs S120C) placed on the emitting side of the pixel measures the emitted optical power.

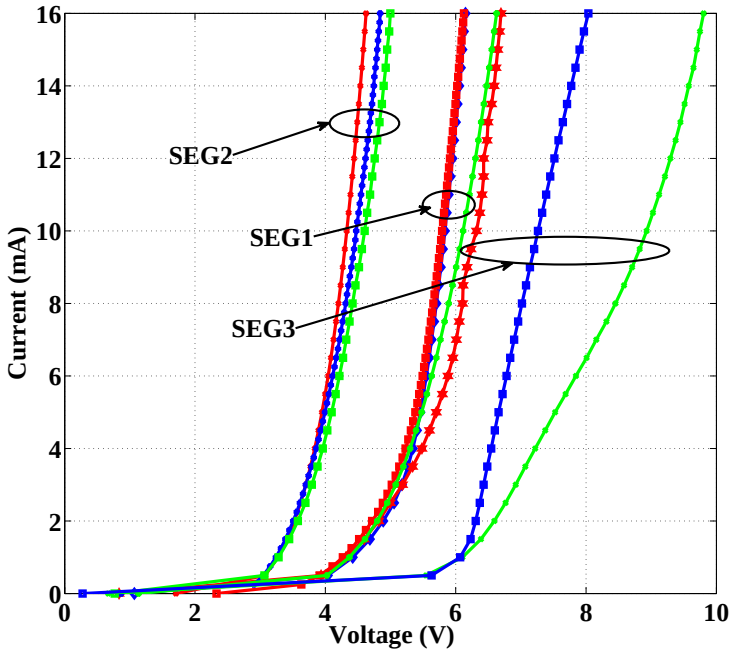


Figure 5.23: V-I characteristics of 3 μLED arrays

Figure 5.23 shows the voltage-current characteristics measured from the bare die of the three μLED arrays. SEG2 has a better voltage-current relation owing to good matching between the measured pixels compared to the other devices. SEG3 shows considerable pixel-pixel characteristic mismatch and high parasitic series resistances.

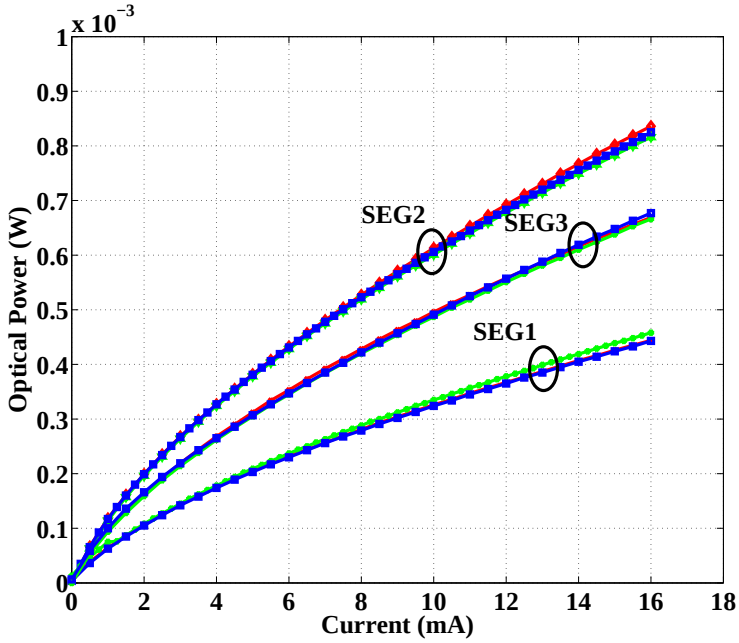


Figure 5.24: I-L characteristics of 3 μLED arrays

The SEG2 device has the best L-I characteristics out of the three variants which can be

seen in Figure 5.24. Unlike for the V-I characteristics, the pixel-pixel matching of optical power is better for each variant.

5.4.2 Experimental Setup

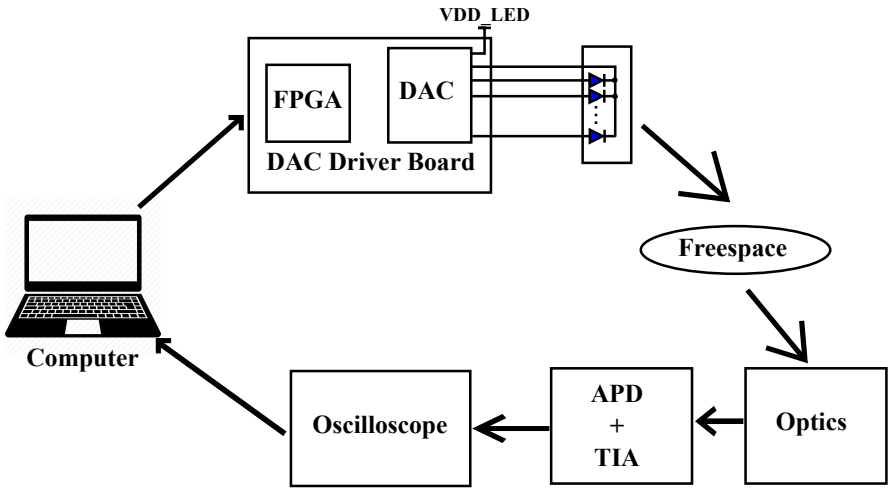


Figure 5.25: Block diagram of DLC experimental setup

Static optical power measurements to estimate DNL,INL, bias current vs optical power, dynamic measurements to estimate SFDR and data transmission measurements using different modulation schemes were performed using the DLC system. Data and control signals were generated off-line in a computer and transferred to the FPGA board and to the DLC circuit (see section 4.3). External power is provided for the hardware and μLED array using DC power supplies. An optical power meter (Thorlabs PM100USB) is used to measure the optical power. This device is controlled through the computer using a custom script written in the Python programming language, which sends digital codes to the DLC circuitry through the FPGA and at the same time reads the optical power from the power meter for processing. For dynamic characterisation and data transmission experiments, a custom built APD receiver is used which is described in Section 5.3.3. The differential voltage output from the APD receiver circuitry is sampled by a DSO (Agilent 7402D) and transferred to the computer for further processing. For the measurements using the power meter, the power meter is attached to the transparent lid of the DLC chip to collect maximum light, whereas for the dynamic measurements and VLC data transmission experiments, the receiver is kept 5 cm from the DLC chip. A block diagram of the experimental setup is shown in Figure 5.25.

5.4.2.1 Input/Output Characteristics

By fixing a supply voltage of 6.5V, the input code is swept over the full range (0 - 15) and the result is shown in Figure 5.26.

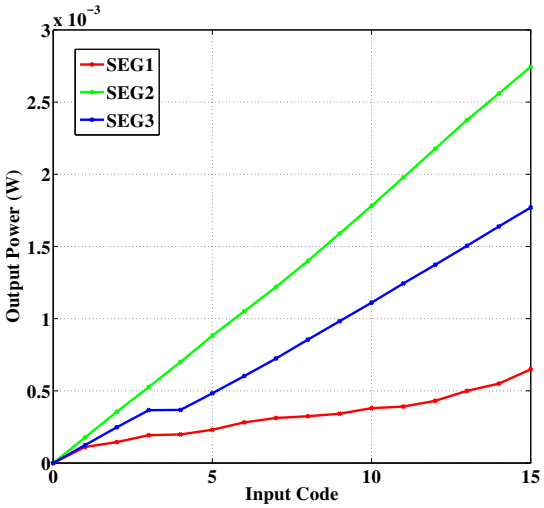
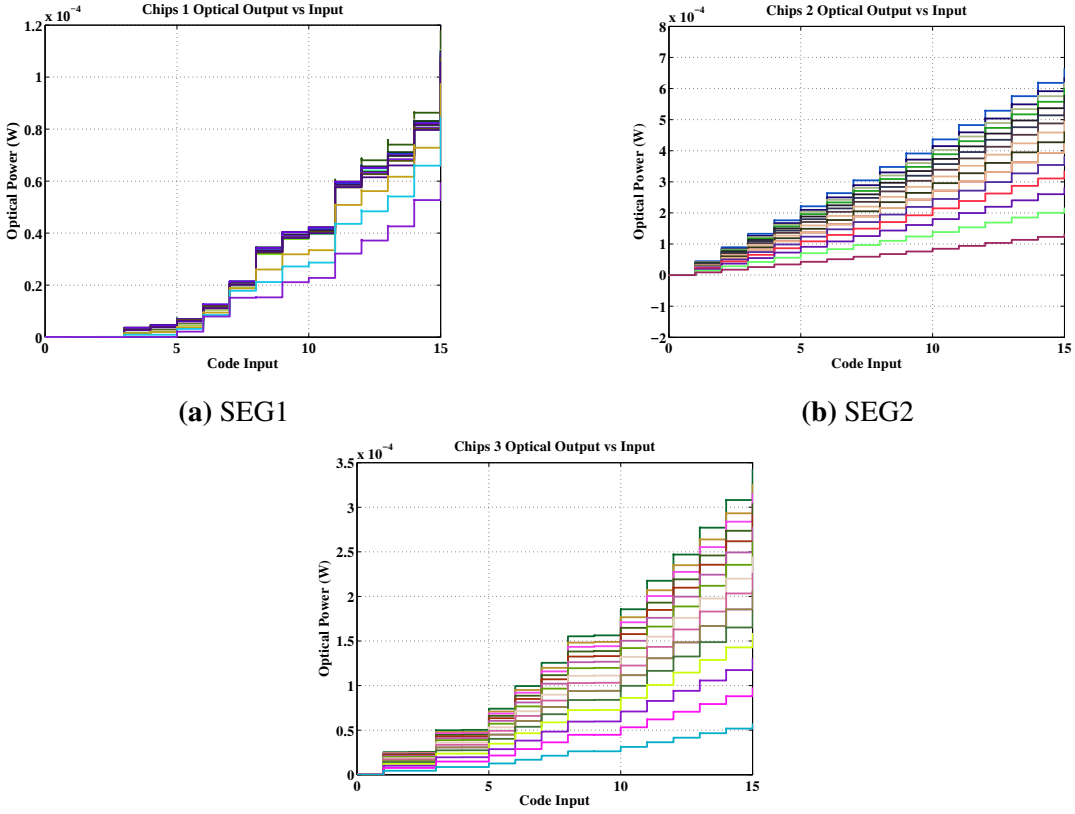


Figure 5.26: Input code - Output optical power of SEG1, SEG2 and SEG3 arrays



(a) SEG1

(b) SEG2

(c) SEG3

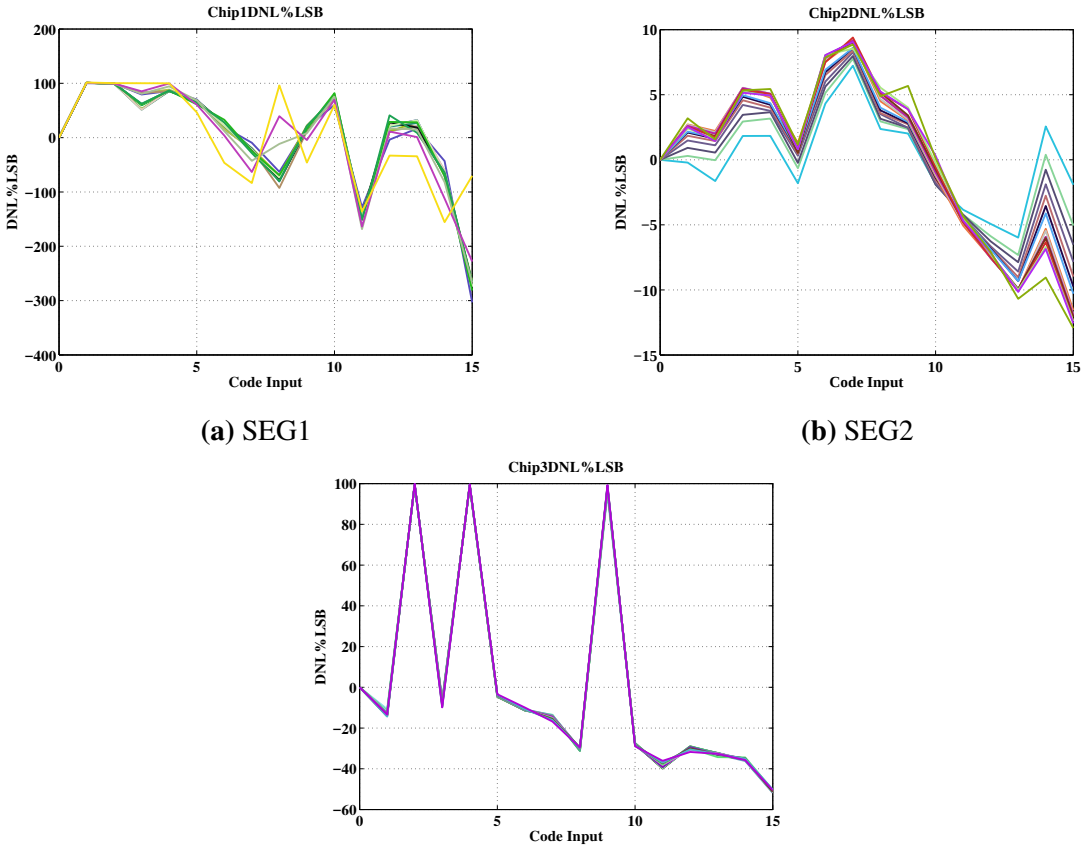
Figure 5.27: Input-Output at different bias settings for DLC variants

A linear optical power to input code characteristics can be observed for the SEG2 array, whereas for the SEG1 array, due to higher contact resistances, the optical power levels are lower than the SEG2 and SEG3 arrays. The SEG3 array generates a linear output characteristic for most of the pixels except one, which malfunctioned. Electrically all

pixels were tested in the bare die to see if they could emit light, which means pixel damage might have occurred either during the wire-bonding process or during initial power up. The SEG3 array is not used for dynamic and data transmission studies due to this dead pixel. The unary DAC used to drive the μLEDs in the array has adjustable biasing similar to the main DACs as discussed in Section 3.4.1.3. A higher bias current translates to a wider swing in the current to optical power output characteristics of the DLC. This also means a different linearity performance at different bias currents due to different full scale ranges in the I-L characteristics. The input code is swept from 0 to 15 at all bias configurations for all the three DLC variants and optical power from each measurement point is captured and plotted in Figure 5.27. The SEG2 device, owing to superior characteristics, has linear characteristics over the whole bias range as seen in Figure 5.27b, whereas the SEG1 device has poor pixel-pixel matching, which can be seen in Figure 5.27a. Both SEG1 and SEG2 devices are monotonic over the whole code range. The SEG3 device, except for the dead pixel, shows a linear performance over the bias range with peak optical power approximately half of that from SEG2 device. The output power observed in this experiment is less than the bare die optical power shown in Figure 5.24. This can be attributed to factors such as the reflectance and transmission efficiency of the transparent lid, responsivity of the optical sensors used in for both measurements and difference in experimental setups.

5.4.3 DNL/INL

INL/DNL are parameters indicating erroneous non-linearities in data converters. They are defined and discussed in Section 2.5.6.6. For the 4-bit DLC system fabricated and characterised in this work, to ensure the linearity within the accuracy of 4-bits, the INL should be within $\pm$ 0.5 LSB and the DNL should be within $\pm$ 1 LSB. The measured DNL at different bias currents for the three variants of DLC can be found in Figure 5.28, where the X-axis represents the digital code input to the DLC and the Y-axis represents the % LSB DNL.



(a) SEG1

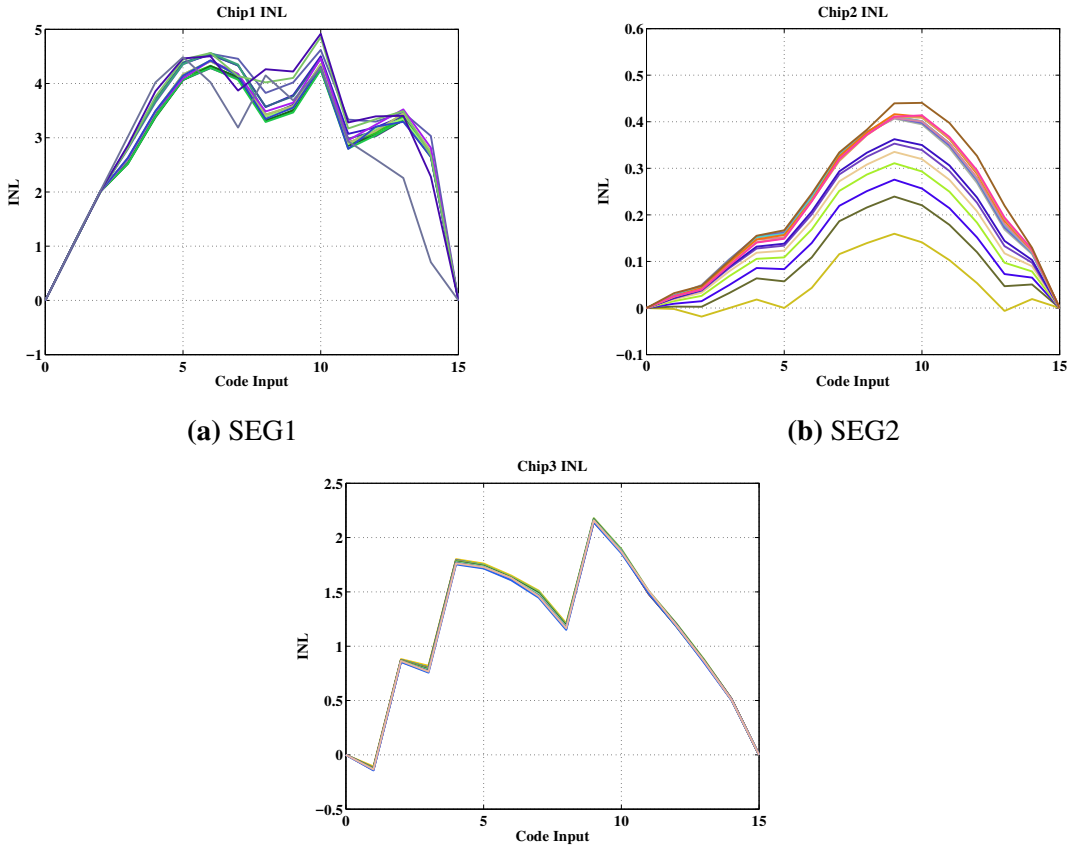
(b) SEG2

(c) SEG3

Figure 5.28: DNL at different bias settings for DLC variants

The optical power corresponding to each input code is measured for a fixed bias setting from all the three variants using an optical power meter. A constant supply voltage of 7.5 was maintained at the anode node for all of the μLED arrays for the measurement. Equation 2.19 is then be used to calculate the DNL. The SEG2 variant has the best DNL characteristics with worst case values of +10 % LSB and - 13 % LSB, which confirms 4 bit linearity over all bias settings. The DNL of SEG1 chip exceeded the $\pm$ 1 LSB limit with worst case values reaching +100 % LSB and -300 % LSB, whereas for the SEG3 chip, due to the dead pixel and comparatively low optical power from the other pixels, the resulting DNL has a range of +100 % LSB to -40 % LSB. For the SEG3 device, the V-I and I-L characteristics indicate a higher operating voltage is required to generate same amount of current compared to the SEG2 and SEG1 devices. Therefore, the supply voltage has been increased to 10V for INL/DNL measurements, which ensures the voltage across the μLEDs in the array could be approximately 8.8V and thereby increased current and optical power output. However no improvement in DNL performance has been noticed, which confirms that the metallisation and annealing scheme used for SEG3 fabrication produces inferior quality devices compared to SEG1 and SEG2. Variation of the INL/DNL in the DLC can be attributed to factors such as pixel - pixel mismatch

in the μLED array, the relative position of the lit up pixel and photo detector [143] and current mismatch from each current cell in the unary DAC. Mismatches in the DLC can be mitigated by adapting element matching schemes used in data converters such as dynamic element matching (DEM)[166].



(a) SEG1

(b) SEG2

(c) SEG3

Figure 5.29: INL at different bias settings for DLC variants

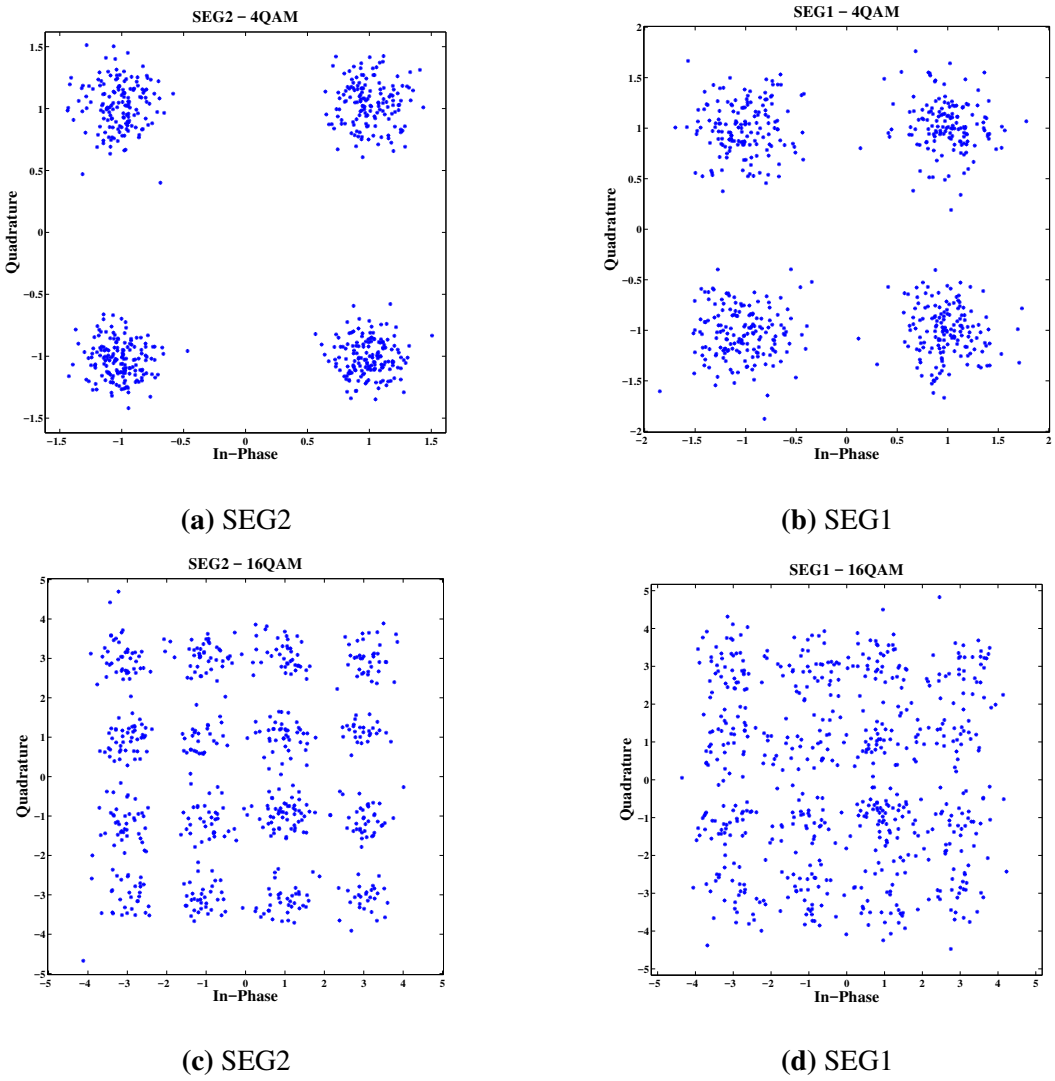
Figure 5.29 shows the INL for each DLC variant. The INL at a particular code is the sum of DNLs up to that code and expressed in number of LSBs. Therefore the DNL performance affects the INL of a variant. Confirming this, the better DNL performance of the SEG2 device has resulted in the INL of the device being less than 0.5 LSB for all bias settings at a constant μLED supply voltage of 7.5V. This ensured the specified 4-bit performance. The SEG1 and SEG2 variants have inferior INL compared to SEG2 and thereby reduced effective resolution in digital to light conversion.

5.4.4 Data transmission results

The data transmission capability of the DLC has been explored to realise free space optical (FSO) links using OFDM and PAM modulation schemes. A fixed link distance of 5 cm was used without having any additional optics. The DLC chip is mounted in the

same hardware described in Section 4.3 with an OTS FPGA board and custom built MB. Modulated digital data from the PC is transferred to the DLC chip through the FPGA.

5.4.4.1 OFDM streaming



(a) SEG2 **(b)** SEG1

(c) SEG2 **(d)** SEG1

Figure 5.30: Constellations from SEG1 and SEG2 at different QAM levels and 200 MHz clock

Matlab and associated toolboxes are used to generate a random data stream modulated with OFDM. Both 4-QAM and 16-QAM schemes were used with a 128 point FFT and CP of 10. The generated OFDM data stream is bipolar and has an amplitude clipped to $\pm 3.2\sigma$. First, bipolar to unipolar conversion is performed by adding a DC offset (the minimum amplitude from the samples) to the generated samples. For DLC inputs 4-bit digital codes are required which ranges from 0 to 15. To generate the 4 - bit digital input code from each OFDM sample, the samples are multiplied by a gain factor, which is the

ratio $15/max(OfdmSamples)$ where $max(OfdmSamples)$ is the amplitude of the sample having the maximum value. Since the maximum amplitude of the sample could be a non-integer, finally all samples are rounded to the nearest integer value which results in a sample set having values between 0 and 15, suitable for DLC inputs. The re-formatted samples are stored in the FPGA block memory and streamed to the DLC along with the sampling clock through the LVDS interface. The DLC chip, receives the data stream and converts it to unary codes before converting it to current and then to light by the μLED array. Intensity variations in the transmitted optical signals are captured by the APD receiver kept 5 cm away. The differential voltage output of the receiver is sampled by a DSO to be processed in the PC. Figure 5.30 shows the received constellations from both SEG1 and SEG2 chips for both 4-QAM and 16-QAM at a sample rate of 200 MHz. Both SEG1 and SEG2 chips realised an error free link when modulated with 4-QAM, however non-linear characteristics in the SEG1 variant makes it error prone when transmitting 16-QAM as seen from Figure 5.30d. An OFDM sample stream consisting of 32768 samples was used to assess the characteristics of the VLC link using DLC. From the BER vs data rate plot in Figure 5.31 for both SEG1 and SEG2 variants, a maximum data rate of 365 Mbps was achieved. The SEG2 variant was within the FEC threshold of 2×10^{-3} [167], whereas the SEG1 variant is limited to 130 Mbps. A BER lower bound of 7×10^{-4} is assumed for the SEG2 chip even though the received BER was 0 since the number of transmitted OFDM samples were limited to 32768. In the case of 4-QAM transmission, both SEG1 and SEG2 variants reported 0 errors for sampling rates up to 200 MHz.

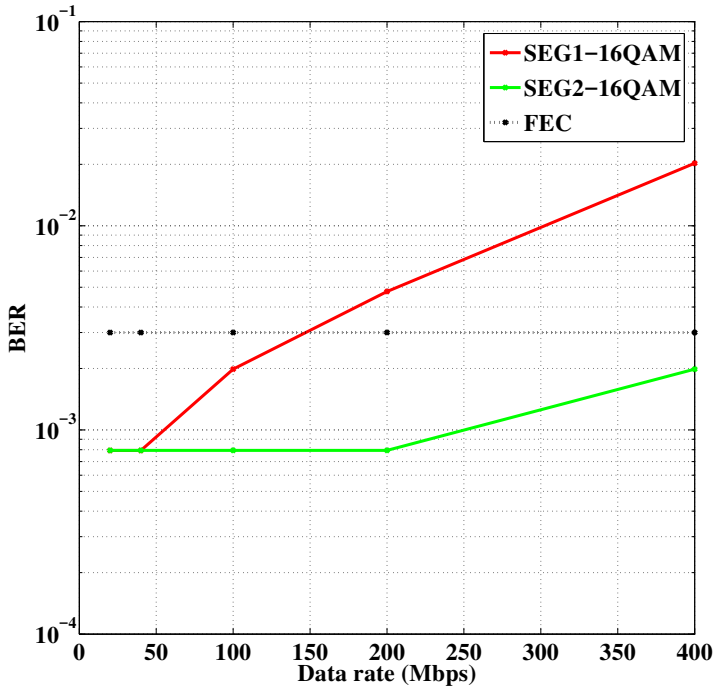


Figure 5.31: BER vs data rate for SEG1 and SEG2 DLC arrays

5.4.4.2 PAM streaming

Results from PAM transmissions performed with the SEG2 chip are presented in this section. Modulated 4-PAM transmission at different sample rates and bias currents were performed. Bias current reduction from 16 mA per LED to 2 mA per LED, which will result in a reduction in generated optical power did not cause any errors while transmitting 4096 samples at 100 MHz (Figure 5.32). The received BER was 0, however a lower bound is set to 2.4×10^{-5} (assuming 0.1 erroneous bits per 4096 transmitted bits) for plotting purpose.

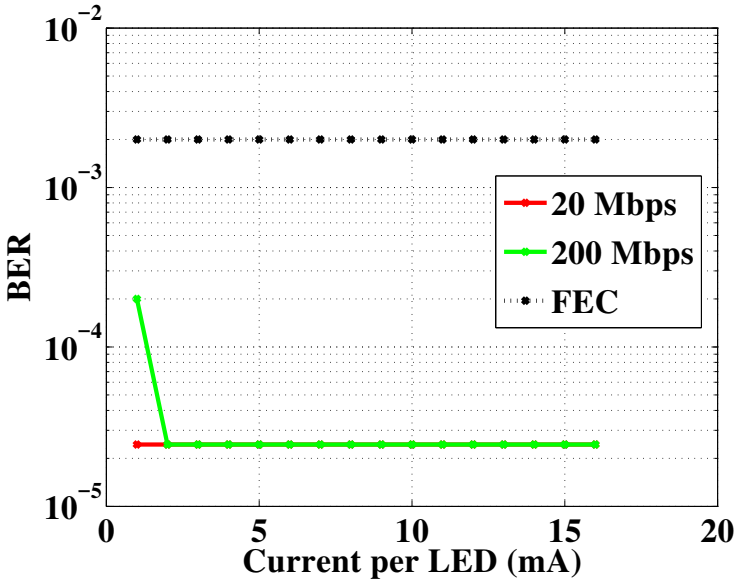


Figure 5.32: BER vs bias currents forSEG2 DLC array

Increasing the sampling rate for 4-PAM transmission indicates that data rates up to 350 Mbps could be achieved with the SEG2 chip as shown in Table 5.3.

Clock (MHz)	Data rate (Mbps)	BER
10	20	0
100	200	0
150	300	0
160	320	1.22E-04
175	350	2.81E-04
200	400	0.4992

Table 5.3: Data rate vs BER for SEG2 4-PAM

5.4.5 Power efficiency of DLC system

A current mode drive approach with the μLED either in the ON or OFF state in the DLC during data transmission should be power efficient and at the same time supports a higher

data rate compared to other drive schemes mentioned in Sections 3.2.4. Each μLED can be driven with 16 mA by the driver in DLC, which means the total current consumed by all the μLEDs when ON is 255 mA. In this state no current flows through the dummy branch and all electrical power delivered by the current mode driver is used to produce light. With a supply voltage of 8.2 V applied across μLED array and current DAC (1.2V for DAC and 7V for μLEDs), power dissipation at different components in the output stage of the DLC can be calculated as shown below.

$$\begin{aligned} P_{TOTAL} &= V \times I \\ &= 8.2V \times 255mA \\ &= 2.091W \end{aligned}$$

$$\begin{aligned} P_{DAC} &= V_{DAC} \times 255mA \\ &= 1.2V \times 255mA \\ &= 0.306W \end{aligned} \tag{5.1}$$

$$\begin{aligned} P_{LED} &= P_{TOTAL} - P_{DAC} \\ &= 1.785W \end{aligned}$$

Where P_{TOTAL} is the total power dissipated, P_{DAC} is the power dissipated in the DAC and P_{LED} is the power dissipated in the μLED array. Power efficiency is defined as the ratio of total power to the power delivered to the μLED array, which can be calculated as shown in Equation 5.2.

$$\eta_{Pall} = \frac{P_{LED}}{P_{TOTAL}} = \frac{1.785W}{2.091W} = 0.85 \tag{5.2}$$

η_{Pall}, which is 85%, is very close to the power efficiency of the DC-DC type drive schemes, this calculation is applicable only when all the μLEDs are turned ON, which is not the case during data transmission. IM/DD results in the number of μLEDs turned ON being dependant on the input digital code and thereby code dependant power efficiency. Best case power efficiency is when all the μLEDs are turned ON, where as when all of them are OFF, current from all current DAC branches are routed to the dummy branch resulting in power wastage. A more realistic estimate of power efficiency (average power efficiency) can be made assuming uniform distribution of ones and zeros in the incoming digital bit stream. This results in an average eight μLEDs to be ON and remaining 8 to be OFF. The total current through the DAC is 255 mA (~128 mA through the μLEDs and ~128 mA to the dummy branch). The dummy branch of the DLC chips are tied to 1.8V, resulting in a power dissipation (P_{DUMMY}) of 0.23 W. Power dissipated in the current DAC cells with activated μLEDs is 0.15 W (P_{DAC}), with a voltage drop of 1.2 V across

them. 0.9 W is dissipated by the μLEDs in ON state (P_{LED}). The total power ($P_{TOTALavg}$) dissipated by the system is the sum of P_{LEDavg}, P_{DAC} and P_{DUMMY} which is 1.28 W and the average power efficiency (η_{Pavg}) is calculated as shown below,

$$\eta_{Pavg} = \frac{P_{LEDavg}}{P_{TOTALavg}} = \frac{0.9W}{1.28W} = 0.7 \tag{5.3}$$

To incorporate power loss in rest of the circuitry (digital logic, biasing etc.) a de-rating factor of 0.85 is applied to the average power efficiency figure, which becomes 60%. 60% average power efficiency and data rates close to 400 Mbps supporting both OFDM and PAM schemes to realise short distance VLC links is achieved using the DLC devices fabricated.

5.5 Summary

The CMOS LED driver has been successfully used to drive different types of μLEDs to realise various VLC links. This chapter presented details of the experiments performed using μLEDs and discussed the results. As part of the UP-VLC project, an integrated high speed (1 Gbps) demonstrator has been built using various components developed by project partners. The CMOS LED driver was used in this work to drive the μLEDs. Various aspects of the current drive scheme implemented in the CMOS LED driver are studied. Options provided in the CMOS LED driver such as adjustable biasing and adjustable DC offset features helped to fine tune the performance of the system. Before performing fully integrated MIMO experiments, individual experiments were performed to characterise system bandwidth and find the optimum operating point for the μLEDs. The CMOS driver based system is compared to a commercial high performance AWG based drive scheme at similar optical power. The passive turn OFF mechanism inherently present in the NMOS based current drive scheme degrades the performance of the CMOS LED driver system at higher speeds. It was also observed that the CMOS DAC driver has approximately three times more rms jitter compared to the AWG based system. Reasons for increased jitter in output could be linked to code dependant delays in turning ON/OFF the switches in the output stage and also mismatch in routing lengths seen by different current cells (clock and data inputs are length matched up to the current cell inputs). Otherwise, by adjusting the bias and DC offset, the CMOS DAC based driver achieves similar bandwidth performance. A 1m, 1 Gbps, 4 x 4 mimo link is established using the CMOS DAC driver, μLED array, CMOS APD receiver and associated optical assemblies. It is the first time an integrated custom built CMOS driver targeting VLC is used to demonstrate a high speed MIMO link successfully. It is possible to increase the link distance or coverage by increasing the number of LEDs used or by using LEDs capable of emitting more optical power.

An integrated optical DAC or DLC is realised by wire bonding a unary current DAC and a 16 x 1 μLED array. Compared to other optical DACs published using discrete components [80] and integrated circuitry [144], this work has a higher data rate and modulation flexibility. Up to 16-QAM OFDM and 4-PAM transmissions were carried out achieving hundreds of Mbps transmission. Even though a fixed link distance of 5 cm was set for the DLC experiments, using suitable optics or a higher power μLED, the link distance can be increased. The resolution of the DLC can be scaled to increase the modulation complexity and signal fidelity by increasing the number of μLEDs in the array. The average power efficiency of the DLC drive scheme is 60%, which is the highest when delivering data at the rate of hundreds of Mbps compared to other LED drive schemes implemented for VLC utilising discrete of integrated components.

Chapter 6

Driving Off-the-shelf (OTS) LEDs

6.1 Overview

Since their inception, the application and installation base of light emitting diodes (LEDs) has increased exponentially due to their favourable features such as long life time and high energy efficiency compared to other light sources. These devices are manufactured primarily aiming for lighting applications and thus not optimised for high speed visible light communication (VLC) due to their limited modulation bandwidth compared to micro light emitting diodes (μLEDs) [64, 168] or laser diodes (LDs). However, by utilising advanced spectrally efficient modulation schemes such as orthogonal frequency division multiplexing (OFDM) and pulse amplitude modulation (PAM) and applying different equalisation techniques, VLC links using OTS LEDs have been realised achieving Gbps operation. These links use either discrete components or commercially available signal generators or arbitrary waveform generator (AWG) to drive the LEDs. The complementary metal oxide semiconductor (CMOS) current digital-to-analog converter (DAC) based LED driver developed in this work can modulate OTS LEDs for VLC owing to its open drain architecture and higher current output than other reported current DACs. This chapter presents the results of VLC links created using the CMOS LED driver and different OTS LEDs. The high power efficiency of the current DAC based drive scheme is maintained when driving OTS LEDs. A single-input single-output (SISO) link is characterised using a blue LED and wavelength division multiplexing (WDM) experiments using a red-green-blue (RGB) LED are carried out. The capability of the link is studied at various link distances, modulation depths and sample rates. A novel drive scheme where both the main and dummy branch of the current DAC are utilised to drive a LED is experimented and results presented. This configuration realise an optical differential transmission system providing higher link SNR and thereby better BER.

6.2 Publication List

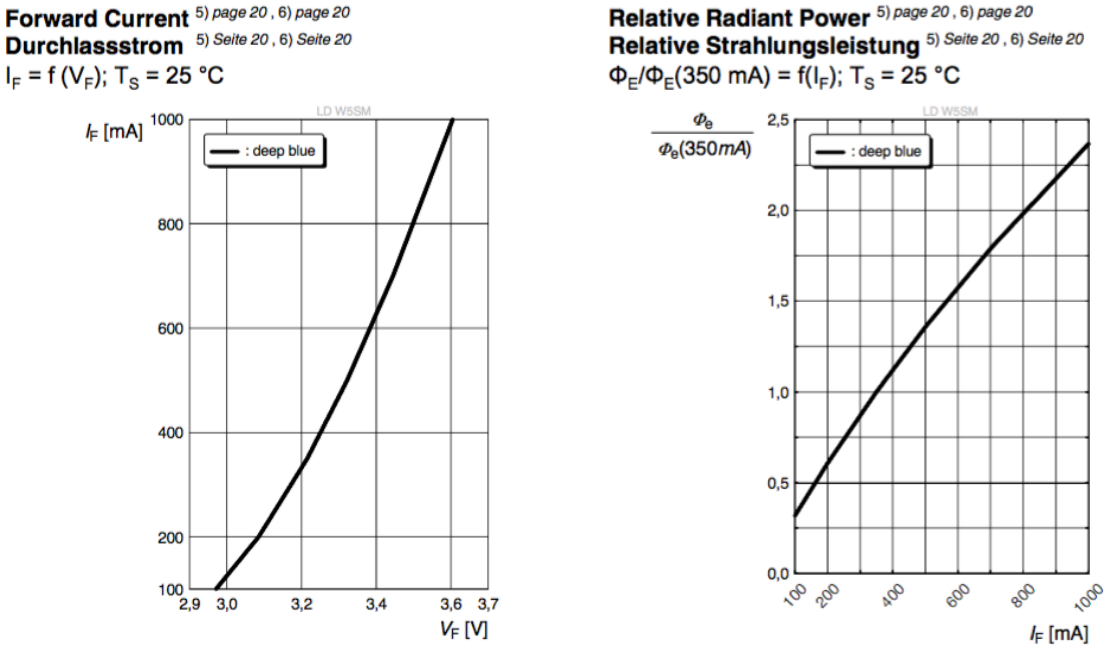
Experiments and results discussed in Sections 6.3.1 and 6.5 have been presented at the International Communication Conference, 2015 and published in the conference proceedings [31].

6.3 SISO links

The single-input single-output (SISO) mode operation of CMOS LED driver along with high current OTS LEDs are used to realise practical VLC links spanning a few meters. Such links, owing to the high efficiency of the LED and high power efficiency of the CMOS LED driver enables an energy efficiency communication system capable of achieving 100's of Mbps link speed. Since the driver circuit is integrated, it could be installed into the LED light bulbs to realise the VLC link. Off-the-shelf (OTS) LEDs are widely available for the purpose of ambient lighting. One of the methods used to generate white light generation for conventional lighting applications is the use of blue LEDs coated with a complimentary yellow phosphor [169]. A portion of the emitted blue light is absorbed and re-emitted as yellow, generating an overall whitish light from the luminary. Phosphor coating results in reduced bandwidth due to the slow response of the phosphor itself. It is possible to ignore the effects of phosphor by using a suitable blue filter in the receiver so that everything except the faster modulation bandwidth blue wavelength is rejected. In this experiment instead of using a filter and there by reduction in received optical power, a blue emitter is used.

6.3.1 Blue variant

An Osram Golden Dragon Blue variant, is a ThinGaN device in surface mount device (SMD) packaging emitting at 455 nm with an optical efficiency of 49% [157]. It has a typical turn ON voltage of 3.2 V. From the V-I characteristics of the device shown in Figure 6.1a, it can be seen that the device is capable of drawing up to 1 A. The modulation bandwidth of the device is measured to be 10 MHz. It is measured by driving the LED with a modulated sinusoid at different frequencies generated by a commercial AWG and capturing the intensity modulated light using a high speed photo PD [170]. The amplitude of the captured sinusoids are recorded in a DSO [171] and analysed to deduce the modulation bandwidth of the device. For the experiments in this work, the LED is biased at a maximum of 255 mA, which is the full scale output of a current DAC in the CMOS LED driver. The daughter boards discussed in Section 4.3.1.1 are used to mount these LEDs and connect them to the CMOS LED driver for experiments.



(a) V-I characteristics **(b)** I-L characteristics

Figure 6.1: V-I and I-L characteristics of the OTS blue LED [157]

6.3.1.1 Experiment Setup

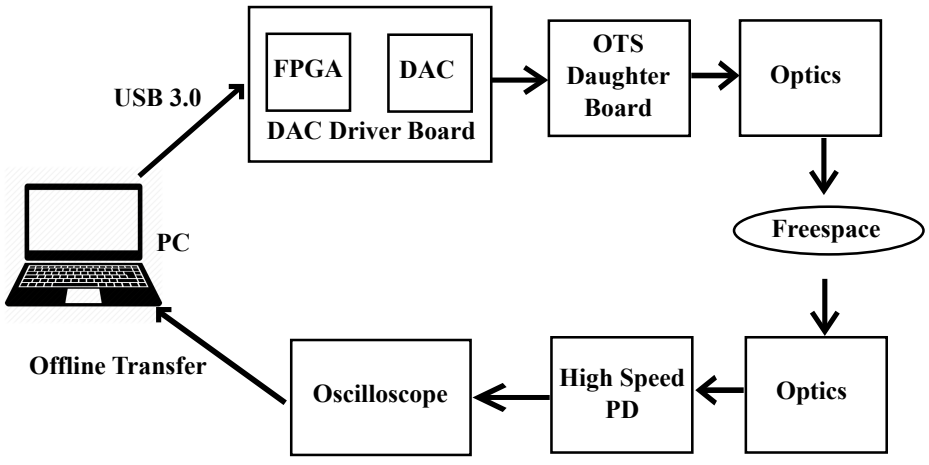


Figure 6.2: Block diagram OTS LED SISO link.

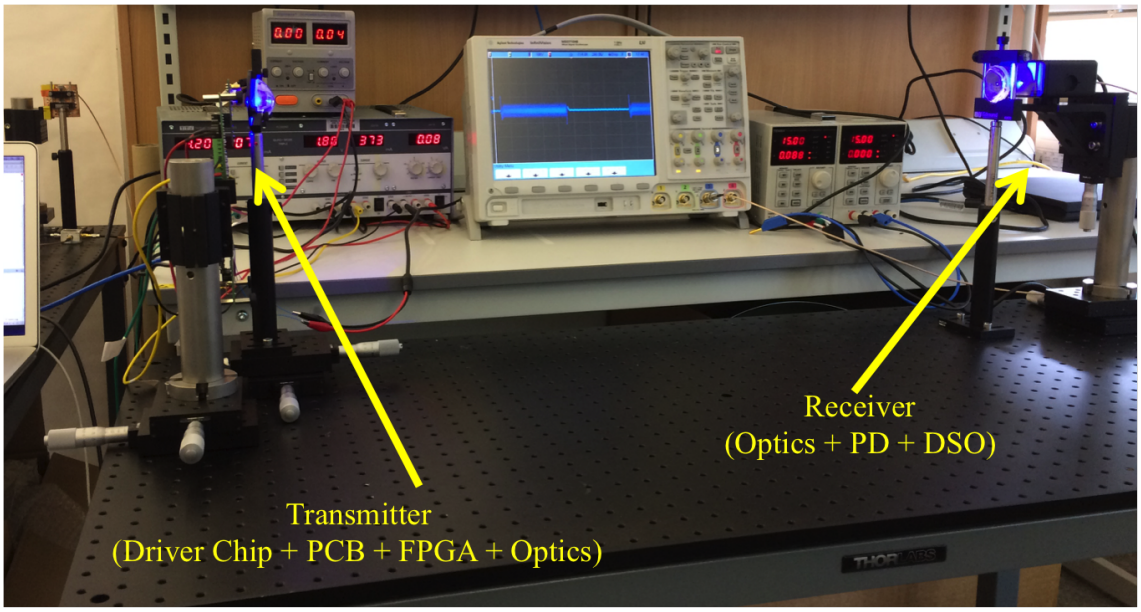
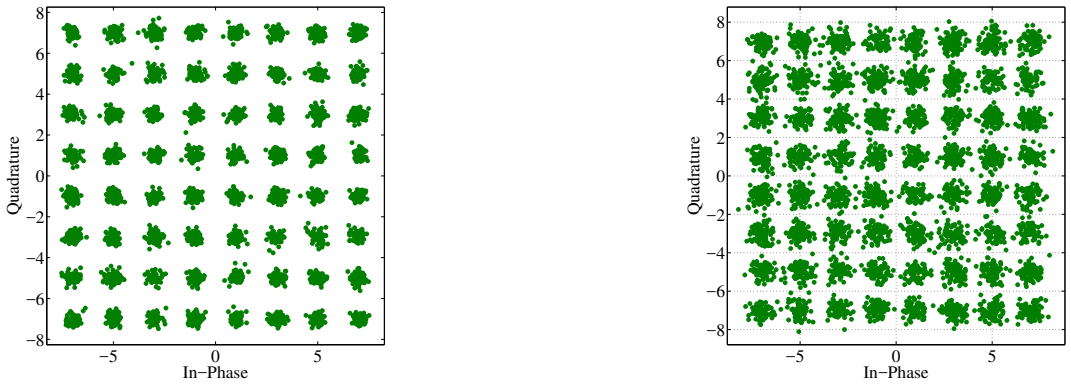


Figure 6.3: Blue OTS LED experiment setup

Figure 6.2 shows the major components used to realise the OTS LED SISO VLC link. The transmitter system is similar to the one used for the UP-VLC demonstrator presented in Section 5.3. It consists of a PC generating the modulated data, which is transferred to the OK FPGA board through the USB 3.0 interface. The CMOS LED driver configured in SISO mode receives the modulated data and generates a proportional output current in the configured channel to drive the OTS LEDs. The OTS LEDs are mounted in the daughter card, which is attached to the MB through board to board connectors (more details about the hardware can be found in Chapter 4). A commercial P-type Intrinsic N-type photo detector (PIN PD) (New Focus 1601 [170]) having bandwidth of 1 GHz and wavelength range of 320 to 1000 nm is used to capture the transmitted signal. For maximum optical power collection, lenses (Thorlabs ACL4532), were used at the transmitter to collimate the light and at the receiver to collect and focus the light on the receiver plane. The distance between the transmitter and receiver is 1 m for this experiment. A DSO (Agilent MSO7104B [171]) is used to sample the output of the photo detector. Collected data is post-processed using the Matlab firmware which is used to generate the data stream.

6.3.1.2 Results

An OFDM modulated data stream is generated in the PC



(a) 20 MHz sample rate and 64 QAM **(b)** 40 MHz sample rate and 64 QAM

Figure 6.4: 64 QAM transmission over OSRAM Golden Dragon Blue LEDs

The received constellations while transmitting 64-QAM are shown in Figure 6.4 and SNR is shown in Figure 6.5. A 120 Mbps data rate is achieved at a link distance of 1 m. Performance improvement is possible by employing advanced bit - power loading schemes in OFDM and by using a higher sampling clock for the DAC.

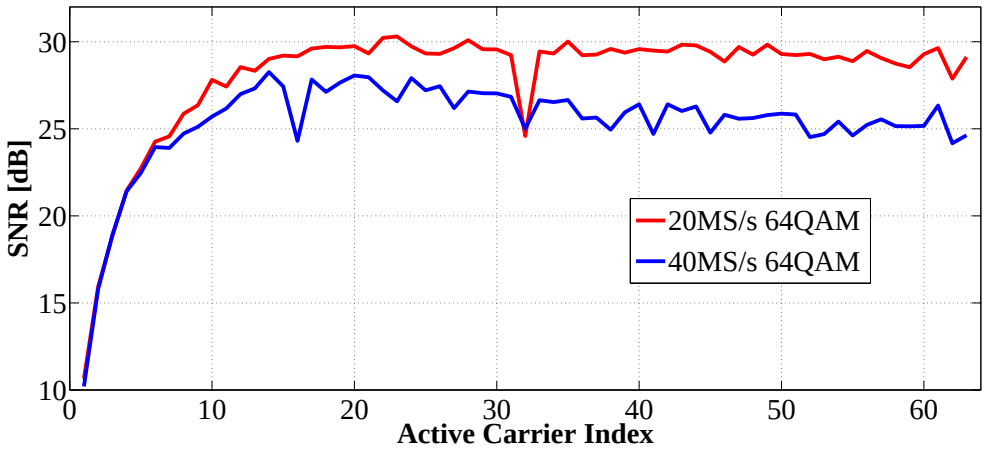


Figure 6.5: Blue LED SNR at different sampling rates

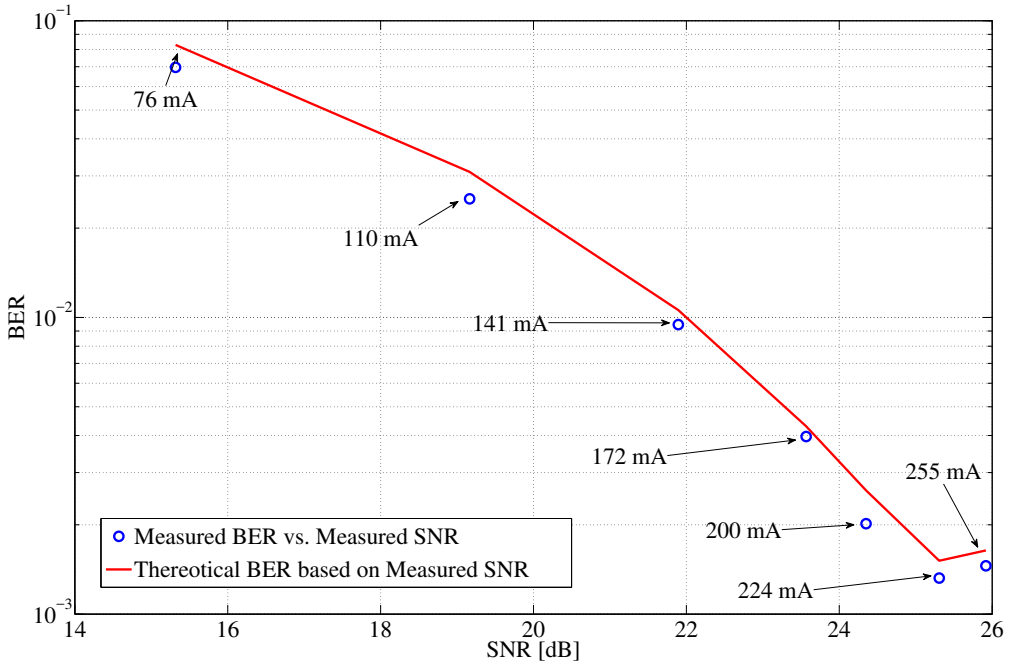
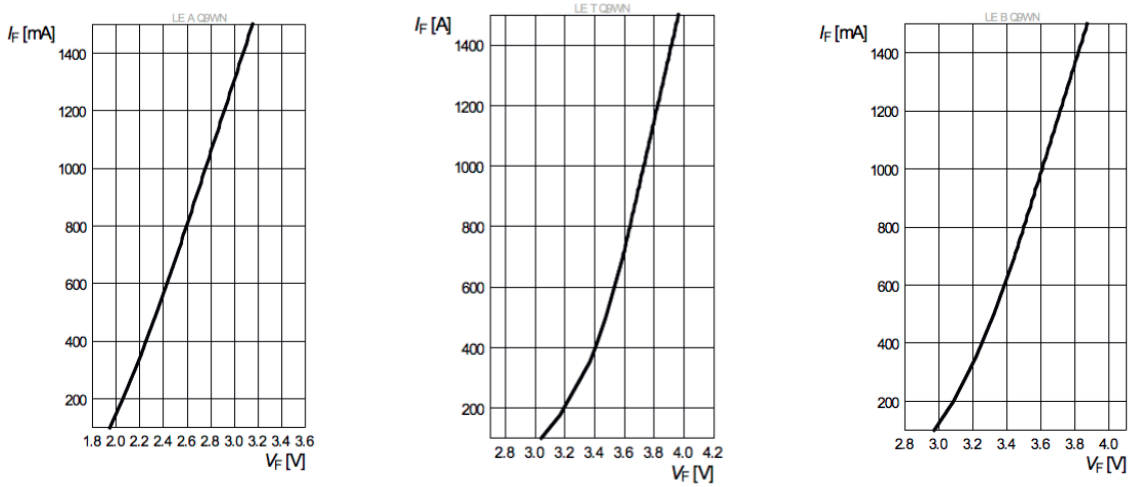


Figure 6.6: BER vs SNR at theory vs measured

The BER vs SNR at different bias currents shown in Figure 6.6. As the full scale current increases, the received optical power as well as SNR goes up. The BER also follows this curve until 224 mA, beyond which the BER improvement was not measured due to saturation at the PD and increased non linear distortions in the DAC at higher bias currents.

6.3.2 RGB variant

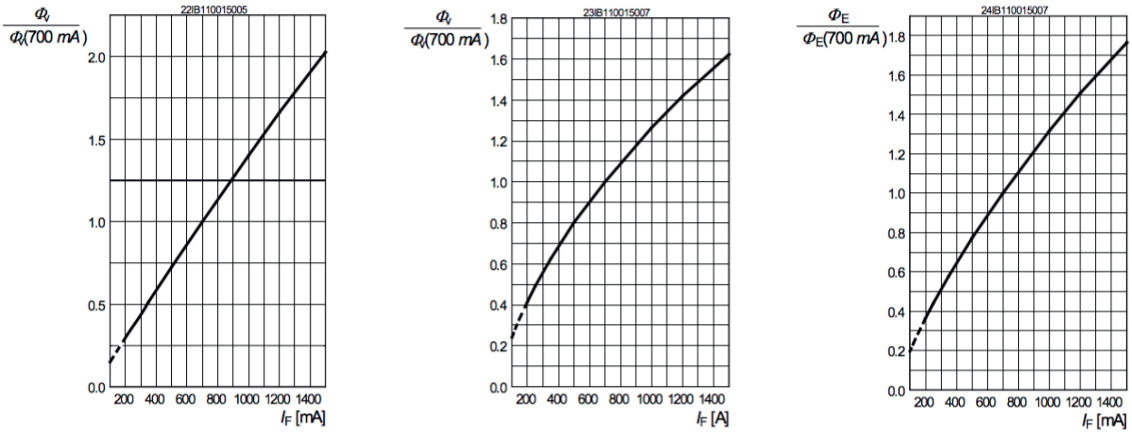
RGB LEDs available commercially can produce white light by turning on the red, green and blue channels. In this section, a VLC system is realised using an OTS RGB LED and performance of each channel is characterised individually (SISO operation). A CMOS LED driver can drive 4 individual LEDs with four independent data streams. The UP-VLC demonstrator has utilised this feature to realise a Gbps MIMO VLC link using an array of custom built μLEDs (detailed in Section 5.3). The SISO mode operation of the CMOS LED driver is explored where incoming digital data is copied to all channels in the CMOS LED driver. The particular RGB LED used for this experiment is an Osram Ostar, LE RTDUW S2W [146]. The RGB variant has four individual LEDs, red (625 nm), green (527 nm), deep blue (453 nm) and a phosphor coated blue LED generating white light. In the experiments discussed in this chapter, only red, green and deep blue LEDs are used. Typical turn ON voltages for each channel are 2.5 V (red), 3.6 V (green) and 3.45 V (deep blue) and each channel is capable of handling currents of up to 1.4 A (see Figure 6.7 for V-I characteristics.).



(a) V-I Red channel **(b)** V-I Green channel **(c)** V-I Blue channel

Figure 6.7: V-I characteristics of RGB module [146]

The I-L characteristics of the RGB variant is shown in Figure 6.8. Since each channel is capable of delivering a maximum full scale current of 255 mA in the CMOS LED driver, it can be assumed that the current to optical output is a linear function for all three channels.



(a) I-L Red channel **(b)** I-L Green channel **(c)** I-L Blue channel

Figure 6.8: I-L characteristics of RGB module [146]

The RGB LED is packaged in an SMT package which requires a re-flow soldering method for mounting on the PCB. The LED daughter board discussed in Section 4.3.1.1 had a suitable footprint to load the RGB LED. A forced convection re-flow oven (C.I.F FT-02) is used to mount the RGB LED to the daughter board.

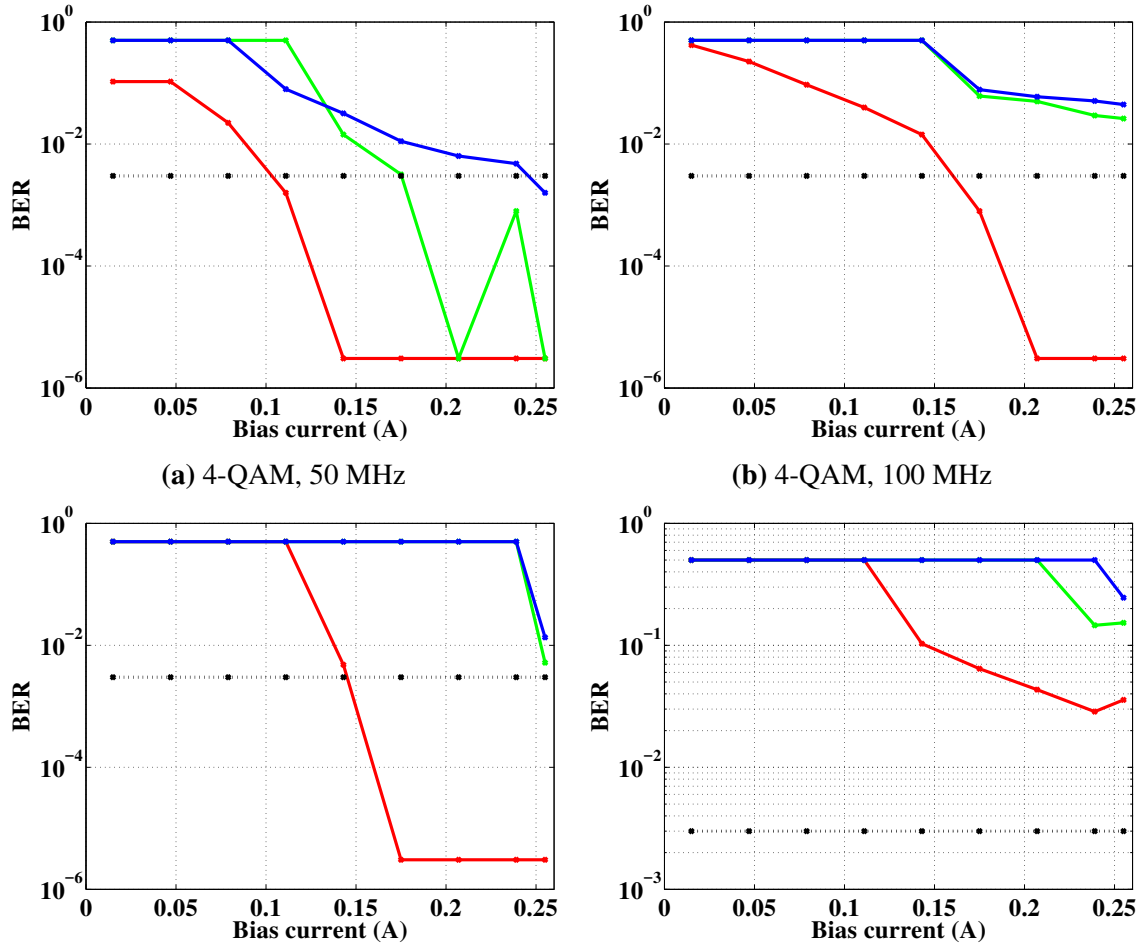
6.3.2.1 Experiment Setup

The experiment setup is similar to the one shown in Figure 6.2, except for the type of photo detector used. The APD used in the receiver circuitry is an OTS Si APD [160]. The red luminary is connected to channel 1, Green to channel 2 and Blue is wired to channel 4 of the CMOS LED driver. Channel 3 of the CMOS LED driver is wired to the White LED of the RGB chip, but not used for experiments. To study the performance of each channel independently, the rest of the channels are disabled during SISO transmission. The OTS RGB chip and APD receiver are kept at the same height from the optical bench used for experiments. Depending on the experiments, the link distance is varied from 40 cm to 2 m. For some experiments, commercial reflector (Ledil, CN12159_LENA-S-DL [172]) is used at the transmitter side to collimate the light beam from the RGB to increase the received optical power. An OFDM scheme was used for the measurements with a 128 point FFT, CP = 10, and N-QAM modulation. The value of N is changed based on the link performance and the SNR estimated from received pilot frames. Initial measurements are done at a link distance of 1 m for all luminaries. The link distance, sample rates, bias currents and constellation levels were varied to find out the optimum link criteria at different distances for each colour channel.

6.3.2.2 Bias current vs BER at 1 m

Keeping the link distance at 1 m, the SISO performance is measured for each colour in the RGB LED chip. Figure 6.9 summarises the important results from these experiments. At a sampling rate of 100 MHz and 16-QAM modulation, none of the bias settings (16 mA to 255 mA) could provide a usable link (Figure 6.9d). The received BER is beyond the FEC threshold for all the three channels. It can be seen that the BER performance of the red channel starts to improve once the bias current exceeds a full scale setting of 111 mA. At a bias current of 239 mA, the red channel has the best BER performance in this configuration 2×10^{-1}. For a 16-QAM configuration, when the sampling clock is reduced to 50 MHz, the red channel BER performance improved. The BER of the received stream dropped below the FEC threshold for all bias currents above 143 mA. Figure 6.9c shows this result. It has to be noted that for the red channel, the received BER was 0 for all full scale bias currents above 175 mA, which means all the 32768 bits transmitted were received without any error in this system. In a real system, as the number of transmitted bits increases, the probability of erroneous bits increases as well. To plot the BER result on a logarithmic axis, the value of 0 is replaced with a BER value of 3.5×10^{-6} (assuming 0.1 erroneous bit per 32768 transmitted bits). The green and blue channels in this configuration do not give an error free link , but at the highest bias setting (255 mA), the BER drops. Reducing the QAM levels from 16 to 4 (Figure 6.9b), whilst using a 100 MHz sampling clock gives a similar performance to 16-QAM

50 MHz, where the red channel is usable for bias currents greater than approximately 150 mA, but the green and blue channels are not usable at all. For the red channel, reducing the sampling rate to 50 MHz at 4-QAM (Figure 6.9a) reduced the bias current required for an error correctable link to 111 mA. In the same configuration, the green channel BER performance improved and it can provide usable links for all bias currents greater than 175 mA, whereas the blue channel is usable only at the highest bias current of 255 mA. To summarise, at a 1 m link distance, the red channel has the best performance for the parameters varied and it was able to achieve data rate close to 100 Mbps, whereas for the green and blue channels, the data rate was 50 Mbps. The red channel performs the best, then green and blue has the worst performance. The performance pattern of the three channels matches the responsibility characteristics of the Si APD, which is more sensitive to the red wavelength than blue.



(a) 4-QAM, 50 MHz

(b) 4-QAM, 100 MHz

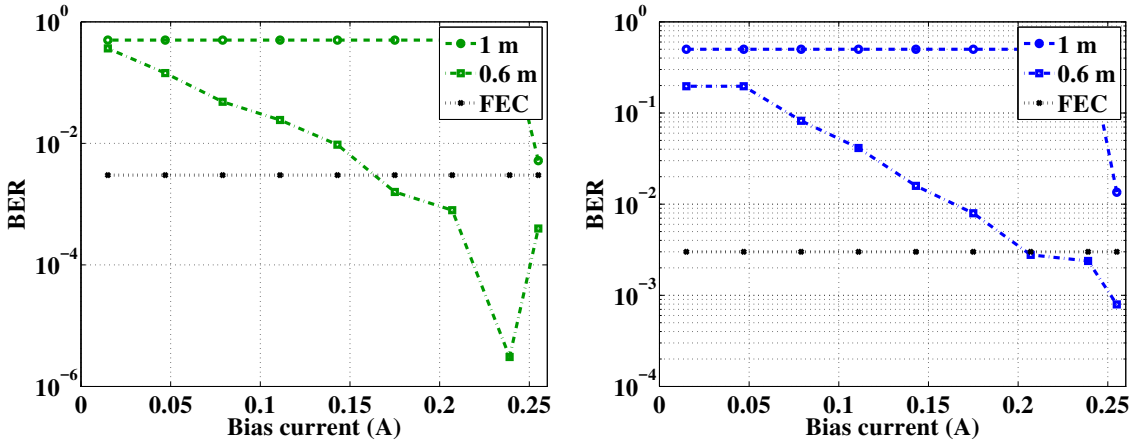
(c) 16-QAM, 50 MHz

(d) 16-QAM, 100 MHz

Figure 6.9: BER vs Bias current at different sample rates and modulation depths

6.3.2.3 Link distance vs Bias current

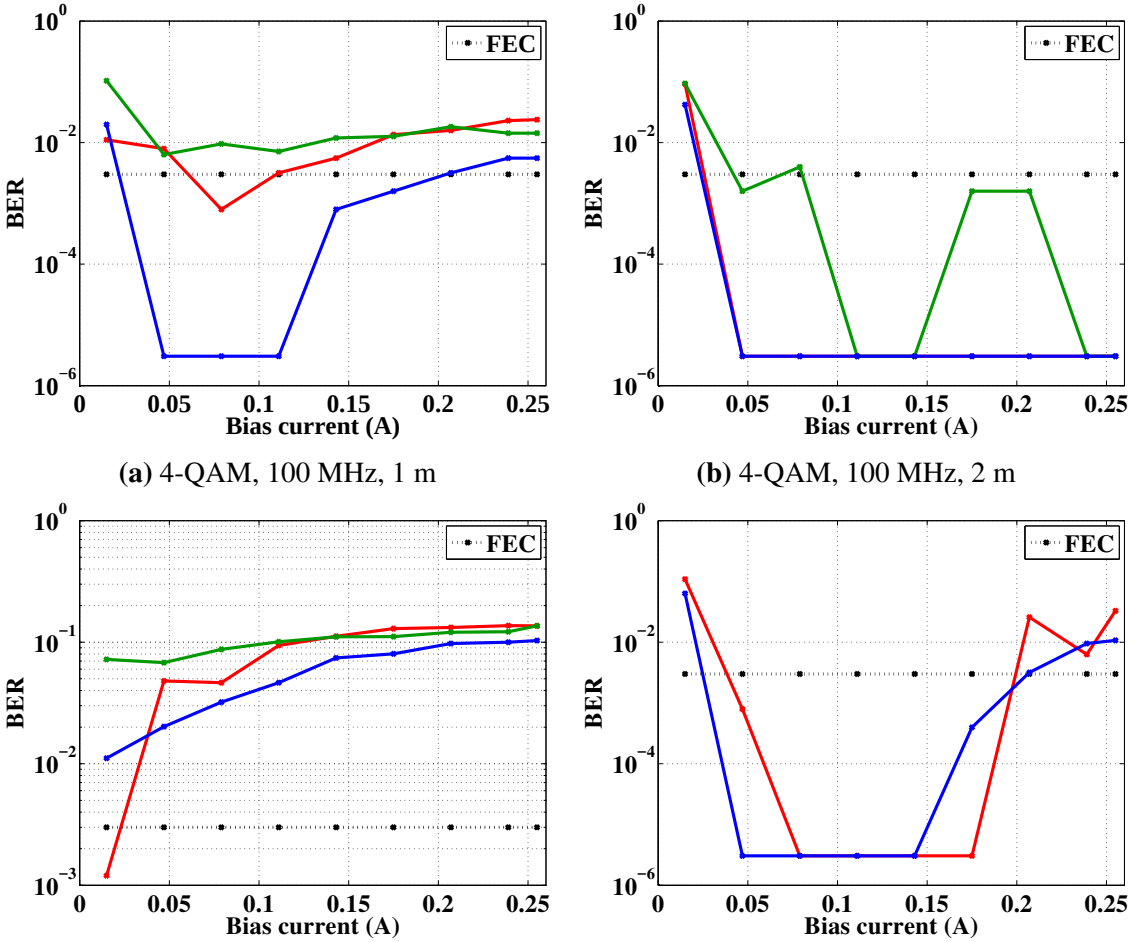
The blue and green channels were not usable for most of the scenarios tested at 1 m as seen before. Reducing the link distance will increase the received optical power for both green and blue channels and thereby increase the received SNR and improve the BER. For this purpose, the sampling clock was fixed to 50 MHz and the QAM levels set to 16. The red, green and blue channel BER performances at 1 m are shown in Figure 6.9c and were discussed earlier. The link distance was reduced to 60 cm and the resulting BER performance of the green and blue channels are shown in figure 6.10a and 6.10b. The performance of the green channel BER (within FEC threshold) improves at this distance for all bias currents above 175 mA and for the blue channel above 207 mA. A dynamic bias control scheme is required to make all the channels usable depending on the link distance.



(a) Green **(b)** Blue

Figure 6.10: BER vs Bias currents at 1 m and 0.6 m (16-QAM and 50 MHz)

6.3.2.4 Improving performance of the SISO link



(a) 4-QAM, 100 MHz, 1 m

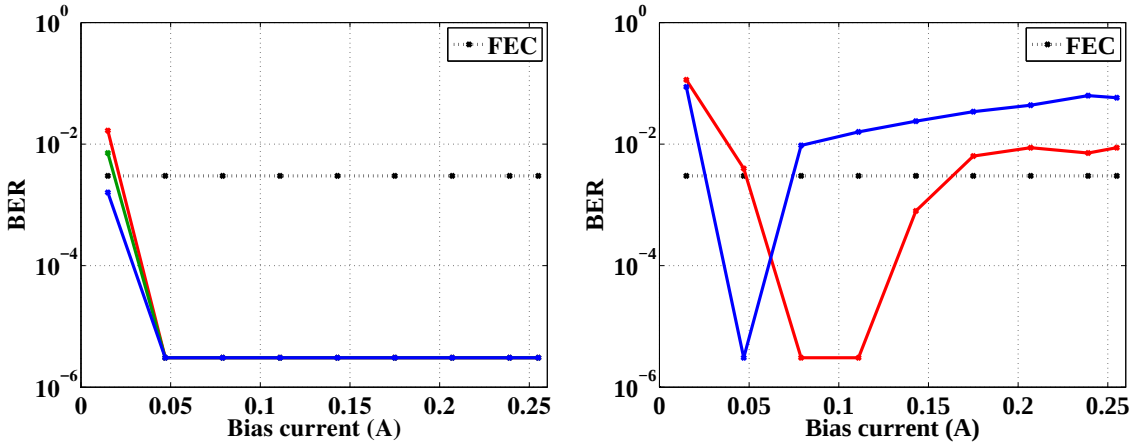
(b) 4-QAM, 100 MHz, 2 m

(c) 16-QAM, 50 MHz, 1 m

(d) 16-QAM, 50 MHz, 2 m

Figure 6.11: BER performance at 2 m and 1 m with parabolic reflector

To increase the link distance beyond 1 m, a commercially available parabolic reflector [172] is added to the transmitter, which collimates the light thereby increasing the received optical power and narrowing the transmission beam. The results of adding the reflector for link distances of 1 m and 2 m are shown in Figure 6.11. For a 4-QAM link (Figure 6.11a), at 1 m , both the red and green channels have erroneous links which is due to a non-linearity introduced in the system by the APD at increased received optical power (photo diode saturation). In the 16-QAM, 50 MHz test, for the red channel, at currents above 15 mA, the link is saturated and unusable, whereas both green and blue channels are unusable. Results from the 2 m link with 4-QAM transmission at 100 MHz (Figure 6.11b) and 50 MHz (Figure 6.11d).



(a) 4-QAM, 50 MHz, 2 m link **(b)** 4-QAM, 200 MHz

Figure 6.12: 2 m link performance highest and lowest sampling clocks

With the reflector added, all the channels were able to give error free performance at 2 meters while transmitting 4-QAM at a rate of 50 MHz which translates to approximately 50 Mbps per channel (ignoring OFDM overheads) for all bias currents above 47 mA (Figure 6.12a). This indicates a very flexible VLC link can be realised using the CMOS LED driver where output intensity can be adjusted by varying the bias current, without compromising the data rate capability of each channel. The red and blue channels were also able to give a peak performance of 200 Mbps per channel at 2 m as for bias currents in the range 50 - 100 mA, which indicates that if the link distance is increased further, data rate can be maintained by increasing the bias current.

6.4 WDM Mode

Using RGB LEDs to generate white light also opens up the possibility of using the individual red, green and blue channels for VLC. This method is suitable for scaling the data rate of a VLC system. This method has been widely studied using LED drivers realised from OTS components or AWGs. One of the first RGB WDM link was reported by [25], achieving 803 Mbps at a distance of 12 cm using a commercial AWG to intensity modulate the luminaries. In [173] a Gbps 10 cm VLC link is established by using an OTS RGB LED and DMT modulation scheme. In this channel, two output channels from a commercial AWG are used to modulate the LEDs in the RGB module. A 2.5 m RGB link using DMT modulation is reported in [75] which employs a commercial AWG and bias tees to drive two channels of the RGB chip. However it was not clear if WDM was implemented in this work. [27] reports a 3.22 Gbps VLC link using a commercially available RGB LED however at a link distance of 25 cm. An RGB and Yellow WDM link is reported in [23] achieving 5.6 Gbps also using a commercial AWG and biasing network

to drive the LEDs. It is also possible to use a single colour channel for data transmission since the switching response of individual channels will be faster than a phosphor coated LED [29]. Pre-emphasis and post-equalisation circuits are used in [29] to improve the frequency response of the system. All the reported works so far used a multi-channel AWG combined with a biasing network to drive the RGB luminaries. In this section, the WDM capability of the CMOS LED driver is explored to drive an OTS RGB LED.

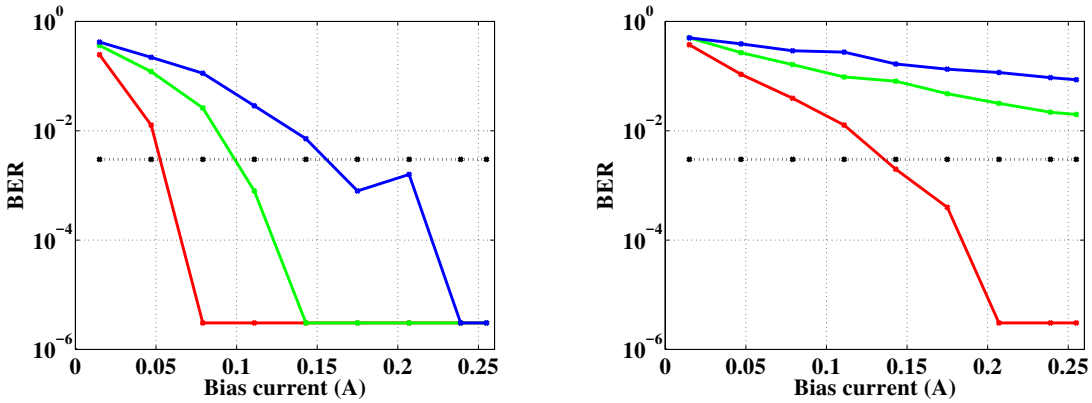
6.4.0.1 Experiment Setup

Matlab is used to generate three different OFDM modulated data streams (128 FFT points and CP = 10). The individual data streams are scaled and quantised to suit the 8-bit digital input for the DACs in the CMOS LED driver. An empty data stream (contains only 0) is generated for the unused channel in the CMOS LED driver. Samples from the four data streams are interleaved and clocked into the CMOS LED driver through the LVDS interface. The CMOS driver is configured to be in MIMO mode with a clock division factor of 4. This results in the incoming data stream being down sampled (Section 3.4.5.3 details down sampler) and passed to the respective channels at $\frac{1}{4}$ of the incoming clock rate. A fixed supply voltage of 4.7 V is used to bias each LED in the RGB chip mounted on the daughter card. A single APD based receiver [160], which is used for the SISO experiments (see Section 6.3.2) is used to capture the intensity variations and generate a proportional voltage. All the channels are transmitted simultaneously, which produces white light, channel separation is performed at the receive side by using optical band pass filters. For the red channel a narrow band laser line filter, FL632.8-10 [174], which has a peak transmission of 70% is used. Similarly for green channel, FB520-10 [175] is used with peak transmission of 50% and for blue channel FB450-10 is used [176] which has peak transmission of 45%. The presence of the filters reduce the amount of optical power captured by the receiver proportional to the peak transmission figures. The red filter has the highest peak transmission and blue has the worst which will be reflected in the results. The output of the receiver is captured by a DSO [171] and transferred to a PC for processing. In the PC, data is demodulated and performance metrics such as BER and link SNR are derived.

6.4.0.2 Results

The transmitter and receiver are kept 1 m apart and a sampling clock of 100 MHz is provided to the CMOS LED driver. An internal clock divider is set to divide the incoming clock by four and provide a buffered version of the divided clock (25 MHz) to each channel. The bias setting is varied from 15 mA to 255 mA for each channel and the BER is estimated from the received data stream. Results from 16-QAM transmission are shown in Figure 6.13b. The green and blue channels failed to provide a usable link across the

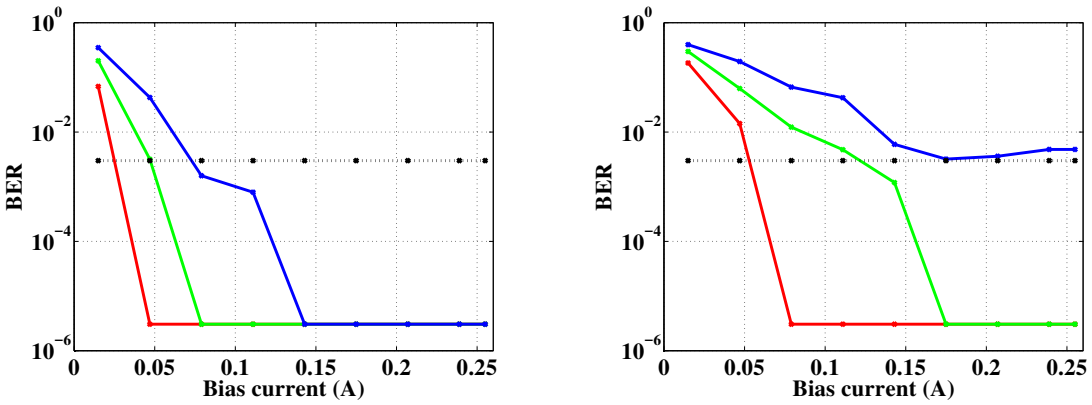
bias current range and the red channel is only usable from 143 mA to 255 mA. Beyond 207 mA, for the number of bits transmitted, no erroneous bits were received. For this configuration, the system is usable only beyond 143 mA with a data rate of approximately 50 Mbps (ignoring OFDM overheads). Performance of the red channel is comparable to the 4-QAM SISO result shown in Figure 6.9a. Reducing the modulation from 16-QAM to 4-QAM (Figure 6.13a) increases the BER performance of all channels. The aggregate data rate of approximately 150 Mbps is achieved (50 Mbps per channel) for all bias currents above 150 mA. Below 150 mA, the blue channel performance deteriorates leaving just the red and green channels suitable for an error correctable VLC link with an aggregate date rate of approximately 100 Mbps. From 50 mA to 100 mA , only the red channel is usable (~50 Mbps) and below 50 mA, none of the channels could provide a usable link.



(a) 4-QAM **(b)** 16-QAM

Figure 6.13: Bias current vs BER at 1 m transmitting WDM

Reducing the link distance to 0.6 m improves the performance of all channels (Figure 6.14) compared to the 1 m link. The aggregate data rate has increased to ~100 Mbps (bias currents above 143 mA) due to better performance by the green channel combating the losses due to filter peak transmission and responsivity of the APD used in the receiver. The performance of the red channel has also improved at 0.6 m for 16-QAM modulation giving an error free link from 79 mA and above up to 255 mA. Compared to 1 m, at 60 cm the bias current required to achieve 150 Mbps ($3 \times 50 Mbps$) has reduced to 79 mA for a 4-QAM scheme (Figure 6.14a).



(a) 4-QAM **(b)** 16-QAM

Figure 6.14: Bias current vs BER at 60 cm transmitting WDM

Reducing the link distance further down (0.4 m) while modulating at 16-QAM results in saturation at the receiver for the red channel at higher currents (175 mA and above) and increasing the BER. However the performance of both the green and blue channels has improved resulting in an increase in aggregate data rate to 150 Mbps from 100 Mbps for the 60 cm link. This can be seen in Figure 6.15

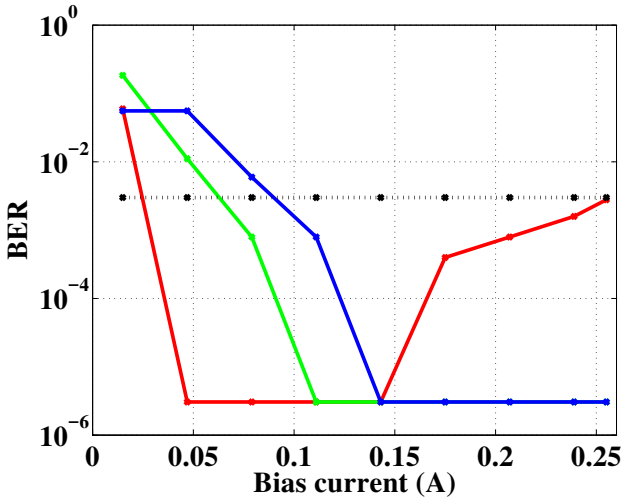


Figure 6.15: Bias current vs BER at 40 cm transmitting 16-QAM WDM

A WDM link realised with the CMOS LED driver and an OTS RGB LED achieved an aggregate data rate of 150 Mbps. The data throughput of the WDM link can be easily increased by, increasing the sampling clock per channel. The CMOS LED driver is designed to operate for input clock rates up to 500 MHz (see Section 3.4.2.2), which means that a per channel clock of 125 MHz is feasible, and thereby aggregate data rates up to 375 Mbps. This is higher than the maximum data rate achieved from the SISO links mentioned earlier using the same LED.

6.4.1 Drive current vs Correlated colour temperature (CCT)

Colour temperature (CT) is defined by CIE as the temperature of a black body radiator when heated up and is expressed in Kelvins. As the temperature is increased, the colour of the black body changes from red to blue. The correlated colour temperature (CCT) of a source generating whitish light is defined as the temperature of a black body radiator, whose colour is closest to the colour of the white light source [97]. Black body emission at different temperatures can be correlated to conventional light sources such as incandescent lamps or LEDs resulting in a CCT [177]. The dominant wavelength of the individual LEDs in the RGB chip changes depending on the forward current (measurements available in [146]), which results in variations in the CCT of the mixed white light produced. Maintaining a constant CCT irrespective of variations in current or temperature is a challenge and different feedback mechanisms has been reported to mitigate this [178, 179]. In a VLC system employing intensity modulation, current flowing through each LED varies continuously depending on the sample rate and type of modulation used. This means the chromaticity coordinates for an intensity modulated luminary varies and there is variation in the colour quality of the luminary. [180] discusses the effect of light quality when the average current varies for VLC enabled luminaries. This means there is a limit to the data rate that can be achieved in a CCT constrained system. SISO and MIMO results from the RGB LED [146] indicate that, an achievable data rate varies over distance and bias current for each colour channel. A compromise is inevitable between the data rate required and CCT of the light from the RGB LED.

6.4.1.1 Experiment setup

CCT measurements are performed in a dark room to prevent any external light source affecting the collected results. Additionally, a dark cloth is placed over the test bench, luminary and sensors to ensure that no light from the computing equipments or other indicators affects the results.

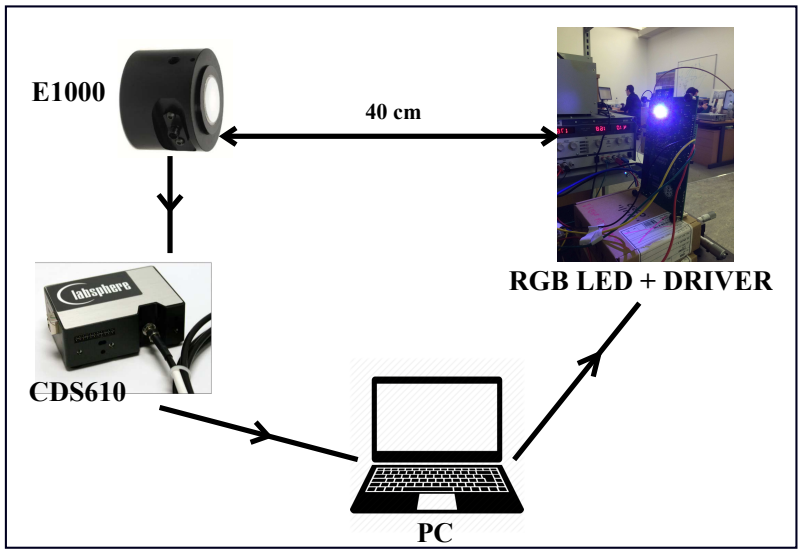


Figure 6.16: CCT measurement setup

Figure 6.16 shows the laboratory setup to measure the CCT of the RGB LED while driven by the CMOS LED driver at different bias currents. A commercial spectrometer, Labsphere CDS610 [181] along with a spectral irradiance receiver E 1000 [182] are used. The RGB LED chip is kept at a distance of 40 cm from the irradiance receiver for all the measurements. The current through each channel is varied from 16 mA to 255 mA, by varying the bias setting configuration in the serial register of the CMOS LED driver from 0 to 15. The spectrometer comes with a software package capable of calibrating the spectrometer system and also capturing various photometric and radiometric parameters including the chromaticity x, y coordinates required to generate the CIE chart [177]. Communication between the spectrometer and the PC is through a USB interface. The spectrometer data (mainly chromaticity points) is collected and saved in the PC for post processing.

6.4.1.2 Bias vs CCT

Chromaticity points are collected over different bias settings for two modulation schemes 4-QAM and 16-QAM at a 50 MHz sampling rate for the red, green and blue channels. The following method is used to derive the chromaticity coordinates (x,y) for the equivalent white colour generated by mixing of red, green and blue colours at specified bias settings. If $(x1, y1)$, $(x2, y2)$ and $(x3, y3)$ can be used to represent the chromaticity coordinates measured for the red, blue and green channels respectively, then the chromaticity coordinates for the mixture of the three primary color is represented by the centroid point of the triangle formed by the coordinates of each colour. Figure 6.17 shows this in the CIE chromaticity chart.

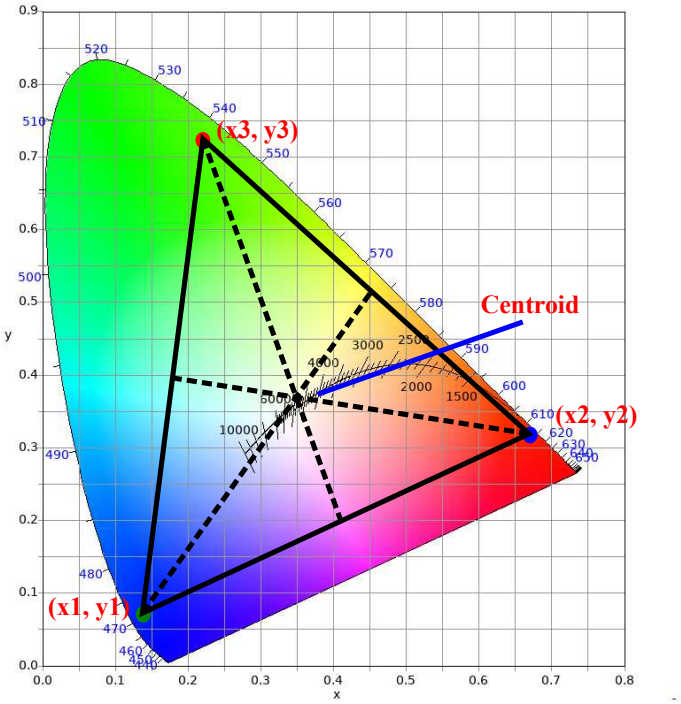


Figure 6.17: Method to estimate equivalent white colour from Red, Green, Blue

The centroid of the triangle can be calculated using Equation 6.1

$$x = \frac{x1 + x2 + x3}{3}$$
$$y = \frac{y1 + y2 + y3}{3} \tag{6.1}$$

where (x,y) is the centroid coordinates.

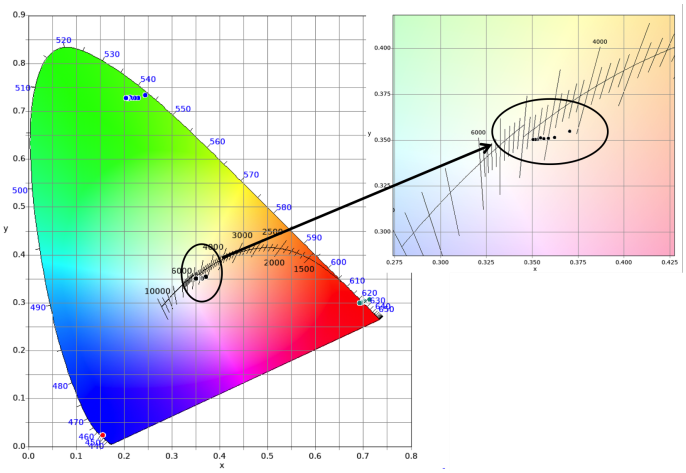


Figure 6.18: CIE 1931 plot showing CCT dispersion at 4-QAM

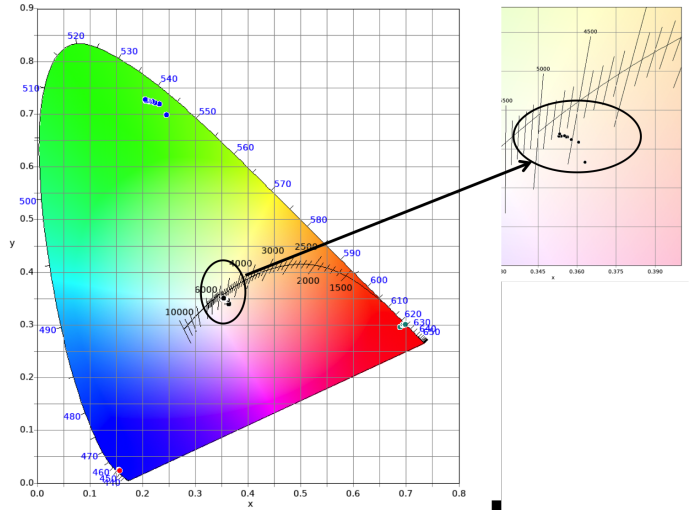
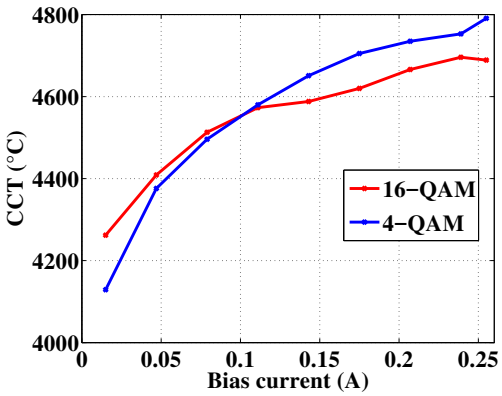
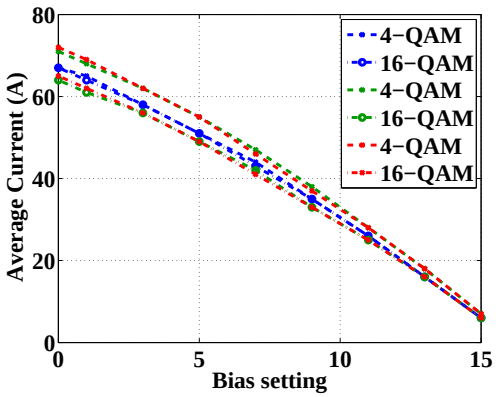


Figure 6.19: CIE 1931 plot showing CCT dispersion at 16-QAM

Figures 6.18 and 6.19 show the CCT coordinates in the chromaticity plot for both 4-QAM and 16-QAM.



(a) CCT vs Bias current at 4, 16 QAM



(b) Average Current vs Bias setting at 4, 16 QAM

Figure 6.20: Correlation between average current and CCT

The measured average current drawn by the each channel while transmitting 4-QAM is greater than 16-QAM for same number of sub carriers (128).

6.5 Differential Optical Drive

Driving signals differentially is a well-known concept and widely used for both short distance and long distance wired communication links. For example, to transfer information between different electrical circuits or different PCBs various differential signalling schemes such as LVDS or peripheral component interconnect express (PCIe) are used. The physical layer of communication technologies such as Ethernet, USB etc. also use

differential signalling techniques. The popularity of differential signalling schemes is due to the lower voltage swing requirements at the transmitter, comparatively higher speed operation, increased received voltage swing and noise immunity. For a communication system, these characteristics could mean and increase in received SNR and thereby better decision making and BER. A proof of concept is presented which uses the differential signalling technique in the optical domain for VLC. Tje differential current cells used in the DACs of the CMOS LED driver make it inherently suitable to implement this drive scheme.

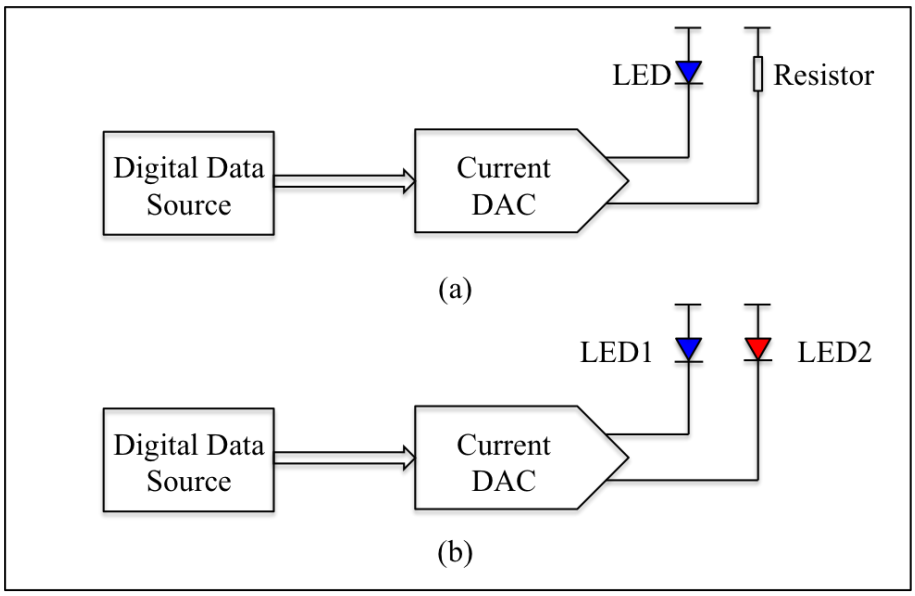


Figure 6.21: Differential optical drive concept

Figure 6.21 illustrates a conventional single ended LED drive scheme (a), and the proposed differential optical drive scheme (b), implemented using a current DAC in the CMOS LED driver. In the conventional drive scheme only the main branch of the current DAC is connected to an LED and the dummy branch is loaded with a resistor whereas in the differential drive scheme, both the output branches of the DAC are loaded with LEDs emitting different colours. For each DAC input, the current through the main branch is proportional to the input code and the total current through the DAC is constant. The input code and main branch current can be related as ,

$$I_{main\_branch} = I_{full\_scale} - I_{dummy\_branch} \tag{6.2}$$

where I_{main_branch} is the main branch current, I_{full_scale} is the full scale current and I_{dummy_branch} is the current through the dummy branch. The light output generated is proportional to

the current flowing through the corresponding branch which can be expressed as,

$$L_{main\_branch} = L_{constant} - L_{dummy\_branch}$$

$$L_{LED1} = k(I_{full\_scale} - I_{main\_branch}) \tag{6.3}$$

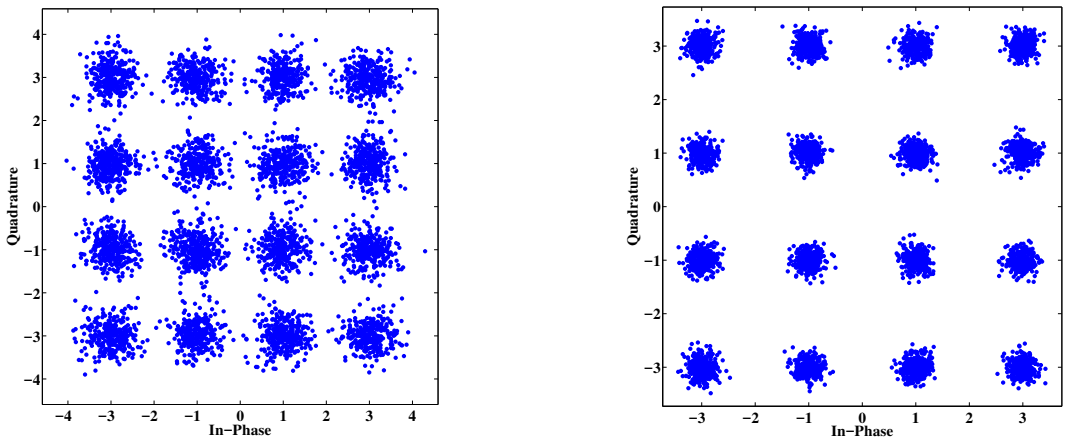
$$L_{LED2} = k(I_{full\_scale} - I_{dummy\_branch})$$

where L indicates the intensity of light generated by the LEDs (LED1 or LED2) and k is the current to light conversion factor. Two receivers are required to capture the light generated by the two LEDs and suitable colour filters are required at the receiving end to filter the required colour. The electrical output from the two receivers is then subtracted and demodulated.

6.5.0.1 Experiment setup

The CMOS driver chip mounted in the MB receives the data to be transmitted from the PC through the FPGA board. In this experiment, instead of using luminaries generating two different colours, two blue LEDs from Osram [157] are connected to the main branch and dummy branch of the DAC1 in CMOS LED driver. Since the daughter card (Section 4.3.1.1) does not support the differential drive scheme, the LEDs are attached to the MB using cables by soldering them onto the PCB. The LEDs and corresponding photo receivers [170] are isolated to avoid constructive interference. To collimate the light generated by both LEDs and to focus it at the receiver plane, lenses (Thorlabs ACL4532) are used in the optical path. The LED and its corresponding photo receiver are kept 30 cm apart for this experiment. The outputs of the each receiver are connected to two different channels of a DSO (Agilent MSO7104B).

6.5.0.2 Differential drive results



(a) Single Ended scheme **(b)** Differential Ended scheme

Figure 6.22: Received constellations Single ended and Differential drive

The performance of the link is estimated by transmitting OFDM modulated data (10 MHz, 16-QAM, 128 point FFT) at a bias setting of 255 mA. The link is characterised as a differential optical link as well as a single ended link (processing the signal received from the main branch), which enables a fair comparison between schemes depicted in Figure 6.21. Comparing the received constellations from the single ended link (Figure 6.22a) and differential link (Figure 6.22b), it can be seen that the differential optical drive has superior performance. The improvement in performance of the differential scheme presented here can be attributed to the improvement in SNR in differential mode due to the increased signal amplitude and also reduction in noise.

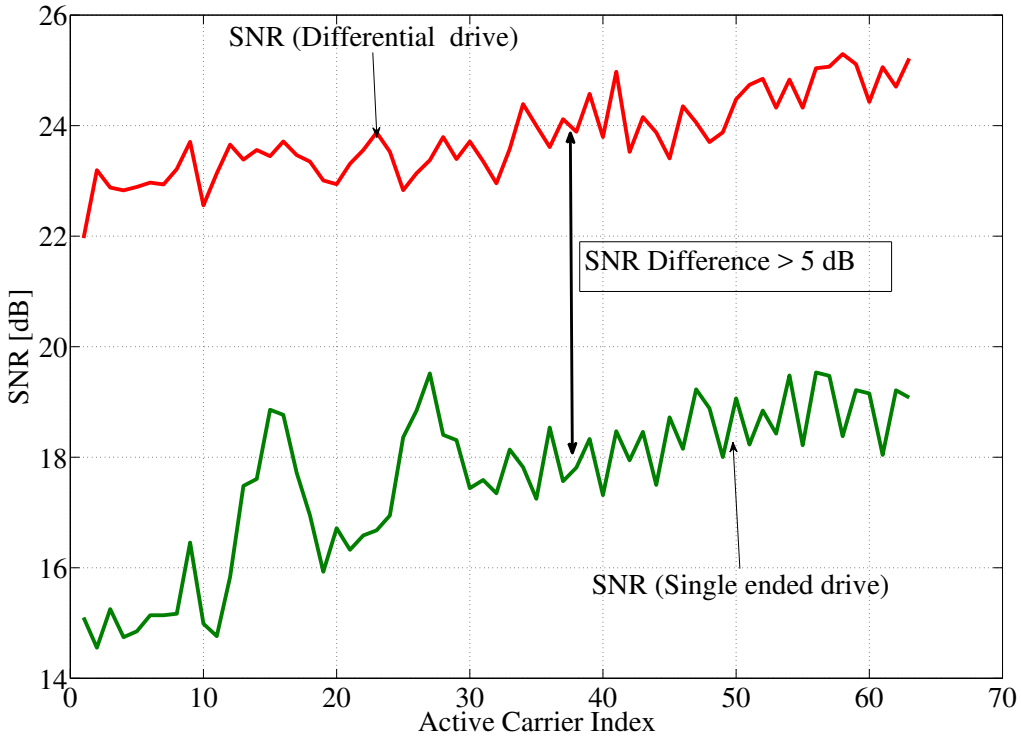


Figure 6.23: SNR improvement using differential drive

6.5.1 Power efficiency (OTS LED)

The CMOS LED driver has been used to realise VLC links using various OTS LEDs. Experiments in previous sections detailed the results from these VLC links. In this section, the power efficiency of these drive schemes are calculated based on the measured average voltage and average current consumption while transmitting OFDM modulated data. OFDM modulation was used in both SISO and WDM links realised using OTS LEDs. If P_{TOTAL} is the total power consumed by output side of the transmitter (DAC and LED) and P_{DAC} is the power consumed by the output stage transistors in the DAC, power efficiency η of the current DAC based LED driver can be calculated as shown in Equation 6.4.

$$\eta = 100\left(1 - \frac{P_{DAC}}{P_{TOTAL}}\right) \tag{6.4}$$

When no data is transmitted and at full scale current of 255 mA through the driver with a supply voltage of 4.3 V, Equation 6.4 can be substituted as show in Equation 6.5.

$$\begin{aligned}\eta &= 100\left(1-\frac{P_{DAC}}{P_{TOTAL}}\right)\\ &= 100\left(1-\frac{V_{DAC}\times I_{DAC}}{V_{SUPPLY}\times I_{SUPPLY}}\right)\\ &= 100\left(1-\frac{1.2V\times 0.255mA}{4.3V\times 0.255mA}\right)=72\%\end{aligned} \tag{6.5}$$

While transmitting OFDM, the average current through the driver is measured and efficiency is re-calculated to be 67% at maximum sampling rate and full scale range. De-rating the power efficiency figure by 85% to incorporate losses in rest of the circuit results in the power efficiency of the driver while driving the OTS LED to be 57%. From the power efficiency analysis of the CMOS LED driver while driving different types of LEDs and in DLC mode Sections 5.3.6 and 5.4.5 , it is clear that power efficiency of the system depends on the type of LED used due to variations in threshold voltage and the voltage headroom required to achieve the necessary current swing. Compared to other integrated drive schemes, the CMOS current steering DAC based LED driver is capable of realising fast VLC links (hundreds of Mbps) without compromising power efficiency.

6.6 Summary

The flexibility of the CMOS LED driver is further explored by using its high current drive capabilities to realise VLC links using OTS LEDs. SISO links established with a blue LED [157] were able to achieve data rates up to 120 Mbps at a link distance of 1 m at a full scale current of 255 mA. The SNR achievable in this link made it possible to use 64-QAM. The achievable data rate was limited by the bandwidth of the LED, which was measured to be approximately 10 MHz. It is possible to increase the speed of this link by using equalisation techniques (pre or post equalisation) or adaptive loading of the carriers (bit and power loading) depending on the channel estimate. Experiments using SISO links were also performed with a commercially available RGB LED chip [146]. The SISO link characteristics were studied by varying different parameters such as link distance, sample rate, QAM levels and bias currents. The APD based receiver used for this experiment was most sensitive to the red wavelength and least to the blue, which affects the results as well. The red channel has the best performance and blue has the worst. If the link distance increases, link performance can be maintained by increasing the bias currents (16 mA to 255 mA) and vice versa. Reducing the link distance and maintaining higher bias currents

results in saturation of the receiver and an erroneous link. The bias current adjustment feature of the DAC is quite useful when realising a flexible VLC link at different link distances. To increase the link distance beyond 1 m, a commercial parabolic reflector is added , which collimates the light beam and increases the received optical power. Data rates up to 200 Mbps were achieved at a link distance of 2 m using the reflector. The VLC link capacity could be increased by a using WDM scheme and a RGB luminary is a suitable choice for this. A multichannel CMOS LED driver is used to realise a WDM link using the RGB LED. Simultaneous transmission using the three different LEDs is made possible by using the MIMO mode of the LED driver. Similar to the SISO mode, bias current adjustment provides the flexibility to configure the link performance needed depending on the link distance or modulation levels. Varying the bias current results in a shift in the emitted wavelength and thereby variation in CCT. The effect of CCT variation is studied by varying the bias currents and it was seen that equal bias variation across all the colours resulted in a CCT variation from 4100°C to 4800°C. This means if the CCT of the luminary has strict specification, achievable data rates and link distances are constrained. A new method of driving two LEDs using a single current DAC to realise a differential optical drive is studied and the demonstrator provided better SNR compared to a single ended scheme. An average power efficiency of 57% is estimated while driving OTSs LEDs modulated with OFDM. The power efficiency of the current DAC based drive scheme varies depending on the type of LED and the equivalent series resistance modelling the slope in the V-I characteristics. OTS LEDs, owing to their lower equivalent series resistance, dissipate less power in them compared to the μLEDs, therefore while driving μLEDs (as seen in UP-VLC demonstrator and DLC), the CMOS LED driver has higher power efficiency. Comparing the achievable data rates and power efficiencies with other integrated drive schemes for VLC shows that the CMOS current steering DAC approach has better performance.

Chapter 7

Conclusion and Future work

7.1 Summary

Work described in this thesis has demonstrated a high current output current steering DAC based LED driver for VLC capable of operating at speeds at 500 MHz whilst maintaining high output stage power efficiency. Figure 3.4 is updated to include the power efficiency of the CMOS LED driver from different experiments conducted as part of this work and is shown in Figure 7.1.

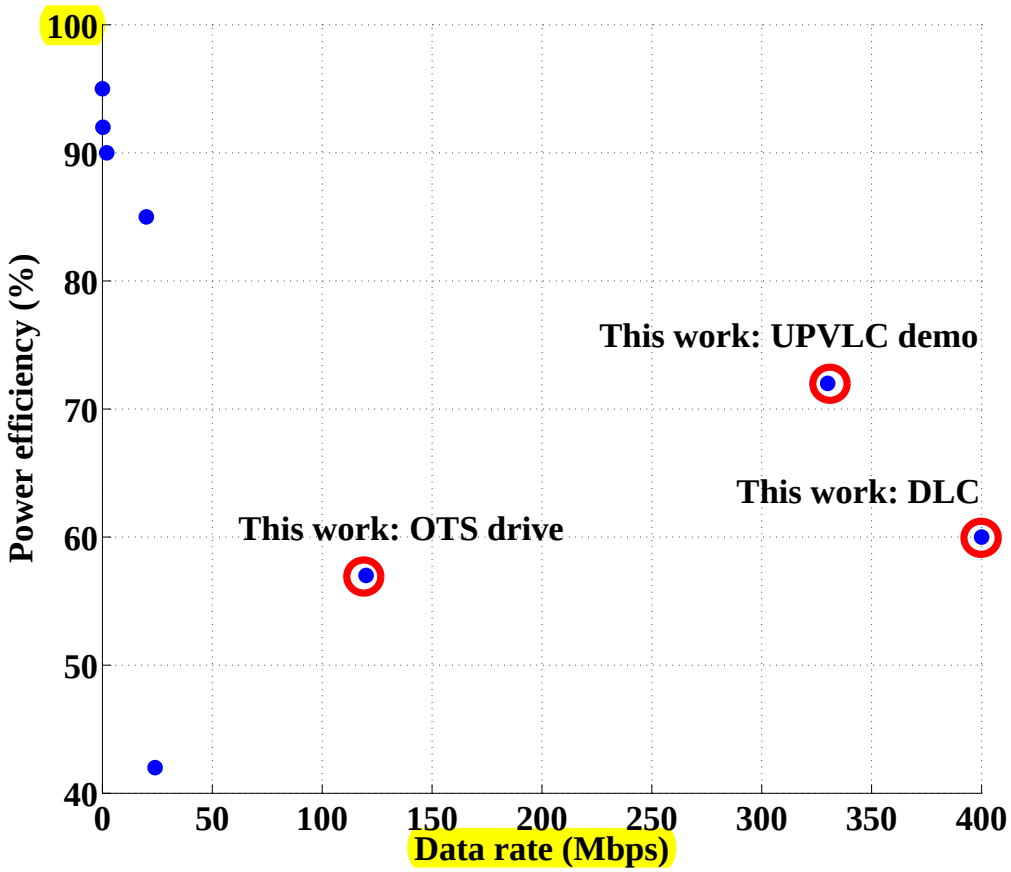


Figure 7.1: Data rate vs Power efficiency of integrated drive schemes for

The driver chip with multi-channel capability is used to realise various VLC links using different types of LEDs (μLEDs, OTS LEDs and a RGB LED). The driver chip is realised in a 180 nm CMOS process with die area of ~30mm^2 is a possible way forward for mass implementation of VLC systems. A multi channel MIMO demonstrator utilising all the four channels in the CMOS LED driver achieved Gbps performance at distance of 1 m by driving four GaN μLEDs. The concept of DLC was implemented as an integrated system by wire bonding a GaN μLED array on to CMOS driver chip die achieving data rates of a few hundred Mbps using OFDM. The integrated DLC reported an average power efficiency of 85%, due to the low voltage compliance required by the drive stage. The SISO and WDM capability of the driver was exploited at high currents while driving OTS LEDs.

A review and discussion of the literature published in the VLC domain is undertaken in Chapter 2. A critical review of the literature reveals a few major road blocks in the search for a wide spread, cost effective implementation of VLC driver circuit miniaturisation and power efficient drive schemes. Understanding of various aspects of the VLC system is crucial to bridge the gaps mentioned. The required level of understanding in different areas such as modulation schemes, the characteristics of the LED, different LED drive

schemes and DAC structures were gained and presented in this chapter.

Chapter 3 discussed the specifications and design aspects of the IC developed. The specification of the integrated circuit was derived from the system demonstrator specifications of the UP-VLC project and the characteristics of the OTS LEDs. A suitable CMOS technology is chosen after considering operating speed requirements, cost of fabrication, availability of PDK and the supporting voltage range needed. Circuit design and simulation details are also presented in chapter 3. The designing of the core analogue block involved sizing the current cells to carry the high currents (up to 255 mA) specified, while at the same time being able to switch at a rate up to 500 MHz. Peripheral digital circuitry is carefully designed to deliver the control and data signals to each driver without any timing or signal errors. High current paths inside the driver chip needed careful consideration in the layout to avoid ground bounce and there by individual current mismatch. Layout techniques to minimise and equalise the resistance of ground net connection for all the cells was crucial to attain the specified linearity. Since the design presented in this work is based on CMOS technology, it can easily be mass produced at lower costs and energy efficiency compared to the discrete driver incarnations or commercial AWG based drive schemes.

The driver circuit designed in chapter 3 needs an electronic platform for characterisation and associated software to control it. The fourth chapter details the custom built characterisation platform and associated software. A custom PCB (MB), designed and fabricated to house the CMOS LED driver, is presented along with description of different configurations for power supplies and current biases. Digital control of the LED driver is realised through an OTS FPGA board attached to the MB. Verilog based firmware is developed to control the FPGA board. Data to be transmitted is generated in the PC and transferred to the FPGA and then to the DAC. The MB has options to attach different types of LED to the DAC. This chapter also presents the electrical characterisation results of the DAC such as INL, DNL and SFDR. For electrical characterisation instead LEDs, two identical resistors were used as load for the DAC. Data transmission tests were also performed electrically with outputs sampled across load resistors. These tests indicated that DAC could operate up to 250 MHz (limited by the FPGA).

Results from μLED based experiments were presented in Chapter 6. μLEDs arrays for the experiments were fabricated and characterised by partners at the University of Strathclyde. These devices are not optimised for power consumption or thermal performance unlike their OTS counterparts, but they have a higher modulation bandwidth owing to their smaller dimension and increased injected current density. A MIMO demonstrator is built using individual components from each partner in the UP-VLC project, including the CMOS LED driver detailed in this thesis. Characterisation was done at the University of Oxford with DAC operation, FPGA firmware and PC interface software support provided by Edinburgh. The demonstrator achieved Gbps operation at a link distance of 1 m

meeting the UP-VLC design objective. A comparison of the performance of the CMOS LED driver and a commercial AWG based drive scheme was undertaken. At low sampling rates, the DAC performance is similar but it degrades at higher sampling rates due to absence of an active extinguishing mechanism for the LEDs. This chapter also presented results from the integrated DLC which achieved a data rate of 400 Mbps at an average power efficiency of 72%.

The high current capability of the CMOS LED driver was put to test by driving a number of different types of OTS LEDs. Results from these experiments are presented in Chapter 7. WDM was demonstrated using an OTS RGB LED. Digital control of the bias current through the DAC makes it possible for dynamic link distance adjustment while maintaining the data rate. CCT variations due to the change in average current through the LEDs will limit change in modulation index or bias current control if a consistent CCT is required.

7.2 Critical Discussion

The aims of the research in this thesis were to miniaturise the LED drivers used for VLC using CMOS technology, investigate a suitable drive scheme that can be implemented as an integrated circuit capable of providing high power efficiency at high data rates and to deliver the high output current levels required by OTS LEDs. We were able to achieve these aims for the first time and reduce the system footprint using the CMOS LED driver and an FPGA. However there are few shortcomings to this system owing to the fact that it is only a first time proof of concept. These shortcomings could be easily overcome by further characterisation and future revision. Key areas for improvement are listed and described in this section.

The CMOS LED driver is capable of operating at a sample rate of up to 500 MHz while supplying 255 mA, however higher performance could be achieved if the sample rate could be increased further. Comparison with the commercial AWG, which has a sampling rate of 4 Gsps revealed this. It is preferable to generate high frequency clocks using an internal phase locked loop (PLL). This could be implemented in future revisions. The FPGA used to control the CMOS LED driver chip had limited output clock rate, which limited the performance of the VLC demonstrators. The SFDR drop as the sample rate went up is a drawback for modulation schemes such as OFDM which uses adaptive bit loading to improve the achievable data rate. In this work, all data generation and processing were done off-line and thereby no live VLC link was demonstrated. A live VLC link would require further development of the characterisation platform, FPGA firmware and PC software which would have consumed more time and was not in the scope of this work. Even though the FPGA board has external memory, only the internal memory of the FPGA was used which limited the number of samples that could be transmitted during

an experiment. Compilation of the FPGA firmware consumed a considerable amount of time while performing experiments since the firmware had to embed the data to be transmitted as well. A variant of the firmware with the ability to access external memory and transfer of data to the memory without the need for recompilation for each measurement is under development. Due to time constraints, we were unable to characterise the device beyond its limits (output current and sample rate), which might have revealed more information regarding the current DAC based LED drive scheme. Even though we were able to characterise the CCT with respect to QAM levels and bias currents, a more detailed study is required to fully characterise the LED driver within a lighting system. The total power consumption of the CMOS LED driver chip was not considered for power efficiency calculations since the design of the digital logic and biasing circuitry are not optimised for power consumption, therefore a de-rating factor is included in the power efficiency figures. For a commercial incarnation of the CMOS LED driver this would have to be done. The matching of individual channels in the CMOS LED driver was not quantified due to time constraints, quantifying this could be a key to understanding and isolating the BER mismatch between channels observed during experiments.

The DLC system presented in this work was characterised at a fixed link distance of 5 cm. It is desirable to characterise this system at different link distance. Increasing the number of μLEDs in the DLC system is also desirable to increase the resolution and modulation index. The differential optical drive proof of concept demonstrator was realised using two blue LEDs. This is not an ideal implementation. A more practical way to do this is to use two different colour LEDs and associated colour filters at the receiver.

7.3 Future Work

Work done as part of this thesis could spawn new research areas to explore from the possibility of circuit integration for VLC. We have demonstrated circuit miniaturisation is feasible using CMOS technology for VLC transmitters. It is possible to port the 180 nm CMOS technology based design to more modern process nodes (For example, 65 nm or 40 nm). This should reduce the circuit area further, however the initial cost for the ported prototype will be higher since development in newer CMOS process nodes is expensive. The core of the transmitter hardware system presented in this work includes two main components, the CMOS LED driver designed as part of this thesis and an FPGA used to control and feed data to the driver. The CMOS LED driver has the minimal amount of digital logic in the chip required for signal routing. The rest of the digital functions and signal processing are done in the FPGA and PC. It is possible to incorporate more computational and signal processing functions into the CMOS LED driver chip to reduce the footprint of the VLC transmitter system further, making it more suitable for portable electronics. This is a promising research direction considering that, in the near future,

Li-Fi compatibility will be required to overcome the spectrum crunch.

Even though an open drain current DAC architecture is implemented, the number of LEDs that can be connected in series to the load branch of the DAC is limited by the maximum voltage tolerance of the transistors in the drive stage (a limitation of the low voltage CMOS technology used). It is desirable to have LEDs in strings (and many such strings in parallel) so that all the LEDs in the string generate similar levels of light. It is possible to use high voltage CMOS technologies to increase the voltage safety limits and thereby more LEDs in the same branch. This is an interesting research direction for VLC enabled lighting infrastructure.

In this work a differential optical drive scheme using a current DAC was proposed. Compared to the single ended scheme, this method increases the average optical power generated by the current DAC based driver (thereby increasing the electrical to optical energy conversion efficiency). Advanced variants of the differential optical scheme supporting multiple channels (WDM/MIMO) can be studied.

7.4 Concluding Remarks

This work has demonstrated that it is possible to use a current steering DAC with high current output to drive LEDs in a VLC transmitter at high data rates maintaining high power efficiency. This method has nullified the need for power amplification output stages which are not power efficient. The three aims initially set for this work namely circuit miniaturisation, power efficient drive whilst at high sample rate and high current output are realised. This research has opened up an alternate integrated drive scheme for VLC to the voltage regulator based integrated low speed drivers reported in literature. This research could lay the path for an integrated VLC transceiver chip. This would be an integral part of any VLC enabled system in the future and could make VLC systems compact, energy efficient, cost effective and ubiquitous.

Chapter A

A.1 Chip pinout

Driver chip pin list

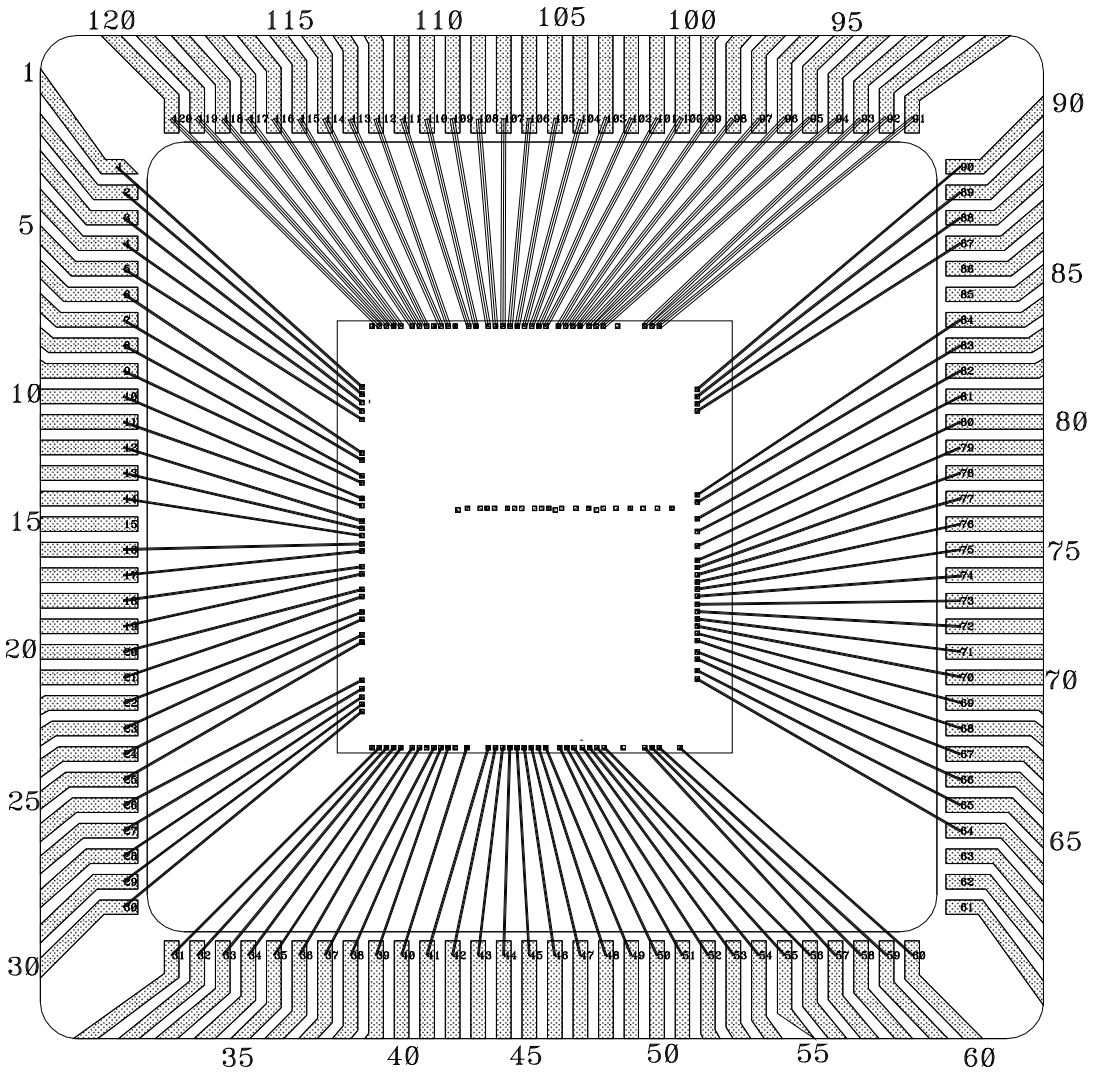
Package → CPGA120 (Ceramic Pin Grid Array 120)
*CPGA package pins (on the table below)
*CPGA package diagram shown after the table

Die - Pin number	Pin Name	Function	Domain	Package Side	CPGA120 pin numbers	Old number
61	Not connected			RIGHT	L11	C3
62	Not connected				M12	B2
63	Not connected				M13	B1
64	GND_ANA	Analog ground	Analog		K11	D3
65	VDD_5P0_ANA_BOT	5V Power (Bottom)	Analog		L12	C2
66	VDD_1P8_ANA	1.8V Power	Analog		L13	C1
67	GND_ANA	Analog ground	Analog		K12	D2
68	RST_N	Active low chip reset	Digital		J11	E3
69	SHIFT_REG_DATA	Data input for shift register	Digital		K13	D1
70	GND_DIG	Digital Ground	Digital		J12	E2
71	GND_DIG	Digital Ground	Digital		J13	E1
72	VDD_1P8_DIG	1.8V Power	Digital		H11	F3
73	VDD_1P8_DIG	1.8V Power	Digital		H12	F2
74	VDD_1P8_DIG	1.8V Power	Digital		H13	F1
75	VDD_1P8_DIG	1.8V Power	Digital		G12	G2
76	GND_DIG	Digital Ground	Digital		G11	G3
77	SHIFT_REG_CLK	Low speed clock input for shift register	Digital		G13	G1
78	SHIFT_REG_LATCH	Latch input for shift register	Digital		F13	H1
79	GND_DIG	Digital Ground	Digital		F12	H2
80	SHIFT_REG_LAT_OP	Shift register latch output	Digital		F11	H3
81	LVDS_B0_OP	LVDS Bit 0 output	Digital		E13	J1
82	DEBUG_EN	Debug Enable	Digital		E12	J2
83	SEG_LED_VDD	Segmented LED anode node	Analog		D13	K1
84	SEG_LED_VDD	Segmented LED anode node	Analog		E11	J3
85	Not connected				D12	K2
86	Not connected				C13	L1
87	VDD_1P8_ANA	1.8V Power	Analog		B13	M1
88	VDD_1P8_ANA	1.8V Power	Analog		D11	K3
89	GND_ANA	Analog ground	Analog		C12	L2
90	GND_ANA	Analog ground	Analog		A13	N1
91	GND_ANA	Analog ground	Analog	Top	C11	L3
92	GND_ANA	Analog ground	Analog		B12	M2
93	GND_ANA	Analog ground	Analog		A12	N2
94	DAC2_LED_CATHODE	DAC2 LED cathode node	Analog		C10	L4

95	DAC2_LED_CATHODE	DAC2 LED cathode node	Analog		B11	M3
96	DAC2_LED_CATHODE	DAC2 LED cathode node	Analog		A11	N3
97	VDD_5P0_ANA_TOP	5V power (Top)	Analog		B10	M4
98	DAC2_DUMMY	DAC2 dummy node	Analog		C9	L5
99	DAC2_DUMMY	DAC2 dummy node	Analog		A10	N4
100	DAC2_DUMMY	DAC2 dummy node	Analog		B9	M5
101	DAC1_LED_CATHODE	DAC1 LED cathode node	Analog		A9	N5
102	DAC1_LED_CATHODE	DAC1 LED cathode node	Analog		C8	L6
103	DAC1_LED_CATHODE	DAC1 LED cathode node	Analog		B8	M6
104	GND_ANA	Analog ground	Analog		A8	N6
105	DAC1_DUMMY	DAC1 dummy node	Analog		B7	M7
106	DAC1_DUMMY	DAC1 dummy node	Analog		C7	L7
107	DAC1_DUMMY	DAC1 dummy node	Analog		A7	N7
108	GND_ANA	Analog ground	Analog		A6	N8
109	GND_ANA	Analog ground	Analog		B6	M8
110	DCO_CASC_BIAS	DC Offset DAC cascade BIAS	Analog		C6	L8
111	DCO_CS_BIAS	DC Offset DAC current source BIAS	Analog		A5	N9
112	GND_ANA	Analog ground	Analog		B5	M9
113	GND_ANA	Analog ground	Analog		A4	N10
114	VDD_1P8_ANA	1.8V Power	Analog		C5	L9
115	VDD_1P8_ANA	1.8V Power	Analog		B4	M10
116	VDD_1P8_ANA	1.8V Power	Analog		A3	N11
117	LVDS_DACEN1_P	DAC1 Enable (LVDS P)	Analog		A2	N12
118	LVDS_DACEN1_N	DAC1 Enable (LVDS N)	Analog		C4	L10
119	LVDS_DACEN2_N	DAC2 Enable (LVDS N)	Analog		B3	M11
120	LVDS_DACEN2_P	DAC2 Enable (LVDS P)	Analog		A1	N13
1	GND_ANA	Analog ground	Analog	**Left**	C3	L11
2	GND_ANA	Analog ground	Analog		B2	M12
3	VDD_5P0_ANA_LEFT	5V Power (Left)	Analog		B1	M13
4	VDD_5P0_ANA_LEFT	5V Power (Left)	Analog		D3	K11
5	VDD_5P0_ANA_LEFT	5V Power (Left)	Analog		C2	L12
6	LVDS6_P	Data bit 6 (LVDS P)	Analog		C1	L13
7	LVDS6_N	Data bit 6 (LVDS N)	Analog		D2	K12
8	LVDS4_P	Data bit 4 (LVDS P)	Analog		E3	J11
9	LVDS4_N	Data bit 4 (LVDS N)	Analog		D1	K13
10	LVDS2_P	Data bit 2 (LVDS P)	Analog		E2	J12
11	LVDS2_N	Data bit 2 (LVDS N)	Analog		E1	J13
12	LVDS0_P	Data bit 0 (LVDS P)	Analog		F3	H11
13	LVDS0_N	Data bit 0 (LVDS N)	Analog		F2	H12
14	LVDS_BIAS_RES	Bias resistor for LVDS receiver	Analog		F1	H13
15	Not connected				G2	G12
16	LVDS_CLK_P	High speed clock (LVDS P)	Analog		G3	G11
17	LVDS_CLK_N	High speed clock (LVDS N)	Analog		G1	G13
18	LVDS1_P	Data bit 1 (LVDS P)	Analog		H1	F13
19	LVDS1_N	Data bit 1 (LVDS N)	Analog		H2	F12

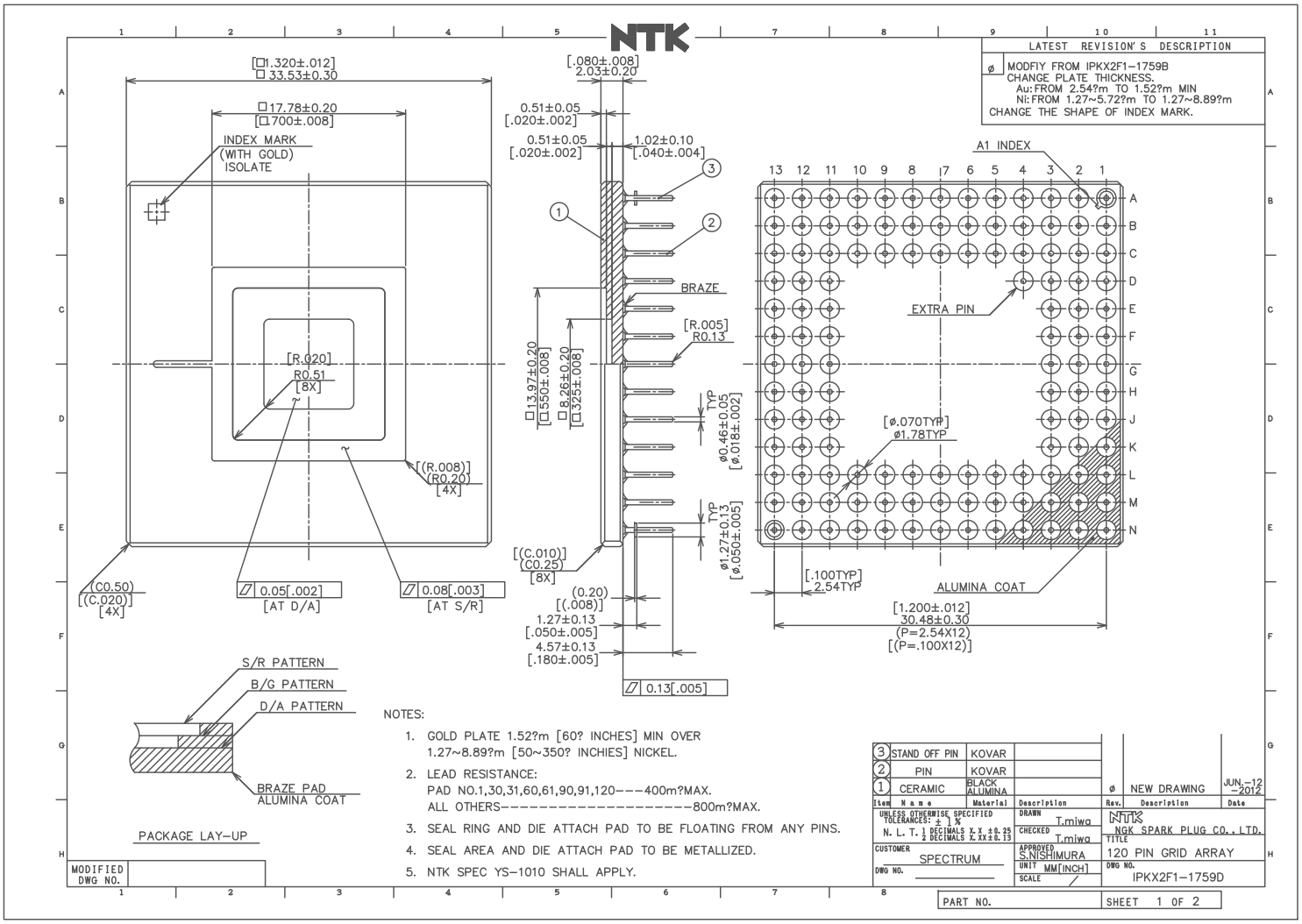
20	LVDS3_P	Data bit 3 (LVDS P)	Analog		H3	F11
21	LVDS3_N	Data bit 3 (LVDS N)	Analog		J1	E13
22	LVDS5_P	Data bit 5 (LVDS P)	Analog		J2	E12
23	LVDS5_N	Data bit 5 (LVDS N)	Analog		K1	D13
24	LVDS7_P	Data bit 7 (LVDS P)	Analog		J3	E11
25	LVDS7_N	Data bit 7 (LVDS N)	Analog		K2	D12
26	VDD_5P0_ANA_LEFT	5V Power (Left)	Analog		L1	C13
27	VDD_5P0_ANA_LEFT	5V Power (Left)	Analog		M1	B13
28	VDD_5P0_ANA_LEFT	5V Power (Left)	Analog		K3	D11
29	GND_ANA	Analog ground	Analog		L2	C12
30	GND_ANA	Analog ground	Analog		N1	A13
31	LVDS_DACEN3_N	DAC3 Enable (LVDS N)	Analog	**Bottom**	L3	C11
32	LVDS_DACEN3_P	DAC3 Enable (LVDS P)	Analog		M2	B12
33	LVDS_DACEN4_N	DAC4 Enable (LVDS N)	Analog		N2	A12
34	LVDS_DACEN4_P	DAC4 Enable (LVDS P)	Analog		L4	C10
35	VDD_1P8_ANA	1.8V Power	Analog		M3	B11
36	VDD_1P8_ANA	1.8V Power	Analog		N3	A11
37	GND_ANA	Analog ground	Analog		M4	B10
38	GND_ANA	Analog ground	Analog		L5	C9
39	GND_ANA	Analog ground	Analog		N4	A10
40	DAC_CS_BIAS	DAC current source bias resistor	Analog		M5	B9
41	GND_ANA	Analog ground	Analog		N5	A9
42	GND_ANA	Analog ground	Analog		L6	C8
43	DAC4_DUMMY	DAC4 dummy node	Analog		M6	B8
44	DAC4_DUMMY	DAC4 dummy node	Analog		N6	A8
45	DAC4_DUMMY	DAC4 dummy node	Analog		M7	B7
46	GND_ANA	Analog ground	Analog		L7	C7
47	DAC4_LED_CATHODE	DAC4 LED cathode node	Analog		N7	A7
48	DAC4_LED_CATHODE	DAC4 LED cathode node	Analog		N8	A6
49	DAC4_LED_CATHODE	DAC4 LED cathode node	Analog		M8	B6
50	DAC3_DUMMY	DAC3 dummy node	Analog		L8	C6
51	DAC3_DUMMY	DAC3 dummy node	Analog		N9	A5
52	DAC3_DUMMY	DAC3 dummy node	Analog		M9	B5
53	VDD_5P0_ANA_BOT	5V Power (Bottom)	Analog		N10	A4
54	DAC3_LED_CATHODE	DAC3 LED cathode node	Analog		L9	C5
55	DAC3_LED_CATHODE	DAC3 LED cathode node	Analog		M10	B4
56	DAC3_LED_CATHODE	DAC3 LED cathode node	Analog		N11	A3
57	GND_ANA	Analog ground	Analog		N12	A2
58	GND_ANA	Analog ground	Analog		L10	C4
59	GND_ANA	Analog ground	Analog		M11	B3
60	DAC_CASC_BIAS	Cascode bias resistor connection	Analog		N13	A1

A.2 Chip bonding diagram and packaging



A) DEVICE-,DRAWING NUMBER:			
B) ASSEMBLY CODE: NMA-X		C) SCALE: 10 / 1	
D) DIE SIZE:		E) DIE ATTACH PAD SIZE: 433X433 mil	
F) PACKAGE TYPE/BODY SIZE: CERAMIC PGA 120 LD / (33.52 mm)			
G) BONDPAD PITCH (MIN):		H) BOND PAD SIZE (MIN):	
I) WIRE SIZE:		J) WAFERTHICKNESS:	
K) CAVITY (UP OR DOWN): UP			
L) REMARKS:	QA - APPROVAL:	REV.:	
		SHEET OF	

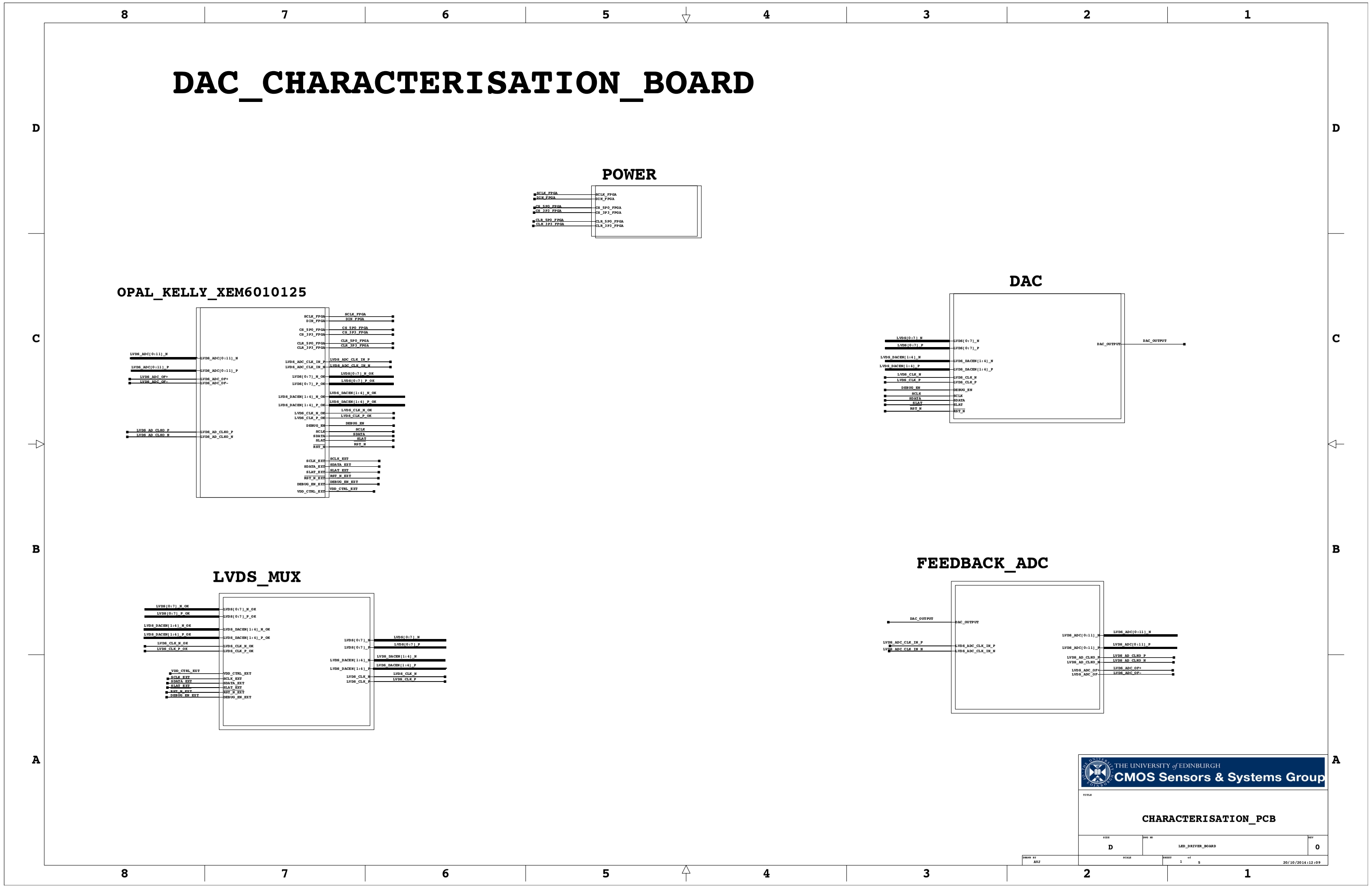
SSM P/N: CPG12034

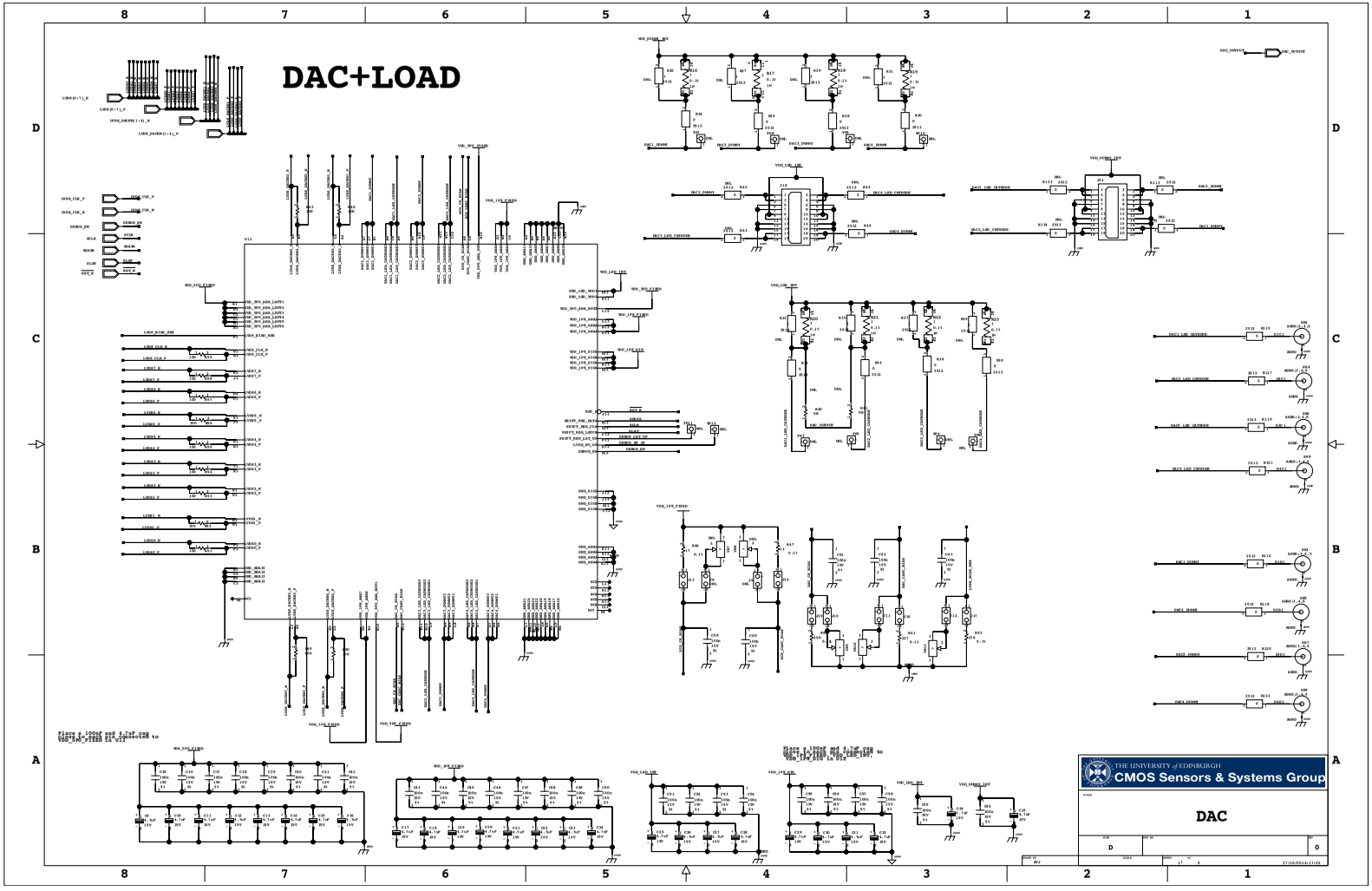


SPECTRUM SEMICONDUCTOR MATERIALS, INC.

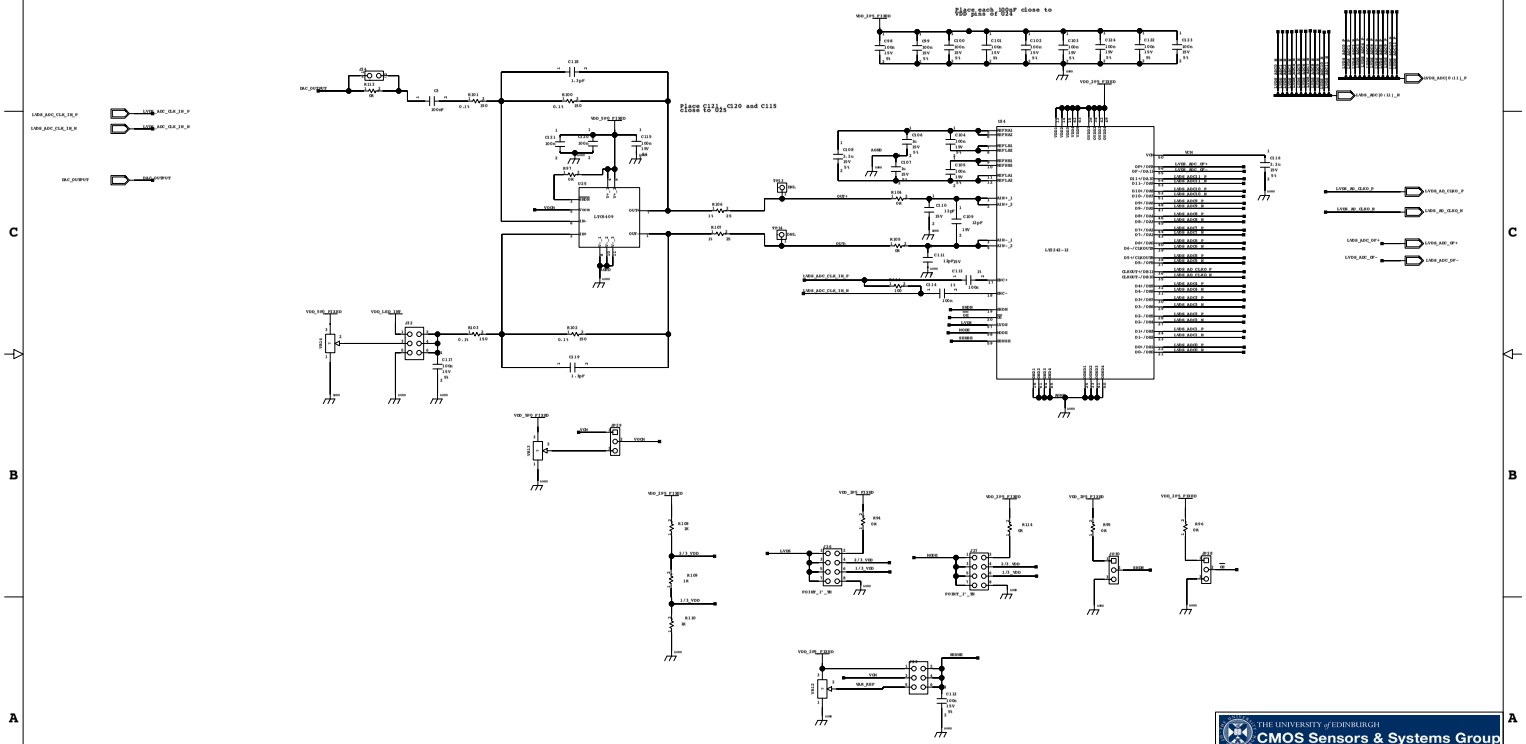
www.spectrum-semi.com Ph: (408) 435-5555 Fx: (408) 435-8226

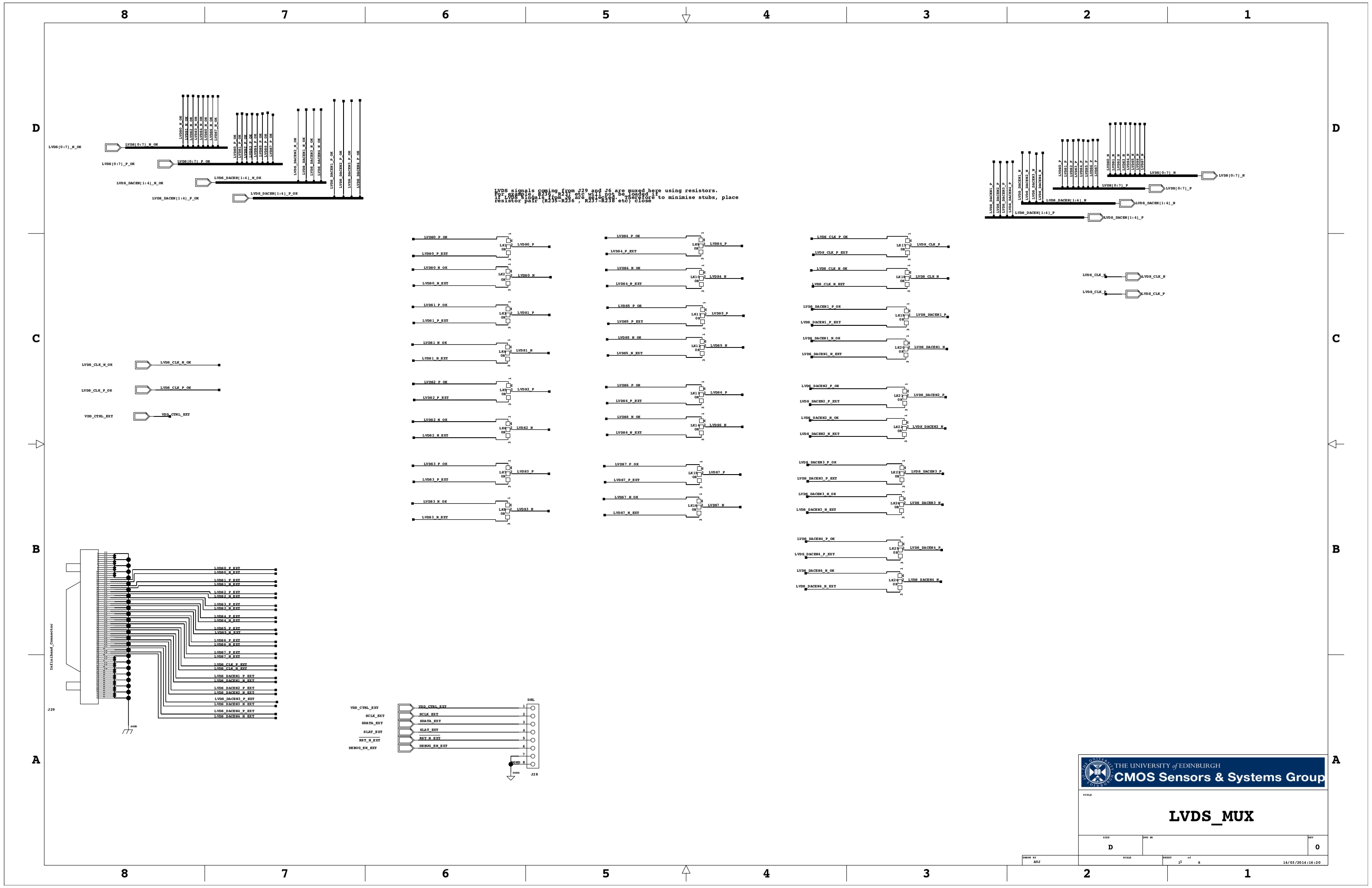
A.3 Mother board (MB) Schematics


DAC_CHARACTERISATION_BOARD
POWER
OPAL_KELLY_XEM6010125
DAC
LVDS_MUX
FEEDBACK_ADC
THE UNIVERSITY of EDINBURGH
CMOS Sensors & Systems Group
CHARACTERISATION_PCB
LED_DRIVER_BOARD
20/10/2014:12:09


DAC+LOAD
THE UNIVERSITY of EDINBURGH
CMOS Sensors & Systems Group
DAC
D
0

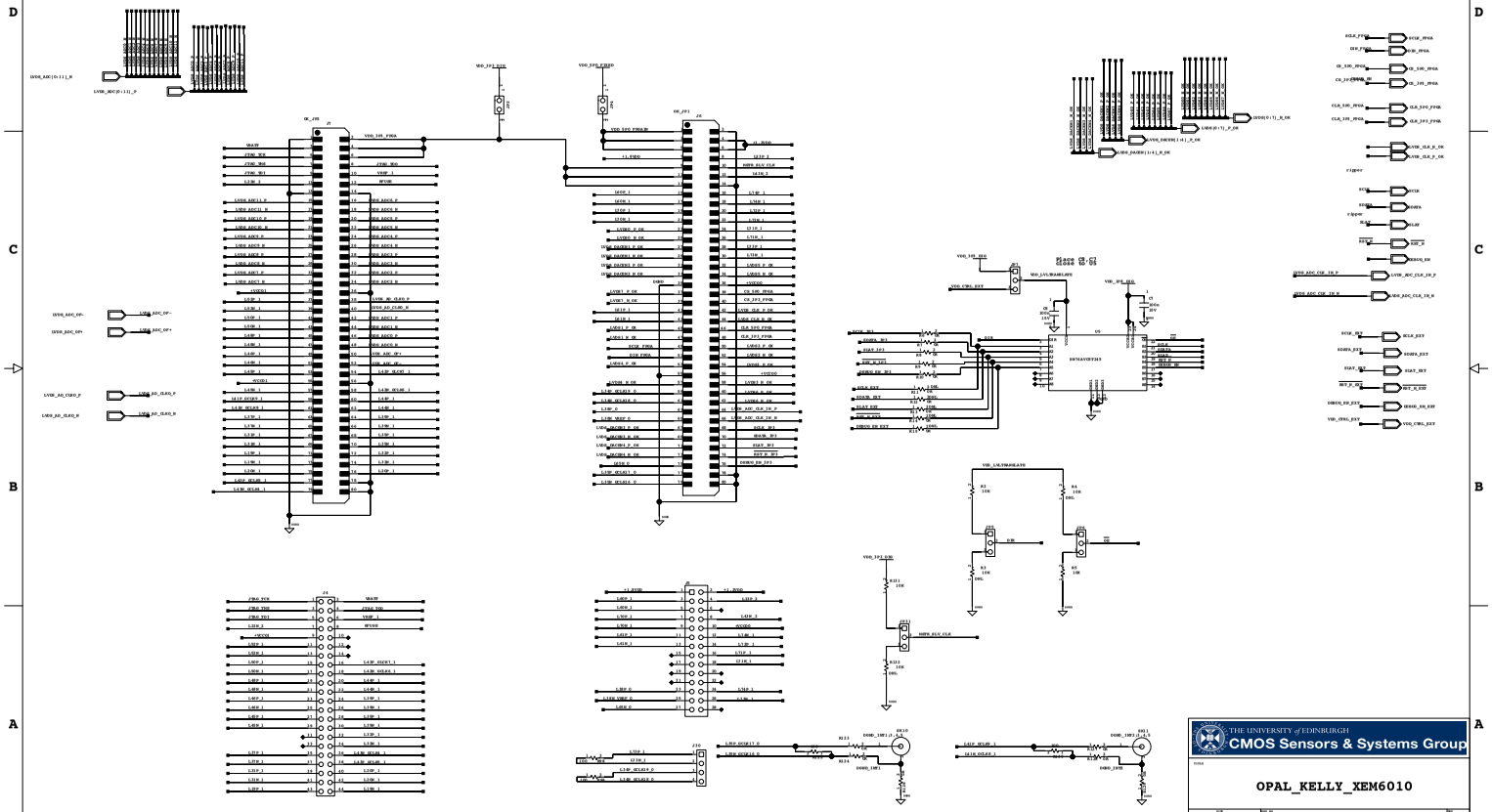
FEEDBACK_ADC





LVDS signals coming from J29 and J6 are muxed here using resistors.
For example, R236, R237 etc will not be loaded if
if LVDS singals from J6 are selected. Therefore to minimise stubs, place
resistor pair (R235-R236 , R237-R238 etc) close
THE UNIVERSITY of EDINBURGH
CMOS Sensors & Systems Group
LVDS_MUX

OPAL_KELLY_FPGA_CONNECTORS



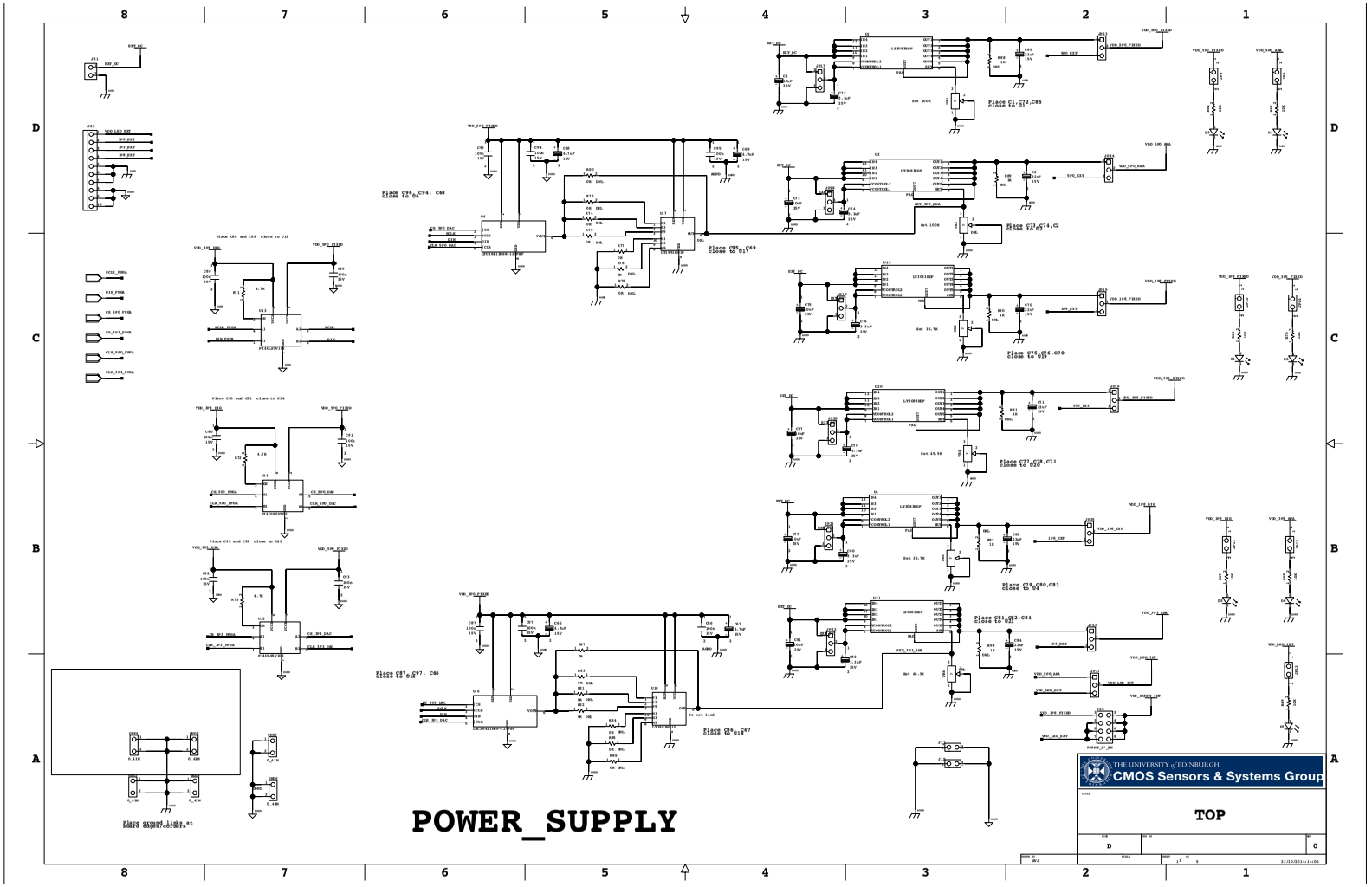
THE UNIVERSITY of EDINBURGH
CMOS Sensors & Systems Group

OPAL_KELLY_XEM6010

SIZE	DWG NO	REV
D	1	0

SHEET	OF
1	1

22/10/2014 10:49


POWER_SUPPLY
THE UNIVERSITY of EDINBURGH
CMOS Sensors & Systems Group
TOP
D
0
22/10/2014 14:08

A.4 Python program

```
#System Libraries
import imp
from struct import unpack
from platform import system
from csv import reader
import time

if 'okBoard' in locals():
    del okBoard

#Register file and FPGA bit file
register_file = 'OpalKelly_Register.csv'
bit_file = 'FPGA.bit'

#Programming the FPGA
if system() == 'Darwin':
    ok = imp.load_source('ok', 'OpalKelly.py')
else:
    raise Exception('OS not recognised')
okBoard = ok.OpalKelly(bit_file, register_file)


#FPGA logic activation and CMOS DAC RESET
okBoard.set_register('ACTIVATE_DAC',1)
okBoard.set_trigger('SYS_RESET')

#DAC CONFIGURATION
okBoard.set_register('DRIVER_DAC_CS',8)
okBoard.set_register('GANG_MIMO',0)
okBoard.set_register('DAC_SEL',3)
okBoard.set_register('DAC1_DC_OFFSET0',0)
okBoard.set_register('DAC2_DC_OFFSET0',0)
okBoard.set_register('DAC3_DC_OFFSET0',0)
okBoard.set_register('DAC4_DC_OFFSET0',0)
okBoard.set_register('DAC1_BIAS',0)
okBoard.set_register('DAC2_BIAS',0)
okBoard.set_register('DAC3_BIAS',0)
okBoard.set_register('DAC4_BIAS',0)
okBoard.set_register('DAC5_BIAS',15)
okBoard.set_register('DEM_EN',0)
okBoard.set_register('CLK_SEL',0)
okBoard.set_trigger('CONFIGURE_SHIFT_REG')

#Internal data source selection for CMOS DAC
okBoard.set_register('SUSTAIN_SINE',1)
okBoard.set_register('SUSTAIN_TRIANGLE',0)
okBoard.set_register('SUSTAIN_SQUARE',0)
okBoard.set_register('SUSTAIN_RAMP',0)

#Start data streaming to CMOS DAC
okBoard.set_trigger('START_DRIVE')
```

Figure A.1: Python code to control OK

A.5 DNL from all channels

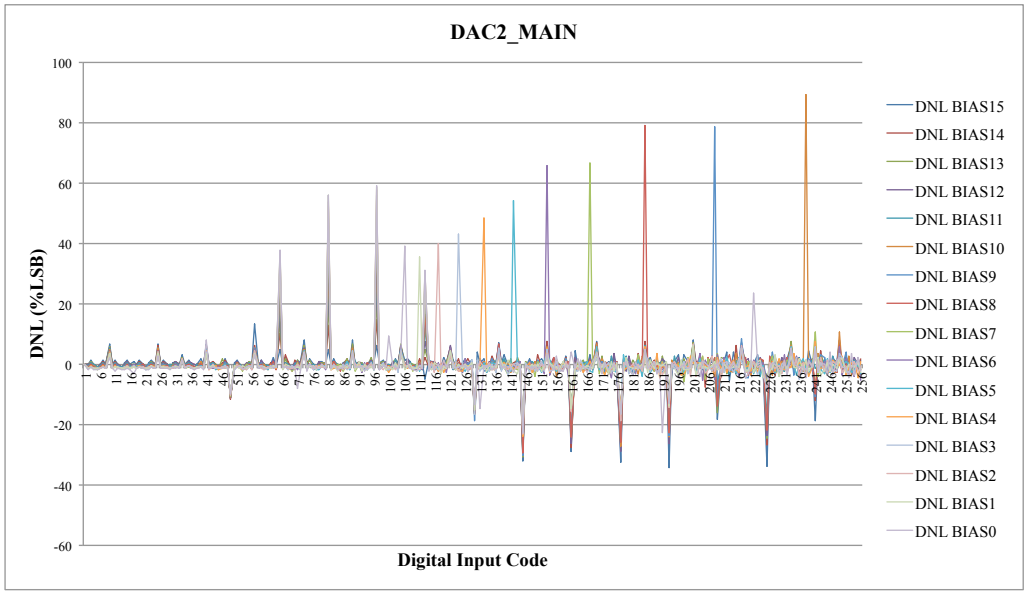


Figure A.2: DNL measurements at various currents of main branch in DAC 2

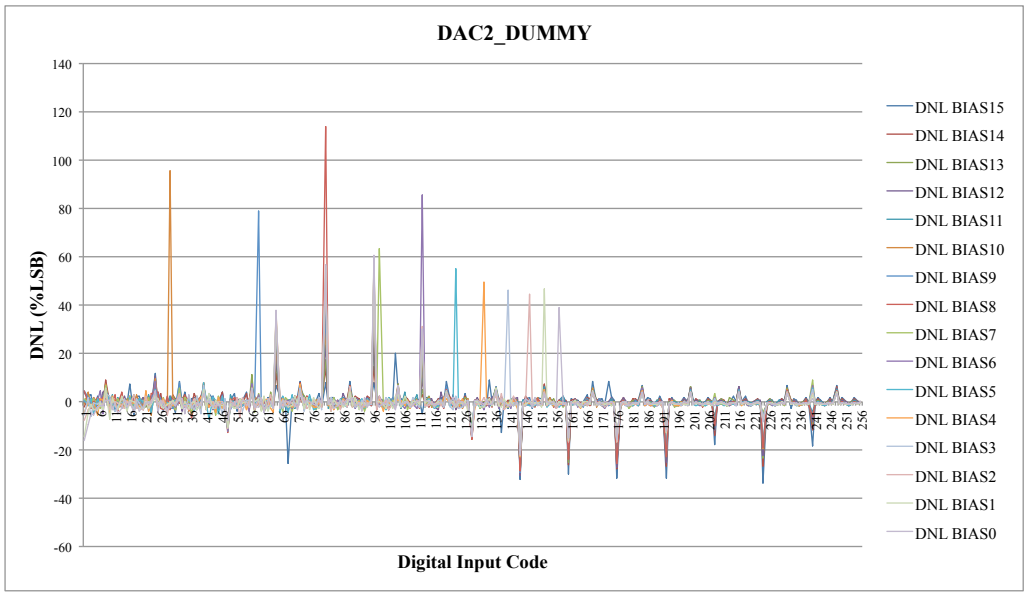


Figure A.3: DNL measurements at various currents of dummy branch in DAC 2

A.6 INL from all channels

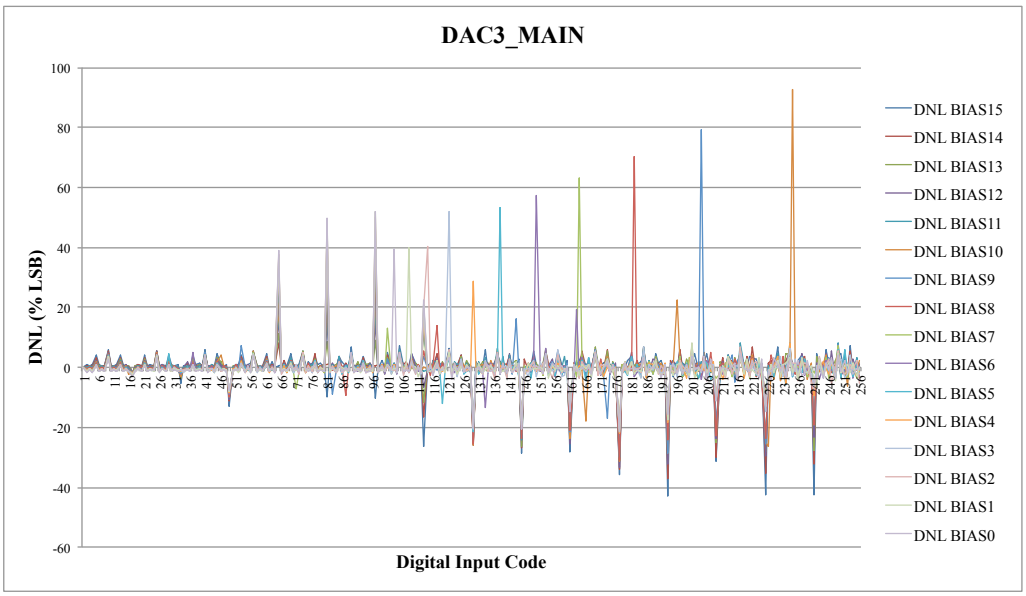


Figure A.4: DNL measurements at various currents of main branch in DAC 3

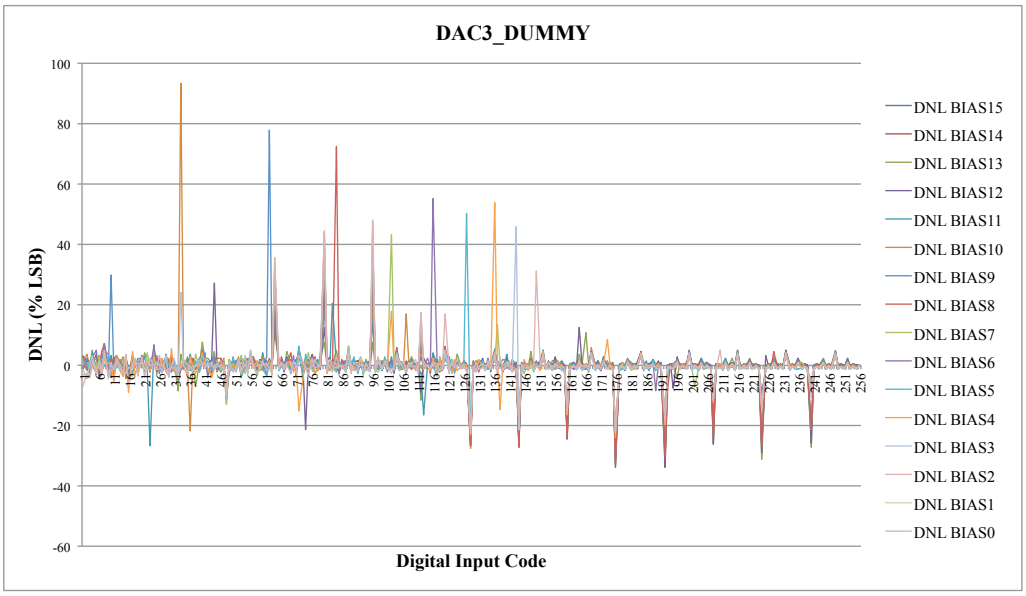


Figure A.5: DNL measurements at various currents of dummy branch in DAC 3

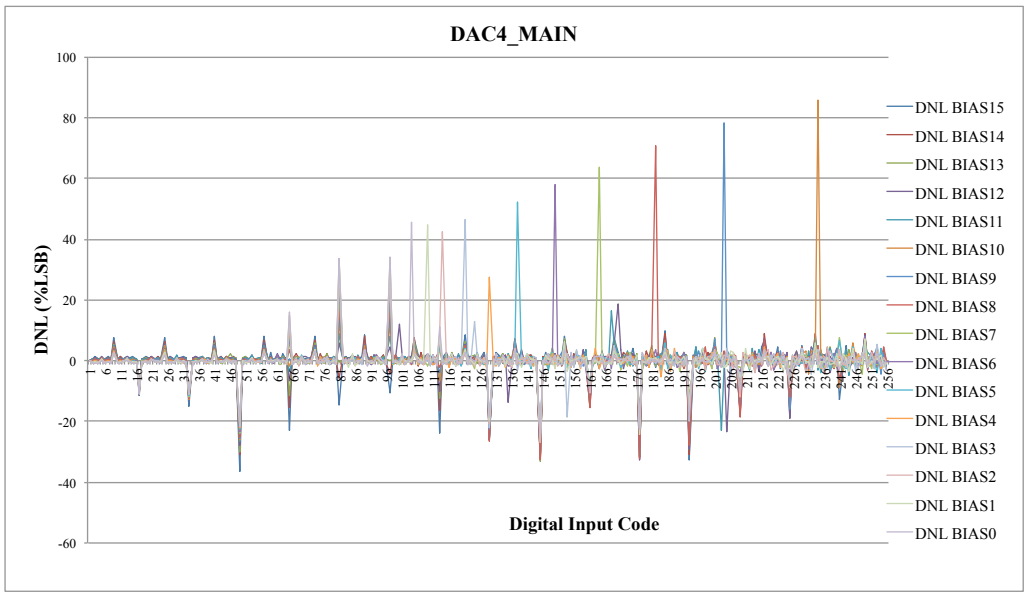


Figure A.6: DNL measurements at various currents of main branch in DAC 4

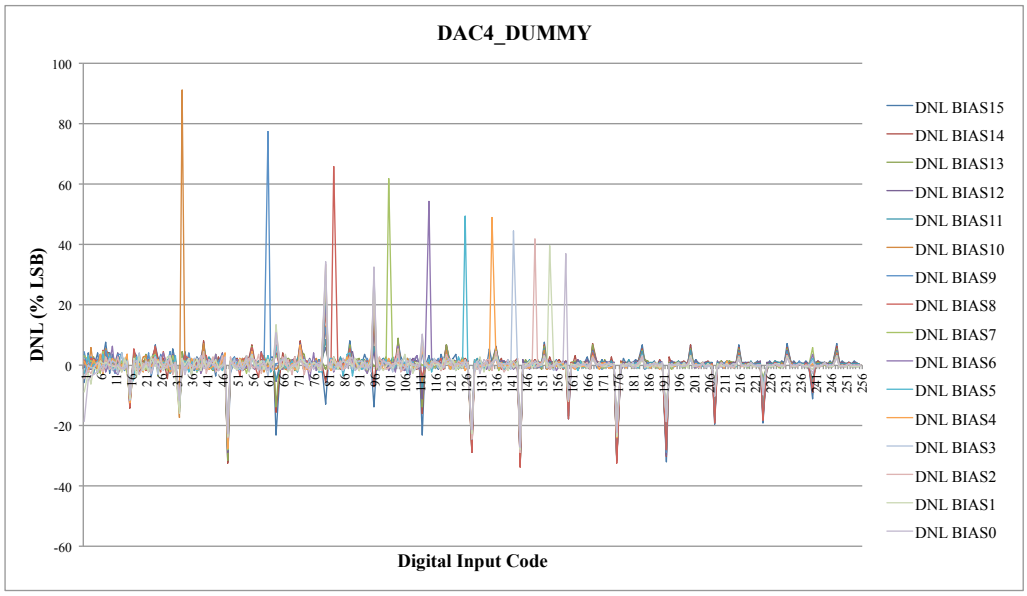


Figure A.7: DNL measurements at various currents of dummy branch in DAC 4

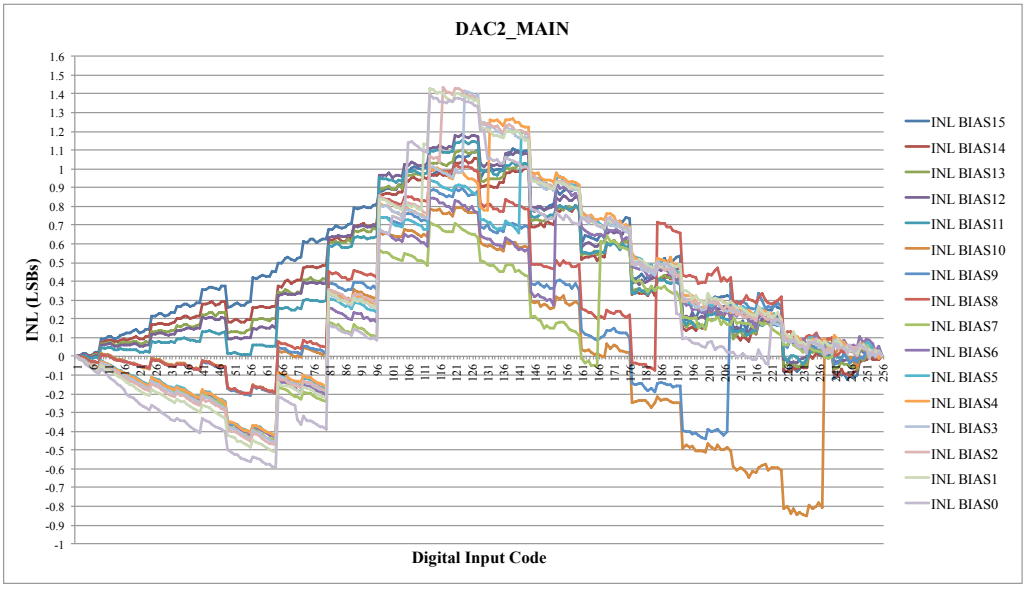


Figure A.8: INL measurements at various currents of main branch in DAC 2

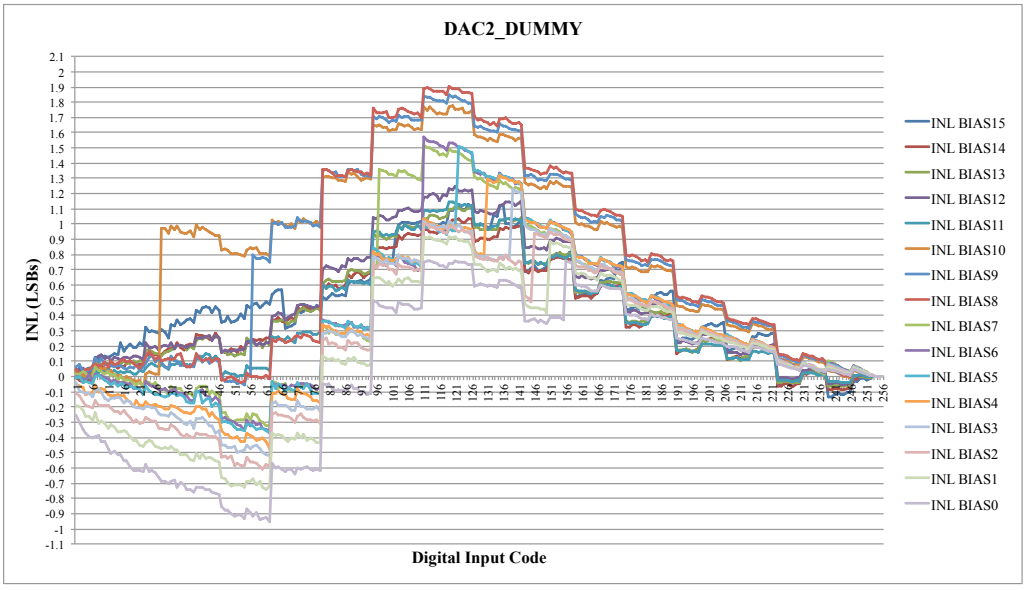


Figure A.9: INL measurements at various currents of dummy branch in DAC 2

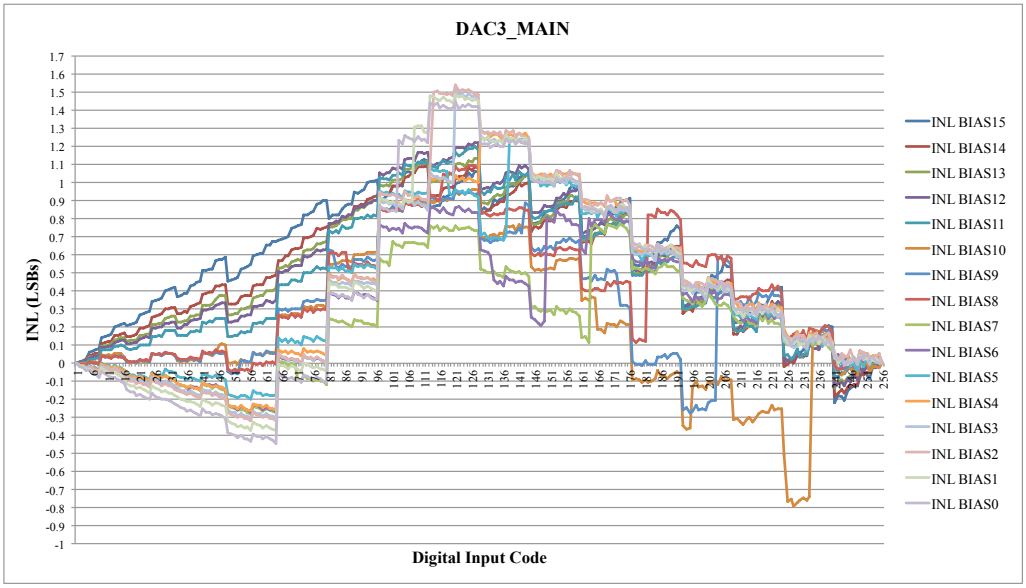


Figure A.10: INL measurements at various currents of main branch in DAC 3

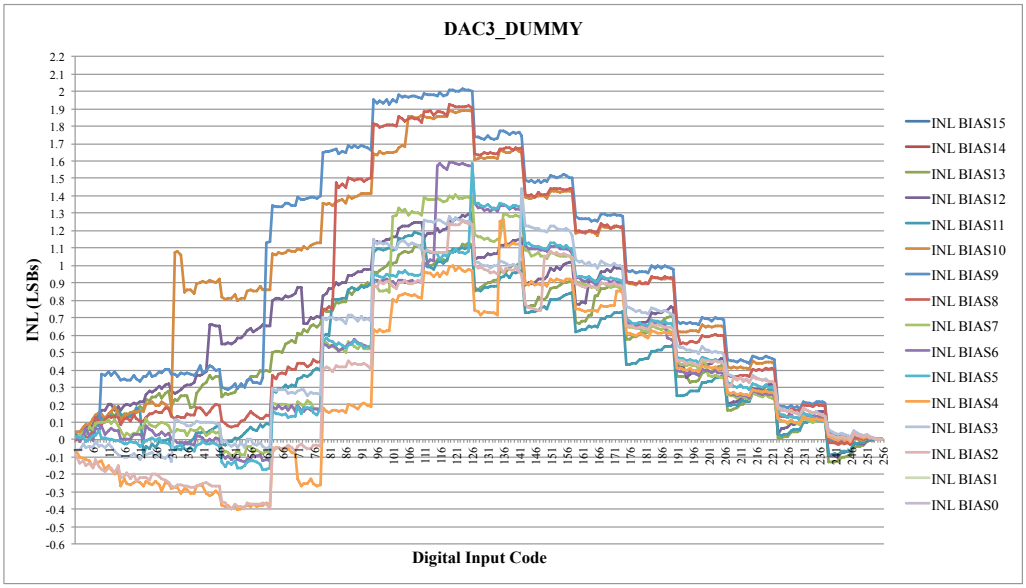


Figure A.11: INL measurements at various currents of dummy branch in DAC 3

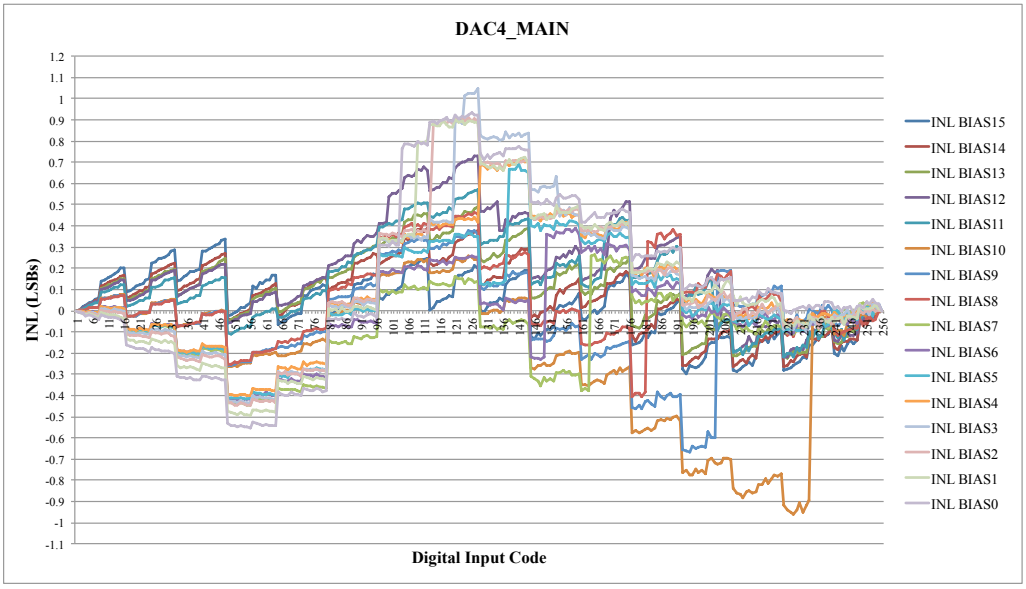


Figure A.12: INL measurements at various currents of main branch in DAC 4

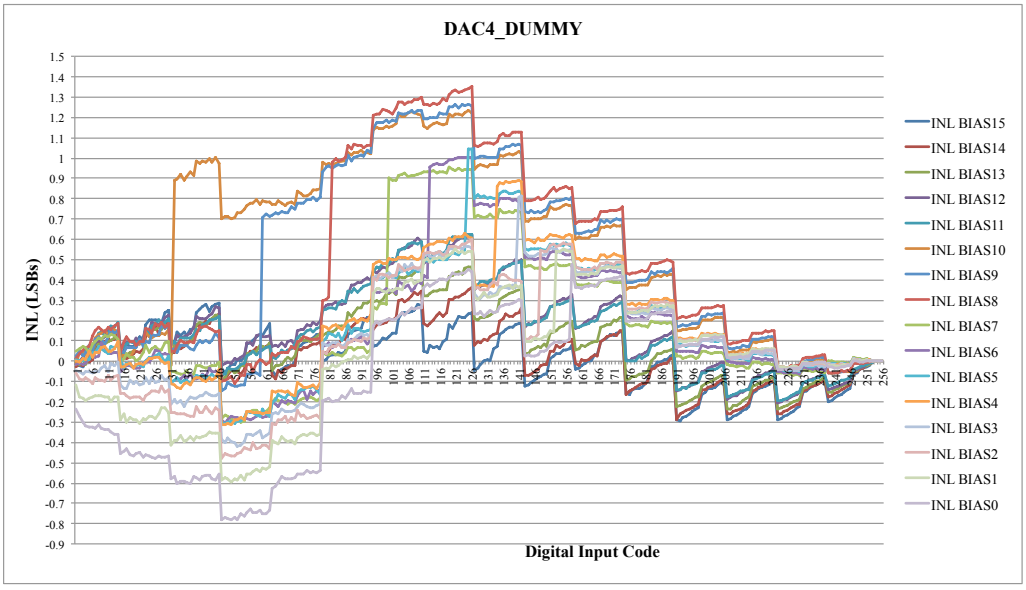


Figure A.13: INL measurements at various currents of dummy branch in DAC 4

Chapter B

B.1 Publications

A.V.N. Jalajakumari et al. “An energy efficient high-speed digital LED driver for visible light communications”. In: *Communications (ICC), 2015 IEEE International Conference on*. June 2015, pp. 5054–5059. DOI: 10.1109/ICC.2015.7249125

A. V. N. Jalajakumari et al. “High-Speed Integrated Digital to Light Converter for Short Range Visible Light Communication”. In: *IEEE Photonics Technology Letters* 29.1 (Jan. 2017), pp. 118–121. ISSN: 1041-1135. DOI: 10.1109/LPT.2016.2624281

An Energy Efficient High-speed Digital LED Driver for Visible Light Communications

Aravind V. N. Jalajakumari, Katherine Cameron, Robert Henderson
Institute for Integrated Micro and Nano Systems
The University of Edinburgh
Edinburgh, UK, EH9 3JL
{a.venugopalan, k.cameron, robert.henderson}@ed.ac.uk}

Dobroslav Tsonev, Harald Haas
Li-Fi Research and Development Centre, Institute for Digital Communications,
The University of Edinburgh
Edinburgh, UK, EH9 3JL
{d.tsonev, h.haas}@ed.ac.uk}

***Abstract*—In this paper an energy efficient light emitting diode (LED) driver circuit for visible light communications (VLC) and results from the electrical and optical characterization are presented. A current steering digital to analogue converter (DAC) based LED driver circuit supporting 4-channels with an 8-bit resolution is realized in a 0.18 µm complimentary metal oxide semiconductor (CMOS) technology. Each channel delivers a full-scale current of 255 mA and achieves up to 67% electrical efficiency when driving 250 MS/s orthogonal frequency division multiplexing (OFDM) signals. Optical differential drive capability is demonstrated by using two output branches of a single channel to drive two different LEDs with an SNR improvement (>5 dB). The chip is also capable of full digital control of color shift keying (CSK) using multi-color LEDs enabling lighting color-temperature adjustment, dimming and multiple-input and multiple-output (MIMO) optical communications and these aspects will be the subject of future research.**

***Keywords —CMOS LED driver, digital to analogue converter,* visible light communications, OFDM**

I. INTRODUCTION

Use of light emitting diodes (LEDs) for simultaneous lighting and data transmission has the potential to supplement conventional radio frequency (RF) communication and to enable new wireless access technologies. The inherent advantages of the visible light spectrum over the RF spectrum are: license-free spectrum availability, energy efficiency, security and safety [1]. Optical links have been demonstrated at data rates up to 1 Gb/s using a single phosphor-coated LED [2], and ~3 Gb/s using a single high bandwidth µ-LED [3] or red-green-blue LEDs [4]. The low modulation bandwidth of commercial white LEDs (around 20 MHz) requires spectrally efficient modulation techniques, such as orthogonal frequency division multiplexing (OFDM) or pulse amplitude modulation (PAM) to be used. OFDM and PAM schemes have been utilized for realizing visible light communication (VLC) systems using discrete off the shelf electronic components [2-4]. Use of discrete components increases the overall system footprint and cost. Component level integration and miniaturization is essential for large-scale implementation of VLC systems. Conventional circuits used to support OFDM or PAM involve a digital to analogue converter (DAC), which can generate complex signal patterns. DAC structures that can deliver up to 30 mA to the load being driven have been reported previously [5] and thus a power amplification stage is required after the DAC in order to drive a typical LED. Fig. 1(a) shows this structure. The non-linear LED output characteristic poses a further challenge to these schemes, requiring pre-distortion or increased modulation complexity to avoid loss of capacity. The high power efficiency of LED lighting is one of its main advantages and so it is critical for VLC LED drivers to preserve this property. This precludes line-driver approaches used in powerline and asymmetric digital subscriber line (ADSL) links consisting of a low-power DAC followed by a class-AB voltage mode driver stage. This is because they provide efficiencies of around 18% at comparable power, crest factor and modulation rates. Class-G or H or self-oscillating designs offer improved efficiency (<50%) [6], but this is less than existing inductor-based lighting LED drivers which have up to 90% efficiency [7].

In this study an open-drain 8-bit current steering DAC based LED driver) is presented. It is similar to [8] but capable of delivering 250 MS/s at a maximum full-scale current of 255 mA and has a power efficiency of 72% (static measurements) A differential optical drive is proposed by employing both current steering branches of the DAC to drive two different color LEDs. This doubles the signal level and efficiency over a single ended approach, and enables the transmitter configuration described in [9]. Fig. 1(b) and 1(c) illustrates the single ended current DAC LED drive and differential drive, respectively. The chip has 4 separate driver channels, where each channel is capable of driving up to 2 LEDs allowing for color shift keying, lighting color-temperature adjustment and multiple-input and multiple-output (MIMO) realizations.

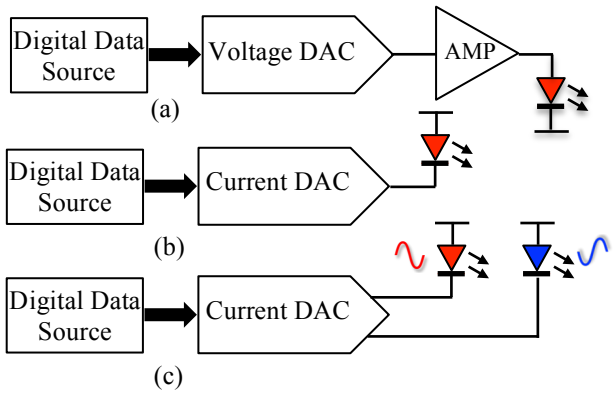


Fig. 1. LED driver concepts for VLC (a) Conventional drive topology; (b) Proposed single ended drive; (c) Proposed differential drive

The rest of the paper is organized as follows. Section II describes the driver circuit and the design involved. Section III presents the experimental setup used to characterize the DAC. Section IV presents the results and Section V gives concluding comments.

II. Integrated Circuit Description

In this section, the design and function of the driver chip is summarized. The driver chip block diagram is shown in Fig. 2. A high-speed clock, 8-bit data and select signals are received through a parallel low voltage differential signaling (LVDS) receiver, similar to [10]. Selector logic can be configured for both high speed ganged mode or MIMO mode. In ganged mode, each driver receives the same data word on every clock edge. In MIMO mode, each driver receives a down sampled, time interleaved data word at a four times lower clock rate. Each channel has its own bias and offset configuration DAC. The bias DAC allows the full-scale current drive of each channel to be varied from 16 mA to 255 mA at a 4-bit resolution. Individual bias configuration enables the drive strength of individual channels to be varied, thereby achieving an overall color-temperature balance of the system. The configurable offset DAC can be used to shift the base operating point of a particular LED to different levels in the current to light transfer characteristic of the LED, thus utilizing the most linear operating regime. Both the bias and the offset DAC functions can be combined to adjust the average light intensity from the LED, realizing a variable dimming function.

Fig. 3 shows the internal circuitry of each DAC. The main differential LED drive DAC is implemented using a 50% segmentation current steering DAC. Incoming 8-bit binary data is split into 4-bit most significant and least significant nibbles. The most significant nibble is decoded into a 15-bit thermometer code. Each bit after buffering and level shifting drives a 16 mA current source. The least significant nibble is delay equalized with the thermometer coded outputs, and is used to drive binary weighted current sources with current strengths 8 mA, 4 mA, 2 mA and 1 mA.

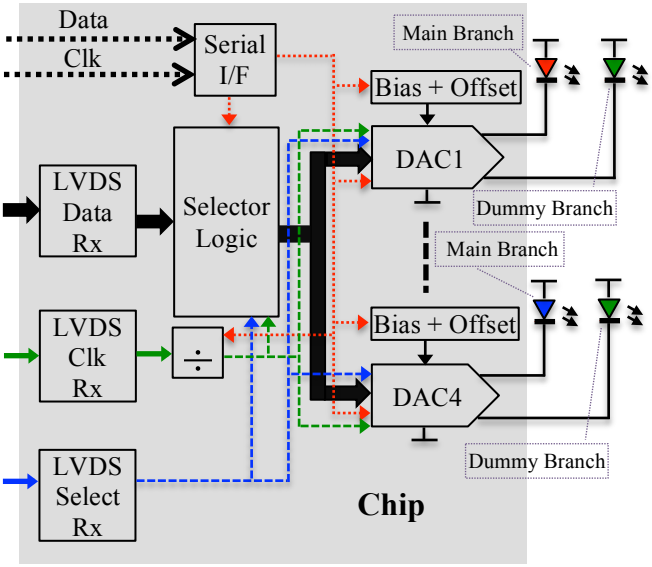


Fig. 2. Block diagram of the driver chip showing internal circuit blocks, data/control path and differential drive.

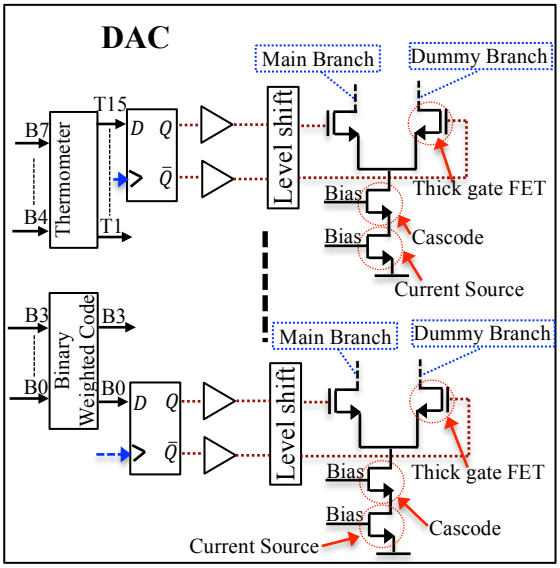
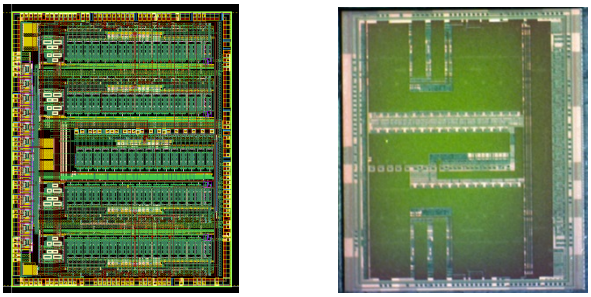


Fig. 3. Internal circuit of a single DAC inside the chip

Each current source has two output branches: a main branch and a dummy branch. For each DAC, the corresponding main branches from the MSB and LSB current sources are connected together. Due to the high current carrying requirement, both the main branch and the dummy branch are connected to multiple bonding pads on the periphery of the chip and bonded out to a ceramic package.

Compared with existing low power designs, the major challenges are the ability to handle very high load currents (up to ~10 times more than what has been reported previously [5]); and the low voltage compliance to ensure power efficiency while operating with a variable voltage LED load. Both thick gate oxide (5 V) and thin gate oxide (1.8 V) transistors are used to realize the unit current source. Thick gate oxide transistors have a maximum drain-source voltage tolerance of 5.5 V, and help absorb voltage variations while driving LEDs at different current levels, thus protecting the thin gate oxide transistors in the current source block.

Current source and cascode transistor sizing has been optimized to ensure low voltage compliance (1.1 V) across them in order to maintain 8-bit matching. A thick top metal layer is used for grounding purposes to reduce the ground path resistance across the chip (0.007 Ω). However due to routing constraints it is not possible to provide low resistance ground connectivity to the 5 MSB current sources. For these current sources, multiple lower metal layers are used to provide a low resistance path, resulting in approximately 0.2 Ω resistance variation across the ground reference between the current source cells. A major challenge during the layout stage was optimizing the ground net layout to minimize the resistance. Similar to the main branch and dummy branch, multiple pads are used to wire out the ground reference net to the ceramic package. Fig. 4(a) shows the finished chip layout. The total area of the micrograph in Fig. 4(b) is 29 mm^2 and the area of packaged chip is 1124 mm^2. The chip was fabricated using ams' 180 nm CMOS technology.



(a) (b)

Fig. 4. (a) Finished chip layout; (b) Chip micrograph (Silicon die)

III. Experimental Setup

There are two parts to the experimental setup, electrical characterization setup and VLC link setup. A custom built printed circuit board (PCB) is used to perform the experiments using the chip. This circuit board has the ability to generate the different supply voltages required for the operation of the driver chip. An off-the-shelf field programmable gate array (FPGA) card (Opal Kelly XEM6310-LX150) is attached to the circuit board, which provides data, sampling clock and chip selects for the driver chip over the LVDS interface and configuration data over the slow speed serial interface. A 100 MHz oscillator on the FPGA board is used to generate multiple sampling clocks for the characterization. Two different clock frequencies were applied to electrical (up to 250 MHz) and optical (up to 40 MHz) measurements. The electrical performance of the chip up to 250 MS/s limited by the FPGA is reported. The designed maximum operating frequency (up to 500 MS/s) of the chip is being evaluated using a higher speed FPGA. Optical measurements were performed at lower clock rates because the LED itself limits the data rate. No increase of data rate was obtained beyond 40 MS/s. Configuration involves internal bias and offset settings for individual DACs in the chip, clock divider setting and mode select (Gang/MIMO) (See Section II). Various current biases for the chip are provided on the PCB with the option to vary them in order to achieve optimum performance. To perform electrical characterization, each DAC in the chip can be loaded with fixed value high power resistors. A daughter card housing different commercial LED modules can be attached to this PCB to perform single ended optical experiments.

A. Electrical Characterisation Setup

Fixed value high power resistors (8.2 Ω, Panasonic - ERJ1TRQF8R2U), are loaded on the output branches of a single DAC to measure its electrical performance. For static measurements, the input and the configuration signals to the DAC are provided from a personal computer (PC) through the Opal Kelly board. For dynamic measurements, the signal pattern to be cycled is loaded into the FPGA memory. The output current generated by the DAC drops a voltage across the load resistors, which is sampled using a digital storage oscilloscope (DSO). The data from the DSO is post-processed using spreadsheets and MATLAB.

B. VLC link setup (Single ended and Differential)

To demonstrate the capability of the driver chip, a VLC link is established using a commercial LED from OSRAM (LD W5SM-4S4T-35) and a photodetector (PD). For single ended measurements, commercial LEDs are mounted on a daughter card, which is connected to the main PCB through board-board connectors. Cathodes of the LEDs are connected to the output of each DAC. Anodes of the LEDs are connected to a DC supply voltage. Data patterns to the DAC are generated in the PC and stored in the FPGA memory. The output current of each DAC varies proportionally to the input code thereby varying the intensity output from the LED. A pair of lenses (Thorlabs ACL4532) is used to collimate the light output of the LED and focus it at the receiver. A P-type Intrinsic N-type photodetector (New Focus 1601) is used to receive the signal, which is sampled by the DSO (Agilent MSO7104B). The distance between the LED and the PD is 1 m for single ended measurements. Post-processing of the data was performed in a similar way as the electrical characterisation. For the optical differential drive experiments, shielded cables were soldered on to the characterization PCB for connecting LEDs to the DAC output branches (main and dummy). The distance between each LED and the corresponding PD is 30 cm in this case. To avoid optical interference, each LED is kept facing away from each other.

IV. Results

The results presented in this paper cover electrical characterization, the VLC link in ganged mode and differential optical drive.

A. Electrical Characterisation Results

The measured electrical performance parameters of the DAC are: differential non-linearity (DNL), integral non-linearity (INL) and spurious free dynamic range (SFDR). The DNL of a DAC can be defined as the variation in analog step size from the ideal least significant bit (LSB). The actual output may differ from the ideal output due to factors such as mismatch between transistors used in the circuit. The INL of a DAC can be defined as the deviation of the DAC characteristics from an ideal straight-line characteristic [11]. Both INL and DNL values are expressed in LSBs. SFDR is defined as the ratio of root mean square (rms) tone amplitude to the rms value of the largest spur present in the band of interest (up to half the sampling rate $F_s/2$ in this case) [12].

Both INL and DNL are static characterizations performed by changing the DAC input from the lowest code (0) to the highest code (255) through the FPGA and by measuring the voltage across the resistive load, which is proportional to the output current of the DAC. Static characterization results show ±0.4 LSB INL and +0.6/-0.2 LSB DNL up to a full-scale current of 176 mA. For the highest full-scale current of 255 mA, INL of +0.8/-0.5 and DNL of +0.4/-0.2 are measured. Beyond 200 mA, an INL reduction is observed; this is related to the difference in ground level experienced by the current sources due to resistive drops in the ground path when large currents are flowing. Fig. 5 and Fig. 6 show the DNL and INL plots for DAC1 on the chip respectively. The DNL values measured also indicate that the DAC is monotonic for all of the input codes.

The dynamic measurements at different sampling rates (F_s) are low frequency ($F_s/512$) single tone SFDR measurements. All dynamic measurement results reported below are -

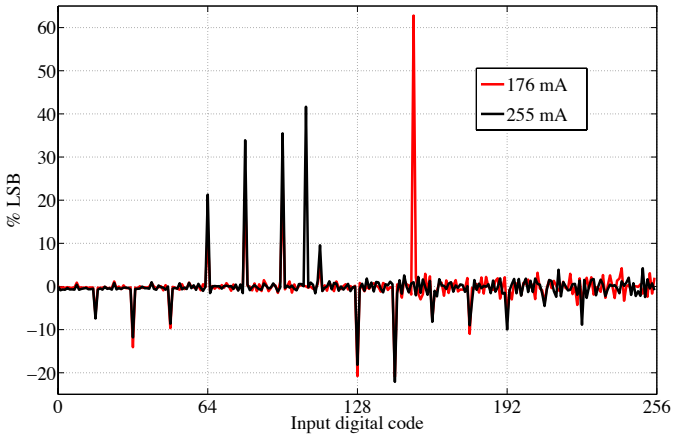


Fig. 5. DNL of DAC1 at full-scale currents of 176 mA and 255 mA

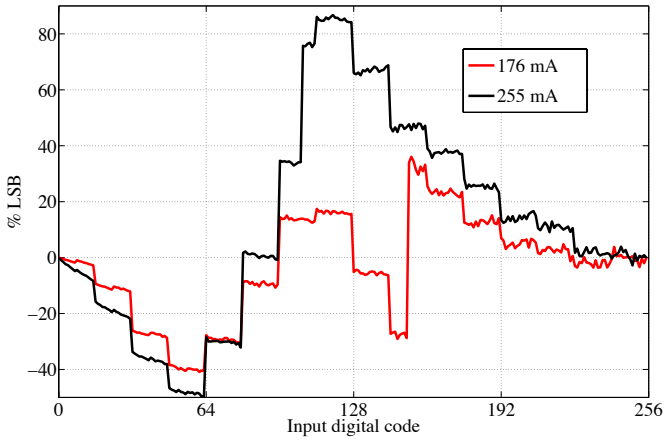


Fig. 6. INL of DAC1 at full-scale currents of 176 mA and 255 mA

quoted at maximum full-scale current of 255 mA and highest sampling rate of 250 MS/s, unless stated otherwise. Fig. 7 shows SFDR results from single tone measurements for different sampling rates, from 10 MS/s to 250 MS/s and different bias currents up to the maximum. A SFDR of 48 dB is achieved at sampling rates up to 100 MS/s. At the highest sampling rate (250 MS/s), 44 dB SFDR is achieved. At low full-scale currents, the SFDR is lower. This can be attributed to increased mismatch at lower bias currents. Glitch performance, linearity of the DAC, and coupled digital noise in the PCB ground net influence the SFDR performance. SFDR reduction at higher sampling rates is explained by degraded glitch performance at these sampling rates and PCB ground net variations due to digital noise coupling.

OFDM frames sent to the driver chip from the FPGA are used to estimate the data rate. For OFDM transmission, the channel is estimated using a sequence of pilot frames: pre-determined OFDM frames, which are known at the receiver. The noise power is computed from the received data. The estimated achievable signal-to-noise ratio (SNR) is computed using the error vector magnitude (EVM) estimation technique, where the signal power is estimated as the channel gain times the original signal power, and the noise power is estimated as the variance of the difference between the received constellation points and the original constellation points. Table1 summarizes the electrical data rate measurement results

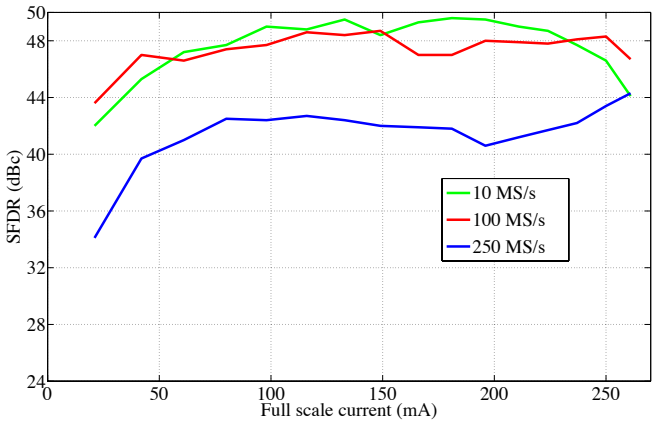


Fig. 7. SFDR vs. Full scale currents at different sampling rates

TABLE I
Electrical data rate measurement results in differential mode

Sampling Rate (MS/s)	QAM levels	Bitrate (Mbps)	BER
100	16	200	$< 10^{-4}$
250	16	500	$< 10^{-4}$

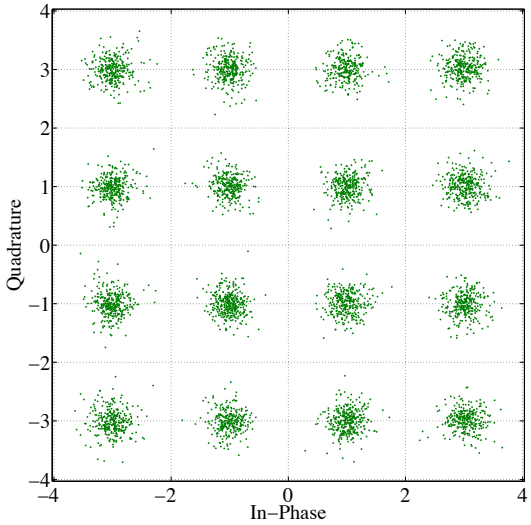


Fig. 8. Scatter plot, 250MS/s 16-QAM, differential electrical measurement using resistive load.

in differential mode from DAC1. The number of bits transmitted (32000) limits the bit error rate (BER) estimation accuracy. Fig. 8 shows the constellation diagram for 250 MS/s 16-QAM. Electrical data rate measurements were performed differentially where the difference voltage across the dummy branch and main branch resistor is demodulated; this cancels out the common mode ground noise induced in the testing PCB.

B. VLC link Results (Single Ended Drive)

The capability of the VLC link established using the driver chip is estimated by decoding the received OFDM frames. The OSRAM commercial LED used for this experiment has a 3 dB bandwidth of 10 MHz, estimated using an Arbitrary Waveform Generator (Agilent, 81180a), Amplifier (Mini-circuits ZHL-

6A-S+), Bias tee (Mini-circuits ZFBT-4R2GW+) and DSO. Fig. 9 shows the VLC link setup. Data rates up to 120 Mbps are achieved at 64-QAM and BER of 3.8 x 10^{-3}. Fig. 10(a) and 10(b) shows the recovered constellation after equalisation for sampling rates of 20 MS/s and 40 MS/s. The estimated SNR of the system including the channel is shown in Fig 10 (c). Full DAC performance (8 bits, 500 MS/s) is not realized in end-to-end system for the following reasons: Limited operating speed of the FPGA board; PCB ground noise; LED non-linearity; free space channel losses; low PD sensitivity at the blue wavelength of the LED; the PD noise contribution; and the frequency profile of the LED which greatly limits the modulation bandwidth. These aspects require further research.

Analysis of the BER versus SNR at different full-scale currents is shown in Fig. 11, which indicates that at higher full-scale currents, higher SNR is obtained due to higher signal strength, which means better BER. Two SNR estimation techniques have been employed. In the first technique, multiple copies of the same pilot frame are used for channel and SNR estimation. In the second technique, multiple different realizations of an OFDM frame are used. As a result, in the first technique, non-linear distortion is not included into the SNR estimation, while the second technique takes the non-linearity into account. Consequently, the second technique provides significantly more reliable estimation of the achieved SNR as apparent from the results in Fig. 11.

C. VLC link (Differential Drive)

In order to demonstrate the optical differential drive capabilities of the driver chip, two commercial LEDs (OSRAM LD W5SM-4S4T-35) are connected to the main branch and the dummy branch of the DAC1 of the chip using shielded cables. Two similar LEDs were used to ensure matching of received signal amplitudes from two similar PDs. LEDs and corresponding PDs were placed as close as possible and facing away from each other to avoid optical coupling. In a practical scenario this would be realised using different colour LEDs coupled to PDs with colour filters. Total current drawn by the whole DAC is constant irrespective of the input code, but current through the main branch is proportional to the input code. Due to the nature of the DAC structure the current through the dummy branch is a complement of the current through the main branch.

The Current through the main branch of the DAC can be expressed as:

$$I_{main\_branch} = I_{full\_scale} - I_{dummy\_branch} \quad (1)$$

where I denote the current. From (1), the intensity of light generated by each LED can be expressed as:

$$L_{main\_branch} = L_{constant} - L_{dummy\_branch} \quad (2)$$

Light generated by each branch can be expressed as follows:

$$L_{blue1} = k\,(I_{full\_scale} - I_{dummy\_branch}) \quad (3)$$
$$L_{blue2} = k\,(I_{full\_scale} - I_{main\_branch}) \quad (4)$$

where L denotes the intensity of light generated. Blue1 and blue2 are the blue LEDs connected to the main and dummy branch respectively, and k denotes the current to light conversion factor. The output from each LED is directed to two PDs. A fair comparison is made between the single ended mode and differential mode in the same measurement setup by-

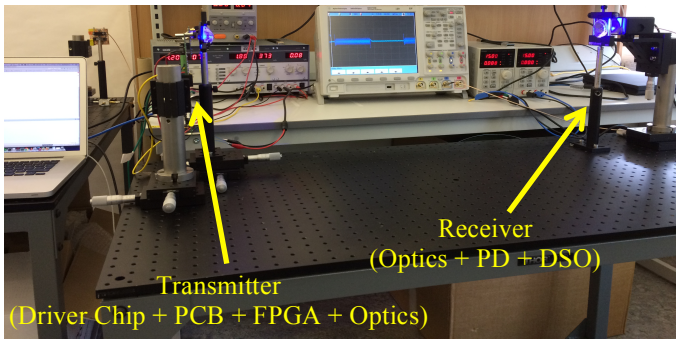


Fig. 9. VLC link setup photograph

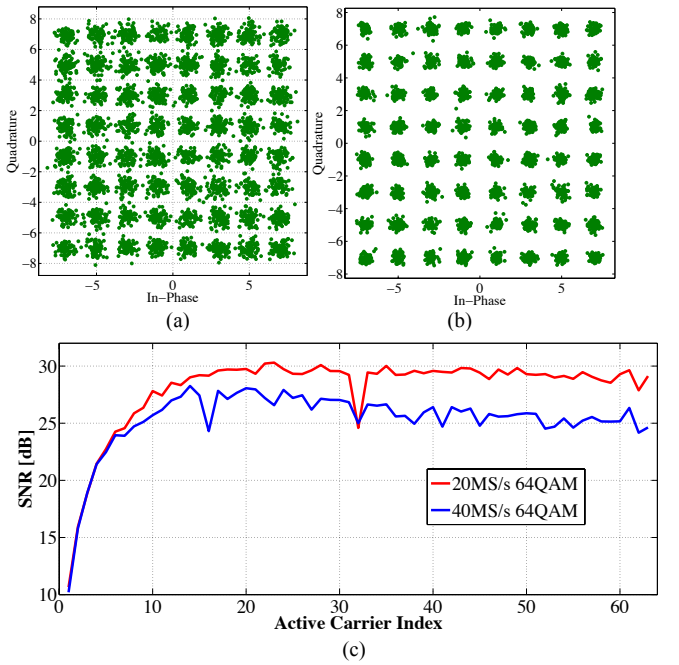


Fig. 10. Scatter plots 64 QAM (a) 40 MS/s; (b) 20 MS/s; (c) SNR plots (VLC link, single ended drive). Subcarrier spacing for a sampling rate of 40 MS/s is 312.5 KHz and 20 MS/s is 156.25 KHz

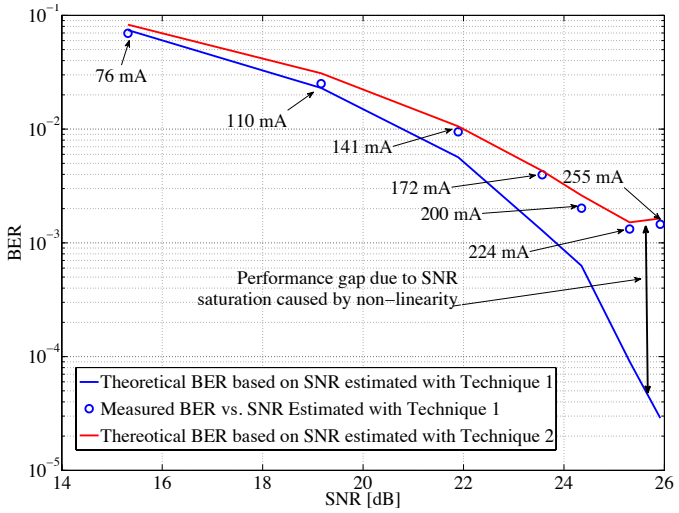


Fig. 11. SNR vs. BER of VLC link at different full-scale currents [40 MS/s, 64QAM]

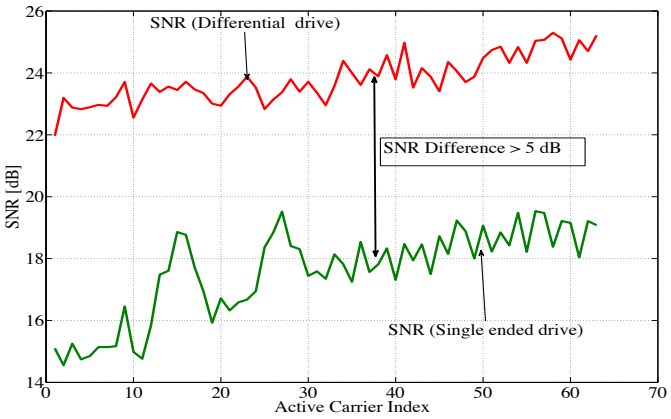


Fig. 12. SNR performance: differential vs. single ended drive. Subcarrier spacing is 156.25 KHz.

using same current bias setting (255 mA), sampling rate (10MS/s) and 4-QAM OFDM signal. In the single ended mode, only electrical output from the PD connected to the main branch is processed, whereas in differential mode, the difference in electrical signal from both PDs is calculated and demodulated. The resultant SNR given in Fig. 12 shows that the differential drive achieves better SNR. This is due to the increased signal amplitude (two times) thereby the increased signal power (four times) from single ended drive, and the reduction in noise power due to cancellation of common mode noise during the difference operation. However, the SNR for differential drive is less than that obtained in the single ended experiment in section B due to the additional losses in the signal path caused by the soldered shielded cable. A future revision of the daughter card with balanced short PCB traces (main branch and dummy branch) should mitigate this.

Average power consumption of the DAC (P_{DAC}) and total power consumed by the system (DAC and LED) (P_{TOTAL}) is estimated by measuring the average voltages across, and currents through each of them, under static (constant data input) and dynamic (OFDM data input) conditions. Power efficiency (η) of the system is then estimated as follows:

$$\eta = 100\left(1 - \frac{P_{DAC}}{P_{TOTAL}}\right) \qquad (5)$$

A power efficiency factor of 72% is observed with static power measurements at maximum full-scale current and constant voltage across the LED and the DAC. Power measurements during OFDM tests indicate an average power efficiency of 67% at the maximum sampling rate and full-scale current. This is much higher than the theoretical limit of class A-B structure (24%) [6]. The high power efficiency of the driver can be attributed to the minimum voltage drop across the transistor stack.

V. CONCLUSIONS

The design and measurement results of a high current (255 mA), high speed (250 MS/s), power efficient (67%) CMOS multi channel LED driver circuit for VLC with capabilities such as differential optical drive, MIMO, CSK and ambient light adjustment are reported. To the authors best knowledge, this is the first high power integrated CMOS LED driver capable of supporting VLC, utilizing complex modulation schemes like OFDM and also at the same time as a LED driver for illumination. Performance limit, assessed through electrical characterization with a resistor load, indicated that DAC is capable of supporting a data rate up to 500 Mbps with BER of < 10^{-4} .VLC link characterization with a commercial LED indicated a data rate up to 120 Mbps with BER of 3.8 x 10^{-3}. Future research will continue to obtain detailed experimental results on the capabilities of the chip such as dimming, CSK and MIMO.

ACKNOWLEDGEMENT

We gratefully acknowledge support by the School of Engineering at the University of Edinburgh for providing a scholarship for this work, which is aligned to the UK Engineering and Physical Sciences Research Council (EPSRC) project EP/K00042X/1. Professor Harald Haas acknowledges support by EPSRC under Grant EP/K008757/1. We would also like to thank Neale Dutton, Luca Parmesan, Richard Walker, Stefan Videv, Muhammed Ijaz, Adean Lutton, Sujan Rajbhandari and Grahame Faulkner for discussions, comments and assistance provided.

REFERENCES

[1] H. Elgala, R. Mesleh, and H. Haas, "Indoor optical wireless communication: potential and state-of-the-art," Communications Magazine, IEEE, vol. 49, pp. 56-62, 2011.

[2] A. M. Khalid, G. Cossu, R. Corsini, P. Choudhury, and E. Ciaramella, "1-Gb/s Transmission Over a Phosphorescent White LED by Using Rate-Adaptive Discrete Multitone Modulation," *Photonics Journal, IEEE,* vol. 4, pp. 1465-1473, 2012.

[3] D. Tsonev, C. Hyunchae, S. Rajbhandari, J. J. D. McKendry, S. Videv, E. Gu, *et al.*, "A 3-Gb/s Single-LED OFDM-Based Wireless VLC Link Using a Gallium Nitride microLED," *Photonics Technology Letters, IEEE,* vol. 26, pp. 637-640, 2014.

[4] G. Cossu, A. M. Khalid, P. Choudhury, R. Corsini, and E. Ciaramella, "3.4 Gbit/s visible optical wireless transmission based on RGB LED," *Optics Express,* vol. 20, pp. B501-B506, 2012/12/10 2012.

[5] B. Schafferer and R. Adams, "A 3V CMOS 400mW 14b 1.4GS/s DAC for multi-carrier applications," in *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, 2004, pp. 360-532 Vol.1.

[6] J. Pierdomenico, S. Wurcer, and B. Day, "A 684-mW adaptive supply full-rate ADSL CO driver," *Solid-State Circuits, IEEE Journal of,* vol. 37, pp. 1831-1838, 2002.

[7] P. Malcovati, M. Belloni, F. Gozzini, C. Bazzani, and A. Baschirotto, "A 0.18µm CMOS 91%-efficiency 0.1-to-2A scalable buck-boost DC-DC converter for LED drivers," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, 2012, pp. 280-282.

[8] A. Van Den Bosch, M. Borremans, M. Steyaert, and W. Sansen, "A 12 b 500 MSample/s current-steering CMOS D/A converter," in *Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC. 2001 IEEE International*, 2001, pp. 366-367.

[9] Z Chen, D. Tsonev, and H. Haas, "A Novel Double-Source Cell Configuration for Indoor Optical Attocell Networks," IEEE Global Communications Conference (Globecom 2014), Austin, TX, USA, 8-12, Dec, 2014.

[10] A. Boni, A. Pierazzi, and D. Vecchi, "LVDS I/O interface for Gb/s-per-pin operation in 0.35 µm CMOS," *Solid-State Circuits, IEEE Journal of,* vol. 36, pp. 706-711, 2001.

[11] W. Kester, "SECTION 2-1 - Coding and Quantizing," in *Data Conversion Handbook*, W. Kester, Ed., ed Burlington: Newnes, 2005, pp. 57-72.

[12] W. Kester and J. Bryant, "SECTION 2-3 - Data Converter AC Errors," in *Data Conversion Handbook*, W. Kester, Ed., ed Burlington: Newnes, 2005, pp. 83-122.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LPT.2016.2624281, IEEE Photonics Technology Letters

High Speed Integrated Digital to Light Converter for Short Range Visible Light Communication

Aravind V. N. Jalajakumari, *Member IEEE,* Enyuan Xie, Jonathan McKendry, *Member IEEE*, Erdan Gu, Martin D. Dawson, *Fellow IEEE*, Harald Haas, *Member IEEE*, Robert K. Henderson, *Senior Member IEEE*

***Abstract*—Design details and characterisation results of an integrated digital to light converter (DLC) for short range visible light communication (VLC) is reported. The integrated DLC can generate 16 light intensity levels at fast switching speeds, up to 500 MHz, thus enabling fast intensity modulated VLC. Data rates up to 365 Mb/s are achieved with bit error rate (BER) 1×10^{-3} at a link distance of 5 cm and average electrical power efficiency of 70%. Optimisation in the micro light emitting diode (μLED) manufacturing process has resulted in approximately three fold increase in data rate of the system. Spectrally efficient modulation schemes like orthogonal frequency division multiplexing (OFDM) and pulse amplitude modulation (PAM) are also demonstrated using this integrated system.**

***Keywords*—Visible light communication, DLC, optical wireless communication, DAC, CMOS**

I. Introduction

In visible light communication (VLC) the intensity of light is modulated to transmit digital data into free space [1]. The availability of the unregulated visible light spectrum and the finite radio frequency (RF) spectrum has led to research interest in VLC. High speed VLC systems require light sources with fast switch ON/OFF times to enable high speed communication. Semiconductor light emitting diodes (LEDs) are suitable candidates for this due to their high inherent bandwidth [2]. Another advantage of LEDs is that they can be controlled electronically. High speed VLC links have been realised using micro light emitting diodes (μLEDs) [3], [4] and commercial LEDs [5], [6], [7]. These VLC links utilise a single LED to establish communications by varying either the voltage or current, thereby achieving intensity modulation.

A single VLC link can be established using multiple LEDs, whereby turning on more than one LED, the intensity of light generated can be varied [8]–[11]. This is achieved using a digital to light converter (DLC), where each input digital code translates to turning on a corresponding number of LEDs to represent a proportional intensity level. Fig. 1 shows a 2-bit DLC output LED operation at 2 different digital input codes. This method of varying the intensity of the light for modulation has advantages including power efficiency and assured monotonicity in the output power levels. Published driver architectures [8], [9] utilise discrete components to realise such communication links, whereas [11] realises an integrated complimentary metal oxide semiconductor (CMOS) Gallium Nitride (GaN) DLC system. Effects of μLED mismatch in such a system was studied in [10]. Symbol rates up to 100 MS/s have been achieved in [11] using 4-PAM and a voltage mode drive scheme.

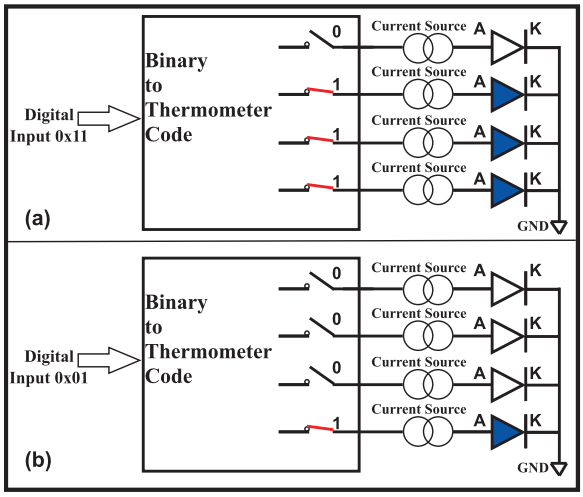


Fig. 1: Illustration of DLC system operation; (a) With digital input of 3 (0x11); (b) With digital input of 1 (0x01)

In this study, a digital current mode driver is employed to drive an array of μLEDs realising a DLC. An improved metallisation scheme has given a better linear response compared with [11]. Since the LED driver is a DLC, it has the flexibility to accept an incoming data stream generated with any standard modulation scheme, however results are presented only for OFDM modulation. In this paper, an integrated VLC transmitter is proposed with 16 μLEDs wire bonded on top of a current steering digital-to-analog converter (DAC) based CMOS driver. Such a driver would be relevant to short range VLC applications including internet of things (IoT).

The rest of the paper is organised as follows. Driver circuit architecture, μLED array construction and wire bonding details are presented in Section II. In Section III the experimental setup is presented. In Section IV, DLC characteristics and data link measurement results are given. Conclusions are given in Section V.

Aravind V. N. Jalajakumari, Harald Haas and Robert K. Henderson are with the School of Engineering, University of Edinburgh, Edinburgh, EH9 3JL, United Kingdom e-mail: [a.venugopalan, h.haas, robert.henderson]@ed.ac.uk

Enyuan Xie, Jonathan McKendry, Erdan Gu and Martin D. Dawson are with the Institute of Photonics, University of Strathclyde, Glasgow G1 1RD, United Kingdom. e-mail: [enyuan.xie, jonathan.mckendry, erdan.gu, m.dawson]@strath.ac.uk

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LPT.2016.2624281, IEEE Photonics Technology Letters

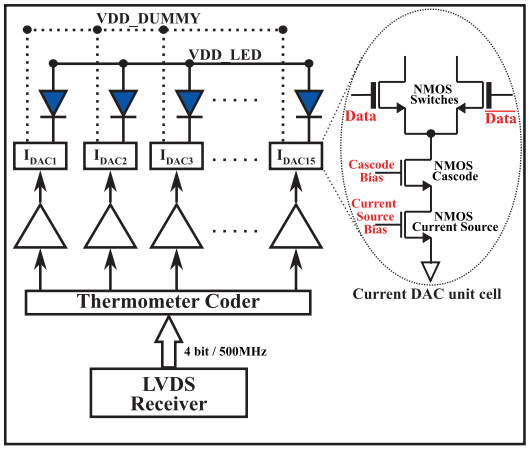


Fig. 2: Block diagram of DLC system with μLED

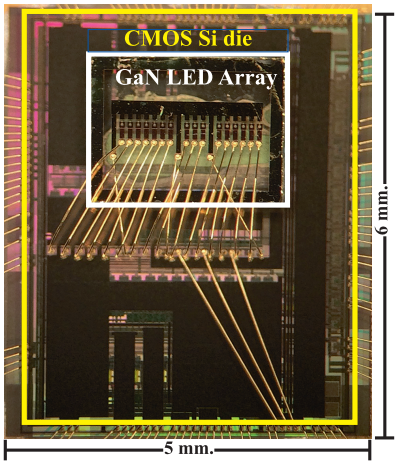


Fig. 3: Photograph of DLC system with μLED

II. System Description

The integrated DLC consists of two components, namely a current steering DAC based CMOS LED driver and GaN based μLED array with 16 μLEDs.

A. Driver architecture

Fig. 2 shows the block diagram of the CMOS DLC. 4-bit data received through a high speed (500 MHz) low voltage differential signalling (LVDS) receiver is converted to a 16 bit thermometer code. Each bit in the thermometer code is converted to a differential mode signal and buffered, which controls 16 differential current cells (I_{DAC}). Each current cell has an adjustable output current (1mA to 16mA) and two output branches (differential structure), with out-of-phase currents, namely, main branch and dummy branch. The current cell architecture is also shown in Fig. 2.

A current cell consists of an N-channel metal oxide semiconductor field effect transistor (NMOS) current source transistor, cascode transistor and differential pair switches. It is capable of operating up to 500 MHz switching speeds. A high bit from the thermometer code will cause all current to flow through the main branch and no current through the dummy branch; a low bit will reverse the current flow. The main branch of each driver is connected to a customized pad opening onto which μLEDs are wire bonded and dummy branch is tied to 1.8 V rail.

B. μLED array construction

The GaN μLED array is fabricated in a common anode process. Since the driver has NMOS current sources with open drain architecture which requires individual cathodes from each μLED, a common anode construction is used. The μLED arrays are fabricated from commercial 450 nm Indium Gallium Nitride (InGaN)/ Gallium Nitride (GaN) LED wafer grown on the sapphire substrate with c-plane (0001) surface orientation. Each one-dimensional linear array consists of 16 top-emitting μLED elements. In order to be compatible with NMOS transistor-based drivers, these arrays have a reversed configuration compared with conventional ones [3]. Each μLED element in these novel arrays is individually addressed by its own n-type contact (cathode) with a shared p-type contact (anode). To achieve this configuration, 16 Gallium Nitride (GaN) mesas are firstly etched down onto the sapphire substrate by Cl2-based inductively coupled plasma (ICP). Then, a disk-shaped μLED element with a diameter of $24\,\mu m$ is generated on each mesa through another ICP etching to n-type GaN. These steps enable the isolation between the μLED elements from the shared p-type and n-type GaN layers. After these etching steps, metal contact to p-type GaN is formed through e-beam evaporation and thermal annealing. Two metal schemes, $20\,nm$ Pd (labelled as SEG1) and $10/20\,nm$ Ni/Au (labelled as SEG2) are employed for comparison. Annealing conditions for the above schemes are 300 °C in Nitrogen (N_2) ambient and 500 °C in air ambient, respectively. The metallisation on the isolated n-type GaN mesa is formed by sputtering a Ti/Au ($50/200\,nm$) metal bilayer. Then, a $300\,nm$ thick SiO_2 layer is deposited by plasma enhanced chemical vapour deposition. After selectively removing SiO_2 on top of each element, another Ti/Au metal bilayer is deposited to interconnect LED elements and, thus, form a shared p-type contact (anode).

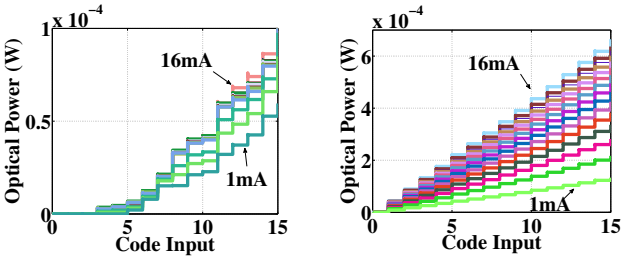
C. Wire bonding and Packaging

The CMOS LED driver and GaN μLED array are wire bonded to establish electrical connectivity. Customised $60\,\mu m$ pads are provided at the centre of the CMOS LED driver to facilitate the wire bond. Standard $25\,\mu m$ gold wire is used for bonding purposes in Palomar 8000 bonding machine. Fig. 3 shows the bonded DLC chip. The bonded chip is packaged in a 120 pin ceramic pin grid array (CPGA) package with transparent lid.

III. Experimental Setup

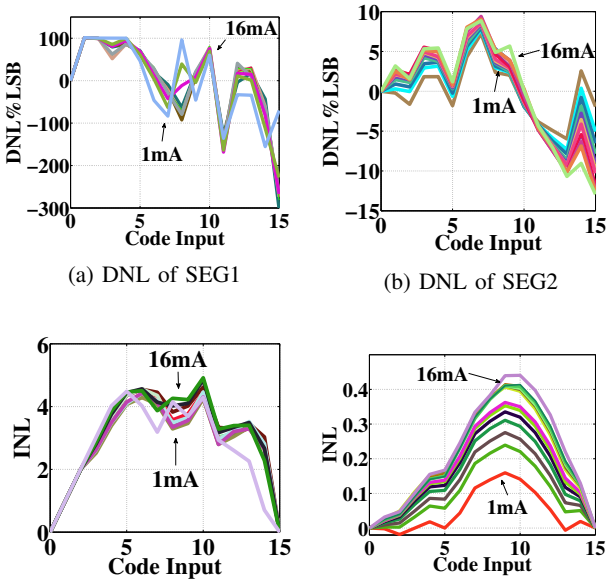
A printed circuit board (PCB) [12] with an off-the-shelf field programmable gate array (FPGA) daughter card (Opal Kelly XEM6310) is used to house the DLC chip. The main functions of the PCB are to provide adjustable external bias control, supply adequate power and control/data interface for the DLC chip. VDD_LED node is supplied from an external 8.2 V direct current (DC), whereas VDD_DUMMY is tied to 1.8 V internally through wire bonding (see Fig. 2). The serial

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/LPT.2016.2624281, IEEE Photonics Technology Letters



(a) SEG1 (b) SEG2

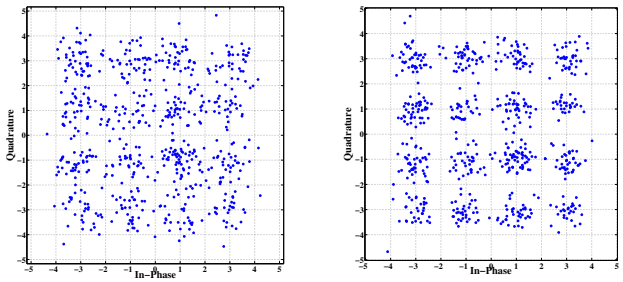
Fig. 4: Input-Output characteristics of SEG1 and SEG2 chips



(a) DNL of SEG1 (b) DNL of SEG2

(c) INL of SEG1 (d) INL of SEG2

Fig. 5: DNL and INL of SEG1 and SEG2 chips



(a) SEG1 (b) SEG2

Fig. 6: 16-QAM constellation of SEG2 and SEG1 chips at a clock rate of 200MHz

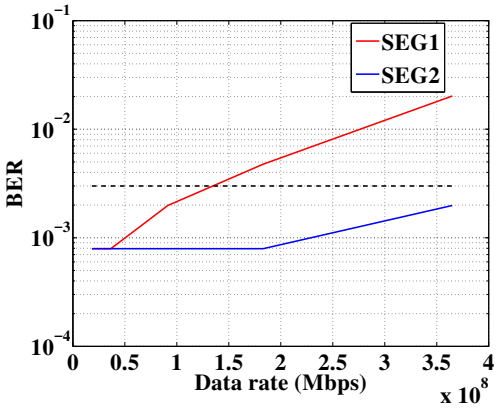


Fig. 7: BER of SEG1 and SEG2 chips at 16-QAM, 200 MHz

interface of the DLC chip enabled current variation during different experiments (1 mA - 16 mA). For the SEG2 chip the bias current was 8 mA at 8.2 V, whereas due to its inferior performance a higher bias current (11 mA) and voltage (11 V) was needed for the SEG1 chip to generate the same light output. Data to be transmitted through the μLEDs and control signals for the DLC chip are generated in a personal computer (PC) and sent to the FPGA card through a universal serial bus (USB) interface. A custom receiver module [13] with electrical bandwidth of 850 MHz is used to receive the data. The receiver module has a Hamamatsu S8890 Si avalanche photodiode (APD), custom built concentrator and an off-the-shelf transimpedance amplifier (Maxim MAX3665). The received data is sampled using a digital storage oscilloscope (DSO) (Agilent 7402D) and processed offline in Matlab. The distance between the μLED array and the APD receiver is 5 cm.

IV. DLC Results

Various static characteristics of the DLC are measured to quantify its performance. These are input-output characteristics; differential non-linearity (DNL) [14], which is the difference between the actual output step and ideal least significant bit (LSB) step expressed in LSBs; and integral non-linearity (INL) [14], which is the difference between actual output and ideal output expressed in LSBs. All static measurements are performed at different bias current configurations (1 mA to 16 mA in steps of 1 mA).

A. Static characteristics

Input-output characteristics of both SEG1 and SEG2 are shown in Fig. 4. The output power of SEG2 is ~6 times that of SEG1. It can also be seen that the SEG2 chip offers better linearity over the code range compared with SEG1. Both SEG1 and SEG2 systems are monotonic due to the thermometer coding scheme in the DAC. Both DNL and INL of the 4 bit segmented DLC system are characterised. For 4-bit linearity, INL of the DLC system should be within 0.5 LSB which implies the DNL should be within ± 1 LSB. Fig. 5 shows DNL and INL for both SEG1 and SEG2 chips. The SEG2 chip has its DNL and INL within limits whereas the SEG1 chip does not due to its inferior linearity. The INL

performance of the SEG2 chip indicates 5 bits performance. Better linearity of SEG2 chip can be attributed to the contact metalisation scheme (Ni/Au) which gives better performance compared with SEG1 (Pd). The average power efficiency of the driver is calculated assuming a uniform distribution of ones and zeros in a random information signal thus on an average 8 LEDs are in ON state and 8 in the OFF state. An individual LED current of 16 mA, results in 128 mA current through both main and dummy branch. VDD_LED of 8.2 V (7 V across LED and 1.2 V across the driver) results in an average ON LED output power of 0.9 W and average ON driver power of 0.15 W. VDD_DUMMY of 1.8 V results in average OFF driver power of 0.23 W. Average power efficiency is the ratio of LED output power (0.9 W) to the total input power to the driver (0.9 + 0.23 + 0.15 W) is then 70%. It is possible to reduce the dummy node supply to 1.2 V, while keeping all of the transistors in saturation thereby maintaining linearity and reducing power dissipation further.

B. Data transmission results

A data rate up to 365 Mbps has been achieved with OFDM modulation (16 QAM, cyclic prefix (CP) = 10, 128 point fast Fourier transform (FFT)) while clocking the SEG2 chip at 200 MHz. A clipping limit of $\pm 3.2\sigma$, which results in negligible distortion [15], was used and kept constant for all experiments. Compared to discrete component DLC implementations [8], this is approximately a 10 fold increase in data rate. This is due to circuit miniaturisation, high bandwidth μLEDs and a better metallisation scheme. Fig. 6 shows the constellation diagram for both SEG1 and SEG2 chips while transmitting data in the configuration mentioned above. It is evident from the constellation that the non-linear transfer characteristic of the SEG1 chip is worsening the BER. The data rate versus BER is shown in Fig. 7. The SEG2 chip has its BER within forward error correction (FEC) limits of 1×10^{-3} [16] up to 365 Mbps, and for the SEG1 chip the maximum possible data rate is ∼130 Mbps. The OFDM bit stream length was 32 kbits limiting the BER to 7.9×10^{-4}. The link distance of 5 cm could be increased further by using additional optical components [17].

V. Conclusion

Integration of GaN μLEDs and a CMOS LED driver into a single package has resulted in a short range VLC transmitter capable of transferring data up to few hundred Mbps. This DLC drive scheme combined with improvements in μLED metallisation scheme are shown to be suited for complex modulation schemes such as OFDM whilst operating at high power efficiency. Applications such as IoT which require short range VLC transmission would benefit from this system.

VI. Acknowledgements

We gratefully acknowledge support by the School of Engineering at the University of Edinburgh for providing a scholarship for this work, which is aligned to the UK Engineering and Physical Sciences Research Council (EPSRC) project EP/K00042X/1. We would also like to thank Grahame Faulkner for providing the optical receiver and Dobroslav Tsonev for providing the decoding firmware.

References

[1] Y. Tanaka, T. Komine, S. Haruyama, and M. Nakagawa, "Indoor visible communication utilizing plural white LEDs as lighting," in *Personal, Indoor and Mobile Radio Communications, 2001 12th IEEE International Symposium on*, vol. 2, Sep 2001, pp. F–81–F–85 vol.2.

[2] C.-H. Wu, G. Walter, H. W. Then, M. Feng, and N. Holonyak, "4-GHz modulation bandwidth of integrated 2×2 LED array," *Photonics Technology Letters, IEEE*, vol. 21, no. 24, pp. 1834–1836, Dec 2009.

[3] J. J. D. McKendry *et al.*, "Individually addressable AlInGaN micro-LED arrays with CMOS control and subnanosecond output pulses," *Photonics Technology Letters, IEEE*, vol. 21, no. 12, pp. 811–813, 2009.

[4] D. Tsonev *et al.*, "A 3-Gb/s single-LED OFDM-based wireless VLC link using a gallium nitride μLED," *Photonics Technology Letters, IEEE*, vol. PP, no. 99, pp. 1–1, 2014.

[5] J. Vucic, C. Kottke, S. Nerreter, K. D. Langer, and J. W. Walewski, "513 Mbit/s Visible Light Communications Link Based on DMT-Modulation of a White LED," *Journal of Lightwave Technology*, vol. 28, no. 24, pp. 3512–3518, Dec 2010.

[6] N. Fujimoto and S. Yamamoto, "The fastest visible light transmissions of 662 Mb/s by a blue LED, 600 Mb/s by a red LED, and 520 Mb/s by a green LED based on simple OOK-NRZ modulation of a commercially available RGB-type white LED using pre-emphasis and post-equalizing techniques," in *Optical Communication (ECOC), 2014 European Conference on*, Sept 2014, pp. 1–3.

[7] A. H. Azhar, T. A. Tran, and D. O'Brien, "A Gigabit/s Indoor Wireless Transmission Using MIMO-OFDM Visible-Light Communications," *Photonics Technology Letters, IEEE*, vol. 25, no. 2, pp. 171–174, 2013.

[8] T. Fath, C. Heller, and H. Haas, "Optical Wireless Transmitter Employing Discrete Power Level Stepping," *Lightwave Technology, Journal of*, vol. 31, no. 11, pp. 1734–1743, June 2013.

[9] J. Yew, S. Dissanayake, and J. Armstrong, "Performance of an experimental optical DAC used in a visible light communication system," in *Globecom Workshops (GC Wkshps), 2013 IEEE*, Dec 2013, pp. 1110–1115.

[10] H. Qian, S. Zhao, S. Cai, and T. Zhou, "Digitally Controlled Micro-LED Array for Linear Visible Light Communication Systems," *Photonics Journal, IEEE*, vol. 7, no. 3, pp. 1–8, June 2015.

[11] J. Herrnsdorf, J. McKendry, R. Ferreira, R. Henderson, S. Videv, S. Watson, H. Haas, A. Kelly, E. Gu, and M. Dawson, "Single-chip discrete multitone generation," in *Summer Topicals Meeting Series (SUM), 2015*, July 2015, pp. 47–48.

[12] A. Jalajakumari, D. Tsonev, K. Cameron, H. Haas, and R. Henderson, "An energy efficient high-speed digital LED driver for visible light communications," in *Communications (ICC), 2015 IEEE International Conference on*, June 2015, pp. 5054–5059.

[13] D. O'Brien, R. Turnbull, H. L. Minh, G. Faulkner, O. Bouchet, P. Porcon, M. El Tabach, E. Gueutier, M. Wolf, L. Grobe, and J. Li, "High-Speed Optical Wireless Demonstrators: Conclusions and Future Directions," *Lightwave Technology, Journal of*, vol. 30, no. 13, pp. 2181–2187, July 2012.

[14] D. Johns, *Analog integrated circuit design*. New York: John Wiley & Sons, 1997.

[15] S. Dimitrov, S. Sinanovic, and H. Haas, "Clipping noise in OFDM-based optical wireless communication systems," *IEEE Transactions on Communications*, vol. 60, no. 4, pp. 1072–1081, April 2012.

[16] ITU-T, "G.975.1 : Forward error correction for high bit-rate dwdm submarine systems," 2004. [Online]. Available: http://www.itu.int/rec/T-REC-G.975.1-200402-I/en

[17] S. Rajbhandari, H. Chun, G. Faulkner, D. O'Brien, A. V. N. Jalajakumari, K. Cameron, R. Henderson, E. Xie, J. J. D. McKendry, J. Herrnsdorf, E. Gu, M. D. Dawson, D. Tsonev, M. Ijaz, and H. Haas, "Multi-gigabit integrated MIMO visible light communication system: Progress and updates," in *2015 IEEE Summer Topicals Meeting Series (SUM)*, July 2015, pp. 230–231.

A Multigigabit per Second Integrated Multiple-Input Multiple-Output VLC Demonstrator

Sujan Rajbhandari, *Member, IEEE*, Aravind V. N. Jalajakumari, Hyunchae Chun, Grahame Faulkner, Katherine Cameron, Robert Henderson, Dobroslav Tsonev, *Member, IEEE*, Harald Haas, *Member, IEEE*, Enyuan Xie, Jonathan J. D. McKendry, *Member, IEEE*, Johannes Herrnsdorf, Ricardo Ferreira, Erdan Gu, Martin D. Dawson, *Fellow, IEEE*, and Dominic O'Brien, *Member, IEEE*

***Abstract*—In this paper, we report the performance of an imaging multiple-input multiple-output (MIMO) visible light communication (VLC) system. The VLC transmitter consists of a two-dimensional (2-D), individually addressable Gallium Nitride micro light-emitting diode (μLED) array. The receiver uses a 2-D avalanche photodiode array fabricated using complementary metal oxide semiconductor (CMOS). Using integrated CMOS-based LED drivers, a data rate greater than 1 Gb/s was obtained at a link distance of 1 m with the system field of view of 3.45° using four channels. At a reduced link distance of 0.5 m, a data rate of 7.48 Gb/s was obtained using a nine channel MIMO system. This demonstrates the feasibility of compact MIMO systems that offer substantial data rates.**

***Index Terms*—Integrated VLC, multiple input multiple output, visible light communications, VLC demonstrator.**

I. Introduction

VISIBLE light communications (VLC) systems, realized using solid-state lighting (SSL) devices, can offer high-speed data communication in addition to their primary purpose of illumination. With the white light emitting diodes (LEDs) expected to be the dominant illumination device in the home and office environment in the near future, the use of VLC systems will grow exponentially over the coming decades [1]. As a result, there has been significant research and commercial interest in VLC systems over the last ten years (see [2] for the detailed review). This is largely due to several key advantages that VLC offers in comparison to the existing radio frequency (RF) technology, including license-free operation, high available bandwidth, high spatial diversity, innate security, and controlled beam shaping.

Phosphor based white LEDs have a low communication bandwidth (a few MHz) due to the long photoluminescence lifetimes of the phosphor [3]. The bandwidth of the blue LED itself is limited to 20–30 MHz. Using pre and post- equalisation for on-off keying (OOK) modulation, a data rate of 550 Mbps was demonstrated using a phosphorescent white LED [4]. Further enhancement in data rate was achieved by adopting advanced modulation schemes including carrierless phase and amplitude modulation (CAP) and orthogonal frequency division multiplexing (OFDM) [5], [6].

To increase the data rates further, VLC systems must use wavelength division multiplexing (WDM) and/or spatial multiplexing (also known as multiple input multiple output (MIMO)) [2]. Using WDM, VLC systems with data rates up to 10 Gbps were demonstrated [7], [8]. However, there are limited practical work using spatial MIMO and most of these are low data rate proof-of-the-concept demonstrations [9]–[11].

Research progress has been substantial in the past few years [2], and whilst a 'killer app' may provide a kick-start for VLC system [12], it is also essential to explore technologies that can make a high-speed bi-directional VLC system compatible for energy-efficient integration with existing CMOS-based consumer electronics (e.g. mobile devices). Except for the use of CMOS-based image sensors [13], [14] and other low-speed demonstrations [15], most of the practical VLC demonstrations used off-the-shelf components that are not suitable for mass production and difficult to integrate into mobile devices. In a real-time application, device and system constraints that are not encountered in the laboratory environment, including limited memory, real-time processing power, and clock rates, also need to be addressed.

In this paper, we report high-speed imaging MIMO systems which address the issues of integrating transmitter and receiver components. We have demonstrated four and nine

Manuscript received February 16, 2016; revised June 16, 2016, August 15, 2016, October 27, 2016, and March 15, 2017; accepted April 2, 2017. Date of publication April 16, 2017; date of current version September 8, 2017. This work was supported by the U.K. Engineering and Physical Sciences Research Council under Grant EP/K00042X/1. *(Corresponding author: Sujan Rajbhandari.)*

S. Rajbhandari is with the School of Computing, Electronics and Mathematics, Centre for Mobility and Transport, Coventry University, Coventry CV1 5FB, U.K. (e-mail: sujan.rajbhandari@coventry.ac.uk).

A. V. N. Jalajakumari, K. Cameron, and R. Henderson are with the CMOS Sensors & Systems Group, University of Edinburgh, Edinburgh EH9 3JL, U.K. (e-mail: A.Venugopalan@ed.ac.uk; K.Cameron@ed.ac.uk; Robert.Henderson@ed.ac.uk).

H. Chun, G. Faulkner, and D. O'Brien are with the Department of Engineering Science, University of Oxford, Oxford OX1 3PA, U.K. (e-mail: hyunchae.chun@eng.ox.ac.uk; grahame.faulkner@eng.ox.ac.uk; dominic.obrien@eng.ox.ac.uk).

D. Tsonev and H. Haas are with the pureLiFi Ltd., Edinburgh EH9 3JL, U.K., and also with the Institute for Digital Communications, Li-Fi R&D Centre, University of Edinburgh, Edinburgh EH9 3JL, U.K. (e-mail: dobroslav.tsonev@purelifi.com; h.haas@ed.ac.uk).

E. Xie, J. J. D. McKendry, J. Herrnsdorf, R. Ferreira, E. Gu, and M. D. Dawson are with the Department of Physics, Institute of Photonics, University of Strathclyde, Glassgow G4 0NW, U.K. (e-mail: enyuan.xie@strath.ac.uk; jonathan.mckendry@strath.ac.uk; johannes.herrnsdorf@strath.ac.uk; ricardo.ferreira@strath.ac.uk; erdan.gu@strath.ac.uk; m.dawson@strath.ac.uk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JLT.2017.2694486

channel MIMO systems with maximum data rate of ~890 Mbps per channel with an aggregate data rate of 7 Gbps for nine channels. Higher data rates have been demonstrated using similar transmitter devices using significantly larger area photodiodes (PDs) and bigger optical aperture at the receiver. However, these demonstrations have a very limited field of view (FOV) as collimating and focusing is used to concentrate most of the emitted power onto the detector [28]. Hence, the contribution of the paper is as follows:

a) Demonstration of fully integrated MIMO-VLC

CMOS technology is widely used to realize integrated circuits, especially for mass production due to low power and high-speed performance. Previously reported CMOS based LED drivers have low driving currents (less than 70 mA) and limited data rate support (up to 155 Mb/s) (see [17], Table x). The CMOS-based LED driver circuit reported here can deliver up to 500 MS/s at a maximum full-scale current of 255 mA and has a power efficiency of 67%. The driver supports different modulation schemes (pulse amplitude modulation (PAM), CAP, OFDM) with the capability to drive multiple LEDs in MIMO or single-input-single-output (SISO) modes. A detailed description of the driver is reported in [18].

The fully integrated system uses an array of blue μLEDs driven by a CMOS driver and an array of avalanche photodiodes (APDs) and processing circuitry manufactured using CMOS technology. Preliminary results using 1st generation APDs receiver with a bandwidth of ~22 MHz (without the CMOS driver) was reported in [19], [20]. Further, results with the second generation of APDs were reported in [21]. To the best of authors' knowledge, this is the first fully integrated MIMO demonstration.

b) Demonstration of spatially dense high-speed MIMO-VLC

MIMO-VLC has so far been demonstrated only for limited data rates (often far below the maximum rate demonstrated using a single channel) [9]–[11]. In this paper, we have demonstrated data rates up to 7 Gbps using nine channels with transmitter separation of 750 μm and receiver separation of 250 μm. This demonstration improves upon /surpass the existing systems in terms of i) **higher data rate**: the previously reported maximum data rates for MIMO system (in an ideal condition i.e. without optical cross-talk) was 1.3 Gbps [10], [22]. In this paper, we have improved the data rate to 7 Gbps. This data rate was achieved using significantly smaller size photodiode ($200 \times 200\ \mu m^2$) instead of using large area PDs such as 7.1 mm^2 in [11], [22], 10.24 mm^2 in [10] and 15 mm^2 in [9] ii) **spatial data density**: in comparison to above-mentioned work, we demonstrated system with a high spatial density. The previous MIMO work was demonstrated with transmitter spacing in cm range (e.g. 5 cm in [11], 15 cm in [10] and 25 cm in [9]). In comparison, the current system has transmitter spacing of 750 μm increasing the spatial density by >4000 channel/cm^2. Though this increase in the spatial density may not directly translate into the similar increment in the data rate, this demonstration provides a platform to use the multiple LEDs chips within each luminaire of the commercial chip-on-board (COB) LED architecture of illumination devices for parallel data transmission iii) **higher MIMO order**: the previously reported high-speed MIMO-VLC system are limited to 4-parallel channels. In the work, we have improved the number of channel to nine, limited by available transceivers and iv) **scalability:** since the transceiver is manufactured in CMOS technology, the system is readily scalable. We have demonstrated that the same system can be scaled from 4-channel to 9-channel. Higher order MIMO system is feasible with a larger array of the transceiver.

To the best of authors' knowledge, this is the first large-scale MIMO-VLC demonstration as we practically demonstrated a 9×9 MIMO system. We have reported a complete system with full devices and communication link characterization including error probability within the coverage distance. With the demonstration of high-speed, high-density, a large-scale MIMO-VLC system using CMOS-based LED driver and APD receiver, we have not only made system compact but also more practical for large scale integration with the existing system.

The rest of the paper is organized as follows: Section II gives an overview of the MIMO VLC system. The sub-systems of the demonstrator are described in detail in this section. Section III details the experimental set-up. The experimental results are presented in Section IV. Finally, conclusions are given in Section V.

II. Integrated System Description

The device parameters for optimum performance of a VLC system depend on the device constraints of both the transmitter and the receiver. At the transmitter, there is an inter-relationship between the μLED area, optical power, and bandwidth. Similarly, the photodiode bandwidth depends on its active area. By incorporating the power penalty for multilevel PAM with μLED constraints (area-bandwidth-output power relationship) and APD constraints (area-bandwidth relationship) in link budget analysis, a realistic target of 1 Gbps at 1 m distance was established for this integrated MIMO-VLC system. A conservative goal of 1 Gbps over 1 m was chosen based on the preliminary modelling of likely available μLED devices and CMOS-based receiver sensitivities. Though the link distance is lower than average distance ceiling/user, the system is scalable to a longer distance. Refer to [19] for detailed derivations of these parameters and numerical values.

A. Transmitter Subsystem

The transmitter subsystem consists of the μLED driver chips, the μLED array and associated printed circuit boards (PCB). The μLED driver chip is designed and implemented in an Austria Micro Systems 0.18 μm CMOS process. Each chip consists of four independent current steering digital to analogue converter (DAC) based driver channels each with 8-bit resolution. The chip can drive four individual LEDs in a ganged mode (i.e. all channels driving the same data stream) or MIMO mode (each channel driving an independent data stream). In MIMO mode, each driver operates with four times lower clock rate. Each driver channel can deliver full-scale current up to 255 mA (i.e. ~1 A per chip), and power efficiency is 67% [18]. The DC bias current of each DAC can be varied independently from 16 mA to 255 mA with a 4-bit resolution. The DAC is designed

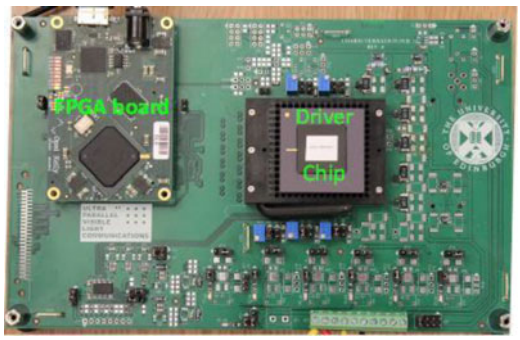


Fig. 1. μLED driver chip with associated PCB and FPGA.

to operate at a maximum sampling frequency of 500 MS/s. A custom PCB platform provides an interface between the driver chip and a field programmable gate array (FPGA) card (Opal Kelly XEM6310) (see Fig. 1). The FPGA provides the data, sampling clock, and other control signals to the driver chip. The full electrical characteristic of driver chip was reported in [18].

B. μLEDs

The MIMO device consists of a 6 $\times$ 6 array of individually-addressable μLEDs with 39 μm diameter and was fabricated from commercially available GaN LED wafer material, grown on a 2" c-plane sapphire substrate. Each individual μLED has a common p-contact and an individually addressable n-contact to make them compatible for driving with an NMOS-based CMOS driver. The MIMO μLED array is arranged in nine 2 $\times$ 2 clusters with a pitch of 69 μm between two adjacent μLED elements (Fig. 2(a)). The separation between adjacent clusters is 750 μm making an end-to-end separation of 1500 μm. The nominal peak emission wavelength for each μLED is 450 nm with 20 nm full width at half maximum line width.

The μLED array is wire bonded to a 132-pin ceramic package which is attached to a daughter card (see Fig. 2(b)). The daughter card is connected to a motherboard through four high-speed connectors, and the motherboard is connected to the LED driving subsystem. This hierarchical approach allows the LED array to be easily exchanged with another array.

C. Receiver

A 3 $\times$ 3 APD array of detectors, each 200 μm $\times$ 200 μm on 240 μm pitch was designed and fabricated in 0.18 μm CMOS process as shown inside the rectangular box in Fig. 3. The outer APDs are test structures not relevant to this work. The APDs have a responsivity of 2.61 A/W at 450 nm with a reverse bias voltage of 9.1 V. Each APD has an associated transimpedance amplifier in a shunt-shunt feedback topology. The shunt-shunt feedback topology was selected as it offers better noise performance than alternatives. The outputs of all nine APDs can be accessed simultaneously via SMA connectors.

D. Optical Design

An imaging MIMO system is preferred over a non-imaging MIMO system, as the channel **H**-matrix of an imaging system

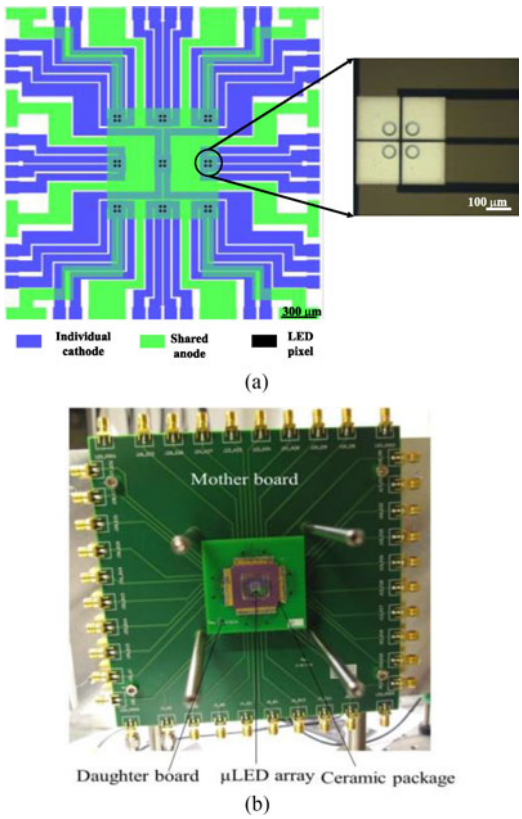


Fig. 2. (a) Schematic of μLEDs. An image of the 2 $\times$ 2 cluster is also shown (b) μLED array with the daughter and motherboards.

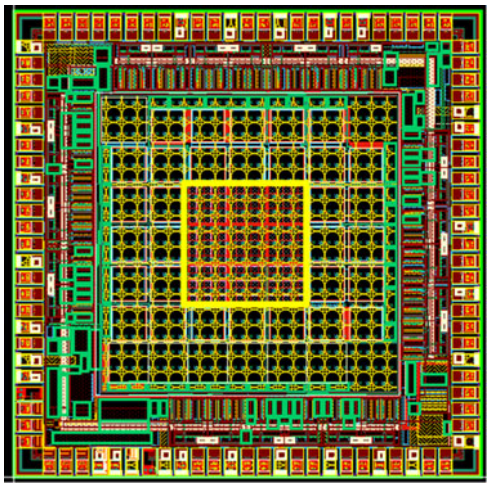


Fig. 3. Image of integrated APD array. APD used for the demonstrator are within the yellow square.

can be well-conditioned [14]. To achieve a full rank matrix in the imaging MIMO system, the image of more than one source should not fall entirely into the same receiver i.e.

$$\frac{p}{f} \leq \frac{s}{d}; \tag{1}$$

where s is the source spacing, p is the PD width, f is the focal length of the receiver optics system and d is the link length. The ratio (p/f) governs the receiver FOV of the imaging system.

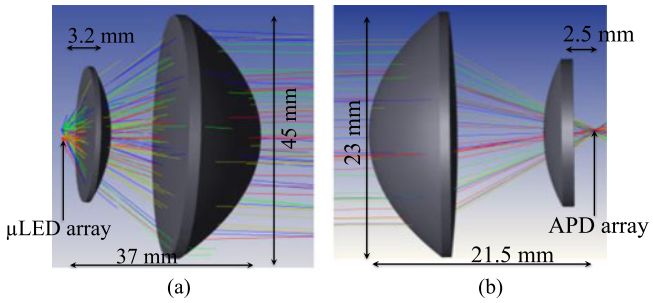


Fig. 4. Schematics of (a) transmitter optics and (b) receiver optics.

The transmitter and the receiver optical systems are designed using a combination of commercially available aspheric singlet lenses (see Fig. 4). The transmitter and receiver optics have apertures of 45 mm and 23 mm, respectively and the distances of 37 mm and 21.5 mm to the lenses front edge from μLED and PD, respectively. The optics system was optimized for a 4×4 imaging MIMO system using ray tracing software. However, there is a flexibility to adjust the optics for other MIMO configurations. The transmitter optics is designed to offer a full divergence angle of 7.5 degrees. The divergence angle and FOV are calculated based on a link budget analysis to offer at least 1 Gbps data rate at a 1 m link distance. The receiver optics does not only create an image of the LED array but also provides an optical gain. The receiver has full FOV of 3.5 degrees. The FOV of the receiver is limited by the number of available APDs in the array. In order to increase the FOV, a significantly larger array of APDs is required [23].

III. Experimental Set-Up

In this paper, we report a practical demonstration of the integrated four-channel MIMO-VLC system using state-of-the-art CMOS technology. We have also demonstrated four and nine-channel MIMO-VLC system driven using arbitrary waveform generator (AWG) that show the high-speed capacity of the system. A simplified block diagram of the MIMO-VLC experimental set-up using CMOS driver is shown in Fig. 5(a) and picture of the setup is given in Fig. 5(b). To achieve an aggregate data rate of 1 Gbps or higher, two DAC driver chips were required as the maximum sampling rate the Opal Kelly FPGA supports was limited to 375 MS/s. Each DAC chip drives two μLEDs in MIMO mode. The synchronization of the two driver chips was achieved by configuring them in a master-slave configuration where a 10 MHz clock from a master DAC chip was used as the reference clock for the slave chip.

In the AWG-based system, DAC drivers are replaced with AWGs (Agilent 81150A). One μLED in each cluster of four were used for nine-channel system whereas only μLEDs from corner clusters were used for the four-channel system (see Fig. 2(a)). The electrical outputs from the APDs were acquired using oscilloscopes for further offline processing which includes low pass filtering, equalisation and signal decoding. The four-channel MIMO systems were evaluated at a link distance of 1 m and the nine-channel system was evaluated at 0.5 m

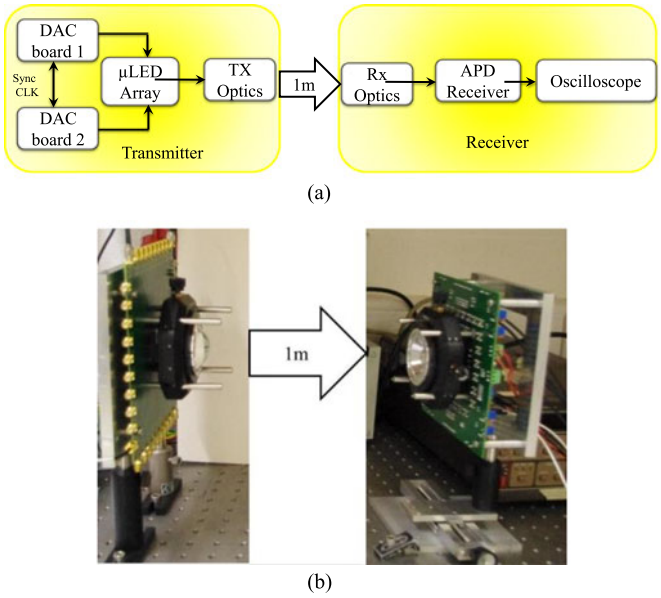


Fig. 5. (a) A simplified block diagram and (b) picture of the experimental set-up.

In a bandlimited MIMO system, both spatial (among MIMO channels) and temporal (intersymbol) interferences occur. To mitigate these interferences, a joint spatial and temporal decision feedback equalization (DFE) as outlined in [24] are adopted in this work.

IV. System Performance

The system under test is fully characterized and optimum operating conditions for both transmitter and receiver are determined. For data rate evaluation, a bit error threshold of 3.8×10^{-3} is adopted as recommended by ITU [25].

A. System Characterization

The measured intrinsic bandwidth and optical power of μLED device are shown in Fig. 6(a). The electrical-to-electrical (E-E) bandwidth and optical power of μLED increase with the driving current. The measured optical power at 100 mA current is $\sim$3.3 mW. The measured frequency response of the APD arrays is given in Fig. 6(b). Except for two APDs which show a resonant dip at 63 MHz, the remaining APDs have a bandwidth $>$90 MHz which is limited by parasitic capacitance. The resonant dips in these two APDs are possibly caused by them being close to the pads. Further investigation on the issue is being carried out and will be rectified in future iterations.

In order to determine if the DAC driver has any adverse effect on the system performance, the bandwidth of the system was evaluated by driving μLEDs with a DAC and with an AWG under similar bias current using sinusoidal signals of different frequencies. The sampling rate of the DAC is fixed to 250 MS/s whereas the AWG has a sampling rate of 2 GS/s. Fig. 7 shows the measured bandwidth of the complete system (μLED + APD). As expected, the bandwidth of the μLEDs increases with an increase in the average current (see Fig. 6(a)). It can be observed

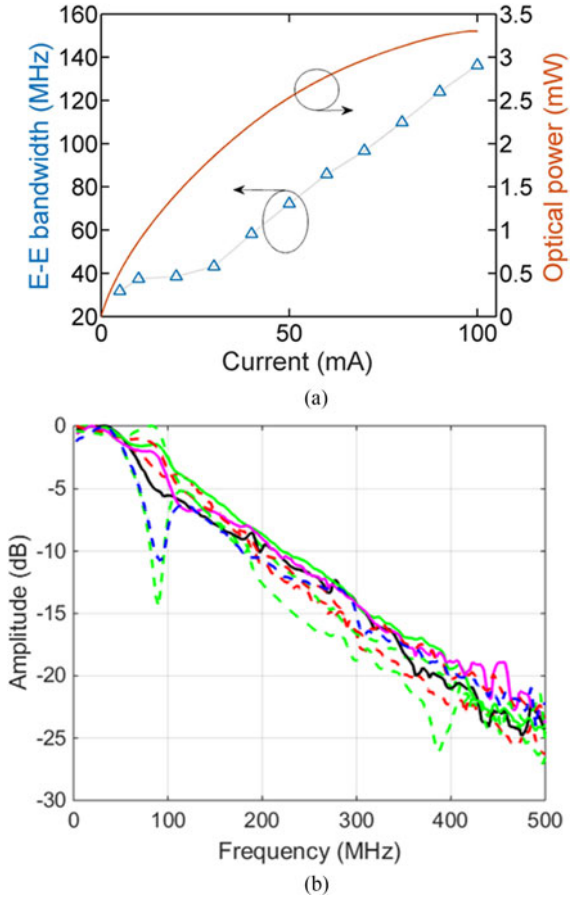


Fig. 6. (a) Electrical-to-electrical bandwidth and optical power against the bias current of μLED and (b) frequency responses of the APD array.

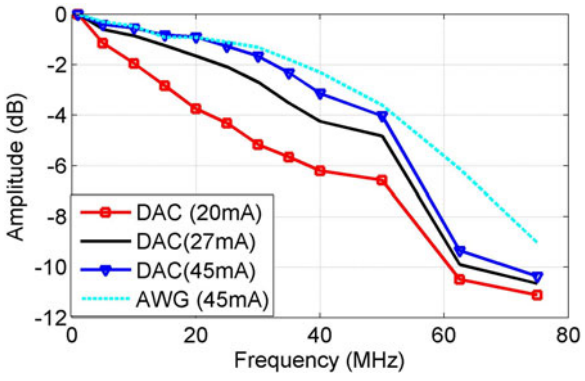


Fig. 7. Frequency responses of the MIMO-VLC system under the test.

that the DAC driver has a lower bandwidth than the AWG. The DAC output waveforms exhibit longer fall times than rise times as the CMOS driver has an active rise and passive fall due to the current-steering approach, which reduces the bandwidth. Nonetheless, the DAC does not significantly degrade the frequency response. For example, a -4 dB level is obtained at 52 MHz and 50 MHz for AWG and DAC, respectively ($\sim$4% difference). Note that frequency response beyond 50 MHz is not reliable for the DAC due to a low sampling rate. Based on this

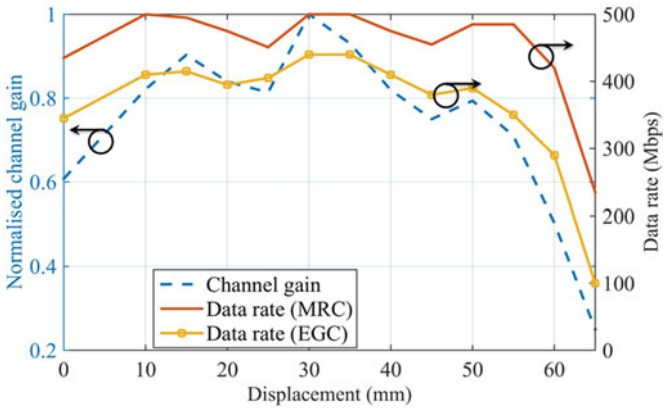


Fig. 8. The normalized total received power vs the horizontal displacements at a 1 m link distance.

result, the average current per LEDs was set to $\sim$45 mA for the results presented in the following sections.

B. System FOV

The overall FOV of the system (transmitter with the transmitter optics and receiver with the receiver optics) was evaluated by driving a single μLED and measuring the output signals from all APDs. The transmitter position was fixed while the receiver was displaced horizontally (perpendicular to the direction of propagation of light) in steps of 5 mm. The total received power was calculated by summing the APDs' output. The normalized total received power (i.e. DC channel gain) versus the horizontal displacement is shown in Fig. 8. The coverage diameter at 1 m distance is $\sim$60 mm, which corresponds to an overall system FOV of 3.45 degrees, limited by the number of available APDs. With a larger APD array, the FOV can be increased e.g. with an array of 5×5 APDs, the FOV is estimated to be $\sim$7 degrees. The maximum achievable data rate using maximal-ratio combining (MRC) and equal gain combining (EGC) methods are also shown in the figure for a 4-PAM scheme with DFE. As expected, MRC offers higher data rate than EGC. The maximum data rate achieved using EGC and MRC are of 440 Mbps and $\sim$500Mbps, respectively.

C. 4-channel MIMO Performance

1) DAC Drivers: To evaluate the performance of the full integrated MIMO system, four μLEDs were driven by two DAC drivers in the MIMO mode with independent data streams. The signals from all the APDs were captured and further processing (filtering, downsampling and equalization) was done offline. The aggregate data rates against the displacement of the MIMO system with 4-PAM modulation scheme is shown in Fig. 9. As it was not feasible to obtain an aggregate data rate beyond 750 Mbps for 2-PAM due to FPGA limitations, 2-PAM results are not presented here. The minimum and maximum data rates achieved were $\sim$1.23 and $\sim$1.3 Gbps, which correspond to a net rate of $\sim$1.14 and $\sim$1.21 Gbps respectively after 7% forward error correction (FEC) overhead reduction. The data rates with

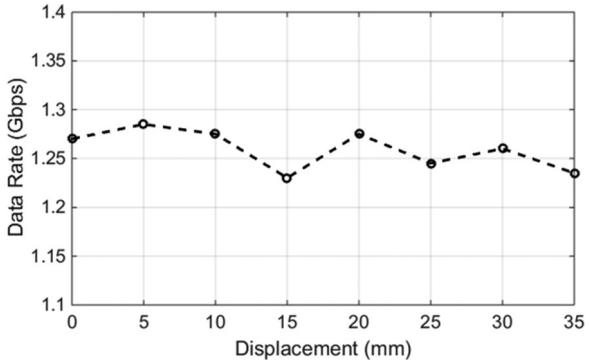


Fig. 9. The aggregate data rate vs the displacement of the integrated MIMO system with the DAC driver for 4-PAM.

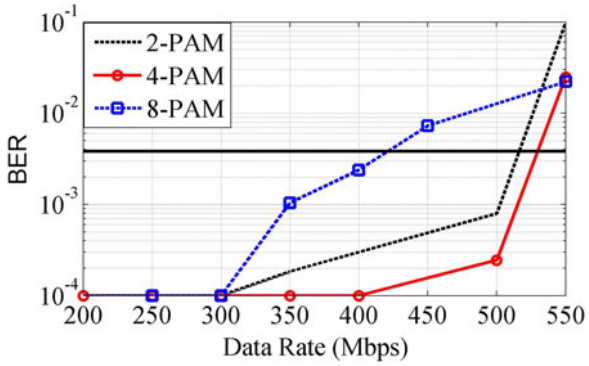


Fig. 10. The data rate vs BER for 2, 4 and 8-PAM with DFE, evaluated for a single channel at 1m link distance.

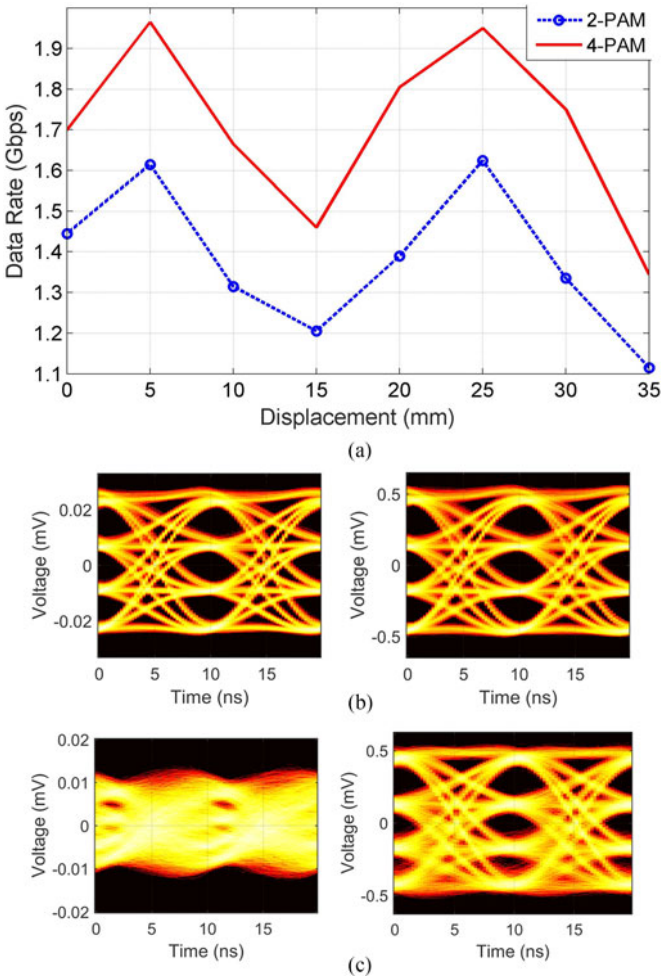


Fig. 11. (a) The aggregate data rates versus the displacement of the integrated MIMO system with the AWGs (b) eye-diagrams of the received 4-PAM signal at 200 Mbps (left) and after applying ZF (right) for channel 2 at a displacement of 5 mm and c) eye-diagrams of the received 4-PAM signal at 200 Mbps (left) and after applying ZF (right) for channel 2 at a displacement of 20 mm.

the DAC drivers were limited by the available sampling rate and lower bandwidth.

2) Waveform Generators: As outlined in [26], the optimum PAM level with a DFE depends on the ratio of the bandwidth and data rate, available signal-to-noise (SNR) and dynamic range. Hence, it is necessary to establish the optimum PAM level case-by-case basis as a generalized conclusion is difficult to draw. In order to determine the optimum PAM level, the BER performance of different PAM level under the identical operating condition is evaluated. Fig. 10 illustrates the data rate against BER of 2, 4 and 8-PAM with DFE, evaluated for a single channel (without any cross-talk) at 1 m link distance. This clearly demonstrates that 4-PAM offers the optimum performance closely followed by 2-PAM. 8-PAM offered a significantly lower BER performance.

The aggregate data rates against the displacement of the four-channel MIMO-VLC system with 2-PAM and 4-PAM modulation schemes for the experiments with AWGs is shown in Fig. 11(a). The minimum and maximum data rates achieved within the coverage area using 4-PAM are 1.35 and 1.96 Gbps (i.e. 1.25 and 1.8 Gbps, respectively after the 7% overhead FEC reduction). This corresponds to a maximum data rate of ∼500 Mbps per channel. Note that higher data rates (2 Gbps using pre-equalised 4-PAM [27] and 3 Gbps using OFDM [28]) were achieved using μLEDs. However, those demonstrations used significantly larger area PDs and bigger optical aperture; and hence had significantly higher SNR with limited FOV.

As shown in Fig. 11, there is a variation in the aggregate data rates within the FOV. The variation in data rates is due to: a) variation in inter-channel interference (ICI) and b) fill factor of APD array. It is feasible to design MIMO optical system with negligible cross-talk for a point-to-point link with the fixed transceiver position. However, when the transceiver positions are not fixed, the ICI (i.e. the condition number of the **H**-matrix and system capacity) depends on the relative position and orientation the transceiver. Secondly, the APD array has a fill factor of ∼80%. As the orientation of the transceiver changes, a significant proportion of the optical intensity may not be detected, this reduces the overall received power. For example, the overall channel gain (i.e. the sum of all the elements in **H**-matrix) at a displacement of 15 mm is 0.16 which is $\sim 11\%$ less than at 5mm where the channel gain is ∼0.18. However, the **H**-matrix condition numbers are 2.7 and 2.2 ($\sim 18\%$ variation) which significantly reduced the achievable data rate at 15 mm. On the other hand, the channel gain at 35mm is 0.12 and a significantly

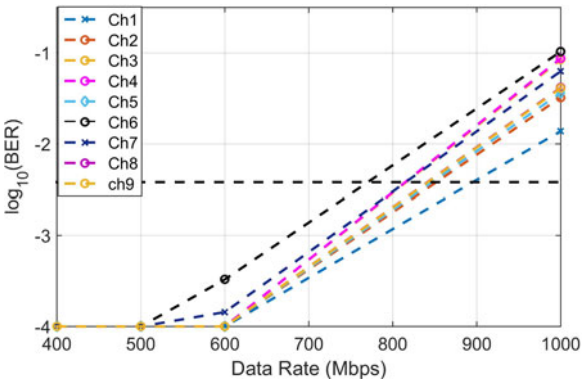


Fig. 12. The BER vs data rate for a 9 × 9 MIMO system with 8-PAM scheme at 0.5 m link distance.

lower data rate is expected. The optical cross-talk at different displacements is demonstrated by Fig. 11(b) and (c). Fig. 11(b) shows eye-diagrams of the received signal and the signal after applying zero-forcing (ZF) equalizer at 5 mm where the cross-talk is negligible. Hence, a clear eye-opening can be observed. On the other hand, Fig. 11(c) demonstrates that the signal recovery is not possible without an equalizer as the eye is completely closed due to ICI.

D. Nine Channel MIMO With AWGs

In order to demonstrate the feasibility of higher order, high-speed, dense spatial density MIMO system, a nine channel MIMO-VLC was studied. Nine is the maximum channel that the current set-up accommodates due to the limited number of available APDs. However, it is feasible to scale the system when the receiver with a higher number of APDs became available. To evaluate the performance of the 9×9 MIMO system, one μLED from each cluster of nine (see Fig. 2(a)) was driven by AWGs. The link distance was reduced to 0.5 m so that the imaging MIMO condition given by (1) was satisfied.

As in the case of 4-channel system, 2, 4 and 8- PAM with DFE were evaluated to determine the best performance. The 8-PAM offered the best performance, followed by 4-PAM as reducing link distance to half (0.5 m) increases the SNR by at least 6 dB (see [26] for a theoretical comparison PAM under different ISI and SNR).

The BER against the date rate for nine channel MIMO system for 8-PAM is given in Fig. 12. The BER for a channel was measured when all μLEDs corresponding to its neighboring channels were active so that the channel experiences the maximum possible inter-channel interference. For example, to estimate data rate for μLEDs in the top-left corner (Fig. 2(a)), all μLEDs except the one in the bottom-right corner were active. The signal from APDs was then captured and joint MIMO decoding algorithm was applied. Each channel can support data rates up to 890 Mbps. The aggregate data rate for the nine channels is 7.48 Gbps, which is ∼6.95 Gbps after removing 7% FEC overhead. Note that the FOV of the 9 channel MIMO system is significantly smaller (theoretically less than 8 mrad) due to a limited number of available APD.

V. Conclusions and Future Work

In this work, we have developed and demonstrated a complete integrated MIMO-VLC system that can support complex modulation schemes such as PAM and. Using two-dimensional arrays of μLEDs and APDs, and imaging optical system specifically designed for this purpose, combined with an imaging optical system, an integrated 4-channel MIMO system was demonstrated with aggregate data rates beyond 1 Gbps. Furthermore, we also we demonstrate a four-channel system with a minimum aggregate date rate of 1.35 Gbps and an FOV of 3.45 degrees at 1 m. This paper also shows the feasibility of a high-speed spatially dense nine-channel MIMO system that achieved data rates beyond 7 Gbps at a link distance of 0.5 m.

The FOV and range of the current system is limited due to the number of available APDs, as well as the source array size. Work to use WDM, improved receiver optics, more efficient sources, and novel receiver designs is underway. This will focus on achieving practical fields of view and coverage areas, whilst maintaining high data rates.

Acknowledgment

Associated data for the figures can be found at http://dx.doi.org/10.15129/bac75eed-3f9e-4a14-81f6-56f25d11138a.

References

[1] A. Jovicic, L. Junyi, and T. Richardson, "Visible light communication: Opportunities, challenges and the path to market," *IEEE Commun. Mag.*, vol. 51, no. 12, pp. 26–32, Dec. 2013.
[2] S. Rajbhandari *et al.*, "A review of gallium nitride LEDs for multi-gigabit-per-second visible light data communications," *Semicond. Sci. Technol.*, vol. 32, no. 2, pp. 1–44, 2017.
[3] H. Le Minh *et al.*, "100-Mb/s NRZ visible light communications using a postequalized white LED," *IEEE Photon. Technol. Lett.*, vol. 21, no. 15, pp. 1063–1065, Aug. 2009.
[4] H. Li, X. Chen, J. Guo, and H. Chen, "A 550 Mbit/s real-time visible light communication system based on phosphorescent white light LED for practical high-speed low-complexity application," *Opt. Express*, vol. 22, no. 22, pp. 27203–27213, 2014.
[5] F. Wu, C. Lin, C. Wei, and C. Chen, "1.1-Gb/s white-LED-based visible light communication employing carrier-less amplitude and phase modulation," *IEEE Photon. Technol. Lett.*, vol. 24, no. 19, pp. 1730–1732, Oct. 2012.
[6] A. M. Khalid, G. Cossu, R. Corsini, P. Choudhury, and E. Ciaramella, "1-Gb/s transmission over a phosphorescent white LED by using rate-adaptive discrete multitone modulation," *IEEE Photon. J.*, vol. 4, no. 5, pp. 1465–1473, Oct. 2012.
[7] H. Chun *et al.*, "LED based wavelength division multiplexed 10 Gb/s visible light communications," *J. Lightw. Technol.*, vol. 34, no. 13, pp. 3047–3052, Jul. 2016.
[8] Y. Wang, L. Tao, X. Huang, J. Shi, and N. Chi, "8-Gb/s RGBY LED-based WDM VLC system employing high-order CAP modulation and hybrid post equalizer," *IEEE Photon. J.*, vol. 7, no. 6, pp. 1–7, Dec. 2015.
[9] A. Burton, H. Minh, Z. Ghassemlooy, E. Bentley, and C. Botella, "Experimental demonstration of 50-Mbps visible light communications using 4×4 MIMO," *IEEE Photon. Technol. Lett.*, vol. 26, no. 9, pp. 945–948, May 2014.
[10] A. H. Azhar, T. Tran, and D. C. O'Brien, "A gigabit/s indoor wireless transmission using MIMO-OFDM visible-light communications," *IEEE Photon. Technol. Lett.*, vol. 25, no. 2, pp. 171–174, Jan. 2013.
[11] W. Yuanquan, C. Nan, Y. Wang, and N. Chi, "Demonstration of high-speed 2×2 non-imaging MIMO Nyquist single carrier visible light communication with frequency domain equalization," *J. Lightw. Technol.*, vol. 32, no. 11, pp. 2087–2093, Jun. 2014.

60 Mb/s, 2 metres Visible Light Communications in 1k Lux Ambient using an Unlensed CMOS SPAD Receiver

John Kosman[1,2], Oscar Almer[1], Aravind V. N. Jalajakumari[1], Stefan Videv[2], Harald Haas[2] and Robert K. Henderson[1], *(1) Institute for Integrated Micro and Nano Systems, (2) Li-Fi Research and Development Centre, Institute for Digital Communications, The University of Edinburgh, Edinburgh, UK (robert.henderson@ed.ac.uk)*

***Abstract*—We demonstrate an optical link operating in indoor ambient lighting conditions using a CMOS single photon avalanche diode (SPAD) optical receiver and a RGB light emitting diode (LED). The high sensitivity of the SPAD receiver allows the link to operate at 2 m distance at a total 60 Mb/s and bit error rate (BER) of 2×10^{-3} without lensing. The transmitter implements colour shift keying (CSK) using a custom 4-channel current mode CMOS digital to analog converter (DAC). The miniaturized, low cost components employed at transmitter and receiver are suited to integration in portable electronic devices or chip-in-a-bulb respectively.**

I. Introduction

The looming Radio Frequency (RF) spectrum crunch and fast growth of solid-state lighting technology have motivated next-generation optical wireless communication systems based on LED transmitters [1]. Visible Light Communications (VLC) or "LiFi" relies on white LEDs to provide communication and illumination simultaneously. Large-scale uptake of VLC technology will depend on cost-reduction and miniaturization of source and receiver components through integration in mainstream CMOS manufacturing technologies.

In this paper, we present the first measurements of a SPAD-receiver optical link operating at practical source-receiver separation, coverage and ambient indoor illumination condition. SPAD detectors have generated recent interest for VLC due to their high sensitivity and ready integration with on-chip digital signal processing [2][3]. However, these detectors are susceptible to saturation in high light conditions or pile-up linearity distortion so an investigation of their performance in practical scenarios is demanded.

We have furthermore chosen to evaluate our SPAD receiver without optics other than a bandpass filter to assess link performance without bulky optics which would dissuade incorporation in portable electronic devices.

II. Optical Link Design

An image of the optical link is shown in Fig. 1. An OSRAM Opto Semiconductors (LE RTDUW S2W) RGB LED is driven by a custom CMOS driver integrated circuit [4]. The LED is mounted with a parabolic reflector and diffuser conventionally found in domestic lighting fixtures.

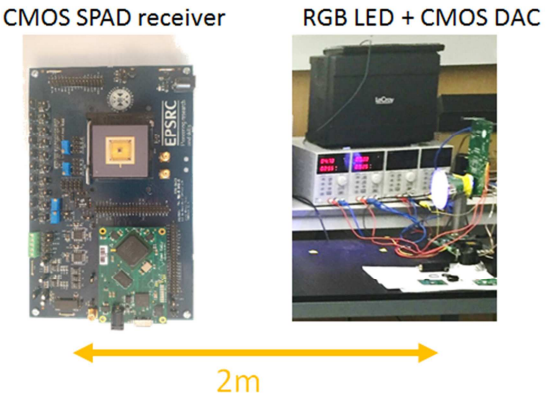


Fig. 1 SPAD VLC optical link

The half power semi-angle is 15° with a 30° full viewing angle. The LED is driven at 256mA from 10-bit, 200MHz DCO-OFDM modulated data sequences loaded into a Xilinx Spartan-6 field programmable gate array (FPGA) card (Opal Kelly XEM6310-LX150) over a USB3 link.

The SPAD receiver consists of an array of 4096 21 μm pitch, 43 % fill-factor SPADs implemented in a 130 nm CMOS image sensor technology [2]. These are arranged as 128 rows of 32 SPADs which are combined by XOR trees into a 128-input parallel adder tree generating a single 16-bit output data sequence. The chip comprises a PLL allowing up to 400 MHz sampling of the SPAD pulses. Data is broadcast off-chip via 4x 400 MHz sub-LVDS lanes to a Xilinx Spartan-6 field programmable gate array (FPGA) card (Opal Kelly XEM6310-LX150) and then to a PC over a USB3 link. Demodulation of the received data sequences is performed off-line using Matlab. The SPAD bias voltage (VHV), is set to 22 V, which corresponds to an excess bias of V_e = 1.5 V above the 20.5 V breakdown voltage of the diodes. At this setting the photon detection efficiency (PDE) of the SPADs is 25.9 % at 450 nm.

A black adhesive tape mask with a 4.6 mm diameter circular aperture was placed onto a bandpass optical filter [5]. This was centred above the 672 μm x 672 μm optically sensitive area of the SPAD receiver chip reducing the FOV of the receiver to 15°. Three bandpass optical filters were interchanged successively corresponding to each of individual RGB channels of the LED (Thorlabs FB450-10, FB520-10, FL632.8-10). The SPAD receiver chip was otherwise unlensed.

III. Experiment and discussion

.

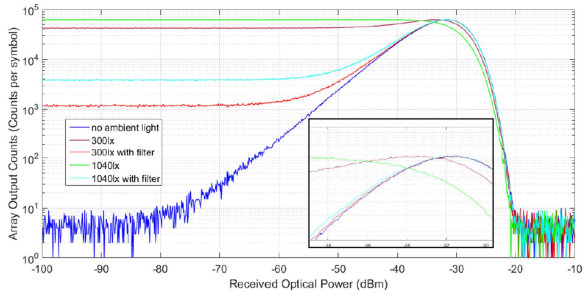


Fig. 2 Photon transfer curve of SPAD receiver under different ambient light conditions

The influence of background light is investigated by sweeping the intensity of the red LED at different indoor lighting conditions. The SPAD sensor is operated at a 1MHz sample rate. It can be seen from Fig. 2 that without optical filter the SPADs are completely saturated at 1040 lux. The red filter and narrowed field of view manage to restore around 2 decades of linearity compared to the 5 decades in darkness.

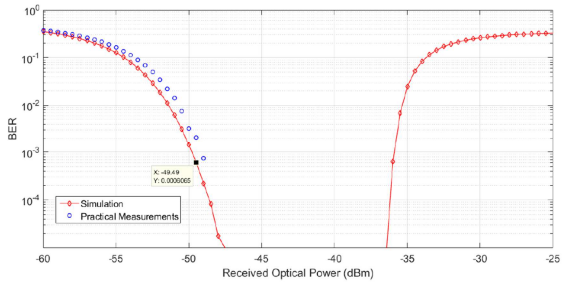


Fig. 3 BER simulation results compared with measurements of red LED link

The SPAD receiver is operated at 100 MHz sampling rate using the red LED channel placed 2 m away (Fig. 3). We achieve a data rate of 20 Mbit/s at BER = 0.91×10^{-3} in 1040 lux ambient lighting at a sensitivity of -49.4dBm using 4-QAM DCO-OFDM. These measurements correspond very closely to a system model implemented using Zemax [5]. With the same link settings, at 20 Mbit/s BER of 9.8×10^{-4} was measured with the 450nm blue filter, and a BER of 1.02×10^{-3} with the 520nm green filter making. Thus a total of 60 Mbit/s would be achievable with three receiver chips with three different color filters.

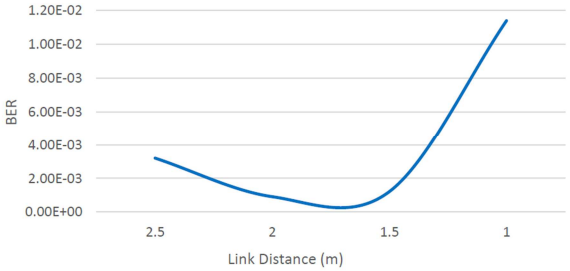


Fig. 4 BER against link distance

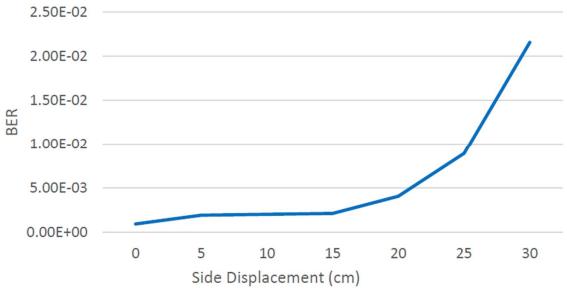


Fig. 4 BER against off-axis lateral displacement at 2 m link distance

Figs. 3 and 4 show the robustness of the link (red filter) against x, y and z displacement from the receiver. A BER of 3×10^{-3} or lower can be attained over link distances between 1.5 m to 2.5 m. At distances less than 1.5 m the nonlinear distortion and saturation of the SPADs greatly increases in the error rate. A maximum lateral displacement of 15 cm is tolerable whilst maintaining a BER of 3×10^{-3}, equivalent to a field of view of 4.3°.

IV. Conclusions

A CMOS SPAD receiver can be rendered robust against practical ambient light levels by simple filtering and restricted field-of-view. The high receiver sensitivity enables lensless, miniaturizable, low-cost VLC systems at data rates suitable for future Internet of Things (IoT) or LiFi networks.

Acknowledgements

The UK Engineering and Physical Sciences Research Council (EPSRC) project EP/K00042X/1. STMicroelectronics for chip manufacture.

References

[1] S. Dimitrov and H. Haas, Principles of LED Light Communications: Towards Networked Li-Fi. Cambridge, U.K.: Cambridge Univ. Press, Mar. 2015.

[2] O. Almer, D. Tsonev, N. A. W. Dutton, T. Al Abbas, S. Videv, S. Gnecchi, H. Haas, and R. K. Henderson, "A SPAD based Visible Light Communications Receiver Employing Higher Order Modulation," in Global Communications Conference (GLOBECOM), 2015 IEEE, Dec 2015.

[3] D. Chitnis and S. Collins, "A SPAD-Based Photon Detecting System for Optical Communications," Lightwave Technology, Journal of, vol. 32, pp. 2028–2034, May 2014

[4] A. Jalajakumari, D. Tsonev, K. Cameron, H. Haas, and R. Henderson, "An energy efficient high-speed digital LED driver for visible light communications," in Communications (ICC), 2015 IEEE International Conference on, June 2015, pp. 5054–5059.

[5] J. Kosman "Optical OFDM Communications with Single Photon Avalanche Diode Receivers", MEng Thesis, University of Edinburgh, 2016.

High-Speed Integrated Visible Light Communication System: Device Constraints and Design Considerations

Sujan Rajbhandari, *Member, IEEE*, Hyunchae Chun, Grahame Faulkner, Katherine Cameron, Aravind V. N. Jalajakumari, Robert Henderson, Dobroslav Tsonev, *Member, IEEE*, Muhammad Ijaz, Zhe Chen, Harald Haas, *Member, IEEE*, Enyuan Xie, Jonathan J. D. McKendry, *Member, IEEE*, Johannes Herrnsdorf, Erdan Gu, Martin D. Dawson, *Fellow, IEEE*, and Dominic O'Brien, *Member, IEEE*

***Abstract*—Visible light communications (VLC) has the potential to play a major part in future smart home and next generation communication networks. There is significant ongoing work to increase the achievable data rates using VLC, to standardize it and integrate it within existing network infrastructures. The future of VLC systems depends on the ability to fabricate low cost transceiver components and to realize the promise of high data rates. This paper reports the design and fabrication of integrated transmitter and receiver components. The transmitter uses a two dimensional individually addressable array of micro light emitting diodes (μLEDs) and the receiver uses an integrated photodiode array fabricated in a CMOS technology. A preliminary result of a MIMO system implementation operating at a data rate of 1 Gbps is demonstrated. This paper also highlights the challenges in achieving highly parallel data communication along with the possible bottlenecks in integrated approaches.**

***Index Terms*—Visible light communications, optical communication system design, multiple input multiple output, optical wireless communications, link budget analysis, integrated optical system design.**

I. Introduction

THERE has been significant research interest in visible light communications (VLC) in the last decade. This is largely due to the possibility of using general illumination light-emitting diode (LED) devices for data communications. The LED is expected to dominate the illumination market by 2020 [1], and can be used for high speed data communications [2]. VLC using LEDs offers many advantages including license free operation, high spatial diversity and innate security.

Two methods of generating white light are commercially popular: a) an RGB method in which light from red, green, and blue LEDs are mixed, resulting in a white color and b) a phosphor conversion method, in which a yellow phosphor absorbs a portion of the blue light emitted by a Gallium Nitride (GaN) LED and re-emits a broad yellow spectrum, which when mixed with the blue wavelength results in a white color. Commercially available illuminations LEDs usually use the phosphor conversion method due to its low cost.

Phosphor based LEDs, however, have low communication bandwidths (a few MHz) due to the long photoluminescence lifetimes of the phosphor [3]. Typically a narrowband short pass optical filter is used at the receiver to the reject the slow yellow component of the received light. The bandwidth of the blue LED, on the other hand, is limited to 20–30 MHz [3] which is a possible bottleneck for high speed data communications. Recently, it has been shown that GaN-based blue-emitting micro-LEDs (μLEDs) can offer optical modulation bandwidths in excess of 400 MHz [4]. Error-free data transmission up to 1 Gbps and 3 Gbps using these μLEDs was demonstrated using on-off keying (OOK) and orthogonal frequency division multiplexing (OFDM) [5], respectively. Although these experiments were carried out over a short distance due to the limited optical power available, these results nonetheless demonstrate the potential of the GaN based μLEDs to offer high-speed communication. The ultimate solution for VLC may be to use an array of these smaller, less powerful μLEDs as building blocks [6].

Work to explore the potential of these devices is ongoing under the Engineering and Physical Sciences Research Council (EPSRC) 'ultra-parallel visible light communications (UP-VLC)' project. The project aims to develop a high speed, highly parallel VLC system that can offer Gbps data rates. This paper focuses on communication using blue μLEDs. Other work in the project focuses on combining light from such devices with high bandwidth color converters [7] to create white light. Ultimately the combination of such color converters and large arrays of μLEDs offers the potential to combine very high data rate communication and illumination in a single transmitter.

Manuscript received May 10, 2014; revised November 13, 2014; accepted April 13, 2015. Date of publication May 14, 2015; date of current version August 17, 2015. This work was supported by the UK Engineering and Physical Sciences Research Council (EPSRC) under grant EP/K00042X/1.

S. Rajbhandari, H. Chun, G. Faulkner, and D. O'Brien are with the Department of Engineering Science, University of Oxford, Oxford OX1 3PJ, U.K. (e-mail: sujan.rajbhandari@eng.ox.ac.uk; hyunchae.chun@eng.ox.ac.uk; grahame.faulkner@eng.ox.ac.uk; dominic.obrien@eng.ox.ac.uk).

K. Cameron, A. V. N. Jalajakumari, and R. Henderson are with CMOS Sensors & Systems Group, The University of Edinburgh, Edinburgh EH9 3JL, U.K. (e-mail: K.Cameron@ed.ac.uk; A.Venugopalan@ed.ac.uk; Robert.Henderson@ed.ac.uk).

D. Tsonev, M. Ijaz, Z. Chen, and H. Haas are with the Institute for Digital Communications, Li-FI R&D Centre, The University of Edinburgh, Edinburgh EH9 3JL, U.K. (e-mail: d.tsonev@ed.ac.uk; m.ijaz@ed.ac.uk; z.chen@ed.ac.uk; h.haas@ed.ac.uk).

E. Xie, J. J. D. McKendry, J. Herrnsdorf, E. Gu, and M. D. Dawson are with the Institute of Photonics, University of Strathclyde, Glasgow G1 1XQ, U.K. (e-mail: enyuan.xie@strath.ac.uk; jonathan.mckendry@strath.ac.uk; johannes.herrnsdorf@strath.ac.uk; erdan.gu@strath.ac.uk; m.dawson@strath.ac.uk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSAC.2015.2432551

The focus in this paper is on the design of the transmitter and the receiver components and on possible approaches for achieving a high-speed data link. The target of the first UP-VLC demonstrator is to realize a 1 Gbps unidirectional data link over a 1 m distance at error rate of 10^{-6}. Links offering similar data rates have been achieved using low bandwidth commercial white LEDs [8]–[10], albeit at a bit error rate (BER) floor of ~10^{-3}. In our case relatively modest data rates were chosen as a target for this initial demonstration, as the focus is to develope integrated components suitable for scaling to much higher data rates in subsequent demonstrators.

Although μLEDs have higher bandwidth than commercial devices, arrays of devices are required to support the target data rates due to the limited optical power available from individual devices. Three approaches are investigated here;

a) A ganging approach: all μLEDs in the array carry the same data
b) A multiple input multiple output (MIMO) approach: each μLED in an array carries an independent data stream
c) A hybrid approach, which combines a) and b)

The MIMO system can offer a linear increment in data rate with number of transmitters but requires channel separation using imaging/non-imaging optics and MIMO data decoding algorithms.

The ganging approach offers simplicity in design as simple receiver circuitry can be used but does not offer a linear increase in data rate with the number of transmitters. The hybrid approach combines the advantage of both approaches. The system components can also implement different transmission schemes including spatial modulation [11], and optically generated modulation [12]. All these approaches will be implemented within the project.

The performance of a VLC system is a function of the constraints of the transmitter (the LED diameter, optical power, and bandwidth) and receiver (photodiodes area and bandwidth/area/sensitivity relationship). In this paper, we report a design approach that includes these constraints and allows the overall optimum configuration to be determined. To our knowledge, this is the first report of such a method.

The paper is organized as follows: Section II gives an overview of the system being developed. Section III details the approach taken to select the device parameters. Optical and electronic system designs are outlined in Sections IV and V, respectively. The experimental results are presented in Section VI. Finally, the conclusions and future work are given in Section VII.

II. System Description

Fig. 1 shows a conceptual block diagram of the system under development. The transmitter consists of a 2-D array of μLEDs operating at a wavelength of 450 nm. These μLEDs are driven by complementary metal-oxide-semiconductor (CMOS) drivers. The μLEDs are Lambertian sources with a divergence angle of 120 degrees (full-angle). Transmitter optics reduces the divergence angle and hence reduces the path loss. Imaging optics at the receiver maps the μLED array to the photodiode (PD) array. For minimum cross-talk between the MIMO channels in an imaging system, the PDs and the μLEDs pitch sizes must be matched. The ganging scheme does not require imaging optics, and a diffuser can be used after the transmitter optics to provide the desired FOV (details of optics designs are given in the following sections).

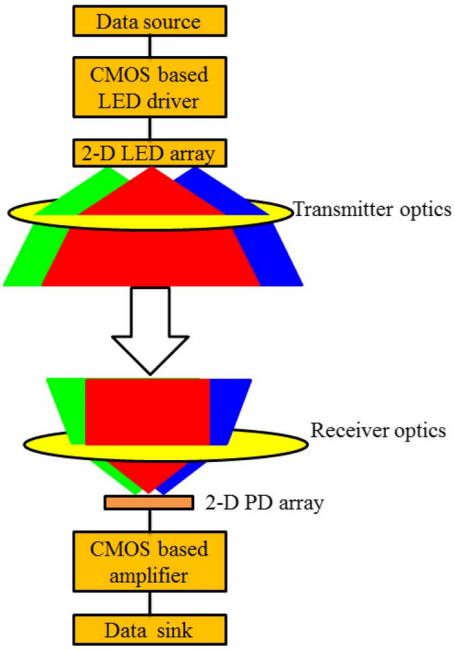


Fig. 1. A conceptual block diagram of the VLC system (different colours are used for illustration only. The central wavelength of μLEDs considered in this design is 450 nm).

At the receiver, the PDs photocurrents are converted to a voltage using transimpedance amplifiers (TIA) and are either summed (for ganging) or processed separately (for MIMO). The MIMO receiver can overcome any crosstalk by estimating the channel H-matrix and recover data using MIMO data decoding algorithms. The details of the MIMO decoding algorithm can be found in [13], [14].

III. Design Methods: System Constraints and Parameter Selections

Both μLEDs and PDs have constraints which need to be considered in the system design. By incorporating the power penalty for multilevel PAM (L-PAM), μLED constraints (bandwidth-power relationship) and PD constraints (area-bandwidth relationship), it is feasible to optimize the device parameters and modulation level to achieve the target data rate with a minimum number of transmitter and receiver elements. The details of the devices selection and link budget analysis are given in the following sections. For simplicity, only a line-of-sight (LOS) link is considered in the design, and only L-PAM is considered. However, the design method has flexibility to incorporate equalization and other complex modulation schemes.

A. Selection of Device Parameters

In order to establish the optimum μLED parameters (i.e., size, power and bandwidth) for the targeted data rate, the

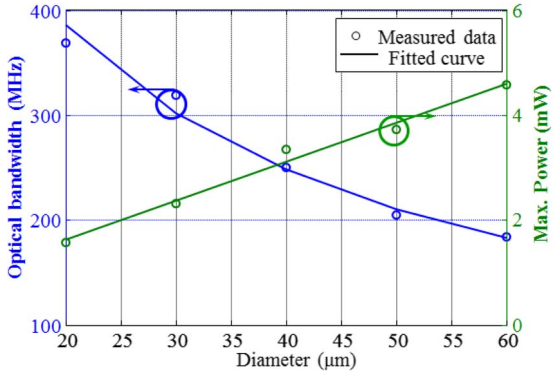


Fig. 2. The relationship among the optical bandwidth, optical power and μLED diameter. The measured data and fitted curves are also shown.

interdependency between power and bandwidth of μLED is investigated. Fig. 2 shows the measured optical bandwidth and the maximum optical power for blue μLEDs with different diameters. It can be seen that there is an approximately inverse linear relationship between the maximum optical power and bandwidth, both of which are a function of the μLED diameter. For the blue μLEDs reported in [4], the following equations approximately describe the relationship between the μLEDs diameter d_{LED}, maximum optical power P_{opt} and optical bandwidth B_{opt} (valid for μLEDs with a diameter of 20–80 μm):

$$P_{\text{opt}}[\text{mW}] = \frac{1013}{B_{opt}[\text{MHz}]} - 0.985; \tag{1}$$

$$P_{\text{opt}}[\text{mW}] = 0.0743 d_{LED}[\mu m] + 0.132 \tag{2}$$

The bandwidth and power requirements for a link depend on: a) the target data rate, b) the required order of the multilevel modulation scheme and c) the system configuration (ganging, MIMO). The MIMO scheme requires lower bandwidth μLEDs as the data rate per MIMO channel can be made significantly lower than the aggregate data rate. For the ganging scheme, the bandwidth requirement can be reduced by increasing the number of levels in a multilevel modulation scheme, at the cost of a higher optical power requirement. Hence, the optimum bandwidth and power requirements for the MIMO and the ganging configurations are different and can only be established by taking into account the device constraints and the modulation scheme.

There are also device constraints at the receiver. For a CMOS PD, the relationship between the PD capacitance C_{PD} and area Area_{PD} can be expressed as [15]:

$$C_{\text{PD}} = \frac{\text{Area}_{\text{PD}} C_J}{\left(1 + \frac{V}{V_B}\right)^{M_J}} + \frac{\mathcal{P} C_{\text{JSW}}}{\left(1 + \frac{V}{V_B}\right)^{M_{\text{JSW}}}}; \tag{3}$$

where C_J is junction capacitance, C_{JSW} is sidewall junction capacitance, M_J is junction grading coefficient, M_{JSW} is sidewall junction grading coefficient, V_B is junction potential and $\mathcal{P}$ is the perimeter. In a shallow junction photodiode, as is considered here, the area component is dominant leading to $C \propto \text{Area}_{\text{PD}}$.

There are a number of different TIA designs that can be used. In [16] chapter 4, it was shown that for a fixed power consumption the shunt-shunt feedback topology (Fig. 3) will have better noise performance than alternatives. As the noise performance is critical, this design is used. In this case the bandwidth B_{TIA} is given by [16]:

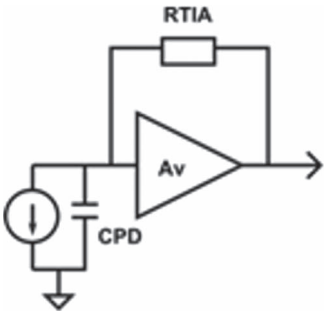


Fig. 3. The schematic of shunt-shunt feedback TIA topology. CPD, the capacitance of the photodiode, is assumed to be the dominant input capacitance.

$$B_{\text{TIA}} = \frac{A_V}{2\pi R_{TIA} C_{\text{PD}}}; \tag{4}$$

where A_V is the voltage gain of the amplifier used in the TIA and R_{TIA} is the feedback resistance. Therefore:

$$B_{\text{TIA}} \approx \frac{A_V \left(1 + \frac{V}{P_B}\right)^{M_J}}{\text{Area}_{\text{PD}} C_J (2\pi R_{TIA})} = \frac{K}{\text{Area}_{\text{PD}}}; \tag{5}$$

where P_B is junction potential and K is a constant whose value is dependent on process parameters and TIA gain/structure.

It can be seen that bandwidth is inversely proportional to area. As the received power is a function of the receiver collection area, this relationship must be taken into account.

B. SNR Analysis of L-PAM Considering Transmitter and Receiver Constraints

PAM is one of the most popular modulation schemes in VLC systems. PAM is attractive because of the simplicity in the transmitter and receiver design.

Multilevel modulation requires higher received optical power to achieve the same bit rate and error performance as binary modulation, but offer a reduction in the bandwidth requirement.

In this paper, designs using L-PAM is considered. To achieve a data rate of R_b in an additive white Gaussian noise (AWGN) channel, the bandwidth B and optical power penalty P_{pb} for L-PAM to achieve a desired error probability relative to OOK is given by [17], [18]:

$$B = \frac{1}{M} \tag{6}$$

$$P_{\text{pb}} = \frac{(L-1)}{\sqrt{M}}; \tag{7}$$

where $L = 2^M$ and M is a positive integer.

The error probability is a function of available electrical SNR which is defined as [18], [19]:

$$\text{SNR}_{\text{available}} = \frac{(RP_r)^2}{\sigma_a^2} = \frac{(RH(0)P_T)^2}{N_0 B} = K_1 \frac{P_T^2 \text{Area}_{\text{PD}}^2}{B}; \tag{8}$$

where R is the PD responsivity, P_T and P_r are the average transmitted and received optical power respectively, σ_a^2 is the amplifier noise variance, N_0 is the double-sided noise power-spectral, K_1 is a constant and $H(0)$ is the channel DC gain. This is a function of propagation distance d, incident angle Φ and order of Lambertian emission m, and is given by:

$$H(0) = \frac{\text{Area}_{\text{PD}}(m+1)}{2\pi d^2}\cos^m(\Phi). \tag{9}$$

Therefore, the available SNR, considering the transmitter and receiver constraints in (1) and (5) is given by:

$$\text{SNR}_{available} \propto \begin{cases} B^{-3} & \text{considering only(5)} \\ B^{-5} & \text{considering (1) and (5)} \end{cases}; \tag{10}$$

Considering the receiver system constraints in (5), the available SNR for L-PAM normalized to that of OOK for a given optical power is given by:

$$SNR_{L-\text{PAM}} = M^3. \tag{11}$$

As indicated from (7), L-PAM requires an additional SNR of $(L-1)^2/M$ to achieve the same bit error rate (BER) as OOK. Assuming the PD area can be adjusted to match the bandwidth requirement for L-PAM, the receiver system can offer an SNR improvement of M^3. Hence L-PAM offers an SNR gain in comparison to OOK if the available SNR gain is higher than the additional SNR requirements i.e.

$$M^3 > \frac{(L-1)^2}{M}. \tag{12}$$

This condition is satisfied for $M < 5$ and a maximum SNR gain $[M^3 - \{(L-1)^2/M\}]$ of 2.5 dB is obtained for 4-PAM. This indicates that 4-PAM requires the minimum transmitted power to achieve the target data rate and BER as long as the PD area can be varied to match the required system bandwidth.

In obtaining (13), the transmitter device constraints are not included in the analysis i.e. it is assumed that the transmitted power is fixed. In our design, it is feasible to manufacture a μLED that can match the system requirements. Hence, the μLED's bandwidth and power constraints can also be included within the link budget analysis. By incorporating transmitter constraints (1) in (9), it can be shown that L-PAM offers an SNR gain if:

$$M^5 > \frac{(L-1)^2}{M}. \tag{13}$$

This condition is satisfied for $M < 10$ and a maximum SNR gain of 12.6 dB is obtained for 16-PAM.

The analysis here is limited to PAM based modulation without an equalizer. The equalization and complex modulation schemes like OFDM offers further improvement in system performance. The analysis of power requirement for equalization and OFDM is beyond the scope of the paper. Interested reader can refer to [20]–[22]. However, the demonstrator allows these schemes to be implemented, so that detailed experimental comparisons can be made.

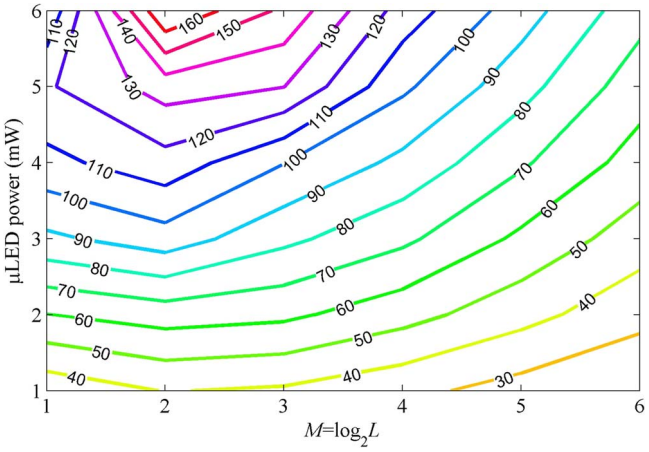


Fig. 4. A contour plot of the maximum achievable data rates (Mbps) using L-PAM for different μLED powers.

TABLE I
DESIGN PARAMETERS OF VLC DEMONSTRATOR-I

Parameters		Values	
		Ganging	MIMO
Data rate (Gbps)		>1	>1
Link Length (m)		>1	>1
Number of parallel channel		1	4
μLEDs	Array size	6×6	6×6
	Wavelength (nm)	450	450
	Diameter (μm)	24	39
	Optical power (mW)	2	3
	Bandwidth (MHz)	175	125
	Pitch size (mm)	0.3	1.5
Transmitter optics	Divergence angle (full)	10°	7.5°
Receiver Optics	FOV (full angle)	8°	3°
	Gain (maximum)	296	1182
Photodiode (APD)	Array size	3×3	3×3
	Width (μm)	200	200
	Pitch length (μm)	240	240
	Responsivity @ 450 nm (A/W)	2.41	2.41
	Bandwidth (MHz)	175	175

C. Approaches to Achieve Higher Data Rate: Ganging and MIMO

Fig. 4 shows the maximum achievable data rates at a 1 m link distance using a single μLED and a single PD. The link budget analysis assumes a target BER of 10^{-6}, a 10 dB link margin and a divergence/FOV of 5 degrees (half angle). As predicted from (12), 4-PAM requires the minimum power to achieve the desired data rate. Though the lower power μLEDs have higher bandwidth, there is not enough link margin to support higher data rates.

In order to achieve a target data rate of 1 Gbps, either ganging or MIMO approaches are required. The optimum device parameters for these approaches are established based on the analysis detailed in previous sections and summarised in Table I.

IV. Demonstration Optics Design

Imaging MIMO systems are reported in [11], [23]. The work reported in [11] provides the theoretical capacity of such a system based on the assumptions that the receiver image is an orthographic projection of the transmitted image. An optical design for an integrated angle diversity imaging receiver is also reported in [24]. In this paper we focus on designs that use commercially available optical components for both the MIMO and ganging schemes. In order to achieve a common optical design the constraints for both schemes need to be considered. Both imaging and non-imaging optical concentrators can be used in the ganging scheme. Though the non-imaging concentrator can provide optical 'gain' close to the theoretical limit set by the constant radiance theorem, the channel H-matrix is ill-conditioned in a non-imaging MIMO system [25]. The H-matrix must be of full rank in order to successfully separate the MIMO channels at the receiver. To achieve this in an imaging MIMO system, the image of more than one source should not fall entirely into the same receiver and hence the imaging MIMO system must satisfy the following condition:

$$\frac{p}{f} \leq \frac{s}{d}; \tag{14}$$

where s is the source spacing, p is the PD width, f is the focal length of the receiver optics system and d is the propagation length. The ratio (p/f) also governs the receiver FOV of the imaging system. The maximum detector area for the target data rate is established from the area-bandwidth relationship (see analysis in Section III). Hence, a higher FOV can be achieved only by reducing the focal length. However, due to physical constraints, it is not feasible to design a lens system with larger input aperture but smaller focal length (note that the optical 'gain' depends on the input aperture and high gain is desirable). Hence there is a trade-off between the optical "gain" and the FOV.

The FOV for an individual PD in imaging system is limited. In order to increase the FOV, the number of PDs is made significantly greater than the minimum requirement for a point-to-point link. For a larger FOV, the desired PD number can be in the order of thousand [26]. Increasing the number of receiver elements also increases the receiver complexity and the cost. With the integrated approach taken here, it is believed that the system is scalable to accommodate a large number of PDs.

The specification for demonstrator-I is a 3×3 array of PDs with dimensions of 200×200 μm^2 on a 240 μm pitch (details of these PD are given in the following sections). This gives a full FOV of 3 degrees for a lens system with $f = 11$ mm. A larger PD array system will be fabricated in the next phase of the project once the initial assumptions and designs are tested and verified. Increasing the number of PDs will increase the FOV and hence will reduce the need to align the transmitter and receiver.

Considering the constraints imposed by (14), the minimum desirable distance between the transmitter elements is 44 mm. In order to limit the chip size, the transmitter optics has been designed in such a way that it generates a virtual image of transmitters with the desired pitch.

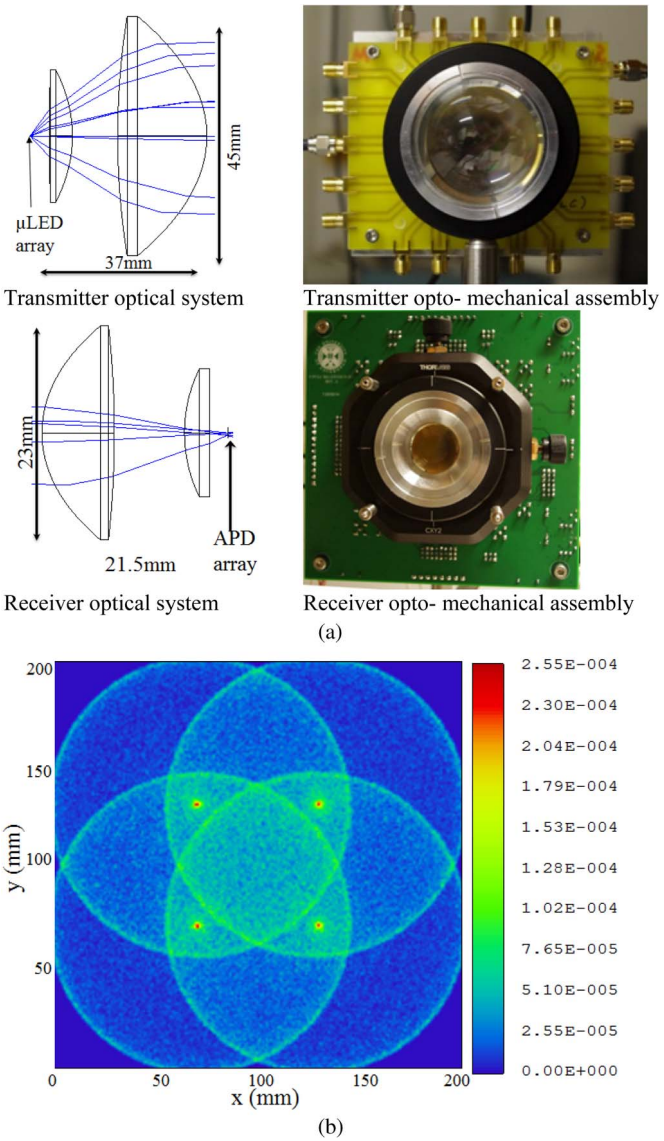


Fig. 5. a) Schematic of optical system and snapshot of the opto-mechanical assemlies. b) simulated optical irradiance (W/cm^2) in a 200×200 mm^2 receiver plane at 1 m distance from the transmitter.

The transmitter optics also limits the divergence angle of the μLED so that the geometric loss can be minimised. The Lambertian emission of the μLED means that a high numerical aperture optical system is required, and a suitable system was designed and optimised using ray-tracing software. The final optical designs and their mechanical assemblies for the MIMO system are shown in Fig. 5(a). Fig. 5(b) shows the optical irradiance at a 1 m distance on a 200×200 mm^2 plane. The transmitter is designed to offer a full divergence angle of 7.5 degrees and an overlapping area of 4.5 degrees, where all the MIMO channels will operate. Note that a MIMO system can operate only in the central overlapping area where all four MIMO channels overlap. The receiver has full FOV of 3 degrees. For the ganging system, an appropriate holographic diffuser is used to create a transmitter beam with a divergence angle of 10 degrees.

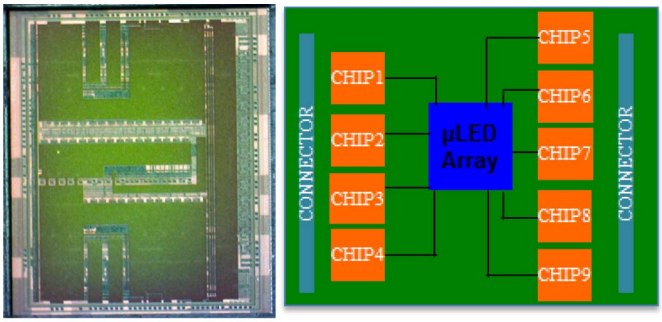


Fig. 6. μLED driver a) fabricated die and b) transmitter PCB block diagram.

V. Electronics Design

A. Transmitter Subsystem

This consists of μLED driver chips, the μLED array and associated printed circuit board (PCB). The μLED driver chip is implemented in an Austria Micro Systems 0.18 μm CMOS process, building on previous designs [4]. Circuit specifications were derived from system level simulations and calculations mentioned in previous sections. Each driver chip consists of 4 independent μLED drivers, interfacing and configuration circuitry. The chip also has an internal buffer/de-serializer to support ganging/MIMO operation. Chip configuration can be performed through the serial interface provided. An n-channel metal-oxide semiconductor (NMOS) transistor based circuit is used to drive the μLEDs, because of the higher carrier mobility and lower area requirement compared with p-channel MOS (pMOS) transistors. Each driver channel can sink an LED drive current up to 255 mA, and is designed to operate at a bandwidth of up to 250 MHz.

Fig. 6 shows driver chip block diagram and photograph of the fabricated chip. Nine driver chips and a 6 × 6 μLED array are interconnected through the transmitter PCB (Fig. 6(b)), which also mounts the transmitter optical assembly. Separate data interface PCBs can be attached to the transmitter PCB for ganging and MIMO operation.

B. μLEDs

Both ganging and MIMO μLED devices consist of an array of individually-addressable 6 × 6 elements in a flip-chip configuration. In order to be compatible with the NMOS-based CMOS driver, each μLED element in these devices has an individual n-type contact, whereas all elements share a common p-contact. The disk-shaped μLED element has a diameter of 24 μm for the ganging and 39 μm for the MIMO device. As shown in Fig. 7(a), the ganging μLED array has a uniform pitch of 300 μm. In order to match the transmitter pitch to that of the receiver, the MIMO array is arranged such that the elements are grouped into 2 × 2 clusters with a pitch of 69 μm between two adjacent μLED elements. There is a separation between the end-to-end elements of 1500 μm (see Fig. 7(b)). The four closely clustered μLED elements also provide the ability of operating in a hybrid mode, as described earlier.

These devices are fabricated on commercial blue InGaN/GaN LED wafers grown on c-plane (0001) sapphire substrates with a 450 nm peak emission wavelength and 20 nm full width at half maximum. In a first step, 6 × 6 mesa structures are deeply etched down to the sapphire substrate by Cl_2-based inductively coupled plasma etching. Then a second etch step defines the μLED elements on each mesa. These steps allow each LED element to be addressed by its own n-contact appropriate for driving with an NMOS-based CMOS driver. A thermally annealed Pd layer with over 50% reflectance at 450 nm is used as the metal contact to p-type GaN. A metal bilayer of Ti/Au serves as the metal contact to n-type GaN and metal tracks. After the μLED fabrication, the ganging and MIMO devices are bonded to the backside of a 132-pin package using Norland optical adhesive and then wire bonded. This backside arrangement reduces the separation between light emission surface (sapphire surface) and the optical system. Finally, the bonded device is contacted with a copper heat sink.

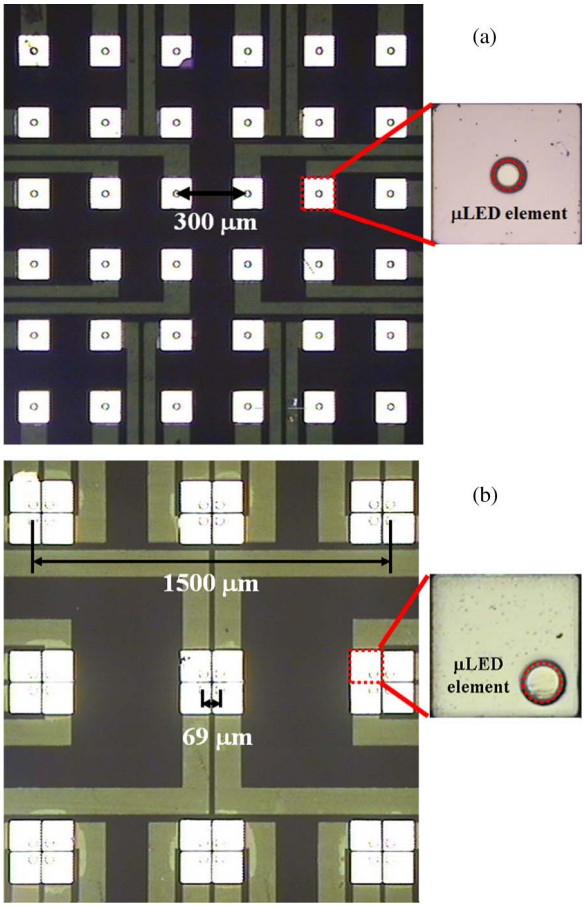


Fig. 7. a) Images of a) μLED array of the ganging device and b) μLED array of the MIMO device. High-magnification images for typical μLED elements are also shown.

C. Receiver

Modelling indicated that in order to obtain sufficient receiver sensitivity, an APD based receiver is required, with a typical input referred noise density of 10pA/$\sqrt{}$Hz. This is challenging compared with some designs. As a comparison, [27] reports referred noise for each channel of 29.9 pA/$\sqrt{}$Hz. In [28], Shimotori *et al.* showed that the APD structure shown in Fig. 8 can be made in a 0.18 μm process and have a responsivity to 405 nm light of 2.61 A/W at a reverse bias voltage of 9.1 V.

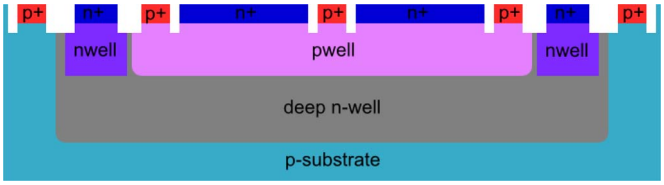


Fig. 8. A potential APD structure as reported in [28].

The measured bandwidth of the structure was 300 MHz which also fits in with the specification in Table I. The APD in [28] is 20 μm $\times$ 20 μm. Our requirement is for 200 μm $\times$ 200 μm. In addition to the bandwidth limitation imposed on the system by the capacitance of the APD (5), the intrinsic bandwidth of the photodiode can limit performance. A full description of the intrinsic bandwidth can be found in chapter 3 of [29] but it is related to the transit time of optically generated carriers across the APD. In [30], it was shown that through this effect the bandwidth reduces with increasing size of APD. This led to the hypothesis that it is better to build the APD out of a 10 $\times$ 10 array of 20 μm $\times$ 20 μm structures, whose outputs can be summed together by connecting the structures in parallel, in order to meet the bandwidth requirements. This method was also used in the paper recently published by Ray *et al.* [31].

The dominant source of noise will come from the TIA connected to the APD. In chapter 7 of [32], it is shown that if the input stage to the amplifier in a shunt-shunt feedback topology is a CMOS inverter then the total input-referred noise is:

$$I_{in} = 4k_B TB\left[\frac{1}{R_{TIA}} + 2\frac{\Gamma_F}{g_{mp}+g_{mn}}\frac{(2\pi C_{PD}B)^2}{3} + \frac{\Gamma_F}{R_{TIA}^2(g_{mp}+g_{mn})}\right] \quad (15)$$

where k_B is Boltzmann s constant, T is temperature, R_{TIA} is the feedback resistor, C_{PD} is the capacitance of the PD, Γ_F is the process dependent gamma factor and g_{mp} and g_{mn} are the transconductances of the input transistors. From the equation it can be seen that to reduce noise, the g_m of the input transistors must be increased which will increase the power consumption of the chip. At this point the power budget is not a limiting factor, but for future revisions there will have to be a trade-off between the number of channels and the power consumption of each channel which will in turn depend on the avalanche gain of the APDs. This may alter some of the design decisions.

VI. Experimental Results

The current status of the demonstration is that most of the components are manufactured and individually tested. The next step is to integrate the individual components to full a scale system demonstration. The measured electrical-to-electrical -3 dB bandwidths of ganging and MIMO μLED devices are shown in Fig. 9. The target bandwidths of 175 and 125 MHz for ganging and MIMO devices are met at bias currents of 55 mA and 100 mA, respectively. The measured optical powers at these currents are 2 and 3.5 mW, respectively. The transmitter and receiver designs were also verified by measuring the intensity profile and channel gain for the MIMO system at a distance of 1m from the transmitter that match the designed profile.

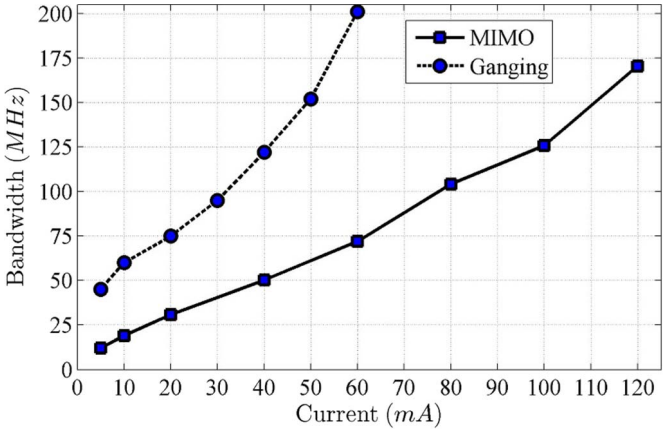


Fig. 9. Measured electrical-to-electrical bandwidths against the bias current of ganging and MIMO devices.

In order to demonstrate the potential of the design, a MIMO communication link using the available components was tested. At the transmitter an array of four μLEDs was used, each channel driven using an arbitrary waveform generator. The 3 $\times$ 3 APD receiver array described earlier is used. Issues with the CMOS process limited the available bandwidth of each APD to 22 MHz. Due to the limited capability of the implementation; an OOK modulation scheme with decision feedback equaliser (DFE) was used in the experiment.

The four μLEDs were driven by four independent pseudo random binary sequences of length 2^{14}-1. The LEDs were biased at a DC current of 50mA and an AC swing of 3.5 Vpp. The received signals from four APDs were then captured simultaneously using an Oscilloscope (MSO7104B), and further signal processing was done offline. The received data sequences were then compared with the transmitted sequence to estimate the bit error rate (BER).

Fig. 10 shows the measured BERs of different channels against data rate for the imaging MIMO system. The BER is estimated using a sequence of at least 40 $\times$ 10^5 bits per channel. The achievable data rates above the forward error correction (FEC) threshold of 2 $\times$ 10^{-3} [32] for channels 1–4 are 270, 290, 325, and 240 Mbps, respectively. The aggregate BERs against the data rates for MIMO system is also shown in Fig. 10. The MIMO system achieves a data rate of 1.070 Gbps, which correspond to a net rate of ˜1 Gbps after an FEC overhead reduction of 7% [33].

The subsystems required to be fully tested the MIMO and ganging schemes, using both OFDM and PAM are almost complete, including a modified APD array that should reach the required design bandwidth. System optimisation and testing will be carried out once all these are available.

VII. Conclusion and Future Work

This paper reports the detailed design of a demonstration VLC link. It shows that the optimum system design must take into account the particular characteristics of an emitter and receiver technology, and in this case there is an optimum modulation scheme that maximizes achievable data rate.

The simulation and analysis also shows that there is significant challenge in achieving highly parallel data links with a

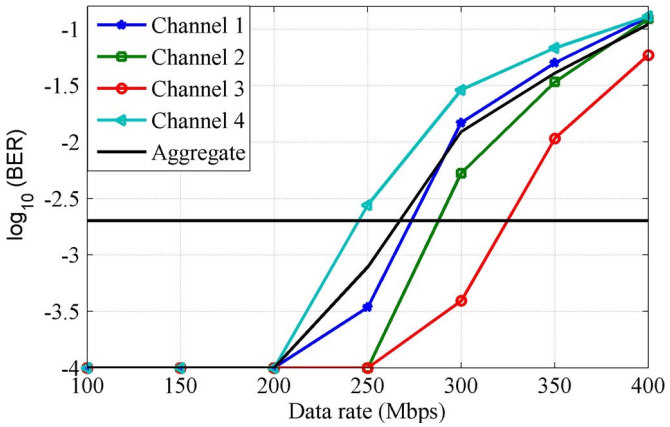


Fig. 10. Data rates against the BER for individual channel and aggregate MIMO system. Note that MIMO data rate is divided by 4 for the clarity of the figure.

larger FOV. The number of receiver elements increases rapidly with the increased FOV. The desire of high optical "gain" at the receiver also makes it challenging to miniaturize such systems for future integration in hand-held devices.

The paper also reports preliminary experimental results. Using a MIMO configuration, an aggregate data rate of ˜1 Gbps after FEC overhead reduction is achieved. Future work includes complete system test and characterisation. A number of modulation schemes including OFDM and PAM will be tested and experimental comparisons will be made. The next phase of the project will address the challenges of scaling the system to higher data rates and wider field of view. This is likely to require large numbers of emitter and receiver channels, and the issues of addressing such devices in a scalable way, as well as the necessary signal processing for schemes such as OFDM. These challenges will be fully considered in the future iteration of the designs.

ACKNOWLEDGMENT

The authors gratefully acknowledge support by the UK Engineering and Physical Sciences Research Council (EPSRC). Associated data, including the ray tracing files and data for the figures can be found at DOI 10.5287/bodleian:xp68kg80s.

REFERENCES

[1] Lighting the Way: Perspectives on the Global Lighting Market, McKinsey & Company, New York, NY, USA, 2012.
[2] L. Grobe *et al.*, "High-speed visible light communication systems," *IEEE Commun. Mag.*, vol. 51, no. 12, pp. 60–66, Dec. 2013.
[3] H. L. Minh *et al.*, "100-Mb/s NRZ visible light communications using a postequalized white LED," *IEEE Photon. Technol. Lett.*, vol. 21, no. 15, pp. 1063–1065, Aug. 2009.
[4] J. J. D. McKendry *et al.*, "Visible-light communications using a CMOS-controlled micro-light- emitting-diode array," *J. Lightw. Technol.*, vol. 30, no. 1, pp. 61–67, Jan. 2012.
[5] D. Tsonev *et al.*, "A 3-Gb/s single-LED OFDM-based wireless VLC link using a Gallium Nitride μLED," *IEEE Photon. Technol. Lett.*, vol. 26, no. 7, pp. 637–640, Apr. 2014.
[6] A. Jovicic, L. Junyi, and T. Richardson, "Visible light communication: Opportunities, challenges and the path to market," *IEEE Commun. Mag.*, vol. 51, no. 12, pp. 26–32, Dec. 2013.
[7] H. Chun *et al.*, "Visible light communication using a blue GaN μLED and fluorescent polymer color converter," *IEEE Photon. Technol. Lett.*, vol. 26, no. 20, pp. 2035–2038, Oct. 2014.
[8] F.-M. Wu *et al.*, "1.1-Gb/s white-LED-based visible light communication employing carrier-less amplitude and phase modulation," *IEEE Photon. Technol. Lett.*, vol. 24, no. 19, pp. 1730–1732, Oct. 2012.
[9] A. M. Khalid, G. Cossu, R. Corsini, P. Choudhury, and E. Ciaramella, "1-Gb/s transmission over a phosphorescent white LED by using rate-adaptive discrete multitone modulation," *IEEE Photon. J.*, vol. 4, no. 5, pp. 1465–1473, Oct. 2012.
[10] C. Kottke, J. Hilt, K. Habel, J. Vucic, and K. D. Langer, "1.25 Gbit/s visible light WDM link based on DMT modulation of a single RGB LED luminary," in *Proc. 38th ECOC*, 2012, pp. 1–3.
[11] S. Hranilovic and F. R. Kschischang, "A pixelated MIMO wireless optical communication system," *IEEE J. Sel. Topics Quantum Electron.*, vol. 12, no. 4, pp. 859–874, Jul./Aug. 2006.
[12] J. F. Li *et al.*, "Superposed pulse amplitude modulation for visible light communication," *Opt. Exp.*, vol. 21, no. 25, pp. 31006–31011, Dec. 2013.
[13] T. Q. Wang, Y. A. Sekercioglu, and J. Armstrong, "Analysis of an optical wireless receiver using a hemispherical lens with application in MIMO visible light communications," *J. Lightw. Technol.*, vol. 31, no. 11, pp. 1744–1754, Jun. 2013.
[14] A. Burton, H. L. Minh, Z. Ghassemlooy, E. Bentley, and C. Botella, "Experimental demonstration of 50-Mb/s visible light communications using 4 by 4 MIMO," *IEEE Photon. Technol. Lett.*, vol. 26, no. 9, pp. 945–948, May 2014.
[15] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*. Oxford, U.K.: Oxford Univ. Press, 2012.
[16] F. Tavernier and M. Steyaert, *High-Speed Optical Receivers with Integrated Photodiode in Nanoscale CMOS*. Berlin, Germany: Springer-Verlag, 2011.
[17] K. Szczerba *et al.*, "Comparison of intersymbol interference power penalties for OOK and 4-PAM in short-range optical links," *J. Lightw. Technol.*, vol. 31, no. 22, pp. 3525–3534, Nov. 2013.
[18] J. R. Barry, *Wireless Infrared Communications*. Boston, MA, USA: Kluwer, 1994.
[19] J. M. Kahn and J. R. Barry, "Wireless infrared communications," *Proc. IEEE*, vol. 85, no. 2, pp. 265–298, Feb. 1997.
[20] J. Armstrong and B. J. C. Schmidt, "Comparison of asymmetrically clipped optical OFDM and DC-biased optical OFDM in AWGN," *IEEE Commun. Lett.*, vol. 12, no. 5, pp. 343–345, May 2008.
[21] S. Dimitrov, S. Sinanovic, and H. Haas, "Signal shaping and modulation for optical wireless communication," *J. Lightw. Technol.*, vol. 30, no. 9, pp. 1319–1328, May 2012.
[22] S. Randel, F. Breyer, S. C. J. Lee, and J. W. Walewski, "Advanced modulation schemes for short-range optical communications," *IEEE J. Sel. Topics Quantum Electron.*, vol. 16, no. 5, pp. 1280–1289, Sep./Oct. 2010.
[23] S. D. Perli, N. Ahmed, and D. Katabi, "PixNet: Interference-free wireless links using LCD-camera pairs," presented at the 16th Annual Int. Conf. Mobile Computing Networking, Chicago, IL, USA, 2010.
[24] J. M. Kahn *et al.*, "Imaging diversity receivers for high-speed infrared wireless communication," *IEEE Commun. Mag.*, vol. 36, no. 12, pp. 88–94, Dec. 1998.
[25] Z. Lubin *et al.*, "High data rate multiple input multiple output (MIMO) optical wireless communications using white LED lighting," *IEEE J. Sel. Areas Commun.*, vol. 27, no. 9, pp. 1654–1662, Dec. 2009.
[26] P. Djahani and J. M. Kahn, "Analysis of infrared wireless links employing multibeam transmitters and imaging diversity receivers," *IEEE Trans. Commun.*, vol. 48, no. 12, pp. 2077–2088, Dec. 2000.
[27] C. Lili, L. Zhiqun, W. Zhigong, L. Wei, and Z. Li, "A 10-Gb/s CMOS differential transimpedance amplifier for parallel optical receiver," in *Proc. ISSSE*, 2010, pp. 1–4.
[28] T. Shimotori, K. Maekita, T. Maruyama, and K. Iiyama, "Characterization of APDs fabricated by 0.18\ μm CMOS in blue wavelength region," in *Proc. 17th OECC*, 2012, pp. 509–510.
[29] S. Radovanovic, A.-J. Annema, and B. Nauta, *High-Speed Photodiodes in Standard CMOS Technology*. Berlin, Germany: Springer-Verlag, 2008.
[30] M.-J. Lee and W.-Y. Choi, "Area-dependent photodetection frequency response characterization of silicon avalanche photodetectors fabricated with standard CMOS technology," *IEEE Trans. Electron Devices*, vol. 60, no. 3, pp. 998–1004, Mar. 2013.
[31] S. Ray, M. M. Hella, M. M. Hossain, P. Zarkesh-Ha, and M. M. Hayat, "Speed optimized large area avalanche photodetector in standard CMOS technology for visible light communication," in *Proc. IEEE SENSORS*, 2014, pp. 2147–2150.
[32] K. Schneider and H. Zimmermann, *Highly Sensitive Optical Receivers*, vol. 23. Berlin, Germany: Springer-Vesrlag, 2006.
[33] Forward Error Correction for High Bit-Rate DWDM Submarine Systems, ITU, Geneva, Switzerland, 2013.

Authors' photographs and biographies not available at the time of publication.

WD1.5 (Contributed)
9:45 AM - 10:00 AM

Multi-Gigabit Integrated MIMO Visible Light Communication System: Progress and Updates

Sujan Rajbhandari, *Member IEEE,* Hyunchae Chun, Grahame Faulkner, Dominic O'Brien, *Member IEEE*, Department of Engineering Science, University of Oxford, Oxford.
Aravind V. N. Jalajakumari, Katherine Cameron, Robert Henderson, CMOS Sensors & Systems Group, the University of Edinburgh, Edinburgh.
Enyuan Xie, Jonathan J. D. McKendry, *Member IEEE*, Johannes Herrnsdorf, Erdan Gu, Martin D. Dawson, *Fellow IEEE,* Institute of Photonics, Department of Physics, SUPA, University of Strathclyde, Glasgow.
Dobroslav Tsonev, Muhammad Ijaz, Harald Haas, *Member IEEE*, Institute for Digital Communications, Li-FI R&D Centre, The University of Edinburgh, Edinburgh.

***Abstract*—This paper reports the progress on an integrated multi-Gigabit multiple input multiple output visible light communication system employing an array of micro-light emitting diodes and photodiodes. A system overview and experimental results obtained so far are presented.**

I. Introduction

Solid-state lighting and display devices have the potential to offer high speed data communications. The large number of individual light emitting diode (LED) devices that are used to light a room make multiple input multiple output (MIMO) data transmission attractive. In this case both the spatial separation and colour dimension can be exploited to increase system capacity.

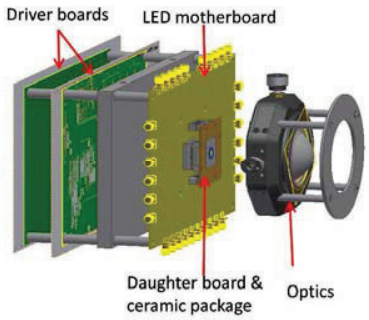
A key challenge in visible light communication (VLC) systems using commercially available white LEDs is the limited bandwidth, typically a few MHz. However, using commercial devices and an orthogonal frequency division multiplexing (OFDM) modulation scheme, 1 Gb/s systems have been demonstrated [1, 2].

In order to increase the available bandwidth Gallium Nitride (GaN) micro-LEDs (µLEDs), with a bandwidth of up to 200 MHz were used for a VLC system [3], and a data rate of more than 3 Gb/s was demonstrated [4]. In this work, the potential of using an array of µLEDs in a MIMO configuration is explored. A complete description of the system design is given in [5] and previous progress is also reported in [6] [7].

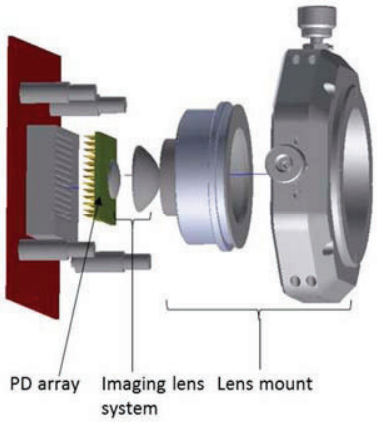
II. System Overview

A schematic of the MIMO VLC system under consideration is shown in Fig. 1. The system parameters are optimized to achieved a data rate of >1 Gbit/s over a link length of >1 m, with a field of view of approximately 5 degrees.

The transmitter consists of a current steering digital to analogue converter (DAC) based LED driver. The driver chip is designed and fabricated in a 0.18 µm complementary metal oxide semiconductor (CMOS) process. Each chip has four independent LED drivers. The DAC can support both analogue and digital modulation. The µLED array consists of individually addressable 6×6 array of blue (450 nm peak emission) devices with diameter of 25 µm (for single input single output configuration) and 39 µm (for MIMO configuration). These devices are fabricated from commercial InGaN/GaN wafers grown on sapphire. The µLED and LED driver connected using a LED motherboard and daughter cards.



a) Transmitter system



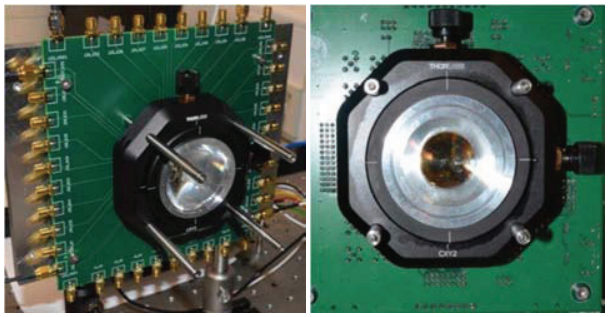
b) Receiver system

Fig. 1. The schematic of VLC system.

The optical system is optimized for a 4×4 imaging MIMO system using ray tracing software. A combination of commercially available singlet lenses is used to design high numerical aperture (NA) transmitter optics to collimate the Lambertian emission from the µLEDs. The receiver optics maps the transmitter µLED image to avalanche photodiode (APD) array. The µLEDs, APDs pitch and optics are optimized in such a way that the image of two µLEDs never falls entirely on a single receiver. The receiver chip has a 3×3 APD array manufactured using a 0.18 µm CMOS process. Each APD has individual transimpedance amplifier and all 9 outputs are available concurrently. The size of the APD is 200 µm x 200 µm.

III. Current Status and Experimental Results

A photograph of a complete system is shown in Fig. 2.



a) Transmitter system b) Receiver system

Fig. 2. Picture of transmitter and receiver subsystems.

A preliminary result from the system, using an APD receiver array with a bandwidth of ~22 MHz at a distance of 1 m was reported in [6]. Four µLEDs, corresponding to four MIMO channels, were driven independently by arbitrary waveform generators. Data rates of ~1 Gb/s was achieved at a 1m distance.

More recently, a second generation of APDs which has a bandwidth of ~100MHz and LED drivers that allow the number of µLEDs that can be driven to be increased has become available. In this case an error free communication link up to 500 Mbps (125 Mbps per channel) was achieved using 4-PAM using a single driver chip in its MIMO configuration. This rate corresponds to the highest sample rate that the current transmitter system can support. In order to increase the data rate, more than one DAC chip is required, and this will be available in the near future. In order to show what is potentially achievable using the current system, the data rate versus the bit error rate (BER) of an individual channel, without optical cross talk, at a link distance of 1m is shown in Fig. 3. This graph indicates that a data rate of more than 1Gb/s is feasible with the system. The LEDs in the current set-up were driven at an average current of ~25 mA, which is not the optimal value. The LEDs can operate at currents of up to 100 mA and the DAC can provide up to 255mA so higher rates will be available. Modelling indicates that with further optimization of bias current, modulation depth and linearization, a data-rate of up to 450 Mbps per channel is feasible. The performance of complete system with optimized operating conditions and PAM and OFDM modulation will be reported at the conference.

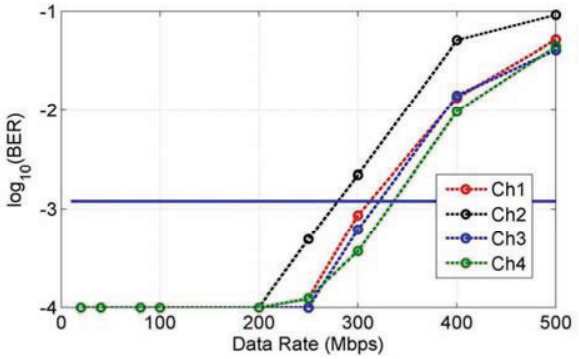


Fig. 3. Data-rate versus BER for individual channels using 4-PAM

IV. Conclusions and Future Work

This paper reports the performance of a MIMO VLC system based on µLEDs and APDs. The full system integration is complete and preliminary results show a data rate over 1Gb/s is feasible. With further optimization, it is expected to enhance the data rate, with feasible rates of up to 2 Gb/s.

V. Acknowledgements

This work was funded under the UK Engineering and Physical Sciences Research Council (EPSRC) grant EP/K00042X/1 ‘Ultra-Parallel Visible Light Communication’.

References

[1] W. Fang-Ming, L. Chun-Ting, W. Chia-Chien, C. Cheng-Wei, H. Hou-Tzu, and H. Chun-Hung, "1.1-Gb/s White-LED-Based Visible Light Communication Employing Carrier-Less Amplitude and Phase Modulation," *Photonics Technology Letters, IEEE,* vol. 24, pp. 1730-1732, 2012.

[2] A. H. Azhar, T. A. Tran, and D. O'Brien, "A Gigabit/s Indoor Wireless Transmission Using MIMO-OFDM Visible-Light Communications," *IEEE Photonics Technology Letters,* vol. 25, pp. 171-174, 2013.

[3] J. J. D. McKendry, R. P. Green, A. E. Kelly, G. Zheng, B. Guilhabert, D. Massoubre, E. Gu, and M. D. Dawson, "High-Speed Visible Light Communications Using Individual Pixels in a Micro Light-Emitting Diode Array," *IEEE Photonics Technology Letters,* vol. 22, pp. 1346-1348, 2010.

[4] D. Tsonev, H. Chun, S. Rajbhandari, J. McKendry, S. Videv, E. Gu, M. Haji, S. Watson, A. Kelly, G. Faulkner, M. Dawson, H. Haas, and D. O'Brien, "A 3-Gb/s single-LED OFDM-based wireless VLC link using a Gallium Nitride µLED," *IEEE Photonics Technology Letters,* vol. 26, pp. 637- 640, 2014.

[5] S. Rajbhandari, H. Chun, G. Faulkner, K. Cameron, A. V. N. Jalajakumari, R. Henderson, D. Tsonev, M. Ijaz, Z. Chen, H. Haas, E. Xie, J. J. D. McKendry, J. Herrnsdorf, E. Gu, M. D. Dawson, and D. O’Brien, " High-Speed Integrated Visible Light Communication System: Device Constraints and Design Considerations," J-SAC [unpublished]l.

[6] S. Rajbhandari, H. Chun, G. Faulkner, K. Cameron, A. V. N. Jalajakumari, R. Henderson, D. Tsonev, M. Ijaz, Z. Chen, H. Haas, E. Xie, J. J. D. McKendry, J. Herrnsdorf, E. Gu, M. D. Dawson, and D. O’Brien, "Imaging-MIMO Visible Light Communication System using µLEDs and Integrated Receiver," in *Globecom Workshops (GC Wkshps), 2014 IEEE*, 2014, pp. 621-625.

[7] D. O'Brien, H. Haas, S. Rajbhandari, H. Chun, G. Faulkner, K. Cameron, A. V. N. Jalajakumari, R. Henderson, D. Tsonev, M. Ijaz, Z. Chen, E. Xie, J. J. D. McKendry, J. Herrnsdorf, E. Gu, and M. D. Dawson, "Integrated multiple-input multiple-output visible light communications systems: recent progress and results," 2015, pp. 93870P-93870P-6.

Bibliography

[1] Philip Ronan. *File:EM spectrum.svg*.

[2] *THE FIRE SIGNALS OF POLYBIUS. » 18 May 1917 » The Spectator Archive*. http://archive.spectator.co.uk/article/19th-may-1917/9/the-fire-signals-of-polybius. (Accessed on 01/30/2017).

[3] Gerard J. Holzmann and Björn Pehrson. *The Early History of Data Networks*. Wiley-IEEE Computer Society Pr, 1994. ISBN: 0818667826. URL: http://people.seas.harvard.edu/~jones/cscie129/papers/Early_History_of_Data_Networks/The_Early_History_of_Data_Networks.html.

[4] Herbert Venghaus and Norbert Grote. *Fibre optic communication: key devices*. Vol. 161. 0342-4111. Springer, 2012. URL: http://link.springer.com/book/10.1007/978-3-642-20517-0.

[5] R. J. Essiambre and R. W. Tkach. "Capacity Trends and Limits of Optical Communication Networks". In: *Proceedings of the IEEE* 100.5 (May 2012), pp. 1035–1055. ISSN: 0018-9219. DOI: 10.1109/JPROC.2012.2182970.

[6] *Historic Demonstration Proves Laser Communication Possible | NASA*. https://www.nasa.gov/content/goddard/historic-demonstration-proves-laser-communication-possible. (Accessed on 01/28/2017).

[7] F. Moll et al. "Demonstration of High-Rate Laser Communications From a Fast Airborne Platform". In: *IEEE Journal on Selected Areas in Communications* 33.9 (Sept. 2015), pp. 1985–1995. ISSN: 0733-8716. DOI: 10.1109/JSAC.2015.2433054.

[8] A.G. Bell. "Photo phone-transmitter". US Patent 235,496. Dec. 1880. URL: http://www.google.co.uk/patents/US235496.

[9] F. R. Gfeller and U. Bapst. "Wireless in-house data communication via diffuse infrared radiation". In: *Proceedings of the IEEE* 67.11 (Nov. 1979), pp. 1474–1486. ISSN: 0018-9219. DOI: 10.1109/PROC.1979.11508.

[10] *LED ADOPTION REPORT | Department of Energy*. http://energy.gov/eere/ssl/downloads/led-adoption-report. (Accessed on 11/20/2016). 2015.

[11] M. B. Rahaim, A. M. Vegni, and T. D. C. Little. "A hybrid Radio Frequency and broadcast Visible Light Communication system". In: *2011 IEEE GLOBECOM Workshops (GC Wkshps)*. Dec. 2011, pp. 792–796. DOI: 10.1109/GLOCOMW.2011.6162563.

[12] H. Haas et al. "What is LiFi?" In: *Journal of Lightwave Technology* 34.6 (Mar. 2016), pp. 1533–1544. ISSN: 0733-8724. DOI: 10.1109/JLT.2015.2510021.

[13] N. Kumar et al. "Visible light communication for intelligent transportation in road safety applications". In: *2011 7th International Wireless Communications and Mobile Computing Conference*. July 2011, pp. 1513–1518. DOI: 10.1109/IWCMC.2011.5982762.

[14] Jong-Ho Yoo et al. "Demonstration of vehicular visible light communication based on LED headlamp". In: *2013 Fifth International Conference on Ubiquitous and Future Networks (ICUFN)*. July 2013, pp. 465–467. DOI: 10.1109/ICUFN.2013.6614862.

[15] H. S. Kim et al. "An Indoor Visible Light Communication Positioning System Using a RF Carrier Allocation Technique". In: *Journal of Lightwave Technology* 31.1 (Jan. 2013), pp. 134–144. ISSN: 0733-8724. DOI: 10.1109/JLT.2012.2225826.

[16] *Ericsson Mobility Report 2016*. Tech. rep. Ericsson, June 2016. URL: https://www.ericsson.com/mobility-report.

[17] *Cisco Visual Networking Index: Global Mobile Data Traffic Forecast Update, 2015–2020, White Paper*. Tech. rep. 1454457600805266. Cisco Systems, Feb. 2016. URL: http://www.cisco.com/c/en/us/solutions/collateral/service-provider/visual-networking-index-vni/mobile-white-paper-c11-520862.html.

[18] C. X. Wang et al. "Cellular architecture and key technologies for 5G wireless communication networks". In: *IEEE Communications Magazine* 52.2 (Feb. 2014), pp. 122–130. ISSN: 0163-6804. DOI: 10.1109/MCOM.2014.6736752.

[19] *Frequency Allocation Table*. National Frequency Planning Group, 2013. URL: http://stakeholders.ofcom.org.uk/binaries/spectrum/spectrum-information/UKFAT_2013.pdf.

[20] X. Huang et al. "2.0-Gb/s Visible Light Link Based on Adaptive Bit Allocation OFDM of a Single Phosphorescent White LED". In: *IEEE Photonics Journal* 7.5 (Oct. 2015), pp. 1–8. ISSN: 1943-0655. DOI: 10.1109/JPHOT.2015.2480541.

[21] D. Tsonev et al. “A 3-Gb/s Single-LED OFDM-based Wireless VLC Link Using a Gallium Nitride μLED”. In: *Photonics Technology Letters, IEEE* PP.99 (2014), pp. 1–1. ISSN: 1041-1135. DOI: 10.1109/LPT.2013.2297621.

[22] C. Kottke et al. “1.25 Gbit/s visible light WDM link based on DMT modulation of a single RGB LED luminary”. In: *2012 38th European Conference and Exhibition on Optical Communications*. Sept. 2012, pp. 1–3. DOI: 10.1364/ECEOC.2012.We.3.B.4.

[23] G. Cossu et al. “5.6 Gbit/s downlink and 1.5 Gbit/s uplink optical wireless transmission at indoor distances (>= 1.5 m)”. In: *2014 The European Conference on Optical Communication (ECOC)*. Sept. 2014, pp. 1–3. DOI: 10.1109/ECOC.2014.6963837.

[24] J. Vucic et al. “513 Mbit/s Visible Light Communications Link Based on DMT-Modulation of a White LED”. In: *Journal of Lightwave Technology* 28.24 (Dec. 2010), pp. 3512–3518. ISSN: 0733-8724. DOI: 10.1109/JLT.2010.2089602.

[25] J. Vučić et al. “803 Mbit/s visible light WDM link based on DMT modulation of a single RGB LED luminary”. In: *2011 Optical Fiber Communication Conference and Exposition and the National Fiber Optic Engineers Conference*. Mar. 2011, pp. 1–3.

[26] A. M. Khalid et al. “1 Gbit/s visible light communication link based on phosphorescent white LED”. In: *2012 International Conference on Photonics in Switching (PS)*. Sept. 2012, pp. 1–3.

[27] Fang-Ming Wu et al. “3.22-Gb/s WDM visible light communication of a single RGB LED employing carrier-less amplitude and phase modulation”. In: *Optical Fiber Communication Conference and Exposition and the National Fiber Optic Engineers Conference (OFC/NFOEC), 2013*. Mar. 2013, pp. 1–3.

[28] Honglei Li et al. “An analog modulator for 460 MB/S visible light data transmission based on OOK-NRS modulation”. In: *Wireless Communications, IEEE* 22.2 (Apr. 2015), pp. 68–73. ISSN: 1536-1284. DOI: 10.1109/MWC.2015.7096287.

[29] N. Fujimoto and S. Yamamoto. “The fastest visible light transmissions of 662 Mb/s by a blue LED, 600 Mb/s by a red LED, and 520 Mb/s by a green LED based on simple OOK-NRZ modulation of a commercially available RGB-type white LED using pre-emphasis and post-equalizing techniques”. In: *Optical Communication (ECOC), 2014 European Conference on*. Sept. 2014, pp. 1–3. DOI: 10.1109/ECOC.2014.6963895.

[30] *Ultra-parallel visible light communications (UP-VLC)*. http://gow.epsrc.ac.uk/NGBOViewGrant.aspx?GrantRef=EP/K00042X/1. (Accessed on 12/11/2016).

[31] A.V.N. Jalajakumari et al. “An energy efficient high-speed digital LED driver for visible light communications”. In: *Communications (ICC), 2015 IEEE International Conference on*. June 2015, pp. 5054–5059. DOI: 10.1109/ICC.2015.7249125.

[32] A. V. N. Jalajakumari et al. “High-Speed Integrated Digital to Light Converter for Short Range Visible Light Communication”. In: *IEEE Photonics Technology Letters* 29.1 (Jan. 2017), pp. 118–121. ISSN: 1041-1135. DOI: 10.1109/LPT.2016.2624281.

[33] J. Kosman et al. “60 Mb/s, 2 meters visible light communications in 1 klx ambient using an unlensed CMOS SPAD receiver”. In: *2016 IEEE Photonics Society Summer Topical Meeting Series (SUM)*. July 2016, pp. 171–172. DOI: 10.1109/PHOSST.2016.7548773.

[34] S. Rajbhandari et al. “Imaging-MIMO visible light communication system using βLEDs and integrated receiver”. In: *2014 IEEE Globecom Workshops (GC Wkshps)*. Dec. 2014, pp. 536–540. DOI: 10.1109/GLOCOMW.2014.7063487.

[35] S. Rajbhandari et al. “High-Speed Integrated Visible Light Communication System: Device Constraints and Design Considerations”. In: *IEEE Journal on Selected Areas in Communications* 33.9 (Sept. 2015), pp. 1750–1757. ISSN: 0733-8716. DOI: 10.1109/JSAC.2015.2432551.

[36] S. Rajbhandari et al. “Multi-Gigabit integrated MIMO visible light communication system: Progress and updates”. In: *2015 IEEE Summer Topicals Meeting Series (SUM)*. July 2015, pp. 230–231. DOI: 10.1109/PHOSST.2015.7248282.

[37] O.B. Hughes. *Improvement in telegraphs*. US Patent 14,917. May 1856. URL: https://www.google.com/patents/US14917.

[38] G. Marconi. *transmitting electrical signals*. US Patent 586,193. July 1897. URL: https://www.google.com/patents/US586193.

[39] *Jagdish Chandra Bose - New World Encyclopedia*. http://www.newworldencyclopedia.org/entry/Jagdish_Chandra_Bose. (Accessed on 01/31/2017).

[40] *short_history.pdf*. https://transition.fcc.gov/omd/history/radio/documents/short_history.pdf. (Accessed on 01/31/2017).

[41] T. S. Rappaport et al. “Millimeter Wave Mobile Communications for 5G Cellular: It Will Work!” In: *IEEE Access* 1 (2013), pp. 335–349. ISSN: 2169-3536. DOI: 10.1109/ACCESS.2013.2260813.

[42] H. J. Song and T. Nagatsuma. “Present and Future of Terahertz Communications”. In: *IEEE Transactions on Terahertz Science and Technology* 1.1 (Sept. 2011), pp. 256–263. ISSN: 2156-342X. DOI: 10.1109/TTHZ.2011.2159552.

[43] Nick Holonyak and S. F. Bevacqua. “COHERENT (VISIBLE) LIGHT EMISSION FROM Ga(As1-xPx) JUNCTIONS”. In: *Applied Physics Letters* 1.4 (1962), p. 82. DOI: 10.1063/1.1753706. URL: http://dx.doi.org/10.1063/1.1753706.

[44] M. G. Craford. “From Holonyak to Today”. In: *Proceedings of the IEEE* 101.10 (Oct. 2013), pp. 2170–2175. ISSN: 0018-9219. DOI: 10.1109/JPROC.2013.2274911.

[45] *Welcome to IrDA*. http://www.irdajp.info/what.html. (Accessed on 11/19/2016).

[46] Shuji Nakamura, Masayuki Senoh, and Takashi Mukai. “pGaN nInGaN nGaN Double-Heterostructure Blue Light Emitting Diodes”. In: *Japanese Journal of Applied Physics* 32.1A (1993), p. L8. URL: http://stacks.iop.org/1347-4065/32/i=1A/a=L8.

[47] G. Pang et al. “LED traffic light as a communications device”. In: *Proceedings 199 IEEE/IEEJ/JSAI International Conference on Intelligent Transportation Systems (Cat. No.99TH8383)*. 1999, pp. 788–793. DOI: 10.1109/ITSC.1999.821161.

[48] G. Pang et al. “Optical wireless based on high brightness visible LEDs”. In: *Conference Record of the 1999 IEEE Industry Applications Conference. Thirty-Forth IAS Annual Meeting (Cat. No.99CH36370)*. Vol. 3. 1999, 1693–1699 vol.3. DOI: 10.1109/IAS.1999.805968.

[49] G. Pang et al. “Visible light communication for audio systems”. In: *IEEE Transactions on Consumer Electronics* 45.4 (Nov. 1999), pp. 1112–1118. ISSN: 0098-3063. DOI: 10.1109/30.809190.

[50] Y. Tanaka et al. “Indoor visible communication utilizing plural white LEDs as lighting”. In: *Personal, Indoor and Mobile Radio Communications, 2001 12th IEEE International Symposium on*. Vol. 2. Sept. 2001, F-81-F-85 vol.2. DOI: 10.1109/PIMRC.2001.965300.

[51] K. Fan et al. “The effect of reflection on indoor visible-light communication system utilizing white LEDs”. In: *Wireless Personal Multimedia Communications, 2002. The 5th International Symposium on*. Vol. 2. Oct. 2002, 611–615 vol.2. DOI: 10.1109/WPMC.2002.1088247.

[52] Y. Tanaka, S. Haruyama, and M. Nakagawa. “Wireless optical transmissions with white colored LED for wireless home links”. In: *Personal, Indoor and Mobile Radio Communications, 2000. PIMRC 2000. The 11th IEEE International Symposium on*. Vol. 2. 2000, 1325–1329 vol.2. DOI: 10.1109/PIMRC.2000.881634.

[53] M. Z. Afgani et al. “Visible light communication using OFDM”. In: *Testbeds and Research Infrastructures for the Development of Networks and Communities, 2006. TRIDENTCOM 2006. 2nd International Conference on*, 6 pp.-134. ISBN: Not Applica. DOI: 10.1109/TRIDNT.2006.1649137.

[54] H. Elgala, R. Mesleh, and H. Haas. “Indoor broadcasting via white LEDs and OFDM”. In: *Consumer Electronics, IEEE Transactions on* 55.3 (2009), pp. 1127–1134. ISSN: 0098-3063. DOI: 10.1109/TCE.2009.5277966.

[55] T. Komine, S. Haruyama, and M. Nakagawa. “Performance evaluation of narrowband OFDM on integrated system of power line communication and visible light wireless communication”. In: *2006 1st International Symposium on Wireless Pervasive Computing*. Jan. 2006, 6 pp.-. DOI: 10.1109/ISWPC.2006.1613633.

[56] Seung Hee Han and Jae Hong Lee. “An overview of peak-to-average power ratio reduction techniques for multicarrier transmission”. In: *IEEE Wireless Communications* 12.2 (Apr. 2005), pp. 56–65. ISSN: 1536-1284. DOI: 10.1109/MWC.2005.1421929.

[57] S. Dimitrov, S. Sinanovic, and H. Haas. “Signal Shaping and Modulation for Optical Wireless Communication”. In: *Journal of Lightwave Technology* 30.9 (May 2012), pp. 1319–1328. ISSN: 0733-8724. DOI: 10.1109/JLT.2012.2188376.

[58] S. Dimitrov, S. Sinanovic, and H. Haas. “Clipping Noise in OFDM-Based Optical Wireless Communication Systems”. In: *IEEE Transactions on Communications* 60.4 (Apr. 2012), pp. 1072–1081. ISSN: 0090-6778. DOI: 10.1109/TCOMM.2012.022712.100493.

[59] H. Elgala, R. Mesleh, and H. Haas. “Practical considerations for indoor wireless optical system implementation using OFDM”. In: *2009 10th International Conference on Telecommunications*. June 2009, pp. 25–29.

[60] Lubin Zeng et al. “Equalisation for high-speed Visible Light Communications using white-LEDs”. In: *2008 6th International Symposium on Communication Systems, Networks and Digital Signal Processing*. July 2008, pp. 170–173. DOI: 10.1109/CSNDSP.2008.4610760.

[61] H. Le Minh et al. “100-Mb/s NRZ Visible Light Communications Using a Postequalized White LED”. In: *IEEE Photonics Technology Letters* 21.15 (Aug. 2009), pp. 1063–1065. ISSN: 1041-1135. DOI: 10.1109/LPT.2009.2022413.

[62] Zhang Shuailong et al. “High-bandwidth parallel data transmission using GaN/CMOS micro-LED arrays”. In: *Photonics Conference (IPC), 2012 IEEE*, pp. 38–39. DOI: 10.1109/IPCon.2012.6358477.

[63] S. Zhang et al. “1.5 Gbit/s Multi-Channel Visible Light Communications Using CMOS-Controlled GaN-Based LEDs”. In: *Journal of Lightwave Technology* 31.8 (Apr. 2013), pp. 1211–1216. ISSN: 0733-8724. DOI: 10.1109/JLT.2013.2246138.

[64] R. X. G. Ferreira et al. “High Bandwidth GaN-Based Micro-LEDs for Multi-Gb/s Visible Light Communications”. In: *IEEE Photonics Technology Letters* 28.19 (Oct. 2016), pp. 2023–2026. ISSN: 1041-1135. DOI: 10.1109/LPT.2016.2581318.

[65] Hyunchae Chun et al. “LED Based Wavelength Division Multiplexed 10 Gb/s Visible Light Communications”. In: *J. Lightwave Technol.* 34.13 (July 2016), pp. 3047–3052. URL: http://jlt.osa.org/abstract.cfm?URI=jlt-34-13-3047.

[66] H. Elgala, R. Mesleh, and H. Haas. “A study of LED nonlinearity effects on optical wireless transmission using OFDM”. In: *2009 IFIP International Conference on Wireless and Optical Communications Networks*. Apr. 2009, pp. 1–5. DOI: 10.1109/WOCN.2009.5010576.

[67] H. Chun et al. “Demonstration of a Bi-directional visible light communication with an overall sum-rate of 110 Mb/s using LEDs as emitter and detector”. In: *2014 IEEE Photonics Conference*. Oct. 2014, pp. 132–133. DOI: 10.1109/IPCon.2014.6995247.

[68] D. O’Brien. “Multi-input multi-output (MIMO) indoor optical wireless communications”. In: *2009 Conference Record of the Forty-Third Asilomar Conference on Signals, Systems and Computers*. Nov. 2009, pp. 1636–1639. DOI: 10.1109/ACSSC.2009.5470195.

[69] Hoa Le Minh, D. O’Brien, and G. Faulkner. “A gigabit/s indoor optical wireless system for Home Access Networks”. In: *2010 7th International Symposium on Communication Systems, Networks Digital Signal Processing (CSNDSP 2010)*. July 2010, pp. 532–536.

[70] J. Vucic et al. “White Light Wireless Transmission at 200 + Mb/s Net Data Rate by Use of Discrete-Multitone Modulation”. In: *IEEE Photonics Technology Letters* 21.20 (Oct. 2009), pp. 1511–1513. ISSN: 1041-1135. DOI: 10.1109/LPT.2009.2028696.

[71] J. Grubor et al. “Wireless High-Speed Data Transmission with Phosphorescent White-Light LEDs”. In: *33rd European Conference and Exhibition of Optical Communication - Post-Deadline Papers (published 2008)*. Sept. 2007, pp. 1–2.

[72] Minh Hoa Le et al. “High-Speed Visible Light Communications Using Multiple-Resonant Equalization”. In: *Photonics Technology Letters, IEEE* 20.14 (2008), pp. 1243–1245. ISSN: 1041-1135. DOI: 10.1109/LPT.2008.926030.

[73] Hoa Le Minh et al. “80 Mbit/s Visible Light Communications using pre-equalized white LED”. In: *2008 34th European Conference on Optical Communication*. Sept. 2008, pp. 1–2. DOI: 10.1109/ECOC.2008.4729532.

[74] Minh Hoa Le et al. “100-Mb/s NRZ Visible Light Communications Using a Postequalized White LED”. In: *Photonics Technology Letters, IEEE* 21.15 (2009), pp. 1063–1065. ISSN: 1041-1135. DOI: 10.1109/LPT.2009.2022413.

[75] G. Cossu et al. “Long distance indoor high speed visible light communication system based on RGB LEDs”. In: *2012 Asia Communications and Photonics Conference (ACP)*. Nov. 2012, pp. 1–3. DOI: 10.1364/ACP.2012.AS3C.2.

[76] J.J.D. McKendry et al. “Visible-Light Communications Using a CMOS-Controlled Micro-Light- Emitting-Diode Array”. In: *Lightwave Technology, Journal of* 30.1 (Jan. 2012), pp. 61–67. ISSN: 0733-8724. DOI: 10.1109/JLT.2011.2175090.

[77] F. M. Wu et al. “1.1-Gb/s White-LED-Based Visible Light Communication Employing Carrier-Less Amplitude and Phase Modulation”. In: *IEEE Photonics Technology Letters* 24.19 (Oct. 2012), pp. 1730–1732. ISSN: 1041-1135. DOI: 10.1109/LPT.2012.2210540.

[78] G. Cossu et al. “3.4 Gbit/s visible optical wireless transmission based on RGB LED”. In: *Opt. Express* 20.26 (Dec. 2012), B501–B506. DOI: 10.1364/OE.20.00B501. URL: http://www.opticsexpress.org/abstract.cfm?URI=oe-20-26-B501.

[79] A. H. Azhar, T. A. Tran, and D. O’Brien. “A Gigabit/s Indoor Wireless Transmission Using MIMO-OFDM Visible-Light Communications”. In: *Photonics Technology Letters, IEEE* 25.2 (2013), pp. 171–174. ISSN: 1041-1135. DOI: 10.1109/LPT.2012.2231857.

[80] T. Fath, C. Heller, and H. Haas. “Optical Wireless Transmitter Employing Discrete Power Level Stepping”. In: *Lightwave Technology, Journal of* 31.11 (June 2013), pp. 1734–1743. ISSN: 0733-8724. DOI: 10.1109/JLT.2013.2257984.

[81] P. H. Binh et al. “Demonstration of 300 Mbit/s free space optical link with commercial visible LED”. In: *2013 IEEE 11th International New Circuits and Systems Conference (NEWCAS)*. June 2013, pp. 1–3. DOI: 10.1109/NEWCAS.2013.6573602.

[82] Babar Hussain et al. “A fully integrated IEEE 802.15.7 visible light communication transmitter with on chip 8W 85% efficiency boost LED driver”. In: *VLSI Circuits (VLSI Circuits), 2015 Symposium on*. June 2015, pp. C216–C217. DOI: 10.1109/VLSIC.2015.7231264.

[83] P. Manousiadis et al. “Demonstration of 2.3 Gb/s RGB white-light VLC using polymer based colour-converters and GaN micro-LEDs”. In: *2015 IEEE Summer Topicals Meeting Series (SUM)*. July 2015, pp. 222–223. DOI: 10.1109/PHOSST.2015.7248279.

[84] José Ramón Durán Retamal et al. “4-Gbit/s visible light communication link based on 16-QAM OFDM transmission over remote phosphor-film converted white light by using blue laser diode”. In: *Opt. Express* 23.26 (Dec. 2015), pp. 33656–33666. DOI: 10.1364/OE.23.033656. URL: http://www.opticsexpress.org/abstract.cfm?URI=oe-23-26-33656.

[85] Y. Wang et al. “8-Gb/s RGBY LED-Based WDM VLC System Employing High-Order CAP Modulation and Hybrid Post Equalizer”. In: *IEEE Photonics Journal* 7.6 (Dec. 2015), pp. 1–7. ISSN: 1943-0655. DOI: 10.1109/JPHOT.2015.2489927.

[86] Dobroslav Tsonev, Stefan Videv, and Harald Haas. “Towards a 100 Gb/s visible light wireless access network”. In: *Opt. Express* 23.2 (Jan. 2015), pp. 1627–1637. DOI: 10.1364/OE.23.001627. URL: http://www.opticsexpress.org/abstract.cfm?URI=oe-23-2-1627.

[87] R. X. G. Ferreira et al. “High Bandwidth GaN-Based Micro-LEDs for Multi-Gb/s Visible Light Communications”. In: *IEEE Photonics Technology Letters* 28.19 (Oct. 2016), pp. 2023–2026. ISSN: 1041-1135. DOI: 10.1109/LPT.2016.2581318.

[88] H. Chun et al. “LED Based Wavelength Division Multiplexed 10 Gb/s Visible Light Communications”. In: *Journal of Lightwave Technology* 34.13 (July 2016), pp. 3047–3052. ISSN: 0733-8724. DOI: 10.1109/JLT.2016.2554145.

[89] Simon Haykin. *Communication Systems*. 5th. Wiley Publishing, 2009. ISBN: 0471697907, 9780471697909.

[90] A. T. Hussein and J. M. H. Elmirghani. “Mobile Multi-Gigabit Visible Light Communication System in Realistic Indoor Environment”. In: *Journal of Lightwave Technology* 33.15 (Aug. 2015), pp. 3293–3307. ISSN: 0733-8724. DOI: 10.1109/JLT.2015.2439051.

[91] C. Lee et al. “2.6 GHz high-speed visible light communication of 450 nm GaN laser diode by direct modulation”. In: *2015 IEEE Summer Topicals Meeting Series (SUM)*. July 2015, pp. 112–113. DOI: 10.1109/PHOSST.2015.7248213.

[92] J. S. Rieh, S. Jeon, and M. Kim. “An overview of integrated THz electronics for communication applications”. In: *2011 IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS)*. Aug. 2011, pp. 1–4. DOI: 10.1109/MWSCAS.2011.6026592.

[93] J. M. Kahn and J. R. Barry. “Wireless infrared communications”. In: *Proceedings of the IEEE* 85.2 (Feb. 1997), pp. 265–298. ISSN: 0018-9219. DOI: 10.1109/5.554222.

[94] S. Kitano, S. Haruyama, and M. Nakagawa. “LED road illumination communications system”. In: *2003 IEEE 58th Vehicular Technology Conference. VTC 2003-Fall (IEEE Cat. No.03CH37484)*. Vol. 5. Oct. 2003, 3346–3350 Vol.5. DOI: 10.1109/VETECF.2003.1286302.

[95] J. Vučić et al. “230 Mbit/s via a wireless visible-light link based on OOK modulation of phosphorescent white LEDs”. In: *2010 Conference on Optical Fiber Communication (OFC/NFOEC), collocated National Fiber Optic Engineers Conference*. Mar. 2010, pp. 1–3.

[96] J. Vucic et al. “125 Mbit/s over 5 m wireless distance by use of OOK-Modulated phosphorescent white LEDs”. In: *2009 35th European Conference on Optical Communication*. Sept. 2009, pp. 1–2.

[97] E. Fred Schubert. *Light-Emitting Diodes*. Second. Cambridge Books Online. Cambridge University Press, 2006. ISBN: 9780511790546. URL: http://dx.doi.org/10.1017/CBO9780511790546.

[98] T. Kishi, H. Tanaka, and Y. Umeda. “A high speed LED driver for visible light communications with drawing out remaining carriers by a CMOS inverter”. In: *Microwave Conference Proceedings (APMC), 2011 Asia-Pacific*, pp. 1234–1237.

[99] M. Salehi and J. Proakis. *Digital Communications*. McGraw-Hill Education, 2007. ISBN: 9780072957167. URL: https://books.google.co.uk/books?id=HroiQAAACAAJ.

[100] Runsheng He, N. Nazari, and S. Sutardja. “A DSP based receiver for 1000BASE-T PHY”. In: *2001 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC (Cat. No.01CH37177)*. Feb. 2001, pp. 308–309. DOI: 10.1109/ISSCC.2001.912651.

[101] D. C. O’Brien et al. “Visible light communications: Challenges and possibilities”. In: *2008 IEEE 19th International Symposium on Personal, Indoor and Mobile Radio Communications*. Sept. 2008, pp. 1–5. DOI: 10.1109/PIMRC.2008.4699964.

[102] S. Randel et al. “Advanced Modulation Schemes for Short-Range Optical Communications”. In: *IEEE Journal of Selected Topics in Quantum Electronics* 16.5 (Sept. 2010), pp. 1280–1289. ISSN: 1077-260X. DOI: 10.1109/JSTQE.2010.2040808.

[103] K. I. Ahn and J. K. Kwon. “Capacity Analysis of M-PAM Inverse Source Coding in Visible Light Communications”. In: *Journal of Lightwave Technology* 30.10 (May 2012), pp. 1399–1404. ISSN: 0733-8724. DOI: 10.1109/JLT.2012.2185780.

[104] L. Grobe and K. D. Langer. “Block-based PAM with frequency domain equalization in visible light communications”. In: *2013 IEEE Globecom Workshops (GC Wkshps)*. Dec. 2013, pp. 1070–1075. DOI: 10.1109/GLOCOMW.2013.6825134.

[105] G. Stepniak, M. Sch?ppert, and C. A. Bunge. “Advanced Modulation Formats in Phosphorous LED VLC Links and the Impact of Blue Filtering”. In: *Journal of Lightwave Technology* 33.21 (Nov. 2015), pp. 4413–4423. ISSN: 0733-8724. DOI: 10.1109/JLT.2015.2472575.

[106] J. Grubor et al. “Bandwidth-efficient indoor optical wireless communications with white light-emitting diodes”. In: *2008 6th International Symposium on Communication Systems, Networks and Digital Signal Processing*. July 2008, pp. 165–169. DOI: 10.1109/CSNDSP.2008.4610769.

[107] X. Li et al. “2 Gb/s uLED-APD based visible light communications using feed-forward pre-equalization and PAM-4 modulation”. In: *2015 European Conference on Optical Communication (ECOC)*. Sept. 2015, pp. 1–3. DOI: 10.1109/ECOC.2015.7341880.

[108] S. Dimitrov and H. Haas. *Principles of LED Light Communications*. Principles of LED Light Communications: Towards Networked Li-Fi. Cambridge University Press, 2015. ISBN: 9781107049420. URL: http://www.cambridge.org/9781107049420.

[109] S. D. Dissanayake and J. Armstrong. “Comparison of ACO-OFDM, DCO-OFDM and ADO-OFDM in IM/DD Systems”. In: *Journal of Lightwave Technology* 31.7 (Apr. 2013), pp. 1063–1072. ISSN: 0733-8724. DOI: 10.1109/JLT.2013.2241731.

[110] E. F. Schubert. *Doping in III-V Semiconductors*. Cambridge Books Online. Cambridge University Press, 1993. ISBN: 9780511599828. URL: http://dx.doi.org/10.1017/CBO9780511599828.

[111] William Shockley. “The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors”. In: *The Bell System technical journal* 28 (1949), pp. 435–489. URL: https://archive.org/details/bellsystemtechni28amerrich.

[112] H. Elgala, R. Mesleh, and H. Haas. "Indoor optical wireless communication: potential and state-of-the-art". In: *IEEE Communications Magazine* 49.9 (Sept. 2011), pp. 56–62. ISSN: 0163-6804. DOI: 10.1109/MCOM.2011.6011734.

[113] J. J. D. McKendry et al. "Visible-Light Communications Using a CMOS-Controlled Micro-Light- Emitting-Diode Array". In: *Lightwave Technology, Journal of* 30.1 (2012), pp. 61–67. ISSN: 0733-8724. DOI: 10.1109/JLT.2011.2175090.

[114] *Global LED Driver Market worth USD 19.03 Billion by 2021*. https://www.zionmarketresearch.com/news/Global-LED-Driver-Market. (Accessed on 01/31/2017).

[115] K. Modepalli and L. Parsa. "Dual-Purpose Offline LED Driver for Illumination and Visible Light Communication". In: *Industry Applications, IEEE Transactions on* 51.1 (Jan. 2015), pp. 406–419. ISSN: 0093-9994. DOI: 10.1109/TIA.2014.2330066.

[116] Shuze Zhao, Jiale Xu, and O. Trescases. "A dimmable LED driver for visible light communication (VLC) based on LLC resonant DC-DC converter operating in burst mode". In: *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE*. Mar. 2013, pp. 2144–2150. DOI: 10.1109/APEC.2013.6520592.

[117] X. Li et al. "Design and Characterization of Active Matrix LED Microdisplays With Embedded Visible Light Communication Transmitter". In: *Journal of Lightwave Technology* 34.14 (July 2016), pp. 3449–3457. ISSN: 0733-8724. DOI: 10.1109/JLT.2016.2562667.

[118] *N8241A Arbitrary Waveform Generator*. N8241A. Keysight Technologies.

[119] Minh Hoa Le et al. "80 Mbit/s Visible Light Communications using pre-equalized white LED". In: *Optical Communication, 2008. ECOC 2008. 34th European Conference on*, pp. 1–2. DOI: 10.1109/ECOC.2008.4729532.

[120] D. Park, Z. Liu, and H. Lee. "A 40 V 10 W 93%-Efficiency Current-Accuracy-Enhanced Dimmable LED Driver With Adaptive Timing Difference Compensation for Solid-State Lighting Applications". In: *IEEE Journal of Solid-State Circuits* 49.8 (Aug. 2014), pp. 1848–1860. ISSN: 0018-9200. DOI: 10.1109/JSSC.2014.2320951.

[121] D. Vassis et al. "The IEEE 802.11g standard for high data rate WLANs". In: *IEEE Network* 19.3 (May 2005), pp. 21–26. ISSN: 0890-8044. DOI: 10.1109/MNET.2005.1453395.

[122] L. Verma, M. Fakharzadeh, and S. Choi. "Wifi on steroids: 802.11AC and 802.11AD". In: *IEEE Wireless Communications* 20.6 (Dec. 2013), pp. 30–35. ISSN: 1536-1284. DOI: 10.1109/MWC.2013.6704471.

[123] Zhong-Yuan Chang et al. “A CMOS analog front-end circuit for an FDM-based ADSL system”. In: *IEEE Journal of Solid-State Circuits* 30.12 (Dec. 1995), pp. 1449–1456. ISSN: 0018-9200. DOI: 10.1109/4.482192.

[124] K. Findlater et al. “A 90nm CMOS Dual-Channel Powerline Communication AFE for Homeplug AV with a Gb Extension”. In: *2008 IEEE International Solid-State Circuits Conference - Digest of Technical Papers* (Feb. 2008), pp. 464–628. ISSN: 0193-6530. DOI: 10.1109/ISSCC.2008.4523258.

[125] F. H. Raab et al. “Power amplifiers and transmitters for RF and microwave”. In: *IEEE Transactions on Microwave Theory and Techniques* 50.3 (Mar. 2002), pp. 814–826. ISSN: 0018-9480. DOI: 10.1109/22.989965.

[126] *Carefully Evaluate Your ADSL Line-Driver Efficiency | EE Times*. http://www.eetimes.com/document.asp?doc_id=1277049. (Accessed on 12/19/2016).

[127] E. Costa, M. Midrio, and S. Pupolin. “Impact of amplifier nonlinearities on OFDM transmission system performance”. In: *IEEE Communications Letters* 3.2 (Feb. 1999), pp. 37–39. ISSN: 1089-7798. DOI: 10.1109/4234.749355.

[128] T. Jiang and Y. Wu. “An Overview: Peak-to-Average Power Ratio Reduction Techniques for OFDM Signals”. In: *IEEE Transactions on Broadcasting* 54.2 (June 2008), pp. 257–268. ISSN: 0018-9316. DOI: 10.1109/TBC.2008.915770.

[129] X. Wu, P. Palmers, and M. S. J. Steyaert. “A 130 nm CMOS 6-bit Full Nyquist 3 GS/s DAC”. In: *IEEE Journal of Solid-State Circuits* 43.11 (Nov. 2008), pp. 2396–2403. ISSN: 0018-9200. DOI: 10.1109/JSSC.2008.2004527.

[130] P. Palmers and M. S. J. Steyaert. “A 10-Bit 1.6-GS/s 27-mW Current-Steering D/A Converter With 550-MHz 54-dB SFDR Bandwidth in 130-nm CMOS”. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 57.11 (Nov. 2010), pp. 2870–2879. ISSN: 1549-8328. DOI: 10.1109/TCSI.2010.2052491.

[131] C. H. Lin et al. “A 12 bit 2.9 GS/s DAC With IM3 < - 60 dBc Beyond 1 GHz in 65 nm CMOS”. In: *IEEE Journal of Solid-State Circuits* 44.12 (Dec. 2009), pp. 3285–3293. ISSN: 0018-9200. DOI: 10.1109/JSSC.2009.2032624.

[132] A. Van Den Bosch et al. “A 10-bit 1-GSample/s Nyquist current-steering CMOS D/A converter”. In: *Solid-State Circuits, IEEE Journal of* 36.3 (2001), pp. 315–324. ISSN: 0018-9200. DOI: 10.1109/4.910469.

[133] David Johns. *Analog integrated circuit design*. New York: John Wiley & Sons, 1997. ISBN: 0-471-14448-7.

[134] P. E. Allen. *CMOS analog circuit design*. New York: Oxford University Press, 2002. ISBN: 0195116445.

[135] H. Nyquist. “Certain Topics in Telegraph Transmission Theory”. In: *Transactions of the American Institute of Electrical Engineers* 47.2 (Apr. 1928), pp. 617–644. ISSN: 0096-3860. DOI: 10.1109/T-AIEE.1928.5055024.

[136] A. R. Hamade. “A single chip all-MOS 8-bit A/D converter”. In: *IEEE Journal of Solid-State Circuits* 13.6 (Dec. 1978), pp. 785–791. ISSN: 0018-9200. DOI: 10.1109/JSSC.1978.1052051.

[137] A. Abrial et al. “A triple low-power voltage output video 8-bit CMOS DAC”. In: *1988., IEEE International Symposium on Circuits and Systems*. June 1988, 2825–2828 vol.3. DOI: 10.1109/ISCAS.1988.15526.

[138] P. Holloway. “A trimless 16b digital potentiometer”. In: *Solid-State Circuits Conference. Digest of Technical Papers. 1984 IEEE International*. Vol. XXVII. Feb. 1984, pp. 66–67. DOI: 10.1109/ISSCC.1984.1156642.

[139] Chunlei Shi, J. Wilson, and M. Ismail. “Design techniques for improving intrinsic accuracy of resistor string DACs”. In: *ISCAS 2001. The 2001 IEEE International Symposium on Circuits and Systems (Cat. No.01CH37196)*. Vol. 1. May 2001, 400–403 vol. 1. DOI: 10.1109/ISCAS.2001.921877.

[140] Walt Kester. *Data conversion handbook*. Amsterdam Boston: Elsevier Newnes, 2005. ISBN: 978-0750678414.

[141] Richard Schreier and Gabor C. Temes. “DeltaSigma DACs”. In: *Understanding Delta-Sigma Data Converters*. Wiley-IEEE Press, 2005, pp. 219–255. ISBN: 9780470546772. DOI: 10.1109/9780470546772.ch7. URL: http://ieeexplore.ieee.org.ezproxy.is.ed.ac.uk/xpl/articleDetails.jsp?arnumber=5264511.

[142] H. Qian et al. “Digitally Controlled Micro-LED Array for Linear Visible Light Communication Systems”. In: *Photonics Journal, IEEE* 7.3 (June 2015), pp. 1–8. ISSN: 1943-0655. DOI: 10.1109/JPHOT.2015.2424398.

[143] J. Yew, S.D. Dissanayake, and J. Armstrong. “Performance of an experimental optical DAC used in a visible light communication system”. In: *Globecom Workshops (GC Wkshps), 2013 IEEE*. Dec. 2013, pp. 1110–1115. DOI: 10.1109/GLOCOMW.2013.6825141.

[144] J. Herrnsdorf et al. “Single-chip discrete multitone generation”. In: *Summer Topicals Meeting Series (SUM), 2015*. July 2015, pp. 47–48. DOI: 10.1109/PHOSST.2015.7248185.

[145] *Big Chip LEDs*. SBT-70. Rev. 3. Luminus Devices Inc. Apr. 2013.

[146] *OSRAM OSTAR Stage LE RTDUW S2W*. LE RTDUW S2W. Ver. 2.0. OSRAM Opto Semiconductors. Sept. 2014. URL: http://www.osram-os.com/Graphics/XPic7/00137402_0.pdf/LE%20RTDUW%20S2W%20-%20OSRAM%20OSTAR%20Stage.pdf.

[147] A. Mirvakili and V. J. Koomson. "High efficiency LED driver design for concurrent data transmission and PWM dimming control for indoor visible light communication". In: *2012 IEEE Photonics Society Summer Topical Meeting Series*. July 2012, pp. 132–133. DOI: 10.1109/PHOSST.2012.6280761.

[148] B. Serneels, M. Steyaert, and W. Dehaene. "A 237mW aDSL2+ CO Line Driver in Standard 1.2V 0.13μM CMOS". In: *2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*. Feb. 2007, pp. 524–619. DOI: 10.1109/ISSCC.2007.373525.

[149] P. Milder et al. "Design and simulation of 25 Gb/s optical OFDM transceiver ASICs". In: *2011 37th European Conference and Exhibition on Optical Communication*. Sept. 2011, pp. 1–3.

[150] A. Boni, A. Pierazzi, and D. Vecchi. "LVDS I/O interface for Gb/s-per-pin operation in 0.35-μm CMOS". In: *Solid-State Circuits, IEEE Journal of* 36.4 (2001), pp. 706–711. ISSN: 0018-9200. DOI: 10.1109/4.913751.

[151] *0.18 μm HV CMOS Process Parameters*. Rev. 2.0. Austria Micro Systems. Sept. 2011.

[152] K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland. "Characterisation and modeling of mismatch in MOS transistors for precision analog design". In: *IEEE Journal of Solid-State Circuits* 21.6 (Dec. 1986), pp. 1057–1066. ISSN: 0018-9200. DOI: 10.1109/JSSC.1986.1052648.

[153] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers. "Matching properties of MOS transistors". In: *IEEE Journal of Solid-State Circuits* 24.5 (Oct. 1989), pp. 1433–1439. ISSN: 0018-9200. DOI: 10.1109/JSSC.1989.572629.

[154] E. F. Schubert et al. "Temperature and modulation characteristics of resonant-cavity light-emitting diodes". In: *Journal of Lightwave Technology* 14.7 (July 1996), pp. 1721–1729. ISSN: 0733-8724. DOI: 10.1109/50.507950.

[155] *LVDS design notes*. SLLA014A. Texas Instruments. 2000. URL: http://www.ti.com/lit/an/slla014a/slla014a.pdf.

[156] *Test & Burn-In PGA Kit Sockets*. 200-6313-9UN-1900. TS-0675-09. 3M Electronic Handling and Protection Division. June 2001. URL: http://multimedia.3m.com/mws/media/1173330/3mtm-textool-tm-pga-test-and-burn-in-kit-socket-ts0675.pdf.

[157] *Golden DRAGON LD W5SM*. LDW5SM. Ver. 2.2. OSRAM Opto Semiconductors. Aug. 2015. URL: http://www.osram-os.com/Graphics/XPic5/00180790_0.pdf/LD%20W5SM.pdf.

[158] *XEM6310 User's Manual*. XEM6310-LX150. Opal Kelly Incorporated. Jan. 2013.

[159] *SourceMeter Source Measure Unit*. 2400. Rev. K. Keithley. Sept. 2011.

[160] D. O'Brien et al. "High-Speed Optical Wireless Demonstrators: Conclusions and Future Directions". In: *Lightwave Technology, Journal of* 30.13 (July 2012), pp. 2181–2187. ISSN: 0733-8724. DOI: 10.1109/JLT.2012.2193874.

[161] S. Rajbhandari et al. "A Multigigabit per Second Integrated Multiple-Input Multiple-Output VLC Demonstrator". In: *Journal of Lightwave Technology* 35.20 (Oct. 2017), pp. 4358–4365. ISSN: 0733-8724. DOI: 10.1109/JLT.2017.2694486.

[162] D. Raychaudhuri and N. B. Mandayam. "Frontiers of Wireless and Mobile Communications". In: *Proceedings of the IEEE* 100.4 (Apr. 2012), pp. 824–840. ISSN: 0018-9219. DOI: 10.1109/JPROC.2011.2182095.

[163] A. Burton et al. "Experimental Demonstration of 50-Mb/s Visible Light Communications Using 4 X 4 MIMO". In: *IEEE Photonics Technology Letters* 26.9 (May 2014), pp. 945–948. ISSN: 1041-1135. DOI: 10.1109/LPT.2014.2310638.

[164] D. Tsonev, S. Videv, and H. Haas. "Unlocking Spectral Efficiency in Intensity Modulation and Direct Detection Systems". In: *Selected Areas in Communications, IEEE Journal on* 33.9 (Sept. 2015), pp. 1758–1770. ISSN: 0733-8716. DOI: 10.1109/JSAC.2015.2432530.

[165] *Keysight 81150A and 81160A Pulse Function Arbitrary Noise Generators*. 81150A. Rev. 1.3. Keysight Technologies. 2016. URL: http://literature.cdn.keysight.com/litweb/pdf/5989-6433EN.pdf?id=1360537.

[166] Richard Schreier and Gabor C. Temes. "Implementation Considerations for ADCs". In: *Understanding Delta-Sigma Data Converters*. Wiley-IEEE Press, 2005, pp. 179–218. ISBN: 9780470546772. DOI: 10.1109/9780470546772.ch6. URL: http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=5264510.

[167] ITU-T. "G.975.1 : Forward error correction for high bit-rate DWDM submarine systems". In: (2004). URL: http://www.itu.int/rec/T-REC-G.975.1-200402-I/en.

[168] Chao-Hsin Wu et al. "4-GHz Modulation Bandwidth of Integrated 2 $\times$ 2 LED Array". In: *Photonics Technology Letters, IEEE* 21.24 (Dec. 2009), pp. 1834–1836. ISSN: 1041-1135. DOI: 10.1109/LPT.2009.2034385.

[169] M. R. Krames et al. “Status and Future of High-Power Light-Emitting Diodes for Solid-State Lighting”. In: *Journal of Display Technology* 3.2 (June 2007), pp. 160–175. ISSN: 1551-319X. DOI: 10.1109/JDT.2007.895339.

[170] *Models 1601 and 1611, High-Speed Photoreceivers*. 81150A. Rev. F. New Focus Inc. URL: http://assets.newport.com/webDocuments-EN/images/15178.pdf.

[171] *Agilent InfiniiVision 7000B Series Oscilloscopes*. 54695-97025. Rev. 1.3. Keysight Technologies. June 2010. URL: http://literature.cdn.keysight.com/litweb/pdf/54695-97025.pdf?id=1852824.

[172] *Product Datasheet Lena series*. CN12159_LENA-S-DL. Ledil Oy. Feb. 2014. URL: http://www.ledil.com/luopdf4.php?s=54&t=3345.

[173] C. Kottke et al. “1.25 Gbit/s visible light WDM link based on DMT modulation of a single RGB LED luminary”. In: *2012 38th European Conference and Exhibition on Optical Communications*. Sept. 2012, pp. 1–3. DOI: 10.1364/ECEOC.2012.We.3.B.4.

[174] *Thorlabs FL632.8-10*. FL632.8-10. Thorlabs. URL: https://www.thorlabs.com/newgrouppage9.cfm?objectgroup_id=1001&pn=FL632.8-10.

[175] *Thorlabs FB520-10*. FB520-10. Thorlabs. June 2003. URL: https://www.thorlabs.com/thorproduct.cfm?partnumber=FB520-10.

[176] *Thorlabs FB450-10*. FB450-10. Thorlabs. June 2003. URL: https://www.thorlabs.com/thorproduct.cfm?partnumber=FB450-10.

[177] Ákos Borbély, Árpád Sámson, and János Schanda. “The concept of correlated colour temperature revisited”. In: *Color Research & Application* 26.6 (2001), pp. 450–457. ISSN: 1520-6378. DOI: 10.1002/col.1065. URL: http://dx.doi.org/10.1002/col.1065.

[178] B. Ackermann et al. “Control of LEDs”. In: *Conference Record of the 2006 IEEE Industry Applications Conference Forty-First IAS Annual Meeting*. Vol. 5. Oct. 2006, pp. 2608–2615. DOI: 10.1109/IAS.2006.256907.

[179] S. Muthu, F. J. P. Schuurmans, and M. D. Pashley. “Red, green, and blue LEDs for white light illumination”. In: *IEEE Journal of Selected Topics in Quantum Electronics* 8.2 (Mar. 2002), pp. 333–338. ISSN: 1077-260X. DOI: 10.1109/2944.999188.

[180] W. O. Popoola. “Impact of VLC on Light Emission Quality of White LEDs”. In: *Journal of Lightwave Technology* 34.10 (May 2016), pp. 2526–2532. ISSN: 0733-8724. DOI: 10.1109/JLT.2016.2542110.

[181] *CDS Mini CCD Array Spectrometers*. CDS610. PB-13008-000 Rev.00. Labsphere Inc. 2015. URL: https://www.labsphere.com/site/assets/files/2502/cds_600_610.pdf.

[182] *E 1000 SpEctraL IrradIancE Receiver*. E1000. 231067v002. Labsphere Inc.