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Tuneable RF MEMS Components Using SU-8

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DECLARATION OF ORIGINALITY

I hereby declare that this thesis has been composed by myself and that except where stated, the work contained is my own. I also declare that the work contained in this thesis has not been submitted for any other degree or professional qualification except as specified.

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ABSTRACT

With the rapid progress in the wireless communication field, radio frequency micro-electro-mechanical systems (RF MEMS) are seen as one of the promising technologies to replace the existing high power communication systems. MEMS based tuneable devices such as varactors and phase shifters offer many advantages over their conventional diode-based counterparts including low loss, low power consumption and high linearity. MEMS varactors in particular can be integrated into many reconfigurable modules such as switching and reconfigurable matching networks. Moreover, distributed MEMS transmission line (DMTL) phase shifters with their linear phase characteristic can be applied to wideband phased array antennas for microwave medical imaging which requires beam steering and high gain antenna systems. This thesis focuses on the design and development of two RF MEMS devices which are a high tuning ratio digital MEMS varactor and a low frequency DMTL phase shifter using SU-8 polymer.

The design and simulation of a 4-bit and a 5-bit digital MEMS varactors have been carried out in the first phase of this study. One of the limitations of the digital MEMS varactors fabricated on silicon substrates is the high fringing field capacitance that reduces the overall capacitance ratios of the devices. To reduce the effect of the fringing fields, two methods have been proposed to elevate the varactors from the silicon substrate. In the first method, a 26.35 μm deep trench is etched in the silicon substrate under the 4-bit digital MEMS varactor which is able to achieve a high capacitance ratio of 35.7. In the 5-bit digital MEMS varactor design, SU-8 material is used to form a 20 μm thick separation layer between the varactor and the silicon substrate instead of the deep trench method applied in the 4-bit MEMS varactor. The simulated capacitance ratio of the 5-bit digital MEMS varactor is 34.8. Additionally, the SU-8 also serves as a sacrificial layer to release the MEMS bridges on the devices hence reducing the fabrication process compared to the conventional MEMS release process that uses oxide as the sacrificial material. To verify the performance of using the thick SU-8 dielectric layer in reducing the fringing field capacitance in the varactor design, single-bridge varactors with different lengths and widths have been fabricated and analysed. A novel truss bridge structure has been proposed in order to reduce the

pull-in voltage of the varactors. It is found that by using the truss structure, the measured pull-in voltage of the bridge can be reduced by 12.5% compared to the conventional solid fixed-fixed bridge structure. However, due to the high residual stress from the fabrication process which causes the bridge to warp over its width, the achievable average down-state capacitance of the fabricated single-bridge varactor is limited to 211 fF compared to the simulated value of 1.28 pF. Nevertheless, the capacitance ratio of the device fabricated on the SU-8 layer increases by 56.75% over a similar device fabricated without the polymer which proves that the fringing field capacitance has been reduced. Furthermore, fabrication of the single-bridge MEMS varactors on low-resistivity silicon has been carried out with the use of SU-8 as the passivation layer without affecting the performances of the varactors. This finding can lead to the realisation of low-cost MEMS varactors in the future.

The second part of this thesis investigates the development of distributed MEMS transmission line (DMTL) phase shifters for operation in the frequency range of 2 GHz to 4 GHz (S-band). The proposed phase shifters are a 2-bit and 3-bit digital DMTL phase shifters. One of the potential applications of the proposed phase shifters is for phased array antenna systems for microwave head imaging that requires wideband performance. The 2-bit and 3-bit DMTL phase shifters have been designed and simulated with 41 MEMS bridges and 105 MEMS bridges respectively. The simulated phase shifts of the 2-bit phase shifter design are 0^0, 90^0, 180^0 and 270^0 whereas for the 3-bit phase shifter, 8 phase shifts have been achieved namely 0^0, 45^0, 90^0, 135^0, 180^0, 225^0, 270^0 and 315^0. To validate the performance of the proposed low frequency DMTL phase shifter, the 2-bit phase shifter design has been fabricated and analysed. The measured impedance matching of the phase shifter shows good performance with reflection coefficients of less than -10 dB across the operating frequency range for all the states of the phase shifter. The measured differential phase shifts of the device are 0^0, 17.89^0, 34.51^0 and 52.39^0. The lower measured differential phase shifts compared to the simulated values can be attributed to the warping of the bridges over their width which causes a formation of an air gap between the bridge and dielectric layer hence reducing the down-state capacitance of the varactors in the phase shifter. Nevertheless, this is the first DMTL phase shifter to achieve a maximum differential phase shift of 52.39^0 at 2.45 GHz. Based on the measured differential

phase shifts, the phase shifter can provide a maximum steering angle of $\pm 5.73^0$ for a 4-element phased array antenna at 2.45 GHz. The maximum measured transmission loss of the phase shifter is -10.51 dB at 2.45 GHz. The high loss of the phase shifter is due to the skin depth effect since the co-planar waveguide (CPW) transmission line of the phase shifter is fabricated using 300 nm thick aluminium. Therefore, further investigation has been carried out to provide better estimation of the transmission loss of the phase shifter by fabricating a CPW transmission line with the same configuration to that of the transmission line in the fabricated phase shifter by using 2 µm thick aluminium. The measured loss of the transmission line is -2.39 dB which shows significant improvement over the loss obtained from the phase shifter. Moreover, several CPW transmission lines with different centre conductor's widths have been fabricated and analysed to further reduce the losses of the transmission lines. An attenuation loss of only 0.122 dB/cm has been achieved using a 500 µm-width centre conductor in the fabricated CPW transmission line which can lead to the realisation of a low-loss DMTL phase shifter for low microwave frequency range.

The characterisation and optimisation of the varactors and phase shifters using SU-8 provide the initial step towards the development of tuneable RF MEMS devices for wide range of applications including wireless communications and radar systems. Moreover, the proposed DMTL phase shifters for operation at the lower end of microwave spectrum particularly in the frequency range of 2 GHz to 4 GHz are vital for the realisation of wideband phased array antennas for microwave medical imaging applications.

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LIST OF ACRONYMS AND ABBREVIATIONS

CMOS	=	Complementary Metal–Oxide–Semiconductor
CPW	=	Co-planar Waveguide
CMP	=	Chemical Mechanical Planarisation
DMTL	=	Distributed MEMS Transmission Line
FET	=	Field Effect Transistor
HRS	=	High Resistivity Silicon
ITU	=	International Telecommunication Union
LSI	=	Large Scale Integrated
MAM	=	Metal-Air-Metal
MEMS	=	Micro-electro-mechanical Systems
MIM	=	Metal-Insulator-Metal
MMIC	=	Monolithic Microwave Integrated Circuit
PEB	=	Post Exposure Bake
PECVD	=	Plasma Enhanced Chemical Vapour Deposition
RF	=	Radio Frequency
Si_3N_4	=	Silicon Nitride
SiO_2	=	Silicon Dioxide
TL	=	Transmission Line
TaN	=	Tantalum Nitride
TL	=	Transmission Line
UV	=	Ultra Violet

Chapter 1: Introduction

The overview and motivation of this research for tuneable RF MEMS components are presented in this chapter.

1.1 Research Motivation

Nowadays, the telecommunications industry has grown and changed rapidly with the introduction of new and advanced technologies. Wireless communication devices such as smartphones, tablets, and laptops are now seen as necessities in life. People use these devices in their daily lives for communications, businesses, and entertainments. As a result, demands for more applications and functionalities particularly on wireless devices are increasing. To meet these demands, new frequency bands have been allocated by the International Telecommunication Union (ITU) to increase the capacity and speed of the existing wireless connections. However, this also leads to a huge increase of electronic components in the wireless device. Therefore, small and low power RF transceivers capable of multiband operation are required.

As shown in Figure 1.1, the existing RF transceivers consist of many off-passive components and several Large Scale Integrated (LSI) chips. By increasing the number of supported frequency bands in wireless devices, the number of components in the circuit increases proportionally, hence making the transceivers larger in size. Moreover, this also increases power consumption and shortens the battery life of the devices. In order to enable multiband operation without having to increase the size of the transceivers, reconfigurable RF circuits such as reconfigurable antennas can be utilised where they can be reconfigured to operate at different frequency bands. In addition, these reconfigurable components can also be applied in wideband microwave imaging systems. This can lead to better imaging systems by providing improved sensing and detection capability. However, the design and implementation of these reconfigurable devices are very challenging, which require a significant amount of research.

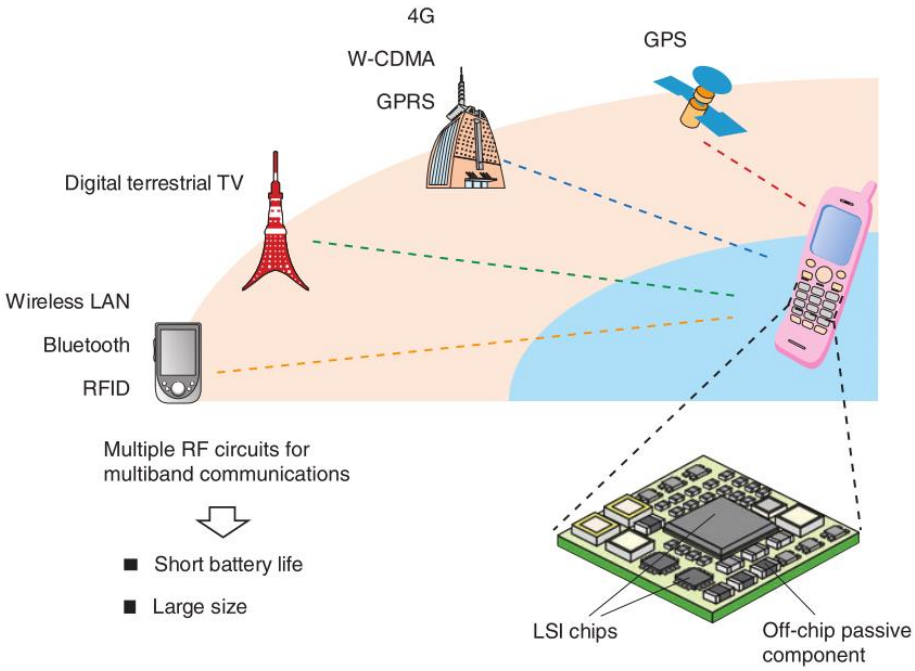


Figure 1.1: Overview of a wireless connection for a mobile device [1].

Micro-electro-mechanical systems (MEMS) are the integration of mechanical elements, sensors, actuators and electronics on common substrates through microfabrication technologies. It is a wide field of study where works on RF MEMS represents only a small part of the field. To date, RF MEMS devices such as switches, varactors, inductors, filters, resonators, impedance matching networks and phase shifters have been actively developed and investigated [1]–[4]. In general, RF MEMS devices are mechanically actuated by external force such as electrostatic, magnetostatic or piezoelectric. The micromechanical components are mainly fabricated using a surface micromachining process.

While the current available PIN diodes and field effect transistor (FET) components suffer from a high loss and narrow bandwidth, RF MEMS devices have shown their superiority by offering more bandwidth and lower loss. In addition, since MEMS devices do not have a semiconductor junction which is often associated with non-linearity, any intermodulation distortion can be eliminated. Furthermore, RF MEMS devices are compatible with the existing integrated circuit (IC) and monolithic

microwave integrated circuit (MMIC) fabrication process which can eliminate the off-chip passive components required in the design, hence reducing the interconnection loss. As a result, RF MEMS technology is seen as the best solution for future wireless communication devices.

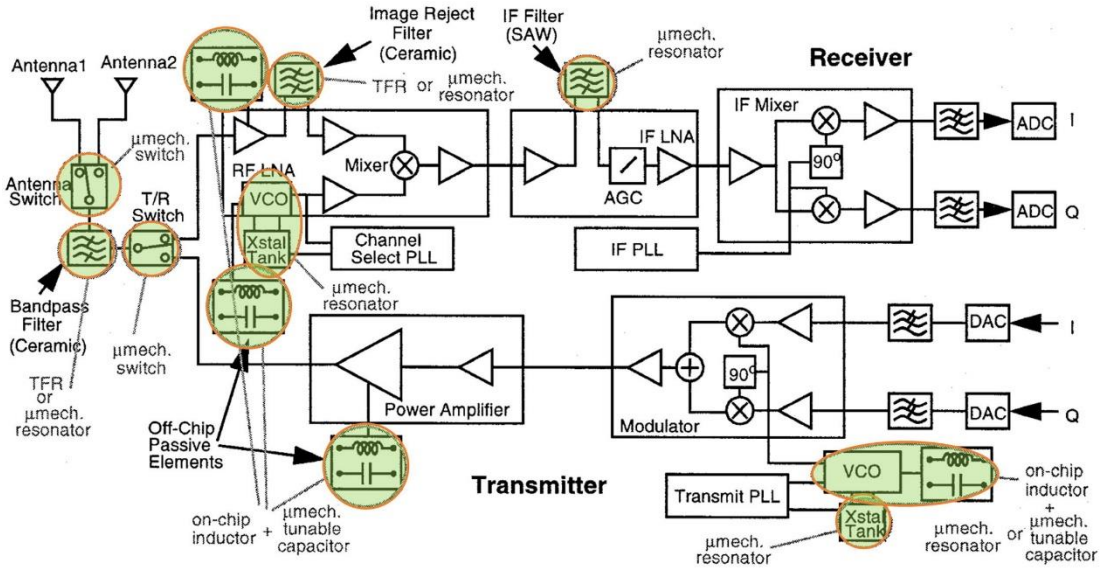


Figure 1.2: Schematic block diagram of an RF transceiver [4].

Figure 1.2 shows the schematic block diagram of a typical RF transceiver design. The components circled should be replaced with the equivalent RF MEMS components in order to improve the performance of the system. Tuneable MEMS components such as varactors and phase shifters are parts of the main components in the wireless transceiver systems for various applications ranging from telecommunication to medical imaging. For example, RF MEMS varactors can be utilised to build tuneable filters, impedance matching networks and phase shifters. Moreover, high tuning ratio MEMS varactors can provide better tuneable performance in a reconfigurable circuit. Another motivation of this research is to develop a MEMS phase shifter that can operate at the lower microwave frequency band of 2 GHz to 4 GHz in order to realise a phased array antenna system for the radar-based microwave medical imaging. Although there are many commercially available phase shifters in the market, most of them have limitations including narrow-band and are of constant-phase type which can lead to the beam squinting problem when implemented on ultra-wideband phased array antennas [5]. To address this issue, phase shifters with a linear-phase design such as distributed MEMS transmission line (DMTL) phase shifters are required. Although

there are many DMTL phase shifters that have been proposed in the literature, none of them have been developed and optimised to work at the frequency band of 2 GHz to 4 GHz used by the microwave head imaging systems [6]–[9].Therefore, the work presented in this thesis is the first demonstration of a DMTL phase shifter to operate at the lower microwave frequency band unlike most DMTL phase shifters in the literature which had been built for operations above 10 GHz.

Polymers such as SU-8 are widely used in MEMS devices to serve as a photo-resist sacrificial mask and to construct a high aspect ratio structure due to its thermal and chemical stability in the fabrication process [10]–[14]. Recently, SU-8 was used as a passivation layer to elevate a co-planar waveguide (CPW) transmission line for realising a low loss transmission line using a low resistivity silicon wafer (ρ<100 Ω·cm) [15], [16]. Moreover, it has been reported in [3], [17] that SU-8 has been used for both lateral support for an RF MEMS switch as well as sacrificial layer. In this thesis, SU-8 is used as a base structure to elevate the proposed MEMS varactor from the silicon substrate which can reduce the parasitic and fringing field capacitance. As a result, a high capacitance ratio MEMS varactor can be realised. Additionally, the varactor can also be fabricated on low resistivity silicon without experiencing a high loss due to the separation layer provided by the SU-8. Moreover, SU-8 also serves as a sacrificial layer and supporting anchor which can simplify the fabrication process of the varactor compared to the typical MEMS release process using oxide.

1.2 Aims and Objectives

The objectives of the research are categorised into four main groups.

1) *Design and simulation of a high tuning range digital RF MEMS varactor*.
   This research focuses on reducing the parasitic and fringing field capacitance by elevating the proposed 4-bit and 5-bit MEMS varactors from the silicon substrate using a polymer, SU-8, to produce high capacitance ratio varactors. Investigations on the mechanical aspect of the truss bridge implemented in the varactors and RF characterisations of the varactors are also conducted.
2) *Fabrication and measurement of a single-bridge RF MEMS varactor*.

The fabrication of a single-bridge MEMS varactor with two different types of bridges namely truss and fixed-fixed configurations of various length dimensions is carried out. The fabrication process is simplified by optimising SU-8 to provide multiple functionalities including as a thick separation layer, a sacrificial layer during the release step and an anchor for the varactor. The proposed truss structure for the bridge is characterised and compared to the standard fixed-fixed bridge construction.

3) *Design and simulation of a DMTL phase shifter for S-band application.*
   A novel wide-band DMTL phase shifter for operation at microwave frequency band of 2 - 4 GHz is designed and simulated for a 2-bit and 3-bit DMTL phase shifter designs. Two-state capacitance MEMS switches are utilised to eliminate the series capacitor typically implemented in digital MEMS phase shifters such as metal-insulator-metal (MIM) and metal-air-metal (MAM) capacitors to reduce the overall phase shifter loss and complexity of the fabrication process.
4) *Fabrication and measurement of a 2-bit DMTL phase shifter.*
   The fabrication process of a 2-bit DMTL phase shifter is carried out in this study. The mechanical and RF characterisations are conducted on the fabricated phase shifter. In addition, investigations on the transmission line loss for different CPW transmission line (TL) configurations are carried out by varying the aluminium thickness and width of the centre conductor of the CPW transmission line used in the phase shifter.

1.3 Contributions

The following contributions can be attributed to this research:

1) Design and simulation of a 3-bit and 4-bit high capacitance ratio digital MEMS varactors using SU-8.
2) The use of SU-8 material to form a thick separation layer to elevate the proposed varactors from the silicon substrate where the parasitic and fringing field capacitance is reduced hence improving the overall capacitance ratios of the varactors. Additionally, the thick SU-8 layer also permits the fabrication of

MEMS varactors on a low-resistivity silicon substrate which can reduce the cost of the varactors.

3) The use of SU-8 to serve as a sacrificial layer and supporting anchor for the realisation of the proposed MEMS varactors and DMTL phase shifters which can simplify the fabrication process.
4) Design and simulation of a 2-bit and 3-bit novel wideband DMTL phase shifters for S-band applications. This is the first demonstration of DMTL phase shifters at this frequency band.
5) Fabrication of a 2-bit DMTL phase shifter with a maximum differential phase shift of 52.39^0 which is the highest reported differential phase shift by a DMTL phase shifter at 2.45GHz to date.
6) Investigation on the performance of a meandered CPW transmission line used in the proposed DMTL phase shifter designs.
7) Investigation on the attenuation loss of different CPW transmission line configurations which can be utilised in low-loss DMTL phase shifters in the future.
8) Comparison of the proposed truss bridge structure and conventional fixed-fixed design for the bridges of the varactors in terms of their mechanical behaviour.

1.4 Overview of the Thesis

The remainder of this thesis is organised into six chapters as follows:

Chapter 2 provides an overview of two RF MEMS devices which are MEMS varactors and MEMS phase shifters. It highlights the variety of the designs and research that have been carried out to improve the performance of the devices. Subsequently, the motivations of designing a high tuning MEMS varactor and low-frequency DMTL phase shifter are explained.

Chapter 3 introduces the basic theory and design of MEMS capacitive switches and MEMS varactors. It presents the design of a high tuning ratio varactor using SU-8 polymer as a base structure to reduce the fringing and parasitic capacitance due to the silicon substrate under the varactor. The proposed varactor designs are investigated

and verified with simulation tools for both the mechanical behaviour and RF performance.

Chapter 4 describes the fabrication procedure of a single-bridge MEMS varactor and the challenges faced during the fabrication process. It describes the mask design and the steps taken to fabricate the novel SU-8 based MEMS varactor. The fabrication challenges and solutions taken to mitigate the issues have also been demonstrated.

Chapter 5 presents the theory, design, and simulation of a 2-bit and 3-bit DMTL phase shifters for S-band application. The sizes of the devices are optimised and their performances have been investigated in terms of the RF characteristics and mechanical aspects of the phase shifters using simulation tools.

Chapter 6 describes the fabrication of the 2-bit DMTL phase shifter presented in Chapter 5. The fabrication procedure has been optimised to realise a two-state capacitance MEMS switch for the DMTL phase shifter. Moreover, investigations on the CPW transmission line loss of the phase shifter have been carried out to analyse the loss in terms of metal thickness and the CPW transmission line configurations due to the design and fabrication technique used.

Chapter 7 presents the conclusion of the objectives and achievements of the thesis. The chapter also suggests some topics for future research.

1.5 Publications

In the course of this research, the following journals and conference papers have been published and submitted.

Journal papers

1) Ramli, N. A., Arslan, T., Haridas, N., & Zhou, W. (2017). "Design, simulation and analysis of a digital RF MEMS varactor using thick SU-8 polymer". Microsystem Technologies.
2) Ramli, N. A., Arslan, T., & Haridas, N.(2017). "A 3 bit S-Band Distributed MEMS Phase Shifter: Design and Simulation". Microsystem Technologies. (Accepted with revisions)

3) Ramli, N. A., Arslan, T., & Haridas, N.(2018). “Fabrication of a 2-bit DMTL phase shifter for wideband phased array antenna” Journal of Microelectromechanical Systems. (Submitted)

Conference papers

1) N. A. Ramli, T. Arslan, N. Haridas and W. Zhou, "Design and modelling of a digital MEMS varactor for wireless applications," 2016 17th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), Montpellier, 2016, pp. 1-5. doi: 10.1109/EuroSimE.2016.746338

2) N. A. Ramli, T. Arslan, N. Haridas and Wei Zhou, "Design and simulation of a high tuning range MEMS digital varactor using SU-8," 2016 Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP), Budapest, 2016, pp. 1-6. doi: 10.1109/DTIP.2016.7514842

3) N. A. Ramli, T. Arslan, "Design and Simulation of a 2-bit Distributed S-band MEMS Phase Shifter," 2017 18th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystems (EuroSimE), Dresden, 2017, pp. 1-5.

4) N. A. Ramli, T. Arslan, and N. Haridas, "Design and simulation of a 3-Bit S-Band Distributed MEMS Phase Shifter for Wideband applications," 2017 Symposium on Design, Test, Integration and Packaging of MEMS/MOEMS (DTIP), Bordeaux, 2017.

Chapter 2: Literature Review

2.1 Introduction

This chapter presents the literature review of two main tuneable RF MEMS components for wireless applications which are MEMS varactors and MEMS phase shifters. Firstly, this chapter describes the existing designs and implementations of MEMS variable capacitors which include several design considerations such as the capacitance ratio, linearity, self-resonance and quality factor. There are two main configurations for MEMS varactors namely analogue and digital designs. Due to limited capacitance ratios of analogue MEMS varactors, digital MEMS varactors are usually preferred in the implementation of tuneable devices.

The second part of this chapter provides the overview of a phase shifter design. Furthermore, several types of phase shifters are presented focusing on the ones that integrate MEMS switches in their designs. The performances of the phase shifters are evaluated in terms of their operating frequency band, transmission loss and phase shift. Although analogue DMTL phase shifters can obtain an infinite number of phase shifts, their limited capacitance ratio, C_r of 1.3 reduces the maximum phase shift that can be achieved over similar digital MEMS phase shifter designs. As a result, this research will focus on the development of a digital DMTL phase shifter.

2.2 MEMS Varactors

MEMS varactors are essential components in an RF transceiver block. The implementation of RF MEMS components in wireless devices can reduce the number of on-chip components in the circuit. MEMS varactors offer a high tuning ratio, low loss and high-Q factor which are the main requirements to realise multiple bands and reconfigurable circuits. This allows the circuits to be reconfigured for operation over a wide range of frequency bands. In addition, their compatibility with complementary metal–oxide–semiconductor (CMOS) process makes MEMS varactors the best

candidate to replace solid-state components in future communication technologies. Basically, there are three different categories of RF MEMS varactors:

1. MEMS parallel-plate varactors with a vertical displacement
2. MEMS interdigitated varactors with a lateral displacement
3. MEMS switched capacitor bank

Moreover, MEMS varactors can be further divided into two main groups which are analogue and digital. Analogue varactors provide a continuous capacitance change by increasing the applied DC bias voltage which results in an infinite number of capacitance values. Several analogue MEMS tuneable varactors have been demonstrated in the literature [1], [18], [19]. However, the performances of these devices have been limited by a low tuning range of less than 1.5. This limitation is due to the pull-in effect experienced by the bridges in the varactors [1]. At two-thirds of the air gap between the bridge and pull-down electrode, the increase of the electrostatic force is greater than the restoring force of the bridge causing the bridge to collapse to the down-state position. However, this pull-in effect that typically hampers the realisation of high tuning analogue varactors can be resolved using a digital varactor design. Generally, digital varactors can be viewed as on and off switches. They are off when there is no DC voltage applied and will be on when there is sufficient DC voltage to actuate them. The off and on conditions will produce two different values for the low and high capacitances for a single digital varactor bridge. Subsequently, a larger tuning range digital MEMS varactor can be achieved with a combination of several bridges in the varactor design.

Basically there are four different forces that cause mechanical actuations for MEMS devices namely electrostatic, magnetostatic, piezoelectric, and thermal. Among all these, electrostatic actuation is the most common implementation as it is easy to design and can produce small and robust components. In addition, this method of actuation is relatively fast and consumes almost no control power. Moreover, it only requires some residual energy to hold the membrane in MEMS devices during actuation [20]. However, the main challenge with the electrostatic actuation is that it is difficult to obtain a low actuation voltage with a good and high isolation especially for MEMS switches due to the small gap distance between the actuation electrodes.

Moreover, the self-actuation effect caused by a passing RF signal due to the low spring constant of the MEMS bridge can be a major problem for the devices. On the other hand, the piezoelectric actuation occurs when there is a differential contraction between two or more materials due to the piezoelectric effect and causes the structure to bend. The advantage of this actuation is that a fast actuation speed can be achieved, while its drawback is mostly associated with the parasitic thermal actuation due to the thermal expansion of different layers in the MEMS structures [20]. This issue can be avoided by implementing a symmetrical structure with respect to the thermal characteristics of the layers. However, integrating piezoelectric materials into a MEMS environment is very challenging especially in terms of the fabrication process because piezoelectric films are difficult to pattern and the processing step involves a high crystallisation temperature.

The advantages of having a low control voltage and high contact force in MEMS devices can be obtained by both the magnetic and electro thermal actuations [20]. However, they suffer from a slow actuation speed and high power dissipation during the actuation state compared to the electrostatic and piezoelectric actuations. Furthermore, magnetic actuators are difficult to fabricate since they require a 3-D coil with a soft-magnetic core and they tend to be large in size.

The next section will highlight several methods that have been proposed in MEMS varactor designs to achieve high tuning range performance.

2.2.1 Two Parallel Plates MEMS Varactors with a Vertical Displacement

Of all the existing MEMS varactor structures, the parallel plate configuration is the most commonly used design to date due to its simple fabrication process. This structure consists of one movable top plate or bridge, one fixed bottom plate and an air gap in between. In terms of actuation methods, electrostatic mechanism is the most prevalent technique compared to other approaches due to its simplicity and virtually low power requirement [1], [21]. However, this method results in the well-known pull-in effect that forces the top membrane to snap down after reaching two-thirds of its initial height. Although this phenomenon does not significantly deteriorate the MEMS switches operation, it can be a major limitation to variable capacitor designs to achieve

a high capacitance ratio and linearity [22], [23]. When a DC voltage is applied between the plates, electrostatic force is generated and pulls the top plate towards the bottom plate thus increasing the capacitance. At the same time, the mechanical restoring force, F_m of the top membrane is also induced. The restoring force F_m is linearly proportional to the spring constant of the membrane, K_m and distance, X. At the equilibrium state as shown in Figure 2.1, the electrostatic force is equal to the restoring force as described in the equations below.

$$F_e = \left[\frac{\varepsilon_0 A V^2}{2g^2}\right] \tag{2.1}$$

$$F_m = K_m X \tag{2.2}$$

By further increasing the DC voltage, a mechanical instability will occur at two-thirds of the total air gap distance of the moving bridge. The top plate will no longer be at the equilibrium position and will snap down to the bottom plate. This pull-in effect significantly reduces the total capacitance ratio of a typical MEMS varactor to about 50% or 1.5 and even less in practical applications due to the parasitic and fringing field capacitance. Nevertheless, fabrications of parallel plate varactors can easily be carried out using a surface micromachining process.

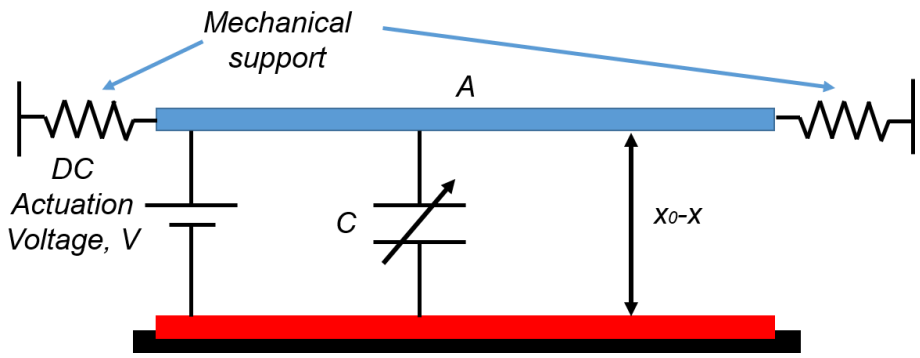


Figure 2.1: MEMS parallel plate varactor [23].

2.2.2 Three Parallel Plates MEMS Varactor

An extended high tuning range MEMS capacitor using a standard parallel plate structure was first developed in [19]. Three-parallel plate design was implemented

using a standard polysilicon micromachining process (MUMP's) which can produce a larger tuning range than 1.5 as shown in Figure 2.2. When the three-parallel plate tuneable capacitor where under zero bias condition, the distances between the parallel plates are d_1 and d_2 respectively.The top and bottom plates of the capacitor are fixed mechanically while the middle plate is suspended by two spring constants of $k/_2$ each. If a bias voltage, $V_1(t) = V_1$ is applied while $V_2(t) = 0\,V$, the electrostatic force will cause the movable plate to move towards the top plate. Likewise, if a bias voltage is applied such that $V_2(t) = V_2$ while V_1 (t) = 0 V, the electrostatic force will cause the movable plate to move towards the bottom plate. While under the DC condition, $x(t) = x$, $V_{1(t)} = V_1$, $V_{2(t)} = V_2$ the equilibrium between the electrostatic and the spring forces can be expressed by

$$kx = \frac{1}{2}\frac{dC_D}{dx}V_1^2 + \frac{1}{2}\frac{dC_P}{dx}V_2^2$$

$$= -\frac{1}{2}\frac{\epsilon_d A V_1^2}{(d_1 + x)^2} + \frac{1}{2}\frac{\epsilon_d A V_1^2}{(d_1 - x)^2} \qquad (2.3)$$

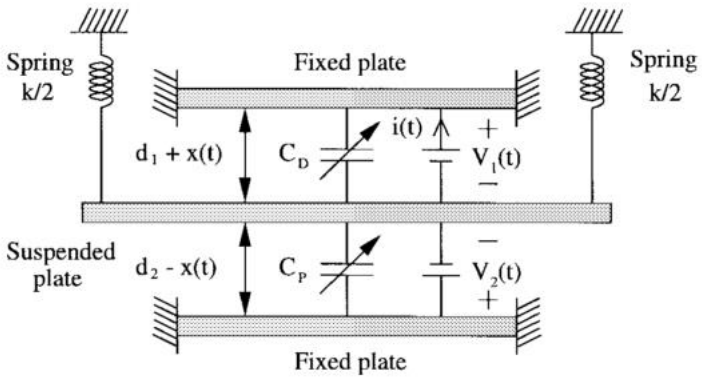


Figure 2.2: Three parallel plate varactor [19].

Similar to the two parallel plate configuration, the maximum capacitance of this type of capacitor is still limited to $3C_D/2$ whereas the minimum capacitance is $3C_D/4$ if the distances d_1 and d_2 are the same. In this case, the maximum theoretical capacitance range that can be tuned for the three parallel plate model has increased to 2:1 compared to 1.5:1 for the two parallel plate design. The tuneable capacitor consists of three layers of polysilicon (poly 1, poly 2, and poly 3) and a layer of gold. The measured tuning

range of this capacitor is 1.87:1 which is slightly less than the theoretical value due to the existence of parasitic and fringing field capacitances. The reported Q-factor of the varactor is 15.4 at 1 GHz. The measured capacitance under zero bias condition is 4 pF. Meanwhile, the measured capacitances when $V_1(t) = 1.8\,V$ and $V_2(t) = 0\,V$, and when $V_1(t) = 0\,V$ and $V_2(t) = 4.4\,V$ are 6.4 pF and 3.4 pF respectively.

2.2.3 Wide Tuning Range MEMS Varactor using Different Gap Spacing

Several extended tuning range MEMS varactors were developed by using a double air gap structure as shown in Figure 2.3 [18], [24], [25]. The bridge in this structure was independent from the bottom coplanar waveguide (CPW) transmission line and actuated by biasing the bridge and ground of the transmission line. Unlike the conventional flat bridge, the bridge in the varactors was modified to make its centre part closer to the centre of the CPW transmission line. When a bias voltage is applied between the ground of the CPW transmission line and the bridge, the bridge deflects and makes a contact with the centre of the transmission line. The height of the bridge

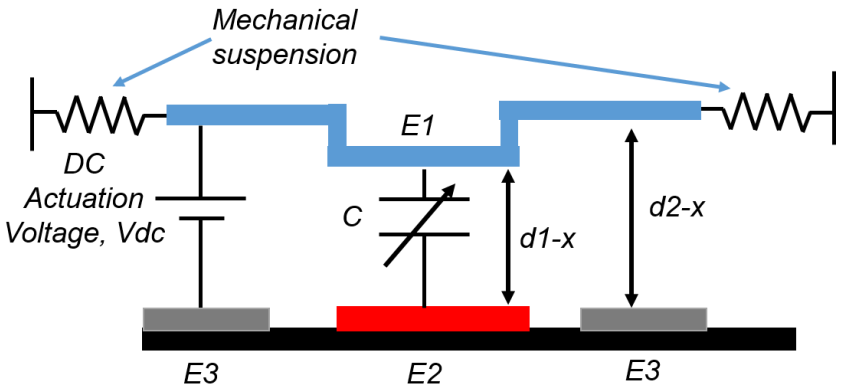


Figure 2.3: Wide tuning range two parallel plate varactor [24].

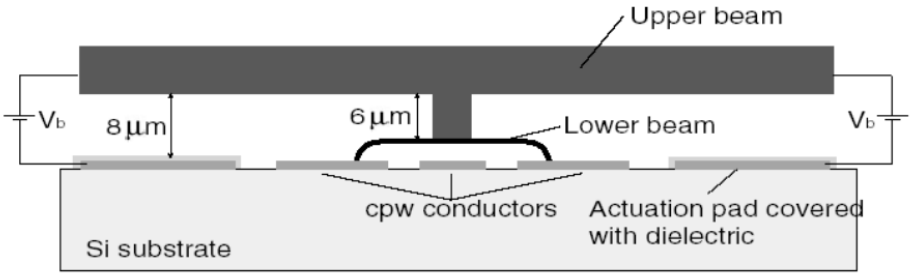


Figure 2.4: Fixed – fixed lower beam varactor [21].

can be accurately controlled to eliminate the pull-in effect hence improving the tuning range of the varactors.

A MEMS varactor which employs the extended approach or the dual gap structure in its design was reported in [21] where it was fabricated using two metals and two sacrificial layers process. This structure is used to increase the capacitance value of the varactor and to overcome the pull-in effect. As a result, the measured capacitance shows a tuning range of 300% [21]. As shown in Figure 2.4, the structure consists of two beams which form the lower and upper beams of the varactor. The lower beam is suspended over a CPW transmission line with a 2 µm air gap using a folded suspension lower beam design. Meanwhile, the upper beam is implemented using a fixed-fixed beam design with an air gap of 6 µm over the lower beam. The CPW transmission line is covered with a dielectric layer to prevent a direct contact between the centre conductor of the transmission line and the lower beam. When a DC bias is applied between the upper beam and the actuation pad, the lower beam deflects due to its lower spring constant value compared to the upper beam. The upper beam will collapse when it reaches a distance of 2.5 µm in the downward direction which occurs when the lower beam touches the centre conductor of the CPW transmission line. However, this design has several limitations due to the fabrication process such as the stress, thickness, and roughness of the dielectric layer. Furthermore, the non-linearity of the tuning capacitance also becomes a drawback for this varactor.

2.2.4 Interdigitated 'Comb' MEMS Varactors with a Lateral Displacement

The second category of RF MEMS varactors is a lateral displacement variable capacitor which typically consists of a series of interdigitated fingers or two electrodes in a comb structure. This type of capacitor is also known as comb drive varactors. The comb structure uses the tuning gap between each pair of the fingers to create capacitance in the device. One set of the comb fingers is suspended over the substrate and the gap between the fingers is kept constant [26]. When applying a DC voltage, the electrostatic force between the fingers causes the suspended fingers to move thus increasing the overlap and the capacitance of the device. It is possible for the comb drive varactors to achieve a tuning ratio of 8.4:1 with a low operating voltage and higher Q factor compared to the parallel plate varactor design [27]. However, these varactors have several limitations including complex geometries and challenging fabrication processes especially for the realisation of a large tuning range varactor. Moreover, a high tuning comb drive varactor requires a large comb separation hence increasing the overall device size.

An analogue comb drive varactor has been designed for tuneable filters in [27]. It was fabricated with a thick silicon device layer suspended on a glass substrate by using the double sided metallisation process. This process can reduce the out of-plane-bending due to the mismatched stress. As a result, 8.4 to 1 tuning range has been achieved with a continuous tuning range from 1.4 pF to 11.9 pF and a Q factor above 100 for 200 to 400 MHz applications.

A high capacitance ratio tuneable capacitor with excellent linearity performance is essential for RF voltage controlled oscillators (VCO). An interdigitated comb MEMS varactor developed for RF VCO in 2GHz RF transceiver was reported in [28]. It consists of a single suspended plate with 608 comb fingers. The plate which is made of 6 μm thick crystal silicon is suspended over a glass substrate using a silicon glass bonding process and chemical mechanical planarisation (CMP). The nominal capacitance of the varactor is 1.4 pF when the tuning voltage is 0 V and increases by 10% linearly at 8 V. The Q factor of this device is 4 at 2 GHz.

2.2.5 MEMS switched capacitor bank

Another approach to realise a high tuning range MEMS varactor is by using a digital design where the mechanical stability issue that limits the performance of an analogue varactor design could be totally eliminated [29]–[32]. A typical digital MEMS varactor design is made of a switched capacitor bank where several MEMS switches are arranged in an array configuration according to a binary weighted scheme. Each of the individual varactor is operated as on and off states similar to a typical MEMS switch to produce the minimum and maximum capacitance values. The total capacitance can then be achieved by summing all the capacitances produced by the varactors.

In 1999, a digital bank MEMS varactor was first developed in [29] which can reach a tuning range of 22:1 from 1.5 pF to 33.2 pF. In Figure 2.5, the capacitor was constructed using a bi-stable MEMS membrane capacitor that acts like an on and off MEMS switch. It has a binary weighted capacitance selection in a 6-bit capacitor design. The bits are 0.5 pF, 1 pF, 2 pF, 4 pF, 8 pF and 16 pF. The construction of this varactor consists of one fixed capacitor and one or several MEMS switches in each bit where the total capacitance of each bit is the series combination of the two types of capacitors. The largest bit of 16 pF is obtained by the combination of six switchable MEMS capacitors (3.4 pF each for a total of 20 pF) in series with a fixed capacitor of 74 pF. On the other hand, the smallest bit is made up of one switchable MEMS capacitor in series with a 0.6 pF fixed capacitor that produces 0.5 pF capacitance value. The MEMS switch is actuated with a DC control voltage that controls each of the bit in the MEMS switch.

A 3-bit and 4-bit digital MEMS varactors have been developed in a circular configuration to minimise the series inductance which increases the upper operating frequency of the devices [32]. The proposed design can be used in either planar circuits or in 3-D resonators with cavity posts as shown in Figure 2.6. A DC bias voltage is applied at each of the binary weighted segment to control the bridges. Furthermore, each binary weighted bit is divided into halves which are arranged symmetrically in a circular configuration to maintain the current symmetry. The result shows that the capacitance ratio obtained is 4 from 1 pF to 3.75 pF for the 3-bit design and 1.25 pF to 3.8 pF for the 4-bit design.

2.2.6 Proposed Digital MEMS Varactor

By utilising the advantages of digital MEMS varactor design described in the previous section, a high capacitance ratio digital MEMS varactor is proposed in this research. The main focus of this work is to reduce the parasitic and fringing field capacitance between the varactor and the silicon substrate in order to increase the capacitance ratio of the varactor. Two methods are evaluated in the varactor design in the simulation work. For the first method, a deep trench is etched in the silicon substrate for a 4-bit digital MEMS varactor. Alternatively, a thick separation layer is implemented in a 5-bit digital MEMS varactor using SU-8 instead of the deep trench method proposed in the 4-bit design. Due to these two techniques, a high capacitance ratio MEMS varactor can be achieved compared to a similar design without the use of the trench and the SU-8 layer. Subsequently, a single-bridge MEMS varactor is

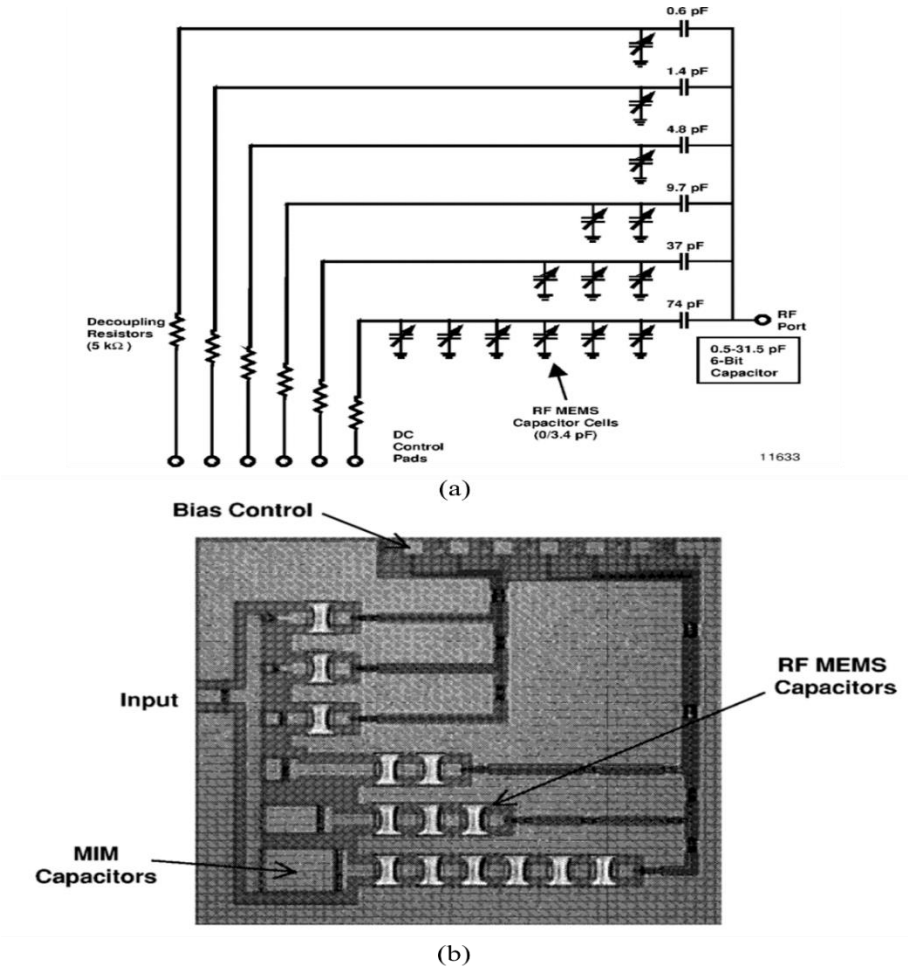


Figure 2.5: Digital MEMS varactor [29].

fabricated to verify the effectiveness of using the thick SU-8 layer to reduce the parasitic and fringing field capacitances caused by the use of silicon substrates in MEMS varactor designs.

2.3 Overview of the Types of RF Phase Shifters

This section provides the overview of various types of the existing phase shifters in the literature. A phase shifter is a two-port network device that provides a phase difference between the input and output signals which can be controlled by a control signal. Both the input and output ports of a phase shifter should have excellent impedance matching to ensure most of the transmitted signal is delivered to its intended loads such as antennas. Phase shifters are widely used in modern phased array antenna applications for electronic beam steering. By varying the progressive phase between the antenna elements in an array system, the array's main radiation beam can be steered to any direction without using any mechanical structure to physically rotate the antennas. A typical phase array antenna may have several to thousands of elements fed individually by a phase shifter. Therefore, phase shifters with a low loss, low cost, low power, lightweight and compact form such as monolithic microwave integrated

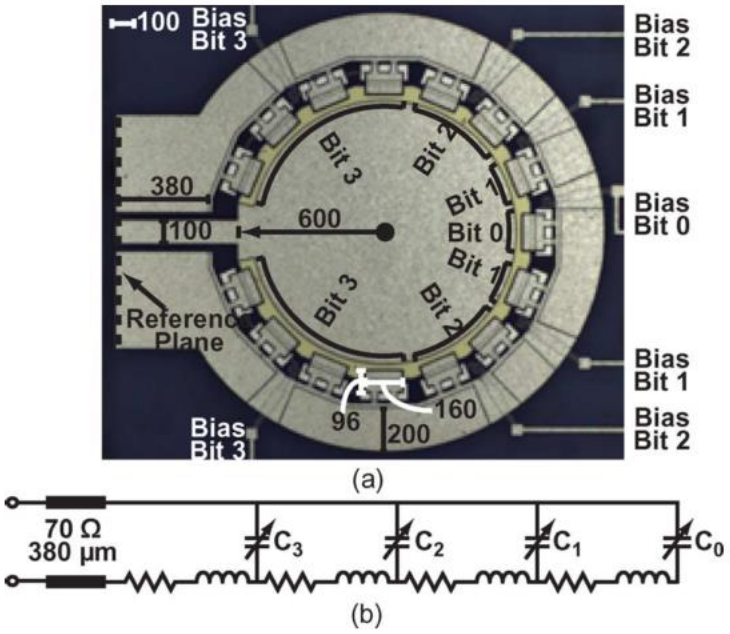


Figure 2.6: Digital MEMS varactors in circular configuration [32].

circuit (MMIC) are vital in the development of an efficient and compact phased array antenna systems.

Phase shifters can be generally classified into two main categories, analogue and digital. In an analogue phase shifter, the phase shift of the phase shifter can be varied continuously between two extreme phase shift values from 0^0 to 360^0. The figure of merit (FoM) for an analogue phase shifter is calculated based on the obtained phase shift divided by its insertion loss, ^{o}/dB. On the other hand, digital phase shifters provide a discrete set of phase shift states that are controlled by two-state phase bit. The number of phase states that can be achieved by digital phase shifters depends on the bits used in the design [33]. For example, a 2-bit phase shifter with $90^o/180^o$ phase delay networks is able to achieve 4 phase shift states which are $0^o/90^o/180^o/270^o$. The FoM for this type of phase shifter is phase shift per bit, ^{o}/bit. Even though analogue phase shifters are the ideal choice due to its infinite number of states, their implementation in MEMS phase shifters are very difficult to realise due to the instability effect which significantly reduces the tuning range of the phase shifters. This section will concentrate on four widely used phase shifter configurations which are reflection type, switched delay line, loaded-line, and distributed line designs.

2.3.1 Reflection-type Phase Shifter

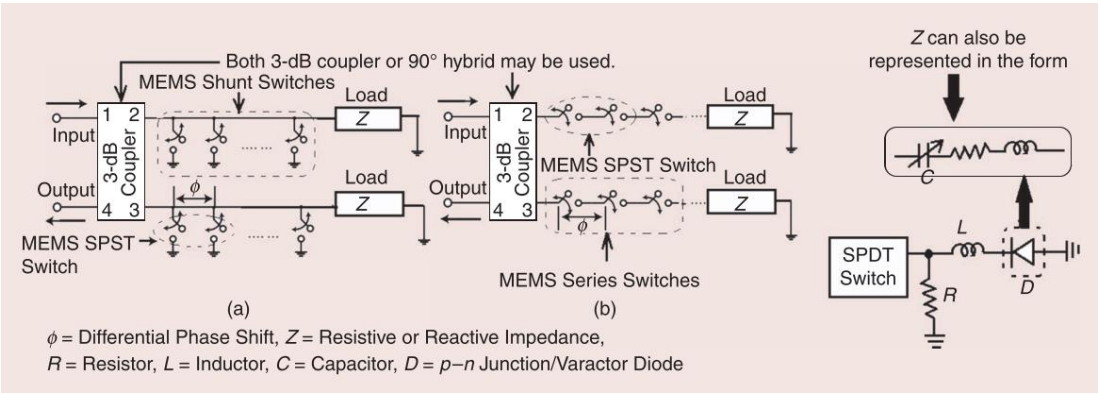


Figure 2.7: Reflection-type phase shifter [34].

Like other types of phase shifters, reflection phase shifters can be either analogue or digital. However, their digital implementation is carried out more often than the analogue type due to its simple design. Figure 2.7 shows a typical structure of

reflection-type phase shifters[34]. Two load impedances, Z_L are connected to the direct (port 2) and coupled (port 3) ports of a 3-dB hybrid coupler. The output can be obtained from the isolated port which is port 4. A differential phase shift is produced when any incident RF signal from port 1 is reflected by both impedances between port 1 and port 4 [33]. A large area occupied by reflection phase shifters is due to the implementation of the directional coupler in the phase shifters. In order to reduce the footprint of the phase shifters, several methods have been employed to modify the 90^0 coupler while maintaining its wideband performance [35], [36].

Furthermore, the reflective loads or impedances at port 2 and port 3 can be optimised using several techniques including using different types of transmission lines (CPW or microstrip) and RF MEMS switches (shunt or series). In addition, a wider phase shift can be attained by adding a series inductor in a π-network where the RF MEMS switches act as the shunt capacitors[33], [34]. A MEMS based reflection-type phase shifter was first developed by Raytheon Systems in 1999 [37]. Subsequently, the reflection phase shifter design was gradually improved in order to obtain a low loss performance and for size reduction [35], [38]. A low loss and compact single-bit reflection phase shifter has been reported in [39]. The phase shifter is based on L and π-type networks which is composed of one transmission line, and one or three identical varactors without any other lumped elements. The overall size of the chip is 0.25×0.4 mm^2 with FoM as high as 319°/dB and insertion loss of 1 dB at 2 GHz.

2.3.2 Switched-line Phase Shifter

A switched-line phase shifter is the simplest approach in designing a phase shifter. The basic operation of switched-line phase shifters involve switching between two transmission lines with different lengths in order to produce a phase shift as illustrated in Figure 2.8. Conventional switched-line phase shifters are mostly built with switching functionality which can be realised in several ways such as using resistive series switches (metal-metal) or capacitive shunt switches (metal-dielectric-metal). However, for high frequency application (> 40 GHz), capacitive shunt switches are normally used due to their lower actuation voltage, and faster switching speed

compared to series switches [1]. Moreover, this type of phase shifter requires a high isolation switch and a matched network.

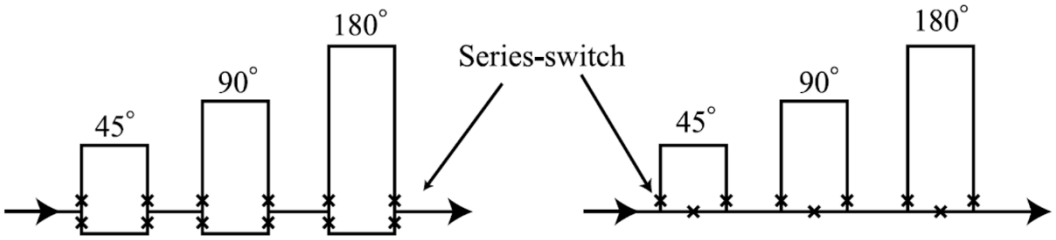


Figure 2.8: Switched line phase shifter [40].

A compact 5-bit switched-line digital MEMS phase shifter was designed and fabricated on a 200µm thick high resistivity silicon in [40]. It comprises 5 bits which are 11.25°, 22.5°, 45°, 90°, and 180° delay line sections. This design is based on a single-pole two-throw (SP2T) which consists of 3 ports, 2 ports for RF signal and one port for a bias voltage. There are twenty metal-to-metal direct contact series cantilever switches that are used for switching between on and off states. The switches are made of thick metal gold using an electroplating technique. The measured insertion loss is around 3.5 dB compared to the simulation result which is in the range of 1.15 dB to 1.3 dB. The measured phase shift error is less than 5^0 at 10 GHz.

The first attempt to use a flexible organic substrate in a phase shifter has been presented in [41]. A one- and two-bit MEMS phase shifters have been realised on a 100 µm Liquid Crystal Polymer (LCP) operated at 14 GHz. LCP substrate was chosen due to its low loss, low cost and near hermetic performance. However, the main challenge of using a flexible and organic substrate in a standard microfabrication process is the curling of the substrate due to the high temperature during the fabrication process. Besides that, the surface roughness of the polymer proves to be an issue which prevents the switches in the phase shifter from deflecting when actuated. It has been shown that the surface roughness can be reduced by polishing the substrate using the chemical-mechanical planarisation (CMP) technique with alumina slurry. The phase shifter produces 0^o, 45^o, 90^o, and 135^o phase shifts with a radial stub placed between the signal lines for bias voltages. The average return loss and insertion loss for the one-bit MEMS phase shifter is 19.0 dB and 0.59 dB respectively. As for the 2-bit design,

the average return loss and insertion loss are 22.5dB and 0.98 dB respectively. The phase error for both designs is less than 1.5°.

2.3.3 Loaded-line Phase Shifter

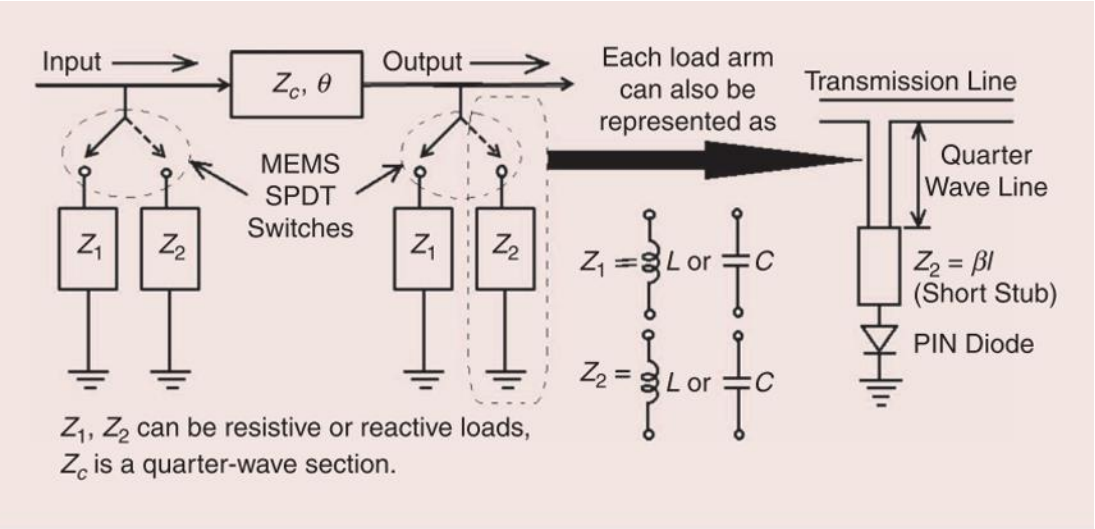


Figure 2.9: Loaded line phase shifter [28].

A loaded-line phase shifter is implemented by loading a transmission line with two different reactive impedance networks as illustrated in Figure 2.9. Typically, a central line segment is used to connect the two impedance networks where it also acts as a matching network to keep the input and output port impedances close to 50 Ω. A phase shift is then realised by controlling the values of the load impedances using MEMS switches.

A 2-bit loaded line phase shifter has been developed and presented in [42]. It consists of four series MEMS capacitive switches to change the load line impedances of the phase shifter. The characteristic impedance of the transmission line in the phase shifter is 50 Ω. Two separate phase shifters were designed to produce 22.5° and 45° phase shifts. Each branch consists of two microstrip transmission lines, MEMS switches and a stub series connection. The distance between the two branches is a quarter wavelength at the centre frequency of 9.25 GHz. The measured phase shifts are 15°, 30°, and 45° compared to the simulation results of 22.5°, 45°, and 67.5°. The

measured average insertion loss and return loss are better than 2.5 dB and 20 dB respectively.

2.3.4 Distributed-Line Phase Shifter

One of the main advantages of using distributed techniques in a phase shifter design is that a wideband performance can be achieved. The basic idea behind this method is to periodically load a transmission line in the phase shifters with transistors, Schottky diodes, or passive components such as capacitors. The design process of distributed-line phase shifters is usually simplified since the analytic model of distributed circuits is often accurate.

2.3.4.1 Diode based Distributed Transmission Line Phase Shifter

A distributed phase shifter implemented using Schottky diode varactors was reported in [43], [44]. The CPW transmission line in the phase shifter is periodically loaded with Schottky diodes as shown in Figure 2.10. The fabrication of the phase shifter was done on GaAs using monolithic fabrication processes. To reduce the loss of the phase

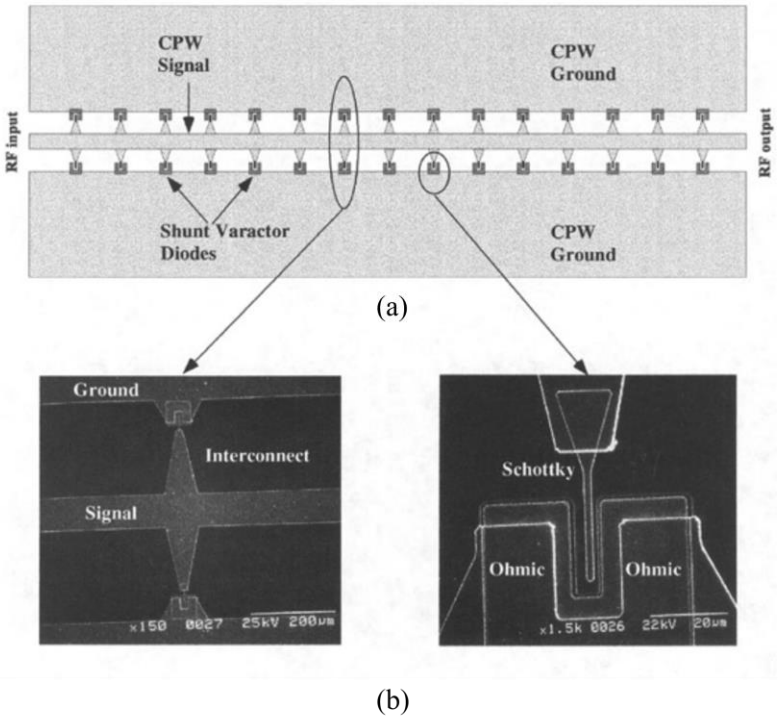


Figure 2.10: (a) Distributed phase-shifter circuit showing the symmetric arrangement of the shunt varactor diodes. (b) SEM images of the Schottky varactors diodes.

shifter, a 1.8 µm thick gold was used to pattern the CPW transmission line using the lift-off technique. The phase shifter is capable of providing continuous 0°-360° phase shift at 20 GHz. The maximum insertion loss of the phase shifter is 4.2 dB. However, these devices have limitation to perform at millimetre wave due to the series resistance of the diodes which is about 2 - 5 Ω, thus resulting in higher loss.

2.3.4.2 Distributed-line MEMS Transmission Line Phase Shifter

To reduce the loss of distributed-line phase shifters, RF MEMS switched capacitors or MEMS varactors can be utilised to replace the Schottky diodes in the previous phase shifter design. The series resistance of MEMS varactors is around 0.15 Ω which can result in excellent performance in mm waves frequencies with the FoMs of 90^0/dB and 72^0/dB at 60 GHz and 100 GHz respectively [45]. The MEMS varactors can be realised by using either cantilever or fixed-fixed bridge configurations. Basically, DMTL phase shifters can be realised by periodically loading a high impedance transmission line (> 50 Ω) using MEMS bridges. The increase of the distributed capacitance on the transmission line when the switches are actuated causes the transmission line impedance and phase velocity to decrease thus providing a differential phase shift between the input and output ports of the phase shifter. It has been reported in [5] that a true-time delay module such as distributed MEMS transmission line (DMTL) phase shifter is required to avoid a beam squint in the radiation pattern of a wideband phased array antenna used for radar applications. There have been many recent demonstrations of DMTL phase shifters using both coplanar waveguide (CPW) and microstrip transmission lines [46]–[48].

Generally, DMTL phase shifter can be realised analogously and digitally. For analogue implementation, a bias control voltage is applied between the centre conductor of CPW and the bridges to vary the height of bridge and thus capacitive loading of the line without completely pulling down the MEMS bridges[49]–[51]. However, the main drawback of analogue DMTL phase shifters is the mechanical instability effect experienced by the MEMS bridge which makes it difficult to achieve high phase shift for a single bridge [50]. In addition, the use of analogue bias voltage will produce electrical noise on the bias line which is then transferred into phase noise at the output of the device [45].

One of the solutions to mitigate this issue has been proposed in [45], [52]–[54] by using discrete capacitors (C_s) in series with the MEMS bridge to obtain a larger tuning ratio. As shown in equation (2.4), when the MEMS bridge is in the up-state position, the bridge capacitance is much smaller than C_s, hence the loading capacitance, C_l is dominated by the MEMS bridge. However, when the bias voltage is applied, the MEMS bridge is now in the down-state position where the bridge's capacitance is much greater than C_s resulting loading capacitance, C_l to be equal to C_s. Therefore, this operation can be viewed as digital implementation where the capacitance states are selected between two values.

$$C_l = \frac{C_s C_b}{C_s + C_b} \tag{2.4}$$

A metal-insulator-metal (MIM) capacitor has been utilised as a series capacitor in a DMTL phase shifter fabricated on quartz substrate in [54]. During the down-state position, the bridge capacitance has increased by a factor of 40 to 80 and becomes much larger than the MIM capacitance. This causes the loading capacitance to be dominated by the series capacitor. One of the challenges in this design is that the size of the MIM capacitor is quite small at 25 × 25 μm^2 making it difficult to be fabricated especially with a high Q for high-frequency operation. Moreover, MIM losses also dominate the insertion loss of the phase shifter. Figure 2.11 illustrates the cross section and circuit model of the DMTL phase shifter using the MIM capacitors.

In order to reduce the losses from the MIM capacitor, metal-air-metal (MAM) capacitor has been proposed in [53]. As a result, the DMTL phase shifter with the MAM capacitors obtains a lower insertion loss which is 1.2 dB instead of 4 dB obtained in the DMTL phase shifter with MIM capacitors in [54]. Moreover, higher

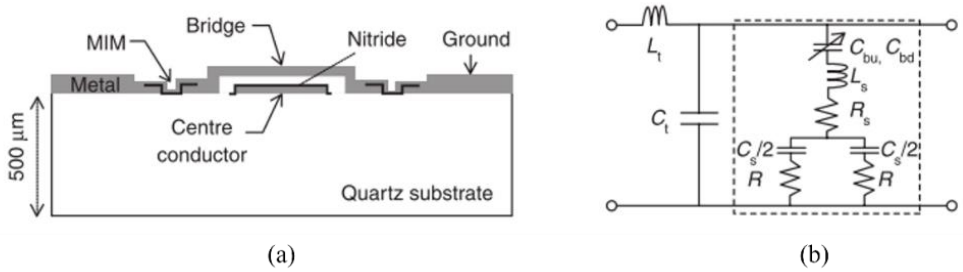


Figure 2.11: (a) Cross section and (b) circuit model of MEMS bridge and MIM capacitor.

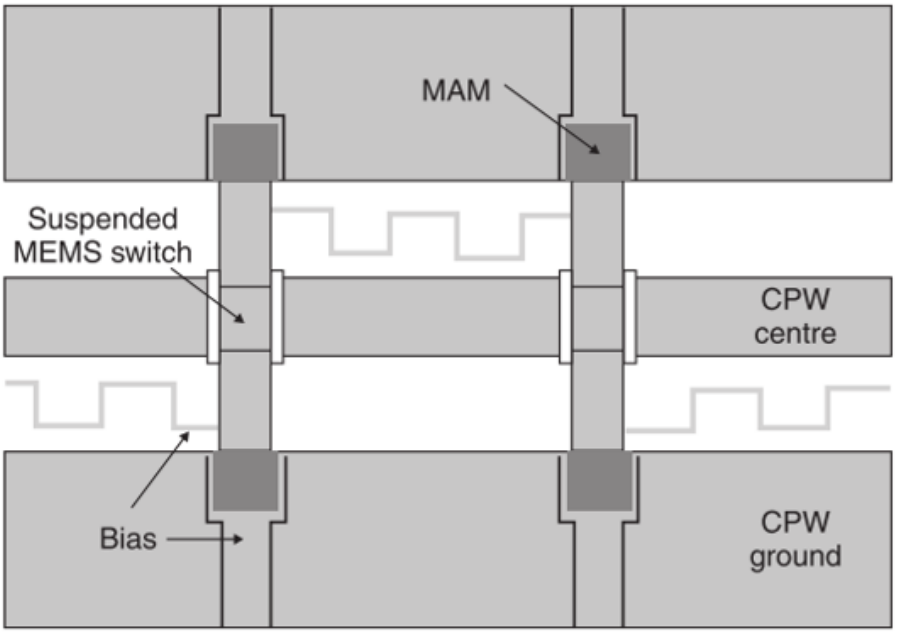


Figure 2.12: Diagram of two units of the DMTL phase shifter using MAM capacitors.

quality factor (Q=25) and larger capacitance ratio have been achieved. Besides that, another advantage of using MAM capacitor is its size is larger than the MIM capacitor which is 100 × 100 μm^2 which is it easier to fabricate. Figure 2.12 demonstrates the implementation of MAM capacitors in a DMTL phase shifter.

Table 2.1 shows the previous work of digital DMTL phase shifters that have been reported in the literature to date. However, all these designs were proposed to operate at higher frequency band ranging from X-band to Ku-band.

Table 2.1: Digital DMTL phase shifter designs in literature

Publication	Frequency (GHz)	Substrate	Insertion loss (dB)	FOM °/dB	Number of bit	Number of Bridge	Size (mm^2)
Borgioli et al[55]	25/35 GHz	Glass	1.7	154/160	1	11	8.58 mm long
Liu et al.[56]	26	Glass	1.7	105	3	14	11 mm long
J.S. Hayden and Rebeiz [54]	10	Quartz	0.9	180	2	16	22 µm long
J.S. Hayden and Rebeiz [45]	18	HRS	3	111	4	23	n/a

Joseph S Hayden and Rebeiz [57]	8-10	HRS	1.3	180	2	18	n/a
Kim et al. [58]	60	Quartz	2.2	122.7	2	24	6.3×1.5
Joseph S Hayden and Rebeiz [53]	14	Quartz	1.2	225	2	21	8.4×2.1
J.S. Hayden and Rebeiz [52]	37	Quartz	1.5	232.6	2	21	18
J. Hung, Dussopt, and Rebeiz [59]	78	Glass	2.7	96	3	28	4.3
J. Hung, Dussopt, and Rebeiz [60]	81	Glass	2.2	106	2	24	8
Topalli et al. [61]	15	Glass	1.5	120	3	28	30 cm
Du et al. [62]	10	HRS	1.5	80.35	5	31	51
Pillans et al. 2012[63]	30	Alumina	2.4	100	4	13	n/a
Pillans et al. 2012[63]	35	Alumina	2.7	94	4	13	n/a
Unlu, Demir, and Akin 2013[64]	15/30/40	Quartz	3.1/5/8.2	116/72/43	1		64
Chakraborty et al[17]	15	HRS	0.8	20	1	4	0.75 mm
Abdellatif et.al [65]	26	Alumina	0.75	26.67	1		0.75
Chakraborty et al [66]	15	HRS	2.1	85.7	1	10	0.88×0.88

2.3.5 Proposed DMTL Phase Shifter

The typical operating frequency of the existing distributed MEMS transmission line (DMTL) phase shifters ranges from 8 GHz to 110 GHz [17], [53], [55], [57], [59]. The measured insertion losses of the DMTL phase shifters are in the range of 1.2 dB for X-band and 1.5 dB for Ka-band operations. However, all of the proposed DMTL phase shifters in the literature operate at the frequencies above 8 GHz. This is driven by the fact that there are limited applications for DMTL phase shifters at L and S-band. Moreover, there are several challenges that need to be addressed for DMTL phase

shifters to function within this low microwave frequency range including the high loss due to a long transmission line and a large number of MEMS switches required.

Currently, several research groups all over the world are actively developing microwave imaging systems for biomedical applications [6], [7]. One of the techniques that can be used for biomedical imaging is by utilising radar-based microwave systems which require the use of ultra-wideband array antennas. The operating frequencies of most of these systems are within the 1 GHz to 4 GHz band [6], [7]. The beam steering capability and improved gain offered by phased array antennas can improve the detection accuracy of the imaging systems. Due to this requirement, DMTL phase shifters that can operate at S-band (2 GHz to 4 GHz) are proposed in this research. A digital DMTL phase shifter utilising a two-state varactor design by eliminating MIM capacitors in the phase shifter is proposed in this thesis to achieve a maximum phase shift of 270^{o} and 315^{o} for a 2-bit and 3-bit designs respectively. To the best of my knowledge, this is the maximum differential phase shift obtained by a DMTL phase shifter in the literature at 2.45 GHz. Moreover, a meandered transmission line is integrated in the design to optimise the size of the proposed phase shifters.

2.4 Summary

This chapter started with the overview of the tuneable RF MEMS varactors and phase shifters. As for the MEMS varactors, the discussion with regards to the design considerations to achieve high capacitance ratio and linearity for MEMS varactors has been highlighted. Additionally, the principle operations of different types of MEMS phase shifters have been discussed. The motivations of designing a MEMS varactor with high capacitance ratio and a DMTL phase shifter that can operate at low frequency range of 2 GHz to 4 GHz have been described. The following chapters focus on the design, simulation, fabrication and characterisation of the proposed MEMS varactors and DMTL phase shifters.

Chapter 3: Design and Simulation of High Tuning-Ratio MEMS Varactors

3.1 Introduction

MEMS varactors have the potential to replace the conventional diode-based varactors in many applications such as phase shifters, tuneable filters, impedance matching networks and oscillators due to their advantages including low loss and high linearity. While there are many configurations to realise MEMS varactors, the parallel plate configuration is the most favourable choice due to its simple design and it is also easy to fabricate. This chapter describes the design and simulation of novel high tuning-ratio MEMS varactors by implementing two methods which are the use of 20 µm deep trench in the silicon substrate and the deposition of 20 µm thick SU-8 layer as a separation layer between the varactor and the silicon substrate. Both methods have been proved to be able to reduce the effect of the fringing field capacitance due to the use of the silicon substrate hence improving the capacitance ratio of the varactor over a similar design implemented without the techniques.

This chapter is mainly divided into 5 main sections. Section 3.2 gives a brief explanation regarding the design of a high tuning-ratio MEMS varactor. The design and simulation of a 4-bit and 5-bit digital MEMS varactors are described in Section 3.3 and Section 3.4. Section 3.5 presents the simulation and analysis of the proposed truss bridge used in the varactors. The fabrication process for the 5-bit MEMS varactor is proposed in Section 3.6.

3.2 Design of a High Tuning-Ratio MEMS Varactor

Generally, there are two types of MEMS varactors: analogue and digital. Various analogue and digital MEMS designs have been demonstrated in the literature [25], [32], [67], [68]. One of the limitations that hampers the performances of analogue designs is their low tuning ratio which is important to obtain a wide tuneable characteristic as a result of the pull-in effect. This phenomena can be explained by the mechanical instability between the electrostatic force and restoring force of the varactor structure, which causes the metal bridge to snap down when it reaches one

third of the air gap [25], [68]. One way to achieve higher capacitance range is by employing digital type MEMS varactors or switched capacitor banks [69], [70]. Digital MEMS varactors are formed by several switches loaded on a transmission line where the capacitance values are selected by switching ON and OFF switches. The capacitance ratio of digital varactors can be calculated by finding the ratio of the maximum and minimum capacitance values obtained when all the switches are in ON states and OFF states respectively. However, the capacitance ratio of a digital design is still limited by the high up-state capacitance (C_{min}) value originating from the fringing field and parasitic capacitance between the silicon substrate and the varactor.

Digital MEMS varactors operate as a typical MEMS capacitive switch based on mechanical movement in lateral or vertical direction to achieve ON and OFF states [1]. Normally, they are made of an array of shunt switches suspended over the centre conductor of a co-planar waveguide (CPW). Both ends of the switches are fixed to ground to realise a digital varactor design. The bottom electrode under the bridge provides the electrostatic actuation of which the RF capacitance is created between the suspended bridge and the transmission line. The minimum capacitance is obtained when all the switches are in the up-state position; while the maximum value is achieved when all the bridges are pulled down. The minimum capacitance during the up-state condition, C_u can be calculated as [1]

$$C_u = \frac{\varepsilon_0 A}{g_o + \frac{t_d}{\varepsilon_r}} + C_f \tag{3.1}$$

where $\varepsilon_o = 8.854 \times 10^{-12}$ is the permittivity of free space, A is the contact area of the plates, g_0 is the initial gap, t_d is the dielectric thickness, and ε_r is the relative dielectric constant of the substrate. Typically, additional fringing field, C_f will contribute around 20% to 60% of the overall capacitance when the switch is in the up-state position [1][71]. On the other hand, the maximum capacitance of the varactor in the down-state position, C_d is given by [1]

$$C_d = \frac{\varepsilon_0 \varepsilon_r A}{t_d} \tag{3.2}$$

The overall capacitance ratio of a digital varactor is defined as [1]

$$C_r = \frac{C_{d\ (max)}}{C_{u(min)}} \tag{3.3}$$

There are three main mechanisms that limit the Q factor of a varactor which are the resistive loss of the conductor lines, the loss of the substrate and the loss of the inter-layer dielectric. Therefore, Q factor can be defined as [3]

$$\frac{1}{Q} = \frac{1}{Q_{metal}} + \frac{1}{Q_{substrate}} + \frac{1}{Q_{dielectric}} \tag{3.4}$$

1) Dielectric loss

The dielectric loss is the result of dissipations associated with damping of the vibrating dipole orientation. In general, dielectric constant is a complex number which is given by [3]

$$\varepsilon_r = \varepsilon_{r'} + j\varepsilon_{r''} \tag{3.5}$$

where $\varepsilon_{r'}$ is the real part that represents the relative permittivity and $\varepsilon_{r''}$ is the imaginary part which represents the energy loss in the dielectric medium. These losses usually can be defined using loss tangent formula (tan δ) which is equal to [3]

$$tan\ \delta = \frac{\varepsilon_{r''}}{\varepsilon_{r'}} \tag{3.6}$$

By using a dielectric with small loss tangent, such as aluminium oxide, parylene, or thermally grown silicon dioxide, the dielectric loss is small and can be neglected. However, it will produce a low capacitance value if the distance between the plates in the varactor is not increased [3].

2) Conductor Loss

The conductor loss in a CPW transmission line can be improved by increasing the thickness of the metal used in the design. At microwave frequency, the current density is maximum on the surface of the conductor and decreases exponentially as the

distance from the surface increases. Therefore, by using a thick conductor, the conductor loss can be minimised. The skin depth of a metal can be calculated as shown below.

$$\delta = \frac{1}{\alpha} = \sqrt{\frac{2}{\omega\mu\sigma}} = 503\sqrt{\frac{1}{\sigma}} \tag{3.7}$$

where σ is the conductivity of the conductor, angular frequency, ω is $2\pi f$ and μ is the permeability of the material given by $\mu = \mu_0 = 4\pi \times 10^{-7}$ $\left[{}^{H}/_{m}\right]$.

Typically, the thickness of a conductor should be at least twice of the skin depth value to minimise the conductor loss. It is to be noted that the skin depth decreases with increasing frequency.

3) Substrate loss

The substrate loss can be reduced by leaving the device suspended on an air cavity [70]. Another approach to minimise the loss is by reducing the loss tangent of the substrate through the implementation of a thick passivation layer, a partial removal of the substrate or the use low loss substrate such as glass [15]. However the use of low loss substrate might incur high cost which is not feasible for mass production.

3.3 Design and Simulation of a 4-bit Digital MEMS Varactor with a Deep Trench in the Substrate

Based on equation (3.1) to (3.3), a 4-bit digital MEMS varactor has been designed and simulated. The structure of the RF MEMS digital varactor and its parameters are illustrated in Figure 3.1 and Table 3.1 respectively. The varactor design consists of four capacitive shunt switches in a binary weighted configuration as shown in Figure 3.2. The bridge was designed based on a new truss structure to maintain its stiffness which would prevent the stiction effect while at the same time is able to reduce the required actuation voltage compared to the standard solid fixed-fixed bridge. Both the coplanar waveguide (CPW) transmission line and the bridges are made from 2 μm thick aluminium to improve the Q factor of the proposed varactors. A 0.25 μm of thin

silicon nitride (Si_3N_4) layer is deposited on top of the signal line as a dielectric layer. Additionally, a 26.35 μm deep trench is etched in the silicon substrate to minimise the fringing field effect between the bridges and the substrate in order to increase the capacitance ratio of the varactor as illustrated in Figure 3.3.

Table 3.1: Design parameter of a 4 bit digital MEMS varactor

Parameter	Value(μm)
Contact Area	Bit 1 (20x40) Bit2 (40x40) Bit3 (80x40) Bit4 (160x40)
Total contact Area	(300x40)
Trench depth (center conductor)	6.35
Deep trench depth	26.35
Length Bridge	550
Silicon Thickness	525
Aluminium Thickness	2

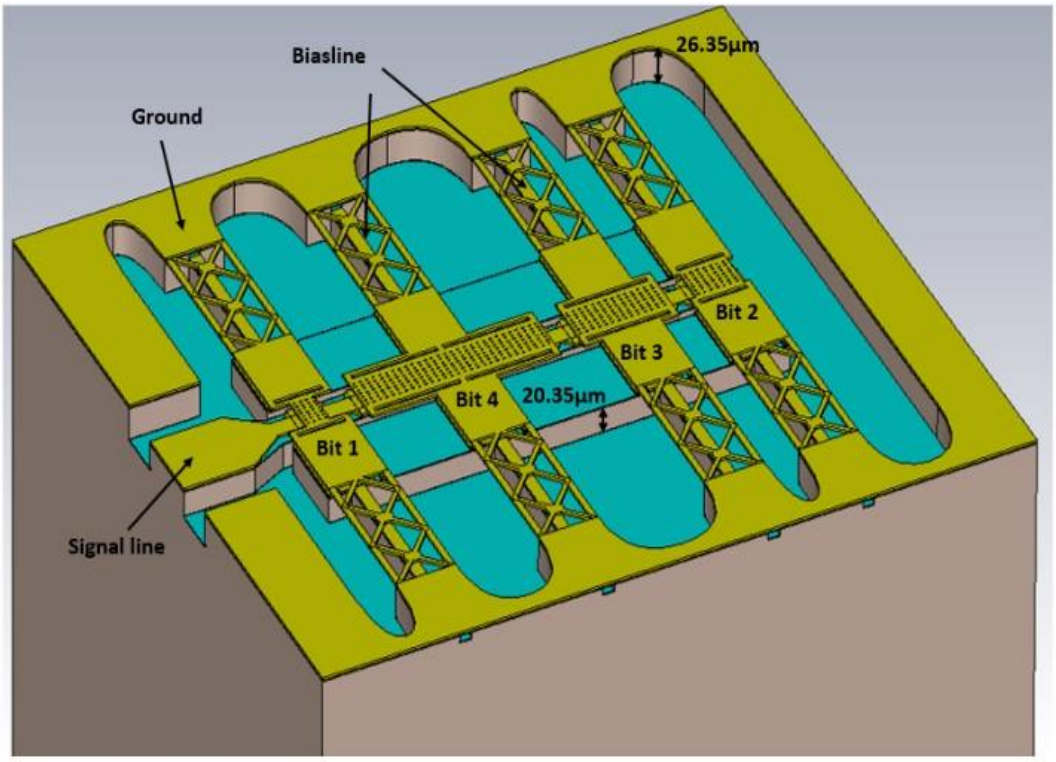


Figure 3.1: Digital MEMS varactor with a deep trench.

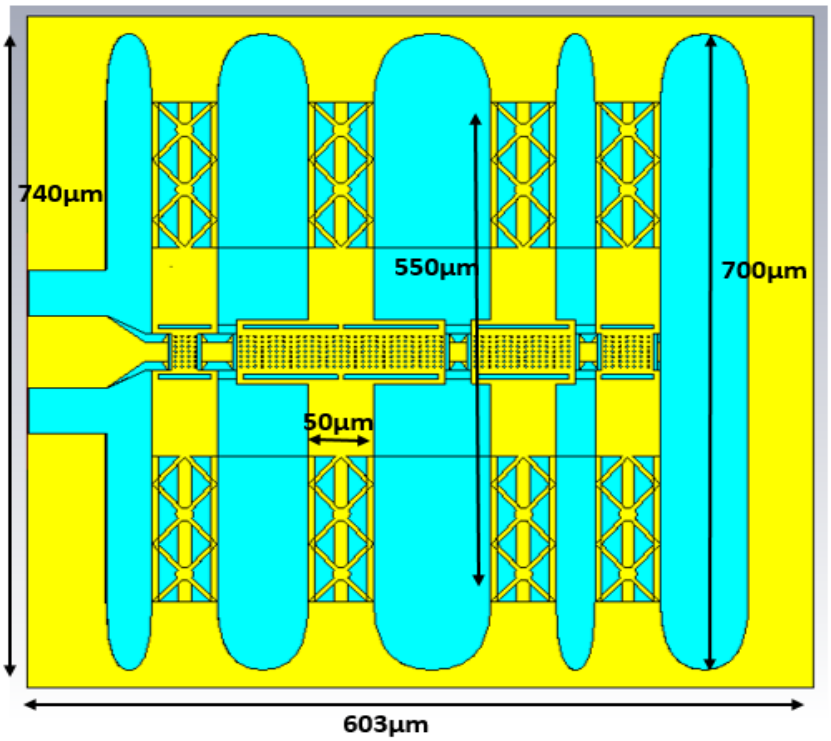


Figure 3.2: Top view of the 4-bit digital MEMS varactor.

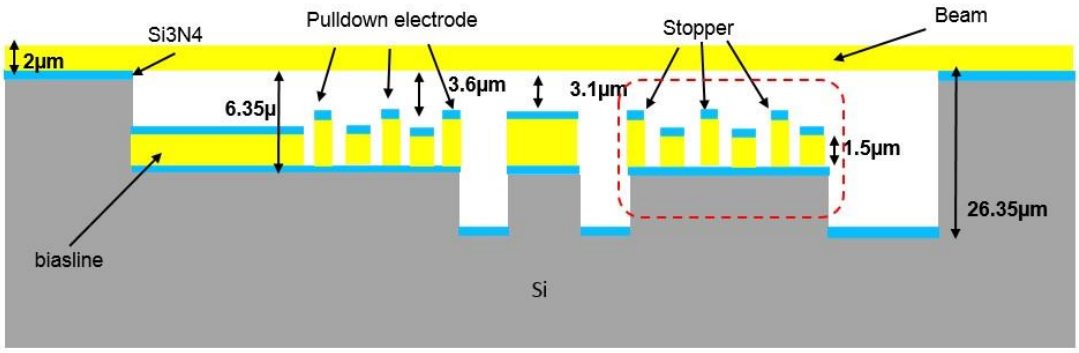


Figure 3.3: Cross sectional view of the design.

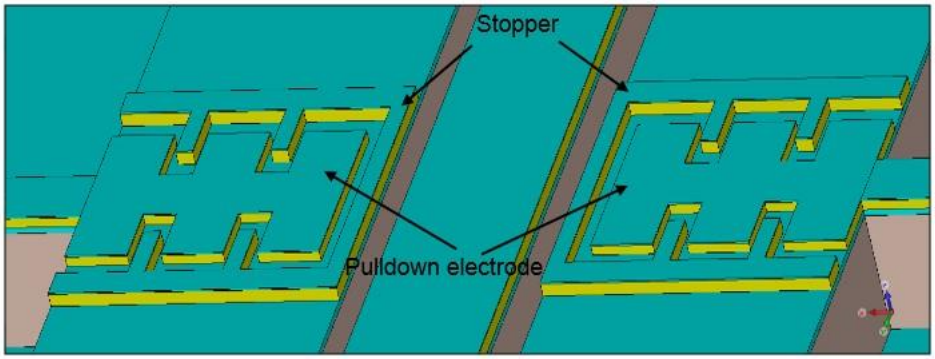


Figure 3.4: Side pull-down electrodes under the beam.

Besides that, the parasitic capacitance due to the CPW transmission line is reduced by varying the width of the RF signal transmission line between 20 µm to 40 µm and etching the ground in semi-circular shape between the bridge anchors as shown in Figure 3.1 to 3.3.

Furthermore, the effect of dielectric charging can be reduced by separating the RF line from the actuation electrode using a side pull-down pad configuration as shown in Figure 3.4. A 2.25 µm thick aluminium stopper design is proposed to prevent a direct contact between the bridges and the actuation pads. When a pull-in voltage is applied between the bridge and the actuation electrode, the electrostatic force which exceeds the mechanical restoring force is created, pulling the bridge down to the signal line where the bridge is now in the down-state position. In this condition, a maximum capacitance for each switch is produced and the total capacitance of the varactors in the down-state position, C_d can be calculated using equation (3.2) [1].

The RF characteristic of the varactor design has been analysed using a full wave simulator, CST Microwave Studio. In the software, the varactor model was built based on the dimensions given in Figure 3.1 and Table 3.1. A high resistivity silicon substrate with conductivity of 0.01 S/m (10 kΩ.cm) was used for improved RF performance in comparison with a low resistivity silicon wafer. The input port impedance of the varactors is designed to be 50 Ω to match most of the existing RF systems. There are 16 capacitance steps which are changing linearly from 95 fF to 3.4 pF with an incremental capacitance step of 0.2 pF at 2.45 GHz as demonstrated in Figure 3.5.

The minimum capacitance (when all the bridges are on the up-state position) and maximum capacitance (when all the bridges are on the down-state position) were obtained from the Smith chart plot as shown in Figure 3.6 and Figure 3.7 where the capacitance value can be extracted using the following formula:

$$C = \frac{1}{2\pi f_0 X} \tag{3.8}$$

where X is the imaginary part of the S_{11} plot of the varactor. Based on equation (3.3), the resulting capacitance tuning range is 35.7. The Q factor of the varactor can be extracted from the S_{11} plot using equation (3.9):

$$Q = \frac{|I_m[Z_{11}]|}{R_e[Z_{11}]} \tag{3.9}$$

The calculated Q factor for Cmin (state 1) and Cmax (state 16) are 540 and 78.4 which indicate low loss performance. For a comparison, the varactor design was simulated without the deep trench and the performances of both designs are compared in Table 3.2. An increase in the capacitance ratio to 35.7 is achieved through the implementation of the deep trench for the proposed digital varactor design compared to only 25 without the trench. It is to be noted that the high capacitance ratio characteristic is essential in implementing a wide tuning front end applications such as impedance matching networks, tuneable filters and phase shifters. As for the proposed truss bridge, its mechanical behaviour will be discussed in Section 3.5.1.

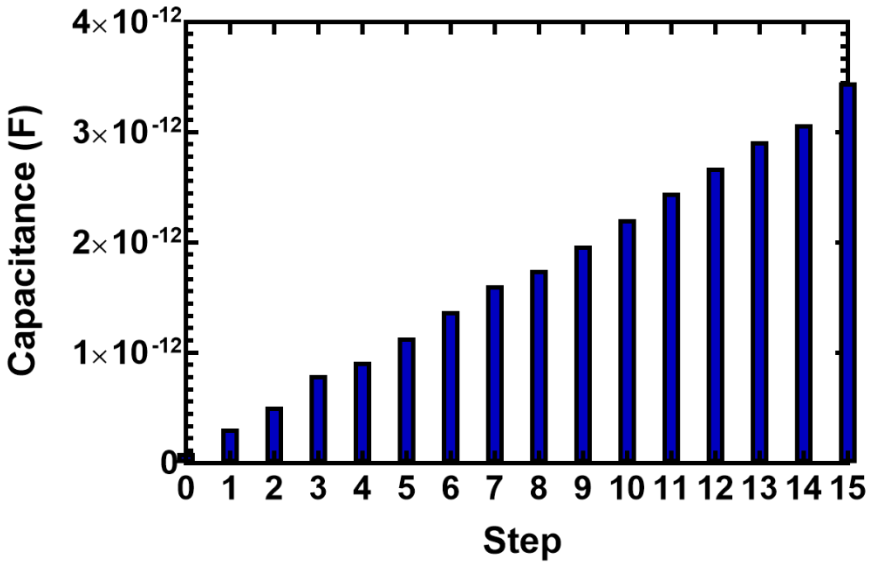


Figure 3.5: Capacitance state of the 4-bit digital MEMS varactor.

Table 3.2: Comparison of the minimum and maximum capacitance values of the varactor with and without the deep trench

Parameter	Without Deep Trench	With Deep Trench
Cmin (F)	133 fF	95 fF
Cmax (F)	3.4 pF	3.44 pF
Capacitance Ratio (Cr)	25	35.7

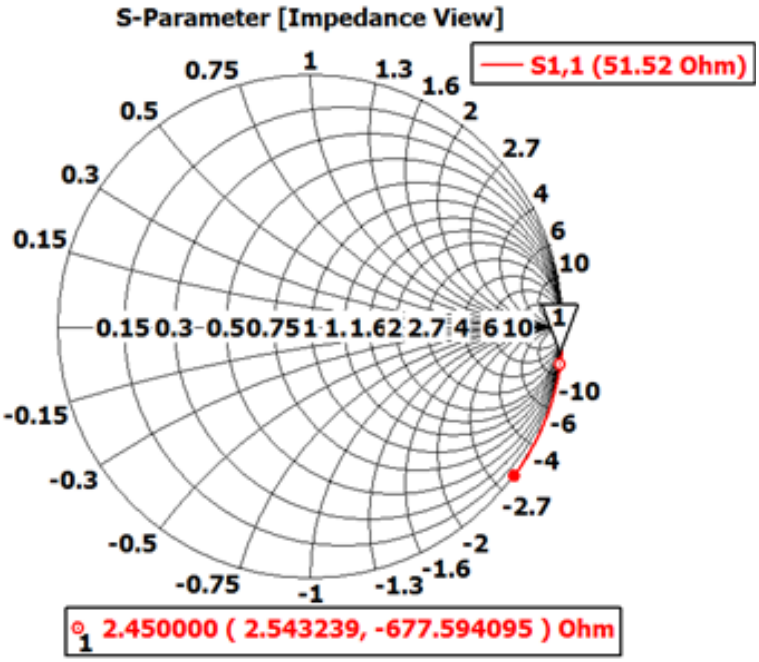


Figure 3.6: S-parameter for state 0 of the 4-bit digital MEMS varactor

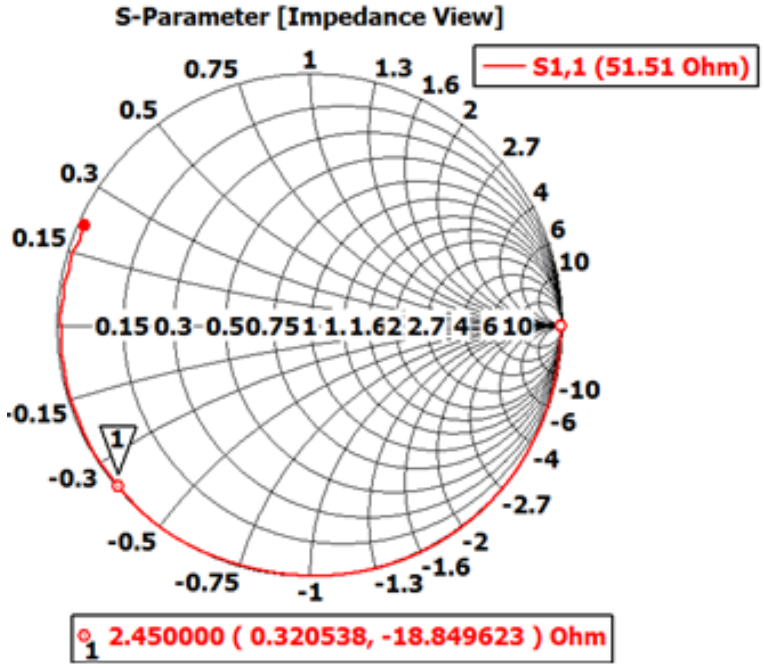


Figure 3.7: S-parameter for state 16 of the 4-bit digital MEMS varactor.

3.4 Design and Simulation of a 5-bit Digital MEMS varactor with the SU-8 Base Layer

In order to simplify the fabrication process of the varactor, a novel digital MEMS varactor design utilising SU-8 material has been proposed. In this design, SU-8 layer is used as a passivation layer to elevate the MEMS varactor to reduce the fringing field capacitance instead of implementing a deep trench in the silicon substrate as proposed in the previous design. Figure 3.8 presents the top view of the proposed digital variable capacitor. The design consists of 5-bit binary weighted capacitive shunt switches over a co-planar waveguide transmission line. The binary weighted capacitance value is realised by varying the contact areas between the centre conductor of the CPW line and the bridges.

The RF MEMS varactor was developed to achieve a high tuning range and Q factor by utilising SU-8 material. To facilitate this, the high fringing field capacitance due to the silicon substrate is reduced by elevating the varactor from the substrate by depositing a 25.35 μm thick SU-8 layer, thus greatly increasing the tuning range of the varactor. Apart from that, SU-8 is also used as the lateral support for the bridges of the varactor [16]. In addition, due to high resistivity characteristic of the SU-8 material, the use of low resistivity silicon for the realisation of the varactor is also possible which would reduce the cost of the proposed varactor design for mass production. For medium and high power applications, a very low pull-in voltage varactor design cannot be used due to the self-actuation effect. Therefore, a novel horizontal truss aluminium bridge with thickness of 2 μm is proposed as shown in Figure 3.10 (a). It is expected that the spring constant of the bridge would lie between the fixed-fixed flexure (k = 0.663 N/m) and the solid bridge structure (k = 5.3 N/m).

One of the major failures of RF MEMS varactors is the stiction problem due to dielectric charging effect and a very low spring constant bridge design. To increase the reliability of the varactor, a side pull-down configuration and a new stopper design are implemented. The design of the stopper is shown in Figure 3.10 (b). A gap of 0.5 μm exists between the actuator pad and the top bridge in the down-state position thus preventing direct contact between them. The introduction of semi-elliptical slot at the ground of the CPW transmission line further reduces the parasitic capacitance induced

in the varactor. The summary of the proposed design parameters are shown in Table 3.3.

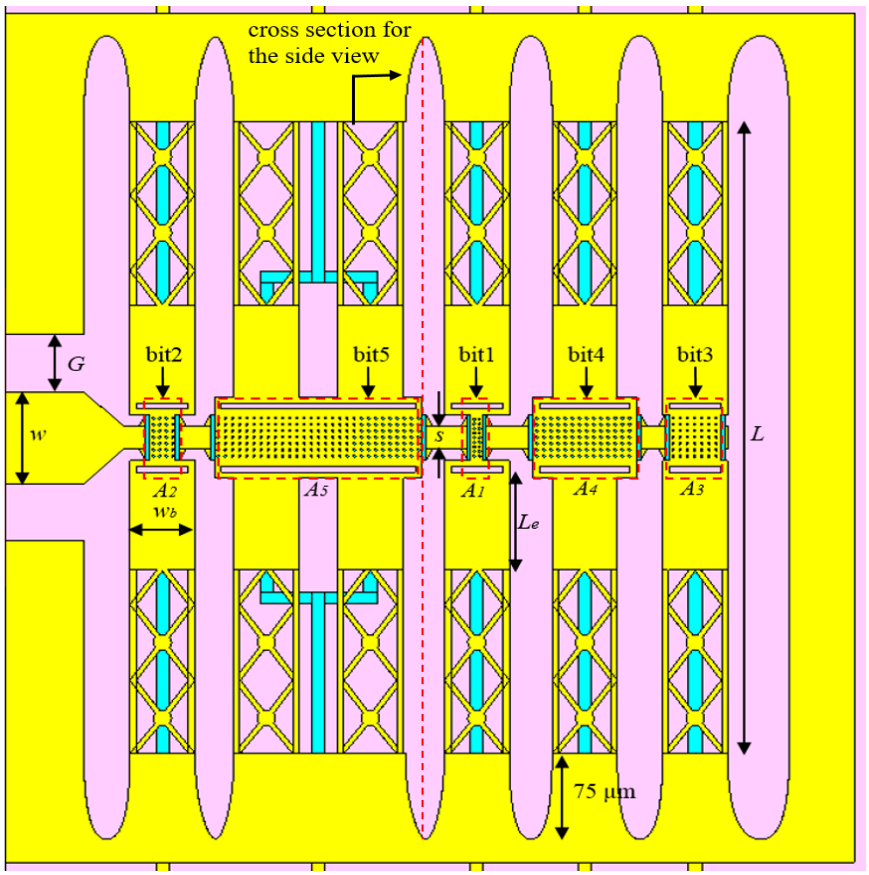


Figure 3.8: Top view of the 5-bit Digital MEMS varactor.

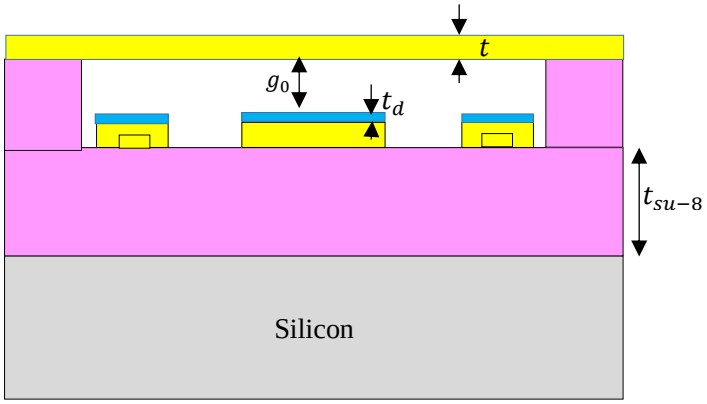


Figure 3.9: Side view the MEMS digital varactor on SU-8.

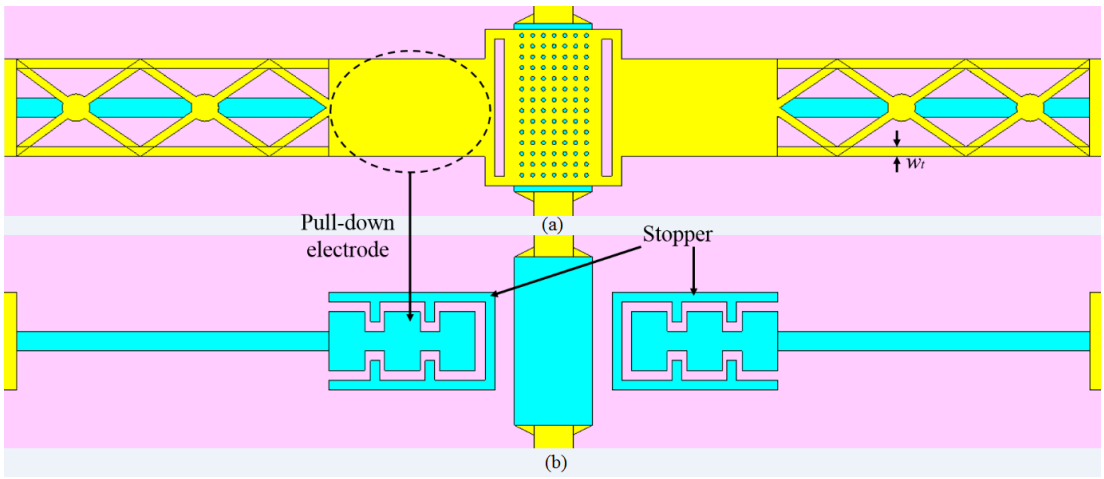


Figure 3.10: (a) Top view of the side pull-down and stopper with the bridge. (b) Side pull-down and stopper underneath the bridge.

Table 3.3: Design parameter of the 5-bit digital MEMS varactor

Symbol	Description	Value
L	Length of the bridge	550 µm
g_0	Air-gap	3.1 µm
t_d	Thickness of dielectric layer	0.25 µm
ε_{r1}	Relative permittivity of dielectric layer	7.5
t	Thickness of the bridge	2 µm
w_t	Width of the truss bridge structure	5 µm
t_s	Silicon substrate thickness	525 µm
ρ	Resistivity of silicon substrate	10k Ω·m
W	Width of the co-planar waveguide transmission line	80 µm
G	Gap of the co-planar waveguide transmission line	50 µm
A_1	Area of bit-1 of the varactor	10 µm × 40 µm
A_2	Area of bit-2 of the varactor	20 µm × 40µm
A_3	Area of bit-3 of the varactor	40 µm × 40 µm
A_4	Area of bit-4 of the varactor	80 µm × 40 µm
A_5	Area of bit-5 of the varactor	160 µm × 40 µm
t_{SU-8}	Thickness of SU-8 layer	{0, 5, 10,15, 20, 25, 30} µm
ε_{r2}	Relative permittivity of SU-8	4
$\tan\delta_{SU-8}$	Loss tangent of SU-8	0.04
A_{el}	Area of pull-down electrode	1.82×10^{-9} µm^2
E	Young's modulus of aluminium	69 GPa

V_p	Pull-down voltage	30.31 V
V_h	Holding voltage	25 V
k_T	Spring constant	1.33 N/m
$C_{d(\max)}$	Maximum capacitance value	3.57 pF
$C_{u(\min)}$	Minimum capacitance value	102.23 fF
C_r	Capacitance ratio	35.7

The proposed MEMS varactor design has been simulated using CST Microwave Studio to evaluate and analyse its RF characteristics. Optimisation of the SU-8 layer has been carried out by varying its thickness to achieve two main goals which are high capacitance ratio and improved Q factor.

A high resistivity silicon substrate, $\sigma = 0.01$ S/m ($\rho = 10$k Ω·cm) was used to improve the RF performance of the proposed varactor by reducing the substrate loss. Based on the Smith chart in Figure 3.11 and Figure 3.12, the capacitance values and the Q factor of the varactor can be extracted from the S_{11} plot using equation (3.8) and (3.9) [1].

The optimal thickness of the SU-8 layer has been achieved by comparing the capacitance ratio and the Q factor for 7 different thickness values which are 0 µm, 5 µm, 10 µm, 15 µm, 20 µm, 25 µm, and 30 µm. The simulated results of the respective thickness are tabulated in Table 3.4. It can be seen that by increasing the thickness of the SU-8 layer, the capacitance ratio of the varactor increases. However, the maximum capacitance ratio is obtained when the thickness of the SU-8 layer is 20 µm while by placing the varactor directly on the silicon substrate results in the lowest capacitance ratio. This is due to the reduction of fringing field capacitance between the varactor and the SU-8 because of its lower dielectric constant compared to silicon. Q factors of 812 and 50 were achieved for the $C_{u(\min)}$ and the $C_{d(\max)}$ respectively for the 20 µm thick SU-8 layer. This shows that good RF performance could also be realised by using SU-8 as the passivation layer in the varactor design.

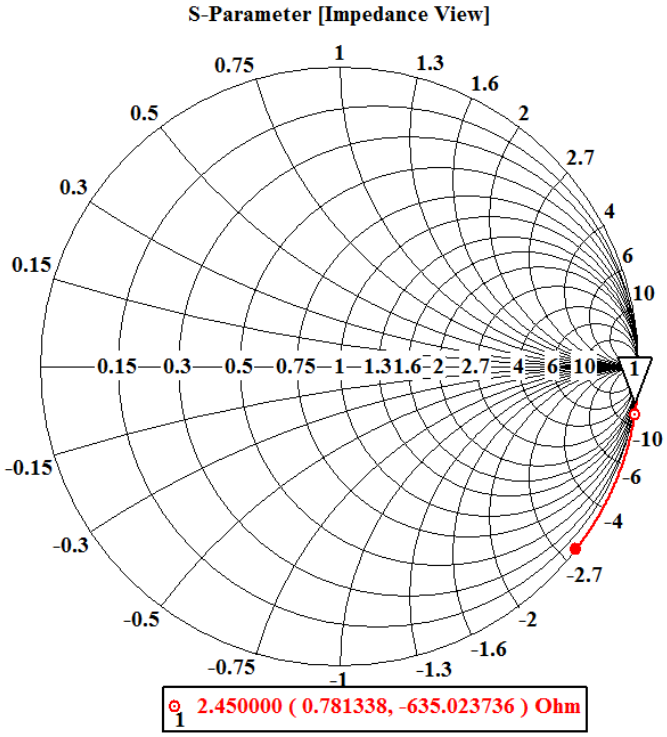


Figure 3.11: S-parameter for state 0 of the 5-bit digital MEMS varactor.

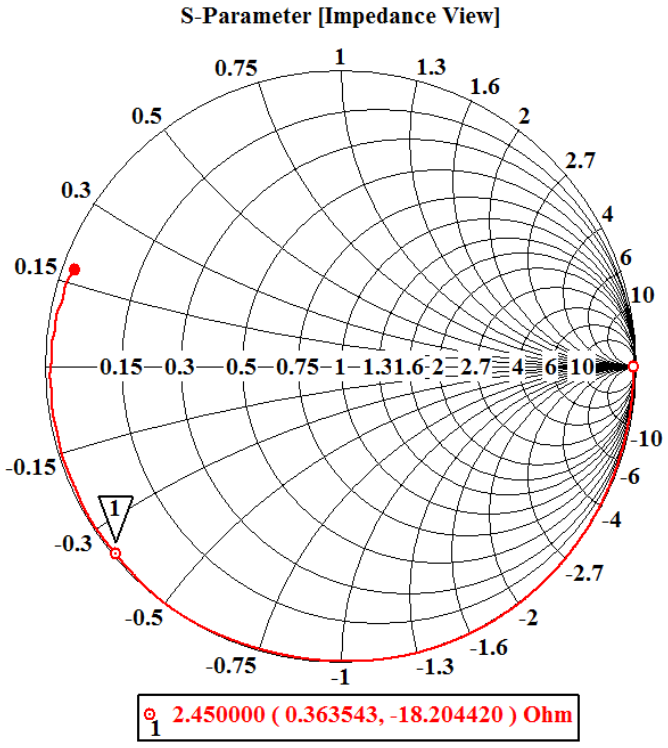


Figure 3.12: S-parameter for state 32 of the 5-bit digital MEMS varactor.

Table 3.4: Capacitance ratio and Q factor for different thickness of SU-8

Thickness (μm)	Capacitance ratio	Q factor (up-state/down-state)
0	16.9	248/95
5	24.5	505/114
10	28.9	613/108
15	34.4	762/93
20	34.8	812/50
25	34.6	648/66
30	33.5	827/62

The power handling capability of the varactor is calculated by simulating the pull-in voltage, V_p between the bridge and the centre conductor for the largest-bit switch since RF power is induced on the centre conductor of the varactor during its operation. The maximum RF power before self-actuation is calculated using equation (3.10) [1].

$$P = \frac{V_p^2}{Z_0} \tag{3.10}$$

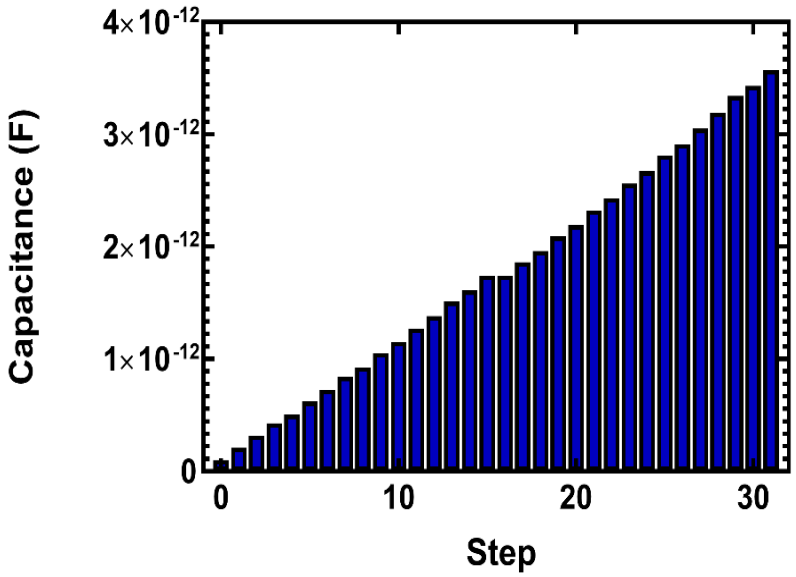


Figure 3.13: Capacitance steps for the 5-bit MEMS varactor.

where P is the incident RF power, Z_0 is the characteristic impedance of the line. In addition, the dielectric strength of SU-8 is 4.43 ± 0.16 MV cm^{-1} which is remarkably high for a polymer material. It is reported that a 15 μm thick SU-8 layer has a voltage

breakdown of around 7 kV and increases over the thickness [13]. The simulated pull-in voltage V_p from the centre conductor is 10.5V and the calculated maximum RF power that can be induced on the varactor is 2.2 W. There are 32 capacitance steps which change linearly from 102.23 fF to 3.57 pF with an incremental capacitance step of 0.11 pF as demonstrated in Figure 3.13.

3.5 Simulation and Analysis of Mechanical Behaviour of the Bridge used in the MEMS Varactors

3.5.1 Truss Bridge

In order to estimate the actuation voltage of the proposed truss bridge with a side pull-down electrode, the spring constant of a fixed-fixed bridge with the same actuation method can be used where the spring constant of the fixed-fixed bridge is given by [72]

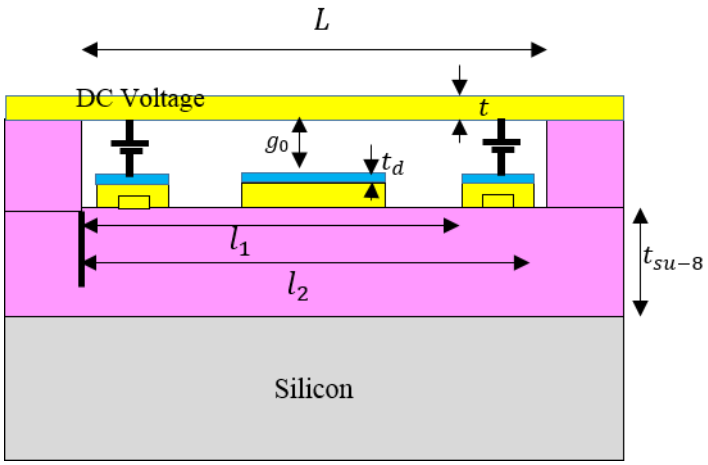


Figure 3.14: Side pull-down configuration.

$$k = \frac{-4t^3wE(l_2 - l_1)}{L^3(l_2 - l_1) - 3L^2(l_2^2 - l_1^2) + 3L(l_2^3 - l_1^3) - (l_2^4 - l_1^4)} + \frac{2tw(1-v)\sigma(l_2 - l_1)}{L(l_2 - l_1) - \frac{1}{2}(l_2^2 - l_1^2)} \ [N/m] \quad (3.11)$$

for $l_2 - l_1 \leq L/2$, where L is the length of the bridge, w is the width of the bridge, t is the thickness of the bridge, σ is the residual stress, E is the Young's modulus of the bridge and v is the Poisson's ratio of the metal used for the bridge. For the fixed-fixed bridge with the same length and width to that of the truss bridge structure, the spring constant of the bridge calculated using equation (3.11) is 58.12 V. For the truss bridge, it is expected that the pull-in voltage will be less than the solid bridge due to the truss structure at both ends of the bridge that causes reduction in the Young's modulus of the bridge [1].

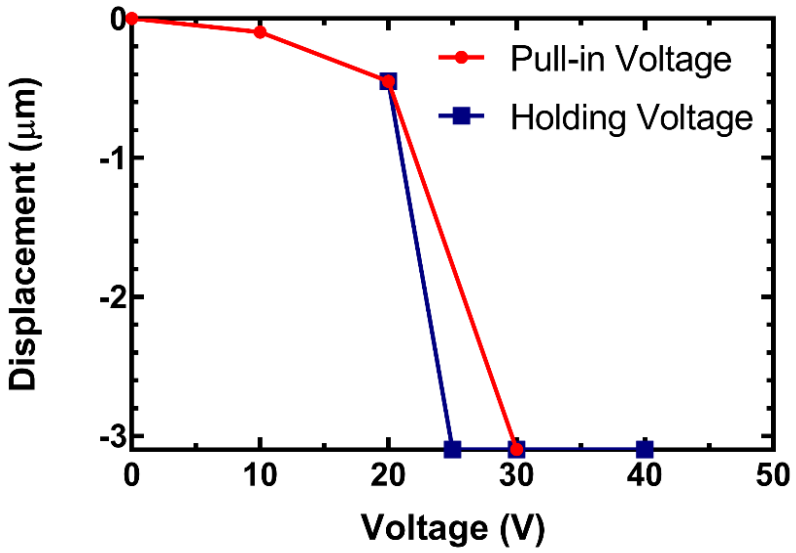


Figure 3.15: Pull-in voltage and holding voltage of the truss bridge.

The structure of the truss bridge as shown in Figure 3.8 was analysed in CoventorWare to calculate the pull-in and holding voltage of the proposed bridge. Moreover, in order to obtain a similar pull-in voltage across all bridges in the varactor, the bridge width is fixed at 50 µm. All the 5 bridges were individually simulated to calculate their pull-in voltage. The side pull-down pads were implemented to separate

the DC voltage and RF signal to reduce the dielectric charging effect. In the simulation, an incremental positive bias voltage was applied at the pull-down pads while the DC potential of the bridge is kept at 0 V. The simulated pull-in voltages of all the bridges are within the range of 28 V to 32 V. The slight discrepancy in the simulated actuation voltage is mainly due to different sizes of the centre structure of the bridges. On the other hand, the lift-off or holding voltage analysis was conducted by decreasing the voltage from the calculated pull-in voltage value until the bridge was released to its initial up-state position. Figure 3.15 demonstrates that the pull-in voltage for the 80 µm centre width bridge is 30 V while its holding voltage is 25 V. The bridge deformation during it down-state position is shown in Figure 3.16 where the red colour in the centre of the bridge determines the maximum displacement of the bridge. The obtained displacement value of 1.8 µm is more than one third of the initial gap height of the bridge indicating that mechanical instability had occurred and the bridge was pulled down. To verify the reduction of the Young's modulus of the truss bridge compared to the solid bridge, the simulated pull-in voltages of the bridges were compared. The simulated pull-in voltages of the truss and solid bridges with 550 µm in length and 50 µm in width are 30.31 V and 58.12 V respectively. It is seen that there is 47.85% reduction in the pull-in voltage for the truss bridge which can be associated with the reduction of the Young's modulus of the truss bridge compared to the solid bridge. Therefore, equation (3.11) can be used to estimate the pull-in voltage of the proposed truss bridge where the Young's modulus of the truss bridge should be reduced to one third of the solid bridge value to account for lesser mass in the truss bridge.

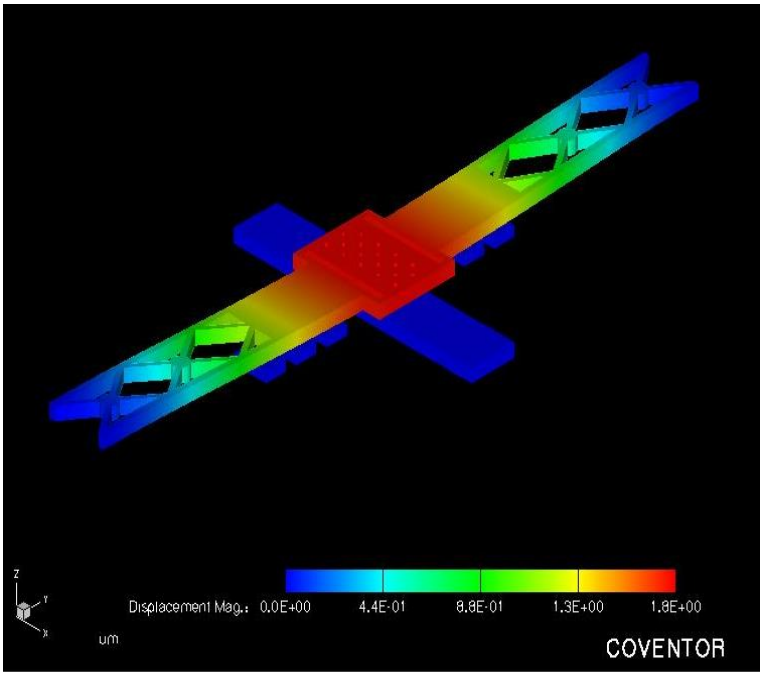


Figure 3.16: Bridge displacement when the pull-in voltage applied.

Subsequently, to investigate the effects of in-plane residual stress and stress gradient on the bridge, different values for both stresses were simulated. Generally, the biaxial residual stress introduced on the MEMS structure is due to the fabrication process of the MEMS device which typically involves high-temperature processes. In this work, in-plane residual stresses of 0 MPa, 50 MPa and 100 MPa were chosen to analyse its effect on the spring constant of the proposed bridge [73], [74].

As a comparison, a solid fixed-fixed bridge of similar configuration (length = 550 µm, width = 50 µm and t =2 µm) was also analysed. The sensitivity analysis due to the residual stress for both bridges was carried out. In addition, vertical stress gradients of 0 to ±8 MPa/µm were induced on the bridge structure to analyse its initial displacement. Further analysis will be discussed in Section 3.5.2 and Section 3.5.3.

3.5.1.1 Modal Analysis

Modal analysis of the bridge varactor was carried out to compute the mechanical natural frequencies of the structure at equilibrium. The calculated frequencies and their associated mode shapes are shown in Figure 3.17 (a), (b) and (c). The finding of these frequencies helps to understand how the bridge would respond to the surrounding noise. The resonance frequencies of the 80 µm bridge is at 53.9 kHz, 110.5 kHz and

142.8 kHz. These resonances occur without any external force applied to the bridge structure. In addition, the switching speed of the bridge can be estimated by one-quarter period of the mechanical primary natural frequency of the bridge [29]. This results in the theoretical switching speed of 4.64 µs.

3.5.1.2 In-plane Stress (Solid Bridge and Truss Bridge)

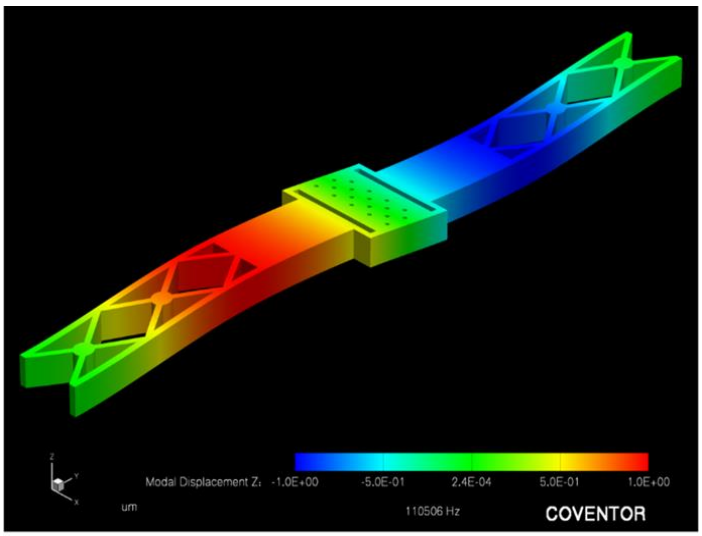
The total spring constant, k_T of a mechanical bridge is given by the summation of the spring constant due to mechanical properties of the bridge, k_1 and the stress-induced spring constant after fabrication process, k_2. The total spring constant is then calculated as

$$k_T = k_1 + k_2 \tag{3.12}$$

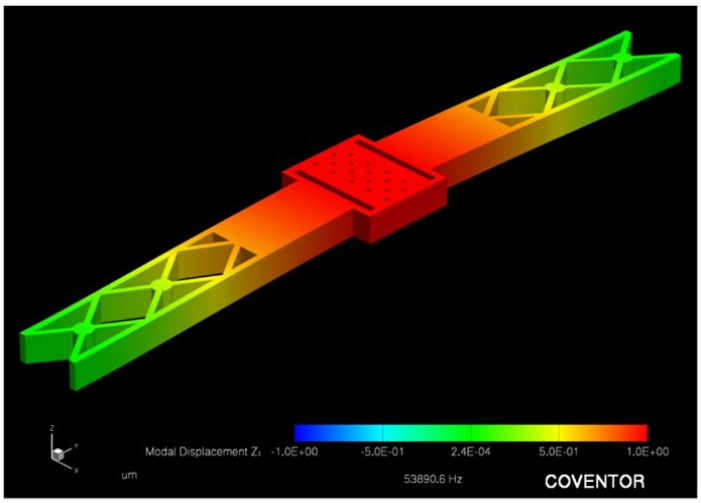
The spring constant of the bridge is calculated by first finding its pull-in voltage using the simulation tool and subsequently using the following equation [1]

$$V_p = \sqrt{\frac{8k_T g_0^3}{27\varepsilon_0 A_e}} \tag{3.13}$$

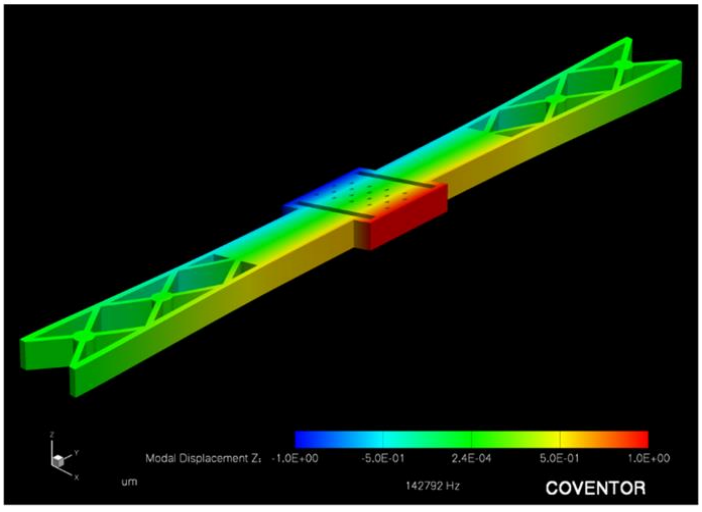
The total spring constant of the bridge without residual stress is 1.33 N/m while for the solid bridge design is 4.88 N/m. The corresponding pull-in voltages are 30.31 V and 58.12 V respectively. This shows that the proposed truss bridge can reduce the actuation voltage by almost 50% compared to the standard solid bridge design. The advantage of the truss bridge over conventional solid bridge design could be further



(a)



(b)



(c)

Figure 3.17: Resonant frequency at (a)1st harmonic 53.9 kHz, (b) 2nd harmonic 110.5 kHz and (c) 3rd harmonic 142.8 kHz.

emphasised by comparing its sensitivity to the in-plane residual stress. Both designs

were simulated with in-plane residual stresses of 0 MPa, 50 MPa and 100 MPa. The simulated spring constants against residual stress are shown in Figure 3.18. It can be seen that the spring constant of the truss bridge increases by only 3 N/m for a residual stress of 50 MPa which results in a maximum k_2/k_1 ratio of 2.6 as shown in Figure 3.19. As a comparison, the solid bridge structure results in a k_2/k_1 ratio of 5 demonstrating its higher sensitivity to in-plane residual stress.

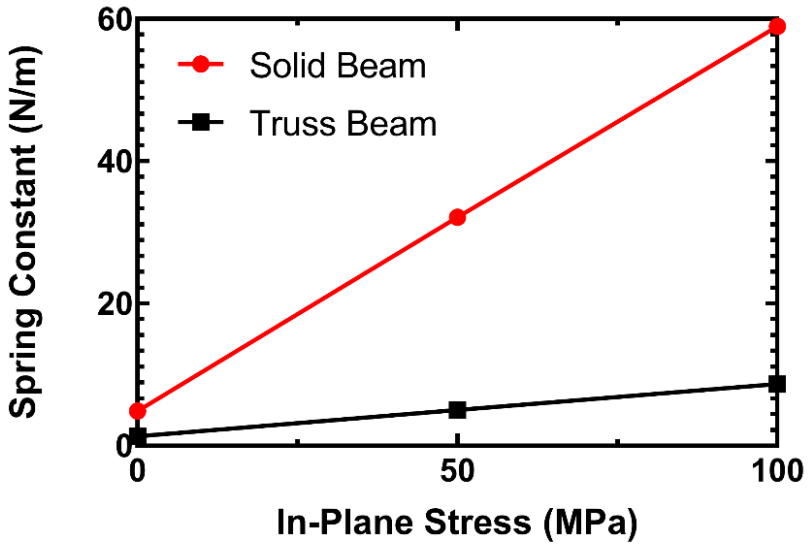


Figure 3.18: Spring constant vs in plane stress.

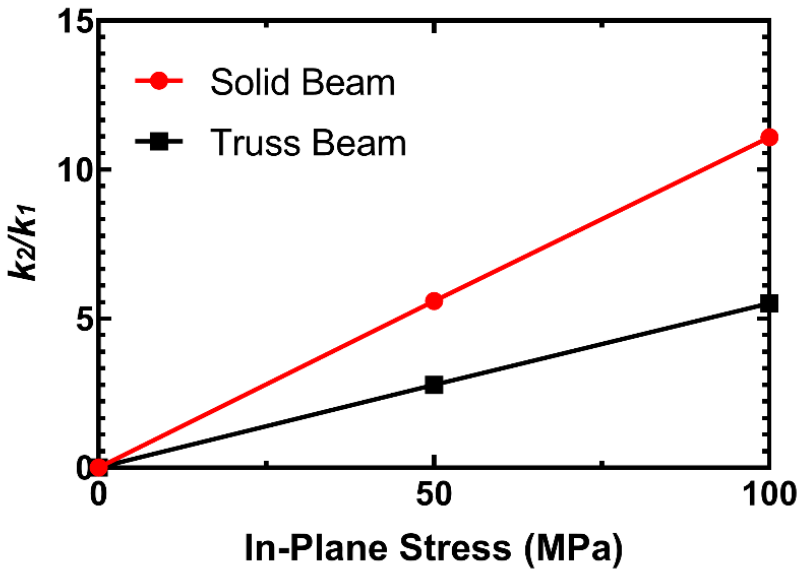


Figure 3.19: k_2/k_1 ratio versus in-plane stress.

3.5.1.3 Stress Gradients

The bridge structure was also simulated versus varying vertical stress gradients. The deformation of the centre plate along the bridge length direction due to vertical stress gradients of 0 to +/− 8 MPa/µm are shown in Figure 3.20. The simulation results show that positive stress gradients cause the bridge to deflect downward while negative stress gradients deflect the bridge in the opposite direction. Stress gradients of +/− 8 MPa/µm will result in maximum centre displacement of 0.3 µm which is still within the acceptable range of a typical MEMS varactor [73].

Further simulation on the von Mises stress was undertaken in order to investigate the stress induced on the bridge during actuation. This analysis is important to ensure that the bridge structure can withstand the maximum applied force during its operation. Figure 3.21 shows that the maximum von Mises stress is located at the end of the bridge. These values are lower than the yield strength of aluminium which is 124 MPa and therefore gives a clear indication that the bridge will not break when actuated.

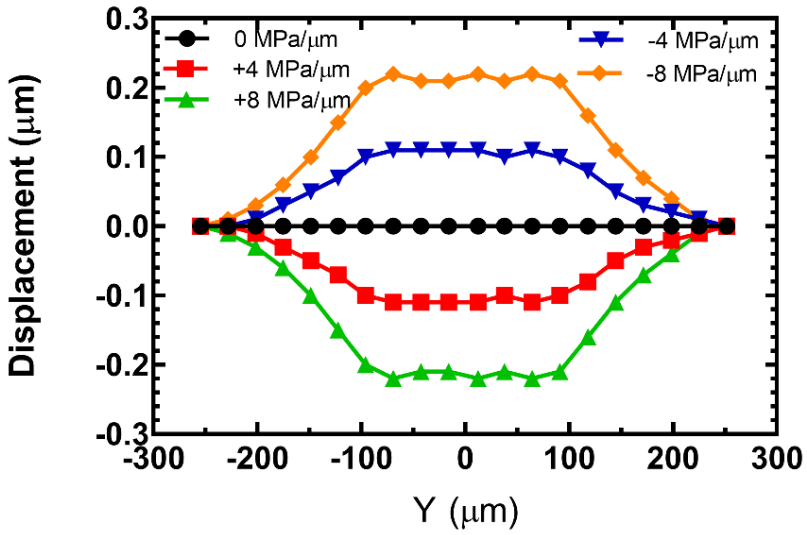


Figure 3.20: Vertical displacement of the bridge for various stress gradient values.

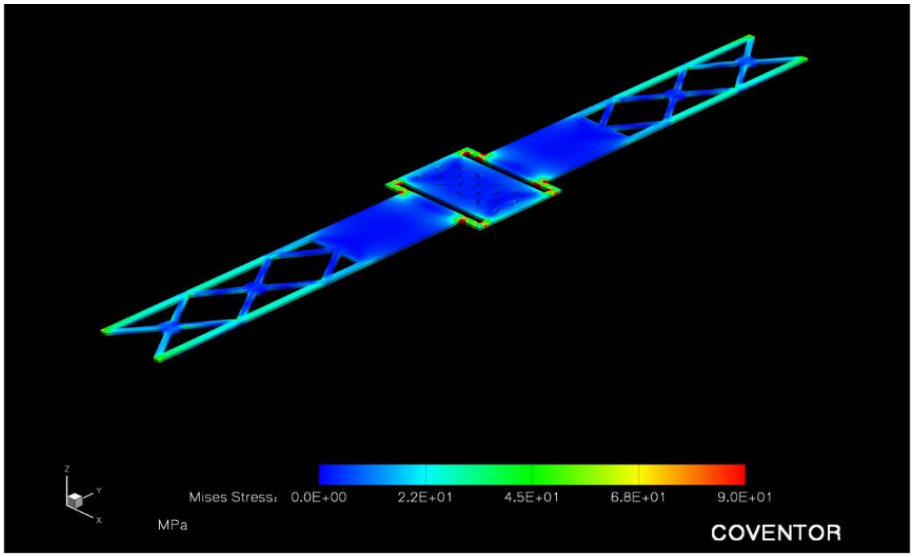


Figure 3.21: Von Misses stress for the truss bridge.

3.6 Proposed Fabrication Process for the 5-bit Digital MEMS Varactor using SU-8

Below are the overview of the proposed fabrication process for the 5-bit digital MEMS varactors design using SU-8. The fabrication process of the MEMS varactor composes of several steps described using the diagram shown in Figure 3.22. A 525 μm thick

high resistivity silicon wafer is chosen as the substrate. A total of five masks are required for the fabrication process. First, 20 µm of SU-8 is spin-coated on the surface of the silicon wafer. Then, the SU-8 is soft baked to evaporate the solvent before it can be exposed under the UV light. Next, post exposure bake (PEB) is performed. To further cross-link and cure the SU-8 layer, hard bake is needed at temperature 210 ^{o}C for 1 hour. As a precaution, the SU-8 cannot be baked at a very high temperature (exceeding 300 ^{o}C) to avoid cracks in the film. On the other hand, the baking temperature must be more than the subsequence process temperature to avoid destroying the SU-8 layer. Therefore, the subsequence processes must not be carried out above 200 ^{o}C. After curing the SU-8, 2 µm thick aluminium is sputtered and patterned using dry etching process to form the CPW transmission lines and stopper. In the next step, 1.5 µm aluminium is deposited and patterned using lift-off process to define the side pull-down electrode. Then, thin tantalum nitride (TaN) is patterned by lift-off process to form the bias lines after its deposition. By using plasma enhanced chemical vapour deposition (PECVD) technique, 2500Å Si3N4 is patterned on top of the centre conductor, stopper, and pull-down electrode as dielectric layer. In this process, 150 ^{o}C instead of 300 ^{o}C for plated shower is used to make sure it will not affect the SU-8 layer. Next, around 7 µm thick polymer or any sacrificial layer such as SU-8 or polyimide is spin coated and cured up to 200 ^{o}C to form the anchor and sacrificial layer [16]. Additionally, adhesion between the sacrificial layer material and SU-8 must be properly observed since it has been found that the standard release process using silicon dioxide as the sacrificial layer is not suitable for this work due to its poor adhesion to SU-8. Then, chemical mechanical planarisation (CMP) technique is then used to level the SU-8 to obtain a 5.35 µm thick SU-8 layer for the realisation of the anchor and sacrificial layer. Then, 2µm aluminium is deposited and patterned to form the bridge and ground. Finally, the sacrificial layer will be removed using oxygen plasma to release the bridge.

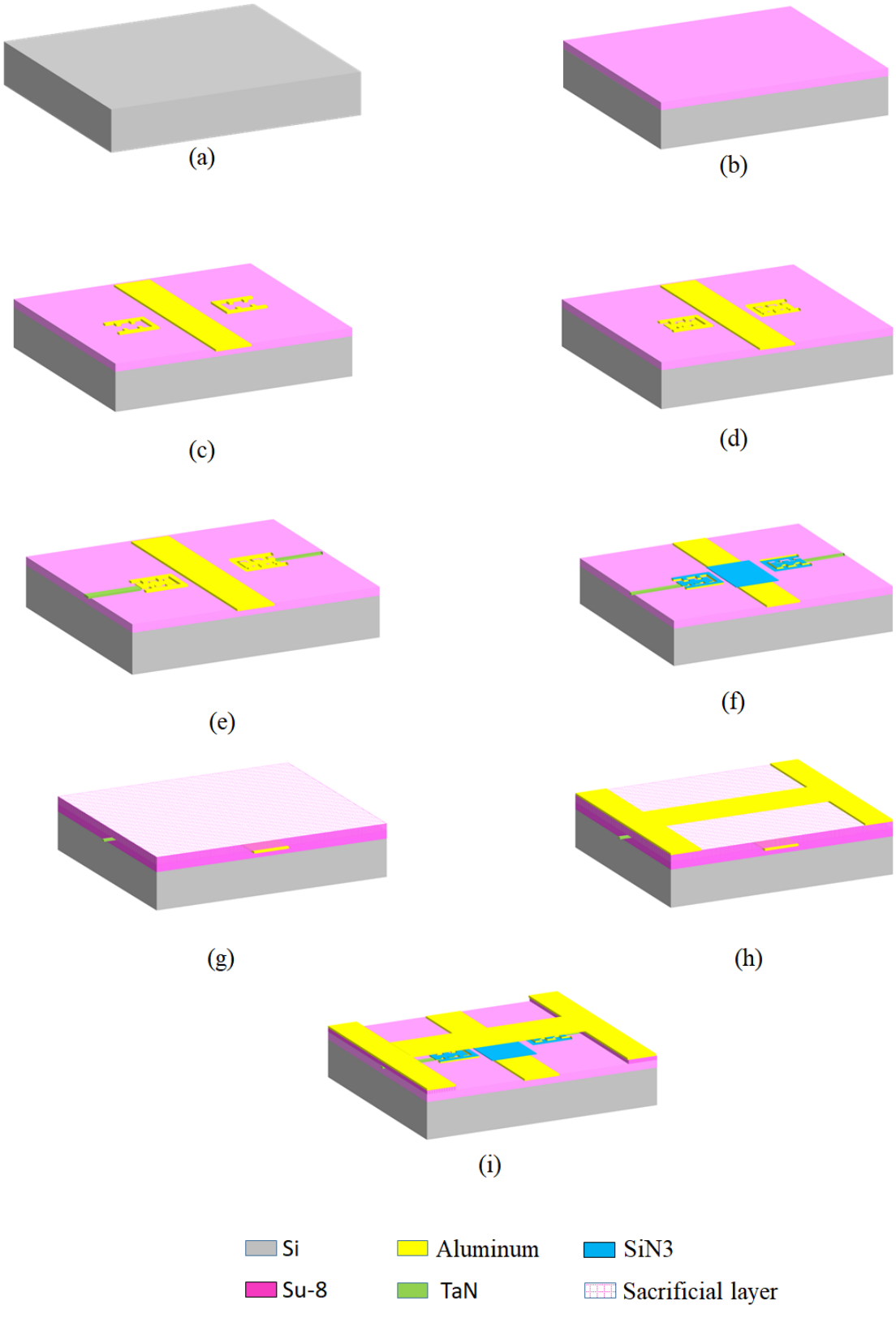


Figure 3.22: Proposed fabrication process for the MEMS digital varactor using SU-8. (a) Fresh silicon wafer (b) Spin coat of thick SU-8 (c) Deposit and pattern aluminium for centre conductor

and stopper. (d) Deposit and pattern aluminium for stopper. (e) Deposit and pattern tantalum nitride (TaN) for bias line. (f) Deposit and pattern silicon nitride (Si3N4) as a dielectric. (g) Deposit SU-8 as an anchor and sacrificial layer. (h) Deposit and pattern aluminium for the bridge and ground. (i) Release the MEMS bridge.

3.7 Summary

The design and simulation of a 4-bit and 5-bit digital MEMS varactors using a deep trench and SU-8 polymer are presented in this chapter. In order to increase the tuning ratio of the MEMS varactors, a deep trench and thick SU-8 separation layer methods are employed in the MEMS devices to reduce the parasitic and fringing field capacitance from the silicon substrate. Based on the simulation results, a high tuning ratio up to 35.7 and 34.8 could be achieved for the 4-bit and 5-bit designs using the proposed techniques. The total number of capacitance values that can be selected from the varactors are 16 to 32 for the 4-bit and 5-bit varactors respectively. Moreover, a new truss bridge structure is implemented in the bridge design to bring down the pull-in voltage of the bridges so that the varactors can be actuated at a voltage lower than 40 V which is the typical pull-in voltage value for the existing MEMS switches in the literature [75]. The simulated pull-in voltage of the bridge is in the range of 28 V to 32 V. To investigate the effect of stress in the bridge, the intrinsic stress in the bridge is varied from 0 MPa to 100 MPa in CoventorWare which corresponds to spring constants of 1.33 N/m, 5.03 N/m and 8.68 N/m respectively. It is concluded that the stress in the bridge resulted from the fabrication process could change the pull-in voltage from the designed value. Finally, a fabrication process using 5 mask layers is proposed for the 5-bit MEMS varactor.

Chapter 4: Fabrication and Measurement of Single-Bridge MEMS Varactor using SU-8

4.1 Introduction

This chapter details the fabrication processes and techniques used to fabricate single-bridge MEMS varactors using the facilities available in Scottish Microelectronics Centre (SMC) cleanroom of the University of Edinburgh. The fabrication of single-bridge MEMS varactors is carried out rather than the multiple bridges varactor designs as presented in Chapter 3 to simplify the fabrication process. The main objective of this fabrication is to investigate and prove the advantages of using SU-8 as a base layer to reduce the parasitic and fringing field capacitance thereby increasing the capacitance ratio of the varactors. Besides, the use of SU-8 as a thick passivation layer on a low resistivity silicon for the fabrication of the varactors can also replace the need for the high resistivity silicon (HRS) which can significantly reduce the cost of the MEMS varactors. Two types of bridges namely fixed-fixed structure and truss configurations have been implemented in the varactors. Several bridges of different lengths and widths have been fabricated for both types of the bridge designs. A comparison and analysis between these two types of structures are carried out to investigate the effectiveness of the proposed truss bridge in reducing the pull-in voltage of the varactors. This chapter also presents the challenges faced during the fabrication of the novel SU-8 based MEMS varactors and the solutions taken to mitigate the issues.

4.2 Mask Design of a Single-Bridge MEMS Varactor

This section discusses the mask design of a single-bridge MEMS varactor using SU-8 as a thick separation layer between the varactor and the silicon substrate. The structure of the single-bridge MEMS varactor as shown in Figure 4.1 requires 4 mask layers. There are several modifications that have been made to the proposed fabrication steps of the multiple bridges MEMS varactors presented in Chapter 3 in order to realise the

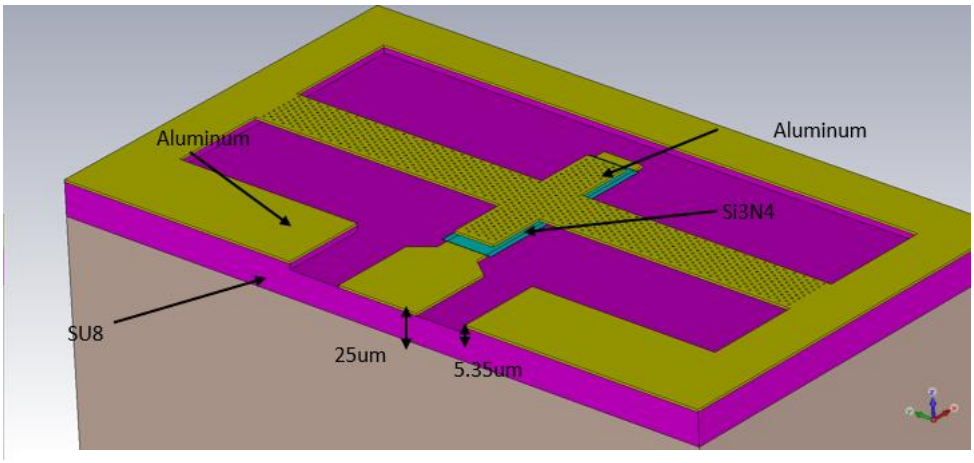


Figure 4.1: Single-bridge MEMS varactor design.

single-bridge MEMS varactor. In addition to using only a single-bridge in the MEMS varactor, the side pull-down electrodes as proposed in the initial fabrication will be removed where the varactors will be actuated by applying a DC voltage on the centre conductor of the CPW transmission line. This step will reduce the number of masks required from 5 layers to 4 layers hence simplifying the fabrication process. The new fabrication process is illustrated in Figure 4.2. Table 4.1 shows the summary of the main structures of the varactor, materials used and masks required for the realisation of the MEMS varactor. It is to be noted that although the varactor design has been simplified compared to the ones proposed in Chapter 3, the use of SU-8 to reduce the parasitic and fringing field capacitance is still maintained in the new varactor structures. Therefore, the main objective of implementing SU-8 in the MEMS varactor design to increase its capacitance ratio as proposed in this thesis can still be validated by the experimental work.

Table 4.1: Layer, material and mask of a single-bridge MEMS varactor

Layer	Material	Mask Required
Base layer	SU-8	No
Centre conductor	Aluminium	Yes
Dielectric	Silicon Nitride	Yes
Anchor of the bridge	SU-8	Yes
Sacrificial layer	Silicon Dioxide	No

Ground and bridge	Aluminium	Yes

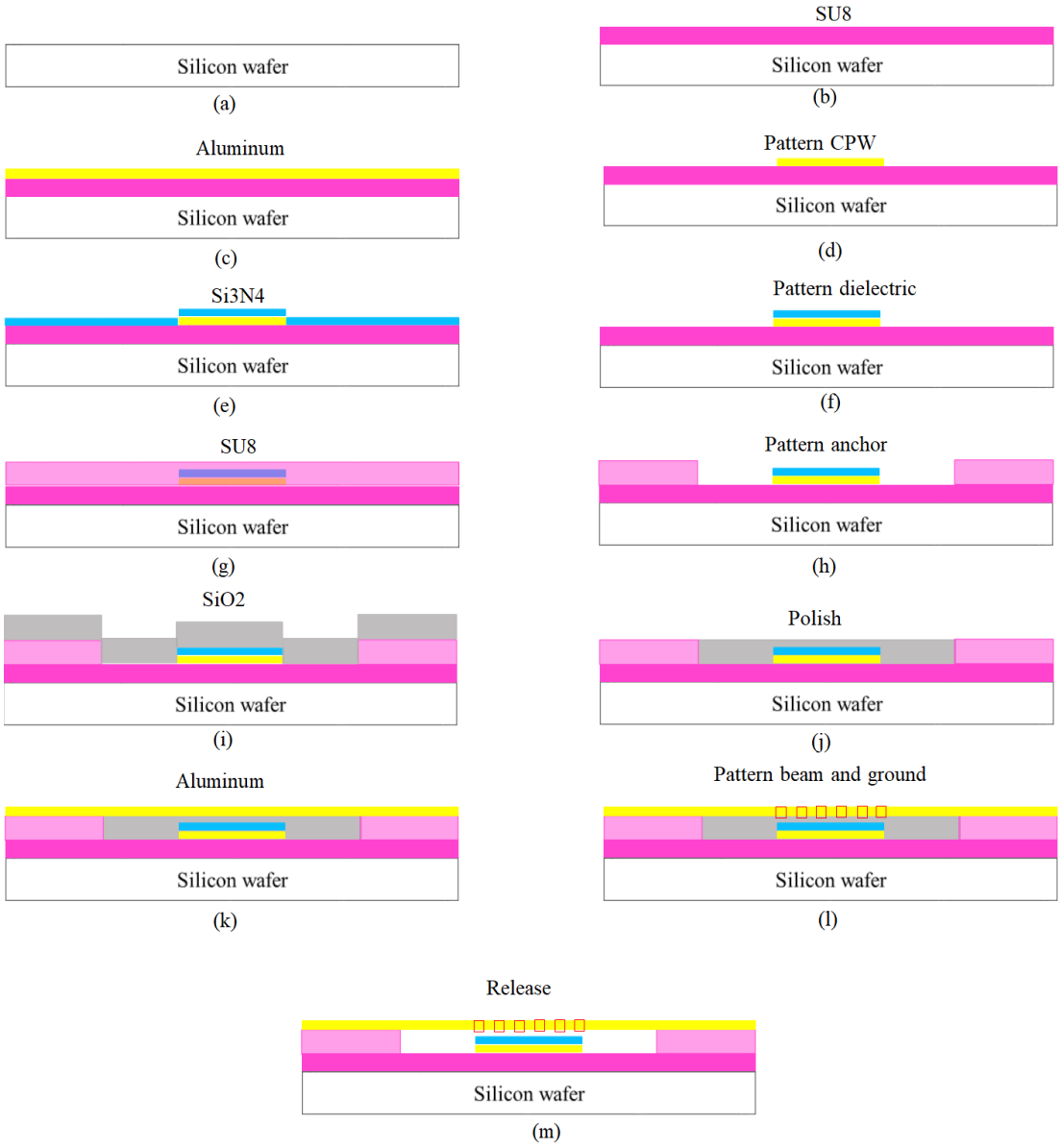


Figure 4.2: Fabrication process of the single-bridge MEMS varactor.

The mask design consists of several variations of the single-bridge MEMS varactor with different lengths and bridge types. Moreover, the width of the structure is also varied in the design. Figure 4.3 and 4.4 shows the detailed dimensions of the bridge structures for the varactor. The entire device consists of 4 process layers as shown in Figure 4.5 to Figure 4.6. The first layer defines the centre conductor of the CPW transmission line utilised in the varactor on a thick SU-8 layer. The dielectric layer

made of silicon nitride (Si_3N_4) is formed using the second layer. The third layer is used to pattern the SU-8 to form an anchor for the subsequent bridge construction process. The final layer defines the bridge and the ground of the CPW transmission line. The final wafer layout on a 4-inch wafer is shown in Figure 4.7.

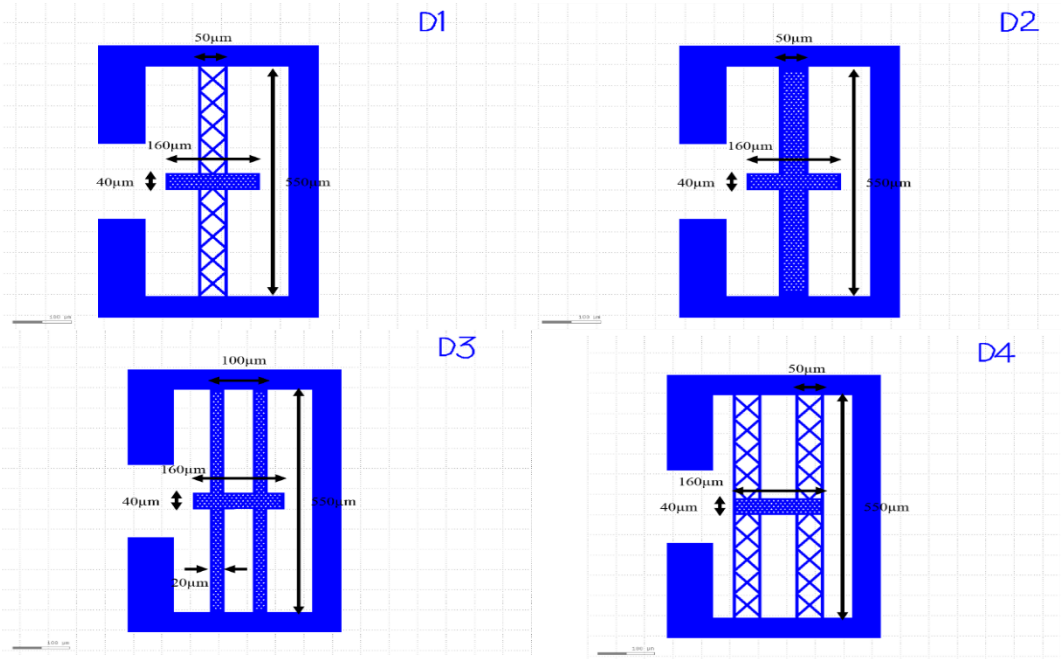


Figure 4.3: Dimensions of the bridge structures for D1 to D4.

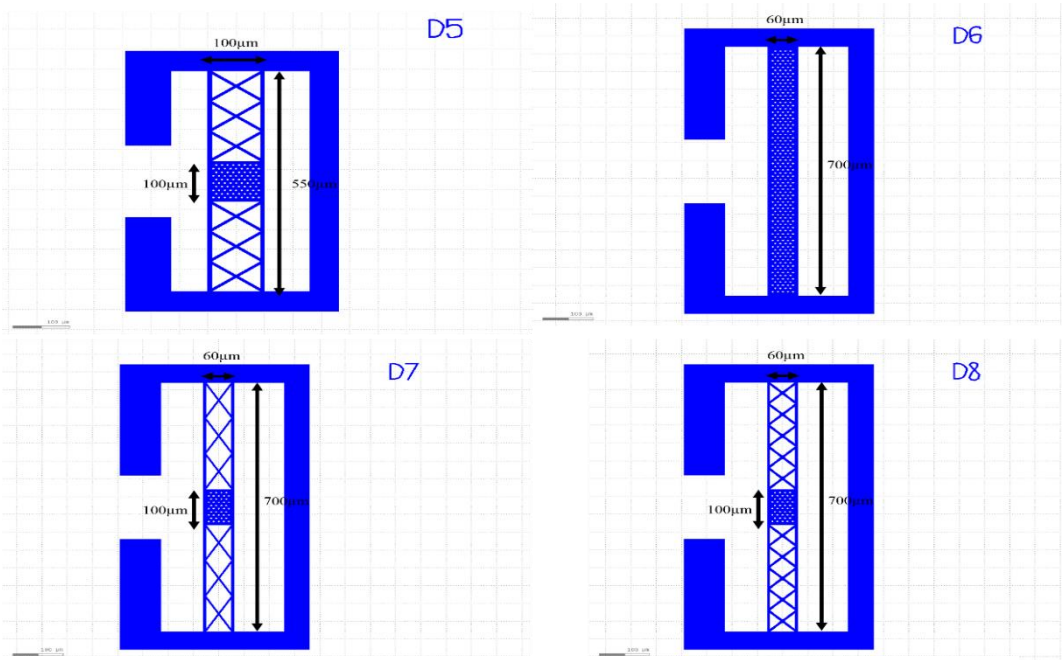


Figure 4.4: Dimensions of the bridge structures for D5 to D8.

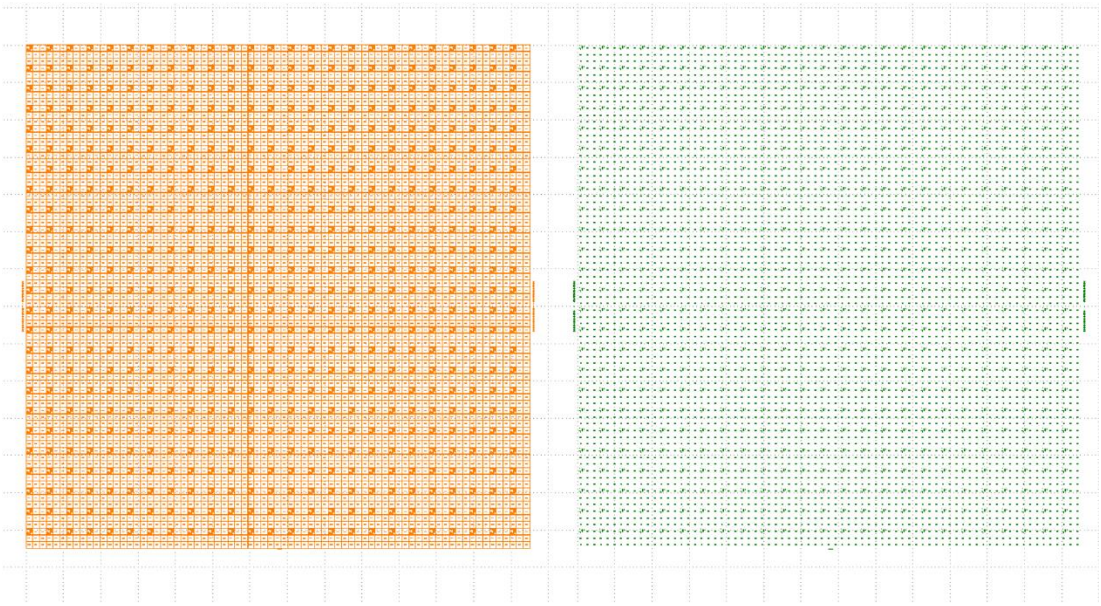


Figure 4.5: Mask layer 1 and layer 2.

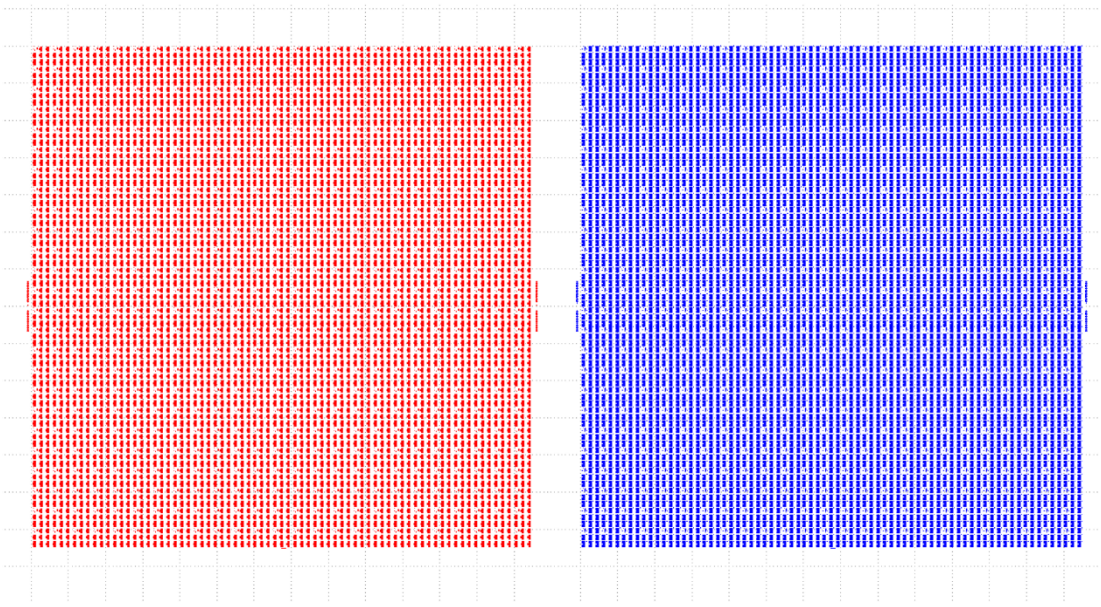


Figure 4.6: Mask layer 3 and layer 4.

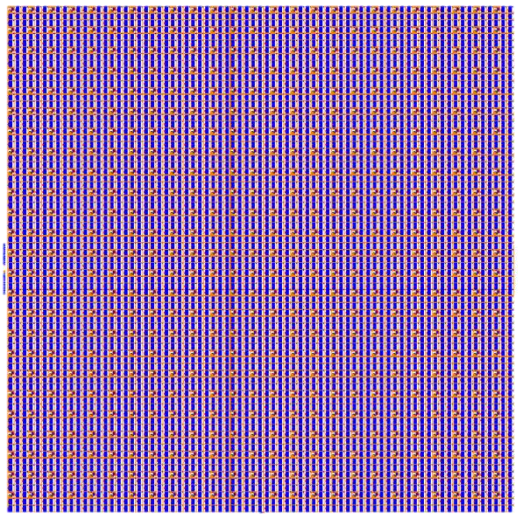


Figure 4.7: Full mask layer.

4.3 Initial Fabrication of the Single-Bridge MEMS Varactor

An initial fabrication was carried out to fabricate the single-bridge MEMS varactor on a dummy silicon wafer. A single MEMS bridge is suspended over a CPW transmission line to form a 1-bit MEMS varactor. The centre conductor of the CPW transmission line is used to apply a DC voltage in order to pull the bridge towards the dielectric layer.

The initial fabrication process has been conducted according to Figure 4.2. The process starts with the exposure of a fresh silicon wafer in a barrel asher for approximately 1 hour to remove any contaminants from the silicon surface. This step is very important in order to obtain maximum process reliability, especially before the coating of a thick SU-8 layer on the substrate in the next process. Alternatively, this step can also be carried out using a hot plate.

In this design, SU-8 polymer is used as a base layer to elevate the device from the substrate in order to reduce the fringing field capacitance and the substrate losses. As with other resist materials, there are several steps that need to be performed to pattern SU-8 including spin coat, soft bake, exposure under ultra-violet (UV) light, post expose bake (PEB) and develop. However, for the implementation of a thick

passivation layer in the design, the SU-8 layer will not be patterned, hence requiring no mask. Therefore, to form a 20 µm thick base layer, SU-8 25 is spin coated on the silicon substrate. Next, the SU-8 is soft baked to evaporate the solvent before it can be exposed under UV light to cross-link the resist. After exposure under the UV light, post exposure bake (PEB) is carried out. Subsequently, to further cross-link and cure the SU-8 layer, hard bake is needed at temperature of 210 ^{o}C for 1 hour using a hot plate. However, it is important not to exceed the temperature above 250 °C in order to avoid cracks in the film as well as to ensure that the subsequent processes' temperature is below the temperature used during the hard bake process. As a result, the subsequent steps have been carried out at a temperature below 200 ^{o}C. After the SU-8 layer has been cured, 300 nm thick aluminium is sputtered and patterned using dry etching process to form the CPW transmission line. Due to moderate adhesion between aluminium and SU-8 as reported in [76], SU-8 must be treated in a barrel asher for 5 minutes to increase its surface roughness. By using plasma enhanced chemical vapour deposition (PECVD) technique, 2500Å Si_3N_4 is patterned on top of the centre conductor as a dielectric layer. In this process, 150 °C instead of 300 °C for plated shower temperature is used to make sure it will not affect the bottom SU-8 layer. Next, around 3 µm thick SU-8 2 is spin coated, patterned and cured up to 210 °C to form the anchor. Afterwards, silicon dioxide with thickness of 4 µm is deposited using PECVD technique. However, it has been observed that after the oxide deposition process, the oxide layer would be delaminated from the bottom SU-8 anchor. This issue will be explained in the next subsection and some suggestions have been carried out to address the problem.

4.3.1 Adhesion Problem between SU-8 and Silicon Dioxide

Based on the previous fabrication process, an adhesion problem between oxide and SU-8 layer has been encountered where the process has to be halted to find a solution to resolve the issue. It was planned that the deposited oxide would fill the cavity formed by the SU-8 anchor where it would finally be planarised using chemical mechanical planarisation (CMP) technique. The main reason for the weak adhesion of

oxide layer on SU-8 is due to hydrophobic nature of the SU-8 and its low surface roughness. The delamination of the deposited oxide on SU-8 is shown in Figure 4.8.

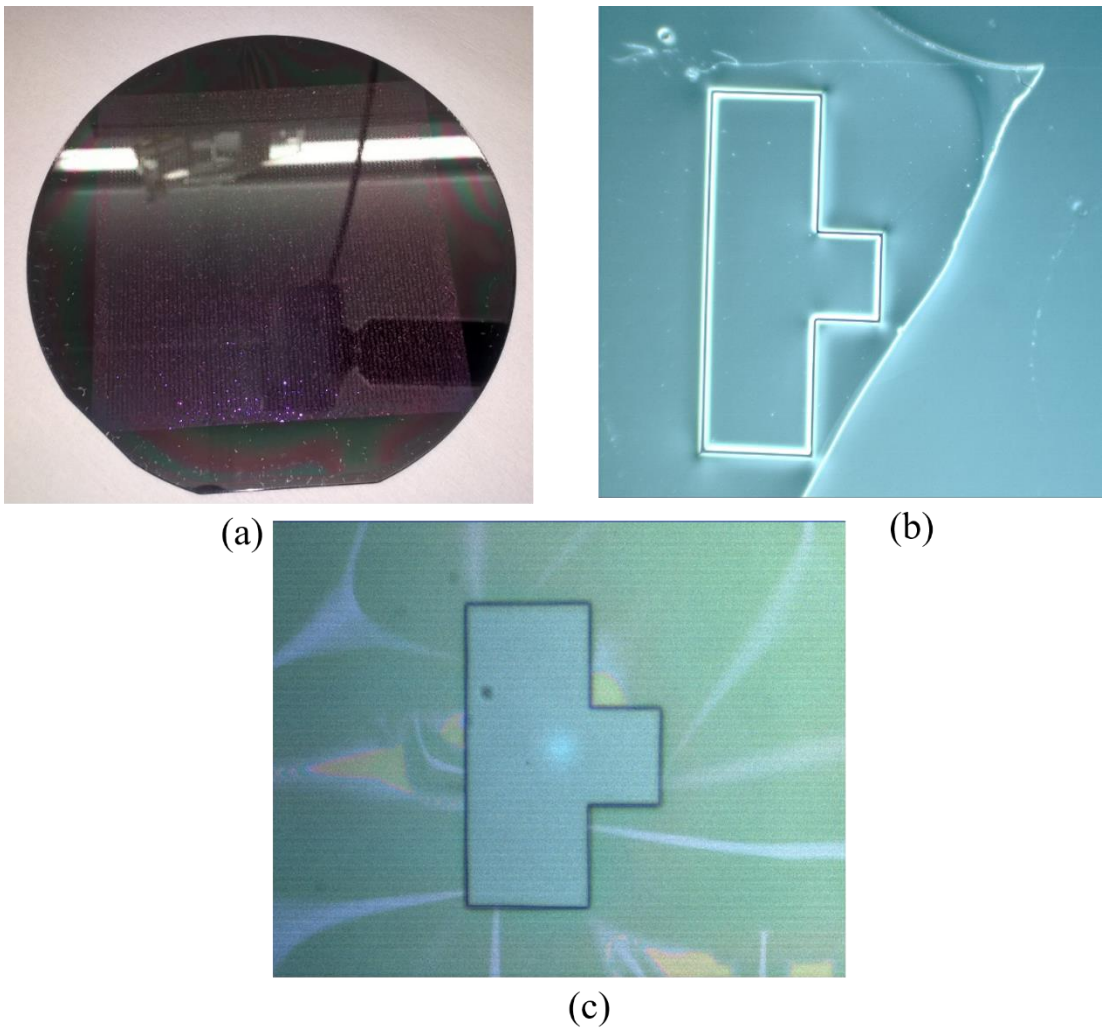


Figure 4.8: Delamination of SiO2 from the wafer. (a) For the whole wafer, (b) and (c) when observed under a microscope.

4.3.1.1 Improvement of the Adhesion by Activating the Surface of the SU-8 using Oxygen Plasma

To improve the adhesion between these two layers, oxygen plasma treatment as suggested in [77] has been conducted on the wafer before the deposition of the oxide where successful adhesion between oxide and SU-8 has been reported. It is expected that by applying this technique, the surface roughness of the SU-8 will increase hence

providing better adhesion with the oxide. In this step, the wafer was placed in the barrel asher for 5 minutes to activate its surface. Next, the deposition of oxide was carried out on the SU-8 layer. The wafer was then inspected to see if there is any improvement on the adhesion of the oxide layer on SU-8. Unfortunately, the delamination of the oxide layer was still observed even after applying the oxygen plasma treatment. To further investigate if additional oxygen plasma treatment time could eventually mitigate the delamination of the oxide from the SU-8 layer, the treatment time was increased to 10, 15 and 20 minutes using several samples. The deposition of oxide was repeated and inspected afterwards. Again, the same delamination effect was observed. It is concluded that due to the adhesion problem of silicon dioxide on SU-8 material, the use of oxide as sacrificial layer for the fabrication of the MEMS varactor is no longer feasible.

4.4 Improved Fabrication Process by using SU-8 as Sacrificial Layer

Due to the delamination of oxide films from the devices, different sacrificial layer materials are needed to complete the fabrication process. It is found that SU-8 can also be used as a sacrificial layer as reported in [16] to fabricate an RF MEMS switch. Based on the reported study, the fabrication process of the MEMS varactor was revised to replace the oxide with SU-8 as the sacrificial layer. In this new process, the mask for patterning the SU-8 as an anchor for the varactor is no longer needed thus reducing the number of mask layers required to three instead of four. Instead, the bridge and the ground of the CPW transmission line can be directly deposited after the SU-8 coating step. To release the bridge, the exposed SU-8 will be etched using dry etch process using oxygen plasma. The unexposed SU-8 below the ground will eventually form an anchor for the bridge. The new fabrication process utilising SU-8 as sacrificial layer is illustrated in Figure 4.9. Based on this modification, the SU-8 in the proposed MEMS varactor design now serves as a thick passivation layer, an anchor to the bridge and as sacrificial layer. This adds to the novelty of the fabricated MEMS device.

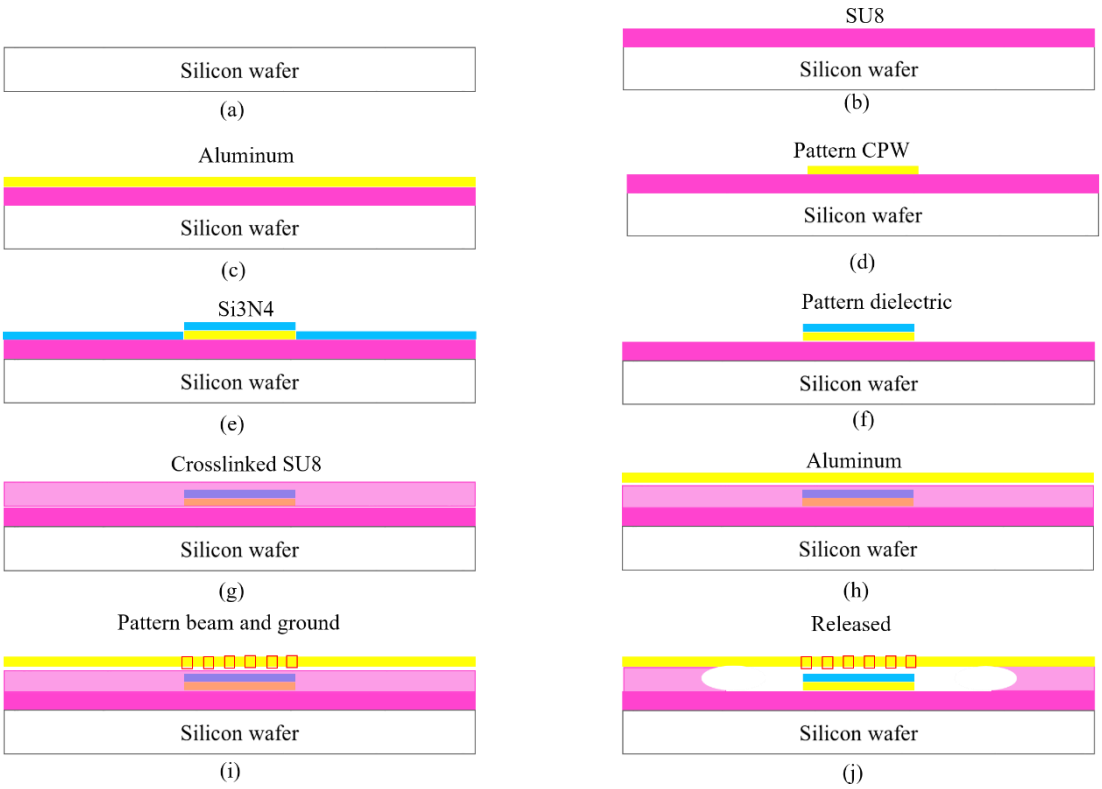


Figure 4.9: Fabrication process using SU-8 as an anchor and sacrificial layer.

Firstly, a simple experiment has been conducted to use SU-8 as an anchor and sacrificial layer in order to investigate the etching rate to release the MEMS bridges. By using only Mask 4, the bridges of the varactor were patterned on the SU-8 layer. The process required only three steps as shown in Figure 4.10. First, SU-8 was spin coated on a fresh test wafer and then soft baked at 65 ^{0} C and 95 ^{0} C for 1 minute and 3 minutes respectively before it was blanket exposed under UV light for 45 s. After that, it was post baked at 65 ^{0} C and 95 ^{0}C for 1 minutes and 3 minutes respectively before being cured at 200 ^{0}C for 1 hour. Next, the ground and the bridge were patterned using a negative photoresist, AZ nLOF 2035 before depositing a 1 µm thick aluminium using an e-beam evaporation technique. The transfer structure has been realised using photolithographic process. Afterwards, the lift-off process was performed by soaking the wafer in Microposit Remover 1165 and placing it in a water bath at temperature of

50 ^{0}C to 60 ^{0}C. The wafer was then agitated using sonic function in order to speed up the lift-off process.

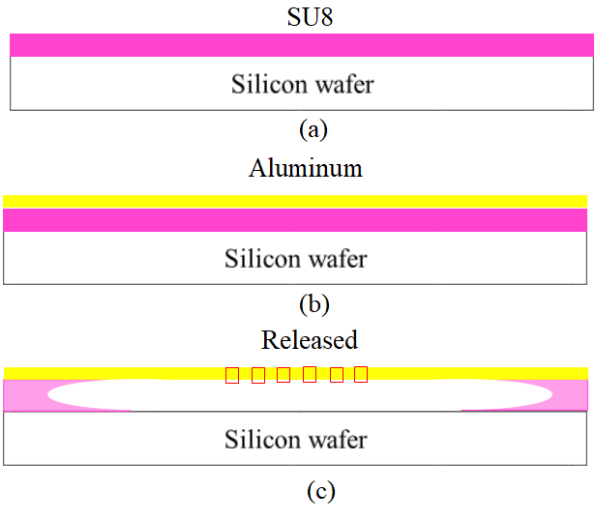


Figure 4.10: Fabrication of the MEMS bridge on SU-8.

Table 4.2: Parameters used to release the bridge

SU-8 thickness	Temperature	Power	O2	N2	Time
3 um	200 °C	5000	1000 sccm	100 sccm	10 minutes

The release step has been carried out using a MEMSSTAR oxygen plasma tool. The time required to completely release the bridge is around 10 minutes with temperature of 200 °C, oxygen flow of 1000 sscm and nitrogen flow of 100 sscm as listed in Table 4.2. Figure 4.11 (a) shows the fabricated devices based on the new fabrication process. To analyse the structure for any abnormalities or defects, scanning electron microscope (SEM) inspection was done as shown in Figure 4.11 (b) and (c). The inspection showed that the anchor of the bridge is almost completely etched at the edges whereas the centre part of the bridge at was not fully released yet. Upon further investigation, this problem comes from the dry etching process that produces isotopic etching of the SU-

8 by the oxygen plasma causing the unexposed SU-8 under the ground of the CPW line to be etched away as shown in Figure 4.12. From this observation, additional exposure time in oxygen plasma is required to fully release the bridges. However, another issue might arise if the exposure time needed to release the bridge is more than

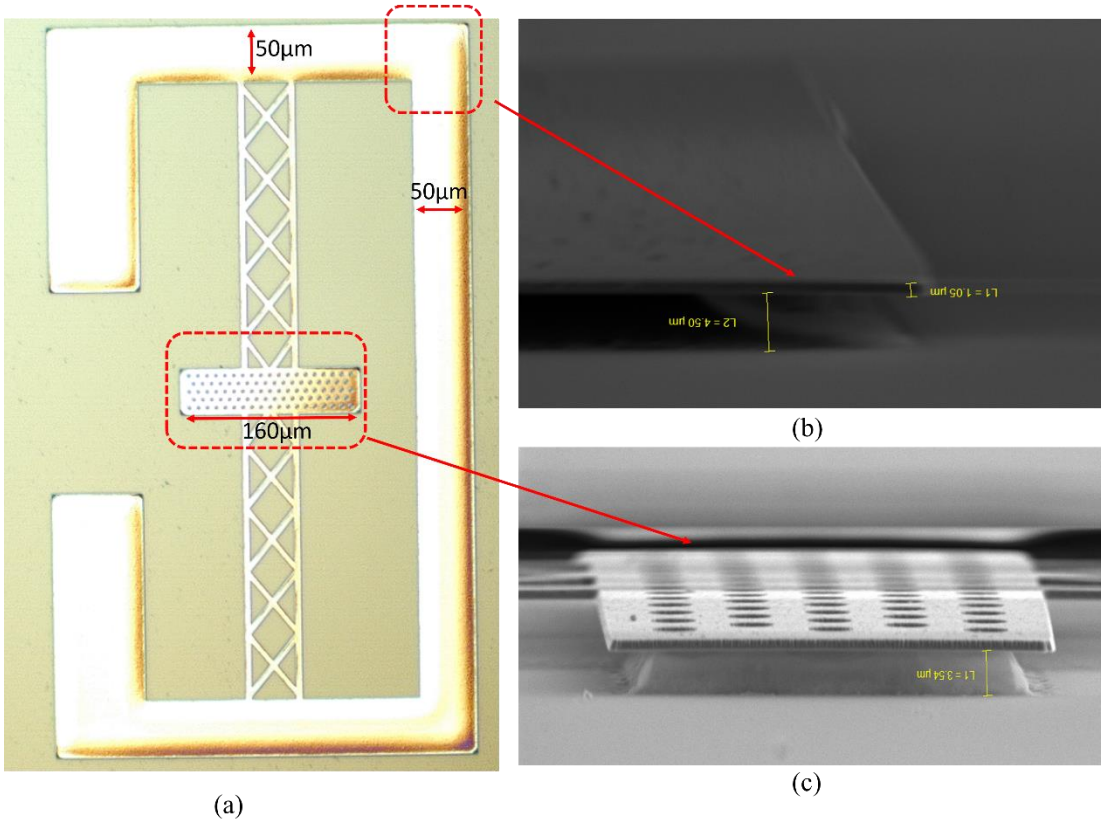


Figure 4.11: (a) Fabricated MEMS bridges under a microscope. (b) MEMS bridge under an SEM where the SU-8 anchor is etched away. (c) MEMS bridge is not completely released.

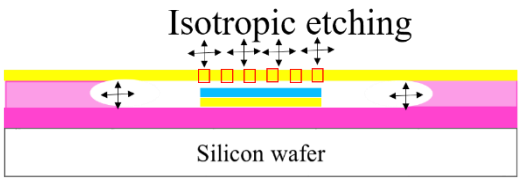


Figure 4.12: Isotropic etching.

the expected time, causing the anchor to collapse due to over-etching of the SU-8 anchor by the oxygen plasma. Therefore, for further investigation, the full device of the single-bridge MEMS varactor have been fabricated completely.

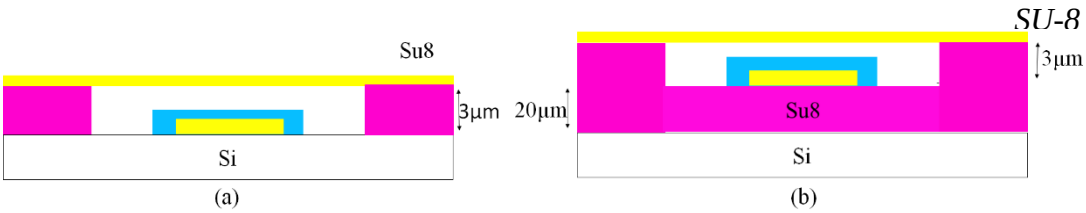


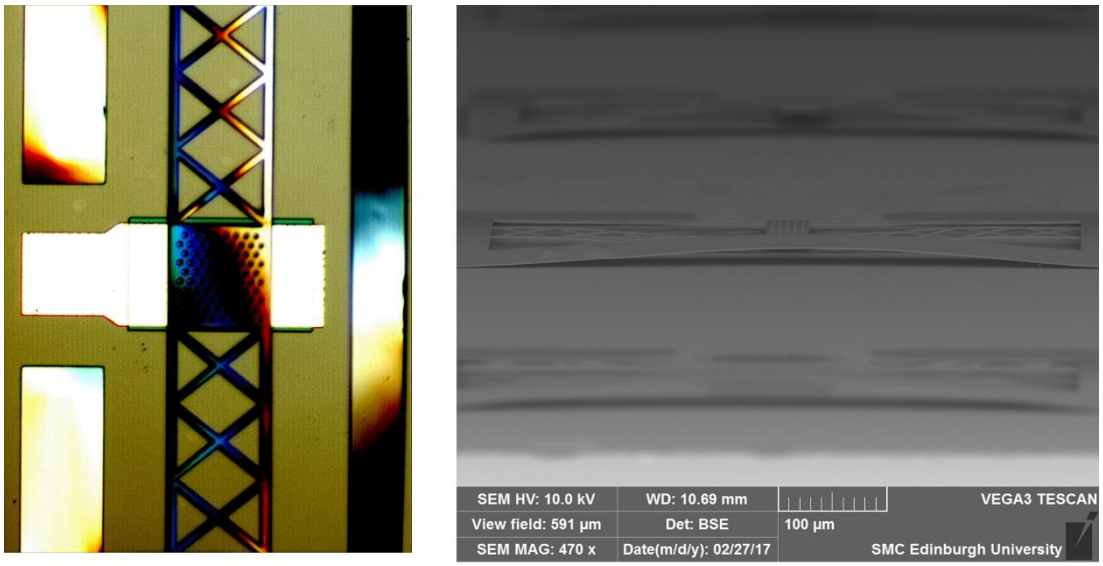
Figure 4.13: (a) MEMS varactors on Silicon (b) MEMS varactors on SU-8.

4.4.1 Fabrication of a Single-Bridge MEMS Varactor using SU-8 as a Sacrificial Layer

To further investigate the ability of SU-8 to serve as both a base layer and sacrificial layer for the MEMS varactor as well as to reduce the fringing field capacitance to increase the capacitance ratio of the varactor, two types of MEMS varactor designs have been fabricated as shown in Figure 4.13. In the first design, a standard MEMS varactor without SU-8 base layer is fabricated. For the second design, the varactor is fabricated by implementing a 20 µm thick SU-8 base layer with the aim to increase the capacitance ratio of the varactor. The fabrication process for both devices has been conducted by following the steps shown in Figure 4.9. However, for the varactor without the SU-8 base layer, step (b) has been skipped, directly proceeding with the deposition of aluminium in step (c). Finally, the MEMSSTAR oxygen plasma tool has been used for the release process of the devices. Table 4.3 shows the parameters used in this fabrication process. The time inside the oxygen plasma tool was varied from 5 minutes, 10 minutes and 15 minutes to obtain the optimum time for the moveable membrane to be released.

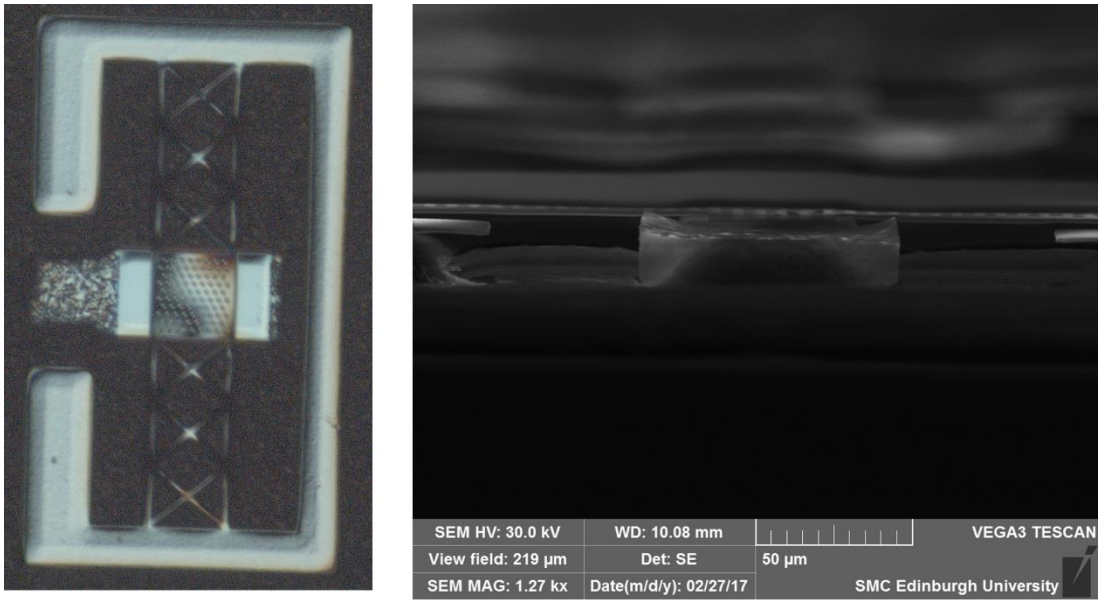
Table 4.3: Parameter used to release the MEMS bridges

Exp	SU-8 Sacrificial Thickness(µm)	Temperature (^{o}C)	Power (W)	O2 (sccm)	N2 (scc)	Time (min)	Observation from microscope	
							SU-8 base layer	Without SU-8 base layer
	3	200	5000	1500	80	15	Most of the bridges and grounds were bulking	Most of the bridges and grounds collapsed
	3	200	5000	1500	80	10	Most of the bridges and grounds were bulking	Most of the bridges and grounds collapsed
	3	200	5000	1000	80	5	The bridges were not released	The bridges were not released but the anchors were already over etched



(a) (b)

Figure 4.14: MEMS varactor without SU-8 base layer seen (a) under a microscope (b) under an SEM.



(a) (b)

Figure 4.15: MEMS varactor with SU-8 base layer seen (a) under a microscope (b) under an SEM.

Based on the inspection under a scanning electron microscope (SEM) as illustrated in Figure 4.14 to Figure 4.16, it is observed that the device with a thick SU-8 layer, the bridge seems to be released at both ends of the bridge. However, most of the centre part of the bridge seem to stick to the layer below indicating that the bridge was still not fully released. As for the varactor without the SU-8 layer, most of the SU-8 anchor to support the bridge was etched away causing the whole structure to collapse to the bottom centre conductor and the substrate. The collapse of the device is more pronounced for structures with bridge length of more than 550 µm. To prevent the varactors from collapsing, a new mask was designed by applying several modifications on the bridge structure such as increasing the size of the holes in the bridge, enlarging the ground of the CPW transmission line and limiting the length of the bridges.

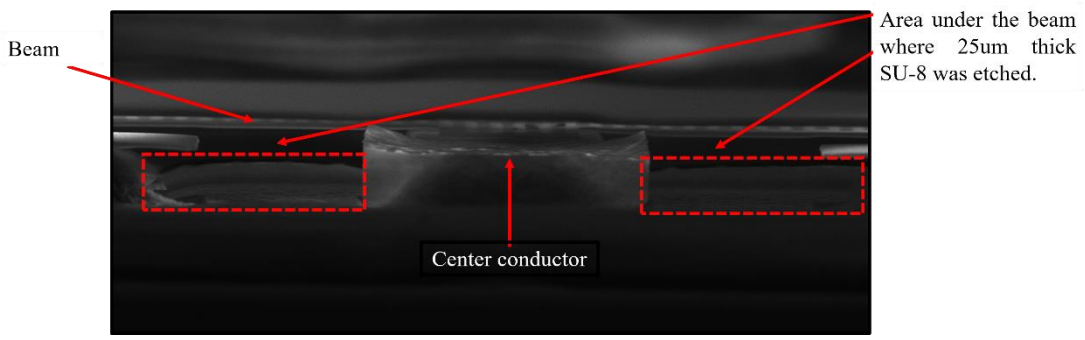


Figure 4.16: Detailed picture of the MEMS varactor under SEM.

4.5 Enlarging the Ground of the CPW Transmission Line in a New Mask Design

Based on the recommendations in the previous section, a new mask design for the final layer was created as shown in Figure 4.17 to Figure 4.19. There are several important changes that have been made to the previous design to prevent the devices from collapsing. One of the main changes is the enlargement of the ground of the varactors in order to ensure the SU-8 layer that acts as an anchor for the bridge will not be completely etched away. The minimum width of the ground was increased from 50 µm to 240 µm. It is expected that a larger ground size will help to sustain the etching

process so that the bottom SU-8 could firmly form an anchor for the varactors. Secondly, in the previous bridge structure, the size of the holes is only 2 µm × 2 µm. Because of its small size, the hole might not be completely removed during the lift-off process. Since the holes are designed to help with the release of the bridge, an incomplete formation of holes increases the etching time required. Moreover, a horizontal etch depth of 25 µm is required to completely release the bridge if the holes are not created. Considering that the oxygen plasma etching process is an isotropic etching where the etch rate is equal in all directions, the SU-8 layer under the ground would also be etched. Therefore, to facilitate the bridge release process, the size of the holes is increased to 10 µm × 10 µm. The fabrication process was again repeated using the new mask design.

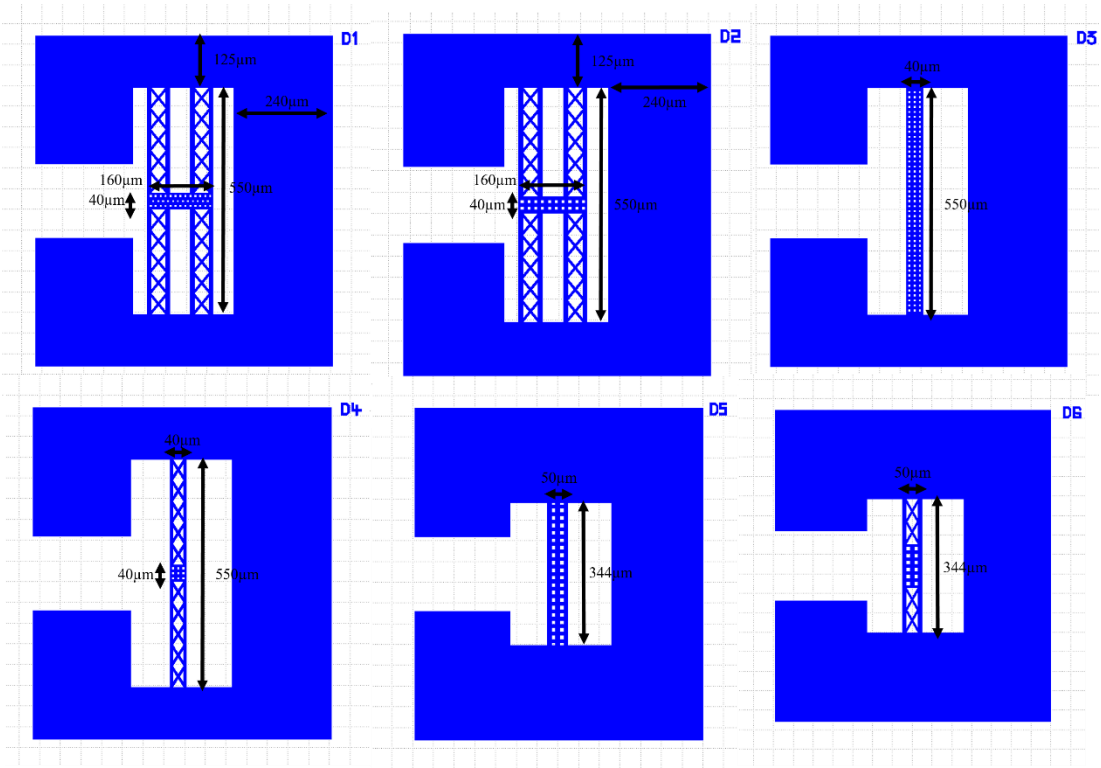


Figure 4.17: New mask for MEMS bridge designs (D1 to D6).

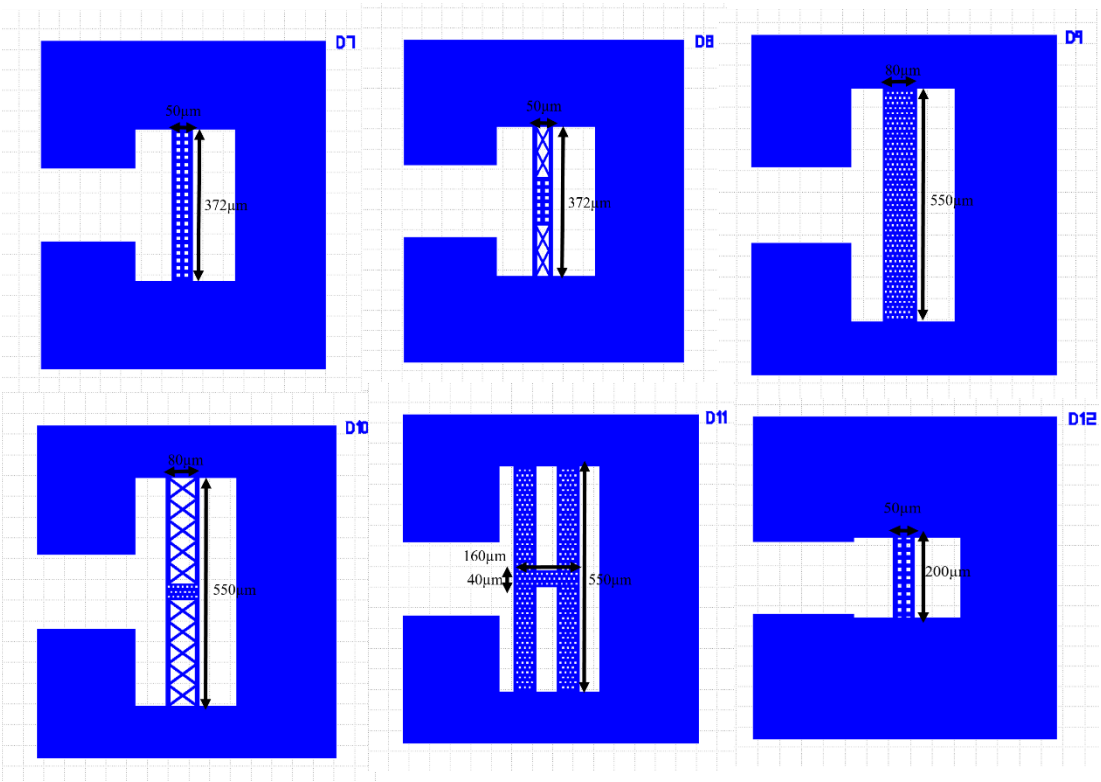


Figure 4.18: New mask for MEMS bridge designs (D7 to D12).

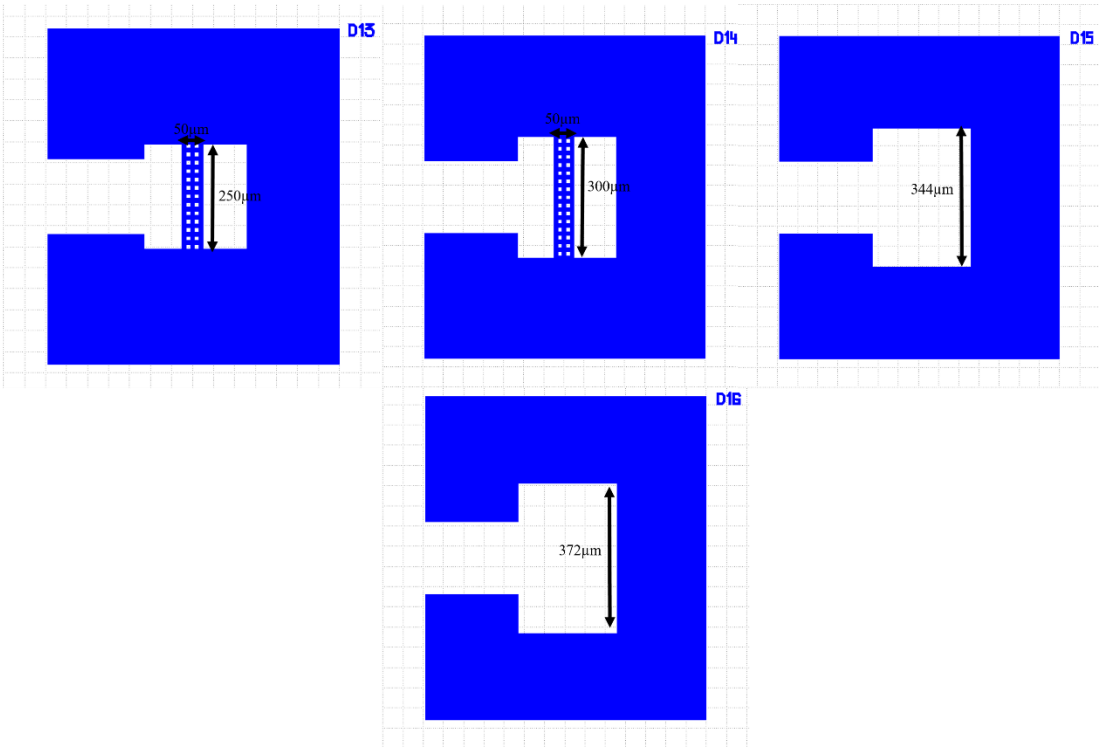


Figure 4.19: New mask for MEMS bridge designs (D13 to D16).

The final fabricated devices using the revised mask were again inspected under an optical microscope and SEM as shown in Figure 4.20. It is observed that majority of the structures are intact and the bridges are suspended over the centre conductor of the one port CPW transmission line as exhibited in Figure 4.21 and Figure 4.22. It is found that the yield from the fabrication is around 90%.

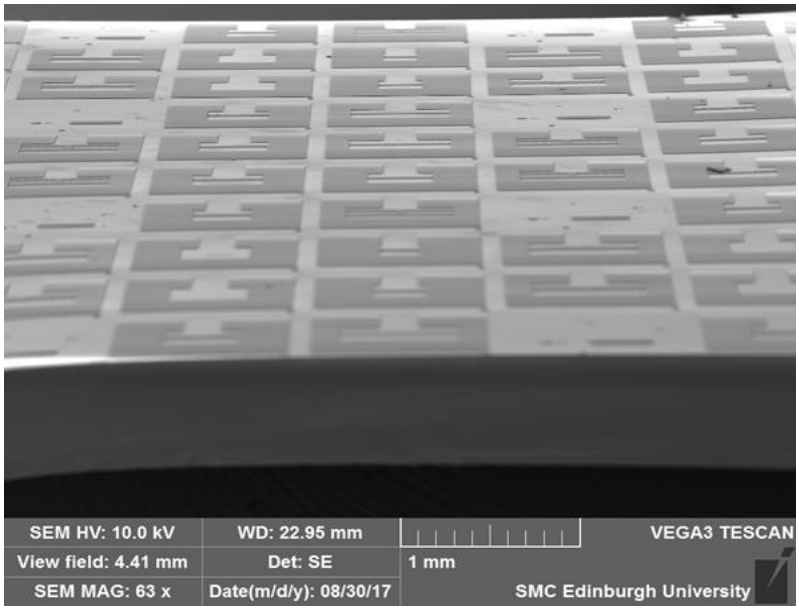


Figure 4.20: Fabricated single-bridge MEMS varactors.

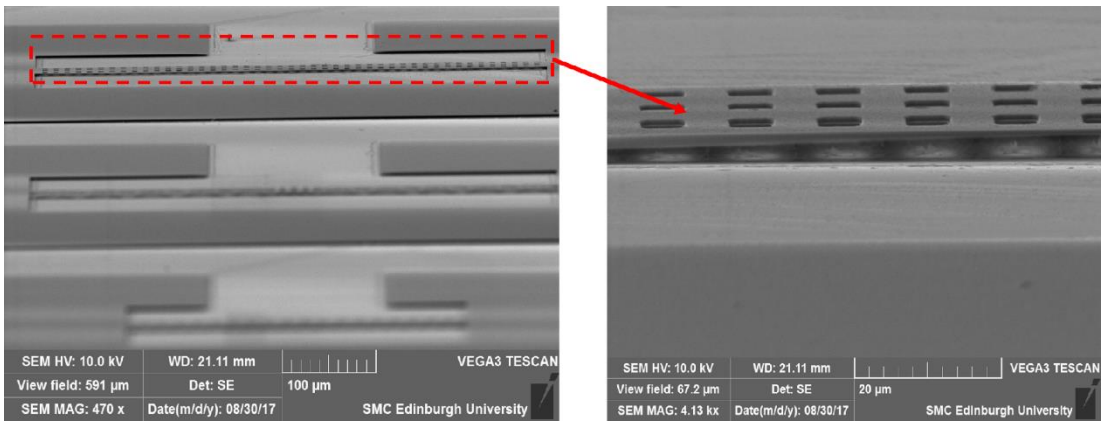


Figure 4.21: MEMS varactor with solid fixed-fixed bridge design.

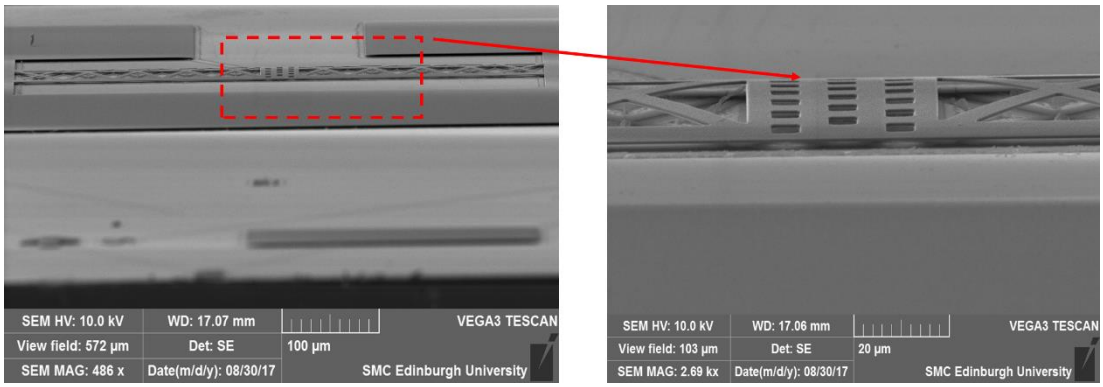


Figure 4.22: MEMS varactor with truss bridge design.

4.5.1 Testing of the Fabricated Single-Bridge MEMS Varactor

To verify the functionality of the fabricated MEMS devices, actual measurements were carried out to verify whether the varactors could be actuated. The best sample or chip was selected based on the visual inspection under the microscope. The selection was carried out by looking at the number of varactors that survived at that particular sample. As a result, fourteen bridge designs have been measured on the selected chip.

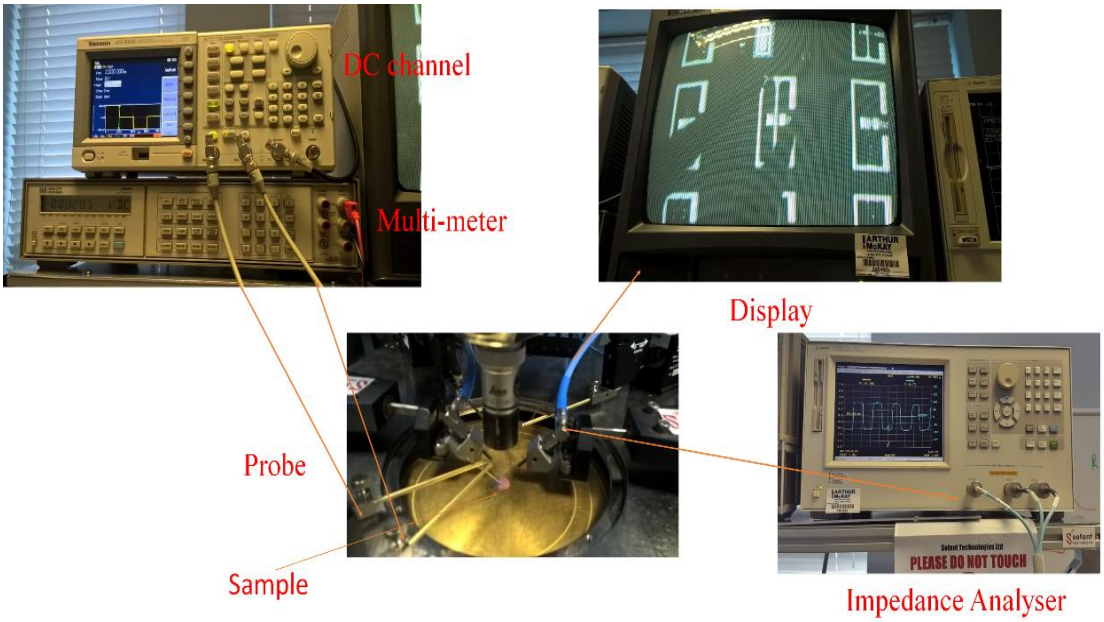


Figure 4.23: Measurement setup for actuation voltage and capacitance of the varactor.

Figure 4.23 shows the measurement setup to measure the actuation voltage and the capacitance of the single-bridge MEMS varactor with various bridge designs. The probe station is connected to an impedance analyser, an LCR multimeter and a DC power supply. A dual channel high voltage wideband amplifier 9200A is used as the DC power supply to supply the voltage to actuate the varactor while the impedance analyser is used to determine the capacitance value from the device.

4.5.2 Pull-in Voltage Measurements

The first test that has been carried out on the MEMS devices is to measure their pull-in voltage. This test can demonstrate the displacement of the bridges under DC voltage which gives positive indication of their functionality. It is known that the pull-in voltage of MEMS bridges is mainly dependent on the bridge thickness, bridge length and the air gap formed between the top and bottom electrodes. The calculated and measured pull-in voltages of the bridge designs are given in Table 4.4. Based on the measurement results, the bridge with a length of 200 µm could not be actuated. This could be due to the high spring constant of the bridge due to its shorter length. In general, for the same bridge dimensions (i.e. length and width), the truss structure has lower pull-in voltage than the standard solid fixed-fixed structure with an average reduction of 12.5%. It can be concluded that the use of truss bridge can potentially reduce the actuation voltage of the MEMS bridge over the standard solid fixed-fixed bridge design.

Table 4.4: Calculated and measured pull-in voltage of the bridges

Design	Calculation Voltage (V)	Measurement Voltage (V)
1	12	30
2	12	35
3	8.98	35
4	6.38	30
5	13	45
6	9.68	40
7	9.68	40
8	13	45
9	10	30
10	7.1	30
11	10	40
12	46.57	-
13	30.81	50
14	22.5	45

4.5.3 Capacitance measurements

The fabricated MEMS varactors were then measured using the impedance analyser to verify the effect of employing the thick SU-8 base layer on the varactor design to reduce the fringing field capacitance. Initially, the single-bridge MEMS varactor designs were simulated to determine their capacitance ratio. Then, a comparison was made between two similar MEMS varactor with and without the utilisation of the SU-

8 base layer on a high-resistivity silicon substrate. Table 4.5 shows the simulated capacitance values and capacitance ratios of the varactors.

Table 4.5: Simulated capacitance ratio with SU-8 and without SU-8 layer

	with SU-8 layer on HRS substrate			without SU-8 layer on HRS substrate		
Design	**Up-state Capacitance (F)**	**Down-state Capacitance (F)**	**Capacitance Ratio**	**Up-state Capacitance (F)**	**Down-state Capacitance (F)**	**Capacitance Ratio**
1	5.29794E-14	1.51053E-12	28.51163	6.54513E-14	1.51053E-12	23.07869
2	5.31311E-14	1.50528E-12	28.3314	6.47585E-14	1.49454E-12	23.07869
3	3.86279E-14	5.28071E-13	13.67073	4.77212E-14	5.28071E-13	11.06575
4	3.99956E-14	5.34591E-13	13.36626	4.94109E-14	5.34591E-13	10.81929
5	8.36211E-14	1.56513E-12	18.71689	1.03306E-13	1.56513E-12	15.15036
6	5.10635E-14	1.68709E-12	33.03896	6.30843E-14	1.68709E-12	26.74334
7	5.48356E-14	1.56513E-12	28.54217	6.63895E-14	1.56513E-12	23.57491
8	5.37389E-14	1.56513E-12	29.12466	6.77444E-14	1.56513E-12	23.10342
9	4.33163E-14	8.959E-13	20.68276	5.35133E-14	8.959E-13	16.74163
10	4.38278E-14	8.71849E-13	19.89262	5.41452E-14	8.71849E-13	16.10205
11	5.19622E-14	1.5283E-12	29.41176	6.41946E-14	1.5283E-12	23.80731
14	5.14681E-14	1.60377E-12	31.16049	6.35842E-14	1.60377E-12	25.22282

It can be seen that by using SU-8 as a base layer to separate the varactors from the silicon substrate, the simulated capacitance ratio of the varactors is improved by approximately 23.46%. To verify this finding, another comparison was made for the fabricated MEMS varactors as shown in Table 4.6. However, it is observed that there is a reduction in the down-state capacitance values of the varactors compared to the simulation results. On the other hand, the measured up-state capacitances of the varactors show good agreement with the simulation results. Although the capacitance ratios of the fabricated varactors were smaller than the simulated values, the effect of employing the thick SU-8 base layer in the design to reduce the fringing field

capacitance can still be observed by comparing the capacitance ratios of the varactors when fabricated with and without the SU-8 layer. An improvement of 56.75% in the capacitance ratios of the MEMS varactors is achieved by using the thick SU-8 base layer.

Table 4.6: Measured capacitance ratio with SU-8 and without SU-8 layer

	with SU-8 layer on HRS substrate			**without SU-8 layer on HRS substrate**		
Design	**Up-state Capacitance**	**Down-state Capacitance**	**Capacitance Ratio**	**Up-state Capacitance**	**Down-state Capacitance**	**Capacitance Ratio**
1	3.34894E-14	1.44752E-13	4.322311	8.33797E-14	2.08516E-13	2.500803
2	4.82418E-14	2.08516E-13	4.322311	8.33797E-14	2.04346E-13	2.450787
3	4.69334E-14	2.00781E-13	4.278009	7.20897E-14	1.96766E-13	2.785162
4	3.36278E-14	1.99855E-13	5.943138	5.16523E-14	1.95858E-13	3.869231
5	5.28587E-14	2.34911E-13	4.444123	8.1191E-14	2.30212E-13	2.893309
6	4.82728E-14	2.31561E-13	4.79692	7.4147E-14	2.26929E-13	3.122995
7	5.01625E-14	2.36192E-13	4.708538	7.70496E-14	2.31468E-13	3.065455
8	5.61207E-14	2.34064E-13	4.170724	8.62014E-14	2.29383E-13	2.715315
9	3.08271E-14	1.87184E-13	3.85328	7.46155E-14	1.8344E-13	2.508646
10	2.86704E-14	1.98632E-13	3.431339	8.89155E-14	1.9466E-13	2.233945
11	5.26612E-14	2.1366E-13	4.057263	8.08876E-14	2.09387E-13	2.641447
14	7.28458E-14	2.43269E-13	3.339506	1.11891E-13	2.38403E-13	2.174157

Additionally, the MEMS varactors were also fabricated on a low-resistivity silicon substrate (5-10 Ω.cm) where SU-8 was again used as a thick separation layer between the varactors and the silicon substrate. A comparison is made between two similar designs with and without the SU-8 layer as shown in Table 4.7. It is seen that the performance of the varactor with the SU-8 layer on the low resistivity silicon substrate shows a significant improvement over the varactor that was fabricated directly on the low-resistivity substrate. It is observed that the up-state capacitance of the MEMS varactors without the SU-8 layer have very a high capacitance value which is due to

the effect of the high conductivity of the LRS substrate. Moreover, the varactors that employ SU-8 layer on the LRS substrate also show similar performances with the ones that use the high-resistivity silicon substrate. It is concluded that by using a thick SU-8 layer to separate the MEMS varactor from the silicon substrate, the capacitance ratio of the varactor can be improved compared to a similar design that do not implement the thick SU-8 layer. Furthermore, fabrication of MEMS varactors on the low-resistivity silicon substrate is also possible by using SU-8 as a thick separation layer to reduce the parasitic field and to prevent the leakage current due to the low-resistivity silicon substrate. Finally, another investigation was carried out to determine the reason for the reduction of the down-state capacitance values of the fabricated MEMS varactors as presented in the next subsection.

Table 4.7: Comparison between the varactors with and without SU-8 on LRS substrate

	with SU-8 layer on LRS substrate			**without SU-8 layer on LRS substrate**		
Design	**Up-state Capacitance**	**Down-state Capacitance**	**Capacitance Ratio**	**Up-state Capacitance**	**Down-state Capacitance**	**Capacitance Ratio**
3	4.576E-14	1.93955E-13	4.23852	3.39179E-12	3.44267E-12	1.015
7	4.91592E-14	2.29106E-13	4.660492	4.48569E-12	4.49915E-12	1.003

4.6 Characterisation of the Fabricated Bridge Structures and their Effect on the Measured Capacitance of the MEMS Varactor

To investigate the reason for the reduction of the down-state capacitance of the fabricated MEMS varactor, the profile of the bridge in the MEMS varactors was measured using a light interferometer as shown in Figure 4.24. It is widely reported that MEMS bridges normally experience high stresses after fabrication process due to several factors including exposure to variable fabrication temperatures[73], [78]–[81]. This causes the MEMS bridges to warp or buckle hence reducing the achievable down-state capacitance.

Figure 4.25 exhibits the top profile of the bridge of the MEMS varactor D7. The detailed profiles along its width and length are shown in Figure 4.26 and Figure 4.27

Figure 4.24: White light interferometer for measuring the bridges profile.

respectively. Based on the profiles of the bridge, it is clearly seen that the bridge warps at both directions at approximately 1 µm. Since the length of the bridge is 377 µm, for it to warp for only 1 µm along its length showed a very good performance. However, the warping of the bridge across its width for 1 µm causes a significant degradation in the down-state capacitance of the MEMS varactors. It was initially speculated that when the bridge was pulled down to the centre conductor, the bridge would not be able to make a flat contact with the bottom dielectric layer creating an air gap of around 1 µm due to its warped structure. Therefore, to verify this finding, the same varactor model which is D7 with a warped bridge structure based on the measured profile of the bridge was built in CST Microwave Studio. The simulated down-state capacitance value is 256 fF which is comparable to the measured value of the varactor. Therefore,

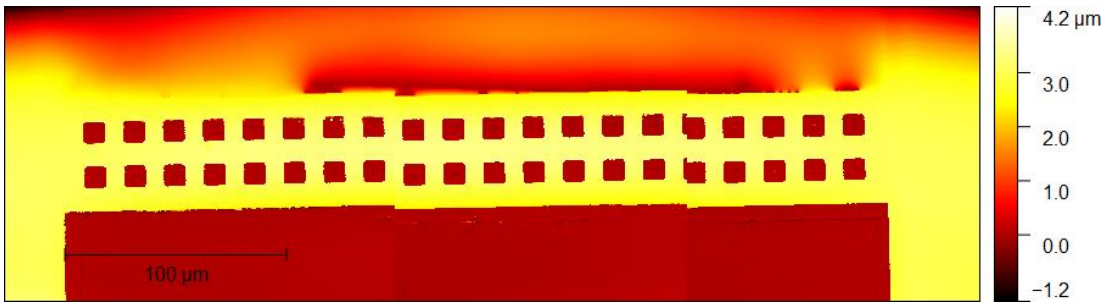


Figure 4.25: Top profile of the standard solid fixed-fixed bridge.

it is concluded that due to the stress in the bridge from the fabrication process, the

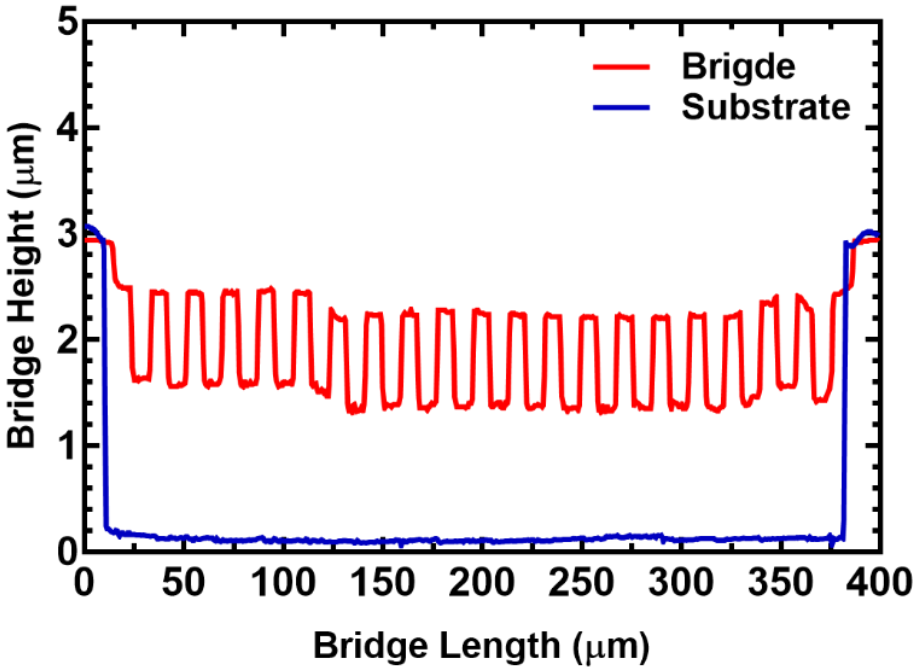


Figure 4.26: Profile of the fixed-fixed bridge along its length.

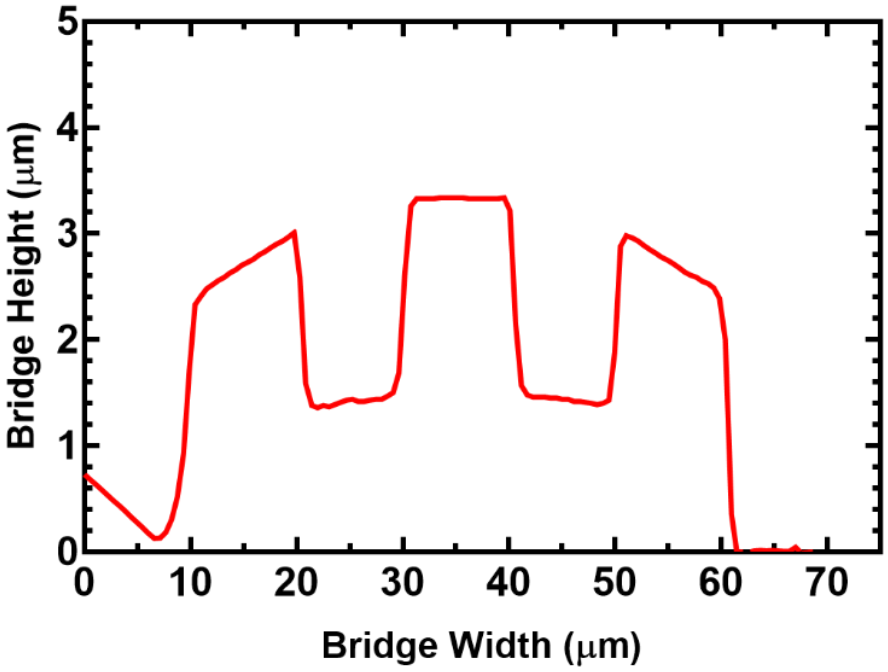


Figure 4.27: Profile of the fixed-fixed bridge along its width.

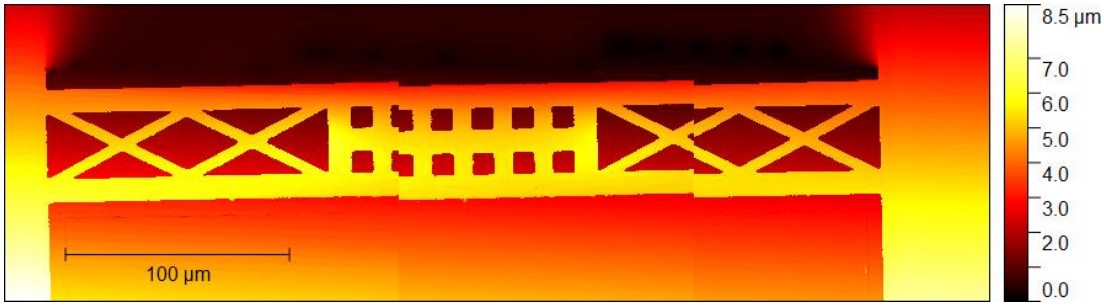


Figure 4.28: Top profile of the truss bridge.

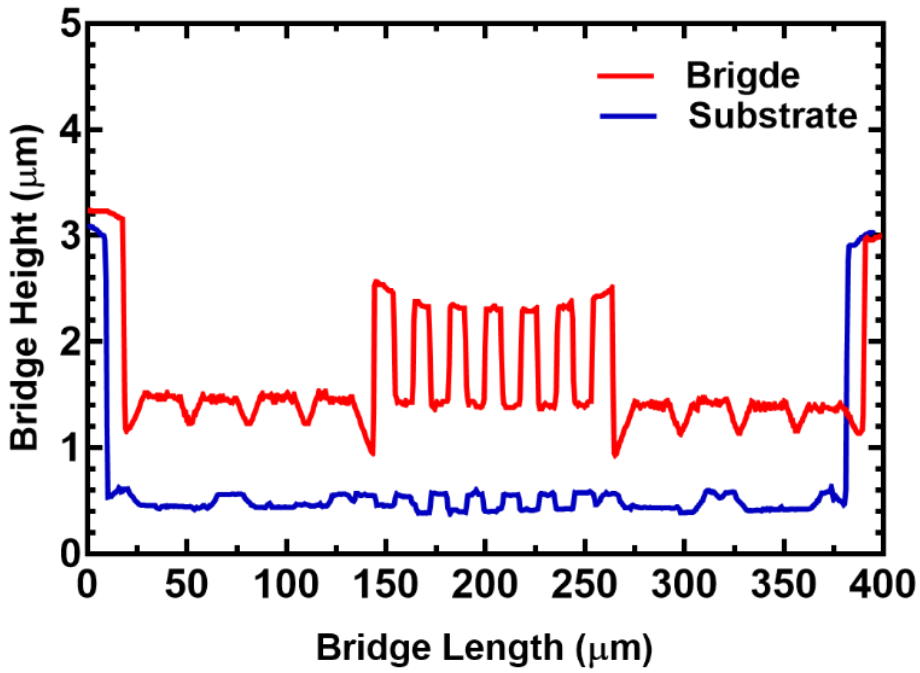


Figure 4.29: Profile of the truss bridge along its length.

bridge in the MEMS varactors warps across its length and width preventing the bridge from making a good contact with the dielectric layer. In the future, optimisations have to be carried out to address the stress issue experienced by the bridge in the varactors.

To compare the performance of the proposed truss bridge and the standard fixed-fixed bridge, their profiles were measured along their widths and lengths. As discussed earlier, the main benefit of using the truss bridge compared to the solid fixed-fixed bridge in the MEMS varactor is the reduction of the actuation voltage of the devices. Figure 4.29 and Figure 4.30 show the truss bridge profiles along its length

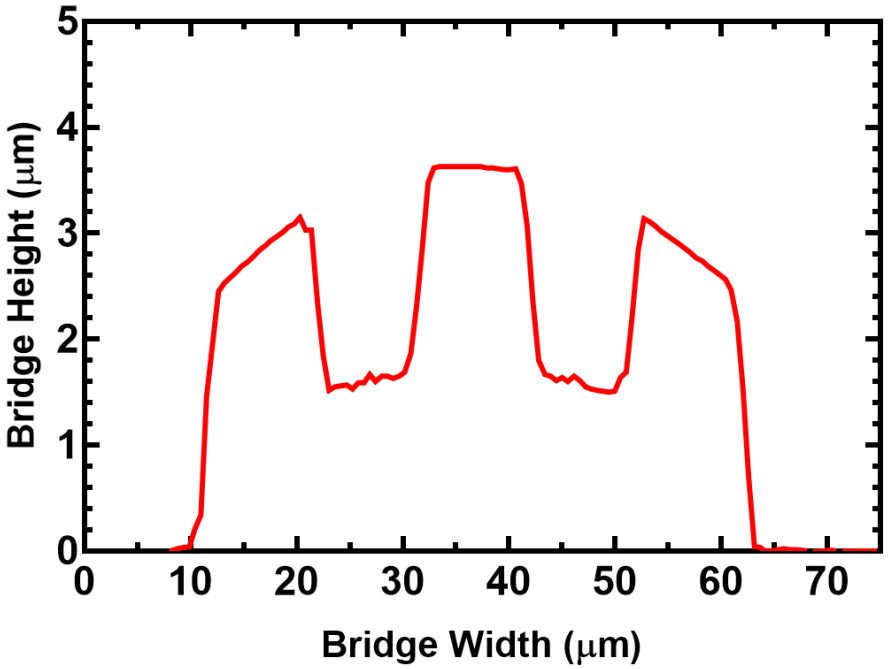


Figure 4.30: Profile of the truss bridge along its width.

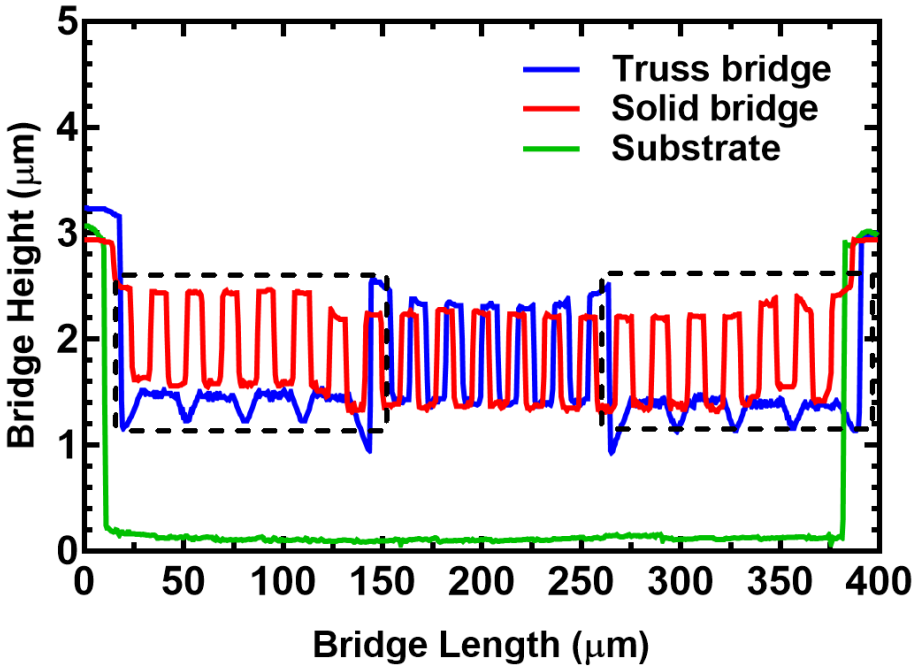


Figure 4.31: Comparison between the truss bridge and the standard fixed-fixed bridge.

and width respectively. Similar profiles can be seen from the truss bridge in

comparison with the solid bridge structure. However, there is one main difference between these bridges where for the truss bridge; the truss structure of the bridge indicated by the dashed black rectangle in Figure 4.31 is not at the same level with the centre of the bridge. The section of the bridge might have been curled downward due to its thin width of 5 µm. However, the whole bridge structure is still suspended above the substrate where it can operate without any degradation in its performance compared to the solid fixed-fixed bridge. Therefore, it can be concluded that the new truss bridge can reduce the actuation voltage of a MEMS varactor compared to standard solid fixed-fixed bridge.

4.7 Summary

This chapter presented the fabrication of single-bridge MEMS varactors with two different bridge types namely fixed-fixed and truss configurations. Furthermore, the dimensions of the bridges mainly the length and width were also varied to investigate their effects on the performances of the MEMS varactors in terms of the actuation voltage. Several modifications have been introduced in the fabrication process including the use of SU-8 as a sacrificial layer and anchor for the MEMS bridges in order to solve the adhesion problem encountered when trying to use oxide as the sacrificial layer in the beginning of the fabrication process. Moreover, it is found that by utilising SU-8 for both sacrificial layer and anchor in the design, the overall fabrication process can be simplified. Subsequently, the objective of implementing a thick SU-8 base layer in the varactor designs by creating a separation layer between the varactors and the silicon substrate has been validated by the increase of the capacitance ratios of the varactors. However, due to the warping of the bridges in the varactors, the down-state capacitance values of the fabricated varactors have been reduced compared to the simulation results. Another benefit of using a thick SU-8 layer in the varactor designs is that the varactors can be fabricated on a low-resistivity silicon substrate without sacrificing the overall performance of the varactors. This can lead to the realisation of low-cost MEMS varactors in the future.

Chapter 5: Design and Simulation of DMTL Phase Shifters

5.1 Introduction

Phase shifter is one of the RF MEMS devices that has attracted significant interest in wireless communication fields. A phase shifter is a two-port network that provides a phase difference between its input and output signals which can be controlled by a control signal. Phase shifters are widely used in modern phased array antenna applications for electronic beam steering. By varying the progressive phase between the antenna elements in an array system, the antennas' main radiation beam can be steered to any direction without having to physically move the antennas. A typical phased array antenna may have several to thousands of elements fed individually by a phase shifter. Therefore, phase shifters with low loss, low cost, low power and lightweight are important in the development of an efficient phased array antenna system. In this chapter, the design and simulation of a DMTL MEMS phase shifter that operates at the lower microwave spectrum intended for microwave head imaging applications is described.

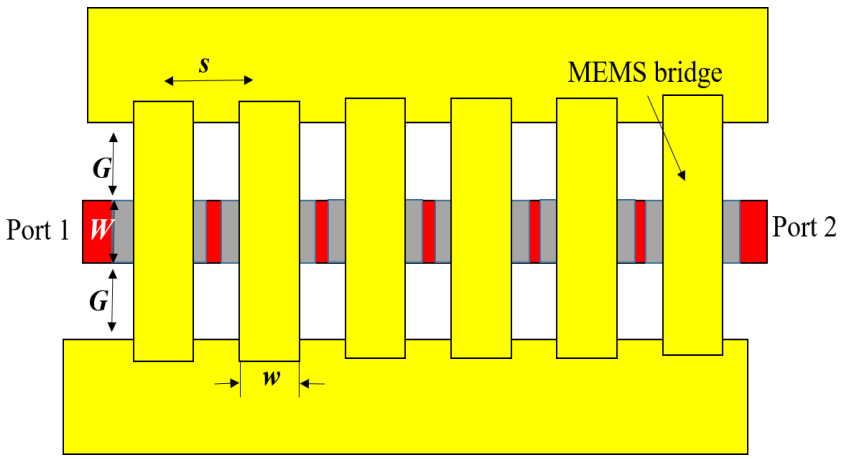


Figure 5.1: Top view of a typical DMTL phase shifter.

5.2 Design Theory

The DMTL phase shifters consist of a transmission line such as CPW or microstrip transmission line and a periodic set of MEMS switched capacitor or varactors positioned along the transmission line. Figure 5.1 shows a typical DMTL phase shifter design implemented using a CPW transmission line where it is periodically loaded with MEMS switches. Bias voltage is used to control the height of the MEMS switches thus changing the capacitance of switches. As a result, the phase velocity of the EM wave travelling inside the phase shifter is slowed down according the change of the capacitance. This leads to a realisation of a true time delay phase shifter.

5.2.1 Transmission Line Theory

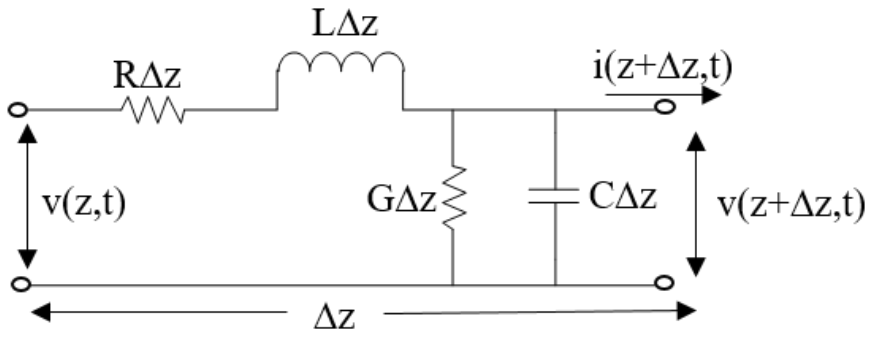


Figure 5.2: Lump element circuit of transmission line [55].

The design of DMTL phase shifters is derived based on the lumped circuit model of a unit cell with length, s of a transmission line loaded with a shunt MEMS switch as illustrated in Figure 5.2 [82]. In general, the lumped circuit of a transmission line per unit length can be represented by four main components which are the resistance due to the transmission line conductivity, R, the inductance of the two conductors, L, the conductance due to the dielectric loss of the substrate, G and the capacitance due to the proximity of the two conductors of the transmission line, C [82].

By using Kirchhoff's law, the closed form equations of the impedance and the propagation velocity of the transmission line in terms of the lumped elements can be obtained as shown in the following equations [82]

$$v(z,t) - R\Delta z i(z,t) - L\Delta z \frac{\partial i(z,t)}{\partial t} - v(z+\Delta z,t) = 0 \qquad (5.1)$$

$$i(z,t) - \mathrm{G}\Delta\mathrm{z}v(\mathrm{z}+\Delta\mathrm{z},\mathrm{t}) - \mathrm{C}\Delta\mathrm{z}\frac{\partial v(z+\Delta\mathrm{z},t)}{\partial t} - i(z+\Delta z,t) = 0 \qquad (5.2)$$

To simplify these equations, each equation is divided with Δz and taking the limit Δz → 0

$$\frac{v(z,t)-v(z+t)}{\Delta\mathrm{z}} = Ri(z,t) + L\frac{\partial i(z,t)}{\partial t}$$

$$\frac{\partial v(z,t)}{\partial z} = Ri(z,t) + L\frac{\partial i(z,t)}{\partial t} \qquad (5.3)$$

$$\frac{i(z,t)-i(z+\Delta z,t)}{\Delta\mathrm{z}} = Gv(z+\Delta z,t) + C\frac{\partial v(z,\Delta zt)}{\partial t}$$

$$\frac{\partial i(z,t)}{\partial z} = Gv(z,t) + C\frac{\partial v(z,t)}{\partial t} \qquad (5.4)$$

In a sinusoidal system,

$$\frac{dV(z)}{dz} = (R+j\omega L)I(z) \qquad (5.5)$$

$$\frac{dI(z)}{dz} = (G+j\omega C)V(z) \qquad (5.6)$$

By taking the forward and reverse travelling waves, the voltage and current in the transmission line can be represented as

$$V(z) = V_o^+ e^{-\gamma z} + V_o^- e^{+\gamma z} \qquad (5.7)$$

$$I(z) = I_o^+ e^{-\gamma z} + I_o^- e^{+\gamma z} \qquad (5.8)$$

By substituting the current in terms V_o using equation (5.5)

$$I(z) = \frac{dV(z)}{dz}\frac{1}{(R+j\omega L)}$$

$$= \frac{\gamma}{R+j\omega L}V_o^+ e^{-\gamma z} \pm e^{+\gamma z} \qquad (5.9)$$

The impedance of the transmission line can be finally defined as

$$Z_o = \frac{V(z)}{I(z)} = \frac{R + j\omega L}{\gamma} = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{5.10}$$

In this thesis, high resistivity silicon is used for the phase shifter design which leads to negligible values for the series resistance, *R* and conductance, *G* in the transmission line. Therefore, the approximate characteristic impedance of the transmission line in the closed form is given by

$$Z_o = \sqrt{\frac{L}{C}} \tag{5.11}$$

And the propagation velocity v_p is

$$v_p = \frac{1}{\sqrt{LC}} \tag{5.12}$$

From these two equations, distributed MEMS transmission lines can be generated by increasing the per unit length capacitance while keeping the per unit length inductance constant. This can be carried out by loading the transmission line by loading the transmission line with a MEMS varactor at a periodic separation, *s*. This results in decrease of the propagation velocity, v_p and characteristic impedance of the transmission line, thus slowing down the wave and providing a true time delay phase shifter.

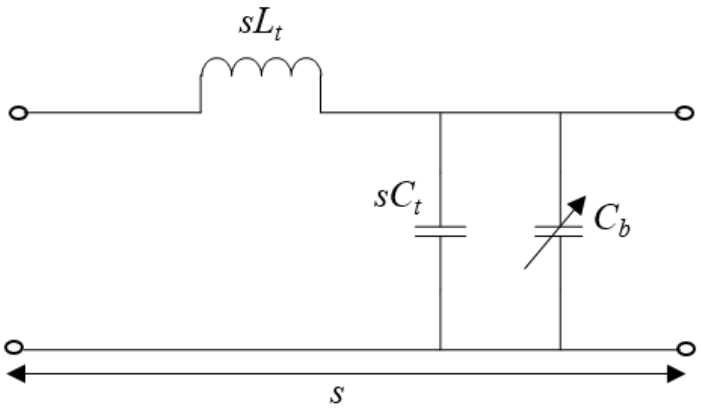


Figure 5.3: The simplified unit cell lumped circuit model of distributed phase shifter.

Figure 5.3 shows that the capacitance of the transmission line can be split into two parts where the capacitance from the MEMS varactor is represented by C_b whereas the capacitance due to the two conductors of the transmission line is given by sC_t. For a loaded transmission line with *s* less than 5% of the design frequency wavelength, the unit cell for the DMTL can be accurately modelled using a single inductor and two capacitors as shown in Figure 5.3. Therefore, for operating frequencies that meet the specification above, the impedance and propagation velocity of the loaded unit cell are given by [1]

$$Z_L = \sqrt{\frac{sL_t}{sC_t + C_b}} \tag{5.13}$$

$$v_p = \frac{s}{sL_t\sqrt{sC_t + C_b}} \tag{5.14}$$

5.2.2 Loading Impedances of DMTL Phase Shifter

As discussed in previous section, DMTL phase shifters comprise a transmission line loaded with a periodic set of varactors or switches to reduce the impedance and propagation velocity of the distributed structure as described in equation (5.11) and (5.12). Therefore, due to the change of the impedance of the transmission line when loaded with varactors, it is important to find the optimal impedance that can be utilised in the DMTL phase shifter design to ensure the impedance matching of the device is maintained throughout its operation. Moreover, considering that the typical length of the transmission line in the phase shifter is comparable to the design operating wavelength, the impedance at the input port of the DMTL will vary depending on the length of the transmission line at the frequency of interest as will be explained below. By placing the DMTL within a 50 Ω system, the input impedance seen at the input of the DMTL is given by

$$Z_{in} = Z_L \frac{1 + \Gamma_{out}e^{-2j\beta l}}{1 - \Gamma_{out}e^{-2j\beta l}} \tag{5.15}$$

where $\Gamma_{out} = (50 - Z_L)/(50 + Z_L)$. By using trig identities, the equation is simplified into

$$Z_{in} = Z_L \frac{50 + jZ_L \, tan(\beta l)}{Z_L + j50 \, tan(\beta l)} \tag{5.16}$$

If βl is $^{\pi}/_{4}$ then Z_{in}= 50 Ω which means that the input impedance of DMTL in the system is passing through 50 Ωs at frequencies where the DMTL is a multiple of a half wavelength. On the other hand, if βl is $^{\pi}/_{4}$, then the quarter wavelength transformer condition occurs resulting in the input impedance of the DMTL to change according to equation (5.17) at frequencies where the DMTL is an odd multiple of a quarter wavelength.

$$Z_{in} = \frac{Z_L^2}{50} \tag{5.17}$$

Therefore, in order to maximize power transfer through the DMTL, the reflected power loss or reflection coefficient due to the mismatch between port 1 and port 2 of DMTL must be minimised. The reflection coefficient of the DMTL can be shown as in equation (5.19) where $RL_{\max}$ is taken in dB

$$\Gamma_{in} = \frac{Z_{in} - 50}{Z_{in} + 50} \tag{5.18}$$

$$\Gamma_{in} = 10^{RL_{max}/20} \tag{5.19}$$

Substituting equation (5.18) into equation (5.17), the loaded impedance of the desired DMTL in terms of maximum desired reflection coefficient is

$$Z_L = 50 \sqrt{\frac{1 \pm \Gamma_{in}}{1 \mp \Gamma_{in}}} \tag{5.20}$$

According to [82], the optimal load impedances of the DMTL at the design frequency when $RL_{\max}$ =-20 dB, -15 dB and -10 dB are given in Table 5.1. The maximum loaded impedance is represented as Z_u during the up-state position and the minimum impedance as Z_d during the down-state position of the MEMS bridges. For our design, the $RL_{\max}$ are chosen to be -15 dB and -17 dB for the 2-bit and 3-bit DMTL design respectively. This is to obtain the maximum phase shift at the design frequency while minimising the reflected power loss at the input of the DMTL. The next step is to find

the optimal impedance for the unloaded transmission line to achieve the highest phase shift per dB loss. This impedance is referred as unloaded impedance, Z_0.

Table 5.1: Optimal loaded impedance for maximum reflection losses at the input of the DMTL [55]

RL_{max}, dB	Z_u	Z_d
-20	55.3	45.2
-17	57	44
-15	59.8	41.8
-10	69.4	36.0

5.2.3 MEMS Bridge Implementation

Generally, there are two methods to implement the MEMS switch in distributed phase shifters. The first method is carried out by using a series DC contact switch as shown in Figure 5.4. On the other hand, a MEMS switch can be arranged in shunt configuration as a varactor. For the first implementation, the combination of the series MEMS switch and a fixed capacitor has minimal loading effect during the up-state position resulting in the highest loaded impedance, Z_u. During the down-state position, the capacitance of the DC contact switch is infinite and therefore the loading capacitance is dominated by the fixed capacitor and the loaded impedance will be at the lowest which is Z_d.

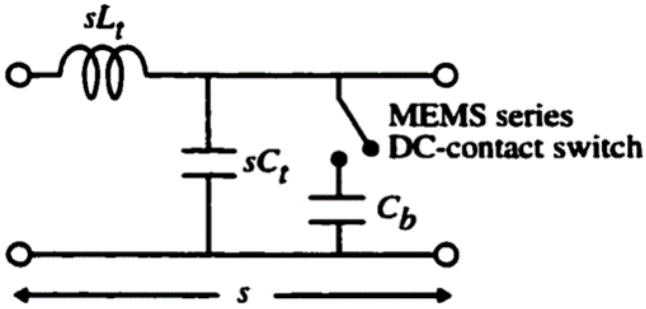


Figure 5.4: The DMTL phase shifter with the MEMS switch in a series [82].

In the second implementation, a MEMS switch acts as a varactor in the distributed transmission line as shown in Figure 5.1. In the up-state position, the capacitance loading in the unloaded line is due to the fields contained between the bottom bridge and signal line. This changes the impedance of the unloaded transmission line to Z_u. When the switch is actuated, the change of height of the bridge causes the loading capacitance to increase. In this case, the impedance and propagation velocity of the DMTL decrease based on the capacitance change. The capacitance of the MEMS switch is based on the bridge design such as width, *w*, thickness, *t*, and suspended height, *h*. The amount of phase shift required can be controlled by specifying the number of MEMS bridges used in the DMTL phase shifter.

5.3 Design Process of DMTL Phase Shifter

In this thesis, a 2-bit and 3-bit digital DMTL phase shifters design have been proposed. These phase shifters operate at the low microwave frequency range of 2 to 4 GHz where this will be the first demonstration of a DMTL phase shifter to operate within this frequency band. Since the phase shifter is required to operate at such low frequency, a long transmission line is needed to accommodate the MEMS bridges in order to obtain the desired phase shift with low loss and maximum power transfer.

1. For DMTL phase shifters designed for 50 Ω systems, the reflection coefficient RL_{max} has been set to <-15 dB and <-17 dB for the 2-bit and 3-bit DMTL phase shifters respectively. This is to make sure that at all four states, the reflection coefficients of the phase shifter will remain below -10 dB especially when the bit segments in the phase shifter are at different states. The loaded line

impedance in up-state position and down-state position, $Z_{u,d}$ can be determined by using equation (5.20).

Table 5.2: Optimal loaded impedance for maximum reflection losses at the input of the DMTL

RL_{max} (dB)	$Z_u\,\Omega$	$Z_d\,\Omega$
-15	60	42
-17	57	44

2. The unloaded Z_0 impedance is chosen to obtain the lowest loss per degree of phase shift. For silicon substrate, it has been reported in [82] that Z_0 in the range of 60 Ω to 70 Ω is the optimal value. Therefore, in our design, 64 Ω and 62 Ω have been optimised for the 2-bit and 3-bit designs by specifying the dimensional layout of the CPW transmission line such as its signal line width (*W*) and gap (*G*).
3. Determine the value of the MEMS bridge capacitance (C_b) and the separation between the MEMS bridges, *s* using equation (5.21) and (5.22) based on the chosen down-state impedance, Z_d.

$$s = \frac{Z_d c}{\pi f_b Z_0 \sqrt{\varepsilon_{eff}}}\ meter \tag{5.21}$$

$$f_b = \frac{2}{2\pi\sqrt{sL_t(sC_t + C_b)}} \tag{5.22}$$

The ε_{eff} value depends on the type of the transmission line used in the DMTL phase shifter. For silicon substrate, ε_{eff} is 6.4 while for Quartz, the value is around 2.3-2.4. The Bragg frequency, f_B is selected to be higher than the design frequency since above this frequency point, the line impedance becomes zero and thus there will be no power transfer between the two ports of the phase shifter [82]. In our design, the $f_B s$ has been chosen approximately 10 and 8.5 times the design frequency at 2.45 GHz for the 2-bit and 3-bit designs which is significantly larger than the typical distributed phase shifters designed for higher frequency bands where their $f_B s$ are around 2 to 3 times the centre operating frequency, f_0 [46], [54]. However, for S-band frequency range,

setting the Bragg frequency to 2 to 3f_0 will contribute to a very large loading capacitance causing the MEMS switches in the phase shifter to act as a reflective switch instead.

4. As such, it has been found that the Bragg frequency of 10f_0 and 8.5f_0 will ensure reasonable capacitance values for the MEMS switch in the up-state (C_{bu}) and down-state (C_{bd}) positions for our phase shifter design as calculated in equation (5.22) and (5.23) at the expense of an increase in the number of MEMS bridges [1], [82]

$$C_{bu} = \frac{(Z_0^2 - Z_u^2)Z_d}{Z_0^2 Z_u^2 \pi f_b} \tag{5.22}$$

$$C_{bd} = \frac{(Z_0^2 - Z_d^2)}{Z_0^2 Z_d \pi f_b} \tag{5.23}$$

The capacitance ratio of the MEMS switch can then be expressed as [1]

$$C_r = \frac{C_{bd}}{C_{bu}} = \frac{Z_u^z}{Z_d^2}\frac{(Z_0^2 - Z_d^2)}{(Z_0^2 - Z_u^2)} \tag{5.24}$$

5. Based on equation (5.14), (5.21), (5.22), and (5.23), the propagation velocity on the DMTL with the MEMS bridges in up-state and down-state positions can also be derived as

$$v_L = \frac{c\ Z_L}{Z_0\sqrt{\varepsilon_{eff}}} \tag{5.25}$$

where Z_L is the loaded impedance of the DMTL phase shifter during the up-state and down-state positions. In the proposed phase shifters, this equation can be used since the operating frequencies of the phase shifters are well below the specified Bragg frequency.

6. The phase shift of this slow wave structure can then be calculated as [1]

$$\Delta\phi = \omega\sqrt{sLsC}\left(\sqrt{1 + \frac{C_{bu}}{sC}} - \sqrt{1 + \frac{C_{bd}}{sC}}\right)$$

$$= \frac{\omega Z_0 \sqrt{\varepsilon_{eff}}}{c} \left(\frac{1}{Z_u} - \frac{1}{Z_d}\right) \quad rad/meter \tag{5.26}$$

where Z_0, $\varepsilon_{r,eff}$, and c are the unloaded impedance of the transmission line, effective permittivity of the substrate and speed of light in vacuum respectively. Based on this equation, the phase shift is determined by the impedance change of the DMTL phase shifter which is also related to the reflection coefficient of the phase shifter. To produce the maximum phase shift of 270^0 and 315^0 for the 2-bit and 3-bit phase shifters, the required total lengths are 76.45 mm and 134.79 mm respectively. The number of segments or MEMS bridges can be determined by dividing the calculated required phase shifts with the separation, *s* obtained from equation (5.21).

7. Using equation (5.22) and (5.23), the MEMS bridge capacitance can be designed using the parallel plate capacitor equation [1]

$$C_{pp} = \frac{\varepsilon_0 A}{g_0 + \frac{t_d}{\varepsilon_r}} \tag{5.27}$$

where $\varepsilon_o = 8.854 \times 10^{-12}$ is the permittivity of free space, *A* is the contact area between the bridge and the centre conductor of the CPW transmission line, g_0 is the initial gap, t_d is the dielectric thickness, and ε_r is the relative dielectric constant of the dielectric.

8. The MIM DC blocking capacitor value can be calculated using equation (5.28) to result in reactance value of 1.1 Ω at the lowest operating frequency which is 2 GHz. The use of blocking capacitors is vital as it serves to block the applied DC voltage between the bit segments of the phase shifter while allowing the RF signal to pass from the input port to the output port.

$$X_c(\Omega) = \frac{1}{2\pi f C} \tag{5.28}$$

9. Finally, since the proposed 2-bit and 3-bit phase shifters require overall transmission line length of 76.45 mm and 134.79 mm respectively to operate at 2.45 GHz, the lateral lengths of the phase shifters have been optimised by meandering the CPW transmission line as shown in Figure 5.5 using 60^0 mitered technique which can be calculated using equation (5.29) below [83]

$$Miter = \frac{x}{d} \times 100\% \tag{5.29}$$

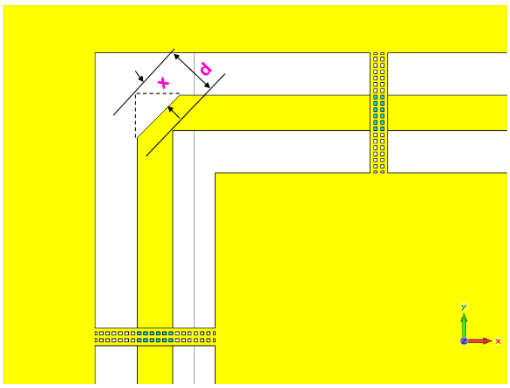


Figure 5.5: Mitered CPW transmission line structure at the right angle bends.

5.3.1 MEMS Bridge Design of the DMTL Phase Shifters

A doubly clamped bridge or fixed-fixed bridge type is used in both designs of the DMTL phases shifters [1]. The dimension of the MEMS bridge was designed based on the dimension of the CPW transmission line used in the phase shifters. The length of the MEMS bridge is the distance between the ground of the CPW transmission line. Therefore, the total lengths of the bridges for the 2-bit and 3-bit DMTL phase shifters are 372 µm and 344 µm respectively. The width of the bridges is set to 50 µm to obtain the required up-state and down-state capacitances as calculated using equation (5.27). In order to understand the mechanical behaviour of the proposed bridge, the spring constant of the bridge was first derived. In general, the total spring constant for the fixed-fixed bridge can be divided into two main components. The first part is due to the stiffness of the bridge which is attributed to its material properties such as Young's

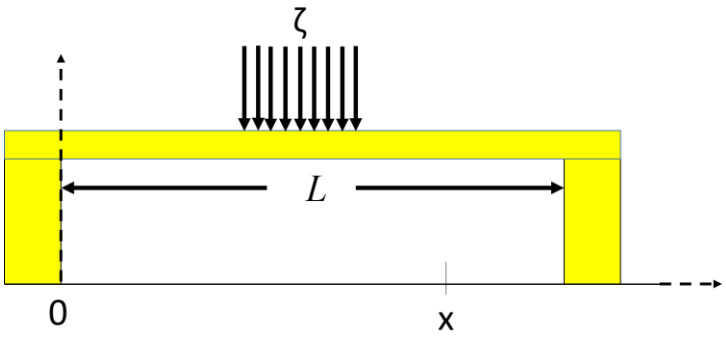


Figure 5.6: Fixed – fixed beam with the force $P = \zeta 2(x - L/2)$ evenly distributed about the center of the bridge [1].

Modulus, *E* and the moment of inertia, *I* while the other part is due to the residual stress, σ developed within the bridge during and after fabrication process. In the proposed phase shifters, the bridge will be pulled down at the centre conductor when actuated. In this case, the applied force will be evenly distributed over the centre portion of the bridge. Thus, the general spring constant due to the material characteristics or the stiffness of the bridge when the force is distributed on the centre can be calculated as [1]

$$k_1 = 32Ew\left(\frac{t}{L}\right)^3 \frac{1}{8\left(x/L\right)^3 - 20\left(x/L\right)^2 + 14\left(x/L\right) - 1} \tag{5.30}$$

where $x = L/2$ for a load at the centre of the bridge while *w* and *t* is the width and thickness of the bridge respectively. On the other hand, the spring constant component due to the residual stress within the bridge is given by

$$k_2 = 8\sigma\,(1 - v)w\left(\frac{t}{l}\right)\left(\frac{3}{5}\right) \tag{5.31}$$

where *v* is the Poisson's ratio for the aluminium membrane. Therefore the total spring constant is

$$k_t = k_1 + k_2 \tag{5.32}$$

$$k_t = 32Ew\left(\frac{t}{L}\right)^3 \frac{1}{8\left(x/L\right)^3 - 20\left(x/L\right)^2 + 14\left(x/L\right) - 1} + 8\sigma\,(1 - v)w\left(\frac{t}{l}\right)\left(\frac{3}{5}\right) \tag{5.33}$$

From the spring constant of the bridge, the pull-in voltage can be calculated using equation (5.34) [1]

$$V_p = \sqrt{\frac{8kg_0^3}{27\varepsilon_0 A}} \tag{5.34}$$

where $A = Ww$, *W* is width of pull down electrode, *w* is the width of the bridge, g_0 is the air gap and ε_0 is 8.854×10^{-12}. Pull-in voltage is the voltage required to pull down the bridge while holding voltage is the minimum voltage required to hold the bridge in down-state position before the bridge is restored to its initial position. Material parameters of the bridge are indicated in Table 5.3 [1].

Table 5.3: Material parameters of the bridge

Parameter	Value
Young's Modulus of aluminium, E	69 GPa
Poisson's ratio of aluminium, *v*	0.32
Density of aluminium, ρ	2700 kg/m^3

The estimated pull-in voltage and spring constant of the MEMS bridge for the 2-bit DMTL phase shifter are 8V and 1.966 N/m while for the 3-bit design, the values are 12.36 V and 1.46 N/m respectively. To verify the performance of the MEMS bridge in terms of its pull-in voltage, mechanical simulation has been carried out using CoventorWare and will be presented in Section 5.5.2 and Section 5.6.3.

5.4 Simulation of CPW transmission line for the DMTL Phase Shifter

In this section, electromagnetic simulation of the CPW transmission line for the proposed DMTL phase shifters has been carried out using CST Microwave Studio software to obtain the RF characteristics of the device. In the phase shifter design, the transmission line of the device has been meandered in order to optimise the size of the phase shifter. Hence, a comparison between a straight and meandered transmission lines was first performed to evaluate their performances in terms of reflection coefficient and transmission loss.

Coplanar wave guide transmission line has been widely adopted in DMTL phase shifters due to its many advantages including low dispersion, low radiation, ease of shunt series connection and integration with other RF components. For the 2-bit and 3-bit DMTL phase shifters, the overall lengths of the straight distributed phase shifter structures at 2.45 GHz calculated using equation (5.26) are 76.45 mm and 134.79 mm respectively. In view of the long lateral dimension of the straight CPW transmission line structures, further optimisation has been carried out by meandering the transmission line to reduce the length of the phase shifter at the expense of increased width. However, the introduction of bends such as right angle bend on the CPW transmission line might degrade the overall performance of the transmission line if not

properly designed due to the introduction of slot line mode. The slot line mode can be excited when the electromagnetic waves between two slots of a CPW transmission line bend travelled at different distant and thus causing radiation losses. To suppress the slot line mode, 60º mitered technique has been utilised in this design [83]

An initial simulation of a meandered CPW transmission line for 3-bit DMTL phase shifter design which has the same length as the straight configuration calculated in Section 5.3 was carried as shown in Figure 5.7. The reflection coefficient and transmission loss performances were compared between the two structures to investigate any performance degradation particularly due to the possible introduction of slot mode excitation caused by the right angle bends along the meandered structure as reported in the literature [84].

The reflection and transmission coefficients of the straight and meandered transmission lines are depicted in Figure 5.8 and Figure 5.9 respectively. It can be seen from Figure 5.8 that the impedance matching of the meandered structure is similar to the straight configuration up to 9 GHz. The characteristic impedance of the meandered transmission line can then be calculated from the simulated reflection coefficient based on equation (5.39)[1]

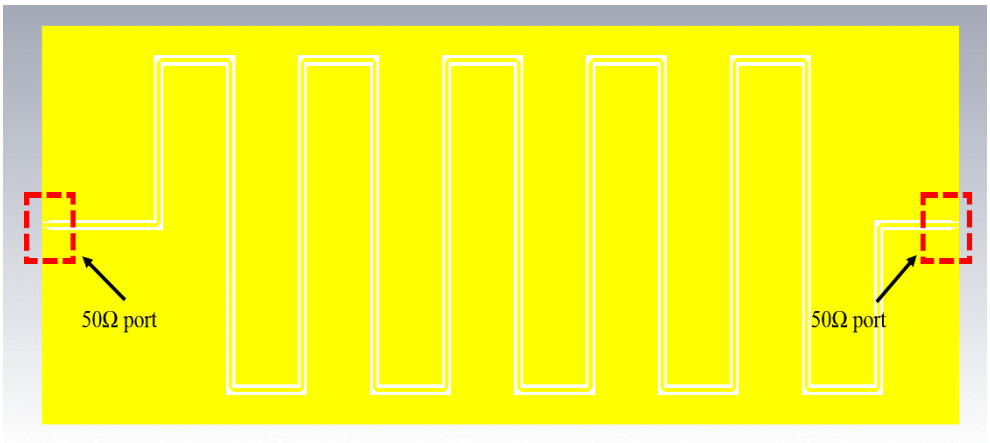


Figure 5.7: Meandered transmission line structure.

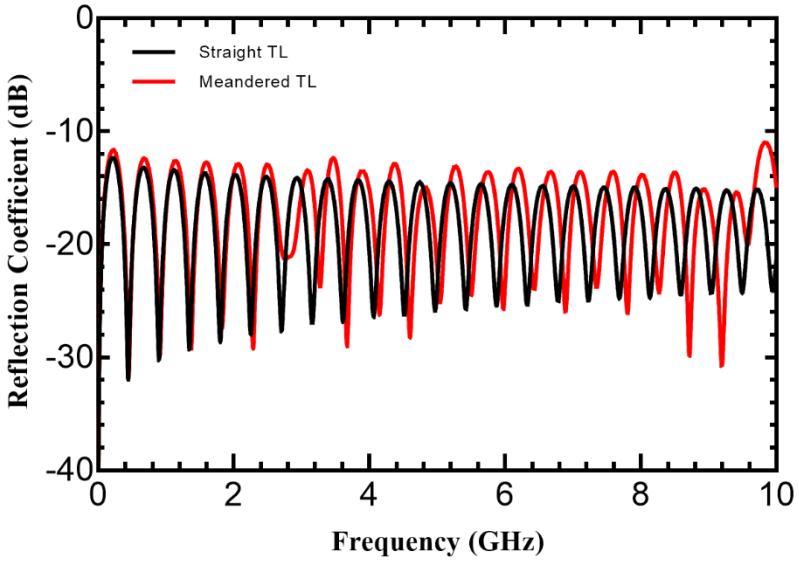


Figure 5.8: Reflection coefficients of straight transmission line and meandered transmission lines.

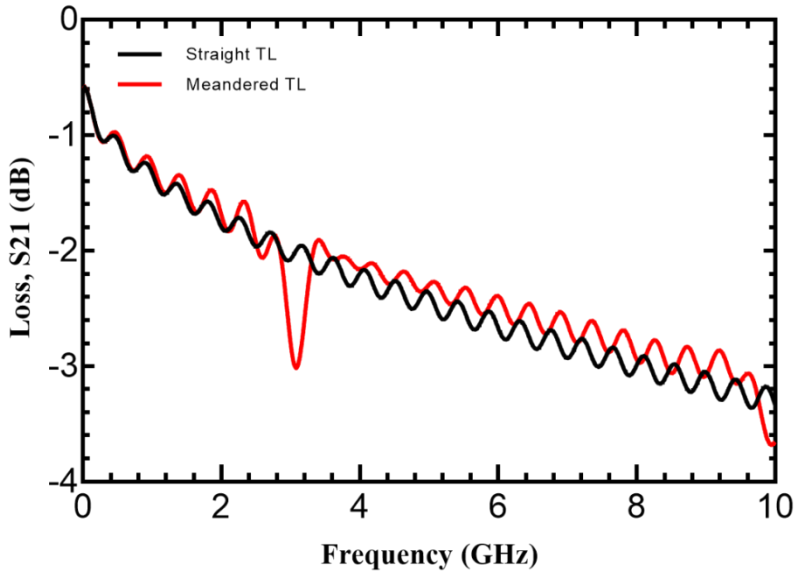
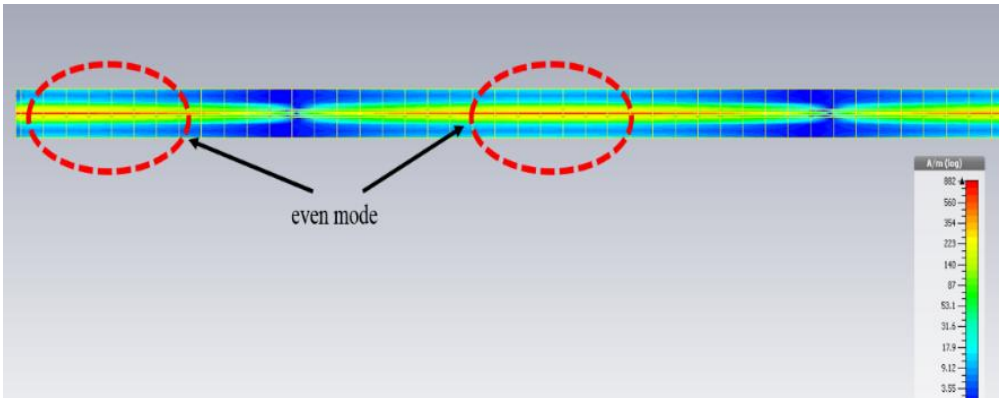


Figure 5.9: Transmission losses of the straight and meandered transmission lines.

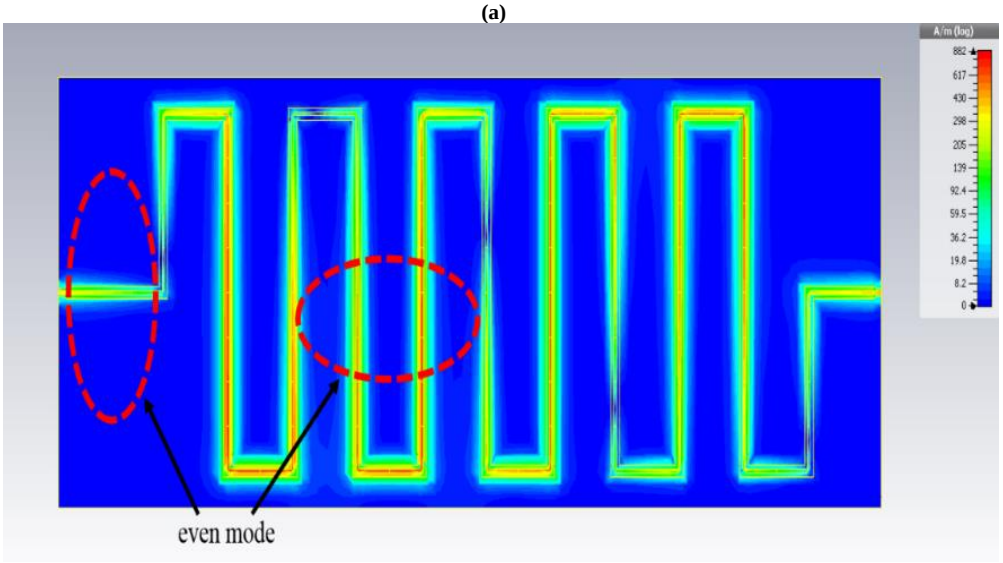
$$Z_{in} = \frac{{Z_0}^2}{50} \tag{5.39}$$

where Z_{in} is the input impedance of the phase shifter seen from the 50 Ω feedline.

The peaks observed in the reflection coefficients correspond to the frequencies where the transmission line is a multiple of a quarter-wavelength long. By taking the peak in the reflection coefficient at around 2 GHz, the characteristic impedance of the



(a)



(b)

Figure 5.10: a) Even mode of straight transmission line (b) Even mode of meandered transmission line at 2 GHz.

meandered transmission line increases slightly from 62 Ω obtained in the straight structure to 63.24 Ω. Although there is a slight increase in the characteristic impedance of the proposed meandered line, the intended phase shifts for the proposed 3-bit phase shifter are intact as will be discussed in the next subsection. For the transmission coefficient performance, similar characteristic is observed between the two configurations although a sudden dip in the transmission loss can be seen at 3.12 GHz. It is to be noted that the dip is no longer observed once the meandered transmission line is loaded with MEMS switches as will be shown in the next section. The surface current distributions of the straight and meandered transmission lines were simulated at 2 GHz as illustrated in Figure 5.10. The current distribution of the meandered transmission line does not show any excitation of slot mode since it can be clearly

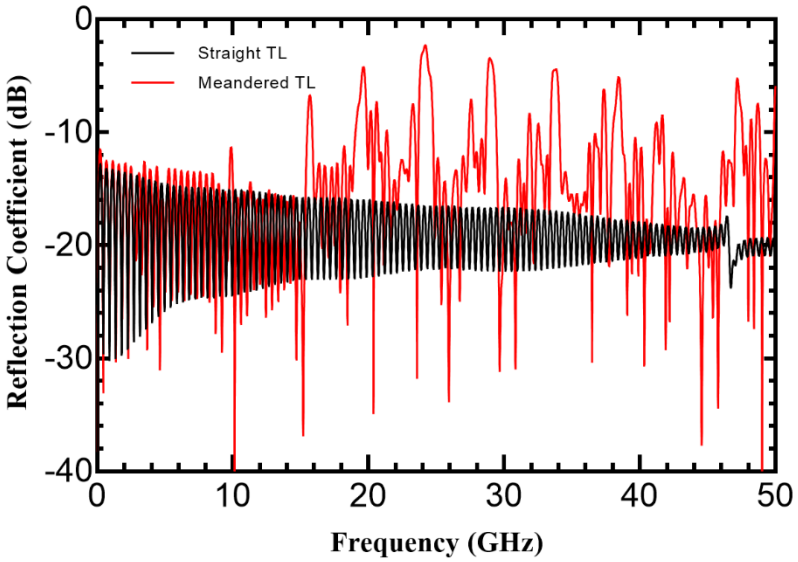


Figure 5.11: Reflection coefficients of the transmission lines up to 50GHz.

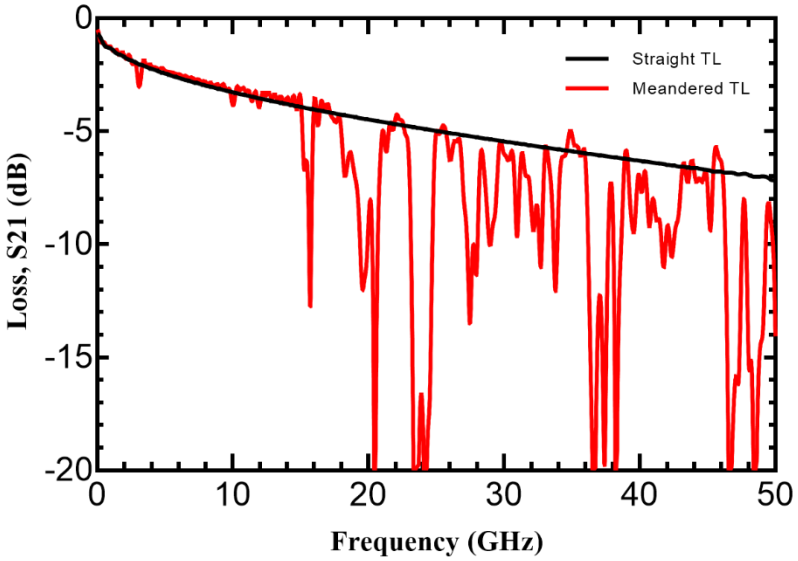
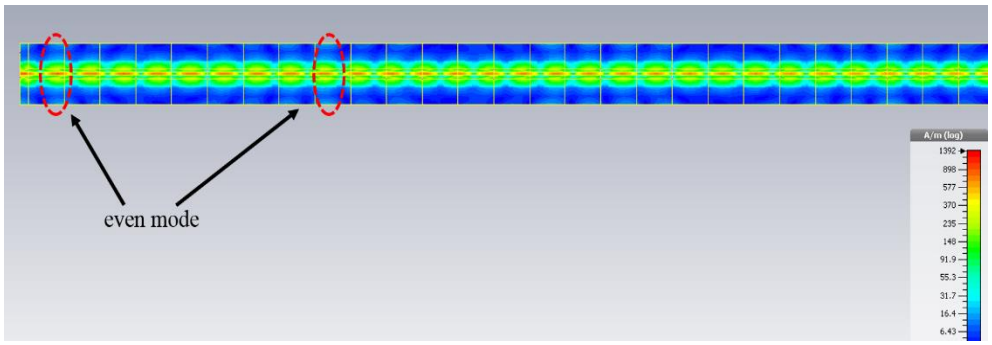


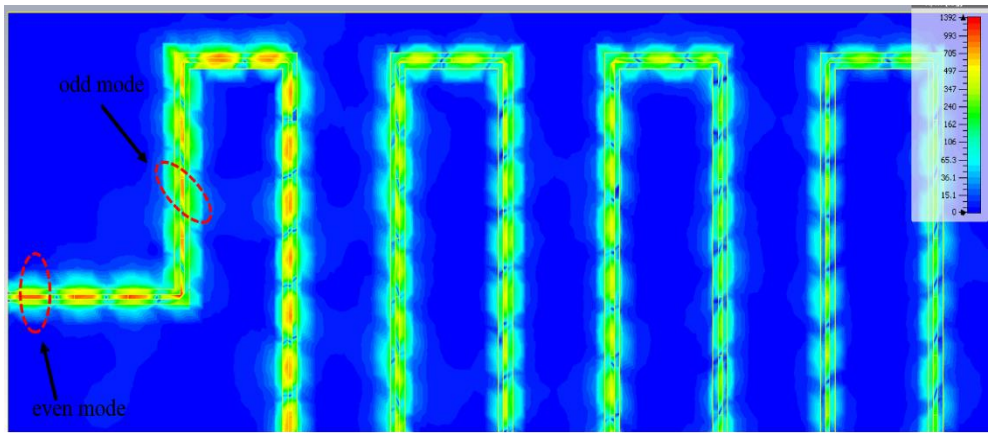
Figure 5.12: Transmission losses of the transmission lines up to 50GHz.

observed that at low frequency range (2 to 4 GHz), the guided wavelength is much larger than the overall length of the right angle bend making the different in the distance between the two slots negligible. This result is confirmed by the finding in [84] that the performance degradation for both the impedance matching and transmission loss was only observed above 10 GHz for the uncompensated right angle bend structure.

To support this claim, the meandered transmission line was simulated up to 50 GHz. The reflection coefficient and transmission loss of the transmission line are shown in Figure 5.11 and Figure 5.12 respectively. It is observed that the performance of the meandered transmission line starts to deviate significantly from the reference straight configuration above 10 GHz with noticeable resonances due to slot-line mode excitation. The current surface distribution at 50 GHz in Figure 5.13 shows significant twist of the surface current pattern confirming the introduction of slot-line mode for the meandered structure compared to the straight line configuration. Nevertheless, for operation at S-band, the mitering technique applied to the proposed meandered phase shifter design is sufficient to reduce the effect of the slot-line mode. Moreover, the resonance responses which cause significant performance degradation on the meandered structure is experienced only at frequency above 10 GHz which is not the intended operating frequency range of the proposed phase shifter design.



(a)



(b)

Figure 5.13 (a) Even mode of straight transmission line at 50GHz. (b) Odd mode of meander transmission line at 50GHz.

5.5 Simulation of the 2-Bit DMTL phase shifter

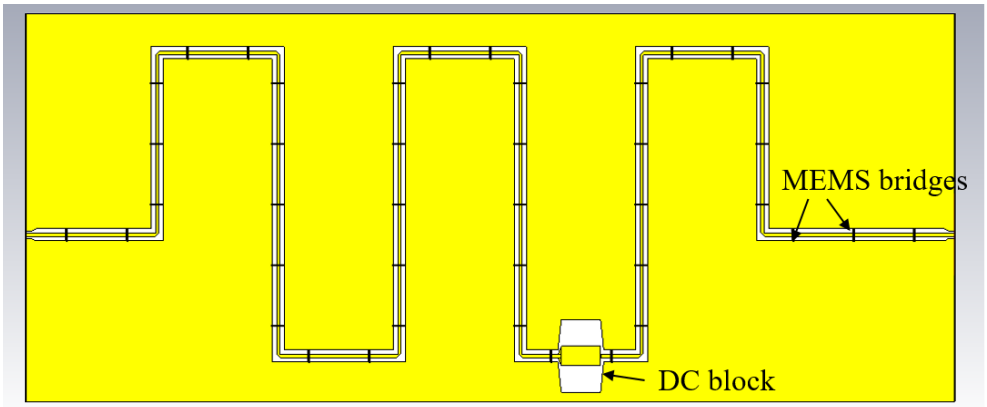


Figure 5.14: Top view of the proposed DMTL phase shifter design.

The structure of the proposed 2-bit DMTL phase shifter was built in CST Microwave Studio as shown in Figure 5.14. The key design parameters of the design are given in Table 5.4. The 2-bit DMTL phase shifter produces four phase shifts which are 0^0, 90^0, 180^0, and 270^0. The MEMS bridge was designed to have a capacitance ratio of 8, which corresponds to the up-state and down-state capacitance values of 45.38 fF and 363.014 fF respectively. The f_B is 24.5 GHz which is ten times greater than the operating frequency and the resulting distance between the adjacent varactors is 1850 μm.

A total of 41 MEMS switches are used in this design. The bit-1 and bit-2 segments of the phase shifter have 14 and 27 MEMS bridges to produce 90^0 and 180^0 phase shift respectively. The combination of both segments will produce the maximum phase shift of 270^0. The bits are actuated by applying DC voltages at the input and output ports of the phase shifter. The spring constant and pull in voltage for the bridge are calculated using equation (5.35) and (5.38) and found to be 1.966 N/m and 8 V respectively. The MIM capacitor with silicon dioxide as a dielectric layer is implemented between the bits as a DC blocking capacitor which is to isolate the two bits. However, to allow the RF signal to pass at the operating frequency band, the MIM capacitor was designed to have an impedance value, X_c of less than 1.1 Ω calculated using equation (5.32). The DC blocking capacitor used in this design has a capacitance value of 72 pF where the reactance is 0.9 Ω.

Table 5.4: Design Parameter of 2-bit DMTL phase shifter

Parameters	**Values**
Z_o	65 Ω
CPW (*G/W/G*)	136/100/136 µm
Thickness of CPW	2 µm
Z_u	60 Ω
Z_d	42 Ω
Distance between bridge, *s*	1850 µm
Bridge dimension ($w \times L$)	50 × 372 µm
Thickness of bridge	1 µm
Air gap, g_o	1.5 µm
Bragg frequency, f_{Bragg}	10 f_o
Up-state capacitance, C_{bu}	45.38 fF
Down-state capacitance, C_{bd}	363.014 fF
Capacitance ratio, C_r	8
90^0 bit	14 unit cells
180^0 bit	27 unit cells
DC blocking capacitor	72 pF

5.5.1 RF Analysis of the 2-bit digital DMTL Phase Shifter

All four states of the 2-bit DMTL phase shifter have been simulated as illustrated in Figure 5.15. It can be seen that the reflection coefficients for all the states are < -10 dB across the frequency 2 GHz to 4 GHz. This has been realised by carefully choosing the loaded impedances to be 60 Ω (up-state) and 42 Ω (down-state) which yield a maximum of -15 dB per bit. This helps maintaining the impedance matching performance below -10 dB when the two bits are cascaded. The average simulated transmission loss is -1.68 dB at 2.45 GHz as shown in Figure 5.16. Figure 5.17 shows the simulated phase shift for the 4 states. It can be seen that the phase shift increases linearly with frequency as expected for a true time delay type phase shifter. The simulated maximum phase shift is 270^0 at 2.45 GHz with an associated transmission loss of -1.8 dB. When all the bridges are on up-state position, the phase shift produced is 0^o.

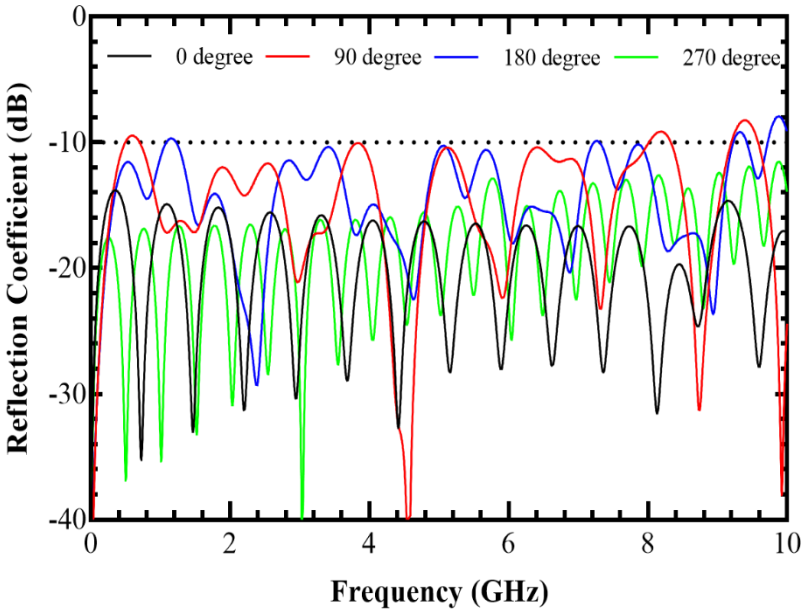


Figure 5.15: Simulated reflection coefficients of the 2-bit DMTL phase shifter.

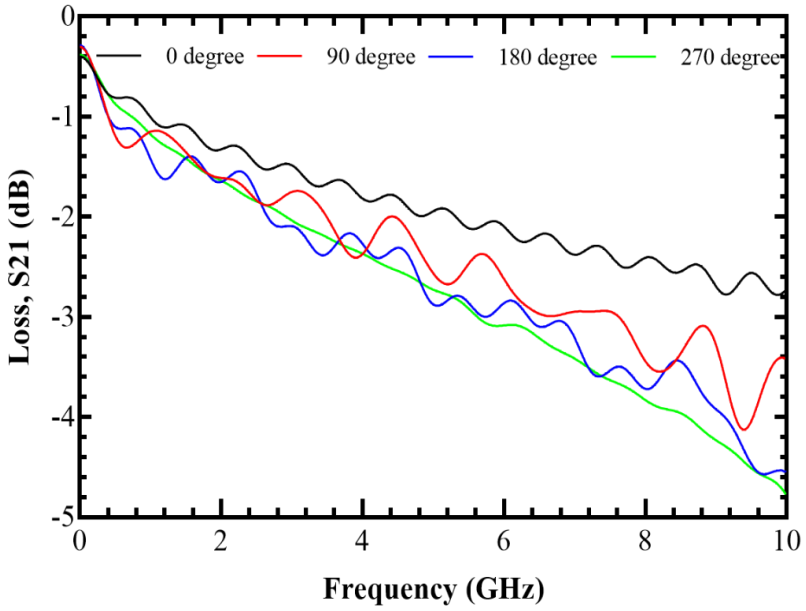


Figure 5.16: Simulated transmission losses of the 2-bit DMTL phase shifter.

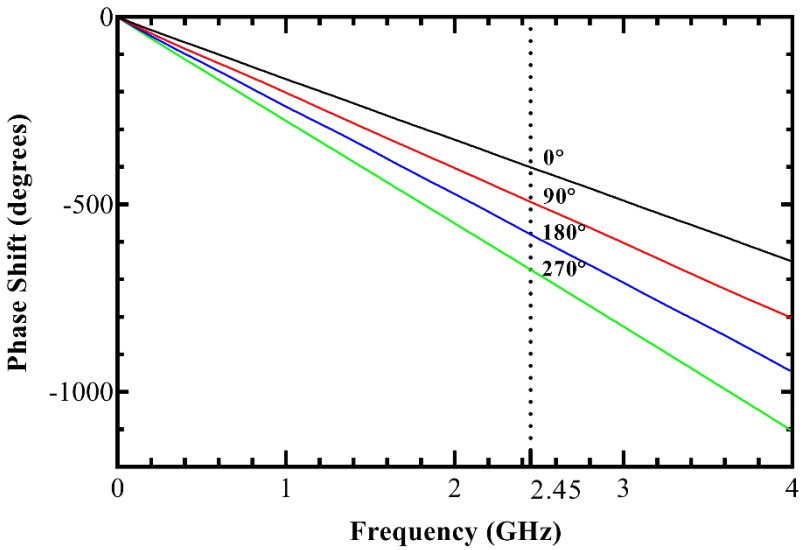


Figure 5.17: Simulated phase shifts of the 2-bit DMTL phase shifter.

5.5.2 Simulation and Analysis of Mechanical Behaviour of the MEMS Bridge for the 2-bit Phase Shifter

The mechanical simulation of the bridge for the proposed 2-bit DMTL phase shifter was carried out using CoventorWare. Figure 5.18 illustrates the deformation of the bridge in the down-state position which shows that the bottom of the bridge completely touches the top surface of the dielectric layer. The simulated pull-in voltage for the doubly clamped bridge is 9.68 V compared to 8 V using equation (5.38). The simulated lift-off voltage or holding voltage is 7 V at which state the bridge is restored to its original position. The pull−in voltage increases to 33.2 V and 45.703 V for in-plane stresses of 50 MPa and 100 MPa respectively. This stress represents the residual stress typically experienced by a MEMS bridge after fabrication process. Figure 5.19 demonstrates the relationship between the pull-in and lift-off phenomena.

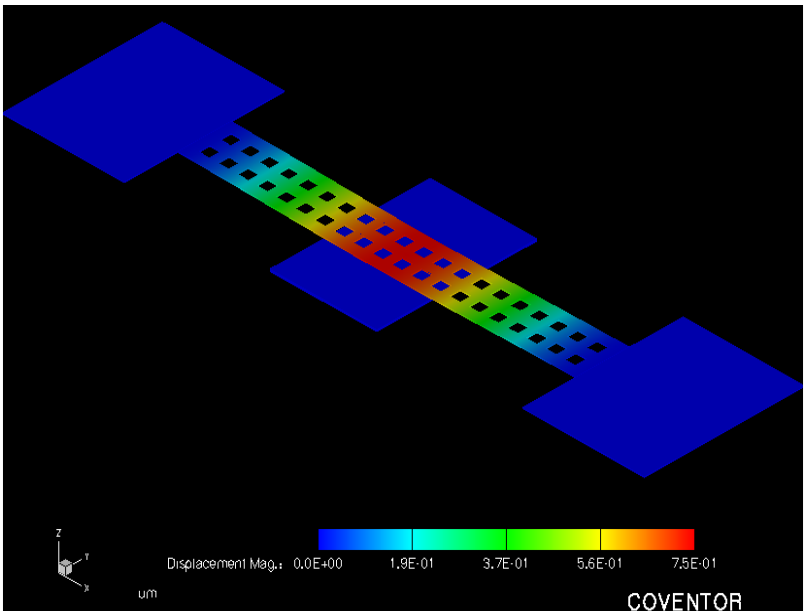


Figure 5.18: Deformation of the bridge during electrostatic actuation.

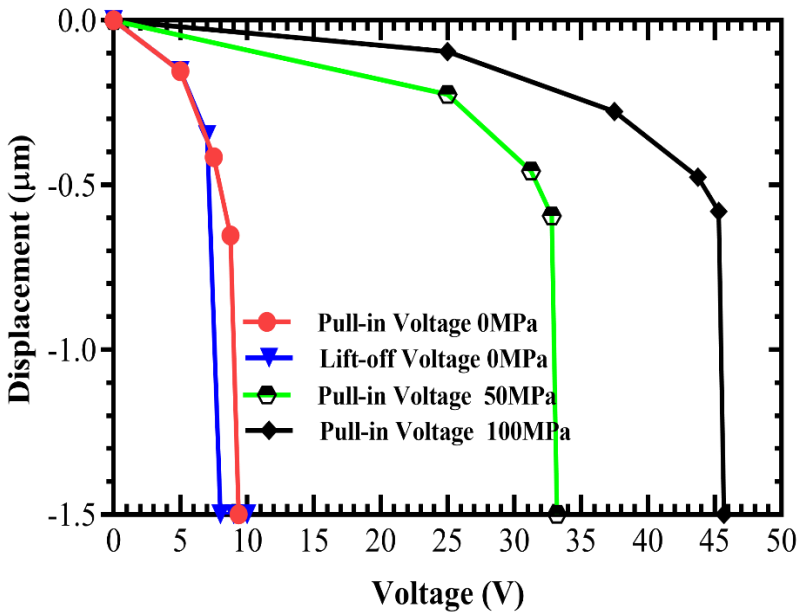


Figure 5.19: Simulated pull-in and lift-off voltage of the 372µm long bridge.

5.6 Simulation of the 3-bit DMTL Phase Shifter

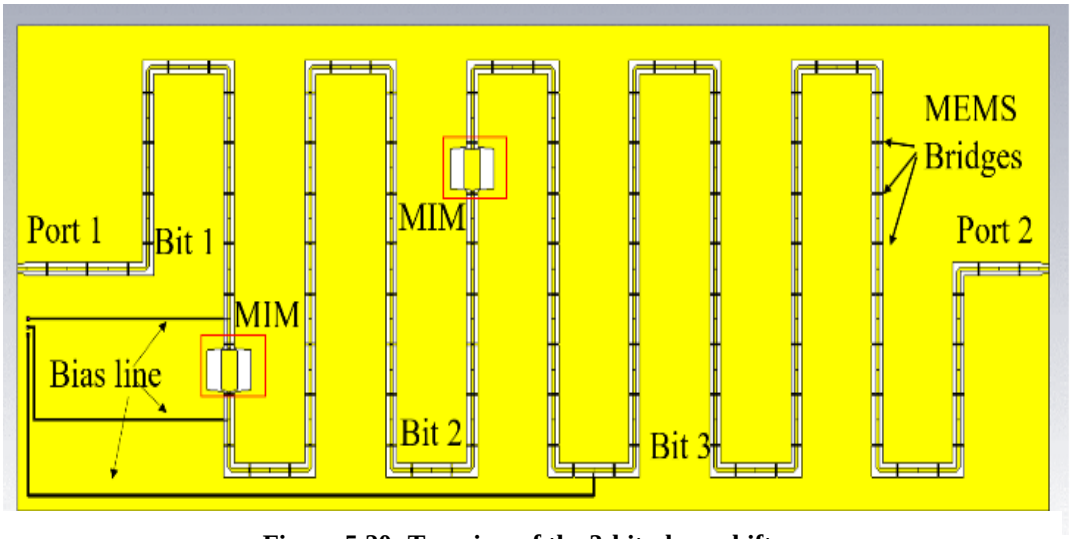


Figure 5.20: Top view of the 3-bit phase shifter.

To increase the number of differential phase shifts that can be selected from the DMTL phase shifter, a 3-bit DMTL phase shifter has been developed. Based on the optimised meandered CPW transmission line design presented in the Section 5.4, the 3-bit distributed phase shifter is designed on a 525 μm thick high resistivity silicon (ρ = 10 kΩ·cm) substrate similar to the previous 2-bit design to reduce the loss due to the substrate. Figure 5.20 shows the full structure of the 3-bit DMTL phase shifter which consists of three bit segments which correspond to 45^0, 90^0, and 180^0. The loaded impedances of the transmission line are chosen to be 57 Ω (up-state position) and 44 Ω (down-state position) for a -17 dB of reflection coefficient per bit. This is to ensure that the reflection coefficients for all eight states are better than -10 dB across the operating band. The f_B is 20.8 GHz which is 8.5 times greater than the operating centre frequency at 2.45 GHz. The separation distance between two adjacent varactors is 1278 μm. The total number of the MEMS varactors in the phase shifter is 105 and the combinations of all bits can produce eight phase shifts which are 0^0, 45^0, 90^0, 135^0, 180^0, 225^0, 270^0 and 315^0 at 2.45 GHz. For this 3-bit design, high resistivity bias lines are required to actuate the MEMS varactors based on the required phase shifts where they are routed under the centre conductor. To separate the bit segments, two MIM capacitors are used as DC blocking capacitors as shown in Figure 5.20. The key design

parameters of the 3-bit phase shifter are summarised in Table 5.5. Simulations of the device have been conducted for RF and mechanical analyses.

5.6.1 RF Analysis of the 3-bit Digital DMTL Phase Shifter

In RF analysis, the performance of the device was characterised in terms of impedance matching, phase shifter loss and the amount of phase shift. The reflection coefficient shows the mount of power reflected back to the source due to the impedance mismatch at the input port of the DMTL phase shifter. The simulated reflection coefficients for all 8 states are shown in Figure 5.21. It can be seen that the reflection coefficients for the eight states are < -10 dB across 2 GHz to 4 GHz frequency range which mean that only 10% of the power delivered to the device are reflected back to the source. This could only be realised by choosing loaded impedances of 57 Ω (up-state) and 44 Ω (down-state) which yields initial impedance matching value of -17 dB per bit. This helps maintaining the impedance matching below -10 dB when the three bits (45^0, 90^0, 180^0) are cascaded together especially for the 90^0 and 225^0 states where the RF signal has to undergo two impedance changes along the transmission line. The simulated average phase shifter loss is -2.94 dB at 2.45 GHz as shown in Figure 5.22. The simulated phase shifts are shown in Figure 5.23.

Table 5.5: Design parameter of 3-bit DMTL phase shifter

Parameters	Values
Z_o	62 Ω
CPW (G/S/G)	122/100/122 µm
Thickness of CPW	2 µm
Z_u	57 Ω
Z_d	44 Ω
Distance between bridge, s	1278 µm
Bridge dimension (w x l)	50 × 344 µm
Thickness of bridge	1 µm
Air gap	1.5 µm
Bragg freq, f_{Bragg}	8.5 f_o
Up-state capacitance, C_{bu}	33.72 fF
Down-state capacitance, C_{bd}	144.31 fF
Capacitance ratio, C_r	5.235
45^0 bit	15 unit cells
90^0 bit	30 unit cells
180^0 bit	60 unit cells
DC blocking capacitor	72 pF

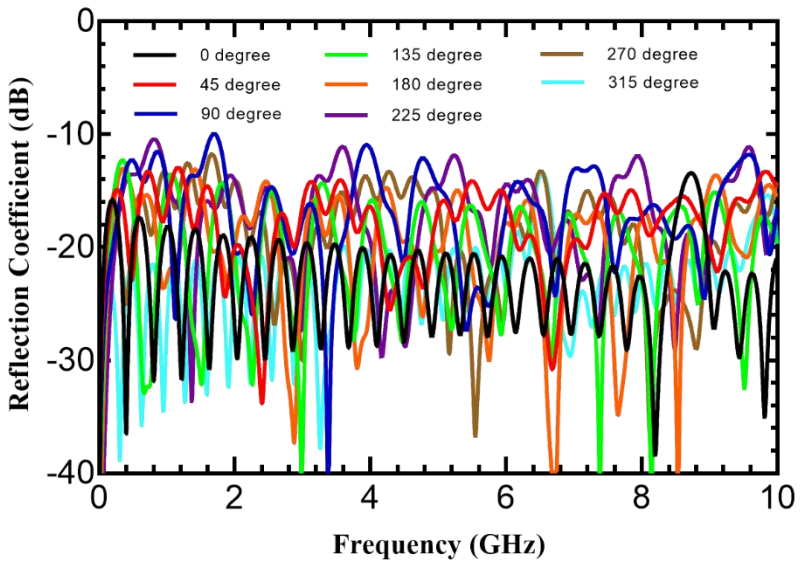


Figure 5.21: Simulated reflection coefficients of the 3-bit DMTL phase shifter.

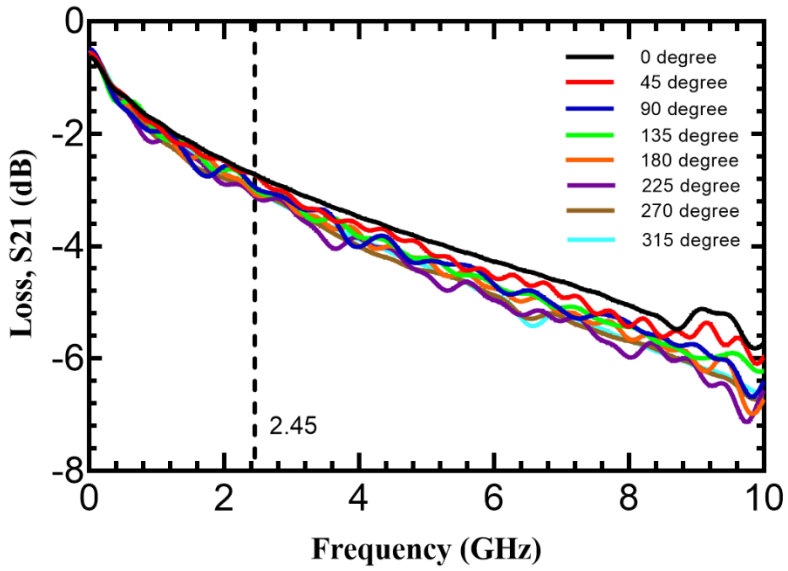


Figure 5.22: Simulated phase shifter losses of the 3-bit DMTL phase shifter at 2.45 GHz.

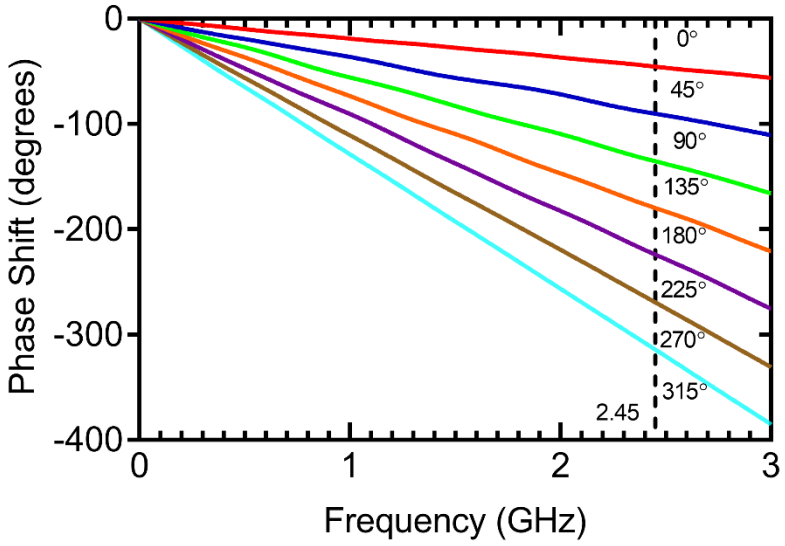


Figure 5.23: Simulated phase shifts of the 3-bit phase shifter at 2.45 GHz.

5.6.2 Simulation and Analysis of Mechanical Behaviour of the Bridge for the 3-bit DMTL Phase Shifter

In order to verify the performance of the bridge design, mechanical simulation has been carried out using CoventorWare. The pull-in and holding voltages of the 344 µm fixed-fixed bridge for the 3-bit DMTL phase shifter were simulated. Moreover, the effect of in-plane residual stress on the pull-in voltage was also investigated. Figure 5.24 shows the deformation of the bridge during actuation.

The results show that the pull–in voltage for the bridge is 17.18 V which is in good agreement with the analytical value calculated using equation (5.34) and (5.38). The simulated holding voltage is 15 V which can be seen in Figure 5.25. The in-plane stress which is typically experienced by a free standing structure was varied in the bridge model from 0 MPa to 100 MPa to investigate its effects on the pull-in voltage of the bridge. The results show that the pull-in voltage increases from 17.18 V to 50.31 V and 68.43 V respectively [85].

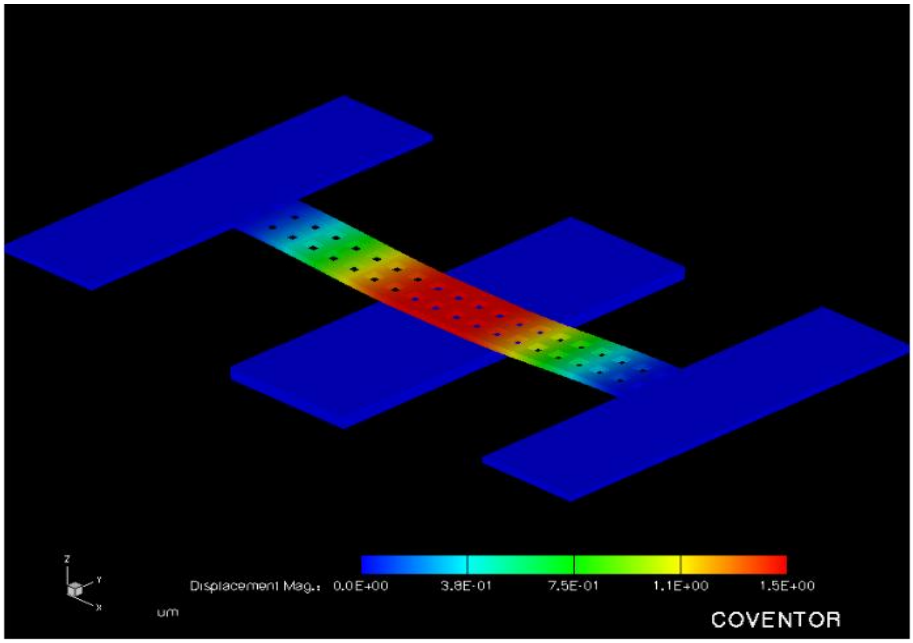


Figure 5.24: Deformation of the bridge during electrostatic actuation.

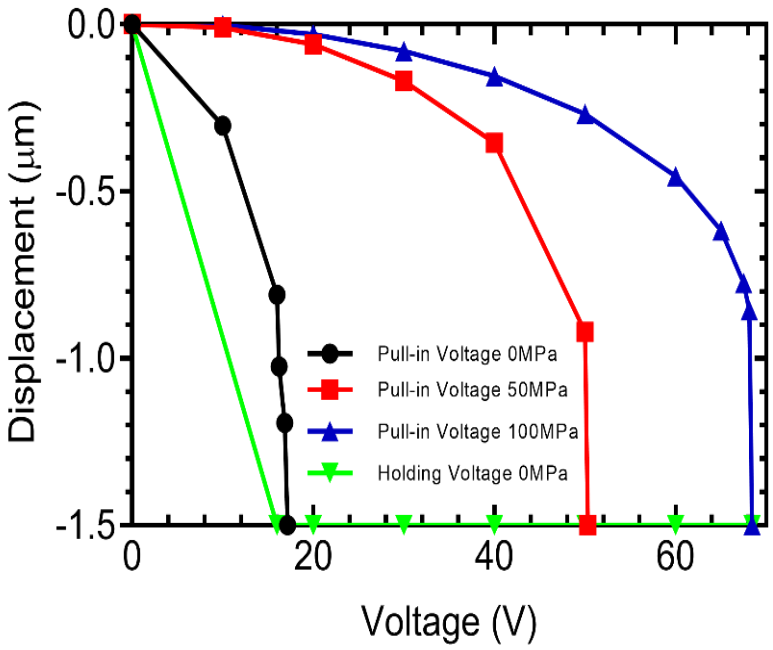


Figure 5.25: Simulated Pull-in and holding voltages.

5.6.3 Mechanical Resonant Frequency and Switching Time

The switching time of the fixed-fixed bridge for the phase shifter can be determined by the frequency response of the bridge. By using Laplace transformation, the frequency response is found to be [1]

$$\frac{X(j\omega)}{F(j\omega)} = \frac{1}{k}\left(\frac{1}{1-\left({}^{\omega}/_{\omega_0}\right)^2 + j\omega/(Q\omega_0)}\right) \tag{5.40}$$

where $\omega_0 = \sqrt{k/m}$ is the resonant frequency, k is the spring constant, m is the bridge mass and Q is the quality factor of the bridge. For an aluminium fixed-fixed bridge, the quality factor can be calculated using equation (19) below [1]

$$Q_{ff} = \frac{\sqrt{E\rho t^2}}{\mu_e\left(\frac{wl}{2}\right)^2} g_0^3 \tag{5.41}$$

where ρ is the density of the aluminium and μ is the coefficient of viscosity of air given by

$$\mu_e = \frac{\mu}{1 + 9.638K_n^{1.159}} \tag{5.42}$$

where K_n is the Knudsen number. For quasi-ideal gases such as air or nitrogen, the coefficient viscosity, μ is given by

$$\mu = 1.2566 \times 10^{-6}\sqrt{T}\left(1 + \frac{\beta}{T}\right)^{-1} \quad kg/m.s \tag{5.43}$$

At standard temperature pressure (STP, T is 273.15 K, and P is 101 kPa) the viscosity, μ of the ideal gases is 1.5829×10^{-5} where β is 110.33 K. It can be seen from equation (5.42) the viscosity of the gases is influenced by Knudsen number. A high Knudsen number shows that the gas in the gap between the bridge and the pull down electrode experiences very few collisions while a small Knudsen number indicates that the gas is viscous. The Knudsen number can be calculated using equation (5.44) [1]

$$K_n = \frac{\lambda}{g} \tag{5.44}$$

where λ is the distance covered by a molecule in a gas between successive collisions called mean free path of the gas and g is gap height. The mean free path is given by

$$\lambda = \frac{1}{\sqrt{2}\pi N\sigma^2} \tag{5.45}$$

where σ is the diameter of the gas. Using equation (5.41) to (5.45) the calculated quality factor of the bridge designed for the phase shifter is 2.4. The resonance frequency of the bridge was then obtained using CoventorWare. Since the calculated Q_{ff} of the bridge is 2.4, equation (5.46) can be used to estimate the switching speed of the bridge [1]

$$t_{s\approx}3.67\frac{V_p}{V_s\omega_0} \tag{5.46}$$

where V_s is the applied voltage. Based on equation (5.46), it is evident that the switching time depends on the applied voltage. The larger the applied voltage, the stronger the electrostatic force created between the bridge and the pull-down electrode causing faster switching time. However, according to experiment done by Barker [1], [86], the applied voltage, V_s should be set to 1.3-1.4V_p to result in fast switching time

at a reasonable voltage. For the 344 μm length bridge, the simulated first order of resonance frequency is 130.4 KHz and therefore the switching time of the bridge for the phase shifter calculated using equation (24) is 1.16 μs where the V_s is set to $1.4V_s$.

5.6.4 Proposed Fabrication Process for 3-bit DMTL Phase Shifter

An overview of the proposed fabrication process of the DMTL phase shifter will be described in this section. The fabrication process of the full structure employs the standard surface micromachining technique which requires five main fabrication stages. The overall process flow is shown in details in Figure 5.26. The DMTL phase shifter is fabricated on a 4-inch high resistivity (10k Ω·cm) silicon wafer. A fresh silicon wafer is first cleaned in a barrel asher in order to remove all possible traces of contaminants and particles before the subsequent process. Then, a 0.5 μm thick silicon nitride (SI_3N_4) is deposited on the wafer to serve as an insulator using PECVD technique. Next, 0.5 μm of tantalum nitride is sputtered on the wafer and then patterned by means of optical lithography followed by wet etching to form a bias line (MASK 1). Then, the CPW transmission line and bottom metal of the MIM capacitors can be realised (MASK 2). By using a negative photoresist with optimised exposure and developing time, an undercut profile of the photoresist is obtained. This step is crucial to ensure that the undesired metal trace will be able to be removed during the lift-off process. Afterwards, a blanket deposition of 2 μm aluminium is performed resulting in an aluminium layer being coated on the top of the photoresist and the exposed substrate area. During the lift-off process, solutions such as Microposit Remover 1165 and ACT is used to lift off the resist along with the unwanted aluminium while the desired aluminium layer is patterned on the exposed substrate. This stripping process can be speeded up by agitating the wafer in a sonic bath with a temperature of 60 °C. Next, a 1 μm silicon dioxide (SiO_2) is deposited as a capacitive contact for the MEMS bridge and the dielectric for the MIM capacitors using PECVD process. The SiO_2 layer is then patterned using lithography (MASK 3) before it is etched using reactive ion etching (RIE) technique. Then, the top metal of MIM capacitor is realized using lift off process (MASK 4) with thickness of 300 nm. After that, epoxy polymer based negative-tone photoresist, SU-8 is employed to act as anchors for the MEMS bridges

and also as the sacrificial layer in a single process. The SU-8 is spun on the wafer, soft baked and crosslinked by exposing it under a UV light. To further crosslinked the polymer, a post exposure bake is carried out at 65 °C for 1 minute and followed by 95 °C for 3 minutes. Subsequently, the SU-8 layer is hard baked at 200 °C for 30 minutes. The temperature is ramped in the hotplate to avoid sudden change in temperature which could lead to internal cracks and stresses in the SU-8 layer [16]. To obtain a flat beam structure, a chemical mechanical planarisation process might be needed to flatten the surface of the sacrificial layer before the subsequent deposition of the beams' pattern. The next process is the third lift-off process for the remaining structure of the phase shifter which includes the beams and ground of the CPW transmission line (MASK 5). A negative photo resist such as AZ nLOF 2035 is used to create the lift-off profile. A layer of 1 µm thick aluminium is blanket deposited using e-beam deposition technique before stripping it using solution such as 1165 where it is put in the sonic bath for 60 °C in order to remove the photoresist and the unwanted aluminium trace. In the final stage of the fabrication process, the SU-8 is removed using oxygen plasma in the barrel asher to release the bridges. During this process, oxygen plasma will etch the exposed SU-8 layer at the same rate in all directions (isotropic etching). The large ground pattern on the SU-8 will protect the underlying SU-8 layer which will serve as anchors for the beam structures. The holes on the bridge will allow the oxygen plasma to etch the sacrificial layer under the bridge more easily in order to expedite the release process.

SU-8 has been chosen for the fabrication process since it can serve as anchors for the MEMS bridges in the phase shifter as well as sacrificial layer. In addition, SU-8 material produces a very planar surface after spin-coating and hard bake process. It can also be used to form a high aspect ratio structure [10]. Moreover, it has high chemical resistance with the materials used in the fabrication steps. The crosslinked SU-8 can only be etched by oxygen plasma for dry etching or piranha solution for wet etching.

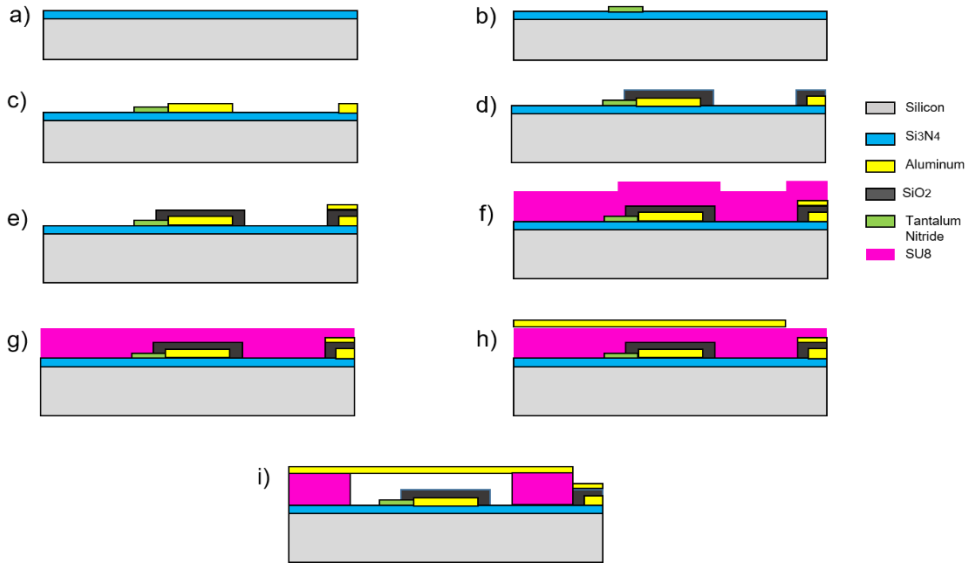


Figure 5.26: Proposed fabrication process flow that consists of the formation of a) passivation layer, b) bias line, c) centre conductor of CPW TL and lower electrode of MIM capacitors, d) dielectric layer for MEMS varactors and MIM capacitors, e) top electrode of MIM capacitors, f) SU-8 anchor and sacrificial layer, g) planarisation of SU-8, h) MEMS bridges and ground of CPW TL and i) suspended bridge.

5.7 Summary

This chapter described in details the design and simulation of the proposed 2-bit and 3-bit DMTL phase shifters for operation at frequency range of 2 GHz to 4 GHz. The development and optimisation of the phase shifters were carried out using an electromagnetic simulator, CST Microwave Studio. For the analysis of the mechanical behaviour of the MEMS bridges of the phase shifters, CoventorWare software was used. 41 and 105 bridges were required for the 2-bit and 3-bit designs respectively. The overall lengths of the CPW transmission lines integrated in the devices are 76.45 mm and 134.79 mm. To facilitate the realisation of a compact DMTL phase shifter, a meandered CPW transmission line was employed in the design. The overall size of the phase shifters are 28.35 mm × 11.62 mm and 30 mm × 10 mm for the 2-bit and 3-bit DMTL phase shifters design respectively.

Chapter 6: Fabrication and Measurement of DMTL Phase Shifters

6.1 Introduction

This chapter presents the fabrication process for the proposed 2-bit DMTL phase shifter presented in Chapter 5. Similar fabrication process used for the construction of the MEMS varactor described in Chapter 4 is adopted for the realisation of the DMTL phase shifter. Several variations of the phase shifter design have been fabricated to verify their functionality. These variations differ in terms of the number of varactors used in the devices. To comply with the specification and capability of the fabrication tools available in the SMC cleanroom and to reduce the complexity of the process, few modifications were made to the phase shifter design proposed in Chapter 5. In this fabrication process, the thickness of the centre conductor of the CPW transmission line of the phase shifter has been reduced to 300 nm instead of 2 μm. It is expected that the final transmission loss of the fabricated phase shifter to be lower than the simulated results. Therefore, to provide better estimation of the phase shifter loss if thicker metal was used in the design, several variations of CPW transmission line with the same characteristic impedance of the fabricated 2-bit phase shifter were fabricated and measured. Furthermore, to reduce the transmission loss of the CWP transmission line due to the formation of surface conduction layer between the passivation layer and the high resistivity silicon, 500nm thick polysilicon layer was introduced between the silicon substrate and the passivation layer. In addition, another method to reduce the loss due to the surface conduction problem has also been carried out by etching the passivation layer at the gap of the CPW transmission line. A comparison has been made between these two methods where it has been found that the use of polysilicon layer provides better performance that the etching technique. The fabricated phase shifter is evaluated in terms of its impedance matching, phase shift and transmission loss. Characterisation of the bridge utilised in the phase shifter has been conducted to investigate the effect of stress to its final structure and the phase shift obtained.

6.2 Mask Design of the 2-bit DMTL Phase Shifter

The fabricated 2-bit phase shifter requires 4 mask layers. To reduce the number of mask layers required, the DC block capacitor utilised in the phase shifter design has been replaced with a surface mount capacitor with a nominal value of 100 pF. The use of the surface mount capacitor will remove the need for the optimisation of the metal-insulator-metal (MIM) capacitor if built using the microfabrication process and therefore can expedite the fabrication time of the device. Nevertheless, the final structure of the phase shifter can be incorporated with the MIM capacitor once the process has been optimised in the future. The fabrication process of the phase shifter is illustrated in Figure 6.4 in Section 6.3. It is noted that similar fabrication process is adopted from the previous process conducted to build the MEMS varactors. Table 6.1 shows the summary of the main structures of the varactor, materials used and masks required for the realisation of the 2-bit DMTL phase shifter.

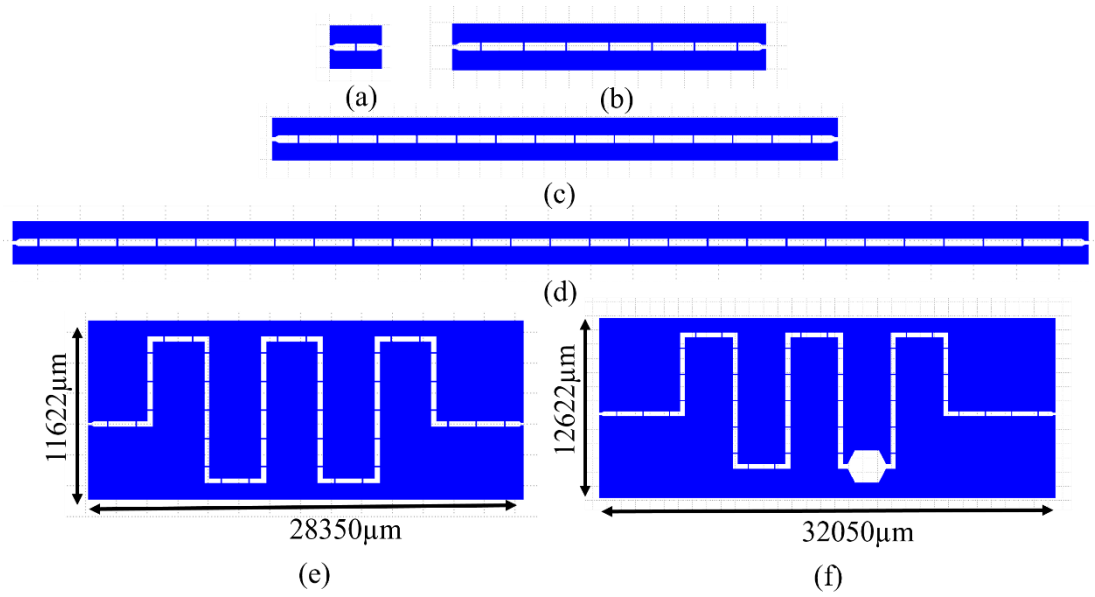


Figure 6.1: Mask design of DMTL phase shifter with (a) single bridge, (b) 7 bridges, (c) 14 bridges, (d) 21 bridges, (e) 41 bridges in meandered transmission line and (f) 2-bit DMTL phase shifter with DC blocking capacitor.

Besides the full 2-bit phase shifter structure, several variations of the DMTL phase shifters with different number of bridges were also designed in the mask representing the individual bit of the device. The bridge structure used in the MEMS phase shifter

is the fixed-fixed bridge type described in Chapter 5. Based on the previous measurement results for the MEMS varactor, the expected pull-in voltage of the bridge will be in the range of 35 V to 40 V. The final wafer layout of the phase shifter on a 4-inch wafer is shown in Figure 6.3. The entire design consists of 3 process layers as shown in Figure 6.2 to Figure 6.3. The first layer defines the centre conductor of the CPW transmission line utilised in the phase shifter. The dielectric layer made of silicon dioxide (SiO_2) is formed using the second layer. The third layer is used to pattern the bridge and ground of the CPW transmission line.

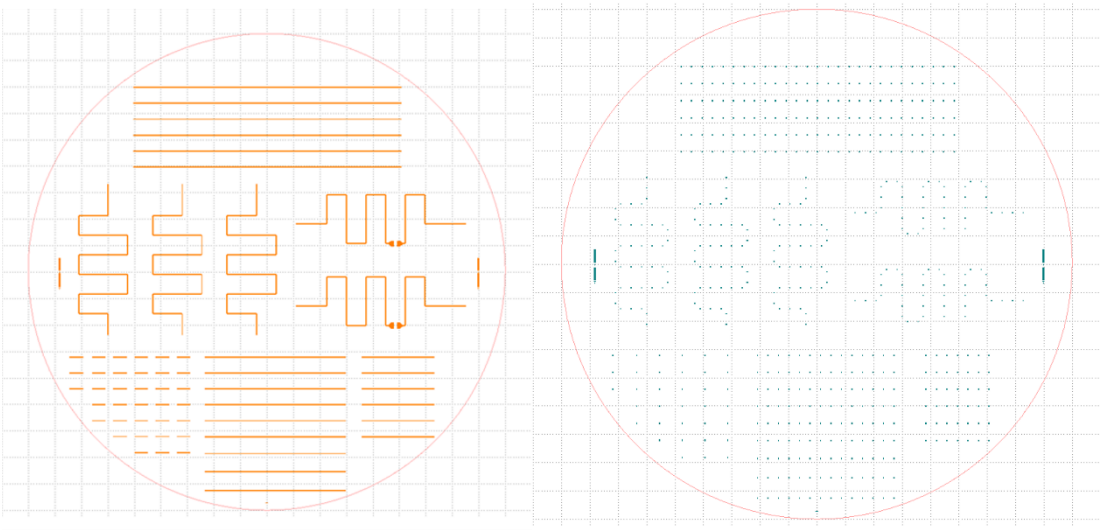


Figure 6.2: Mask layer 1 and layer 2.

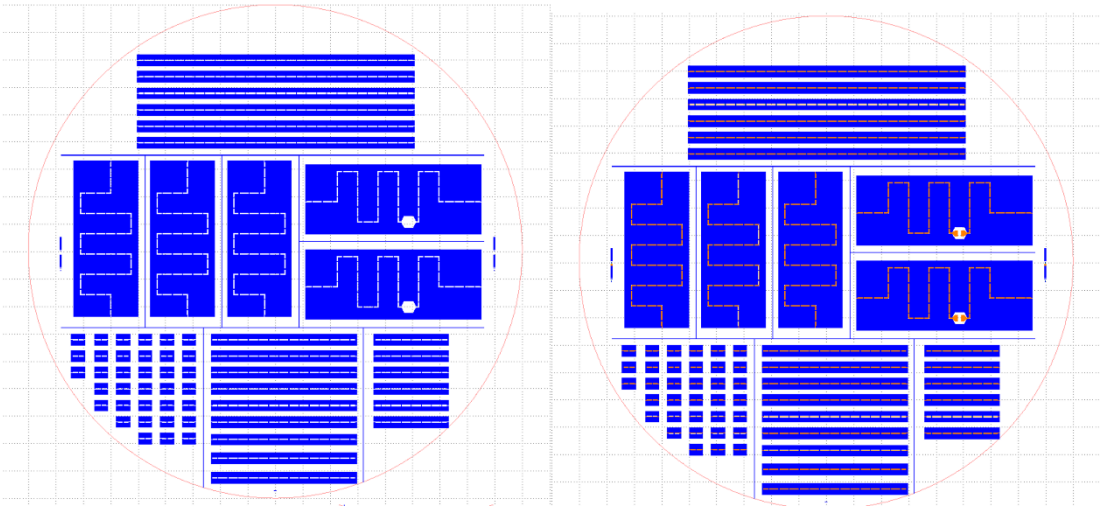


Figure 6.3: Mask layer 3 and full layer.

Table 6.1: Layer, material and mask of DMTL phase shifter

Layer	Material	Thickness (µm)	Mask Required
Passivation layer	Polysilicon	0.5 µm	No
Centre conductor	Aluminium	0.3 µm	Yes
Dielectric	Silicon dioxide	0.5 µm	Yes
Anchor of the bridge	SU-8	2 µm	No
Sacrificial layer	SU-8	2 µm	No
Ground and bridge	Aluminium	1 µm	Yes

6.3 Fabrication of a 2-bit DMTL phase shifter

Figure 6.4 shows the fabrication process of the proposed 2-bit DMTL phase shifter. Firstly, a fresh high resistivity silicon (HRS) wafer is treated using oxygen plasma in a barrel asher for approximately 1 hour to remove any contaminant or any solvent from the silicon surface. As reported in [87], microwave components such as transmission lines would experience significant loss when they are constructed directly on a high-resistivity silicon (HRS) wafer with a thin passivation layer made of nitride or oxide materials. The formation of a charge-trapping layer between the HRS wafer and the passivation layer has been reported to increase the attenuation of a transmission line considerably. To address this issue, several techniques have been suggested to eliminate the formation of the conduction layer [88]–[91]. One of the methods is to grow a thin layer of polysilicon on the HRS wafer before the deposition of oxide or nitride layers. By having a thin layer of polysilicon on top of the HRS substrate, it could act as a stabilising layer by trapping the electrons thus reducing the attenuation of the fabricated transmission line [87]. Therefore, a 0.5 µm thick polysilicon layer is grown on the HRS wafer in a furnace. The time required to complete the deposition of the polysilicon layer is one hour. Next, a 300 nm thick aluminium is sputtered and patterned using dry etching process to form the centre conductor of the CPW transmission line. The deposition of the aluminium is achieved using electron beam evaporation technique while the dry etching process is carried using reactive-ion-

etching (RIE) plasma etcher tool. Afterwards, 0.5 µm SiO_2 is deposited on top of the centre conductor and subsequently patterned to act as a dielectric layer. The process is carried out at 300 °C for 30 minutes. To create anchors of the MEMS bridges for the phase shifter as well as to serve as sacrificial layer, a 2 µm thick SU-8 2 is spin coated, patterned and cured up to 210°.

The bridges and ground of the CPW transmission line are then deposited on the SU-8 layer. A dry etch process using oxygen plasma is carried out to release the bridges. During this etching process, the exposed SU-8 will be etched, while the unexposed SU-8 below the ground of the CPW transmission line will form the anchors for the MEMS bridges. The release step has been carried out using a barrel asher. The time required to completely release the bridges is 1 hour and 30 minutes. The final device is shown in Figure 6.5 and Figure 6.6.

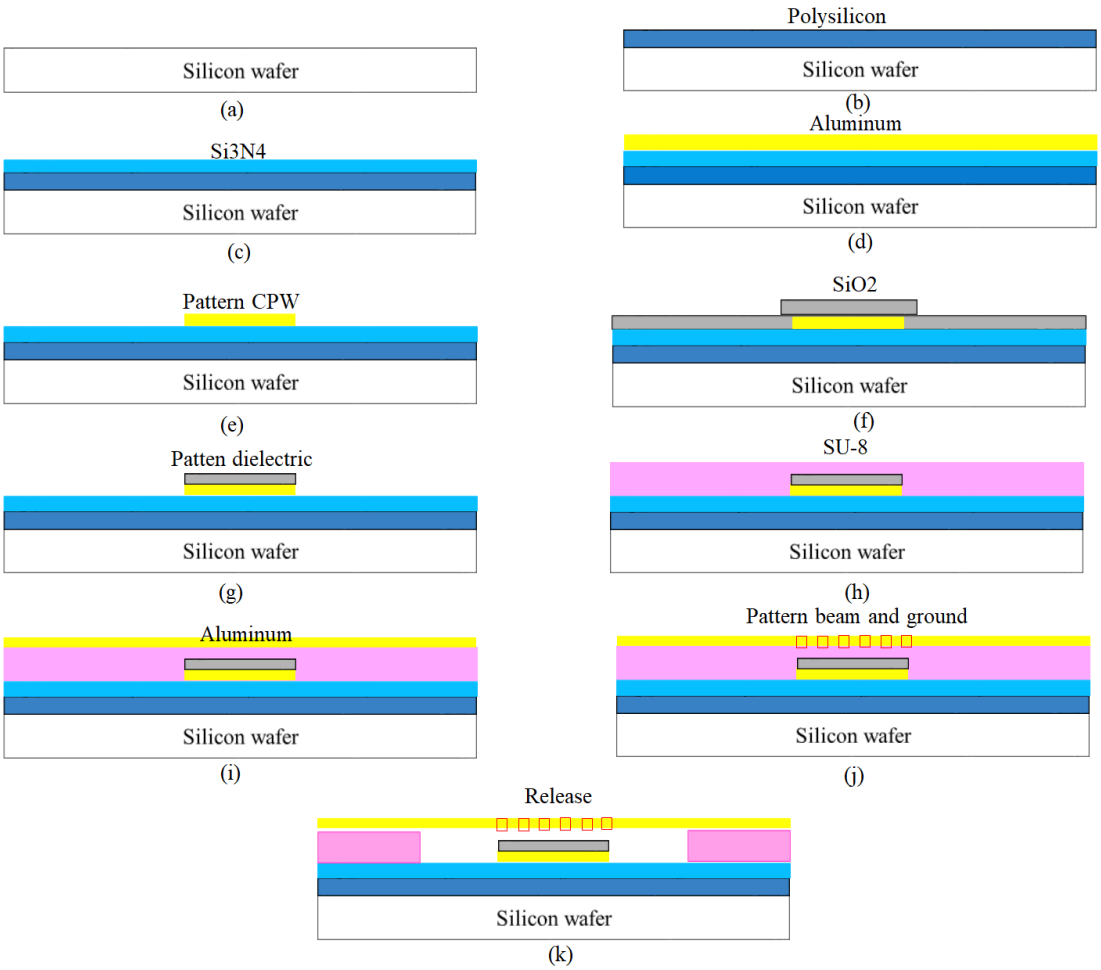


Figure 6.4: Fabrication process of the 2-bit DMTL phase shifter.

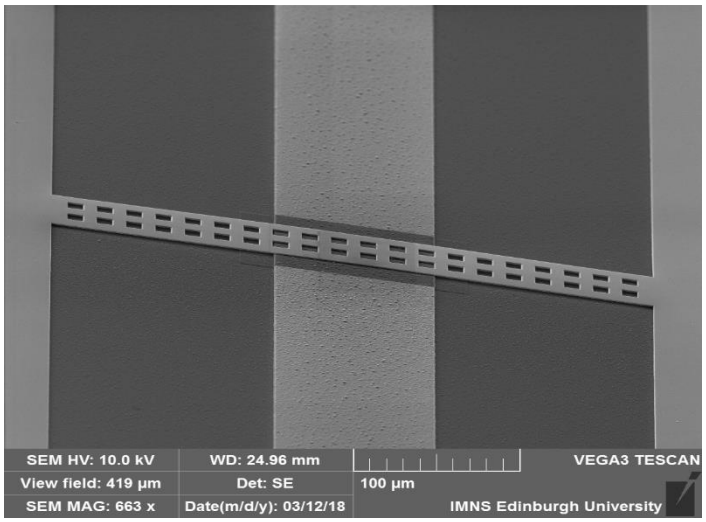


Figure 6.5: Single bridge of DMTL phase shifter.

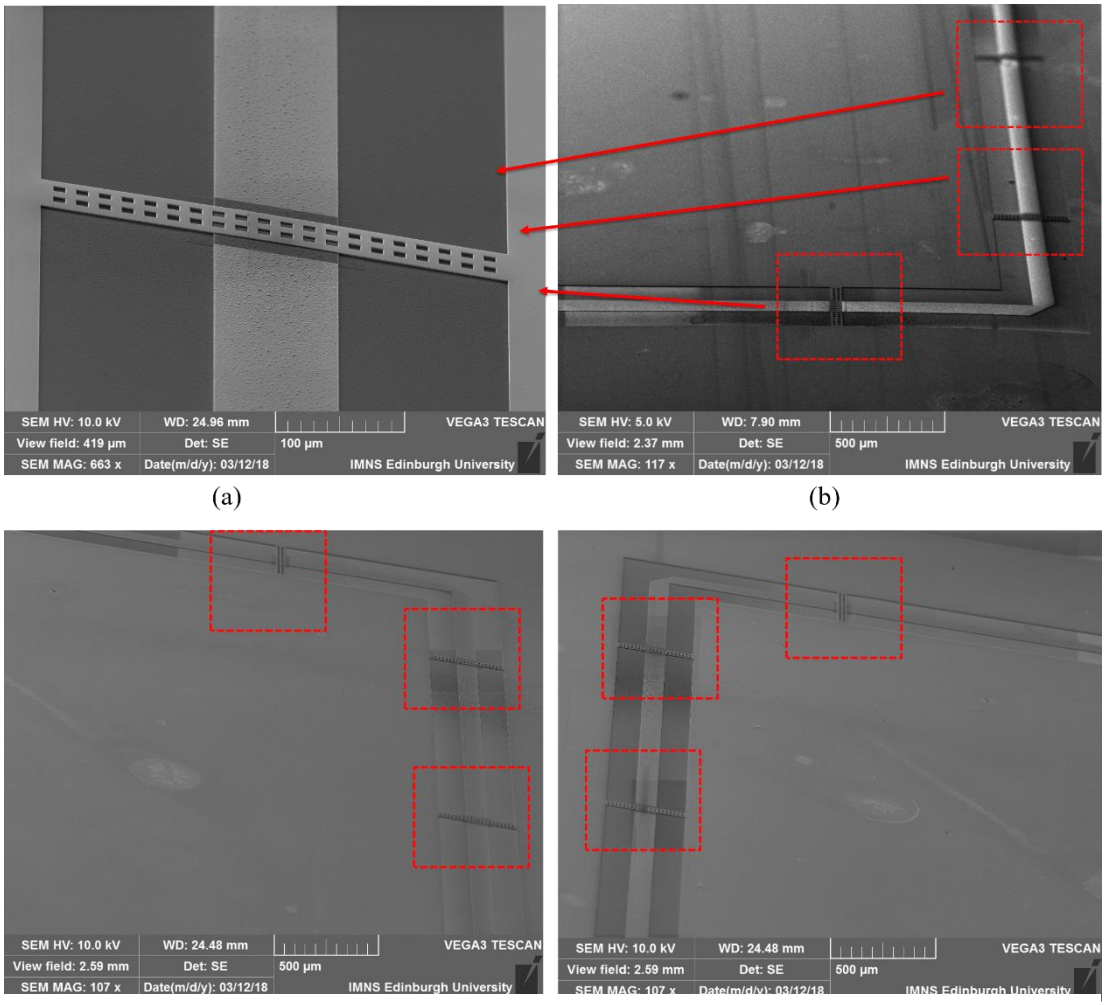


Figure 6.6: (a) Close up image of one of the released bridges in the phase shifter. (b)(c)(d) Images of several released bridges in the DMTL phase shifter.

6.4 RF Measurements of DMTL Phase Shifter

In order to characterise the RF performance of the proposed phase shifter, a test setup that consists of a HP8753 vector network analyser (VNA), two Cascade GSG probes and a DC voltage supply has been used. A GPIB connection was made between the VNA and a laptop to acquire the measured data. A calibration process was performed on the VNA using a calibration kit before the measurements were made from 300 kHz to 10G Hz. This is to ensure accurate measurements are made by removing any parasitic effects that may come from the test cables and the probes. There was no packaging for the device and thus the measurements were conducted on a bare die level.

Before connecting the device to the VNA, an initial DC test was performed to measure the pull-in voltage of the bridges on the device. It is found that the bridges were actuated when a DC bias of 40 V was applied. This encouraging result makes it possible to actuate and measure the device using the VNA since the available bias-tee can only limit up to 40 V of DC bias from going to the VNA.

For the 2-bit DMTL phase shifter, there are 4 states (phase shifts) that can be selected which are 0^0, 90^0, 180^0 and 270^0 based on the simulation results presented in Chapter 5. The number of bridges required to be actuated to obtain these phase shifts is given in Table 6.2. The reflection coefficient, S_{11} of a device is a measure of the signal loss due to imperfect impedance matching which reflects back some of the signal to the device. For the case of digital DMTL phase shifter, the changes of impedance along the transmission line when any of its bit segment is actuated must be taken into careful consideration when choosing the characteristic impedance, Z_0 of the transmission line in the phase shifter. A maximum reflection coefficient of -15 dB was chosen to ensure that all the states produce S_{11} below -10 dB.

Table 6.2: Number of bridges required to produce phase shifts

State Number	Simulated phase shift (at 2.45 GHz)
1	0º (no bridge actuated)
2	90º (14 bridges actuated)
3	180º (27 bridges actuated)
4	270º (41 bridges actuated)

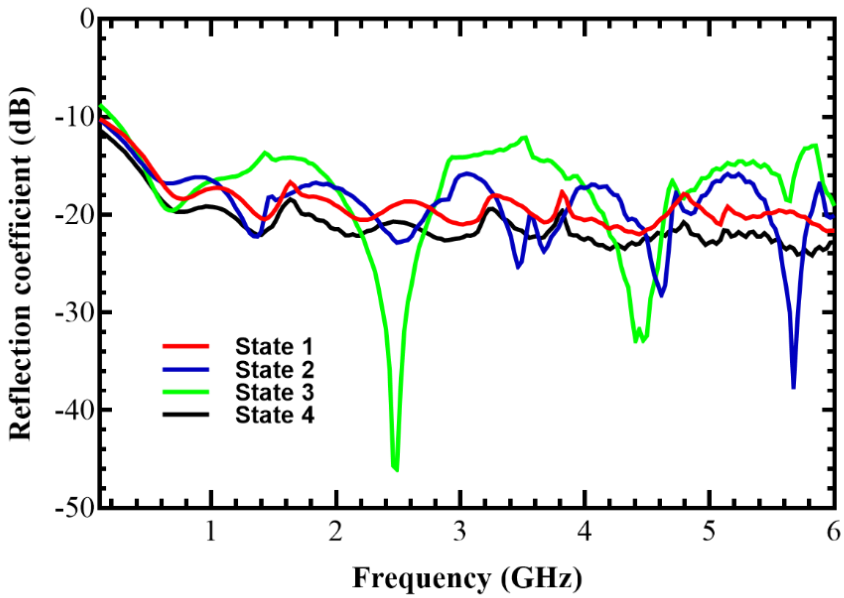


Figure 6.7: Measured reflection coefficients of the 2-bit DMTL phase shifter.

Figure 6.7 shows the measured S_{11} data for all states of the phase shifter. It is seen that the phase shifter demonstrates good impedance matching performance at each state across the operating frequency range. This gives a clear indication that the CPW transmission line incorporated in the phase shifter has been properly designed.

To measure the losses that are dissipated in the phase shifter, the transmission coefficients, S_{21} between the input and output ports of the phase shifter were measured. The measured transmission losses for all the states are given in Figure 6.8. The measured losses at 2.45 GHz for all four states are -9.38 dB, -10.31 dB, -9.74 dB and -10.51 dB respectively. The high losses obtained were expected due to the use of 300 nm thick aluminium in the fabricated phase shifter compared to the 2 µm thick aluminium in the simulated. Moreover, more investigations on the phase shifter loss will be investigated in the next section where CPW transmission lines with different configurations and thickness were fabricated and measured.

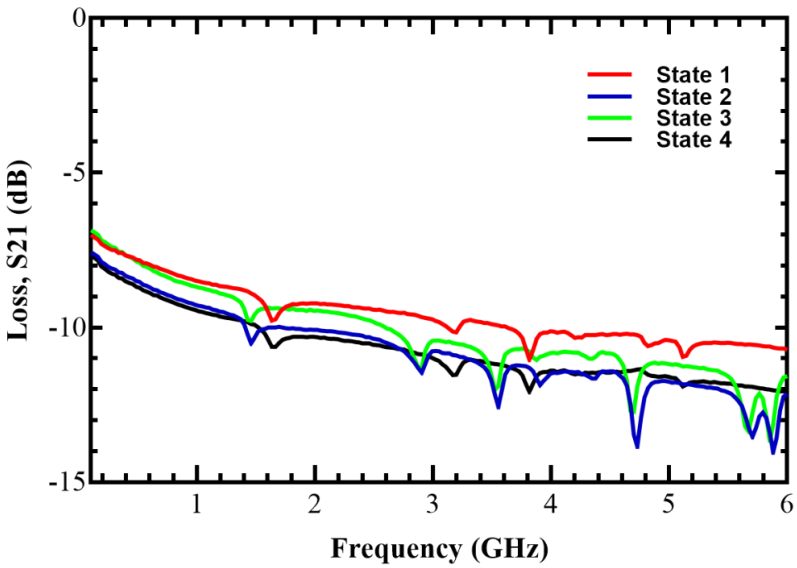


Figure 6.8: Measured transmission losses of the 2-bit DMTL phase shifter.

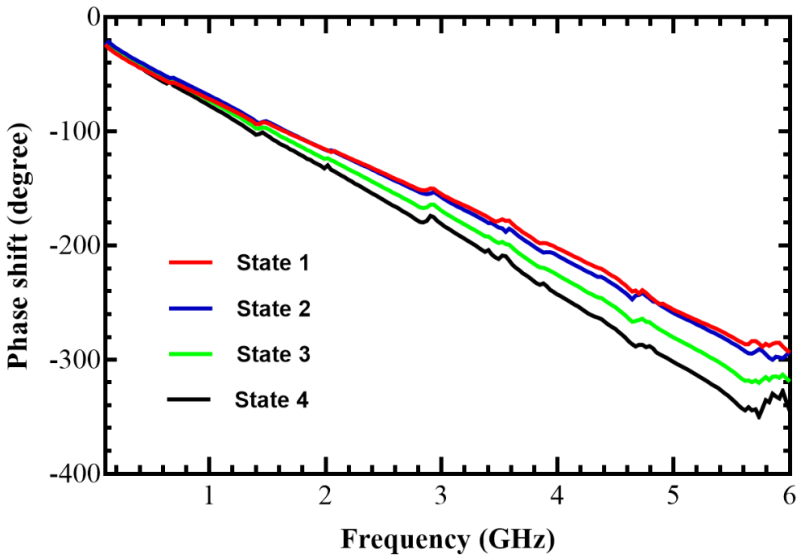
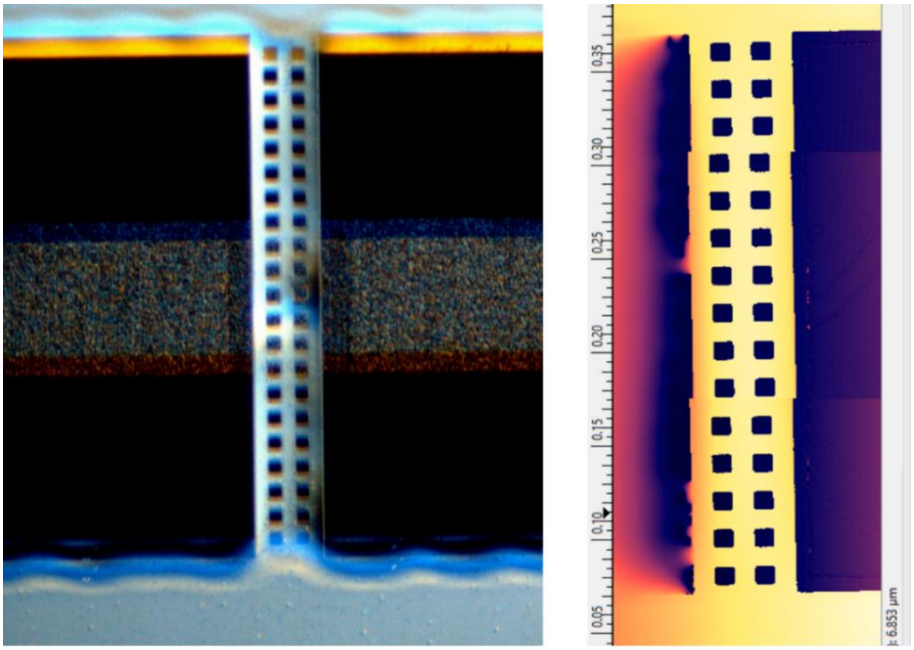


Figure 6.9: Measured phase shift of 2-bit DMTL phase shifter.

Next, the phase shifts of the phase shifters were measured as illustrated in Figure 6.9. The measured phase shifts at 2.45GHz for all four states are 0^0 (state 1), 7.96^0 (state 2), 15.91^0 (state 3), and 23.87^0 (state 4), respectively. This attributes to 0.567^0 of phase shift per bridge whereas the simulated value is 6.59^0. Compared to simulation results which yield phase shifts of 0^0 (state 1), 90^0 (state 2), 180^0 (state 3), and 270^0 (state 4), the measured phase shifts obtained from the device are quite low. Further analysis has been carried out in the next section to investigate the reason for the reduction of the measured phase shift compared to the simulation results.

6.5 Characterisation of the Bridge of the Fabricated Phase Shifter and its Effect on the Phase Shifts

One of the potential reasons for the reduction of the phase shifts from the fabricated phase shifter could be attributed to the final structure of the MEMS bridges after release. This issue has also been encountered in the MEMS varactors presented in Chapter 4. It is to be noted that reductions in measured capacitance values of MEMS varactors or switches due to wrapped or buckled bridges have been widely reported in the literature [78], [92]–[94].



(a) (b)

Figure 6.10: (a) MEMS bridge profile under microscope (b) MEMS bridge profile under interferometer.

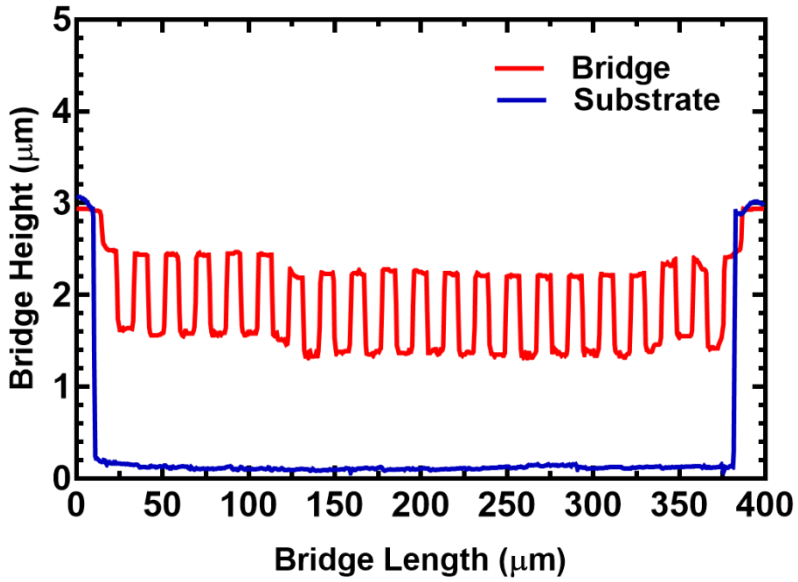


Figure 6.11: Profile of the fixed-fixed bridge along its length.

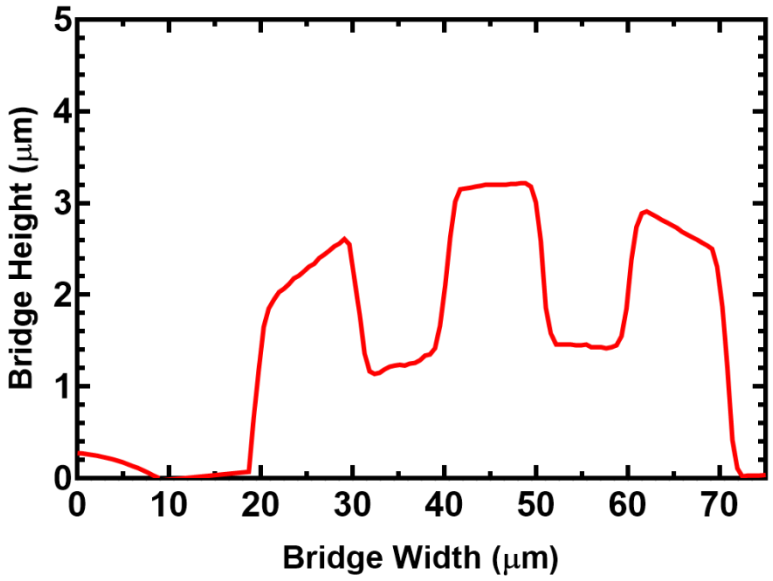


Figure 6.12: Profile of the fixed-fixed bridge along its width.

There are several reasons that cause a free standing structure to buckle including the effect of thermal cycling in fabrication process, release technique, bridge design and metal selection and thickness. Therefore, the profile of the bridge was measured using a light interferometer to investigate for any warping or buckling in the bridge structure as shown in Figure 6.10. The profiles of the bridge along its length and width directions are illustrated in Figure 6.11 and Figure 6.12 respectively. It is seen that the bridge warps at both directions at around 1 µm. Even though a warping of around 1 µm seems very good for a bridge with 372 µm in length and 50 µm in width, it still causes a formation of air gap of 1 µm on top of the dielectric during the pull-down state of the bridge which reduces the capacitance hence the phase shift of the phase shifter. This scenario was then modelled in the EM simulator to verify the effect of this air gap on the resulting phase shift as experienced by the phase shifter. A single cell of the phase shifter with a warped bridge similar to the fabricated bridge structure was simulated as shown in Figure 6.13 and Figure 6.14. The simulated phase

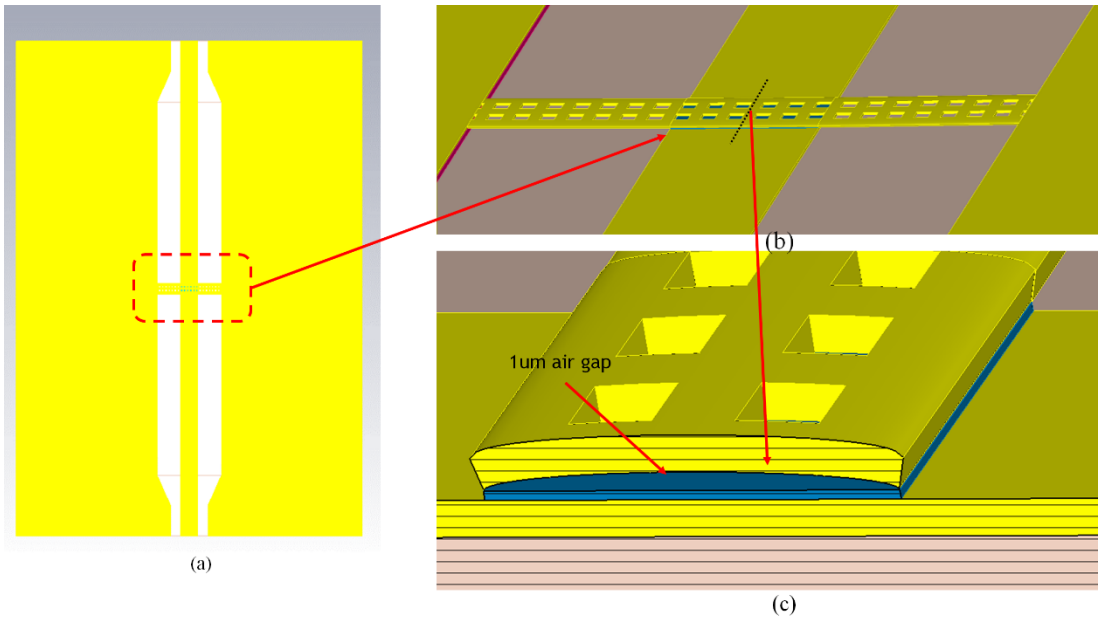


Figure 6.13: Profile of the warped bridge model in EM simulator. (a) Top view, (b) perspective view and (c) cross-section view at the middle of the bridge.

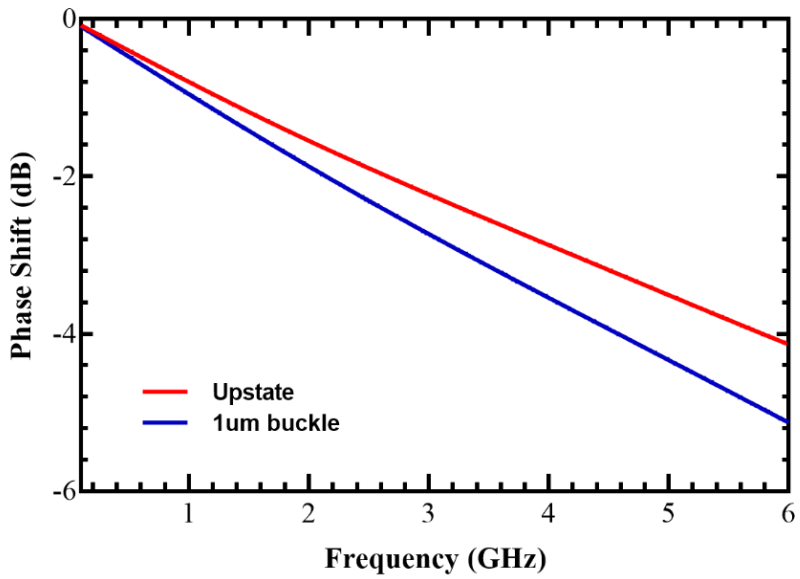


Figure 6.14: Simulation of phase shift for a warped bridge.

shift between the up-state and down-state positions with the buckling profile around 0.54^0 which is comparable to the measured value of 0.567^0. Thus, it can be concluded that the measured low phase shift obtained is due to the warping profile of the bridge. This issue could be solved if a flat bridge can be realised.

The residual stress and stress gradient developed within the fabricated bridge were investigated through analytical and simulation models. To find the residual stress in the bridge, the bridge was modelled in CoventorWare with various stress values ranging from 30 MPa to 100 MPa as shown in Figure 6.15. It is seen that the pull-in voltage of the bridge increases linearly with the stress. By interpolating the data using the measured pull-in voltage of 40 V, the residual stress developed in the bridge is found to be 79 MPa. Moreover, the stress gradient that causes the bridge to warp over its length and width was investigated by varying its value from 50 MPa/µm to 300 MPa/µm as demonstrated in Figure 6.16. It is observed that when the stress gradient is 300 MPa/µm, the bridge warps about 1 µm over its width which shows good agreement with the measured profile of the bridge. The simulated warped bridge model is shown in Figure 6.17.

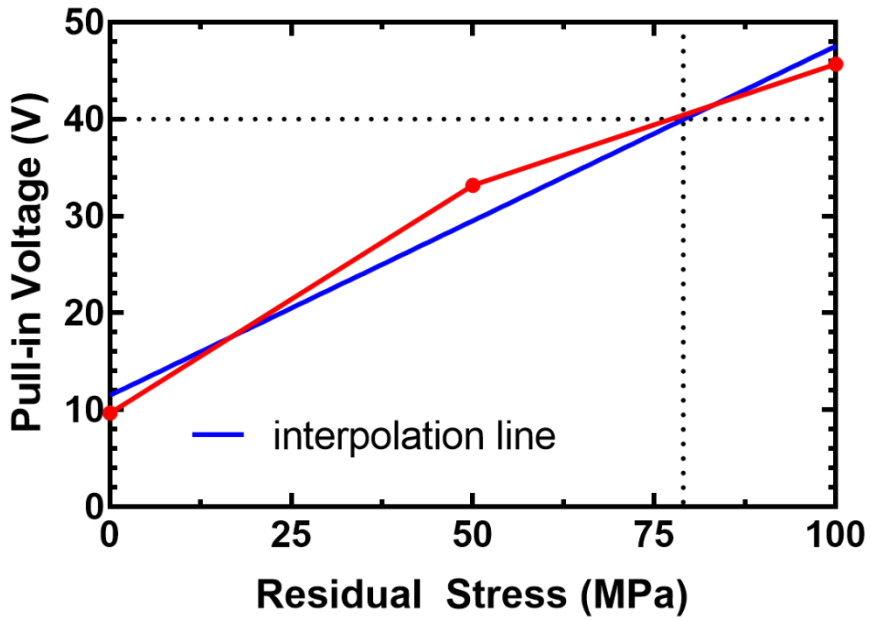


Figure 6.15: Effect of residual stress on pull-in voltage of the bridge in the phase shifter.

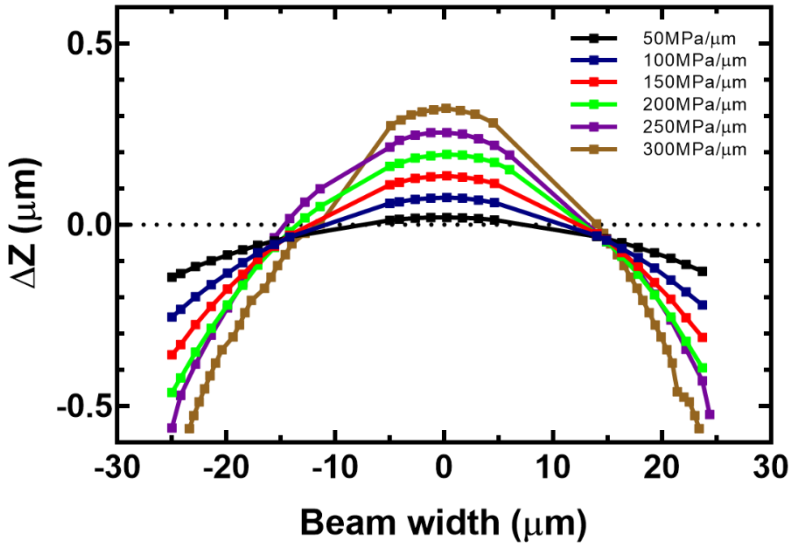


Figure 6.16: Effect of stress gradient on the bridge.

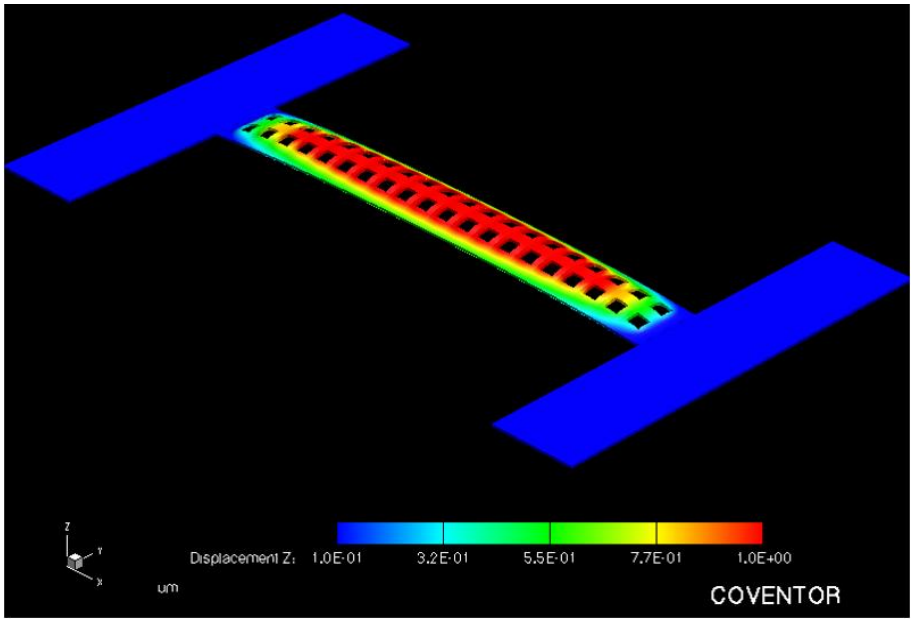
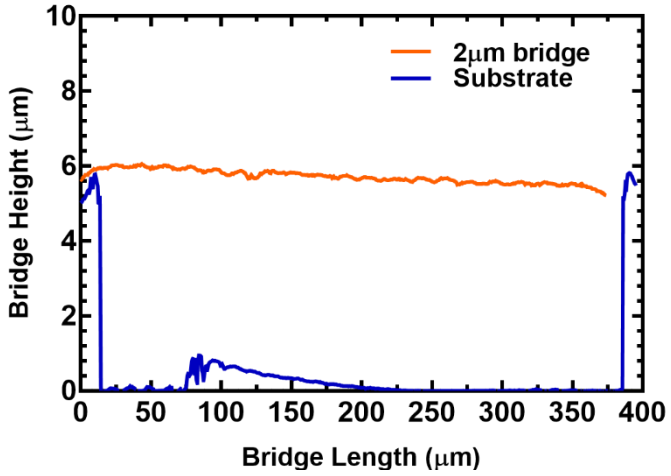


Figure 6.17: Simulation of the warping effect on the bridge.

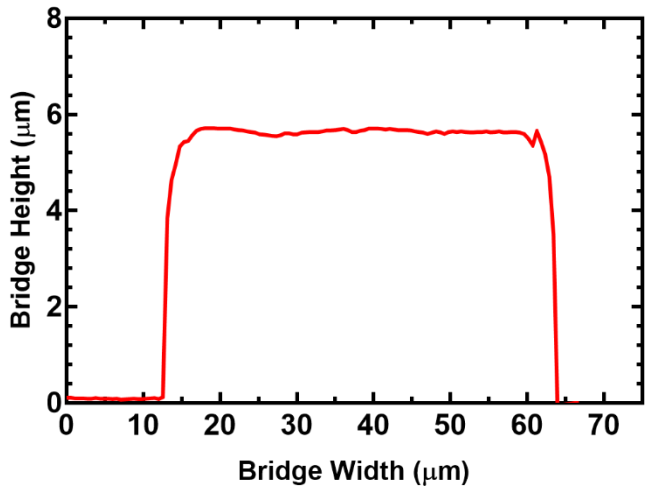
6.5.1 Realisation of Flat MEMS Bridge using 2μm Aluminium

To address the warping effect on the bridge, a simple fabrication has been carried out using 2 μm aluminium for the construction of the bridge. The final release bridge structure was then measured using a light interferometer in order to obtain its profiles. Figure 6.18 demonstrates the profiles of the 2 μm bridge along its length and width

directions. It is observed that the fabricated bridge has a very flat profile at both directions which could potentially improve the performance of the phase shifter. However, it is expected that the pull-in voltage of the bridge will increase compared to the 1 µm thick bridge configuration used in the phase shifter. This requires further optimisations on the bridge design to reduce the actuation voltage to a reasonable value in the future.



(a)



(b)

Figure 6.18: Measured profile of the 2µm along its (a) length and (b) width.

6.6 Increasing the Phase Shift of the Phase Shifter using Nitride as Dielectric Layer

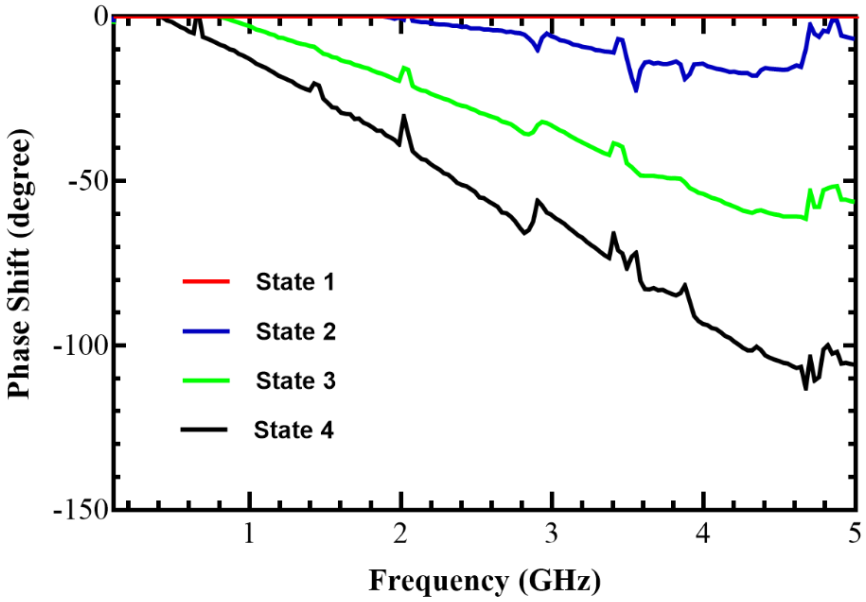


Figure 6.19: Measured phase shifts using Si_3N_4 as dielectric.

Based on the finding in the previous section that confirms the warping of the bridges in the MEMS phase shifter reduces the phase shifts of the device, another fabrication process has been carried out to investigate whether the phase shifts of the phase shifter could be increased by using different dielectric layer than the oxide. By using equation (3.2), it is shown that the down-state capacitance of the varactor hence the phase shift can be increased by using a dielectric layer with higher dielectric constant than the oxide. Due to the availability of silicon nitride deposition in the cleanroom, the oxide layer has been replaced with silicon nitride which has higher dielectric constant of 7.5 compared to oxide with reported dielectric constant of 3.4. Therefore, based on the calculation using equation (3.2), the down-state capacitance of the varactor can be increased by 2.2 times the original value thus increasing the phase shift of one MEMS varactor from 0.567^0 to 1.251^0. Based on the same fabrication process, another batch of the phase shifter has been fabricated by replacing the oxide layer with silicon nitride to improve the phase shift of the phase shifter.

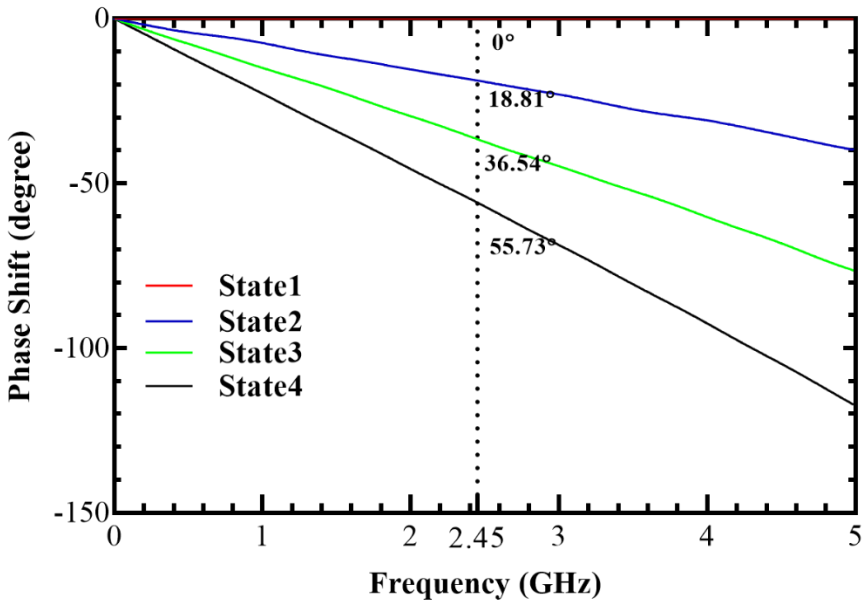


Figure 6.20: Simulated phase shifts by implementing the warped bridge in the phase shifter.

The fabricated phase shifter was then measured using the same measurement setup used in the previous measurements. Figure 6.19 demonstrates the measured phase shifts of the 2-bit DMTL phase shifter with nitride as its dielectric layer. It is seen that the phase shifts of the device increase by 125.4% compared to the previous phase shifter design that uses oxide as the dielectric layer. Table 6.3 shows the comparison of the measured phase shifts between the phase shifters fabricated using oxide and nitride as the dielectric layer. The increase of the phase shifts observed validates the earlier calculation hence proving that the capacitance of the varactor used in the phase shifter can be increased by utilising a dielectric material with higher permittivity value. It is to be noted that the measured phase shift values are still below the simulated values since the warping issue experienced by the MEMS bridge was not being addressed in this fabrication. Nevertheless, it can be concluded that the phase shifts of the MEMS devices could be easily increased by using different dielectric materials with higher dielectric constant. Furthermore, to the best of my knowledge, this is the highest measured phase shift a DMTL phase shifter has achieved at 2.45GHz. The phase shifter was then simulated by incorporating the warped bridge structure in the simulation to verify the measured results as shown in Figure 6.20. It is seen that the simulated phase shifts agree well with the measured results and hence validating the

effect of warping to the reduction of the differential phase shifts of the fabricated device.

Table 6.3: Comparison of the measured phase shifts between oxide and nitride as dielectric layer

State	Measured phase shift using oxide (°)	Measured phase shift using nitride (°)
1	0	0
2	7.96	17.89
3	15.91	34.51
4	23.87	52.39
Phase shift/ bridge	0.567	1.278

6.7 Simulation of the Beam Steering Performance of Phased Array Antenna using the Fabricated Phase Shifter

To investigate the maximum beam steering angle that can be achieved using the measured phase shifts of the fabricated phase shifter, a 4-element phased array antenna as shown in Figure 6.21 designed using a sensing antenna proposed for microwave head imaging in [6] has been developed in CST Microwave Studio. The distance, d between the adjacent antennas in the array is kept at 62.5 mm calculated using equation (6.1).

$$d = \frac{\lambda_0}{1 + |\sin \theta_{max}|} \tag{6.1}$$

where λ_0 is the operating wavelength of the antenna specified at 2.45 GHz and θ_{max} is the maximum steering angle of 90^0. Based on the measured phase shifts obtained from the fabricated 2-bit phase shifter as shown in Table 6.3, the maximum steering angle can be estimated using equation (6.2).

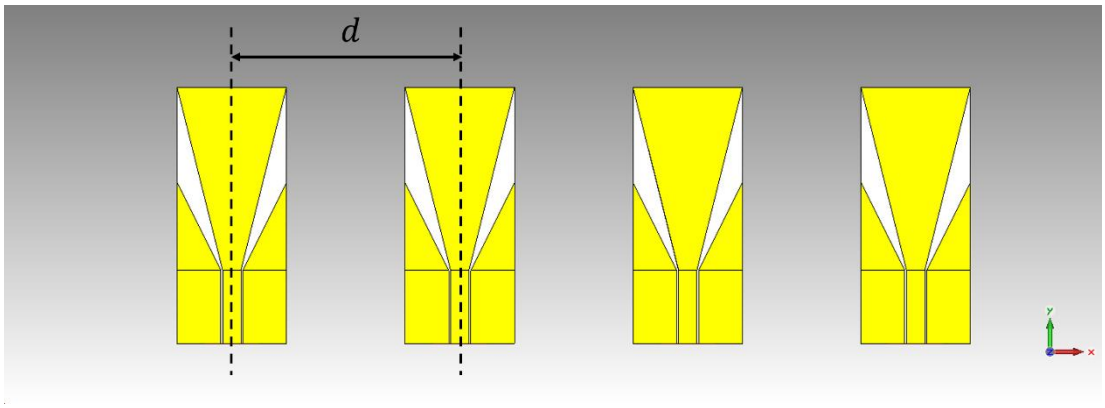


Figure 6.21: Simulation of the phased array antenna using measured phase shift values of the phase shifter.

$$\theta_0 = \sin^{-1}\left(\frac{\Delta\phi\lambda}{2\pi d}\right) \tag{6.2}$$

where $\Delta\phi$ is the progressive phase shift provided by the phase shifter which is 17.89^0. The calculated maximum steering angle is $\pm 5.73^0$. The calculated value was then verified via the simulation where it is seen that the direction of the main beam of the phased array antenna is steered to 5^0 from its boresight direction as shown in Figure 6.22 and Figure 6.23. It is expected that a maximum steering angle of $\pm 30^0$ can be

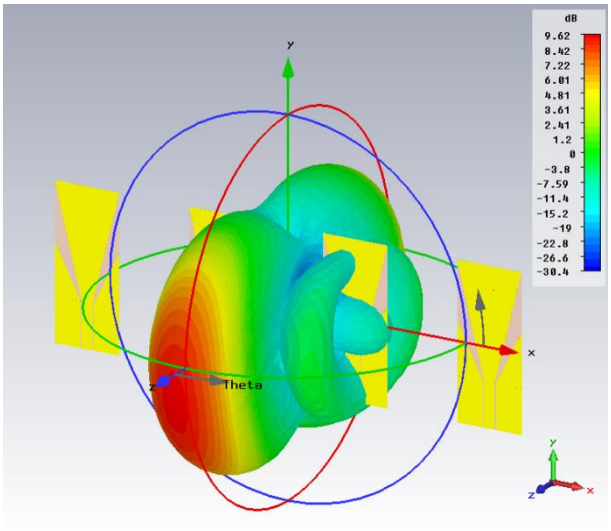


Figure 6.22: 3-D radiation pattern of the phased array antenna.

achieved if the maximum phase shift of the phase shifter can be increased to 270^0 compared to 52.39^0 obtained from the fabricated phase shifter.

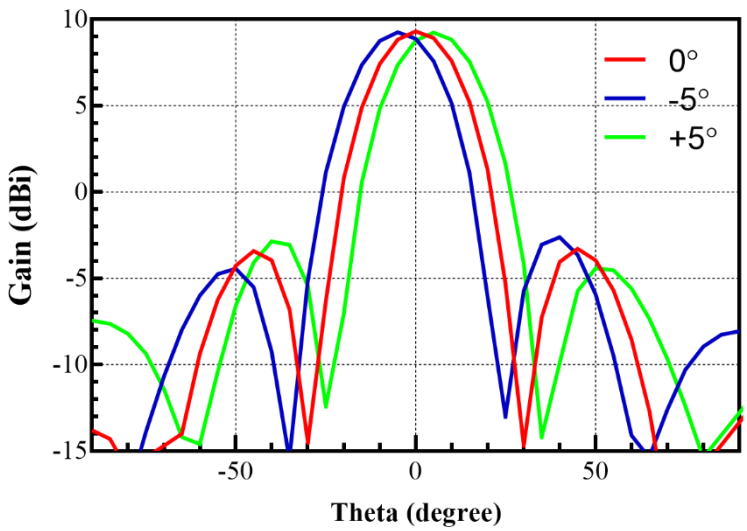


Figure 6.23: Maximum beam steering angle using measured values of the phase shifter.

6.8 Characterisation of co-planar waveguide transmission line

One of the main contributors for DMTL phase shifters loss is due to the attenuation of the transmission line. The loss becomes more prominent when the phase shifter requires a long transmission line to provide a phase shift up to 315^0 at low frequency band such as S-band (2 GHz to 4 GHz) which is proposed in this thesis. For the 2-bit and 3-bit DMTL phase shifters presented in this thesis, the required lengths for both devices are 76.45 mm and 134.79 mm which are significantly longer than the DMTL phase shifters designed for higher frequency range applications such as for space applications [75]. As such, further investigations on the loss of the CPW transmission line is important to verify that the main reason for high loss in the fabricated phase shifter is due to the use of 300 nm thick aluminium. In general, attenuation of a transmission line can be separated into two main categories which are attenuation due to losses in the substrate, α_d and the conductor, α_c. For silicon substrate, the dielectric attenuation is given by [89]

$$\alpha_d = \frac{\varepsilon_{eff}(f) - 1}{\sqrt{\varepsilon_{eff}(f)}} \left\{ 1.7095 \times 10^{-3} f + \frac{153.09}{\rho} \right\} \left(\frac{dB}{cm} \right) \tag{6.3}$$

where f is the frequency in GHz and ρ is the resistivity of the silicon substrate in Ω·cm. Based on equation (6.3), the calculated dielectric loss of the CPW transmission line on the HRS wafer (10k Ω·cm) used for the phase shifter is less than 0.09 dB/cm which is reasonably low. It can then be estimated that the dielectric loss of the fabricated 2-bit DMTL phase shifter is around -0.7 dB which is very small compared to the measured average transmission loss of -10 dB. Thus, it was predicted that the high loss of the phase shifter must come from the use of 300 nm thin aluminium due to skin depth effect. To verify this finding, the phase shifter was again simulated with 300 nm thick centre conductor in CST Microwave Studio. In the EM simulator, the skin depth effect can be imposed on the model by utilising the surface impedance model provided in its macro as shown in Figure 6.24. The simulated and measured phase shifter losses using 300 nm thick aluminium for State 1 are illustrated in Figure 6.25. It is seen that the

simulated loss of the phase shifter are comparable to the measured data thus confirming that the high loss experienced by the phase shifter is due to the skin depth effect where the skin depth value of aluminium at 2.45 GHz is 1.66 µm. Thus, 300 nm thick aluminium used for the fabrication of the phase shifter is much lower than the skin depth of aluminium at the operating frequency. Nevertheless, it is expected that significant improvement on the phase shifter loss can be made if the device is fabricated using thick metal process. To investigate the effect of using 2 µm aluminium on the loss of the phase shifter as proposed in the initial design, another simulation was carried out where the aluminium thickness was changed to 2 µm instead of 300 nm. The simulated loss for State 1 of the 2-bit phase shifter has greatly improved from -9.38 dB to -2.4 dB as illustrated in Figure 6.26. This shows that the loss of the phase shifter can be significantly reduced by using 2 µm thick aluminium instead of 300 nm used in the fabrication. Moreover, the simulated loss of the phase shifter using 2 µm aluminium was experimentally verified and will be presented in the next section. Additionally, detailed characterisation of co-planar waveguide transmission line with various centre conductor widths is presented with the aim to further improve the loss of the phase shifter.

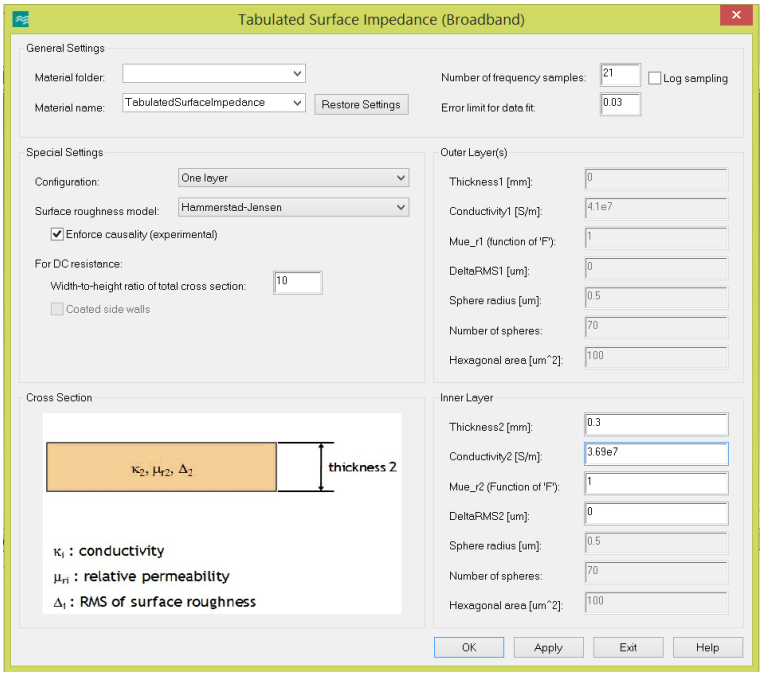


Figure 6.24: Surface impedance feature in CST Microwave Studio.

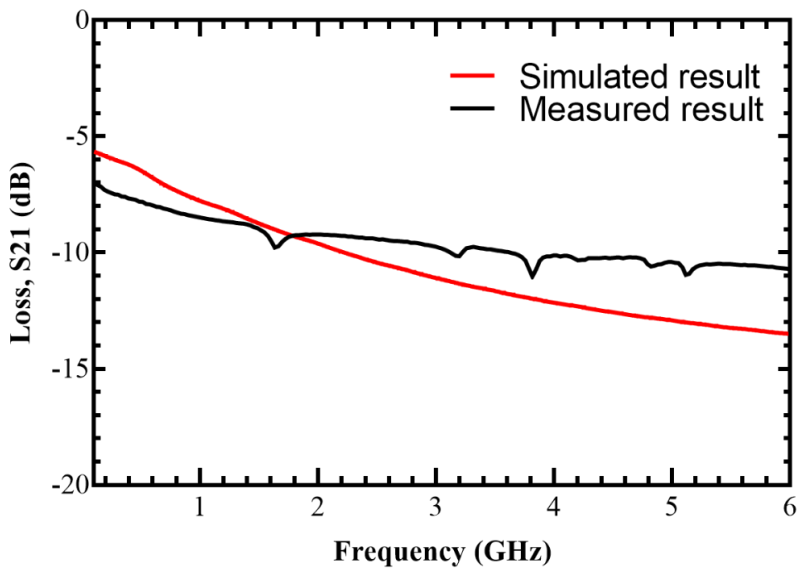


Figure 6.25: Loss comparison between simulated and measured phase shifter for State 1.

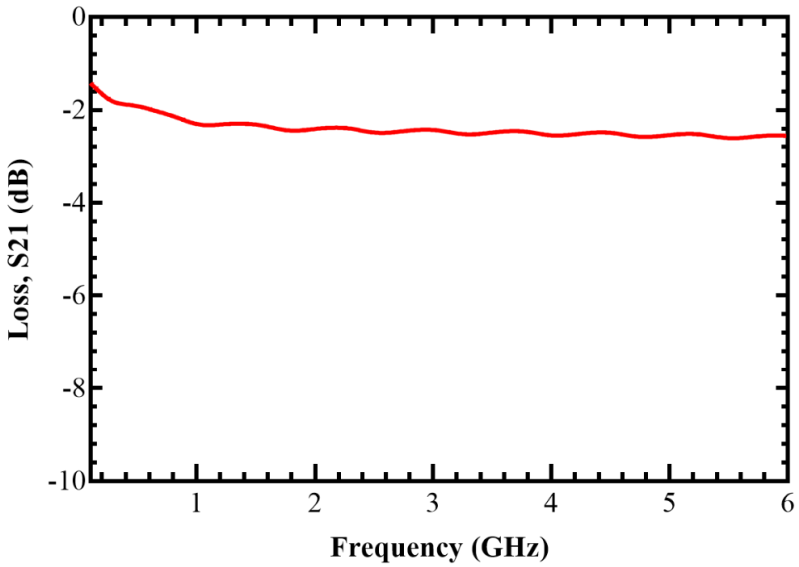


Figure 6.26: Simulated transmission loss of the phase shifter for State 1.

Typically, CPW transmission lines fabricated using standard photolithography technique on PCB circuit have a metal thickness, *t* of several times the skin depth, δ

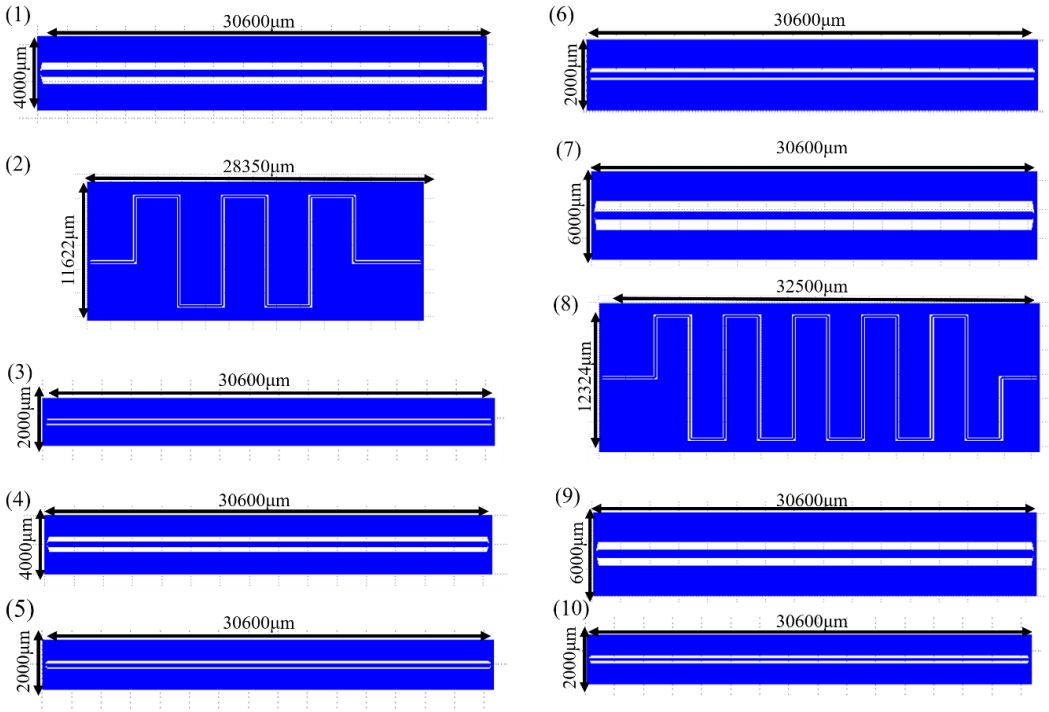


Figure 6.27: Variations of the CPW transmission line.

where a thickness of more than 17 µm is generally implemented . However, to achieve this thickness using standard surface-micromachining technique in cleanrooms is very challenging. Thus, RF MEMS devices are first fabricated using thin metal structure where additional electroplating process is done to increase the thickness of the devices to reduce the loss[1]. For the fabricated phase shifter, a 300 nm thick aluminium is used for the centre conductor of the CPW transmission line whereas the ground and

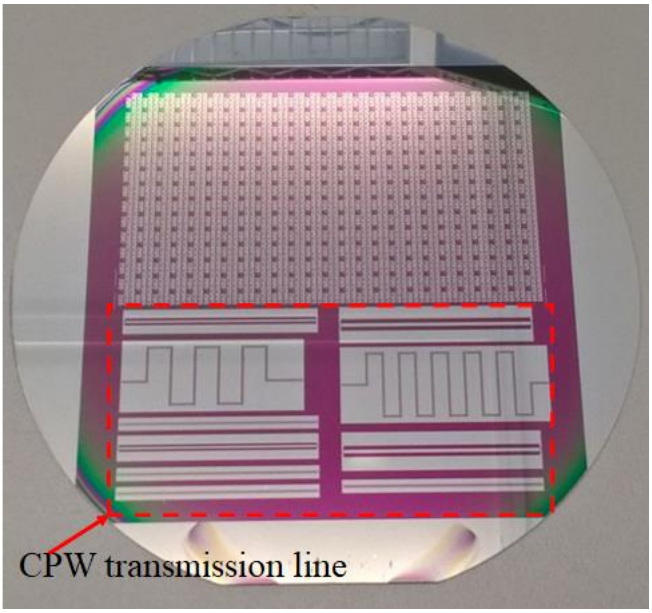


Figure 6.28: Fabricated CPW transmission lines

the bridges are made of 1 µm thick aluminium. The use of a thin metal is to comply with the fabrication tools in the cleanroom and to eliminate the need for chemical-mechanical planarisation (CMP) process for the planarisation of the SU-8 sacrificial layer before the deposition of the MEMS bridges since the deposited sacrificial layer will follow the contours of the structure below it. Thus, a thick centre conductor structure could potentially cause the bridges to break at the points where there is a large step height change if the CMP process was not carried out. Another reason to skip the CMP process is that the optimisation of the process on SU-8 could be time-consuming. Nevertheless, this step could be optimised in future work. Figures 6.28 and 6.29 show the variations of the CPW transmission lines that were fabricated and measured to investigate the effect of different thicknesses and geometries of the transmission lines using the aluminium deposition tools in the cleanroom. The dimensions of the CPW transmission lines are given in Table 6.4. Moreover, this study

will improve the phase shifter loss if thicker aluminium at 2 µm and wider centre conductor width is integrated in the phase shifter design.

Table 6.4: Dimensions of the CPW transmission line

Design	$Z_0(\Omega)$	S/G
1	64	300/450
2	64	100/136
3	62	100/122
4	62	300/390
5	63	100/130
6	64	100/136
7	64	500/750
8	62	100/122
9	62	500/650
10	65	100/150

6.8.1 Varying the Thickness of the Aluminium of the CPW Transmission Line

The characteristic impedance, Z_0 of the fabricated CPW transmission lines is fixed at 64 Ω similar to the characteristic impedance used in the fabricated 2-bit phase shifter. The transmission lines were fabricated using 300 nm and 2 µm aluminium using electron-beam deposition and sputtering process respectively. The surface trapped charge effect has been removed by etching the nitride (passivation layer) at the gap of the CPW transmission as shown in Figure 6.29. The dimensions of the CPW are fixed

Figure 6.29: (a) Si_3N_4 as passivation layer. (b) Etched Si_3N_4 to eliminate surface conduction layer.

where the width of the centre conductor is 100 µm and the gap is 136 µm. The length of the transmission line is fixed at 30.6 mm. The measured transmission losses at 2.4 GHz are -1.69 dB and -5.6d B for 2 µm and 300 nm aluminium respectively as shown in Figure 6.30. This shows that increasing the metal thickness could significantly reduce the loss of the transmission line.

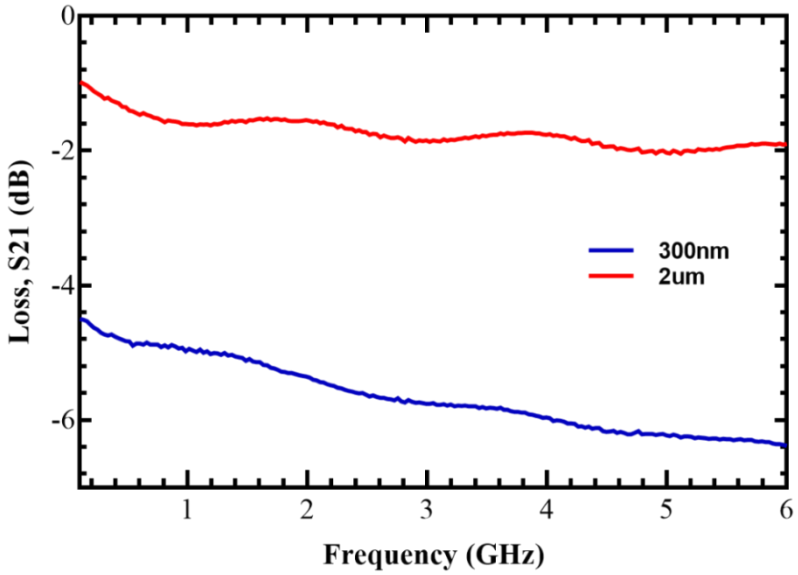


Figure 6.30: Measured transmission loss by varying the thickness of the CPW transmission line.

6.8.2 Varying the Centre Conductor width of the CPW Transmission Line

In addition to using 2 µm aluminium for the CPW transmission line, further improvement on the attenuation can be made by increasing the width of its centre conductor where the characteristic impedance of the CPW transmission lines were kept at 64 Ω. The measured transmission losses at 2.4 GHz are -1.69 dB, -0.78 dB, and -0.61 dB for a centre conductor width of 100 µm, 300 µm, and 500 µm respectively as illustrated in Figure 6.31 where the length of the CPW line is fixed at 30.6 mm. This proves that increasing the centre width of the CPW transmission line could further improve the loss of the CPW transmission line. The thickness of the aluminium is 2 µm for all cases. The lowest measured transmission loss that has been achieved using the

etching gap method is 0.193 dB/cm where the width of the centre conductor the CPW transmission line is 500 µm.

6.8.3 Comparison between Straight and Meandered CPW Transmission Lines

The effect of using right angle bends in the phase shifter for device miniaturisation is verified by fabricating the meandered transmission line using 2 µm thick aluminium and comparing its loss with the straight line CPW transmission line structure of similar

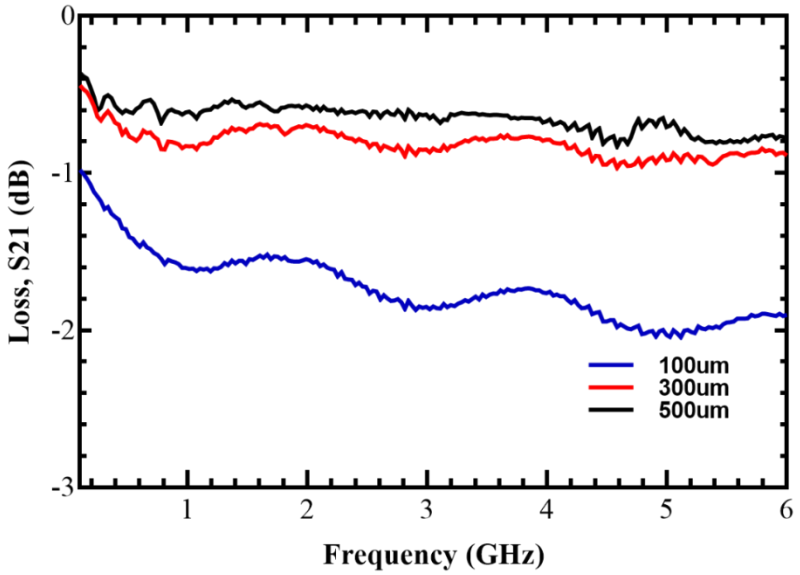


Figure 6.31: Transmission loss of varying centre conductor width.

length. Figure 6.31 depicts the transmission loss between the two CPW transmission line configurations where the length of both lines is 76.45 mm. It is seen that the transmission losses at 2.4 GHz are -3.3 dB and -4.23 dB for meandered and straight lines respectively. The CPW transmission line with bends has less loss than its straight counterpart by around 1 dB. This finding has also been reported in [83]. It is concluded that the use of right angle bends on the phase shifter for miniaturisation purpose does not lead to additional loss. On the contrary, the loss experienced by the meandered CPW transmission line is lower than the straight CPW structure by 1 dB.

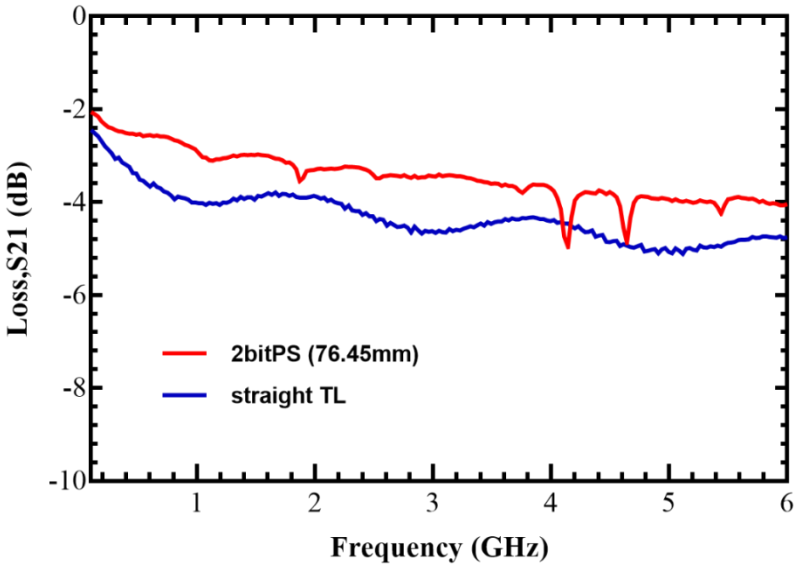


Figure 6.32: Transmission line loss of varying CPW transmission line configurations.

6.8.4 Improving the CPW Transmission Line Loss by Using Poly-Silicon Layer

The previous CPW transmission line has been evaluated by etching the passivation layer at the gap of the CPW transmission line to prevent the current leakage that leads to the increased of the transmission line loss. In this section, an investigation has been conducted to further improve the loss experienced by the transmission line by using a polysilicon layer between the passivation layer and the silicon substrate. It is to be noted that all the phase shifters that has been fabricated used polysilicon to eliminate the surface conduction layer that typically formed between the HRS silicon substrate and passivation layer which can greatly increase the loss of the transmission line [87], [88]. The same masks have been used to fabricate the transmission line with the polysilicon layer. Next, the fabricated transmission lines were measured and compared to the previous designs. A comparison is made between the previous etching gap method and the use of poly-silicon to improve the performance of the transmission line as shown in Figure 6.33 and Figure 6.34 respectively. It is clearly seen that an improvement of 1 dB has been achieved using the polysilicon method at 2.45 GHz. The transmission loss for the meandered CPW transmission line used for the 2-bit phase shifter fabricated using 2 µm aluminium is -2.39 dB, comparable to the simulated value presented in Figure 6.26. Moreover, the lowest measured transmission

loss that has been achieved is 0.122 dB/cm when the width of the centre conductor is increased from 100 µm to 500 µm for the same characteristic impedance value. Therefore, it is expected that with a very low loss CPW transmission line structure, the loss of the proposed 2-bit phase shifter can be greatly improved to around 0.93 dB.

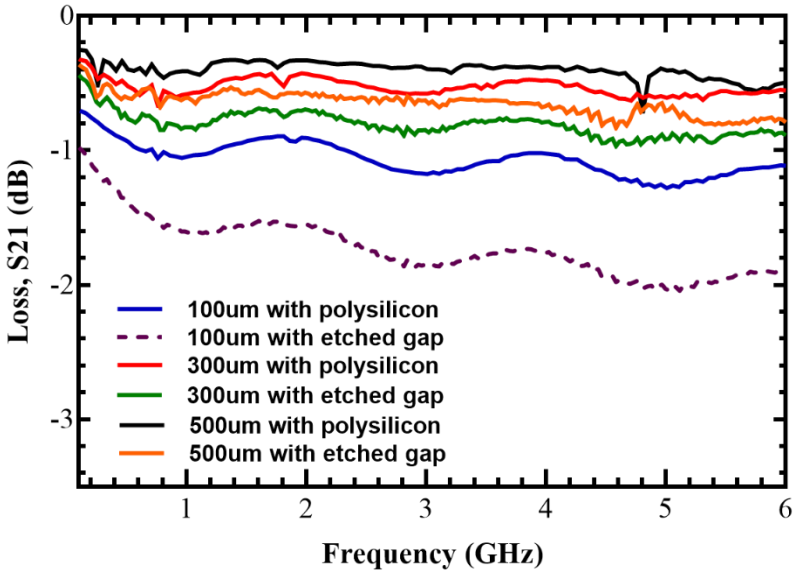


Figure 6.33: Comparison of transmission line loss between etched gap method and polysilicon.

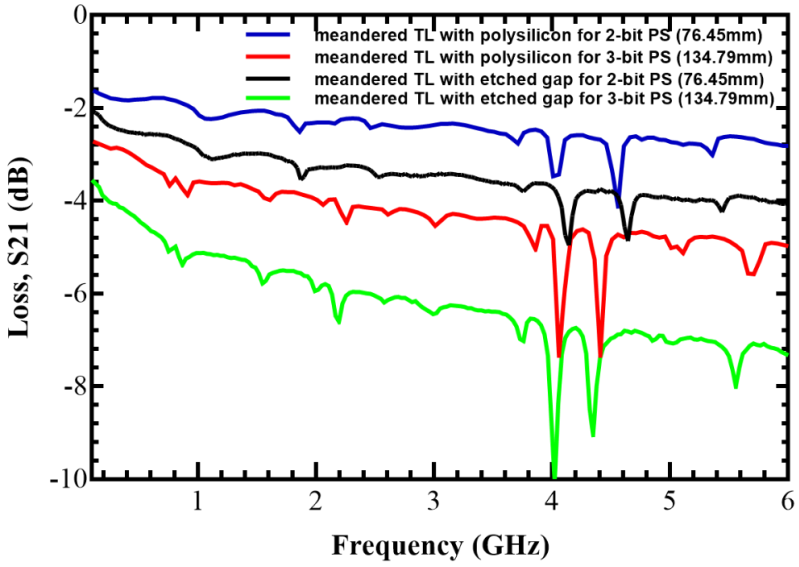


Figure 6.34: Comparison of transmission line loss between etched gap method and polysilicon.

6.9 Summary

In this chapter, the fabrication of the proposed 2-bit DMTL phase shifter presented in Chapter 5 has been described and analysed. The mask design and detailed fabrication process of the phase shifter were presented. Compared to the initial fabrication steps proposed in Chapter 5, several changes have been made to the process due to the limitation of the deposition tools in the cleanroom and to simplify the overall process needed to build the phase shifter. The main modification is the use of 300 nm thick aluminium instead of 2 µm thick aluminium for the CPW transmission line of the phase shifter. RF measurements have been carried out to verify the phase shifter performance in terms of impedance matching, transmission loss and phase shift. The measured reflection coefficients of the phase shifter at all four states are below -10 dB which show good impedance matching. The phase shifter obtained differential phase shifts of 0^0, 17.89^0, 34.51^0 and 52.39^0 compared to designed values of 0^0, 90^0, 180^0 and 270^0. The main reason behind the low measured phase shifts is because of the warping of the bridges over its width by 1 µm which created an air gap during the pull-down position hence reducing the capacitance of each of the varactor in the phase shifter. The warped bridge structure was remodelled in an electromagnetic simulator to verify the effect of the air gap towards the phase shift. Moreover, the residual stress and stress gradient of the fabricated bridge have been modelled using CoventorWare. It is found that the residual stress and the stress gradient arising from the fabrication process of the phase shifter are 79 MPa and 300 MPa/µm. It is confirmed that the formation of air gap significantly reduces the achievable phase shift of the phase shifter. On the other hand, the maximum measured transmission loss of the device is -10.51 dB at 2.45 GHz. However, the high loss experienced by the fabricated phase shifter was expected due to the use of thin aluminium of 300 nm compared to 2 µm specified in the simulated design where it has been confirmed using CST Microwave Studio. The main reasons for the changes are to comply with the fabrication capability of the available deposition tools in the cleanroom and to simplify the fabrication process. Nevertheless, additional fabrications of CPW transmission lines using 2 µm-thick aluminium have proved that the overall loss of the phase shifter could be improved significantly where transmission line loss of around -2.39 dB could be

achieved compared to the current performance of the fabricated phase shifter. In addition, the transmission loss can even be further improved to be less than 1 dB if a 500 µm wide centre conductor CPW transmission line with 2 µm aluminium is implemented in the phase shifter design. This fabrication has shown that it is possible to build a DMTL phase shifter design that can operate at lower microwave band such as S-band where a large number of MEMS bridges are required in the design with no significant deterioration on the performance of the phase shifter. Moreover, the highest measured phase shift of the phase shifter is 52.39**°** which is the highest measured phase shift by a DMTL phase shifter at 2.45 GHz reported in the literature. Table 6.5 shows a comparison with other DMTL phase shifters presented in the literature.

Table 6.5: Comparison with other works in the literature

Publication	Frequency (GHz)	Substrate	Insertion loss (dB)	FOM °/dB	Number of bit	Number of Bridge	Size (mm^2)
Borgioli et al[55]	25/35 GHz	Glass	1.7	154/160	1	11	8.58 mm long
Liu et al.[56]	26	Glass	1.7	105	3	14	11 mm long
J.S. Hayden and Rebeiz [54]	10	Quartz	0.9	180	2	16	22 µm long
J.S. Hayden and Rebeiz [45]	18	HRS	3	111	4	23	n/a
Joseph S Hayden and Rebeiz [57]	8-10	HRS	1.3	180	2	18	n/a
Kim et al. [58]	60	Quartz	2.2	122.7	2	24	6.3×1.5
Joseph S Hayden and Rebeiz [53]	14	Quartz	1.2	225	2	21	8.4×2.1
J.S. Hayden and Rebeiz [52]	37	Quartz	1.5	232.6	2	21	18
J. Hung, Dussopt, and Rebeiz [59]	78	Glass	2.7	96	3	28	4.3
J. Hung, Dussopt, and Rebeiz [60]	81	Glass	2.2	106	2	24	8

Topalli et al. [61]	15	Glass	1.5	120	3	28	30 cm
Du et al. [62]	10	HRS	1.5	80.35	5	31	51
Pillans et al. [63]	30	Alumina	2.4	100	4	13	n/a
Pillans et al. [63]	35	Alumina	2.7	94	4	13	n/a
Unlu, Demir, and Akin [64]	15/30/40	Quartz	3.1/5/8.2	116/72/43	1		64
Chakraborty et al[17]	15	HRS	0.8	20	1	4	0.75 mm
Abdellatif et.al [65]	26	Alumina	0.75	26.67	1		0.75
Chakraborty et al [66]	15	HRS	2.1	85.7	1	10	0.88×0.88
This work (Simulation)	1-4GHz	HRS	1.6	168.75	2	41	28.35 mm × 11.62
This work (Fabrication)	1-4GHz	HRS	10dB (300nm centre conductor	5.329	2	41	32.05mm × 12.62mm
This work (Simulation)	1-4GHz	HRS	2.94	107.14	3	105	30 mm × 10 mm

Chapter 7: Conclusions

7.1 Summary and Conclusions

This thesis covers the research studies on designing and developing tuneable RF MEMS devices namely digital MEMS varactors and DMTL phase shifters for wireless communications and bio-medical applications. In general, the studies can be divided into two main sections which are the development of MEMS varactor with improved capacitance ratio using SU-8 material and the realisation of digital DMTL phase shifters targeting low microwave frequency range applications mainly wideband microwave head imaging. SU-8 material, due to its capability to be sacrificial layer and as a permanent structure of the final device, has been incorporated in the fabrication process and design of the proposed devices in this thesis.

Chapter 2 presents the literature review of the existing MEMS varactors and DMTL phase shifters. The advantages and limitations of the devices are highlighted and discussed. One of the limitation of analogue MEMS varactors is its low tuning ratio of approximately 1.5 due to the pull-in effect which causes the top electrode to collapse when it reaches one third of the air gap. To build a high tuning MEMS varactor, a digital design instead of analogue configuration is commonly adopted. However, a digital MEMS varactor design still suffers from high parasitic and fringing field capacitances hence reducing its capacitance ratio. This effect is more pronounced with the use of silicon substrates because of its high permittivity value. Although this problem could be solved using low permittivity substrate materials such as quartz as a substrate for the devices, its high cost hinders its adoption. The design and development of a 4-bit and 5-bit digital MEMS varactors are presented in Chapter 3. The 4-bit and 5-bit MEMS varactors are proposed where the capacitance ratios of the devices have been improved by reducing the parasitic and fringing field capacitances due to the silicon substrate. Several methods have been explored and applied in the varactor design including implementation of trenches below the varactors, deposition of a thick SU-8 layer to elevate the devices from the substrate and increasing the distance of the ground of CPW line from the MEMS bridge. Successful simulation

results have been obtained for the 4-bit and 5-bit MEMS varactors with maximum capacitance ratios of 35.7 and 34.8 respectively. In addition, a novel truss structure has been introduced in the varactor design with the aim to reduce the bias voltage required. The analysis and comparison of the new bridge structure over the standard fixed-fixed solid configuration are carried out to validate its performance particularly in reducing the actuation voltage of the varactor.

The fabrication of a single-bridge MEMS varactor is presented in Chapter 4 to validate the efficacy of using SU-8 in suppressing the fringing field due to the high permittivity silicon substrate. The proposed varactor designs in Chapter 3 have been simplified to utilise only a single bridge in the varactor. This is carried out to reduce the complexity of the fabrication process. Although the varactor design has been simplified, the main aim to reduce the parasitic and fringing field capacitance using SU-8 could still be verified. For the final fabrication process, SU-8 has been used for the sacrificial layer. DC and capacitance measurements have been carried out to validate the performance of the SU-8 based MEMS varactor. The fabricated single-bridge MEMS varactor demonstrates improved capacitance ratio compared to a similar design without the thick SU-8 layer by 56%. It is also proved that a low-resistivity silicon wafer can be used for the construction of MEMS varactor with comparable performance to the one built on a more expensive HRS wafer. The proposed truss bridge structure shows an improvement over a standard fixed-fixed bridge with reduction of measured pull-in voltage from 40 V to 35 V with similar dimensions where the length and width of the bridge are 550 µm and 50 µm respectively. Additionally, investigation on the warping effect due to stress on the bridges of the varactors has been conducted. This issue has lowered the down-state capacitance of the fabricated varactors compared to the simulated values.

Recently, wideband microwave medical applications are gaining a lot of attention among researchers in the microwave community. One of the challenges in the wideband microwave imaging is to design an efficient sensing antenna. To improve the performance of the antenna, a radical approach using phased array systems integrated with phase shifters is required. However, wideband phase shifters that could operate at low microwave frequency range needed for the medical imaging applications are very limited. Most of the commercial phase shifters in the market are

either narrow-band or are of constant-phase type which are not suitable for wideband phased array system. Therefore, it is necessary to develop phase shifters that can offer wideband characteristic at frequency range of 2 GHz to 4 GHz. Chapter 5 presents the design and simulation of a 2-bit and 3-bit DMTL phase shifters that can fulfil these requirements. The simulated maximum transmission loss of the 2-bit and 3-bit phase shifters are -1.6 dB and -2.94 dB respectively. The simulated phase shifts for the 2-bit design are 0º, 90º, 180º and 270º while the 3-bit phase shifter can provide 0º, 45º, 90º, 135º, 180º, 225º, 270º and 315º phase shifts. To minimise the size of the phase shifters, CPW transmission line is meandered where mitred CPW bends are applied to eliminate radiation loss. The effectiveness of the bends in the CPW transmission line is evaluated in terms of impedance matching and transmission loss. It has been observed that comparable performance is achieved for the meandered transmission line compared to the typical straight CPW configuration.

The fabrication of the 2-bit MEMS phase shifter presented in Chapter 5 is carried out as described in Chapter 6. Similar fabrication process for the MEMS varactors is adopted for the DMTL phase shifter. To eliminate the surface conduction layer formed between the HRS wafer and passivation layer, a 500 nm thick layer of polysilicon is grown on top of the silicon wafer before deposition of the passivation layer. A 300 nm thick aluminium metal is used for the centre conductor of the CPW transmission line instead of 2 µm thick proposed in the earlier design parameter to facilitate the construction of MEMS bridges with flat structure. The measured S_{11} signal for the phase shifter for all the states are less than -10 dB up to 6 GHz showing good impedance matching performance. For the phase shift performance, the maximum measured phase shifts for State 1, State 2, State 3 and State 4 are 0º, 17.89º, 34.51º and 52.39º respectively. This results is lower than the simulated designed phase shift. To investigate the reason behind this, the bridge structure is characterised and analysed. It is clear from the profiles of the bridge measured under an interferometer that the bridge warps over its width by 1 µm thus forming an air gap when it is in down-state position. This reduces the capacitance value required to provide the desired phase shifts. The measured transmission losses for all four states of the phase shifter at 2.45 GHz are -9.38 dB, -10.31 dB, -9.37 dB and -10.52 dB. The high measured phase shifter loss compared to the simulation results is mainly due to the skin depth

effect which comes from the use of 300 nm thick aluminium for the construction of the centre conductor of the CPW transmission line in the fabricated phase shifter. To verify this, the 2-bit DMTL phase shifter is simulated in the EM simulator where the thickness of the aluminium for the CPW line is changed to 300 nm. It is found that the simulation results show good match with the measurement results hence confirming the earlier assumption regarding the skin depth effect that causes the high loss in the fabricated phase shifter. Moreover, to investigate and optimise the loss of the CPW transmission line used in the DMTL phase shifter, several CPW transmission lines with different thickness and dimensions have been fabricated. To eliminate the surface conduction layer that formed between the HRS silicon substrate and passivation layer, two different methods have been performed. The first method is carried out by etching the passivation layer at the gap of the CPW transmission line to prevent current leakage. For the second method, a thin layer of polysilicon has been deposited between the silicon substrate and passivation layer to trap electrons from forming an electron charge layer which would increase the loss of the transmission line. It has been observed that deposition of polysilicon layer gives better performance where the loss of the transmission line can be reduced by 1 dB at 2.45 dB compared to the etched gap method. Moreover, from the measurement results, a 2 µm thick CPW transmission line with similar characteristic impedance, signal width and length of the fabricated phase shifter has transmission loss of -2.33 dB. Therefore, it is expected that similar phase shifter loss can be achieved if 2 µm aluminium is used in the fabrication of the phase shifter. Additionally, the loss of the CPW transmission line can be further improved by using centre conductor widths of 300 µm and 500 µm where the measured insertion loss are 0.169 dB/cm and 0.122 dB/cm respectively. This results show that a low-loss wideband DMTL phase shifter for low microwave frequency applications with loss less than 1 dB is feasible.

Overall, it is concluded that it is feasible to design tuneable MEMS devices using SU-8 based on the studies conducted in this thesis. It is expected that with better and optimised fabrication process, high capacitance ratio digital MEMS varactors for future wireless applications and low-loss DMTL phase shifters for phased array systems intended for wideband microwave medical imaging can be realised.

7.2 Summary of Contributions

This section summarises the research studies carried out in this thesis and the proposed solutions to address the challenges faced. In general, the research areas include design and simulation of high tuning range MEMS varactors, fabrication of a single-bridge MEMS varactor, design and simulation of digital DMTL phase shifters for low microwave frequency applications and fabrication of a 2-bit DMTL phase shifter which are discussed as follows.

7.2.1 Design and Simulation of a 4-bit and 5-bit High Capacitance Ratio Digital MEMS Varactors using SU-8.

One of the main contributions from the proposed digital MEMS varactor design is the use of SU-8 as a thick passivation layer to elevate the devices from the silicon substrate hence reducing the parasitic and fringing field capacitance. This technique is able to improve the capacitance ratio of the MEMS varactor over a similar MEMS varactor design without the SU-8 layer. Moreover, the thick SU-8 base layer can be used to fabricate MEMS varactors on a low-resistivity silicon substrate rather than the more expensive HRS wafer.

7.2.2 Fabrication of a Single-Bridge MEMS Varactor

A single-bridge MEMS varactor design has been successfully fabricated in this section. The design of this MEMS varactor is derived from the simulated multi-bit design with several modifications including the use of a single MEMS bridge instead of multiple bridges to reduce the complexity of the fabrication process. Nevertheless, it is noted that the fabricated devices are still able to validate the main features of the full devices. The main novelty of the device is the utilisation of SU-8 material to provide several functionalities in the fabrication of the MEMS varactor. Apart from reducing the fringing field capacitance, SU-8 also serves as an anchor and sacrificial layer for the varactor. As a result, the total fabrication steps required is reduced compared to the standard MEMS process using oxide as sacrificial material.

7.2.3 Design of a 2-bit and 3-bit Novel Wideband DMTL Phase Shifter for S-band Applications

One of the main components of phased array antenna systems is a phase shifter. In wideband microwave medical imaging applications, the use of a phased array antenna

could potentially improve the sensing and detection of the imaging system. Consequently, a phase shifter with wideband performance is needed for the wideband phased array antenna. Due to its wideband characteristic, a DMTL phase shifter is seen as the best candidate for this purpose. However, most of the available DMTL phase shifters in the literature operate mainly at high frequency range from 10 GHz up to 90 GHz. This is due to the main challenge in designing DMTL phase shifters for low microwave frequency band (below 4 GHz) that requires a long transmission line in order to provide sufficient phase shifts at the intended frequency band. In this thesis, a 2-bit and 3-bit DMTL phase shifters are proposed to function at operating frequency range of 2 GHz to 4 GHz which can be applied in many applications from radar to microwave medical imaging systems. This is the first attempt to design DMTL phase shifters to operate at this frequency range. Simulation results indicate that the phase shifters is able to provide phase shifts up to 270° and 315° for the 2-bit and 3-bit designs respectively. A 76.45 mm and 134.79 mm long CPW transmission lines are required for both designs. The maximum simulated transmission loss is -1.83 dB for the 2-bit DMTL phase shifter whereas -3.15 dB is achieved for the 3-bit configuration.

7.2.4 Fabrication of a 2-bit DMTL Phase Shifter

A successful fabrication of a 2-bit DMTL phase shifter is achieved in this thesis. 41 bridges are implemented in the phase shifter where all the bridges were completely released during the fabrication. A high yield of 90% is also achieved in the process. The bridges are actuated at 40V with no stiction problem observed during the measurements. Although the measured phase shifts and transmission losses differ from the simulated values, the main reasons for the discrepancies have been properly investigated and analysed.

7.2.5 Reduction of Pull-in Voltage of the MEMS bridge in the Proposed Varactor using Truss Bridge Structure

A new truss bridge structure is proposed in this study in order to reduce the pull-in voltage of the MEMS bridge in the proposed varactor. The measured pull-in voltage of the truss bridge is around 35 V where a reduction of 12.5% is achieved over the standard solid fixed-fixed bridge structure. This could potentially decrease the effect of dielectric charging which causes the bridge to permanently stick to the bottom electrode and therefore improving the reliability of the proposed varactors[95]–[99].

7.2.6 Characterisation of the Fixed-Fixed Aluminium Bridge deposited using Electron-Beam Deposition Technique.

The fixed-fixed aluminium bridge used in the phase shifter design has been characterised to investigate the effect of stress due to the fabrication process. The deposition of aluminium for the bridge was done using an electron-beam deposition method. It is found that the deposited bridge warps along its width direction which results in lower phase shift compared to the designed value. This is due to the formation of an air gap between the warped bridge and dielectric layer in the down-state position that reduces the capacitance of the varactor in the phase shifter. On the other hand, the bridge warps only by 1 µm over its length which is very promising for a bridge structure with 372 µm in length. Moreover, it is shown that by using 2 µm aluminium for the MEMS bridge, a flat structure can be obtained which would improve the performance of the phase shifter. It is concluded that the phase shift of the DMTL phase shifter can be greatly improved by addressing the stress issue experienced by the bridge.

7.2.7 Investigation on the use of thick aluminium for the CPW transmission line of the phase shifter

The measured transmission loss of the fabricated phase shifter is in the range of -9 dB to -10 dB. However, the high loss experienced by the phase shifter is mainly due to conductor loss considering that the device was fabricated using 300 nm thick aluminium instead of 2 µm aluminium specified in the simulation. The reason for opting thin aluminium in the fabrication process is to reduce the complexity of the process. Nevertheless, based on the fabrication conducted, it is found that it is feasible to build a DMTL phase shifter with high number of bridges where all the bridges in the fabricated phase shifter have been successfully released and actuated. To give better estimation of what would be the transmission loss of the phase shifter if thicker aluminium and a CPW transmission line with wider centre conductor are used, several variations of CPW transmission lines with the same characteristic impedance to that of the transmission line used in the fabricated phase shifter have been fabricated and measured. By using a 2 µm CPW line with the same configuration and length to that of the fabricated phase shifter, the measured transmission loss of -2.6 dB is achieved which a significant improvement over the loss is obtained in the phase shifter using

300 nm aluminium. Moreover, the loss of the CPW transmission line can be reduced up to 0.122 dB/cm for a centre conductor width of 500 µm. This could result in a DMTL phase shifter with a loss of less than 1 dB that can operate at low microwave frequency range.

7.3 Future works

There are several improvements that can be made to the studies reported in this thesis which are listed and discussed as follows.

7.3.1 Improving the adhesion between SU-8 and silicon oxide

One of the main issue in realising high tuning ratio varactors as proposed in the research is the adhesion problem between SU-8 and silicon oxide. Based on the method suggested in [77], a similar approach was carried out to improve the adhesion between these two layers by treating the surface of the SU-8 layer using oxygen plasma. However, it was found out the adhesion issue still persists which led to the use of SU-8 as the sacrificial layer instead of silicon oxide. Although the proposed method was able to mitigate the problem, a detailed investigation should be carried out in the future to address this subject. In [100], a new method was presented to characterise the adhesion of SU-8 using surface acoustic wave (SAW) sensors. By employing this technique in future work, accurate adhesion model between SU-8 and silicon oxide can be first developed. Then, a new technique can be developed to improve the adhesion issue. Recently, a modified RF plasma method has been proposed in [101] to improve the adhesion strength of SU-8 for metals. The RF plasma is made up of oxygen where the treatment process was carried out at a power of 25 W and at a pressure of 3×10^{-3} Torr. Therefore, to improve the adhesion between SU-8 and silicon oxide, several parameters of the treatment process can be varied to obtain the desired performance. A part from this technique, a new method using additional layer can be implemented to create an adhesion layer between SU-8 and oxide to create a strong bond. Based on the research presented in[102], a strong bond between SU-8 and PDMS has been realised using aminosilane-mediated irreversible bonding method. In [103], it has been reported that the adhesion between silicon oxide deposited by plasma-enhanced chemical vapour deposition and polydimethylsiloxane (PDMS) was

greatly improved using the surface functionalisation of injection moulded polypropylene. Thus, based on these studies, the use of adhesion layer in such as PDMS could create a strong adhesion layer to bond SU-8 and silicon oxide.

7.3.2 Development of a new low-cost varactor design with enhanced performance

In this thesis, the high tuning ratio of the proposed fixed-fixed MEMS varactors was achieved by creating a thick passivation layer with low dielectric constant using SU-8. Due to the implementation of the SU-8 layer, the fringing field which is caused by the interaction between the MEMS varactors and the silicon substrate has been reduced compared to a typical design without the passivation layer. However, there are many other aspects of the design that need to be addressed for commercialisation purpose. One of the issue is the cost associated with the fabrication of the devices. In order to reduce the cost, new fabrication processes and materials could be investigated. Recently, a low-cost microfabrication technique has been proposed in [104] to build RF switches and varactors where the whole fabrication process utilises only laser micro-structuring technique, standard wet-bench, non-clean room microlithography and hot-film emboss of SU-8 and ADEX polymers. For the proposed MEMS devices, a low-cost FR-4 has been used as a substrate compared to more expensive high-resistivity silicon which is typically used in RF MEMS devices.

One of the limitations of the proposed varactors in this work is that the capacitance values are fixed due to the used of two-state switches design. There are many applications that require continuous capacitance value such as voltage controlled oscillators (VCO). A broad analog tuning range MEMS varactors has been presented in[105]. By embedding the MEMS varactor in the back end of line (BEOL) metallisation stack of a state-of-the-art Si/SiGe BiCMOS semiconductor process, an overall capacitance ratio of 2.4:1 has been achieved. Hence, a similar approach could be pursued in the future where the varactors can work in both modes; digital and analog.

7.3.3 Realisation of a flat MEMS bridge for the proposed MEMS devices

The main reason for the low measured capacitance and phase shift from the fabricated MEMS varactor and DMTL phase shifter is due to the warping of the bridge utilised

in the devices over its width, causing a formation of an air gap during its down-state position. Based on the analysis and initial work presented in the thesis, this issue could be rectified by using a thicker bridge construction for the realisation of a flat bridge structure. This would eliminate the air gap formed between the bridge and dielectric layer which will increase the capacitance of the varactor and therefore increase the phase shift of the fabricated phase shifter. To carry out the process using thick metal structure, a better understanding of stress-strain relationship of the deposited aluminium must be first established. As presented in [106], the effect of geometrical dimensions of free-standing MEMS structures made from electroplated gold was analysed and studied in details. This study is crucial in order to find the main cause of the stress before any prevention methods could be applied. Hence, in the future, a similar approach should be carried out to address the low capacitance effect due to stress issue experienced by the aluminium beam. Another method that can be utilised to realise a flat bridge is to use different metal such as gold. A capacitive RF MEMS switch has been realised using gold as the free standing structure in [107]. The thickness of the gold bridge is 1 µm which has the same thickness as the aluminium bridge used in this research. Moreover, the bridge was also released using oxygen plasma process although the sacrificial layer is AZ6130 positive photoresist compared to SU-8.

7.3.4 Fabrication of the MEMS devices using thick metal process

One of the main challenges in fabricating RF MEMS devices is the need for thick metal structure to reduce the conductor loss due to the skin depth effect. To address this issue, a thick CPW transmission line is required in the phase shifter where it has been observed that by using 2 µm aluminium, the transmission loss of the transmission line can be improved to -2.6 dB. Moreover, the loss can be further improved by utilising a CPW transmission line with a wide centre conductor configuration. Future research will involve further optimisations in both the design and fabrication of the DMTL phase shifter to facilitate the proposed suggestions in order to realise a low loss DMTL phase shifter that is able to operate at low microwave frequency range.

7.3.5 Packaging of the MEMS Device

For future use, the devices need to be packaged for integration with other RF components and to ensure its reliability. The overall cost associated with the packaging must be low in order for the MEMS devices to be mass-manufactured and therefore be available at a reasonably low price to compete with the existing competing devices in the market.

7.4 Final Comment

This research paves the way for the realisation of tuneable MEMS devices namely digital MEMS varactors and DMTL phase shifters for wide range of applications ranging from wireless communications to microwave medical imaging systems. The utilisation of SU-8 polymer in the construction of the MEMS devices offers many advantages such as increased tuning ratio, capable of forming a permanent structure in the devices and to facilitate the release of the MEMS structures. The proposed MEMS devices presented in this thesis will facilitate the development of compact, tuneable and wideband RF systems in wide range of applications in the future.

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