THE UNIVERSITY *of* EDINBURGH

Time Domain CMOS ISFET Systems for pH Sensing

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A thesis submitted in partial fulfilment of the requirements for the degree of

DOCTOR OF PHILOSOPHY

The University of Edinburgh

April 2023

Declaration of Originality

I declare that this thesis was composed by myself, that the work contained herein is my own except where explicitly stated otherwise in the text, and that this work has not been submitted for any other degree or professional qualification except as specified.

Part of this work has been published in [1].

Jose Cortes-Guzman
April 2023
Edinburgh, UK

Acknowledgements

The conclusion of years of work on this thesis is one more chapter that I have the pleasure to complete, and it only became a reality thanks to the kind support and help of many individuals and organisations. To all of them, I extend my greatest recognition.

I would like to express my gratitude to my supervisor Srinjoy Mitra, whose guidance, vision and support were vital during my PhD. Despite the obstacles we faced, his encouragement, leadership and mentoring allowed me to perform world-class research to create the foundations for future research. A greater acknowledgment to my co-supervisor David R. S. Cumming for giving me the opportunity to work in this challenging and exciting PhD project.

I would also like to thank Dr Andreas Tsiamis, who provided fundamental guidance, training and technical support for the post-processing work within the cleanroom. His years of experience and knowledge on the topic were a major advantage and were vital to completing my studies.

I want to also thank the people who helped me with the training and technical support during my studies in the SMC: Andrew Bunting, Peter Lomax, Stewart Ramsay, Camelia Duran and Ewan Macdonald, as well as Dr Thomas Glen, who was the instrument scientist at the time, managing the Cryo FIB/SEM equipment from the School of Physics and Astronomy. I also thank my friends and colleagues for their time, encouragement and knowledge that allowed us to work together during our studies.

I want to acknowledge my parents, Guadalupe Cortes and Telma Guzman, for being the strength I always needed. Their sacrifices, support and love throughout my life, particularly during this period, have made them the greatest inspiration, and I am honoured to have them with me on this journey. This work is theirs as much as it is mine. My gratitude also goes to my brothers, Jordan and Bryan, for their support and time in encouraging me to follow my dreams.

My journey would not have been a reality without a few more people who I should thank. First, Prof. Agustin Carvajal and Dr Jose Gomez, who introduced me to the area

of specialisation I am interested in, instilled their passion for science in me and supported me through this journey; Diana, whose love, support and admiration were the main drive that motivated me to take this path; and my friends Deneb, Paola, Ale, Maria Jose and Jorge, who are part of my closest circle and gave me their love and support whenever I needed it.

I want to also thank CONACyT, the I^2T^2 and the CDT in Sensing and Measurement for their economic and administrative support through my PhD. Thanks for believing in this project, which now comes to an end.

Finally, I would like to dedicate this work to those who are no longer with us. Unfortunately, life did not allow us to enjoy this path together. Still, you will always be in my thoughts: my grandmother Maria de la Luz Peña Lozano, my great grandmother Geronima Guel Cuellar, and my dearest friend Antonio Zaachila. This is for you.

Abstract

In recent years, there has been a focus on integrating and miniaturising complementary metal-oxide-semiconductor (CMOS) electrochemical sensors, particularly ion-sensitive field-effect transistors (ISFETs), for applications in healthcare and environmental monitoring. However, CMOS-based ISFETs do not always show stable behaviour, and their interface circuits are not suited to supply voltage variation. This work aims to develop a stable platform for sub-pH detection by addressing these challenges.

This work presents two front-end architectures for pH signal frequency conversion, suitable for low supply voltage and pH-sensing arrays. These circuits offer nonlinear and linear responses to pH changes, with a focus on the linear version. CMOS post-processing steps are used to further improve the sensitivity in the sensing area. The linear pulse frequency modulator (LPFM) architecture exhibits the best outcome in long-term response against pH variations and a highly stable signal with up to 25% variation in the power supply range. This could be a very significant feature for implantable and other wireless applications.

Two data acquisition techniques are employed to increase long-term stability: the standard ‘Static Method’ and a ‘Dynamic Method’ using a pulsed reference signal. The Dynamic Method outperforms conventional techniques, addressing the common issue of the rapid pH signal decay in the time domain measurements evaluated in this work.

Lay Summary

Electrochemical sensors play a significant role in today's biomedical and environmental applications. These sensors help us comprehend and interact with the world around us by providing valuable insights into the composition of substances and their respective chemical processes. Whether measuring pH levels in a lake to monitor its toxicity or detecting glucose levels in the blood to manage diseases like diabetes, these sensors can significantly improve our lives.

Recent advances in this area have been driven by the increasing demand for portable, affordable and accurate devices for various applications, including environmental monitoring, medical diagnostics and food safety, among others. This work provides a review of the technology and proposes an electronic architecture in CMOS technology using ISFETs as pH sensors to develop a platform with high sensitivity, stability and repeatability that can overcome some of the major challenges present in these devices.

Electrochemical sensors allow us to see the invisible and understand the unknown in many applications, and they can have a fundamental impact in countless industries and fields. These sensors are shaping our future and are close to guaranteeing a significant improvement in people's quality of life around the globe.

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Abbreviations and Acronyms

V_{abs}	Absolute Potential of the Standard Hydrogen Electrode
T	Absolute Temperature
AER	Address-Event Representation
Al_2O_3	Aluminium Oxide
A	Area
ALD	Atomic Layer Deposition
AMS	Austria Microsystems
BEOL	Backend-of-the-Line
BCD	Bipolar CMOS DMOS
k	Boltzmann Constant
V_{cap}	Capacitor Voltage
CF_4	Carbon Tetrafluoride
CVD	Chemical Vapour Deposition
CMOS	Complementary Metal Oxide Semiconductor
γ	Constant Chemical Term
CVCC	Controlled-Voltage Controlled-Current
DI	Deionised Water
DNA	Deoxyribonucleic Acid
C_d	Depletion Capacitance
DRC	Design Rules Check
DC	Direct Current
K_a	Dissociation Constant for Deprotonation
K_b	Dissociation Constant for Protonation
DPI	Dots per Inch
V_d	Drain Voltage
DIL	Dual-in-line
DMO	Durham Magneto Optics
E	Effective Division of the Surface Potential due to the Oxide,

	Depletion and Passivation Capacitances
$V_G^{"}$	Effective Gate Voltage
C_{eq}	Equivalent Capacitance
EDL	Electrical Double Layer
EIS	Electrolyte-Insulator-Semiconductor Interface
χ_e	Electrolyte-Insulator Surface Dipole Potential
EMI	Electromagnetic Interference
q	Electron Charge
EDS/EDX	Energy Dispersive X-Ray Composition
ED	Event-Drive
FET	Field-Effect Transistor
V_{FB}	Flat-band Voltage
FIB	Focused Ion Beam
ε_0	Free Space Permittivity
V_{GC}	Gate Capacitor Voltage
V_g	Gate Voltage
GB	Gigabytes
C_{Gouy}	Gouy-Chapman or Diffuse Layer Capacitance
HfO_2	Hafnium Oxide
C_{Helm}	Helmholtz Layer Capacitance
HDMS	Hexamethyldisilazane
HDP	High Density Plasma
V_H	High Voltage
HCl	Hydrogen Chloride
S_n	Ideal Sensitivity
IHP	Inner Helmholtz Plane
C_i	Insulator Capacitance
Q_i	Insulator Effective Charge per Unit Area
IC	Integrated Circuit
β_{int}	Intrinsic Buffer Capacity
ISFET	Ion-Sensitive Field-Effect Transistor
V_{ISFET}	ISFET Voltage

JWNC	James Watt Nanofabrication Centre
LVS	Layout Versus Schematic
LCC	Lead/Leadless Ceramic Chip Carriers
LED	Light Emitting Diode
LPFM	Linear Pulse Frequency Modulator
$\boldsymbol{\varphi_{lj}}$	Liquid-Function Potential Difference between Reference Solution and Electrolyte
$\mathbf{V_L}$	Low Voltage
MB	Megabytes
$\mathbf{C_{mem}}$	Membrane Capacitor
MET	Metal
MOS	Metal Oxide Semiconductor
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MEK	Methyl-Ethyl Ketone
MS	Mixed Signal
MPW	Multi Project Wafer
NMOS	N-Channel Metal Oxide Semiconductor
$\mathbf{N_2}$	Nitrogen
NPFM	Nonlinear Pulse Frequency Modulator
NSF	Noise Scale Factor
$\boldsymbol{\delta_\chi}$	Number of Variations of χ Potentials
OTA	Operational Transconductance Amplifier
OHP	Outer Helmholtz Plane
$\boldsymbol{F_{out}}$	Output Frequency
$\mathbf{V_{out}}$	Output Voltage
$\mathbf{C_{ox}}$	Oxide Capacitance
$\mathbf{O_2}$	Oxygen
$\mathbf{A_{pass}}$	Passivation Area
$\mathbf{C_{pass}}$	Passivation Capacitance
$\boldsymbol{S_{pH}}$	pH Sensitivity
PVD	Physical Vapour Deposition
PECVD	Plasma Enhanced Chemical Vapour Deposition

PVC	Polyvinyl Chloride
KCl	Potassium Chloride
$\boldsymbol{\psi_0}$	Potential Drop in the Electrolyte at the Insulator-Electrolyte Interface
pH	Potential of Hydrogen
$\boldsymbol{\varphi_{eo}}$	Potential of the Electrolyte-Insulator Interface
PSD	Power Spectral Density
VDD	Power Supply
PSRR	Power Supply Rejection Ratio
PCB	Printed Circuit Board
PGMEA	Propylene Glycol Methyl Ether Acetate
PFM	Pulse Frequency Modulation
PWM	Pulse Width Modulation
RF	Radio Frequency
RIE	Reactive-Ion Etching
$\mathbf{V_{ref}}$	Reference Electrode Potential
$\mathbf{V_{rel}}$	Reference Electrode's Potential Relative to the Hydrogen Electrode
REFET	Reference Field-Effect Transistor
$\boldsymbol{\varepsilon_r}$	Relative Permittivity
RST	Reset
RC	Resistor-Capacitor Circuit
$\mathbf{RuO_2}$	Ruthenium Oxide
G	Scaling Factor
SEM	Scanning Electron Microscope
SMC	Scottish Microelectronics Centre
RS	Set-Reset
Si	Silicon
$\mathbf{SiO_2}$	Silicon Dioxide
ϵ_{SiO2}	Silicon Dioxide Permittivity
$\mathbf{Si_3N_4}$	Silicon Nitride
ϵ_{Si3N4}	Silicon Nitride Permittivity
Ag/AgCl	Silver/Silver Chloride

NaOH	Sodium Hydroxide
SF	Source Follower
V_s	Source Voltage
SF_6	Sulphur Hexafluoride
σ_{Ox}	Surface Charge Density
N_S	Surface Site Density
TSMC	Taiwan Semiconductor Manufacturing Corporation
Ta_2O_5	Tantalum Pentoxide
V_T	Thermal Voltage
3D	Three Dimension
V_{thres}	Threshold Voltage
TiN	Titanium Nitride
TiO_2	Titanium Oxide
UV	Ultraviolet Light
ΔV	Voltage Range
V-to-I	Voltage to Current
ϕ_{Si}	Work Function of the Metal Gate (ref. electrode) Relative to Vacuum
ZnO	Zirconium Oxide

The work presented in this thesis was manufactured in two different CMOS Chips: CMOS-V1 and CMOS-V2. CMOS-V1 contained the NPFM-V1 circuit and was used for the Ta_2O_5 deposition process, while CMOS-V2 had the NPFM-V2 circuit (improved version) and the LPFM circuit and was used for the thinning passivation process.

Chapter 1

Introduction

The need for precision health care and monitoring environmental threats has pushed the scientific industry to seek technological improvements to develop devices at low cost and high performance. Since the invention of the semiconductor transistor, research for biomedical, environmental and industrial applications has been exploited to create novel technologies for different purposes, like glucose monitoring, detection of water contamination, and in-line control of gas mixtures, among others [2].

1.1 Motivation

In recent decades, the semiconductor industry has been working on developing integrated systems capable of providing high performance at high speed, low cost and low power consumption for applications in telecommunications, healthcare and intelligent systems. Until recently, the development of integrated circuits (IC) had been dictated by Moore's Law, which establishes a correlation between the number of transistors on a chip and the time it takes for the industry to reach them [3]. However, more promising More-than-Moore technologies and integration systems are emerging that have potential advantages over the existing technology.

One of the applications that have been exploited is the fabrication of large arrays of ISFETs used in the Ion Torrent and Ion Proton DNA sequencing systems [4]. An ISFET is an electrochemical sensor used to measure ionic concentrations of hydrogen in a solution. This sensor requires a reference electrode, which provides a stable and well-known potential that controls the device's conductance, determining its active or saturation stage. It is commonly made of silver/silver chloride (Ag/AgCl) [5]. Bergveld developed this device more than 40 years ago [6]. Since its inception, researchers have tried to exploit its benefits, mainly its high sensitivity, and improve its limitations as a chemical sensor to develop novel applications.

ISFETs have become particularly relevant in the last couple of decades since they can be used as a sensing platform for multiple applications, from environmental monitoring, like water contamination, food waste and soil sampling, to point-of-care and biomedical applications, like deoxyribonucleic acid (DNA) sequencing, pH monitoring, and a variety of biosensors for healthcare. This device's inherent advantages include its miniaturisation capabilities, large-scale integration and cost-effectiveness [7]. These types of sensors can be designed as ion sensors, electrochemical sensors, biosensors, and wearable sensors, depending on the practical applications of each proposed design. A summary of ISFET applications is presented in Figure 1.1.

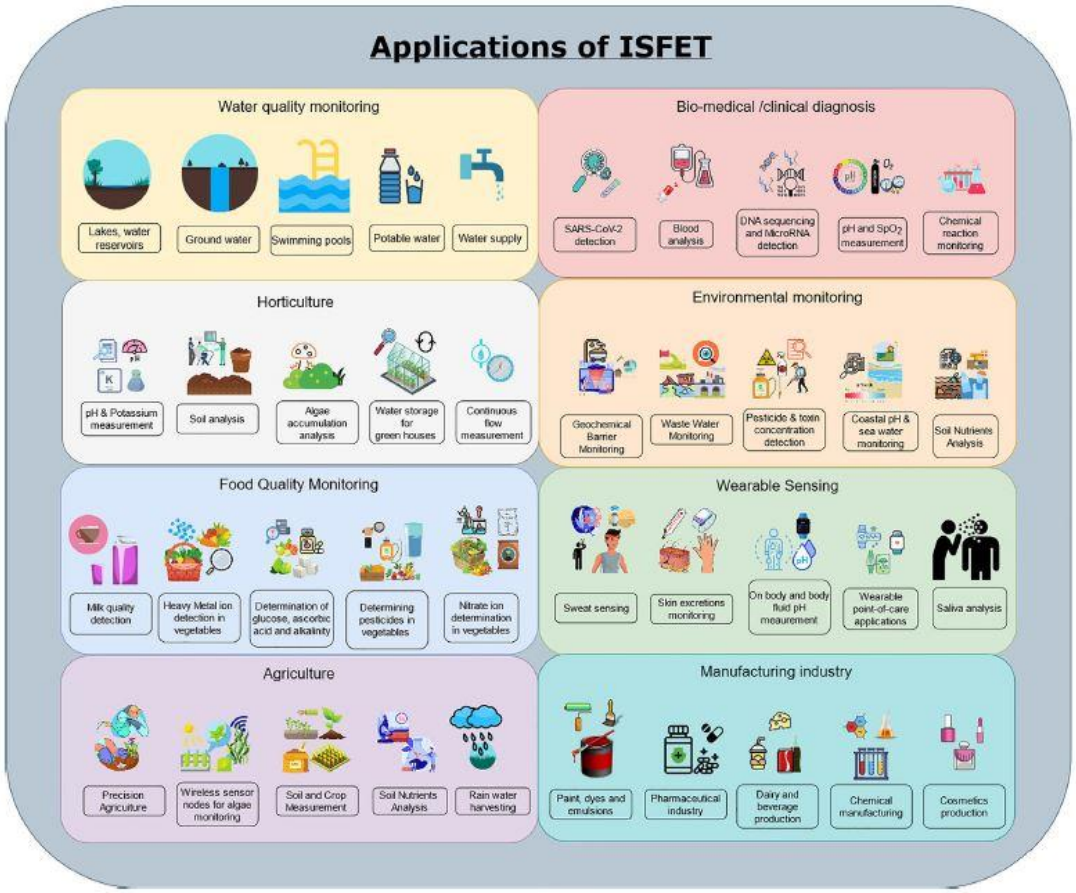


Figure 1.1 ISFET's applications [8].

However, these devices have shown fundamental challenges, needing improvement in their current designs to overcome some or all of them. These challenges include noise corruption, capacitive attenuation, drift, light sensitivity, trapped charge and thermal

dependence. The current literature provides some solutions that include complex circuit architectures [9], but better instrumentation is still needed to take full advantage of its benefits as an electrochemical sensor. This is even more necessary if more advanced applications are intended to work (like wearable and implantable devices for healthcare monitoring, as shown in Figure 1.2) for a long time, under unreliable power supplies and in large arrays.

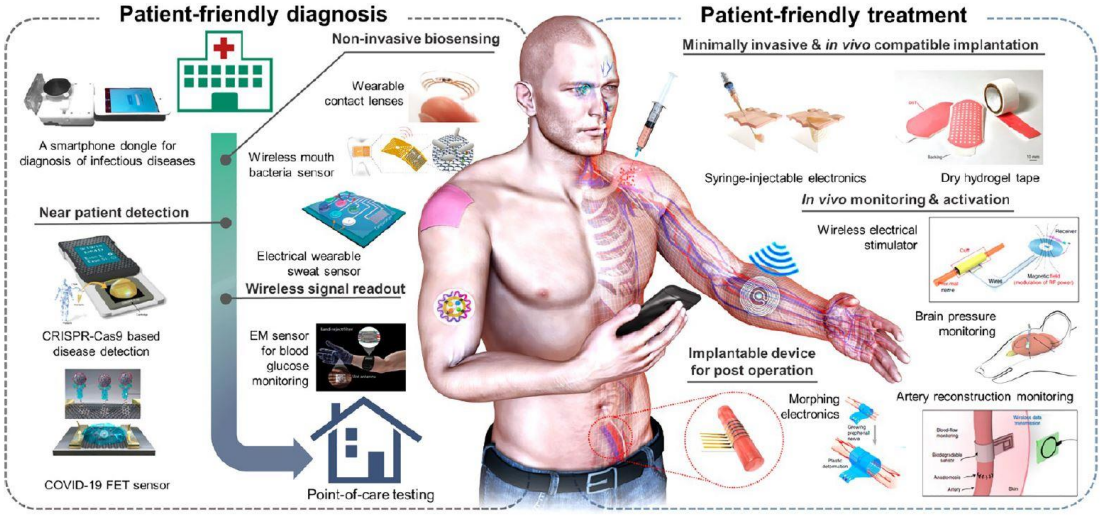


Figure 1.2 Biomedical devices for implantable applications [10].

1.2 Research Objectives

This research seeks to develop a microchip capable of monitoring pH for environmental or biomedical applications by fabricating ultra-small size, ultra-low power sensors. The main objective is to create a front-end architecture that can accurately sense pH variations by overcoming some of the main challenges presented in ISFET technology. The work in this thesis involved both instrumentation designs and microfabrication processes to achieve a reliable and acceptable outcome in terms of sensitivity, accuracy, repeatability and stability.

This research aims to develop a sensing platform with this front-end architecture that can be functionalised to work with environmental applications, such as food waste or water contamination, and healthcare applications for personalised medicine, such as chronic disease monitoring through the sensing of metabolites in implantable devices. This research focuses on developing the technology to transduce multiple pHs into

readable signals by fabricating CMOS designs that can then be functionalised to create sensors for various applications.

The specific objectives of the research are the following:

- Chip Design
    - Develop ISFET front-end architectures that can overcome some of the main challenges of the technology, like electronic transient noise, capacitive attenuation, light sensitivity and drift, as well as giving added benefits compared to other designs in terms of sensitivity, repeatability and power consumption.
    - Simulate and characterise the proposed ISFET front-end architectures with accurate ISFET chemical models using high-level simulation software.
    - Generate the IC layout of the proposed CMOS chips, considering factors like floor planning and placement optimisation for a specific area under 5 µm x 5 µm. Perform design rule check (DRC), layout versus schematic (LVS), and parasitic extraction tests for the verification process.
- Chip Post-processing
    - Test different sensing layers for sensitivity improvement using post-processing techniques for their deposition and thin the original passivation layer for the technologies used to manufacture the Ics.
- Chip Packaging
    - Develop hermetic packaging to ensure the device's correct functionality under solution and prevent potential damage.
- Chip Analysis
    - Characterise the microchip to get information about the signal's linearity, sensitivity, power consumption and stability.
    - Verify the stability of the output signals in wet conditions using pH buffers by performing long-time measurements to evaluate their behaviour over time and compare them to the simulated results to analyse their behaviour.

1.3 Contribution to Knowledge

In this study, integrated CMOS sensor architectures were developed as a single sensing platform to detect pH changes using pH-to-frequency transduction in two different designs. Using the frequency domain to evaluate pH change, the architectures showed several advantages over the more conventional designs presented in the literature. Nonlinear and linear versions of a pulse frequency modulator (PFM) were developed and characterised to reflect their advantages and disadvantages in comparison to the conventional architectures.

The LPFM was the design that showed the best features, as it provides a robust digital output of a fixed duty cycle and variable frequency, allowing the dynamic range to increase. The system can also get a steady response even with a 25% power supply variation, which is of particular interest for implantable applications. The work presented here showed minimal electronic transient noise in simulation (different from electrochemical noise corruption), and an average standard deviation of 567 Hz between pH values, demonstrating its capability for detecting even sub-pH levels. This design showed a linear response to simulated pH changes and a low-power consumption of 144.2 μW, making it a potential sensing platform for the next stage of the project.

This architecture has been tested for a wide range of pH values using an alternative method that eliminates the long-term drift issue in the standard measurement setups. The frequency peaks were detected every minute to acquire a representative signal that shows good consistency for the time domain (pH-frequency) signals. Using Taiwan Semiconductor Manufacturing Corporation (TSMC) technology, the design demonstrated consistent frequency peaks for a wide range of pH values.

1.4 Thesis Overview

Despite the advances that have been made in terms of ISFET instrumentation for pH detection, some of the main challenges remain, and solutions have yet to be proposed, with no single design that can overcome most of them. This thesis surveys the work done over the years and proposes a CMOS sensing architecture that shows low

electronic transient noise, high sensitivity, repeatability and low drift, overcoming some of the main challenges in this technology. The subsequent chapters are divided as follows:

Chapter 2 provides an overview of the state of the art in environmental and biomedical microsystems using ISFETs. First, it briefly describes the operation of an ISFET sensor, the chemical interaction behind the detection, and the current challenges present in these sensors. Next, simulation models are described together with a summary of different ISFET instrumentation to highlight their main advantages and disadvantages. Finally, it describes the post-processing work regarding the sensing layers used in CMOS technology and the leading applications in healthcare, environmental monitoring and the food industry.

Chapter 3 describes the front-end architecture of two proposed designs in two different CMOS chip tape-outs. The designs comprise the block diagram and transistor-level designs, the circuit simulation results, the layouts, and the electrical characterisation of both architectures. This chapter also includes the reasoning behind the contribution and challenges present in testing the designs in terms of the expected electrical response.

Chapter 4 includes the different post-processing work made on the surface of the CMOS chip to improve the actual chemical interaction and subsequent electrochemical response based on the literature, as well as some of the main challenges entailed in the process. The CMOS chips underwent a tantalum pentoxide layer coating and passivation thinning to characterise the device's sensitivity at different passivation thicknesses. An encapsulation process was also tested as part of the post-processing work to make it suitable to work under solution for long periods.

Chapter 5 presents the final electrochemical testing using the designed CMOS chip under different conditions and pH solutions to characterise its sensitivity, reproducibility, reliability and accuracy using different single chips. This chapter describes the setup configuration, different types of testing and a distinct way of taking a measurement considering the challenges present during the testing period.

Finally, ***chapter 6*** summarises the main findings of this thesis, as well as suggesting potential future work based on the literature and the author's experience with the current technology.

1.5 Publications Arising from the Research

During this research, the following conference paper was published and submitted:

Conference paper:

1. J. Cortes-Guzman, A. Tsiamis, D.R.S. Cumming, and S. Mitra, " Linear Pulse-Frequency Modulator ISFET with a Wide Supply Range," in IEEE Sensors, pp. 1-4, Dec. 2021, doi: 10.1109/SENSORS47087.2021.9639752.

A journal paper is also in progress based on the results of the electrochemical characterisation of the front-end architecture presented in the conference paper, extending the knowledge and ongoing research for developing novel instrumentation for pH sensing applications. The journal paper with the name 'A Linear Pulse-Frequency Modulator ISFET with Dynamic Reference Switching' is under internal review.

Chapter 2

ISFETs for Environmental and Biomedical Microsystems

2.1 Introduction

Bergveld first presented the concept of an ISFET in 1970 [6]. This signalled the beginning of a new biochemical sensor, which was first used to measure ionic concentrations and potentials around a nerve, opening up the possibility of electrophysiological measurements as the future of this device. Since then, ISFETs have been studied extensively due to their potential scalability and compatibility with CMOS technologies, making them excellent candidates for developing biosensors that can be used in several research fields. Thus far, large-scale integration of these sensors as microarrays has been successfully demonstrated for different applications, such as ion imaging, DNA amplification, biomolecule and DNA detection, DNA sequencing, drug discovery, water, soil and food assessment.

These devices have quickly drawn attention due to their ability to be built on an IC. They have been used as biochemical sensors by extending the metal gate of a regular MOSFET with a permeable membrane to ions. However, several factors discussed in this chapter affect the device's performance due to its inherent interaction with a solution. Over the last few decades, research groups have studied and developed microfabrication techniques and instrumentation to improve ISFET performance regarding sensitivity, stability and durability. Numerous efforts have been made to improve their performance, including novel instrumentation designs and new post-processing sensing layer materials to enhance the sensitivity and overcome some of the common challenges present in these devices. Unfortunately, despite the extensive research into improving ISFET devices, the literature still needs more detailed information about the integration of these sensors in CMOS chips, their long-term usage and characterisation techniques.

The following sections discuss the current literature on ISFET devices, from their principle of operation, common challenges and simulation models to the latest instrumentation and sensing layers researched in commercial CMOS ISFET devices. Finally, the chapter ends with the most promising ISFET applications to provide a comprehensive review of important aspects of these devices.

2.2 ISFET Microsensor

Due to their ability to transduce a chemical signal to an electrical one, ISFETs are potentiometric devices tied with an integrated reference electrode [11]. More than 50 years have passed since their introduction, but in the last two decades, they have become very popular for various scientific applications. The following sections will describe the concept of an ISFET, as well as the most common challenges presented in the literature over the years.

2.2.1 ISFET Operation

ISFETs originated with field-effect transistor (FET) devices, which were first presented by Lilienfeld in 1926 [12]. Different types of FET devices depend on the structure of the gate. The metal oxide semiconductor field-effect transistor (MOSFET) technology is the most valuable for the semiconductor industry due to its advantages of low cost, easy fabrication, and large-scale integration over other FET devices [13]. A MOSFET's basic structure consists of three terminals: a source, a drain and a gate. To establish the source and drain, specific silicon regions are doped with an opposite-type impurity, typically P-type for N-channel MOSFETs, employing ion implantation or diffusion techniques. The channel, located between these regions, is typically lightly doped. Subsequently, an annealing process activates and uniformly distributes dopant atoms in the silicon wafer. A thin insulating layer, often SiO_2, is grown or deposited on the wafer, and the gate terminal is created by depositing a conductive material, typically aluminium or polysilicon, onto this gate oxide layer [14]. MOSFET operation centres on manipulating the channel's conductivity between the source and drain. By applying a voltage to the gate, an electric field is created within the channel, influencing charge carriers (electrons or holes) and controlling

current flow between the source and drain. These MOSFETs can be categorised as N-channel or P-channel types [15].

An ISFET was proposed by removing the metal gate of the metal oxide semiconductor (MOS) structure to create direct contact between a solution and the oxide to detect concentrations of ions, and a further sensing film was then immobilised in the surface to form the actual structure of the device. Therefore, an ISFET follows the same electrical principle as a MOSFET. The main difference is that the gate is exposed and immersed in a solution instead of directly connecting to an electrical pad [16]. The ISFET requires the gate to be covered with an insulating membrane that allows for the formation of an interface potential between the surface and the electrolyte. The applied electrical potential generates an electrical field in the gate, which controls the amount of charge in the channel and, therefore, the conductivity between the drain and source [17]. This potential is provided by an external reference electrode, which can be defined as a solid electric conductor through which an electrical current flows into a non-metallic medium, such as an electrolyte, serving as the location where the oxidation-reduction equilibrium is established, These electrodes, commonly made of a combination of a metal wire coated with a layer of solid metal chloride and immersed in a saturated filling solution, provide a stable and well-known electrode potential, and some of them are widely used because of their low cost of fabrication, particularly the Ag/AgCl electrodes [18]. Figure 2.1 shows a cross-sectional view comparison between a MOSFET and an ISFET device.

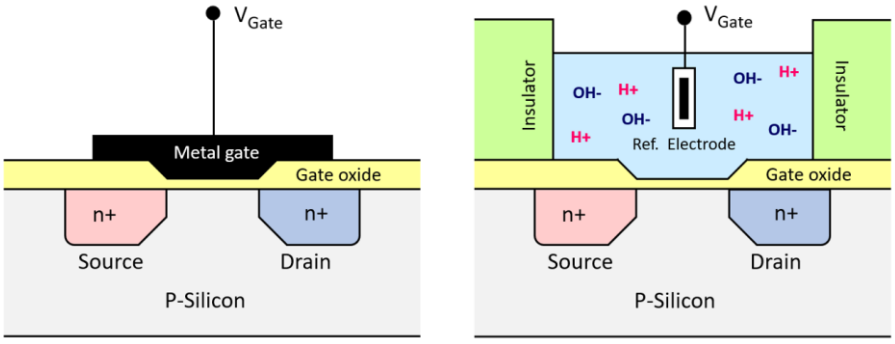


Figure 2.1 Cross-sectional view comparison between a MOSFET and an ISFET device [16].

The interaction between the gate oxide and the solution through the sensing membrane generates a shift in the threshold voltage caused by the ionic concentration in the

electrolyte. This threshold voltage can be represented by combining the physics of a MOSFET with the electrochemical properties of the insulator surface governed by the site-binding theory for ions and the Stern model, which describes a capacitive double layer formed by the Helmholtz and Gouy-Chapman layer [19], concepts detailed in the following section. Therefore, the threshold voltage of an ISFET can be expressed as follows:

$$V_{thres\,(ISFET)} = V_{thres\,(MOSFET)} + V_{ref} + \varphi_{lj} + \chi_e - \varphi_{eo} - \frac{\phi_{Si}}{q} \tag{1}$$

where V_{ref} is the potential of the reference electrode, which is equal to V_{rel} (potential of the reference electrode relative to the hydrogen electrode) plus V_{abs} (absolute potential of the standard hydrogen electrode), φ_{lj} is the liquid-function potential difference between reference solution and electrolyte, χ_e is the electrolyte-insulator surface dipole potential, φ_{eo} is the potential of the electrolyte-insulator interface, ϕ_{Si} is the work function of the metal gate (ref. electrode) relative to vacuum, and q is the charge of an electron [20].

From this set of mathematical parameters, the one responsible for the pH sensitivity is φ_{eo}, which can be expressed as:

$$\varphi_{eo} = S_{pH} * \left(pH_{pzc} - pH_{ref}\right) \tag{2}$$

where S_{pH} represents the pH sensitivity, defined as follows:

$$S_{pH} = -\ln(10) * \frac{kT}{q} * \alpha \tag{3}$$

where $kT\ /\ q$ is the thermal voltage V_T, and α is a scaling factor from 0 to 1 to define the sensitivity from the ideal Nernstian response ($59mV\ /\ pH$), which corresponds to a scale of 0.95 [21]. This scaling factor depends in turn on:

$$\alpha = \frac{1}{\frac{\ln(10) * kT * C_{eq}}{q^2 * \beta_{int}} + 1} \tag{4}$$

where C_{eq} is the equivalent capacitance, also called the differential capacitance or the capacity of the electrolyte to store electric charge in response to a modification in the

electrostatic potential, and β_{int} is the intrinsic buffer capacity, or the change in the number of charged groups as a result of an infinitesimal increase in pH [22].

However, the equation for the threshold voltage of an ISFET can be rearranged as follows:

$$V_{th(ISFET)} = V_{th(MOSFET)} + V_{ref} + \gamma + \alpha * S_n * pH \tag{5}$$

where γ is a constant chemical term composed by the interactions defined above, S_n is the ideal sensitivity of 59 mV/pH, pH is a measure of how acidic or basic water is depending on the concentration of hydrogen ions in a solution ($= -log_{10}([H^+])$, and α is the sensitivity deviation caused by the double layer capacitance [23], which can be calculated as an equivalent capacitor:

$$C_{eq} = \frac{C_{Gouy} * C_{Helm}}{C_{Gouy} + C_{Helm}} \tag{6}$$

C_{Gouy} represents the Gouy-Chapman or diffuse layer, while C_{Helm} corresponds to the Helmholtz layer [24]. According to this analysis, neither the threshold voltage of the MOSFET nor the electrochemical parameters can be modified since they depend directly on the manufacture and interaction of the solution with the FET structure respectively, leaving V_{ref} as the only control variable that can intervene to modify V_{thres}*(ISFET)*.

Figure 2.2 shows a more precise representation of the parameters mentioned above, with the addition of the passivation capacitance that depends directly on the passivation stack's thickness and the ISFET gate's area.

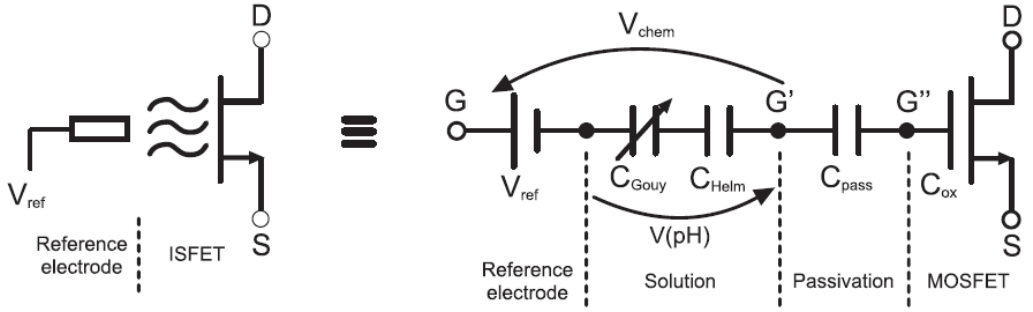


Figure 2.2 ISFET symbol and extended behavioural macromodel [9].

An ISFET offers several advantages regarding its sensitivity, selectivity and miniaturisation. These sensors allow accurate detection of pH, even in small changes, depending on the ionic concentration. The simple integration and inexpensive production also enable it to be used in CMOS technology, exploiting its capabilities in a wide range of applications. Finally, its suitability for mass production makes it a great candidate for commercial biomedical applications, from pH monitoring in biological applications to implantable devices for personalised medicine [25].

2.2.2 Electrolyte-insulator-semiconductor Interface

The electrolyte-insulator-semiconductor (EIS) interface, responsible for sensing the pH in a solution, comprises three layers. The electrolyte is the medium containing ions that are electrically conducting through their movement, providing the gate potential of the ISFET through a reference electrode; the insulator, which is typically made of silicon dioxide (SiO_2), serves as a barrier between the electrolyte and the semiconductor, and it prevents the ions in the electrolyte from directly affecting the semiconductor; and the semiconductor, which is typically made of silicon (Si), is where the ISFET's electrical characteristics are determined. The most important parameter of this interface is the flat-band voltage, which can be defined as the voltage applied to the solid-liquid interface that makes the silicon surface potential zero; it is derived from [26]:

$$V_{FB} = V_{ref} - \frac{\Phi_{Si}}{q} - \psi_0 - \frac{Q_i}{C_i} + \chi_e + \delta_\chi$$

where $\frac{\Phi_{Si}}{q}$ is the silicon's work function, ψ_0 is the potential drop in the electrolyte at the insulator-electrolyte interface , C_i and Q_i are the insulator capacitance and effective charge per unit area, and δ_χ collects a number of variations of χ potentials [27].

When a potential difference is applied across the EIS interface, ions from the electrolyte migrate towards the semiconductor, creating a charge build-up at the interface. This charge build-up in turn modifies the electrical characteristics of the semiconductor, such as its threshold voltage [28]. Upon reaching electrochemical equilibrium, the charge carriers of the chemical phases accumulated at the interface

generate an electrical double layer (EDL), which was first described by Helmholtz in the 19th century.

The interface between the concentration of ions in a solution and the gate generates an ionic distribution near the surface of the passivation layer based on the Gouy-Chapman-Stern model, shown in Figure 2.3 [29]. The Stern layer, also called the immobile layer, can be defined into two groups: the inner Helmholtz plane (IHP), which includes specifically adsorbed unhydrated ions onto the surface together with polarised solvent molecules, and the outer Helmholtz plane (OHP), which are hydrated ions that stay close to the surface due to the hydration sheath created by solvent molecules [30].

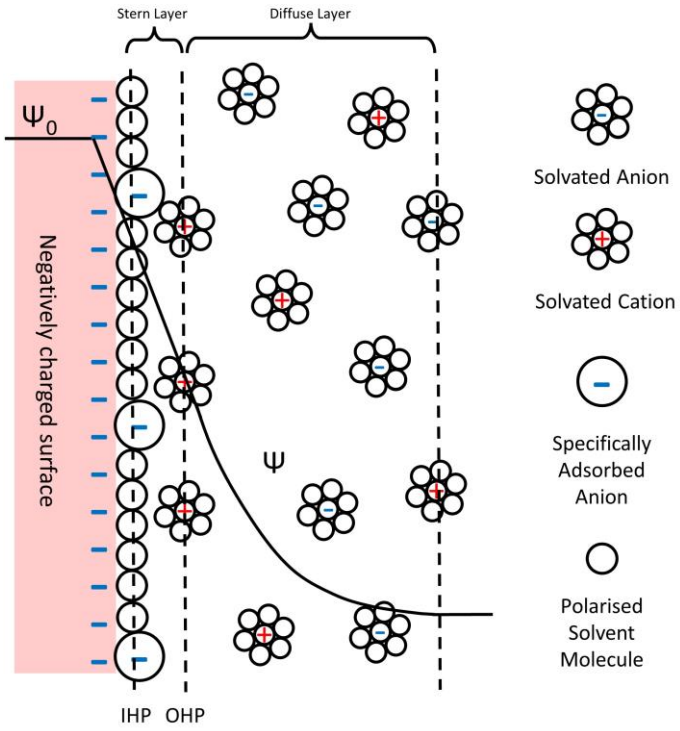


Figure 2.3 Potential distribution across electrolyte-insulator modelled by the Gouy-Chapman-Stern model [31].

A diffuse layer is located between the OHP and the bulk solution, called the Gouy-Chapman layer, and this corresponds to the remaining solvated cations/anions and water dipoles in the solution [32]. This layer can be modelled as a variable capacitor and is called C_{Gouy}, giving the entire interaction between the electrolyte and the interface presented in Figure 2.2 as V(pH).

2.2.3 Site Binding Model

Although the Gouy-Chapman-Stern model describes the main contributions of the electrostatic interactions to the EDL, it does not contemplate the chemical reactions in the solution, which can provide a net charge presence at the insulator's interface.

The site-binding model is a theoretical model that explains the behaviour of EDLs at interfaces between two phases, such as an electrode and an electrolyte solution. EDLs are thin layers of charge that form at the interface due to the movement of ions in the electrolyte solution. According to the site-binding model, the ions in the EDL interact with specific sites on the surface of the electrode, rather than being uniformly distributed across the surface. These sites may be defects or impurities on the surface of the electrode, or they may be specific functional groups present on the surface [33].

Unlike electrostatic forces, chemical reactions only occur within molecular distances, making them only possible within the OHP layer. Due to their radius and the fact that they are not shielded by water layers, only hydrogen and hydroxyl ions can penetrate the OHP, enabling chemical reactions at the surface [34]. As shown in Figure 2.4, there is a substantial number of unsaturated bonds at the surface of an insulator, called active sites, which are amphoteric, basic and acidic. The difference arises because amphoteric substances have the ability to function as either proton donors and receptors, whereas the other two can only function solely as proton donors or receptors, respectively.

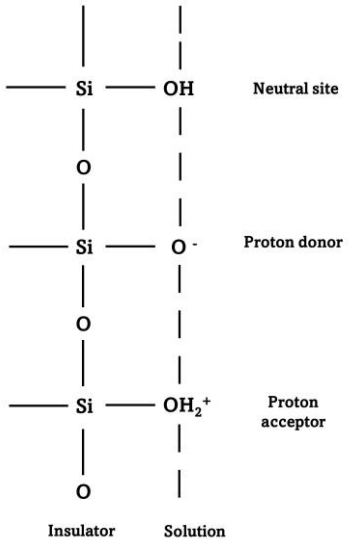


Figure 2.4 Schematic representation of site binding model for a SiO_2 layer [34].

Yates, Levine and Healy [33] developed the site binding model in 1973 to better describe the interaction at a general oxide-electrolyte interface, which defines the equilibrium between the amphoteric surface sites and the H+ ions in the solution. Normally, the following chemical reactions are balanced in the membrane:

$$MH_2^+ \Leftrightarrow MH + H^+ \tag{8}$$

$$MH \Leftrightarrow M^- + H^+ \tag{9}$$

where *M* represents the insulator material, such as SiO. The first reaction charges the oxide surface positively, while the second charges the insulator surface negatively. The final charge density is defined by the number of initial bonding sites and the local density of hydrogen ions. These reactions can be rearranged using the law of mass action into:

$$K_a = \frac{[MH][H^+]}{MH_2^+} \tag{10}$$

$$K_b = \frac{[M^-][H^+]}{[MH]} \tag{11}$$

where K_a and K_b are the dissociation constants for deprotonation and protonation reactions respectively. For the surface charge, only the activity of hydrogens as a surface potential should be used and this can be expressed as:

$$[a_{H+}] = [H^+]_b e^{-\beta\psi_0} \tag{12}$$

where q is the electron charge ($1.60217657 * 10^{-19}\, Coulombs$) and ψ_o is the interface potential. Using (12) into (10) and (11) relates the connection between the surface potential of an electrolyte and the charge density added to the surface of the insulator by chemical reactions.

The total surface charge density can be defined as:

$$\sigma_{Ox} = q([MH_2^+] - [M^-]) \tag{13}$$

While the surface site density is given by:

$$N_S = q([MH_2^+] + [MH] + [M^-]) \tag{14}$$

The surface charge density resulting from a chemical reaction can be obtained by combining the five equations that came before:

$$\sigma_{Ox} = qN_S \frac{\frac{[H^+]_b}{K_a} e^{-\frac{q\psi_o}{qk_bT}} - \frac{K_b}{[H^+]_b} e^{\frac{q\psi_o}{qk_BT}}}{1 + \frac{[H^+]_b}{K_a} e^{-\frac{q\psi_o}{qk_BT}} + \frac{K_b}{[H^+]_b} e^{\frac{q\psi_o}{qk_BT}}} \tag{15}$$

where *k* represents the Boltzmann constant ($1.3806488 * 10^{-23} m^2 kg^{-2} K^{-1}$) and T is the absolute temperature in Kelvin ($K = ℃ + 273.15$). The maximum amount of surface change is directly proportional to the number of surface sites per unit area [35].

2.2.4 Common Challenges

The most recent literature has focused on dealing with the non-idealities present in ISFET devices. These represent a significant limitation that has prevented the development of this technology on a large scale. Several ways to tackle these challenges include novel instrumentation, ISFET layout and post-processing techniques. Some promising results have shown the capacity to use these electrochemical sensors for several applications, including implantable devices. This section will summarise the main challenges present in these devices, highlighting their source and effects on the overall performance. Figure 2.5 shows a visual representation of the most common challenges in ISFET devices.

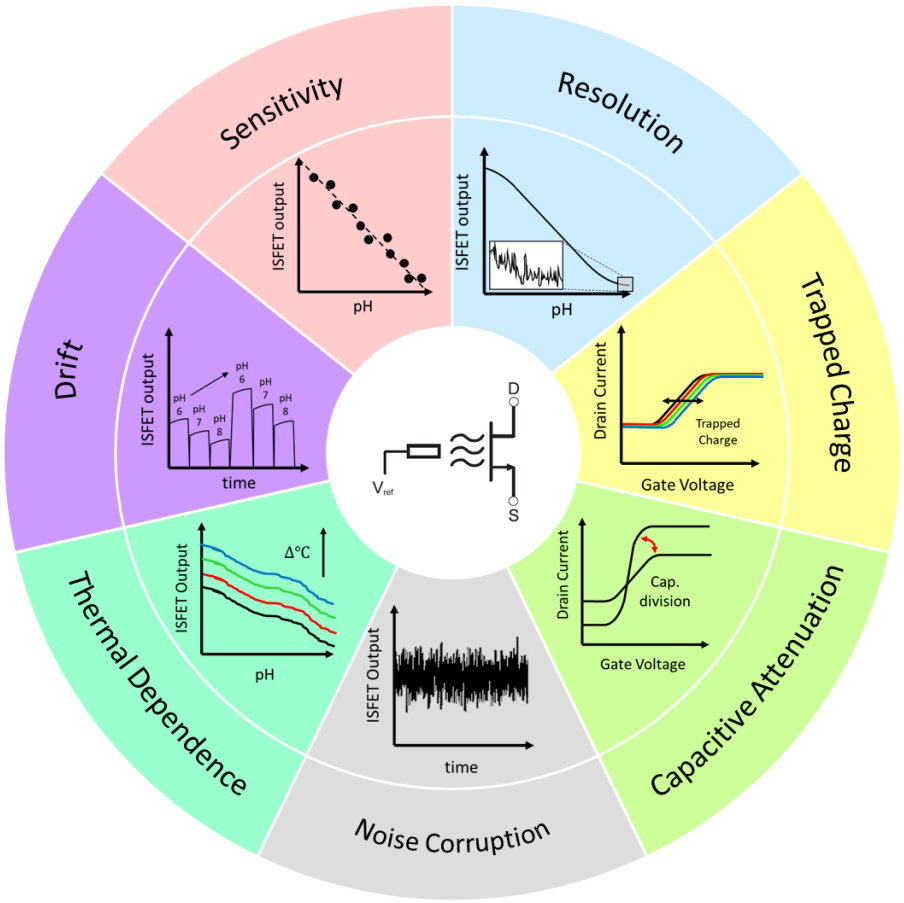


Figure 2.5 ISFET sensing parameters, including the most common challenges [36].

A. Trapped Charge

The accumulation of charges in the gate oxide and passivation layers due to the fabrication process at the foundry is known as trapped charge. This represents an unknown added potential that varies in each device, introducing mismatch [37]. The literature has shown that there is a large margin of magnitude in which the trapped charge can fall, from a few volts in n-channel devices [38] to as much as tens of volts in p-channel ISFETs [39], making this an uncertain that must be resolved to improve their performance. This behaviour can be seen as a shift in the threshold voltage on an I-V curve and is added as an offset of the device [9], as shown in Figure 2.5. Some methods have been successfully proven to remove or work around the trapped charge of a device, including the use of ultraviolet (UV) light [40], hot electron injection/electron tunnelling [41], and instrumentation compensation [42] [43] [44].

B. Drift

Drift can be defined as a temporal monotonic change in the threshold voltage of the ISFET under stable conditions over time. This non-ideality arises from a transport occurrence at the interface between the solution and the surface [45]. Drift has been attributed to several phenomena such as ion migration, mobile ionic charge, slow surface effects, and hydration of the insulator surface [46] [47]. It is one of the most relevant problems with ISFETs, as it is usually unpredictable. Several factors, including the solution, the sensing layer, and the size of the device, have been shown to influence the drift [48] [49]. Drift has been characterised into three categories: fast, slow and a baseline phase. The main category is the fast response (90% of the drift), which occurs due to the reaction between the solution and the surface sites [50]. Then, the slow response turns out to be minimum in magnitude, but it takes a few hours to be noticeable, and it is related to the loss of sensitivity of the binding sites at the surface of the insulator [51]. Finally, the baseline drift corresponds to a shift under constant environmental and biasing conditions, but its long-time constant usually surpasses the device's lifetime [52].

C. Capacitive Attenuation

The passivation layer incorporated in CMOS processes is usually composed of two different layers of silicon nitride (Si_3N_4) and SiO_2, but sometimes the addition of a third thick layer of polyimide can be requested, which is beyond the scope of this thesis, as it makes the devices very insensitive to pH. This surface bilayer adds a passivation capacitance, which is already present in the extended macromodel shown above. Usually, the passivation capacitance (C_{pass}) tends to be more than an order of magnitude smaller than C_{Helm} and C_{Gouy}, playing a fundamental role in the equivalent capacitance as it is the dominant component [53]. This non-ideality affects the output behaviour by attenuating the signal depending on the size of the capacitance present in the passivation layer. In the case of unmodified CMOS chips, the passivation capacitance can be easily calculated using the following formula:

$$C_{pass} = \frac{\epsilon_{Si3N4} * \epsilon_{SiO2}}{\epsilon_{Si3N4} * t_{SiO2} + \epsilon_{SiO2} * t_{Si3N4}} * \epsilon_{0 * A_{pass}} \tag{16}$$

where C_{pass} represents the passivation capacitance, A_{pass} the area of insulating passivation, and ϵ_{Si3N4}, ϵ_{SiO2} and ϵ_0 are the Si_3N_4, SiO_2 and absolute dielectric constants, while *t* corresponds to the thickness of each independent layer [45]. The impact it has on the overall ISFET structure results in a division of the surface potential, which can be calculated using the following formula:

$$V_G^{"} = V_G' * E = V_G' \frac{C_{pass}}{\left(C_{pass} + \left(\frac{C_{ox}C_d}{C_{ox} + C_d}\right)\right)} \tag{17}$$

where $V_G^{"}$ is the effective gate voltage, C_{ox} and C_d are the oxide and depletion capacitances, and *E* is the effective division of the surface potential due to these capacitances [37]. One way around this issue is to add a new sensing layer instead of the passivation layer that comes from the foundry, but this requires extra post-processing steps, making it difficult to replicate on a larger scale [9].

D. Temperature Dependency

The following non-ideality corresponds to temperature variations caused by the intrinsic thermal agitation and subsequent electron flow related to the MOS threshold voltage temperature coefficient, the reference electrode potential drop and the electrolyte-insulator potential temperature variability [9] [54]. This temperature sensitivity results in a variation in the behaviour of the current flowing through the ISFET, which increases in magnitude as it reaches high temperatures [55]. A previous study showed that the temperature dependence of a reference electrode could be estimated as [56]. In contrast, the other two can be calculated from the equations in Section 2.2.1 corresponding to the electrochemical behaviour and the MOSFET threshold voltage.

E. Light Sensitivity

ISFETs tend to be light-sensitive due to the pn junction contained in the source and drain in the substrate. In theory, when enough light strikes the sensing area, electrons in the substrate will excite, creating free electrons and holes. Due to the open gate configuration, both the spectral distribution and intensity of the light will influence the sensor's performance, affecting the threshold voltage [57]. One way to overcome this challenge is to avoid the exposure of the

sensing area to light during measurement. However, further solutions need to be investigated as there are some scenarios where this is not possible.

F. Noise Corruption

Finally, the last challenge affecting the output signal performance is noise corruption, coming from the MOSFET's intrinsic properties and the chemical interaction between the surface and the solution [58]. The primary noise sources to consider in both cases are the thermal and flicker noise. The first is caused by thermal excitation of charge carriers, while the second is caused by channel energy band traps that randomly capture and release carriers. [59]. It has been found that chemical interaction noise predominates over electrical noise by one order of magnitude [9]. In contrast, flicker and thermal noise are present in both sources, suggesting that noise can be interpreted as the sum of all three noises. However, although studies have been done on customised ISFETs, limited information is available on CMOS ISFETs.

2.3 ISFET Simulation Models

Thanks to the mathematical development of the ISFET structure, various simulation models have been created to represent the behaviour of these devices. Due to several drawbacks presented in the first ISFET macromodels, mainly related to the complexity of their use and adaptability to different circuit simulators, Martinoia and Massobrio [24] developed a general behavioural model for SPICE version software. This macromodel considers a sensing membrane of Si_3N_4. The code defines the electronic devices and their respective voltages considering the electrochemical variables mentioned in equation (5) that establish the threshold voltage of an ISFET. The equivalent circuit of the ISFET is shown in Figure 2.6. This model allows the user to change the sensing layer by modifying the properties of the materials on the surface of the sensing gate area. The simulation was compared to experimental data to validate the physicochemical model results, as shown below.

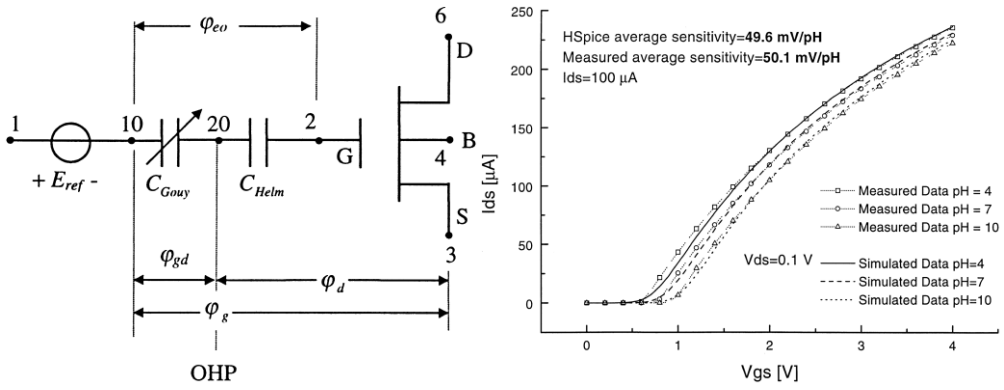


Figure 2.6 Left: Equivalent circuit of the ISFET structure; Right: I-V characteristic curve comparison between simulated and experimental data for different pHs with Si_3N_4 gate [24].

This model allowed for the adaptation of more versions in different software, and Sohbati [45] developed a Veriloga model based on the SPICE version. The main difference between the two models is that the Veriloga macromodel is a behavioural model, providing only the electrochemical behaviour without defining electrical components. The benefit of this version is that it is compatible with Cadence and allows the user to specify the sensitivity through a scaling factor variable, thus giving even fewer parameters to modify and making it the easiest macromodel to handle.

2.4 ISFET Instrumentation

The following categories cover the main ISFET circuitry designs to analyse their advantages and disadvantages. Moser et al. [9] provide a detailed review focused extensively on three different approaches and their variations: pH-to-voltage, pH-to-current and pH-to-time. This section will focus on single-ended designs. Detailed analysis of differential ISFET structures is beyond the scope of this thesis.

2.4.1 Single Architectures

A. pH-to-voltage

One of the prevailing measurement techniques in the literature involves the correlation of ISFET gate pH-induced voltage with instrumentation output voltage, yielding a pH-to-Voltage conversion. The most popular topology is the source-drain follower [60] [61], mainly due to its compactness, low power supply voltage and low power consumption. The simplicity of this design has

led researchers to explore different configurations to maximise its performance. One of the most characteristics designs was developed by Nakazato et. al. [62], where they kept the ISFET current and reference electrode voltage constant, leaving the gate voltage to determine the correlation with the output, giving good accuracy and minimum power dissipation. Other alternative designs focused on achieving minimal power consumption while adhering to the same principle, operating with voltages below 1 Volt and having a great dynamic range for the detection of a broad pH range [63] [64]. However, they lack compensation schemes to tackle these devices' common challenges and are vulnerable to power supply variations. Three designs cover the main topologies: controlled-voltage controlled-current (CVCC) [65], I-to-V converter [66], and global current feedback [67]. These architectures have different advantages, like immunity to capacitive scaling and amplification methods. Unfortunately, in addition to the previous disadvantages, the complexity of these designs increases the system size and power consumption.

B. pH-to-current

The following approach has not been explored as much as the previous one. However, two main circuitries stand out: an ISFET current mirror and a translinear principle architecture. The ISFET current mirror has drift and temperature compensation due to a differential configuration [68], while the translinear principle architecture exhibits good linearity at the current output [69]. However, both have some disadvantages. The current mirror output exhibits nonlinear behaviour with respect to the gate voltage, the reference current source should be ideal and the sensitivity is relatively low compared to the reported in the literature (27 mV/pH) [68]. On the other hand, the translinear principle architecture has one of the largest transistor areas to minimize the effect of matching errors, the linear range is compressed in a small voltage variation, and the architecture has intrinsic leakage current and a wide variation in process parameters [69].

C. pH-to-time

The following approach consists of encoding the signal in the time domain by digitising the output signal through a pulse width modulation (PWM). All of the architectures follow the same base circuitry: CMOS inverters with different configurations [70] [7] [71] [72] [73]. The designs have the same inherent configuration advantages, like less susceptibility to environmental noise and less signal processing. Some configurations also show the potential to reduce the size and power consumption, as well as several compensation schemes for nonidealities. However, some disadvantages include nonlinear systems, calibration phases and minimum pulse width variations between pH measurements, making it less suitable for sub-pH applications [72].

D. pH-to-frequency

The latest approach has been to encode the signal in the frequency domain using several methods. Historically, frequency modulation was developed based on two criteria: to make systems as efficient as possible in terms of power and to provide consistent data with good reliability, particularly for telemetering data from satellites and space probes [74] [75]. This approach varies from the previous one in the way data is being manipulated. pH-to-time uses PWM, which modifies the duty cycle of a fixed frequency square wave to regulate the output of the system, while pulse frequency modulation (PFM) uses a constant duty cycle and modulate the square wave's frequency to achieve regulation [76].

Architectures can be divided into four groups: pulse frequency modulators [77], integrate-and-fire architectures [78] [79], ring oscillators [80] [81] and current-controlled oscillators [82] [83]. All these designs include the inherent advantages of the topology, which are the robustness of the signal against noise and less signal processing. Furthermore, depending on the configuration, some benefits can be acquired regarding size, power consumption, linearity, signal stability against power supply variations, programmable output response, and immunity to capacitive attenuation scaling. Frequency conversion was chosen over other architectures because the criteria of power efficiency and data reliability aligned with the objectives of this work, plus its inherent advantages

like noise immunity and digital compatibility are suitable for applications of interest, such as wearable and implantable devices.

However, noise in these systems remains a challenge to address due to the complexity of the signal transduction. Addressing low-frequency noise can be achieved through techniques such as the incorporation of ISFET/MOSFET pairs employing chopping stabilization. This approach effectively diminishes 1/f noise while simultaneously resetting the surface potential of the floating gate of the ISFET, eliminating any trapped charges within the buried sites and having an impact on the system's drift with minimal disturbance of the sensing gate. [84] [85]. Other sources of noise, such as phase noise, are not a primary concern, as it become significant in applications involving high-frequency or precision timing, and the emphasis is on the accuracy and linearity of the pH-to-frequency conversion [86]. Nevertheless, some potential sources of phase noise and jitter include clock sources, power supplies, temperature variations, component noise and external electromagnetic interference [87] [88]. Maintaining signal integrity, suitable operating conditions, and implementing filtering and shielding to reduce interference are essential to minimize these issues.

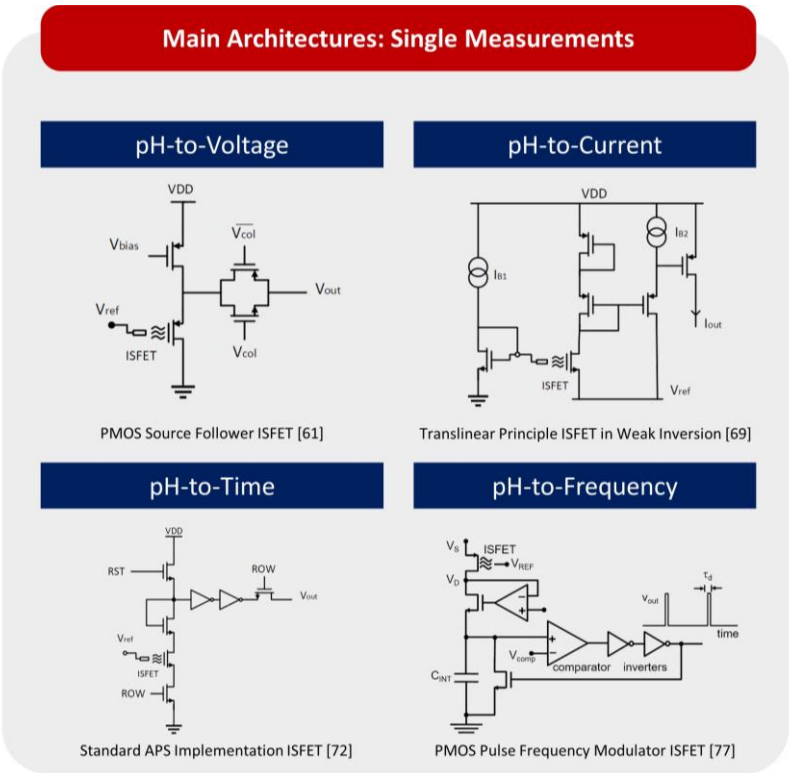


Figure 2.7 Overview of the main analogue front-end architectures for single ISFET readouts categorised by type of transduction.

2.5 ISFET Sensing Layers

One key component of a CMOS ISFET sensor is the sensing membrane, which separates the ISFET from the solution being measured. The sensing membrane can be made from various materials, such as Si_3N_4 or aluminium oxide (Al_2O_3), which are characterised by their dielectric constant. The ability of the insulator interface to resist changes in pH (β_{int}, shown in equation 4) is determined by the dissociation constants and ionic concentration and is affected by the density of binding sites. A higher density of sites leads to increased sensitivity and a wider range of pH values that the device can operate within [89]. The choice of the sensing membrane material, its thickness and uniformity can significantly impact the sensitivity, selectivity and stability of the ISFET sensor. Although research has been done using a wide variety of sensing membranes, some of them are beyond the scope of this thesis due to their limited applicability in CMOS technology.

The most common sensing layers available in the literature for CMOS chips are Si_3N_4, Al_2O_3, hafnium oxide (HfO_2) and tantalum pentoxide (Ta_2O_5). All these layers have shown positive results in terms of the sensitivity and stability of the sensors. However, they have never been cross-verified and compared systematically using the same underlying CMOS technology. It is important to note that the first reported ISFET device used SiO_2 as a gate insulator layer, but it has been shown to have a relatively low pH sensitivity, an unstable response over time, and hydrating properties that cause surface membrane ruptures, making it permeable to water [90] [91].

Si_3N_4 is the most common sensing layer researchers use as it is the default passivation layer for standard CMOS processes, thus avoiding further microfabrication steps. This sensing layer has been reported as a significant improvement compared to SiO_2 [92]. It can give better sensitivity and a nearly linear response to pH changes. Despite the differences found in terms of the sensitivity by different groups, Si_3N_4 can provide an average sensitivity of 25–40 mV/pH, with the possibility of getting responses near (45 mV/pH by thinning the passivation layer) or beyond the Nernstian response

(149.7 mV/pH due to an equivalent inherent amplification in the readout [93]). Table *2-1* summarises the major findings in the literature related to each sensing layer described above.

Layer	Sensitivity	Main contributions	pH range	Ref
Si_3N_4	45 mV/pH	Thin passivation layer	-	[94]
	40-45 mV/pH	Differential readout	1 - 14	[95] [96] [97] [98] [99] [100]
	25-41 mV/pH	Unmodified chip	4 – 12	[101] [93] [7] [102] [103] [104]
Al_2O_3	37.45 mV/mM	Exposed native oxide by an etching process	6 – 8	[105]
	31.6 us/pH			[106]
	2.2 kHz/pH		6 – 8	[83]
	215 µA/pH		6.9 – 8	[107]
HfO_2	44-45 mV/pH	Atomic layer deposition (ALD)	4 - 10	[108] [109]
Ta_2O_5	52 mV/pH	Ta film was deposited by PVD and then oxidised in deionised H_2O	3.4 – 6.4	[110]
	40-55 mV/pH	RF-magnetron sputtering	4 - 12	[111] [112] [113]

Table 2-1 Most common pH sensing layers in CMOS in the last two decades.

However, there is still no consensus on the best sensing layer. The range of variation in sensitivity can be even greater if a different CMOS foundry or the technology node (even within the same foundry) is varied. Further to the list above, solo efforts have been made to innovate with different sensing layers beyond the most successful cases. Chin et al. [114] deposited a 250 nm layer of titanium nitride (TiN) above the aluminium gate with an outcome sensitivity of 57 mV/pH. In contrast, Kuo et al. [115] deposited a ruthenium dioxide (RuO_2) thin film with a sensitivity of 8.6 mV/(mg/dL), both using RF sputtering for the metal deposition. On the other hand, [116] and [117] provided a stack of layers of Ta_2O_5/Si_3N_4 and ZnO/TiO_2 with sensitivities of 45 and 46.9 mV/pH each. However, Si_3N_4 is still the preferred choice because it does

not require any further microfabrication process, and it can provide consistent results in terms of sensitivity, which is the main objective for these sensors.

2.6 ISFET Applications

ISFETs have become widely used in various applications due to their high sensitivity, fast response time, and ease of integration with microelectronic devices. These sensors have been used in portable and disposable devices due to their small size, low power and low cost. They are ideal for monitoring variables of interest through pH detection, such as DNA, metabolites, enzymes, genes and cancer markers, among others. For clarity, this section will focus on applications using CMOS technology, except for environmental monitoring due to the lack of research in this area.

One of the main applications of ISFETs is in biosensing and medical diagnostics. ISFETs have been used to measure pH levels/detect various molecules in blood [118] and other body fluids, which can provide information about a patient's health, like states of alkalosis or acidosis due to a high or low pH level, which is a clear indication of some organ dysfunction. They have also been functionalised to be selective to various ions in the same chip [19], making them good multiple-sensing monitoring platforms. For example, ISFETs can be used to monitor: glucose levels in people with diabetes, which can help to control blood sugar levels and prevent complications [119]; urea levels [107]; dopamine [120]; DNA detection and sequencing [104] [121] [66]; cholesterol [122]; uric acid [115]; L-carnitine [110]; and cancer biomarkers [123] [124], among others. Some other interesting applications in this area are ion imaging [125] [126] [61], on body pH detection [80] and cell membrane injuries [127].

Another application of ISFETs is in environmental monitoring. ISFETs can measure the pH levels of water and soil, providing fundamental information about the health of ecosystems and the potential impact of pollutants. ISFETs can also be used to measure the concentration of heavy metal ions in water and soil, which can help to identify and mitigate contamination. Portable sensors have been designed to monitor soil cultivation [128] and examine soil nitrogen on-site in agriculture [129]. Several attempts haven been undertaken to develop robust monitoring systems [130] for

multiple sub-applications, like potable water assessment [131] and geochemical barrier monitoring [132] by characterising the interstitial water in a geochemical barrier to assess the hydro-geochemical factors that regulate the transport and migration processes of radionuclides [133]. It is important to mention that this area has yet to be studied using standard CMOS processes, but it is a possible area for further research.

ISFETs can also be used for safety screening applications in the food and beverage industry. For example, these sensors can measure the acidity, sugar/starch content, firmness and presence of heavy metals in fruits [134] and vegetables [135], as well as analyse aromas and flavours [136], and detect food-borne bacteria like E. coli [137], which can help to control the quality and extend the shelf life of commercial products.

In addition to these applications, ISFETs are being investigated for use in other areas, such as drug discovery [138] [139] and gene expression analysis [140] [141]. The potential of ISFETs is still being explored due to their ability for large-scale integration, miniaturisation and low-cost manufacturing, and new applications are likely to be discovered in the foreseeable future.

2.7 Summary

ISFETs are a type of sensor sensitive to ionic concentrations in a solution. They consist of a thin layer of semiconductor material, such as silicon, coated with a thin layer of insulating material, such as silicon dioxide or silicon nitride. When a voltage is applied between two nodes of the ISFET system, an electric field is created, which can be used to measure the concentration of ions in the solution.

One of the key advantages of ISFETs is their high sensitivity, which allows them to measure even small changes in ion concentration accurately. They are also relatively simple and inexpensive to produce, making them widely available and widely used. Their ease of integration with CMOS technology and potential mass production makes them ideal for developing commercial devices for environmental and biomedical applications.

However, ISFETs have their limitations. They have several common challenges, such as capacitive attenuation, noise corruption, temperature dependency, drift and trapped charge. They also require a reference electrode to function correctly, which must be considered if they want to be used in some specific applications.

ISFETs are commonly used in various applications, including medical diagnostics, environmental monitoring, the food and beverage industry and analytical chemistry, among others. They are particularly useful for measuring ion concentrations in dilute solutions, which are too dilute for traditional ion-selective electrodes to be effective.

Despite their limitations, ISFETs are an important tool in many scientific and industrial applications, and they continue to be an active area of research and development. As our understanding of these devices improves, we can expect to see even more sophisticated and reliable ISFETs being developed in the future. Overall, ISFET sensors in CMOS technology offer high sensitivity, selectivity and stability. They can also be integrated with other electronic components on a single chip, making them a powerful tool for chemical sensing in various applications.

Chapter 3

Sensor Front-end Architectures

3.1 Introduction

This chapter overviews the architecture designs, simulations and electrical characterisations performed during this project. The chapter describes two designs: an improved non-linear pulse frequency modulator (NPFM) with two prototypes, and a linear pulse-frequency modulator (LPFM). These front-end architectures and their main advantages over other read-out sensors are described here, along with a more in-depth analysis. For clarity, the NPFM architectures and electrical characterisations will first be described before moving to the LFPM.

Over the course of this project, two multi-project wafers (MPW) submissions were made to be manufactured by TSMC in 0.18 µm CMOS technology. The results and discussion for this chapter involve two frequency-domain architectures intended to be used as pH sensors in the following chapter. The analysis provided uses an environment to emulate the pH changes in each design, showing their applicability as sensing platforms for the next stage of the thesis.

3.2 Overview of Foundry Technology

The design and manufacturing of the CMOS chips were done using two different processes by the same manufacturer: 0.18 um CMOS TSMC High Voltage BCD Gen II and 0.18 um CMOS TSMC Logic or MS/RF, General Purpose 1.8V/3.3V as provided by the Europractice IC MPW service. BCD Gen II is a 6-metal process (MET<6>) with the top metal capable of handling up to 70 V devices with a core voltage of 1.8 V and I/O voltages of up to 5 V, while the General Purpose technology is also a 6-metal process suited to MS/RF applications with a core voltage of 1.8 V and I/O voltages of up to 3.3 V. SiO_2 is deposited between metallisation layers as an insulating material, with metal vias (VIA<x>) used to interconnect layers. The chip is

then covered with a protective layer of SiO_2 and S_3N_4, exposing pads for external electrical connections. The main objective is to develop low-power front-end architectures for pH detection so that both processes comply with the requirements of this project. The protective layer of Si_3N_4 also works as a sensitive layer, so no further processes were required for the initial testing of these devices.

The service integrates multiple designs from different customers onto a single wafer to minimise costs to approximately 5-10 % of the full size. Wafers are then diced and packaged into a standard waffle chip carrier by Europractice. The wafer cross-sectional view of the TSMC technology is shown in Figure 3.1.

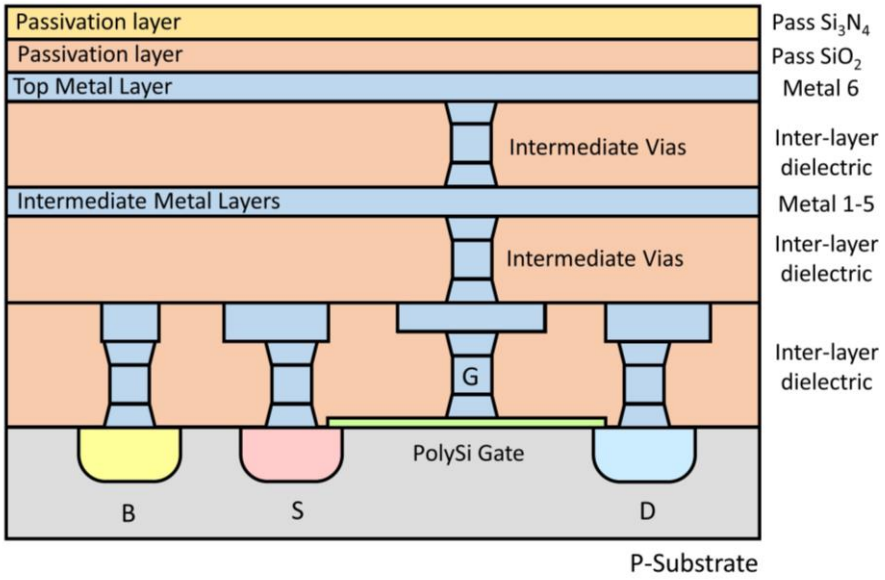


Figure 3.1 Cross-sectional view of the 6-metal layer-0.18 µm TSMC CMOS process.

3.3 ISFET Simulation Model

The first step in ISFET circuit simulation is determining an appropriate model compatible with the simulator. Described in Section 2.3, two ISFET models were simulated to evaluate their performance against each other using different circuit simulation software, considering that only the Martinoia's model was tested against measured data. The I-V characteristic curves for pH 4, 7 and 10 show considerable similarities. The PSpice model was modified to work with free access software from a Hspice code, while the Veriloga model is compatible with Cadence. As shown in

Figure 3.2, both models showed similar behaviours depending on the simulated pH. However, although both reached similar voltages over time, they exhibited different damping behaviours. Martinoia's model was designed for a specific case, which means it is more precise. In contrast, Sohbati's model represents a general chemical behaviour, so additional components must be added to achieve the desired output response.

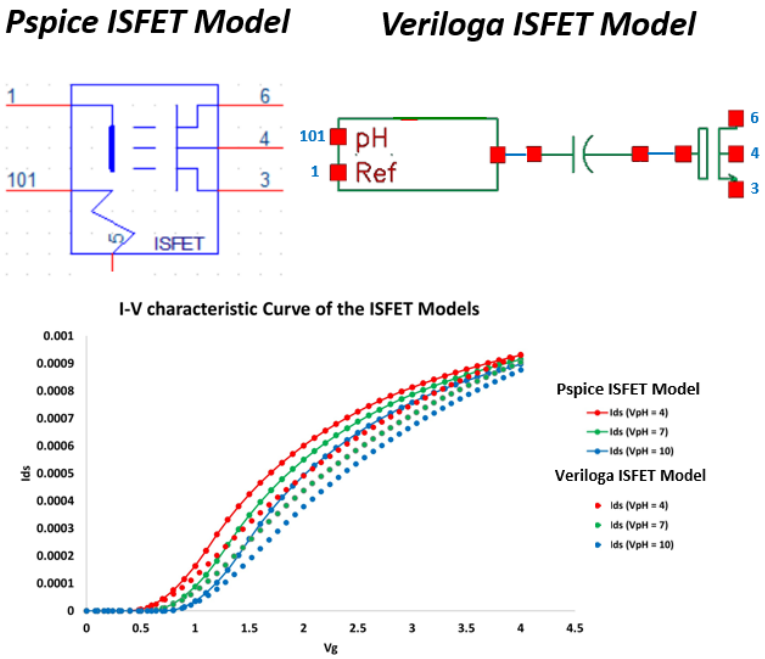


Figure 3.2 Schematic view and simulation results of PSpice and Veriloga ISFET models.

3.4 Nonlinear Pulse-frequency Modulation Architecture

The primary motivation for this type of signal transduction (pH-to-frequency) is to take advantage of some of its benefits over different conversions. These designs offer a simple and compact solution to conventional ADCs in size and power consumption. They provide a robust quasi-digital signal with codified information in the frequency domain, making it easier to communicate and reconvert the data via wireless. This type of architecture achieves high accuracy in code-to-frequency conversion. It allows specifications to be defined depending on the type of application, like a rail-to-rail input, linearity, programmable frequency range, and supply voltages compatible with and independent of batteries over time.

3.4.1 Front-end Architecture

The first proposed architecture, the nonlinear pulse-frequency modulator, is shown in Figure 3.3. The original application consists of a photodiode whose voltage signal is immediately converted into a semi-digital signal by allowing the charging and discharging of a signal capacitor, giving a frequency response that changes depending on the intensity of the light [142]. In this case, the photodiode was replaced by an ISFET, and the design provides a train of pulses each time the capacitor discharges down to a specific threshold voltage, depending on the pH in the solution.

The circuit diagram consists of two stages: a current integrator and reset, and a control circuit for the feedback, which determines the signal to open the digital switch to charge the capacitor fully. When the voltage of the membrane capacitor (C_{mem}) V_{cap} surpasses the specified threshold voltage, the comparator turns off the digital switch, allowing the capacitor to discharge at a rate depending on the pH in the solution. The higher the pH, the lower the current flow through the ISFET, decreasing the frequency response.

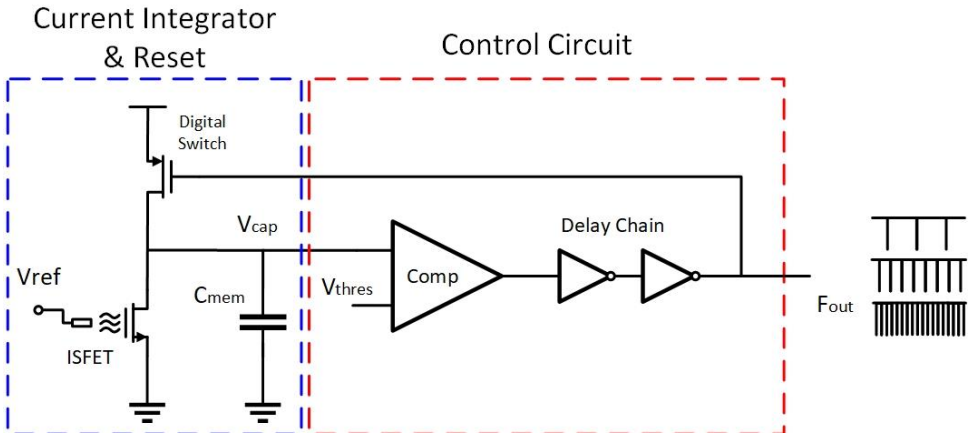


Figure 3.3 NPFM diagram-level schematic.

The architecture requires five inputs, plus the reference electrode in the solution, as shown in Figure 3.4. V_{Thres} represents the threshold voltage limiting the capacitor discharge to this value. V_{ctrl} is an on/off switch that controls if a power source provides the threshold voltage internally or externally. V_{CG} corresponds to one end of an extra capacitor connected to the gate, which is used to momentarily calibrate the input voltage range. Finally, the reset (RST) input is used to generate internal current sources

through a bandgap voltage reference. According to simulations, the circuit works with a power supply (VDD) of 1.8 V and has an average power consumption of 66.21 µW, considering standard setup conditions (V_{bias}: 700 mV, V_{thres}: 900 mV, V_{ctrl}: 18V and V_{CG}: 0V; V_{pH}: 7 V and V_{ref}: 300 mV for the Veriloga model).

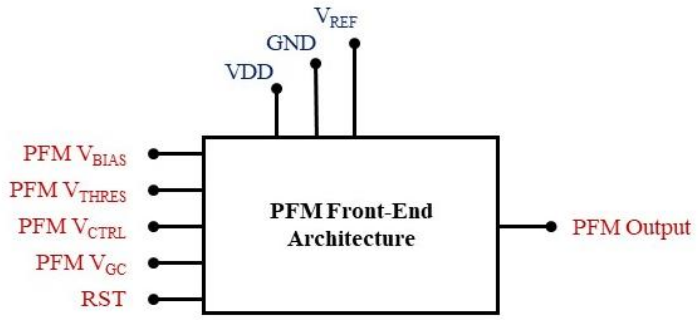


Figure 3.4 Schematic representation of NPFM architecture control block.

The current integrator and reset consists of three transistors: the ISFET for the slowly discharging phase; the digital switch for the instantly charging phase; and a bias transistor to isolate and rectify the charging and discharging voltage from the passivation capacitance. C_{mem} completes this stage and is connected to one of the inputs of the comparator, while the threshold voltage is provided in the other. The control circuit is then divided into two parts: a hysteresis-based comparator architecture to prevent undesired peaks from noisy input variations [143] and a delay stage consisting of a set of inverters and capacitors to get a specific delay time that allows C_{mem} to reach the threshold voltage in the discharging phase. Figure 3.5 shows the complete transistor-level schematic.

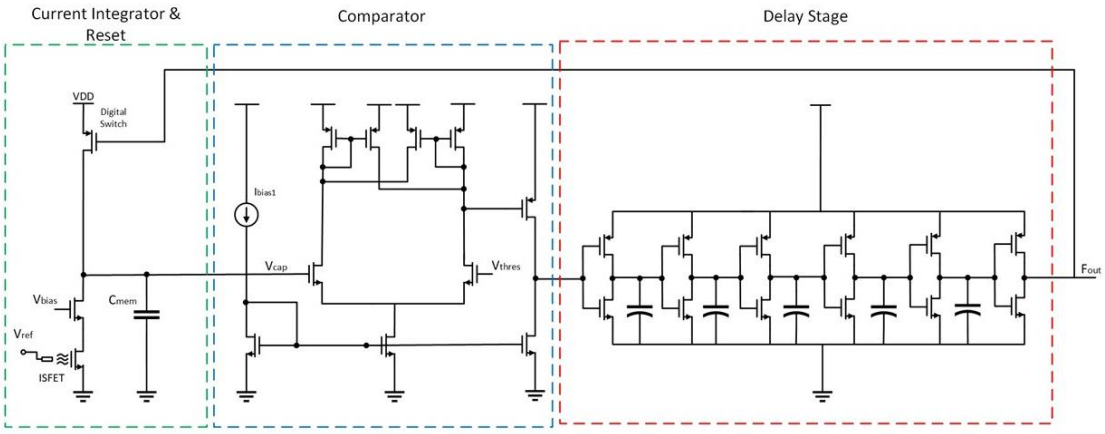


Figure 3.5 NPFM transistor-level schematic.

3.4.2 Simulation Results

The architecture underwent two rounds of simulations, one for each tape-out, enabling design improvement based on the characterisation of the first prototype. Both designs are described in the following section.

A. Chip CMOS-V1: NPFM-V1

The first tape-out included an initial design of the nonlinear pulse-frequency modulator. The simulation in ideal conditions for different input voltages, as shown in Figure 3.6, exhibited the expected nonlinearity and limited region of interest for the pH sensing, as the intention was to limit the working region to a range where the nonlinearity was not large, stepping down to approximately 100 mV of input voltage. The design showed its ability to work as a sub-pH sensing platform because more minor changes in pH transduced in much bigger changes in frequency.

In ideal conditions, and using an unmodified CMOS chip, a S_3N_4 sensing layer allows a sensitivity of approximately 30 mV/pH [7], which can be transduced in a 200 kHz change in the higher end of the working region, meaning that detection of 0.1 pH changes can be achievable with 15-25 kHz differences per sub-pH value. However, the calibration required was an area for improvement due to the low practicality in its implementation and high sensitivity to making it a functional design. The architecture also needs to work in a very specific region and working with aqueous solutions added more instability to the design.

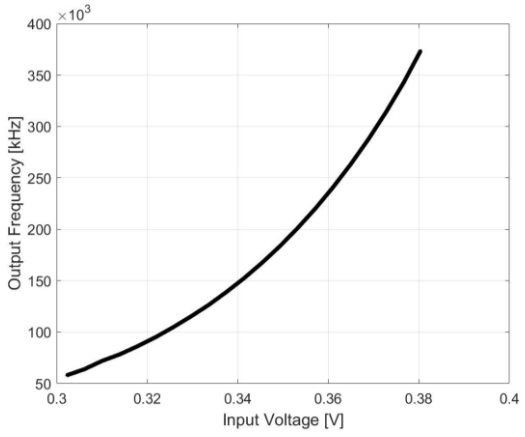


Figure 3.6 Simulation results of frequency response at different input voltages for a specific region.

This architecture was designed to give a train of pulses indicating each time the capacitor fully recharges up to VDD. Therefore, a minimum duty cycle is expected (0.013%, according to simulations). The inherent properties of the design made the output dependent on the electronic principles of the ISFET by having the relationship $V_d > V_g > V_s$. The output current only depends on the input voltage to the gate, therefore giving a nonlinear response that requires a look-up table for its analysis to identify the input voltage needed for the respective output frequency.

However, a more extensive analysis of the design in simulation, as shown in Figure 3.7, demonstrated how sensitive the design was to any capacitance at the output. The simulation consisted of adding a capacitance at the output to mimic the parasitic capacitance that is inevitably added during the testing process. This analysis allowed for a better understanding of the corresponding behaviour of the design. It showed how the output pulses were being affected by an increased output capacitance, meaning the architecture's delay stage (initially designed with two inverters with 95 ns of delay each as a buffer) needed to be increased to allow the capacitor to fully charge up to VDD.

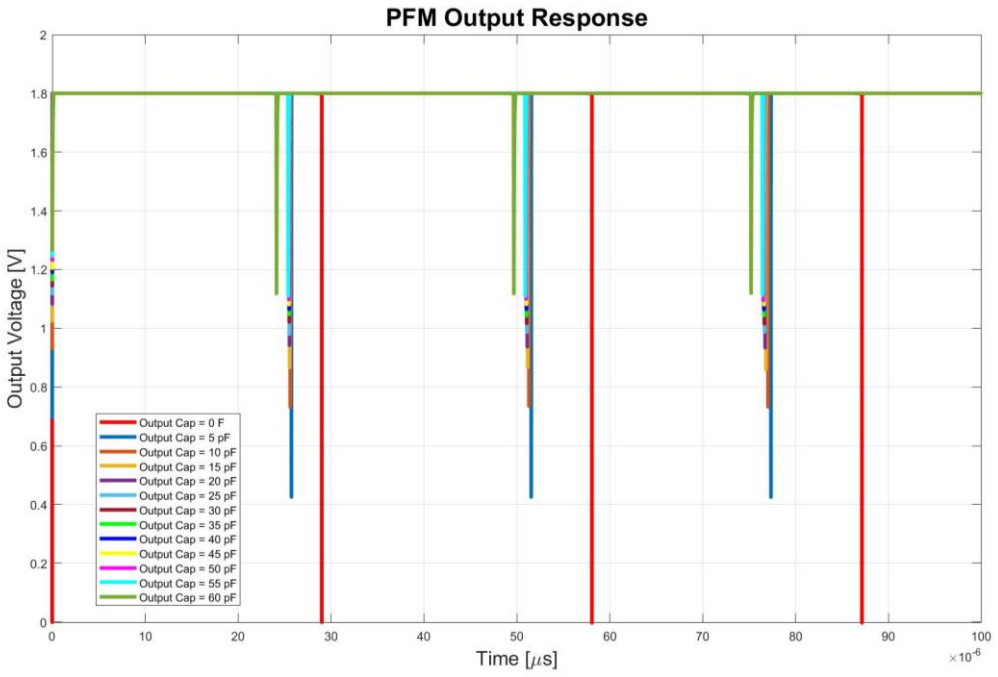


Figure 3.7 Simulated data of frequency response with different output capacitances.

B. Chip CMOS-V2: NPFM-V2

The next version of the NPFM was improved by increasing the delay stage (six sets of inverters and capacitors completed the design, where the first 5 provided 204 ns of delay each while the last one gave 147 ns for a total of 1.167 µs) to ensure C_{mem} had enough time to charge through the digital switch. The bias transistor was also included in this second prototype to isolate the charging/discharging phase from the effects of the passivation capacitance. Finally, an analogue buffer of three increasing stages was added between the output and the pad connection to guarantee the full swing of the train of pulses.

The architecture was simulated for the entire pH range (1–14), showing a response that varied depending on the pH value. The higher the pH at the gate of the ISFET, the lower the current allowed to pass through it, resulting in a slower train of pulses. However, during the simulation, it was noticed that this particular design has flaws that require a more complex design due to the balance needed to get ideal behaviour. By increasing the delay time, C_{mem} had sufficient time to reach the threshold voltage, but the delay allowed C_{mem} to surpass this limit, as shown in Figure 3.8. V_{thres} represents the limit voltage that C_{mem} should reach; however, the faster it works, the greater the difference between the threshold and C_{mem} voltage. Therefore, the saturation happens when the C_{mem} voltage reaches 0 V, meaning the delay time was big enough for it to fully discharge through the ISFET before the digital switch could be opened.

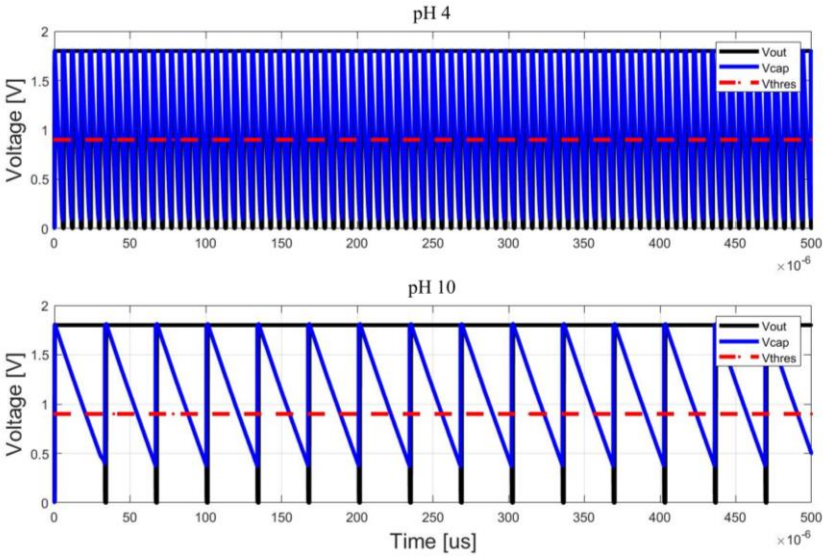


Figure 3.8 Train of pulses and C_{mem} voltage response for pH 4 and 10.

The architecture was simulated under different threshold voltages, depending on a control switch determining whether V_{thres} came from an internally generated or external power source. The simulation in Figure 3.9 gives a better view of the working region of this device. However, as shown above, C_{mem} quickly surpasses the corresponding limit of V_{thres}, making the working region even smaller to approximately the first 100 mV where the limit is complied, representing a maximum change of 3 pHs.

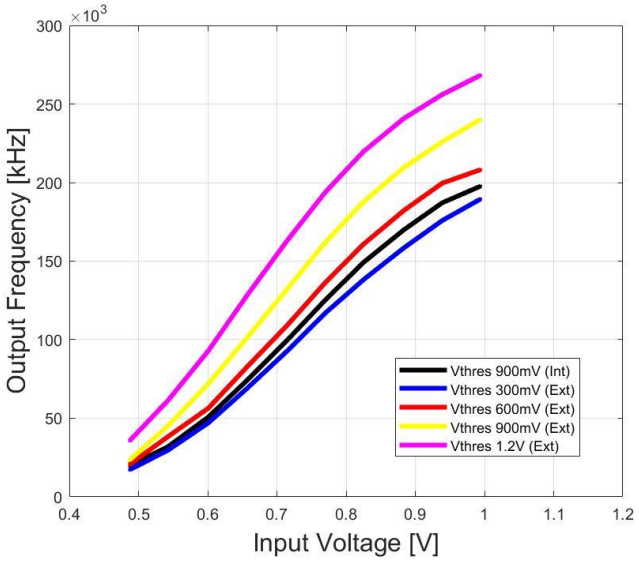


Figure 3.9 Simulation data of the frequency response for different threshold voltages.

A Veriloga ISFET model, already discussed in Chapter 3 and taken from [45], was added to evaluate the frequency behaviour at different pH values. V_{in} represents the voltage going into the gate of the ISFET. Figure 3.10 shows the output frequency from pH 3 to 12, considering an ideal sensing layer as a 59 mV/pH sensitivity response. The ISFET model allows the user to determine the sensitivity response using a scaling factor. This model, as shown above, requires an external capacitor to represent the passivation capacitance, which is mainly determined by the electrode area.

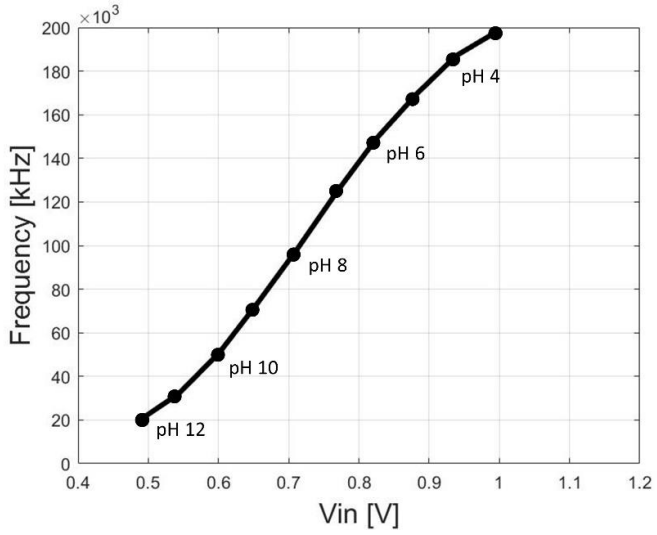


Figure 3.10 Output frequency response of improved NPFM architecture from pH 3 to 12.

Although the design represents an improvement on the first version, the limitations remain the same, as it can only be used to detect a narrow pH range. The required calibration demands very specific parameters regarding the reference and gate capacitor voltages to calibrate the working region for a specific pH range no greater than three values to get the expected outcome.

3.4.3 Layout Design

The improved sensor was implemented in 0.18 µm CMOS TSMC Logic or MS/RF, General Purpose 1.8 V / 3.3 V, and the layout is shown in Figure 3.11. The sensing area corresponds to an extended gate ISFET with dimensions of 125 µm × 125 µm to have a large ion-sensitive capture area and provide a geometry that can be easily post-processed through microfabrication processes. The readout instrumentation is

complemented with one bias current source through a bandgap voltage reference and a programmable gate capacitor, which is a floating capacitor connected to the gate of the ISFET for trapped charge compensation that allows for the temporal calibration of the ISFET threshold voltage. The total area of the circuit design is 155 µm × 409 µm. A micrograph of the fabricated chip is shown in Figure 3.12, where the features in metal-6 are visible, particularly the extended gate electrode.

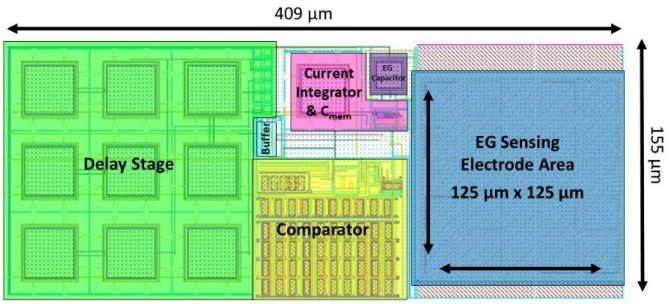


Figure 3.11 NPFM architecture layout.

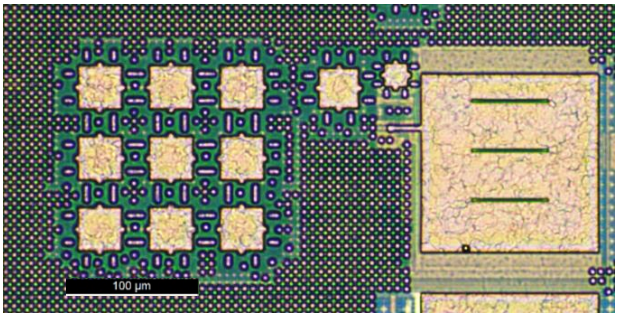


Figure 3.12 Micrograph of the fabricated NPFM architecture in the chip.

3.4.4 Electrical Characterisation

A. Chip CMOS-V1: NPFM-1

The electrical characterisation of these chips required the use of a dual power supply and a manufactured printed circuit board (PCB) to provide and control the necessary input voltages, such as the bias, threshold and control voltages through an array of potentiometers, switches and analogue and digital inverters. A Picoscope 6404D was used to measure the output voltage and calculate the corresponding frequency using the deep measurement tool provided by the software, which allows for the detection of the frequency, cycle

time, pulsed width and duty cycle. Figure 3.13 shows the schematic diagram of this setup for both designs.

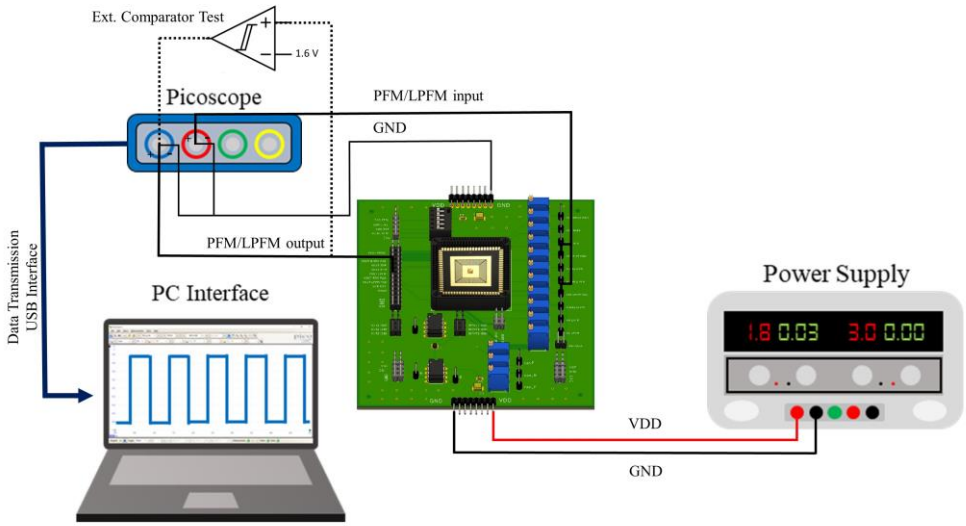


Figure 3.13 Schematic diagram of the setup to perform an electrical characterisation on the CMOS chips.

The output response of the first prototype indicated a design error in the architecture, as the train of pulses at the output never reached 0 V, but the frequency changed in relation to the input voltage provided. Therefore, a small test was performed using an external 5 V comparator (LM311N/NOPB) to show the expected outcome at a higher voltage compared to the actual output, as shown in the bottom graph in Figure 3.14.

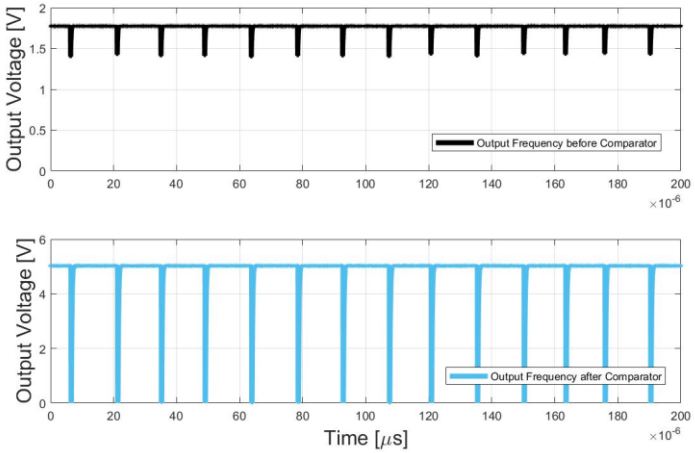


Figure 3.14 NPFM response of defective chip. Top: original output frequency before external comparator. Bottom: output frequency after external comparator.

Although the measurement was unsuccessful, a complete analysis of the output frequency response at different input voltages was performed using the previous setup to allow the design to work as a digital counter with the full swing through VDD. Figure 3.15 shows how the signal deviates from the expected result, working at a faster rate. Nonetheless, the signal partially provides the required behaviour because the architecture responds to changes in the input voltage. An alternative test (red graph in Figure 3.15) shows how the programmable gate capacitor can be used to momentarily change the threshold voltage of the ISFET. However, the change in the frequency decreases with respect to the change in the input voltage, which is consistent with the findings related to the reduction of sensitivity by the programable gate capacitor due to the increase in the total capacitance seen at the gate [44].

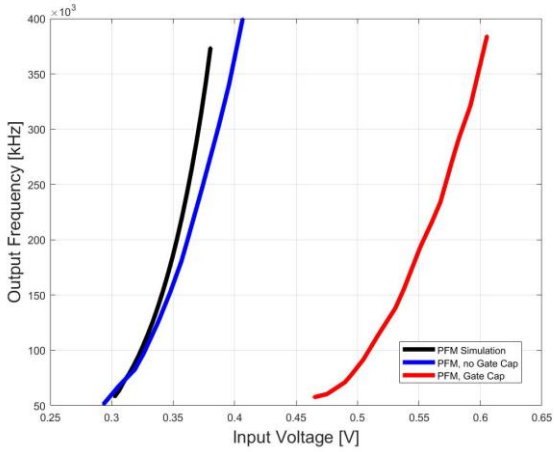


Figure 3.15 NPFM frequency output response against input voltage.

B. Chip CMOS-V2: NPFM-2

The optimised version of the nonlinear PFM was characterised and compared to the simulation data. Figure 3.16 shows how the train of pulses reaches 0 V every time the capacitor discharges beyond the threshold voltage, which means the capacitor has enough time to fully charge before a change of state by the digital switch. However, as shown in the simulation data, the delay time can easily surpass the threshold voltage, limiting the architecture working region to a maximum of 100 mV of input voltage.

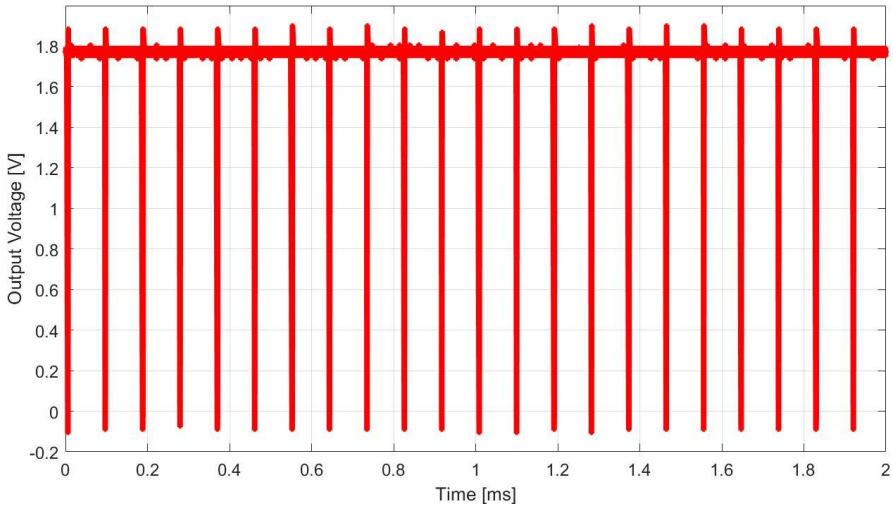


Figure 3.16 NPFM response of improved CMOS chip.

A complete characterisation of the output frequency against different input voltages was performed, using both an internally generated current source and an external voltage source to modify the threshold voltage value in steps of 300 mV. As shown in Figure 3.17, the results deviate from the simulation data regarding the correlation between V_{thres} and the saturation for different input voltages. This shows an inverse behaviour where a V_{thres} of 300 mV seems to have a wider linear range and higher saturation point. At the same time, a V_{thres} of 1.2 V quickly saturates at a maximum frequency of 160 kHz. The difference arises from the slow reaction of the design to the threshold voltage. The faster it works, the quicker C_{mem} reaches 0 V before it charges back to VDD because it now has a significant delay time that prevents a faster reaction. Therefore, saturation occurs first as it stops following V_{thres} properly. Nevertheless, the comparison concludes a similar maximum output frequency saturation and working region from 0.5 to 1 V input voltage, with good matching behaviour between the internal and external V_{thres} of 900 mV.

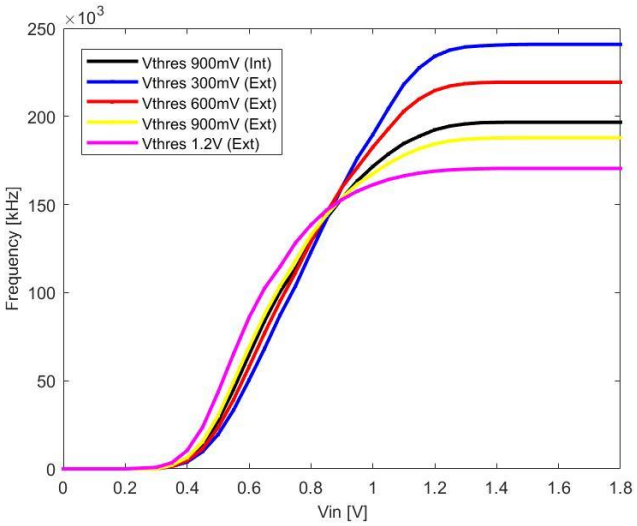


Figure 3.17 NPFM frequency output at different V_{thres}.

This architecture complies with certain characteristics of interest. It involves a simple design that can be used for pH detection with a low power consumption. The design provides a semi-robust digital output that is immune to noise and supports quick data acquisition for its analysis. However, as mentioned in the previous section, it comes with major disadvantages, such as the calibration required for the correct functionality, the extremely narrow range it needs to be in to work as expected, the balance required between the delay time and the charging/discharging phase of the capacitor, and the need for a lookup table due to the nonlinearity present, combined with the already difficult task of detecting pH in a solution.

3.5 Linear Pulse-frequency Modulation Architecture

3.5.1 Front-end Architecture

After considering the strengths and weaknesses of the PFM design, a different approach was adopted. The front-end architecture of the linear pulse-frequency modulator is shown in Figure 3.18. The circuit diagram consists of three distinct stages: a voltage-to-current (V-to-I) converter, a bidirectional current integrator, and a control circuit for feedback, which allows the charging and discharging of the membrane capacitor (C_{mem}). The ISFET corresponds to the positive input of the

differential transistor pair of the operational transconductance amplifier (OTA) in the V-to-I converter and C_{mem} represents the ability to store and release charge at different rates depending on the amount of current allowed to flow through it, partially emulating the behaviour of a cell membrane. This configuration allows the signal to be encoded in the frequency domain with a linear response to pH changes for the entire range [1].

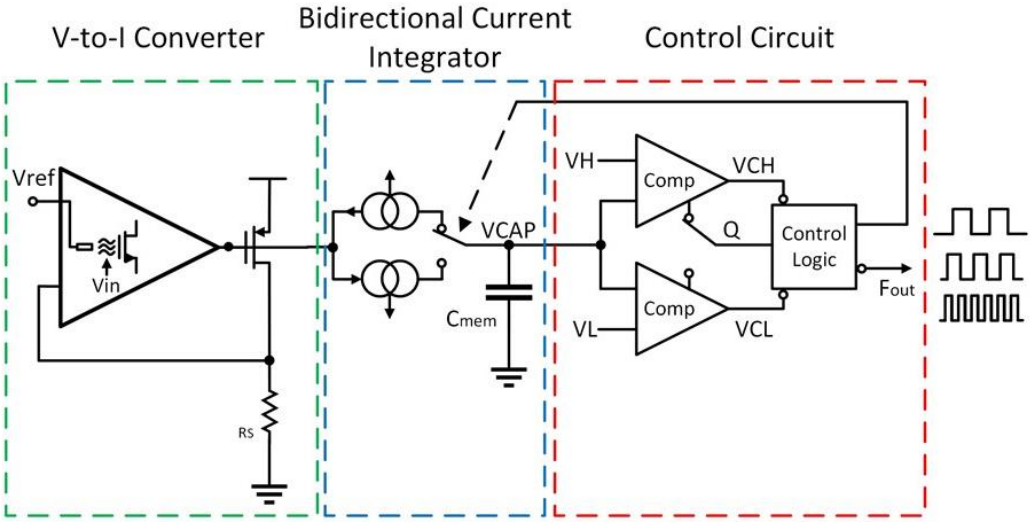


Figure 3.18 LPFM diagram-level schematic.

The architecture requires five analogue inputs, plus the reference electrode in the solution, as shown in Figure 3.19. Two inputs control the high (V_H) and low (V_L) voltages that determine the thresholds for C_{mem}. V_{GC} corresponds to one end of an extra capacitor connected to the gate, which is momentarily used to calibrate the input voltage range. The RST input is used to generate internal current sources through a bandgap voltage reference. The circuit works with a VDD of 1.8 V and has an average power consumption of 144.2 µW, considering standard setup conditions (V_{bias}: 700 mV, V_H: 1.2 V, V_L: 600 mV and V_{CG}: 0 V; V_{pH}: 7 V and V_{ref}: 300 mV for the Veriloga model.

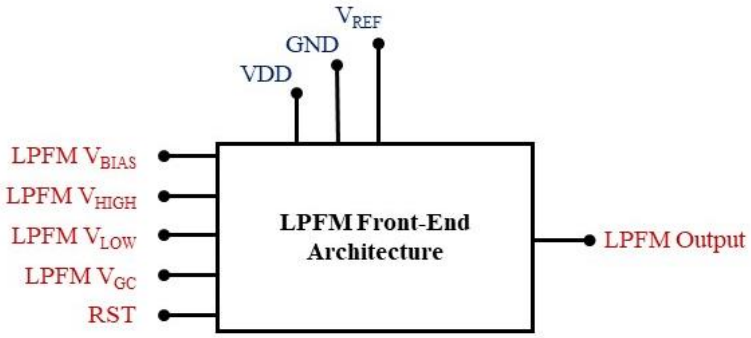


Figure 3.19 Schematic representation of LPFM architecture control block.

The V-to-I converter, shown in Figure 3.20, is based on an OTA common source amplifier. This two-stage amplifier allows a rail-to-rail voltage operating range to keep a wide linear range. A conventional resistor-capacitor circuit (RC) compensation design is incorporated between A and B to prevent undesirable peaks and oscillations in the frequency response. The converted current is mirrored through a bidirectional current integrator to allow C_{mem} to charge and discharge through M1 and M2, creating a path for a controlled charge-discharge phase. V_H and V_L set the higher and lower voltage limit for the capacitor through the control circuit, which consists of two high-speed differential pair comparators followed by a delay stage and a NAND-based set-reset (RS) flip-flop (more details of the control logic in Appendix B.2), which is behind the logic for the charging and discharging phase with a 50% duty cycle. Finally, Q controls the status of the comparators, making only one of them work at a time.

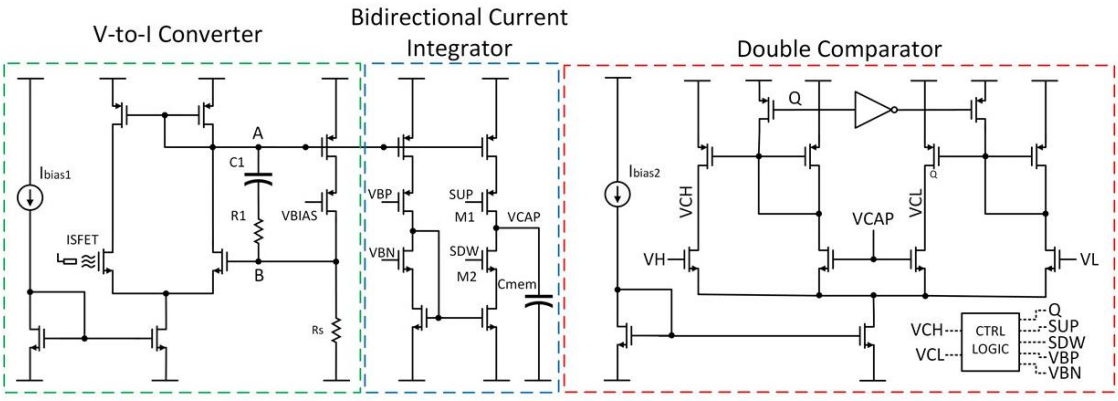


Figure 3.20 LPFM transistor-level schematic.

The output frequency of the pulse can be defined by the linear relationship between the input voltage and output current of the V-to-I converter, which is used to charge/discharge C_{mem} at the same rate, following the equation:

$$F_{out} = \frac{V_{in}}{2 * G * C_{mem} * R_s * (V_H - V_L)} \quad (2)$$

where G corresponds to a scaling factor of 10. V_H and V_L can be tuned to work in a specific voltage range (ΔV) to calibrate the desired frequency range, increasing the dynamic range of the frequency response when the ΔV decreases.

3.5.2 Simulation Results

Simulated results in Figure 3.21 show an output response with a 50% duty cycle, demonstrating the correct functionality of the architecture, as well as the charging/discharging phase of C_{mem}. This characteristic means that the device spends half of the time charging and half of the time discharging at a constant rate, which is a good indicator of the circuit's performance. It also makes communication easier for further signal processing. The architecture was tested for the entire pH range (1–14), showing a sensitivity that varies depending on the pH value. The higher the pH at the gate of the ISFET, the lower the current allowed to pass through it, resulting in a slower frequency response.

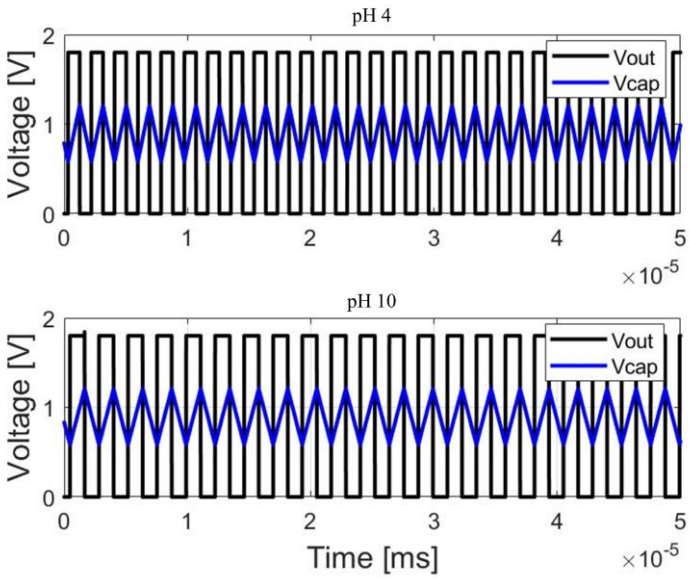


Figure 3.21 Simulated pulse output signal and C_{mem} voltage response for pH 4 and 10.

The frequency response depending on the voltage range between V_H and V_L is shown in Figure 3.22. The lower the ΔV, the faster the frequency response, reaching a maximum output of 2.3 MHz at a linear rate of 683 kHz/V. The linear sensitivity for a ΔV of 600 mV in the control circuit is 17.3 kHz/pH, with a linearity of 0.99934. The configuration allows a min-max sensitivity of 11.6–50.66 kHz/pH depending on the setup conditions. This is useful because it allows the architecture to increase the dynamic range of the output frequency response. It allows a higher sensitivity to pH changes so that sub-pH values can be measured with a higher degree of certainty. Depending on the requirements, working at a slower rate is also possible for less precise measurements and much lower power consumption to provide a longer shelf-life of the device in case it is required for battery-operated devices like in implantable applications.

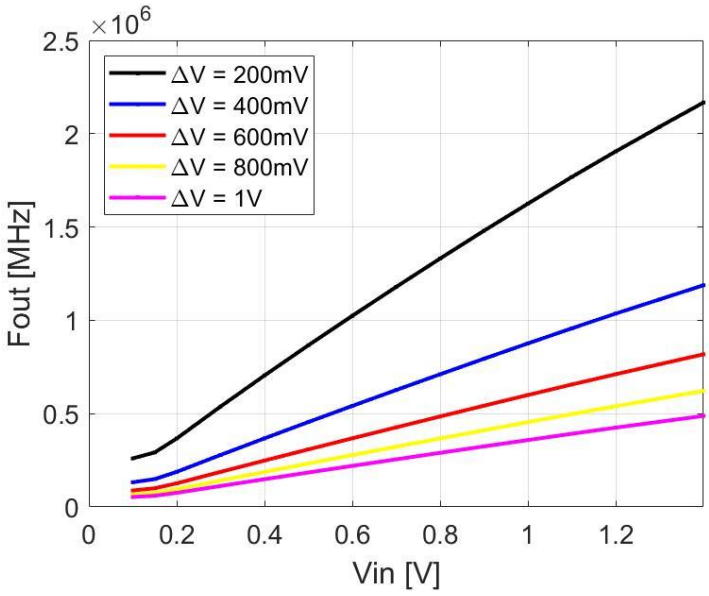


Figure 3.22 Simulation data of the frequency response for different ΔV between VH and VL.

A Veriloga ISFET model was incorporated to evaluate the frequency's behaviour at different pH values. Vin represents the voltage going into the gate of the ISFET. Figure *3.23* shows the output frequency from pH 1 to 14, considering a Si_3N_4 sensing layer as a 30 mV/pH sensitivity response. The ISFET model allows the user to determine the sensitivity response using a scaling factor. The differences between the NFPM and the LFPM are linearity, the possibility of using this design for the entire pH range, and the wider working range. This allows the user to calibrate which region of interest better

suits the application of interest by using the lower or higher end of the input voltage range.

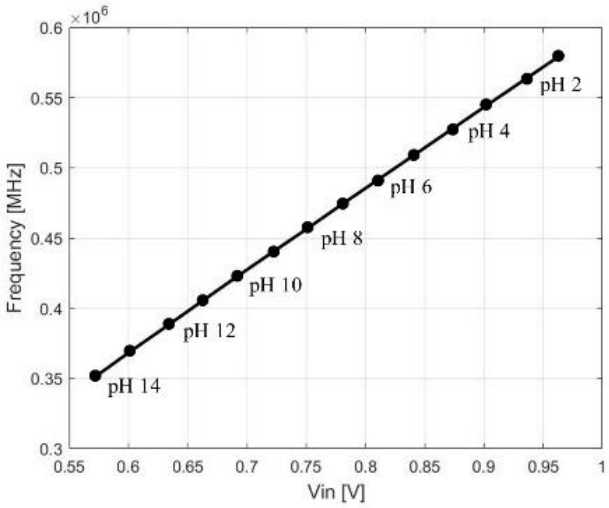


Figure 3.23 Output frequency for different pH values using the Veriloga model.

Due to the versatility and applicability of this design for pH detection, a more extensive analysis was performed. Figure 3.24 presents the circuit's response for a wide variety of supply voltages. This characteristic is especially relevant for wireless implant applications where the received power can vary widely depending on the position and orientation of the sensor. The results show that, despite a slight drop in the output frequency, the circuit can work robustly down to 1.4 V. The power supply rejection ratio (PSRR) was determined at 1.6 V and showed a magnitude of 75.91 dB.

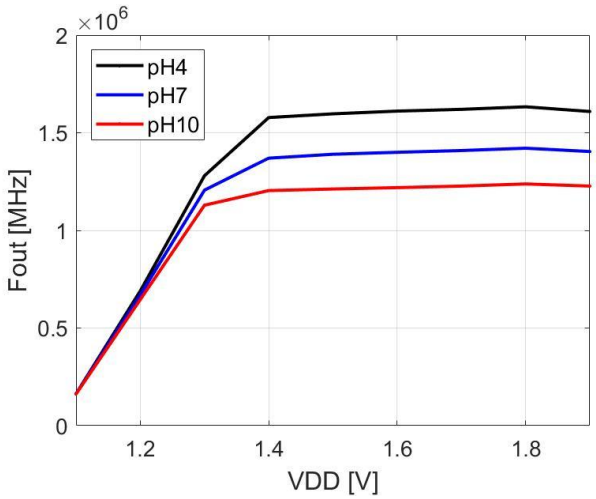


Figure 3.24 Output stability with a ~25% power supply variation.

The circuit was also simulated for transient noise with different noise scale factors (NSF), which is a feature that artificially inflates the small noise present in the design to make it visible over the transient analysis. Figure 3.25(a) shows the temporal response for an expected value of 473.6 kHz output for pH 7, with a minimum average variation of 200 Hz. A similar time domain noise simulation plots the power spectral density (PSD) for three pH values in Figure 3.25(b). The fundamental waves correspond to the expected frequency for each pH and can be easily distinguished. It is essential to clarify that this noise differs from the electrochemical noise present during the testing phase, as it only relates to sources originating from the ISFET structure.

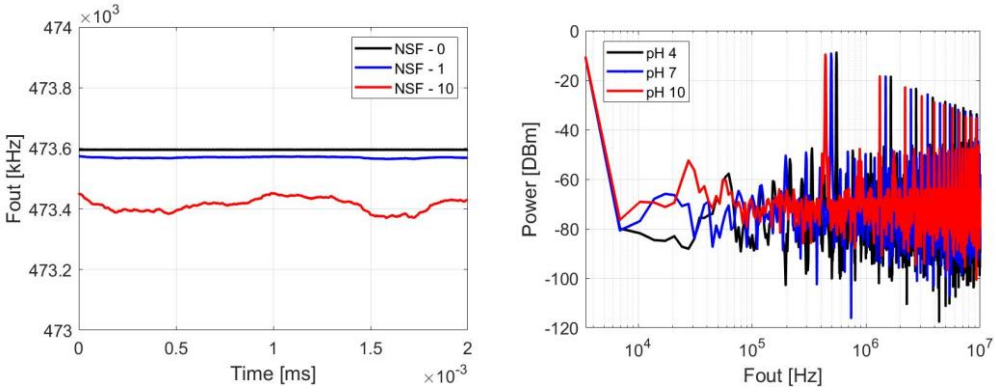


Figure 3.25 a) Frequency variation with a noise scale factor (NSF) of 0, 1 and 10; and b) power spectral density (PSD) of the frequency response at different pH values

A Monte Carlo simulation for mismatch was also performed to analyse the response for the entire pH range in 50 runs each. The resulting histogram plot is shown in Figure *3.26*. The mean frequency remained close to the expected value for each pH, with an average standard deviation of 567.76 Hz, showing remarkable consistency against mismatch variations. However, it is acknowledged that process variations can still affect the output response. This can be reduced by using the adjustable frequency feature to isolate the peaks or by using an array of pixels to get an average of a data group instead of single data points.

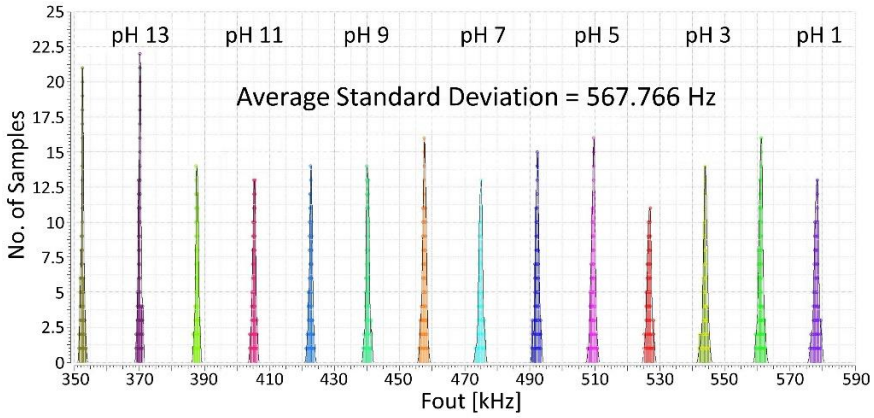


Figure 3.26 Monte Carlo analysis of frequency output for the entire pH range.

This architecture is of particular interest for implantable applications. It provides a robust digital output with a fixed duty cycle. This reduces the consequent signal processing for data manipulation; the adjustable frequency increases the dynamic range, making it suitable for sub-pH detection. The system can also get a steady frequency response even with a ~25% variation in the power supply voltage. The architecture, however, involves a more complex design that inevitably increases the power consumption and occupied area, which are relevant for future improvements.

3.5.3 Layout Design

The sensor was implemented in 0.18 µm CMOS TSMC Logic or MS/RF, General Purpose 1.8 V / 3.3 V technology; the layout is shown in Figure 3.27. The sensing area was kept as an extended gate the same size as the previous design. The readout instrumentation is complemented with two bias current sources through a bandgap voltage reference and a programmable gate capacitor for trapped charge compensation. It is important to highlight that two diodes were placed, one on each side of the programmable gate capacitor, to comply with antenna rules imposed by the technology. The total area of the architecture corresponds to 220 µm × 410 µm. A micrograph of the fabricated chip is shown in Figure 3.28, where the features in metal-6 can be seen.

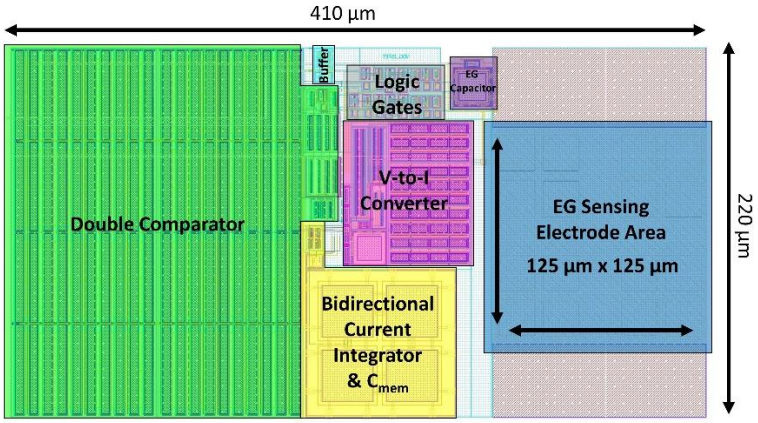


Figure 3.27 LPFM architecture layout.

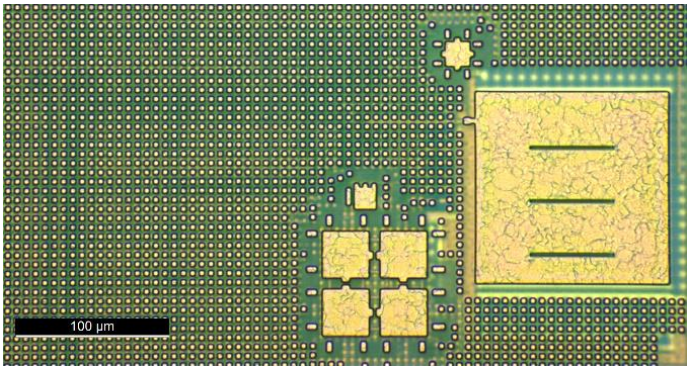


Figure 3.28 Micrograph of the fabricated LPFM architecture in the chip.

3.5.4 Electrical Characterisation

Electrical characterisation was performed and compared to the simulation data. Figure *3.29* shows the output response with a 50% duty cycle, consistent with the expected outcome according to the simulation. The output frequency changes depending on the value of the input voltage, showing a linearity of 99%. The working region of interest covers a wide input voltage range, from 150 mV to 1.4 V, making it much easier to calibrate, and this can be used to detect the entire pH range, which should cover a maximum of 840 mV considering an ideal Nernstian response of 59 mV/pH.

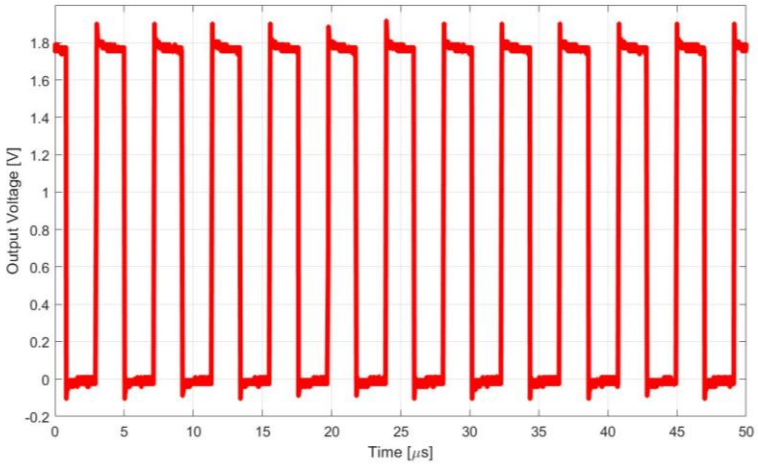


Figure 3.29 LPFM pulsed output signal response.

The system's linearity with steps of 200 mV in ΔV to up to 1 V is shown in Figure *3.30* for two different CMOS chips. The adjustable frequency feature works as expected by modifying the dynamic range depending on the high and low voltages provided to the system. The difference between chips, although present, varies less than 5% from each other's results. The design allows the user to determine the dynamic range to work with, considering that the faster the system works, the greater the power consumption and inconsistencies between individual measurements. Using an array of pixels to average the frequency response can give repeatable and accurate values for pH variations, even for the higher output frequencies. This is the next step to consider in evaluating these designs.

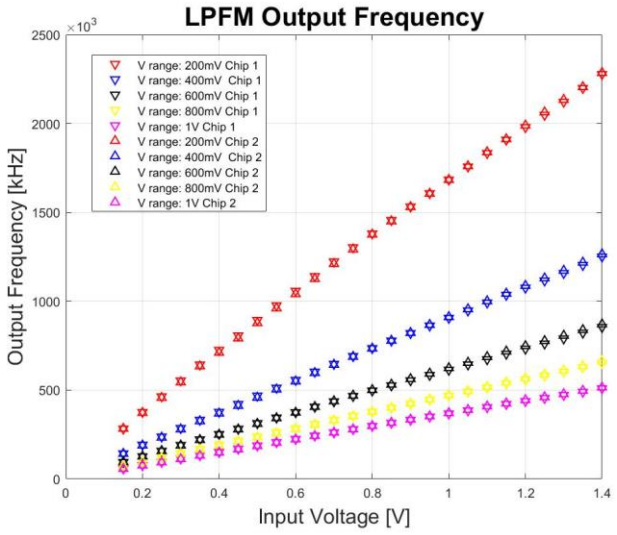


Figure 3.30 Electrical characterisation of the LPFM architectures with different ΔV.

3.6 Summary

The design and fabrication of both architectures in two different tape-outs were described in detail. The nonlinear pulse-frequency modulator was fabricated using 0.18 µm CMOS TSMC High Voltage BCD Gen II for the first prototype and 0.18 µm CMOS TSMC Logic or MS/RF, General-Purpose 1.8 V / 3.3 V for the final version, as well as the linear pulse frequency modulator, with both designs in the same chip. The architectures were described in detail, and a discussion of each design's advantages and disadvantages was presented during the simulation and electrical characterisation analysis. The nonlinear PFM was the first design manufactured that transduced an electrochemical signal to a frequency signal. However, the difficulties, especially the calibration steps, led the work to look for a similar architecture with better properties. The linear PFM kept most of the advantages in the nonlinear version and included more benefits, making it the design of choice for the following testing with buffer solutions. The nonlinear PFM, although promising for sub-pH detection in a very specific working region, was set aside to focus entirely on the LPFM, which shows better characteristics for pH detection, like linearity, stability over power supply reduction, and immunity to transient electronic noise, as well as easier calibration for its operation.

Chapter 4

CMOS Chip: Post-processing

4.1 Introduction

Throughout this chapter, the post-processing of the CMOS ISFETs will be described to evaluate the sensitivity response with different sensing layers or thicknesses. The chapter will discuss three different scenarios and their microfabrication methods. From unmodified chips to adding an extra layer of Ta_2O_5 for better sensitivity and low drift over time [111], these methods are not typically supported by a commercial foundry and even more so at a singulated chip level. The main section will focus on thinning the original passivation layer to different thicknesses to compare the effects of each case on the sensitivity. Although this was previously demonstrated by [94] on AMS technology, this is the first time the results have been shown on TSMC technology. Finally, some packaging and encapsulation techniques will be addressed to enable the use of the CMOS chips in wet environments, while still preserving the electrical connectivity and response.

4.2 ISFET Sensitivity

CMOS ISFET chips are shielded by a layer of Si_3N_4/SiO_2, known as the passivation layer, which comes into contact with the analyte solution. Researchers have explored various materials for this passivation layer over the years to enhance the sensitivity towards targeted ion concentrations. One promising option is Ta_2O_5, which exhibits a nearly ideal sensitivity in terms of the Nernstian response, measuring 59 mV/pH, as reported in [144]. The sensitivity of this particular layer stands out because it has a high surface charge density, which means it can interact effectively with ions in the surrounding solution; it forms a stable and high-quality oxide layer when deposited in silicon substrate, which is essential for the ISFET operation as it acts as a dielectric; and it has a relatively high dielectric constant, enhancing its ability to respond to changes in surface charge due to ion concentration in the solution [144] [145]. In the

following sections, three scenarios will be described. A post-analysis of the processing methods will be discussed in the next chapter regarding the sensitivity of the ISFETs in each case, highlighting their advantages and disadvantages.

4.3 Post-processing and Microfabrication Techniques

4.3.1 Unmodified Silicon CMOS Chip

One of the easiest ways to assess the sensitivity of CMOS chips is to test them unmodified since the passivation layer functions as the sensing layer. The literature has demonstrated that Si_3N_4/SiO_2 layers can provide an average sensitivity of 30 mV/pH under the right conditions [7], making them a tentative approach as no further processing is required. However, evidence of the materials and thicknesses of the current layers on the surface of the manufactured CMOS chips was needed to proceed with the post-processing methods. This data determined some of the steps to follow for the etching and thinning of the sensing layer.

TSMC provides a generic overview of the stacked backend-of-the-line (BEOL) metal layers, summarising each layer's thickness and material. Figure 4.1, which was recreated from TSMC documentation, gives an insight into the passivation layer, which includes three different processes: the deepest layer consisted of the deposition of SiO_2 in a high-density plasma (HDP) system through plasma-enhanced chemical vapour deposition (PECVD) using argon plasma enhanced source depending on the thickness of the top metal, which in this case was 8 kÅ top thick metal, for a thickness of 10 kÅ; the following two layers comprised a generic deposition of SiO_2 and Si_3N_4 through chemical vapour deposition (CVD) for a thicknesses of 1.5 kÅ and 6 kÅ respectively. An additional layer of photo-definable polyimide PI-8124-ER with a thickness between 9.2–40 kÅ after curing can be supplied upon request by the foundry, but this was not the case for this tape-out.

Passivation Layer		
PASS 1	Material	SiO2 (HDP using Argon Plasma Source)
	Thickness	10kÅ = 1 µm
PASS2	Material	SiO2 (PE-OX)
	Thickness	1.5 kÅ = 0.15 µm
PASS3	Material	Si3N4 (PE-SiN)
	Thickness	6kÅ = 0.6 µm

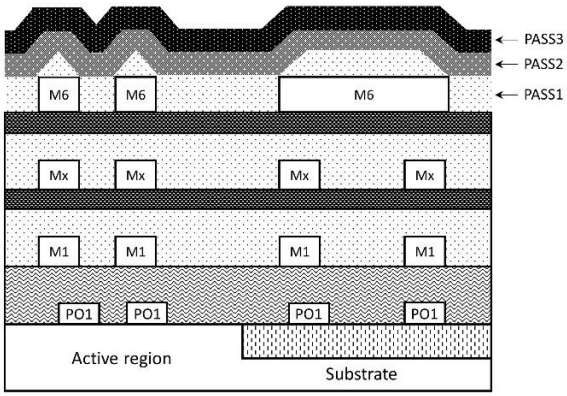


Figure 4.1 TSMC documentation for passivation thickness.

The next step for verification of the chip's surface was to get a cross-sectional view of the layers and composition analysis of the materials to compare to the data provided by the foundry. For this process, the ZEISS Crossbeam 550 Focused Ion Beam – Scanning Electron Microscope (FIB-SEM) [146] with a cryogenic attachment from Quorum Technologies was required, one of only a few available in the UK, as shown in Figure 4.2. The benefit of using this equipment comes from the possibility of performing an energy dispersive X-ray composition (EDS/EDX) to analyse the composition of the elements located on the surface of the chip, as well as the visual analysis of the thickness of the corresponding layers of interest.

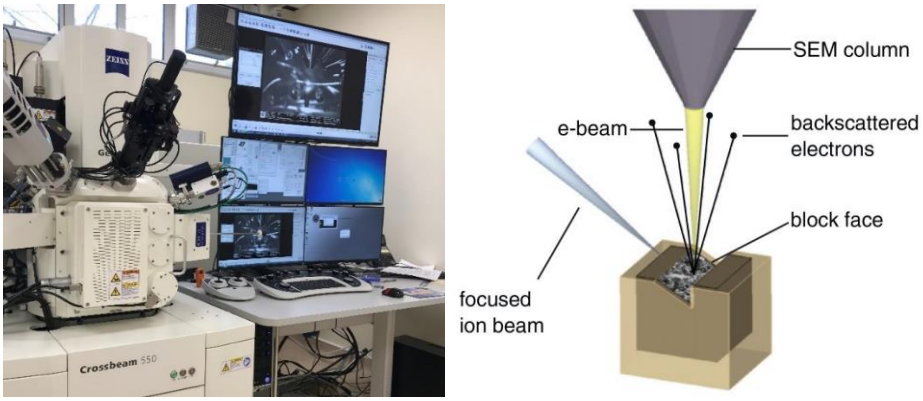


Figure 4.2 ZEISS Crossbeam 550 FIB-SEM.

Two chips were provided for the analysis. First, the samples were glued to a carrier and transferred to a sample holder. The sample was then sputter-coated with 2 µm of platinum with an argon gas supply of 0.7 bar and purity of 6.0 (99.9999%) in the cryo preparation chamber. This protects the sample from high-energy ions during imaging

with either the electron or ion beam and reduces charging effects caused by the ion beams during the FIB milling, followed by polishing the crystal surfaces prior to data collection for higher signal-to-noise ratio and resolution [147]. The sample was then transferred to the ZEISS crossbeam chamber, a highly stable cold stage used for milling and acquiring high-resolution images at < -140 °C. Next, the FIB was used to mill out a trapezoid-shaped trench, enabling the viewing of a flat and smooth cross-section using the SEM. This could then be used to measure the thicknesses of all the layers, as long as they were between 5 nm and 50 µm [148] [149]. Finally, the raw images were recorded using a tilt correction of 54° to have a cross-sectional view of the layers.

Figure 4.3 shows the cross-sectional view of the samples provided. Five layers can be identified: the aluminium of the top metal layer at the bottom; the SiO_2 layer with a thickness of 1.242 µm; the Si_3N_4 layer with a thickness of 0.527 µm; the addition of the 2 µm platinum layer; and the polished platinum surface at the top, confirming the information provided by TSMC about the thickness of the passivation layer.

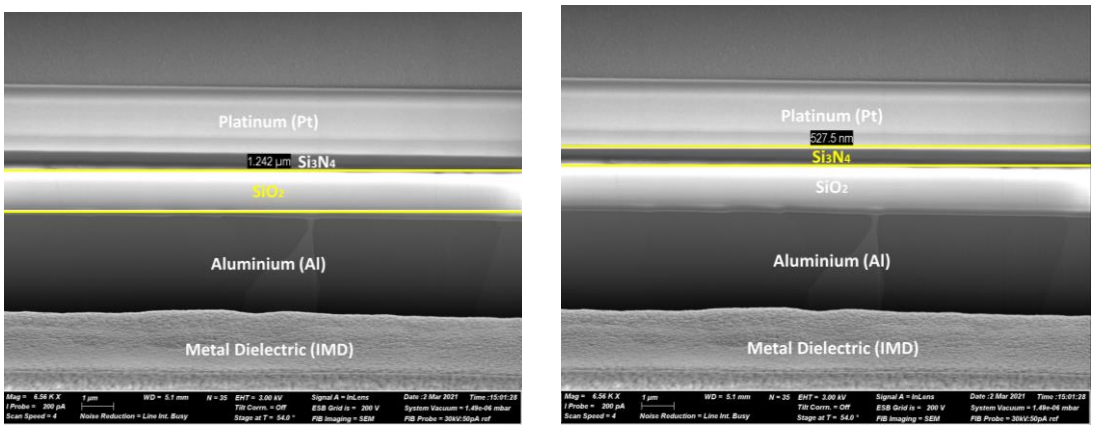


Figure 4.3 Micrographs of a cross-sectional view of chip samples with FIB/SEM.

An EDS/EDX for elemental composition analysis was performed regarding the materials. An EDS measures the elemental composition of a given scanned region at a pixel level. By analysing the X-rays that are generated when the primary electron beam stimulates atoms in the outermost 100 nm of the sample, the EDS is able to match these X-rays to elements from the periodic table and determine the atomic concentration of each element based on the intensity of its corresponding X-ray signal. [150] [151]. Figure 4.4 shows the elemental composition analysis of the samples. The

spectrums, labelled from 4 to 7, correspond to the elements expected in each layer, going from platinum to aluminium, and correctly identifying the presence of Si_3N_4 and SiO_2 from top to bottom.

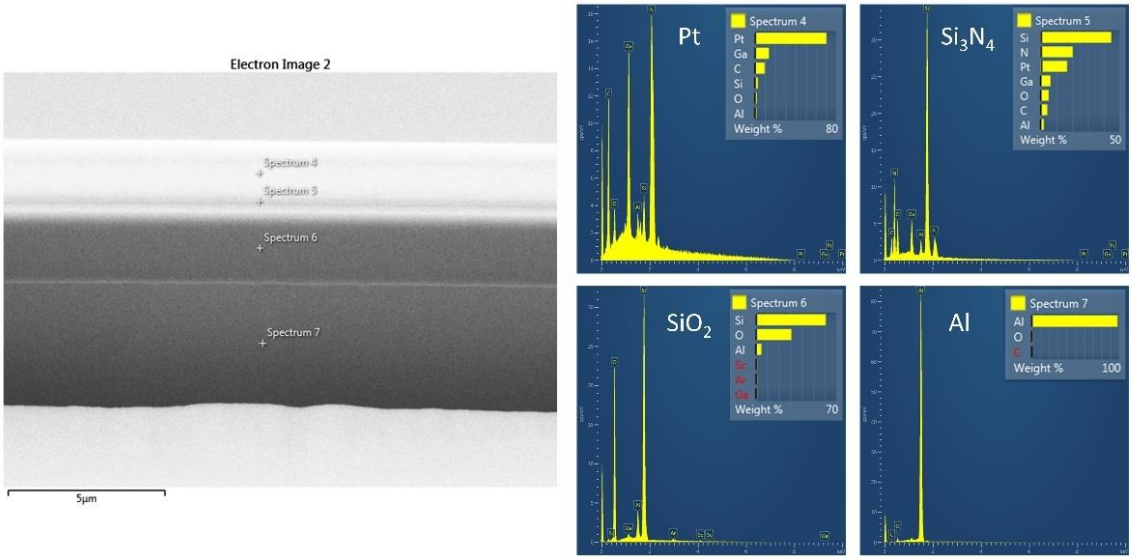


Figure 4.4 Energy dispersive composition (EDS) for elemental composition analysis.

4.3.2 Tantalum Pentoxide Deposition

For the deposition of Ta_2O_5, two different cases were developed. The platform used for this process corresponds to the CMOS-V1, NPFM-V1, where the nonlinear PFM design was included. Ten chips were post-processed in two groups: half had the passivation layer removed, while the other half did not. The literature has demonstrated that a sensing layer of Ta_2O_5 can provide the closest results to a Nernstian response [152]. Evidence has also shown that using multiple sensing stack layers can further improve the sensitivity of the devices [153]. The baseline of the post-processing steps for the etching and lift-off methods was developed by [154] in the Scottish Microelectronics Centre (SMC) cleanroom facilities, and a few modifications were made to make them suit the specifications of TSMC technology. For the Ta_2O_5 deposition, the Plassys MP 900S DC/RF Sputtering Tool in the James Watt Nanofabrication Centre (JWNC) in Glasgow provided standard recipes depending on the thickness required.

A. Etching Process

For the first batch of five dies, an etching technique was the initial post processing step to remove the passivation layer from the top of the sensing areas of 125 µm × 125 µm. The chips were placed in groups of two on a 4-inch wafer carrier. Megaposit SPR 220-7 photoresist was placed underneath, and a heat treatment was applied for 30 min at 90 °C in a hot plate to stick the dies in a fixed position. This was done to handle the full wafer instead of each chip, avoiding possible damage in the process as most of the tools were compatible with wafer processing. The wafer was then placed in a chamber with hexamethyldisilane (HMDS) for 10 min to improve the adhesion of the photoresist to the surface. Subsequently, two spraying passes of SPR 220-7 photoresist diluted with methyl-ethyl-ketone (MEK) and propylene-glycol-methyl-ether-acetate (PGMEA) were applied using the EVG 101 Spray Coater to coat the surface of the dies, giving a total thickness of 10 µm of photoresist to have enough margin for the upcoming etching without affecting the rest of the passivation layer. The photoresist mixture consisted of 6.5 % SPR 220-7, 68 % MEK and 25.5 % PGMEA A soft bake was performed on a hot plate for 90 seconds at 90°C.

For the photolithography, a virtual mask was designed to be 50 µm smaller per side than the sensing area (75 µm × 75 µm). This mask was aligned with the area of interest before the chips were exposed to ultraviolet light (wavelength of 385 nm) with a light emitting diode (LED) light source using the Durham Magneto Optics (DMO) MicroWriter ML3 with an exposure dose of 525 mJ/cm^2. The chips were developed for 60 seconds using the Megaposit MF26-A developer and then rinsed with deionised water (DI) and dried with N_2. After a quick inspection, a hard bake was applied for 60 seconds at 115 °C. The next step was removing the passivation layer using the JLS RIE 80 Etching System, which includes an automatic computer-controlled RF and reactive ion etching system that can accurately control etch depths. The parameters for the etching process are shown in Table 4-1 [154]. The process took 60 minutes to remove the entire passivation layer, which includes both the Si_3N_4 and SiO_2. Finally, the chips were removed from the wafer and cleaned from the photoresist using acetone,

isopropanol and DI water, followed by nitrogen (N_2) drying. The cross-sectional schematic diagram of the technique is shown in Figure 4.5.

Parameter	Specs
Runtime	60 min
RF Power	150 W
Pressure	60 mT
Gases	O2: 4sccm CF4: 60sccm

Table 4-1 JLS RIE 80 conditions for the etching process of CMOS chips.

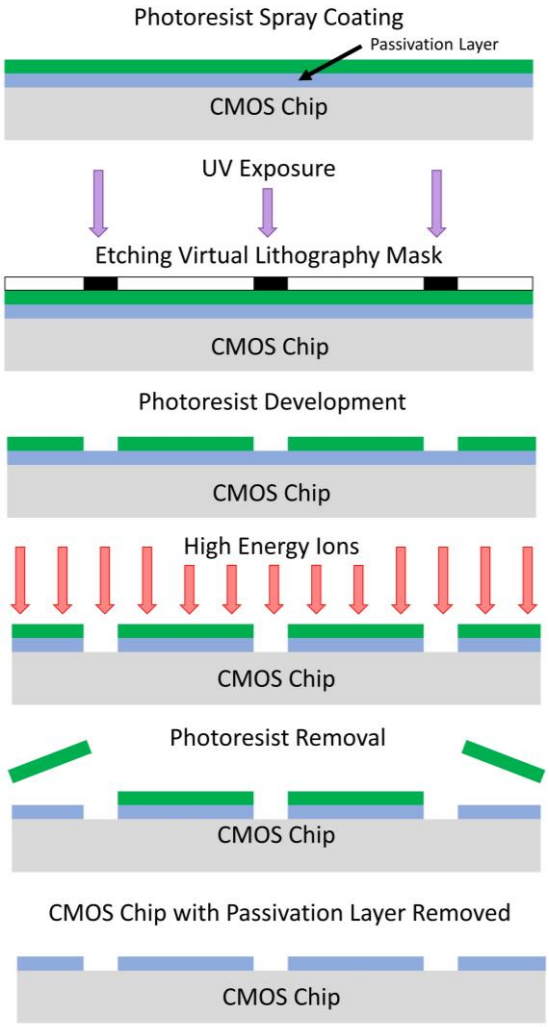


Figure 4.5 Schematic diagram of the etching technique to remove the passivation layer over the electrodes of a CMOS chip.

As a verification method at the end of the process, a NanoSpec 3000 was used to confirm that no passivation layer remained on top of the sensing areas. The

device requires calibration using a clean wafer, and the software allows the measurement of the thickness of SiO_2 over the pads of aluminium, showing no signs of SiO_2 and therefore Si_3N_4 if the post-processing method is correctly performed.

B. Metal deposition and lift-off process

The next post-processing step for the whole group of chips was the deposition of a metal oxide and lift-off technique, which is a method of patterning a target material (typically a metal) using a sacrificial layer (typically a photoresist) to define a pattern. The dies had a similar treatment to that described above, with the difference that the chips were placed in individual pieces of a wafer and coated with only one spraying pass of photoresist, giving a thickness of 5 µm. The patterns were then developed on top of the electrodes with a virtual mask of the same size as the electrodes, and the chips were packed and transported to the cleanroom facilities at the JWNC. Figure 4.6 shows the difference between the virtual masks used for the etching and lift-off processes compared to the area of the electrodes.

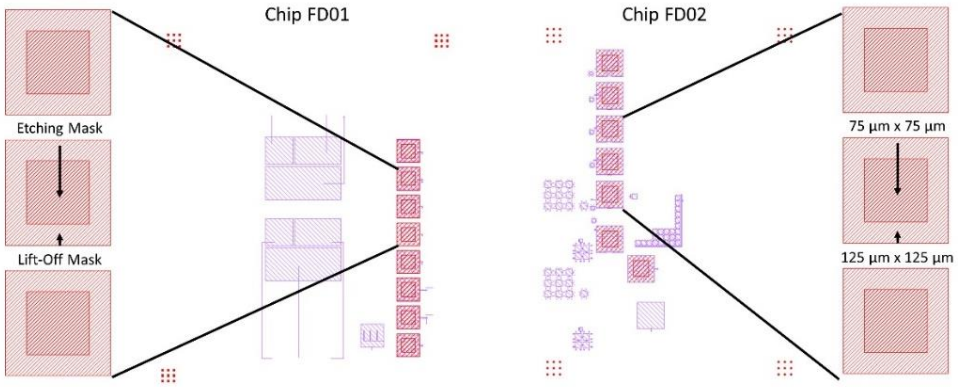


Figure 4.6 Virtual masks designed for the etching and lift-off process for both tape-outs.

The chip carriers were placed in a sample holder and into the chamber of the RF sputtering tool, which employs a thin film deposition technique that involves bombarding the surface with energetic particles to eject target material. The target material was located at the cathode, while the substrate was situated at the anode. High energy positive argon ions, accelerated by an

RF electric field, struck the target, and the atoms that are ejected were transferred to the substrate, where they condensed to create a thin film [155]. In order to deposit compounds such as oxides, nitrides or carbides, a reactive gas was introduced to the target material in the reactive sputtering process. A standard recipe to deposit 100 nm of Ta_2O_5 was applied, with the specifications shown in Table 4-2 [116]. The chips were then removed from the equipment to complete the lift-off process using a Microposit Remover 1165, leaving the desired pattern of Ta_2O_5 on top of the electrodes and removing the rest of the photoresist with Ta_2O_5 using acetone and an ultrasonic water bath, followed by isopropanol, water and N_2 for drying. The schematic diagrams of both cases, with and without the passivation layer, are shown in Figure 4.7. A list of all the reagents and their manufacturers can be found in Appendix D.

Parameter	Specs
Runtime	55 minutes
RF Power	300 W
Working Pressure	100 µbar / 75 mTorr
Gas Mixture Ratio	9:1 sccm (Ar:O_2)
Chamber & Substrate Temp	20 °C

Table 4-2 RF sputtering conditions for Ta_2O_5 film deposition in CMOS chips.

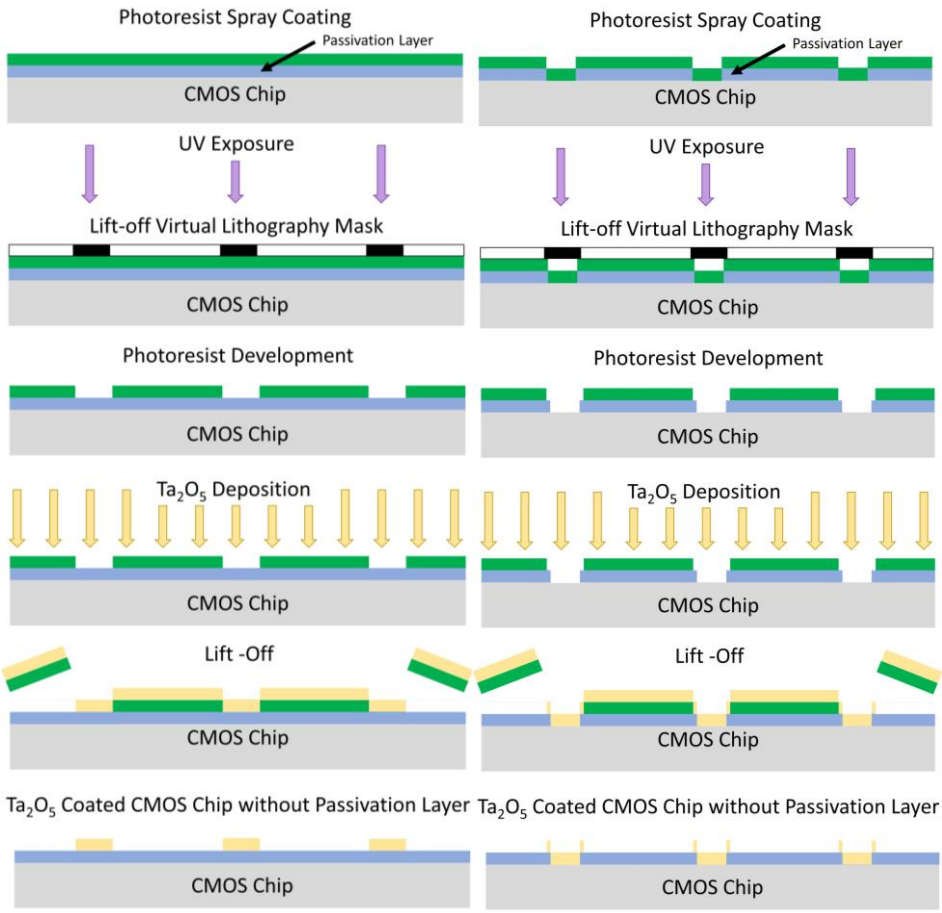


Figure 4.7 Schematic diagram of CMOS chips' metal deposition and lift-off techniques for both cases. Right side: CMOS chip with passivation layer. Left side: CMOS chip without passivation layer.

Figure 4.8 and Figure 4.9 show the outcomes of the Ta_2O_5 deposition, demonstrating the differences between the two cases. The first batch of CMOS chips had the passivation layer removed from the top of the sensing areas with a smaller window, to then deposit the target material. In contrast, the second batch only required the Ta_2O_5 deposition. The surface of the sensing areas looked smooth and clear.

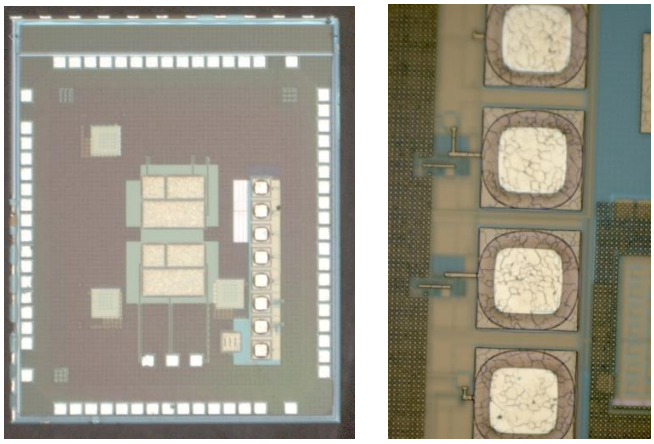


Figure 4.8 Ta_2O_5 deposition in first batch without passivation layer.

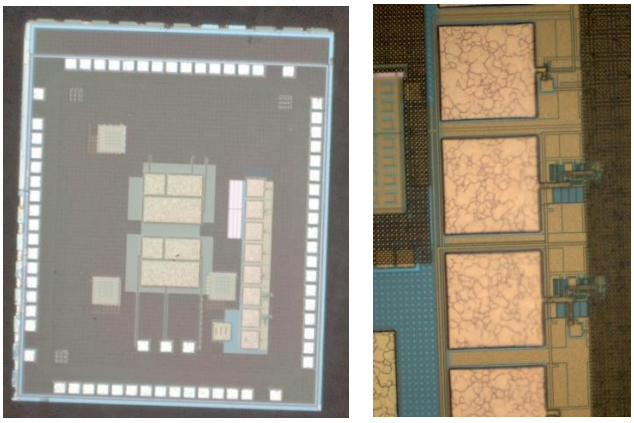


Figure 4.9 Ta_2O_5 deposition in second batch with the passivation layer.

Ta_2O_5, as a sensing layer, offers better properties than Si_3N_4, such as better immunity to interference ions, higher sensitivity, no degradation from surface oxidation, lower drift over time, and higher chemical resistance [152] [156]. However, an excellent sensitivity depends on the following factors: surface roughness, which comes from the pressure inside the chamber when the sputtering process happens [157], and several oxygen sites on the sensing membrane surface, which can be modified depending on the chemical atomic ratio Ta:O. Using a ceramic target with non-reactive sputtering only requires a tiny amount of oxygen atoms to compensate for the loss of these molecules during the deposition [158]. Finally, the thickness of the layer depends on the RF power and duration of the sputtering process, where the literature has shown that between 50 and 120 nm of thickness is ideal for pH sensing [159] [160].

4.3.3 Si_3N_4 Passivation Layer Thinning

The final post-processing protocol involved thinning the original passivation layer deposited by the foundry. According to [94], one way to significantly improve the performance of CMOS ISFET sensors is by reducing the Si_3N_4 layer very close to the limit, leaving a thin Si_3N_4 film in contact with the SiO_2 underneath. Using a reactive ion etching system to gradually remove the top passivation layer of the surface, they were able to show a 125% improvement in pH sensitivity, a 5,700% increase in the passivation capacitance, and a 96% decrease in capacitive attenuation.

The CMOS chips used for this study differed slightly from the ones analysed in this work. These were fabricated in 0.35 µm Austria Microsystems (AMS) technology, a 4-metal process with a different passivation layer thickness. Their manufacture included an additional polyimide layer on top of the Si_3N_4. Therefore, the etching recipe suggested in this study was designed considering the presence of the polyimide layer. The proposed gas composition was 50% oxygen (O_2) and 50% sulphur hexafluoride (SF_6) to reduce surface roughness by creating stronger bonds C-F than oxygen C-O, leading to a slower etching time [161]. It took ten minutes to remove the polyamide layer and less than five minutes to go through the Si_3N_4 layer before it reached the SiO_2 layer.

The RIE recipe used for this study, shown in Table 4-1, corresponds to [154], with a gas composition equal to 6.25% O_2 and 93.75% carbon tetrafluoride (CF_4). This recipe has shown higher efficiency in selectively etching Si_3N_4 over both SiO_2 and Si, making it ideal for reducing the top layer while maintaining the integrity of the SiO_2 underneath and a good surface roughness for post-analysis of the functionality of the pH sensing device [162]. However, one possible downside is related to the etching speed, as the Si_3N_4 sensing layer has a thickness of 1.242 µm according to the analysis shown in previous sections, and several experiments performed concluded that the recipe etches the entire layer in less than five minutes, limiting the ability to reach precise thicknesses. Nevertheless, for these initial experiments, the results were promising regarding the expected change in the sensitivity, and this will be analysed in the following chapter. Further research should be done into slow the etch rate

process to better control the desired thicknesses by reducing the RF power, for instance.

This work considered six cases: unmodified chips and etching times of 1, 3, 5, 7 and 15 minutes. In order to assess the quality of the RIE etching, CMOS chips were inspected under a microscope, as shown in Figure 4.10. The dies were post-processed to selectively etch the passivation layer on top of the sensing area only. The colour variations indicate different etching times, changing the light interference characteristics.

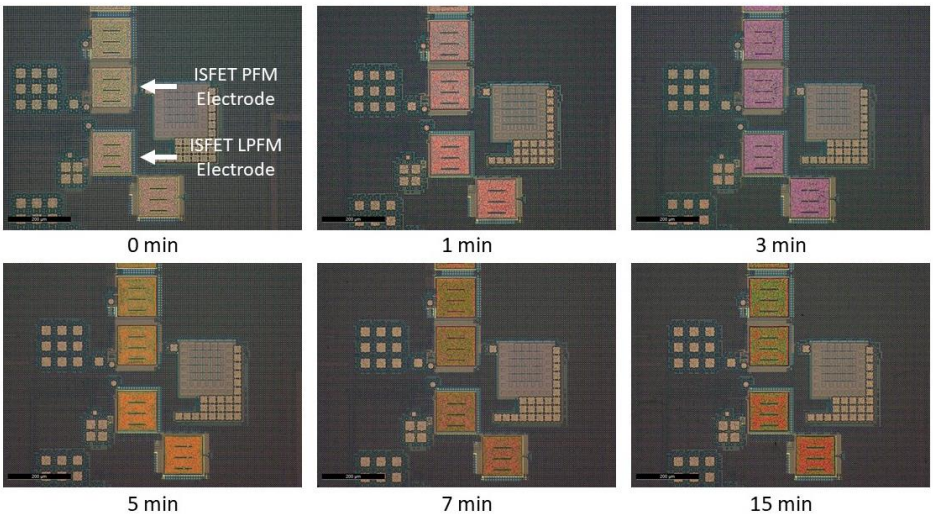


Figure 4.10 Micrographs of the CMOS chip's surface for different etching times.

A Bruker Dektak XT profilometer was used to scan the CMOS chips' surface to extract each layer's remaining thickness until the SiO_2 layer was reached. Figure 4.11 shows the results for the first four post-processed cases. The analysis consisted of a scan that covers a line on top of the sensing area of an extended gate, having an unmodified device as a reference. It is important to clarify that, in Figure 4.11 c), the scan was performed over the slots required by the technology for large metal extensions, representing three places inside the sensing area that went below the average surface. None of the other scans were performed over these slots. The graphs also show that the etched window is smaller than the actual size of the sensing area, with the edges remaining intact, a feature contemplated by design for subsequent metal deposition in the area of interest. The Si_3N_4 was removed by approximately 40% during the first minute, while 80% was gone after three minutes. The last measurement performed was

on the dies with five minutes of etching time, as it went beyond the Si_3N_4 and into the SiO_2, which will significantly reduce the expected sensitivity according to the literature [94]. Therefore, considering the depth of the five-minute etching, the cases of seven and fifteen minutes should not give any response to the voltage provided through the reference electrode, as they went deep into the SiO_2. The scans were replicated in 2 CMOS chips per case that underwent the same post-processing, observing similar results around the mean in each case.

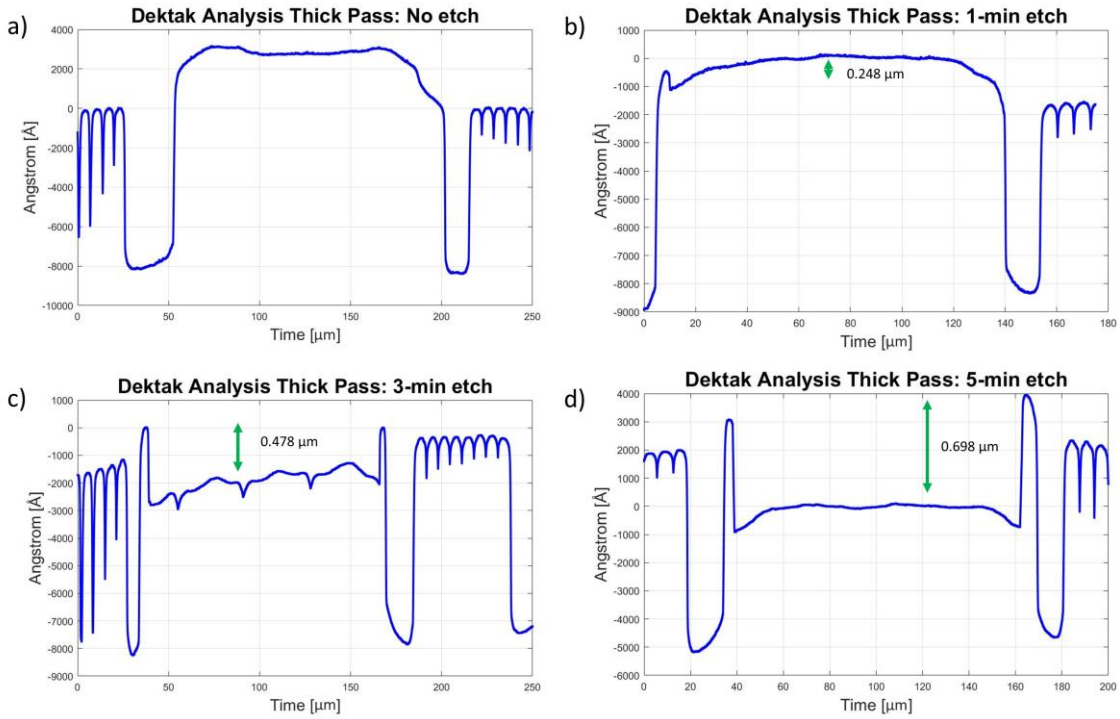


Figure 4.11 Dektak analysis to evaluate the thickness of the passivation layer with different etching times. a) Unmodified chip; b) 1 min etch; c) 3 min etch; and d) 5 min etch.

Figure 4.12 shows a graph of the etching time against the passivation thickness in µm with a representative view of the Si_3N_4 and SiO_2 layers according to the previous data. The last two cases (seven and 15-min etch) went very deep into the SiO_2. Further testing in these cases confirmed the insensitivity to pH, as both cases showed no response against a voltage input to the reference electrode. The five-minute case was over the limit, but testing showed it was still slightly sensitive to pH. However, the first three cases represent the main section of interest, as they got different thicknesses

of Si_3N_4, with different sensitivities to compare against each other. The following chapter will describe in detail the outcomes using a variety of pH values.

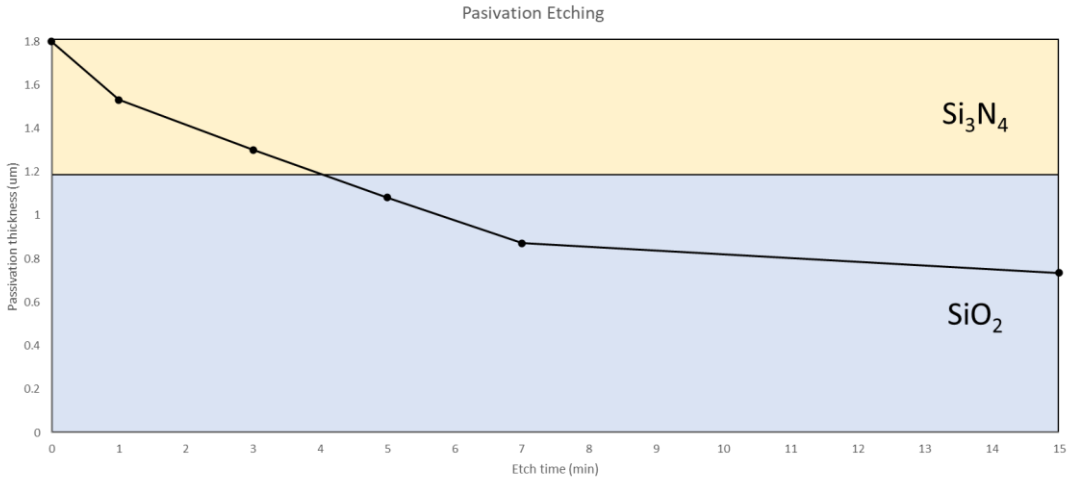


Figure 4.12 Etching times against passivation thickness of TSMC CMOS chips.

4.4 Packaging and Encapsulation

All CMOS chips were packaged onto a chip carrier to enable access to the bond pads for electrical and electrochemical characterisations and evaluate their performance. The pH buffers used for testing are aqueous solutions, so the electrical connections have to be well insulated while leaving the surface of the ISFETs sensing areas exposed to the wet environment. The following sections describe the main criteria for packaging and encapsulation. This analysis was performed using both generations of tape-outs in different stages of the research, providing insight for the final batch of packaged CMOS chips that were characterised with a solution.

4.4.1 Housing

To make the electrical connections accessible from the bond pads, CMOS chips were packaged in different ceramic packages, from Dual in Line-48 (DIL48) to J-Lead/Leadless Ceramic Chip Carriers-84 (JLCC84), providing enough connections for both cases (32 for chip CMOS-V1, NPFM-V1 and 35 for chip CMOS-V2, LPFM). The DIL48 consisted of a through-hole package that provided 48 gold leads, a cavity of 8x8 mm, and a pitch of 2.54 mm, while the JLCC84 worked as a surface-mounted

package containing 84 pins and a cavity of 7.62 × 7.62 mm for both the lead and leadless versions. The dies included multiple designs for different research purposes, so only half of each CMOS chip corresponded to the designs presented in this work. Chips were glued onto the centre of the chip carriers using a quick-cure standard adhesive ultra-strong epoxy, and a wire bonding process took place to make the interconnections between the IC and the corresponding packaging.

The following subsections describe this process:

A. In-house Wire Bonding

Due to the limited number of bond pads on the CMOS chip, the decision was made not to have ISFET readouts available for electrical characterisation. Therefore, the passivation of the ISFET's floating gate had to be opened to access these nodes for initial testing. An in-house wire bonding was performed using a Kuliche and Sofia Model 472 Gold Wire Ultrasonic Ball Bonder. The procedure connected the bond pads of the chip to the right and bottom sides of the package cavity. In contrast, the sensing areas, consisting of eight floating gates with a surface area of 125 × 125 µm, were linked using the left side, crossing the chip's surface, as shown in the right micrograph of Figure 4.13. Nonetheless, the process presented limitations due to the equipment capabilities and human error, making it complicated to achieve a perfect wire bonding of the entire design.

The CMOS chip shown below was used for initial characterisation, but the in-house wire bonding process was done individually, significantly limiting the workflow if more chips were needed for testing. The equipment also required a qualified professional for its use, so this approach was only considered when individual tests of specific sections of the CMOS chips were needed to be compared against simulated data. In this case, the need to access the sensing areas inside the chip for an electrical characterisation made it the best choice, as the university had the capabilities for both the passivation removal and chip bonding.

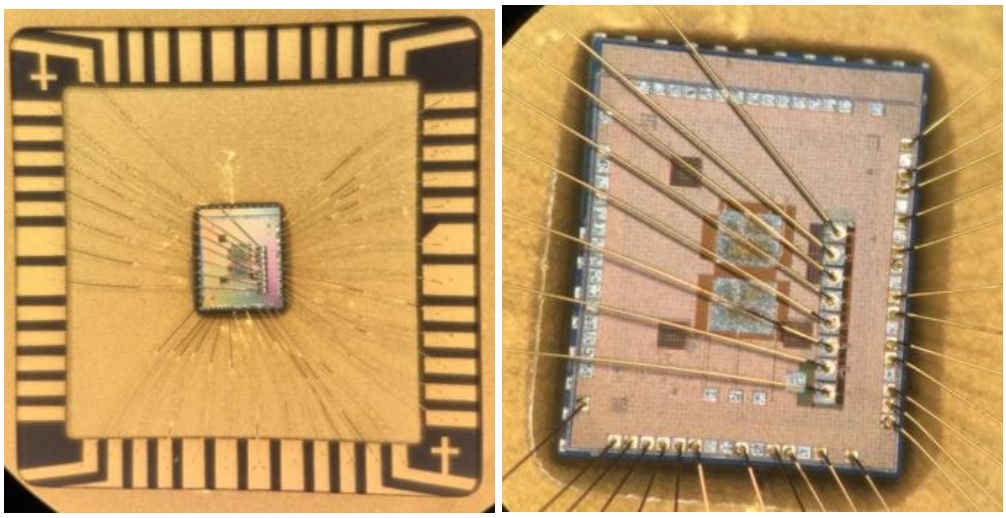


Figure 4.13 CMOS chips with in-house wire bonding. Left: full view of wire-bonded CMOS chip. Right: zoom view of the CMOS chip surface.

B. Commercial Wire Bonding

Due to the need for many dies for electrical and electrochemical characterisations, the wire bonding service was outsourced to Alter Technology. Dies were plasma cleaned before they were assembled into the chip carrier with a non-conductive epoxy, and a 25 µm Au ball bonding was used to connect the bond pads to the internal lids of the cavity. This service guarantees a standardised wire bonding, providing more efficient and faster manufacturing than in-house equipment. Figure 4.14 shows the commercial wire-bonded chips.

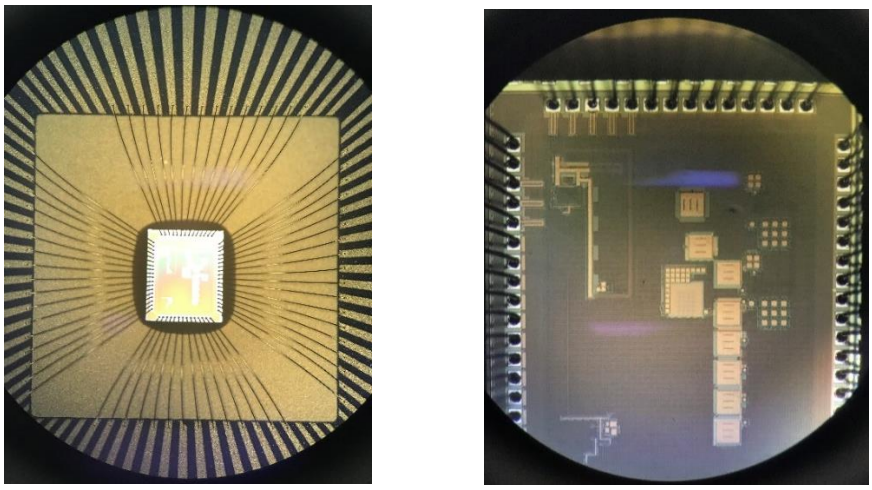


Figure 4.14 CMOS chips with automated wire bonding provided by Alter Technology.

4.4.2 Encapsulation

For electrochemical characterisation, the electronic architectures of the CMOS chips needed to be well insulated while leaving the electrodes exposed for experimentation in aqueous solutions of different pH values. This requires hermetic sealing or encapsulation of the rest of the chip. Three different methods were explored in this work to see the operation of the packaged CMOS chips under solution. The following subsections describe them in more detail.

A. Manual Encapsulation

Manual encasing with DELO KATIOBOND 4696 UV-curable epoxy is one of the easiest and quickest ways of encapsulating a device. Using a small spatula, one side of the wire-bonded CMOS chip was carefully covered until the section was full without reaching the centre of the device. Then the chip carrier was placed under UV light for five minutes. The process had to be repeated with the remaining sides of the CMOS chip, covering the whole area and leaving the centre exposed where the sensing area is located. Figure 4.15 shows the outcome of this process.

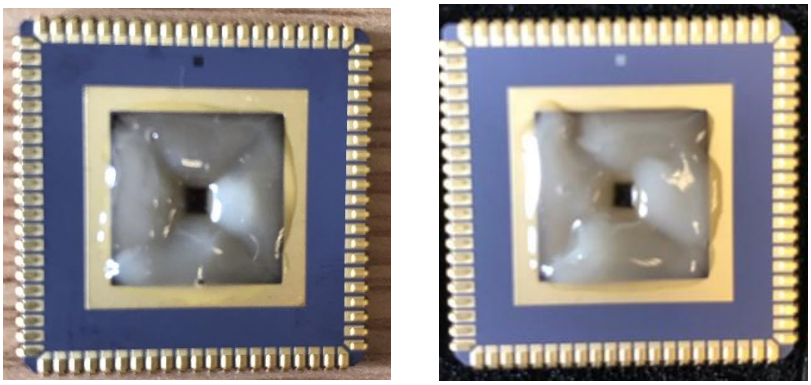


Figure 4.15 Manual encapsulation of CMOS chips. The right-side case partially covered the electrodes.

However, this approach had several disadvantages, especially with the design of chip CMOS-V1, NPFM-V1. The sensing area in NPFM-V1 was very close to one of the device's edges, making it challenging to cover the bond pads without touching the area of interest. This layout design was improved for CMOS-V2, NPFM-V2, leaving the sensing area closer to the centre of the design. One of the downsides of quick-curing epoxies is that they offer less

long-term stability and physical strength, and low chemical, thermal and water resistance [163] [164], factors that are relevant to the applications of interest in this work, as the sensors needed to remain under solution for 90 minutes during the characterisation, meaning that high chemical resistance is required.

B. Printed Mask Alignment Encapsulation

Due to the disadvantages presented by the previous method, a more precise encapsulation was required. Therefore, a mask was designed to cover the area where the sensing areas were located, and the design was printed in an acetate using a standard Altalink C8035 printer with a maximum printing resolution of 1200 x 2400 dots per inch (DPI). The printed mask was then taped to a glass substrate. The encapsulation process used an EPO-TEK OG116-31 biocompatible grade epoxy in anticipation of eventually transferring the technology to implantable devices. This epoxy offers a slower curing time along with the advantages of long-term stability, greater physical strength, high viscosity and high chemical resistance [165], which are ideal for more extended measurements over time. The uncured epoxy was dispensed slowly over the whole surface, and the chip carrier was placed in a wafer. Figure 4.16 shows a picture of the final version of the printed mask.

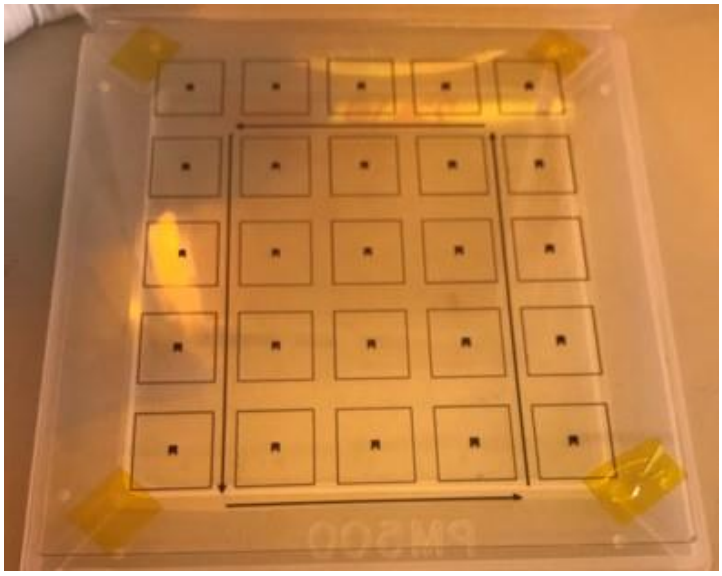


Figure 4.16 Printed mask taped to a glass substrate for CMOS chip encapsulation.

For the UV exposure of the epoxy, a conventional mask aligner was used (Karl Suss MA/BA8), which is a precision mask/wafer aligner used to transfer a pattern onto a wafer or substrate. The procedure requires the mask's alignment with the CMOS chip's surface on the chip carrier before exposure. The parameters for the exposure time were investigated and refined in [166] [167], and slight modifications were required to ensure proper curing over time. The average exposure time was 1,800 seconds in two cycles of 900 seconds (due to the parameter limitations of the mask aligner) and an exposure gap of 10 µm. It is important to highlight that the exposure gap was larger than 10 µm because the chips were immersed in the cavities of the multiple ceramic packages used in this work. After the UV exposure, CMOS chips were removed from the equipment to remove the remaining uncured epoxy. The process required a constant flow of acetone to the centre of the device for approximately 20 minutes, using an average of 500 ml of acetone, following DI water, before drying in N_2 for a final inspection. Figure 4.17 shows an initial trial using the printed mask in a glass substrate.

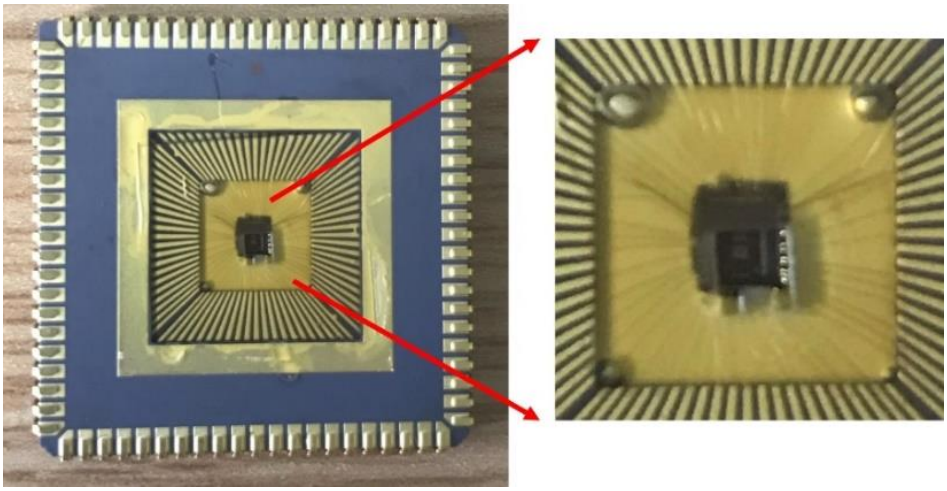


Figure 4.17 Printed mask alignment encapsulation, showing the misalignment of the exposure.

The main issues during the process can be divided into two aspects. First, the poor screen resolution of the chip’s surface during the alignment caused the mask to be misaligned on top of the CMOS chip surface. The levelling of the vertical alignment for when the gap between the mask and the package was reduced to 10 µm may also not have been appropriately set. The package was

placed at the top left of the wafer, leaving room for the mask aligner to tilt the levelling differently because it had only one reference to follow. It is important to note that two lids with 1 mm of thickness were taped to the sides of the desired mask to avoid contact with the epoxy on the surface of the package. The reference for the alignment was the CMOS chip, which was inside a deeper cavity of the package, so it was possible to make contact between the viscous epoxy and the mask if the gap was too small. Figure 4.18 illustrates the issue mentioned above. The top image shows the lack of a reference package, causing the mask aligner to tilt the levelling, while the bottom provided a good fix for the issue.

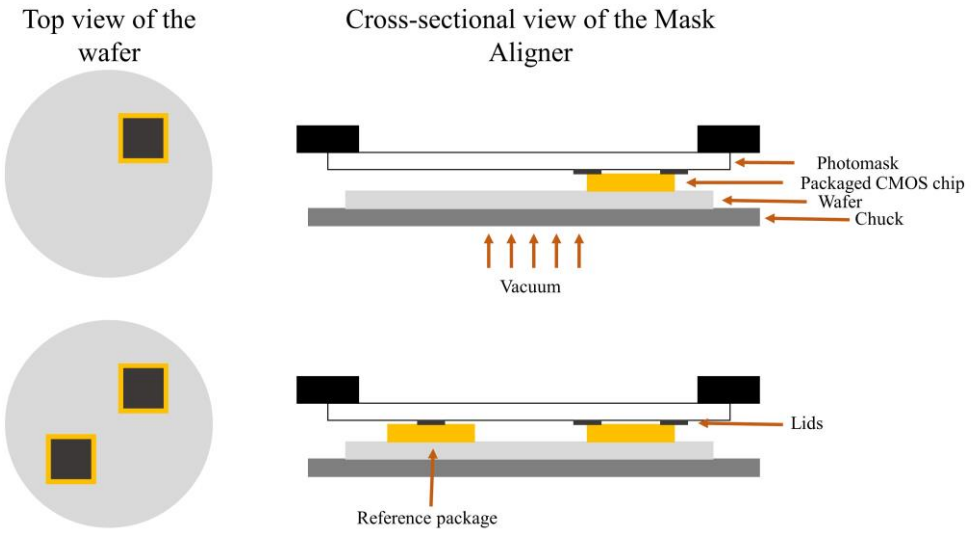


Figure 4.18 Illustration of the vertical alignment issue. Top view of the wafer and cross-sectional view of the loaded mask aligner. Top: wafer without reference package, making it tilt the levelling. Bottom: wafer with reference package, setting the height correctly.

C. High-quality Mask Alignment Encapsulation

The manufacturing of a high-quality chrome mask was outsourced to Compugraphics International Ltd, which provides high-quality photomask solutions for semiconductor and optoelectronics applications. The design of the manufactured chrome mask is shown in Figure 4.19, with a dimension of 5 × 5 × 0.090 inches. It contains four different designs in repeated patterns to facilitate the alignment with the CMOS chips in the mask aligner, magnifying the size of the patterns of interest for this work.

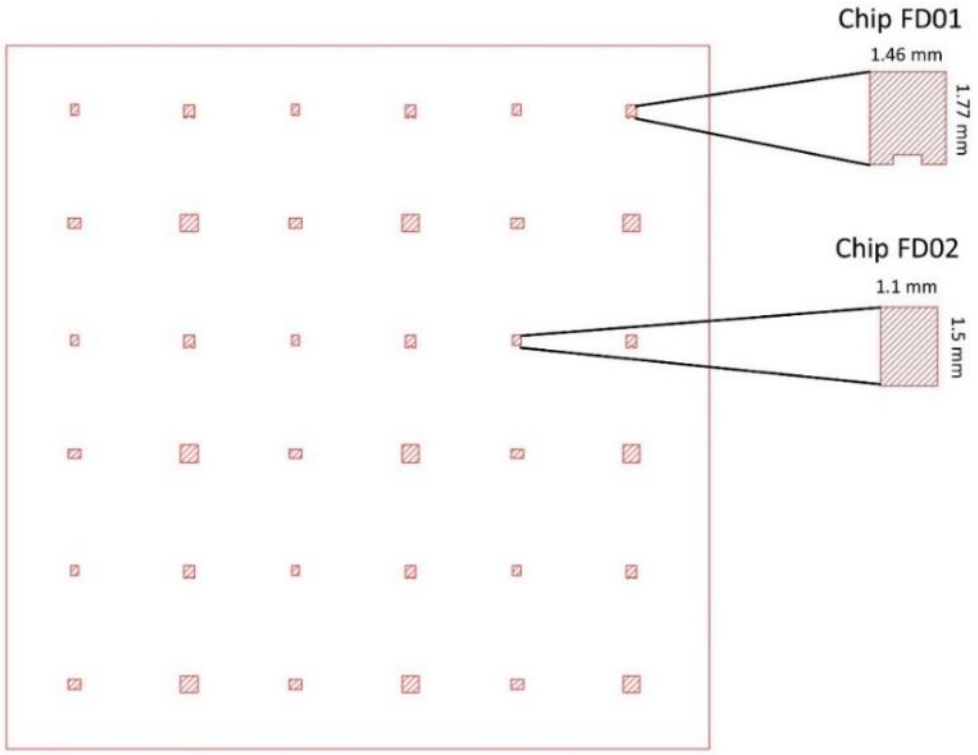


Figure 4.19 Mask layout for multiple layouts. Patterns of interest are highlighted in a larger size.

The process for the encapsulation followed the same method as above, with the difference in the high-quality mask and the addition of an empty package of the same size to the bottom left side of the wafer (shown in Figure 4.18), which ensured the correct levelling of the alignment in the mask aligner. An extra step was also included in the encapsulation process to increase the lifetime of the devices. First, packaged CMOS chips were placed on a hot plate from room temperature to 80 °C for two hours. Then the temperature was increased to 120 °C and CMOS chips were kept there for five more minutes. This first step makes the epoxy biocompatible, while the second improves the mechanical strength of the epoxy, allowing measurements over a more extended period. Figure 4.20 shows the successful encapsulation using this method in both types of JLCC84 package, leaving only the area of the electrodes ready to be in contact with the aqueous solutions.

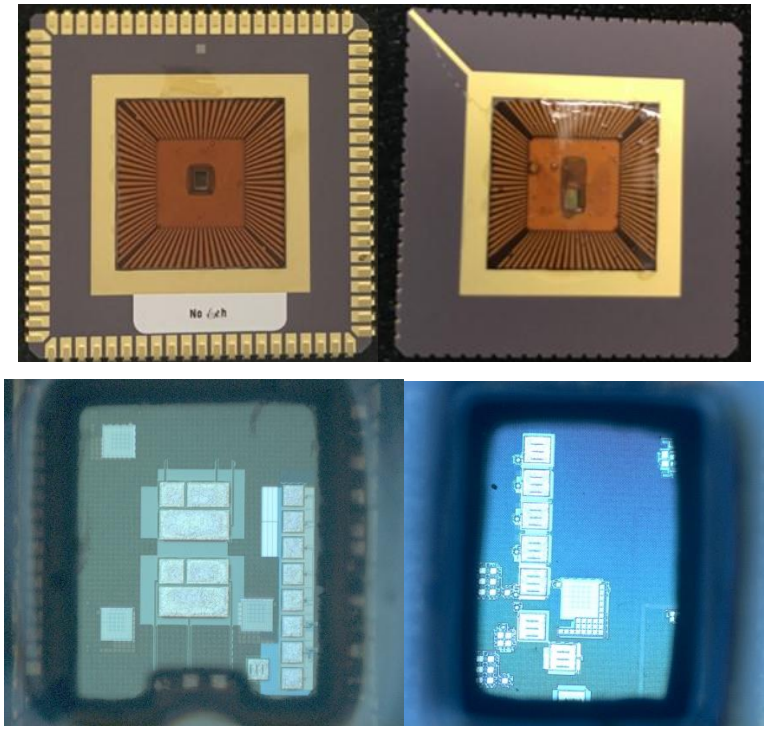


Figure 4.20 Top: high-quality mask alignment of CMOS chips in different JLCC packages. Bottom: higher magnification of actual sensor opening for each case.

Once the encapsulation method was defined, two batches of six post-processed CMOS chips were encapsulated. The chip carriers were labelled to identify the etching time of each die, and the CMOS chips were observed under a microscope to evaluate if any remaining epoxy was left inside the cavity of each chip. The results are shown in Figure 4.21.

Figure 4.21 Batch of encapsulated post-processed CMOS chips.

4.5 Summary

In this chapter, three different ISFET post-processing methods were described. According to the literature, these scenarios were chosen based on their advantages over other sensing layers and post-processing methods. These are direct sensing with unmodified chips, deposition of a Ta_2O_5 sensing layer and the thinning of the original Si_3N_4. Several methods were also explored to package the CMOS chips for use under pH solutions. This includes the whole process, from the wire bonding to the final encapsulation. Different techniques were evaluated for a suitable encapsulated package for the following testing. After the post-processing and packaging of the CMOS chips, the next step is to perform an electrochemical characterisation of these chips to analyse their response to pH changes and compare them to the expected outcome in both simulations and electrical characterisation.

Chapter 5

CMOS Chip Sensor: Electrochemical Characterisation

5.1 Introduction

The previous chapter focused on post-processing methods for improving the pH sensitivity of ISFET sensors. This chapter describes a series of experiments carried out on the manufactured CMOS chips to evaluate their performance in relation to the output response against pH using different measurement techniques and post-processed cases. The ISFET sensors (with different front-end architectures and some post-processing for sensitivity improvement) were tested to demonstrate pH sensitivity over a long time. These electrochemical characterisations are the most important results for evaluating ISFET sensors.

5.2 Experimental Setup Specifications

Once the CMOS chip was packaged, a plastic chamber was placed on the surface and attached using a UV light epoxy for five minutes. This cylindrical cavity was used to deposit the pH buffers to be in direct contact with the sensing layer of the CMOS chip. The sensing layer, either the unmodified passivation layer or the one composed of Ta_2O_5, is located between the solution and the top metal-6 of the extended gate electrode. Figure 5.1 shows the addition of the chamber to a batch of CMOS chips ready to be tested. An off-chip readout system was developed for the data acquisition, allowing the user to test the response in real time.

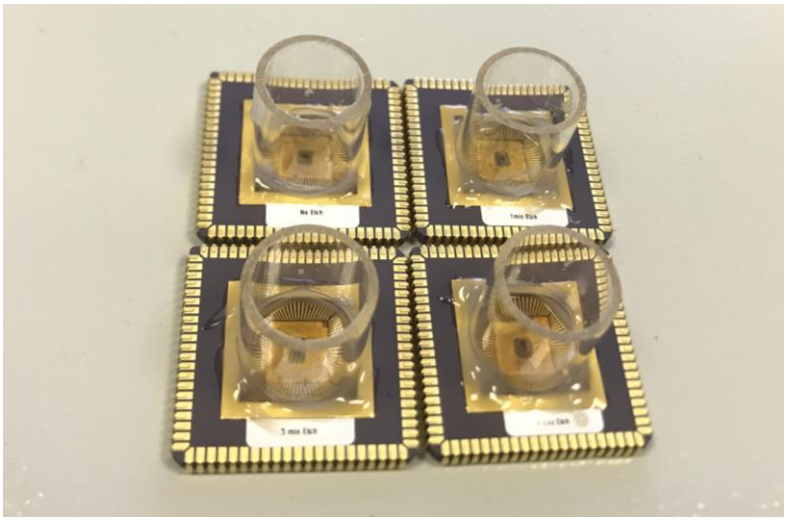


Figure 5.1 Final stage of CMOS chips for electrochemical characterisation.

Testing the CMOS chips required a custom-built system that allows an easy and compact way to provide the power and extract the necessary data from the corresponding outputs. This system consists of a custom PCB design to provide the input voltages internally using a single power source. This was done by calibrating the required values with linear potentiometers, digital switches for on/off control variables, and other active components for signal conditioning. Figure 5.2 shows a 3D representation of the final PCB design using JLCC packages for the CMOS chips. More details of the schematic and layout views can be found in Appendix E.

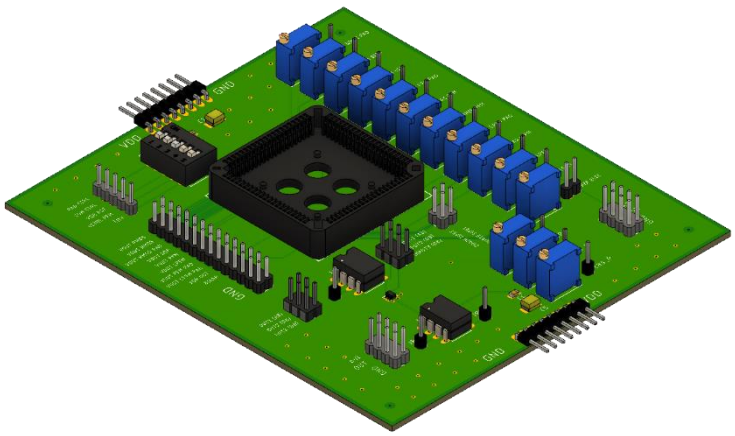


Figure 5.2 3D representation of custom PCB design.

The complete setup included an Aim-TTI EX345RD Dual Power Supply, an Agilent 33220A Function Generator to provide the reference electrode voltage, and a Picoscope 6404D with interface software directly connected to a workstation. Figure *5.3* shows the schematic diagram of the complete setup. The custom PCB with the packaged CMOS sensor was placed inside a Faraday cage to block external electromagnetic interference (EMI). This was necessary to carefully characterise the chip without being affected by the long cables required for the measurement setup. However, implantable medical devices, including neurostimulators, pacemakers, and implantable drug infusion pumps, among others, are known to be vulnerable to EMI, which can lead to a range of outcomes from discomfort to fatality. Since these devices must be both well-protected from EMI and able to send/receive signals, implementing EMI filters that can effectively differentiate between desired signals and unwanted noise is crucial. The use of feedthrough filters is a well-known solution as they have low equivalent series resistance (ESR) and can be hermetically sealed and designed for low or high voltage [168] [169]. However, these filters were not considered for this work as the design was first tested as proof of principle.

The pH buffers, commonly used in biological research, were created shortly before use as they do not store well over time. When the electrolyte is exposed to air, this mixture of gases contains 0.04% of CO_2, which is absorbed by the buffer, dropping the pH of the solution. The decision was made to prepare the buffers in-house, as commercial buffers contain other unknowns in their preparation that might affect the measurements, likes dies to artificially change their colour and preservatives to make them last over time. The buffers were prepared by adding 800 mL of distilled water in a suitable container, 7.45 g of potassium chloride (KCl) at a concentration of 100 mM, and 0.772 g of hydrochloric acid (HCl) at a concentration of 20 mM. Then, the solution was adjusted to the desired pH by using either HCl or sodium hydroxide (NaOH). Finally, distilled water was added until the volume was 1 L. A standard pH meter from SciQuip was used to verify pH variations before and after each measurement to avoid wrong readings and change the solution when needed.

The buffers were placed using a micropipette to avoid the formation of a surface bubble covering the whole microcavity with trapped air inside. The chips were tested

under different configurations, explained in the following sections. After each test, the solution from the chamber was removed, and the sensors were cleaned with DI water to dilute and remove the remaining buffer, then dried with N_2 before a different solution was applied for the next test. A waiting time of five minutes was suggested before introducing a new pH solution to ensure any remaining solution could dry/evaporate at room temperature. The pH buffers were used alternately (pH 7 – pH 4 – pH 10 – pH 2 – pH 12)

The NPFM and LPFM designs required a bias voltage and different thresholds voltages to control each architecture's charging and discharging phase. The circuit designs included an extra capacitor connected to the gate that could be momentarily used to calibrate the threshold voltage, making it valid for a brief time. The NPFM also had an external switch to control whether the threshold voltage came from an internal or external source. These different input voltages were controlled through the personalised PCB design.

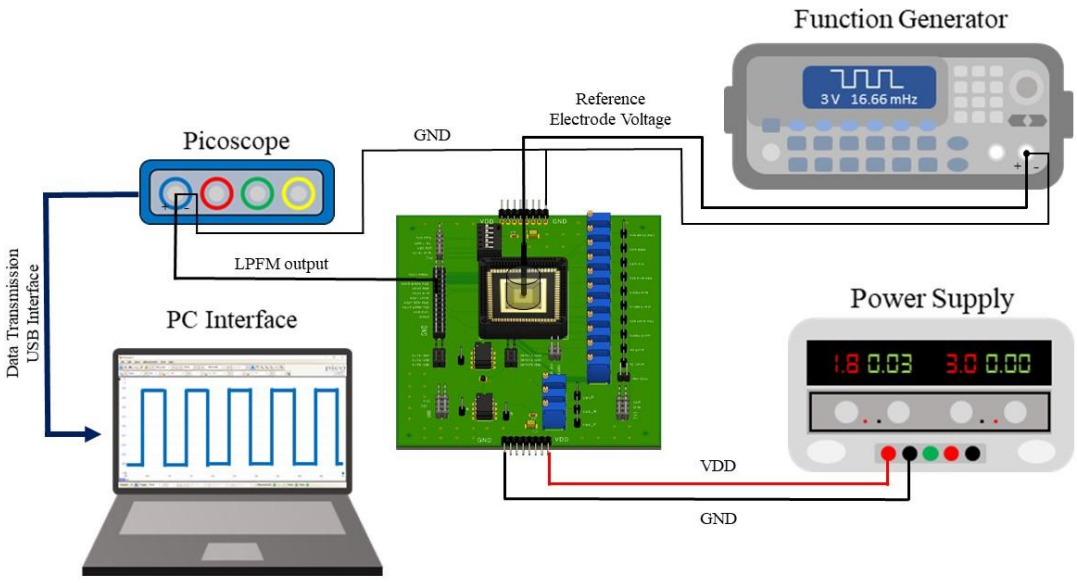


Figure 5.3 Schematic diagram of the setup used to test the CMOS chips under solution.

The Picoscope is a USB-controlled device with four independent channels, 250 to 500 MHz bandwidth, real-time 5GS/s sampling and 2 G sample buffer memory. It also includes a built-in DC to 20 MHz function generator, spectrum analyser, serial data

decoding and high-speed data acquisition with its software package. This device's principal feature of interest is the deep measurement option, which allows for the analysis and recording of full waveform data, including the cycle time, frequency, low and high pulse widths and duty cycle. This Picoscope-based technique was necessary due to the unusual nature of the digital output (sudden high-frequency bursts with long gaps in between). In the future, a system could be designed for automated frequency measurement that does not require manual intervention.

Figure 5.4 shows an example of the deep measurement tool characteristics. This feature accurately detected the frequency response at a fixed input voltage, confirming a 50% duty cycle with minimum undershoot and overshoot.

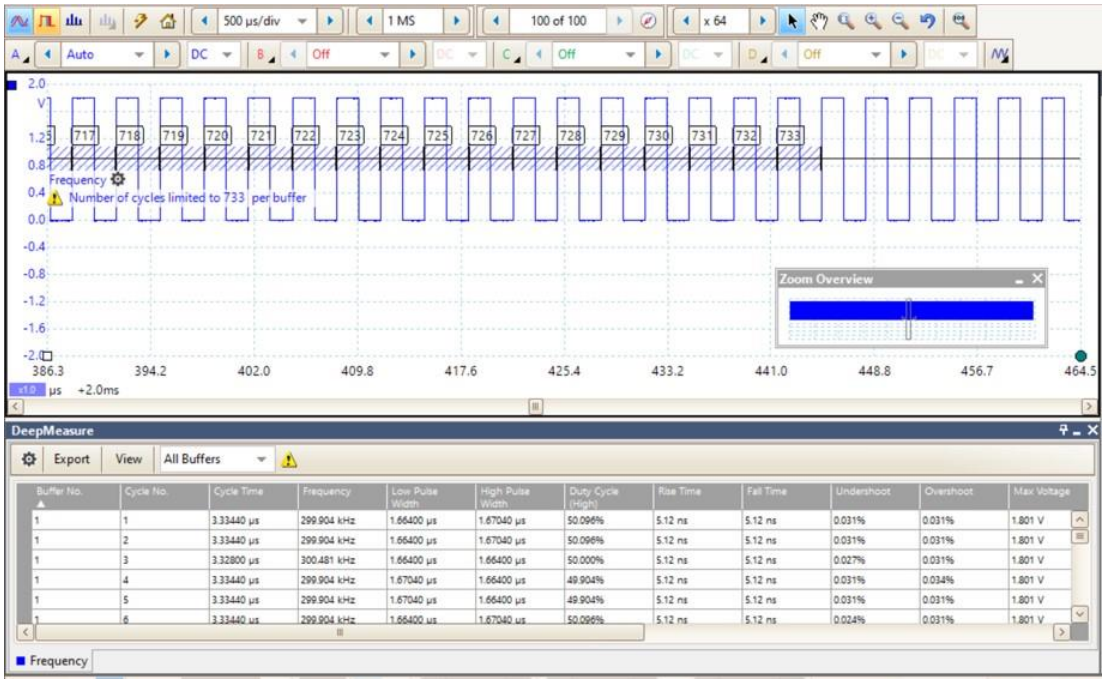


Figure 5.4 Picoscope deep measurement feature in LFPM architecture.

5.3 Electrochemical Characterisation

5.3.1 Static Electrochemical Measurements

In the published literature, the measurement results of ISFET sensors are typically presented without too many details on the initial electrical setup, leaving room for interpretation. However, during the testing phase, it was noticed that the start-up

conditions and the measurement duration could significantly impact the results. The most common way to measure such a sensor is to power-ON all the necessary external voltages at the beginning, as shown in Figure 5.5. In this case, VDD, V_{bias} and V_{ref} are the external signals, while V_{ISFET}, V_{cap} and V_{out} are generated internally. The external signals are generally kept constant during measurement and even when the pH buffer changes. This is defined as the Static Measurement Method. The plots below represent the ideal and current results from an LPFM architecture that can be obtained from such a measurement. V_{ISFET} describes the behaviour of the voltage that reaches the gate of the ISFET, which is different from the voltage provided through the reference electrode. It shows how the gate voltage decays over time, significantly impacting the frequency response using this method. This is an illustration of the behaviour seen during the testing phase.

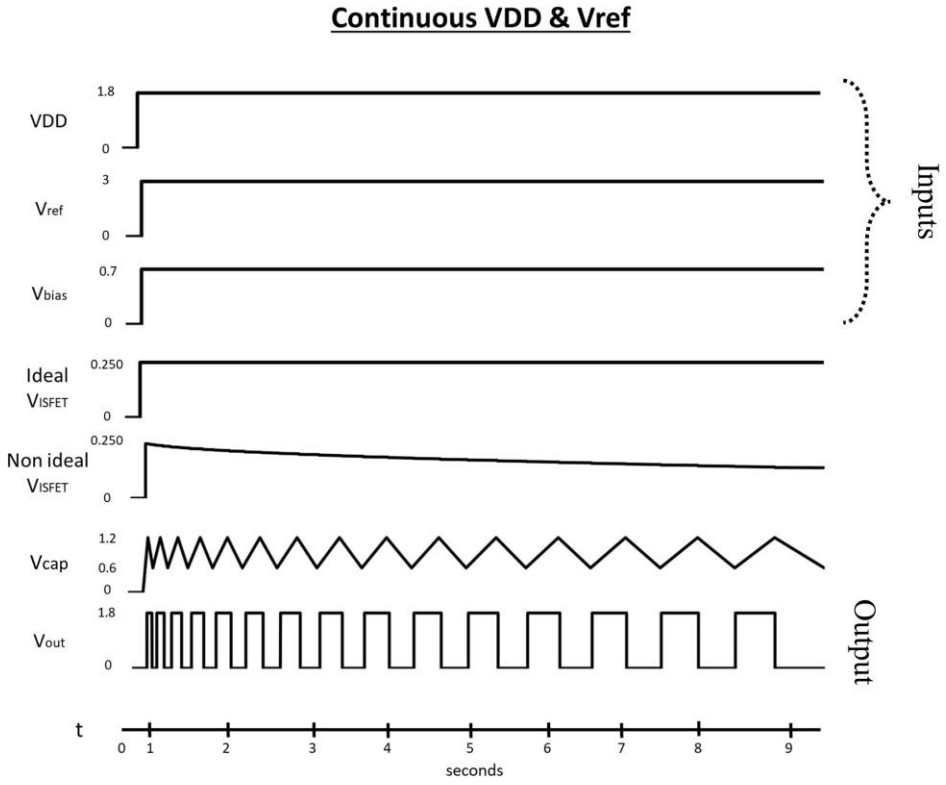


Figure 5.5 Time diagram of static electrochemical measurement.

However, it can be seen from long-term simulation results that a static measurement is not ideal for a capacitive sensor like an ISFET. Since there is no resistive path between the liquid interface and the gate of the transistor, the time constant of the

circuit depends entirely on the unknown capacitances of the interface and sensing layers. The internal node between the sensing capacitor and the MOSFET gate capacitance is also a floating node with no predetermined voltage. This can be easily shown with a simpler simulation using an NMOS source-follower-based (NMOS SF) ISFET sensor, as shown in Figure 5.6. The results show a consistent decay/drift in the output voltage, even in the most simplified ISFET model.

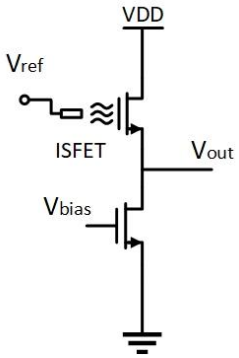


Figure 5.6 NMOS source-follower architecture.

Since the exact capacitance to be used in the ISFET simulation was unknown, the simulation was repeated with multiple passivation capacitances in a parametric analysis, as shown in Figure 5.7. It is believed that this decaying behaviour of V_{out} is not the typical trapped charge-related drift reported in ISFET literature. Instead, it is most likely due to the inherent RC constant of the ISFET structure and connecting circuit [170].

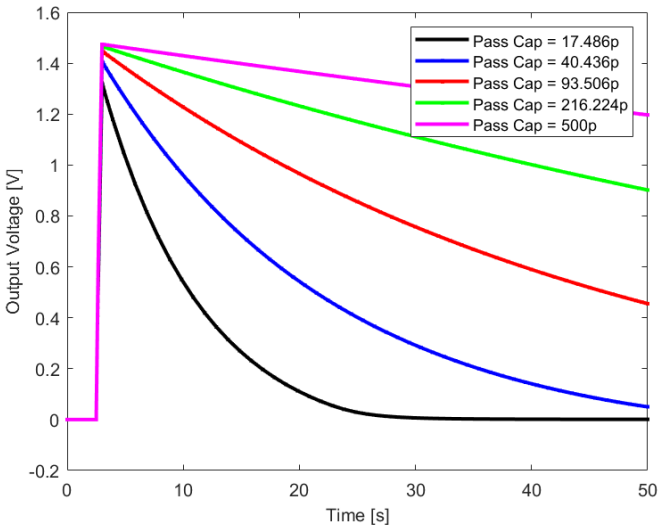


Figure 5.7 Simulation of NMOS SF output response at different passivation capacitances.

The output voltage of the NMOS SF was plotted for different V_{ref} voltages, as shown in Figure 5.8. The curve shows the result for a 'Static Measurement'. Unlike standard simulation methods done for a short time, we intentionally kept the simulation running for much longer. While the results immediately after the start of the simulation match the expectation, a rapid decay in the output (down to zero) was noted over a much longer timeframe. Although the ISFET models are approximate and the simulation does not include the complex liquid interface layers, the overall trend in V_{out} is still important. In Figure 5.8, VDD and V_{ref} are turned on at 2.5 seconds, showing a response to V_{out} in the y-axis, but slowly decaying over time over a period of approximately 20 seconds.

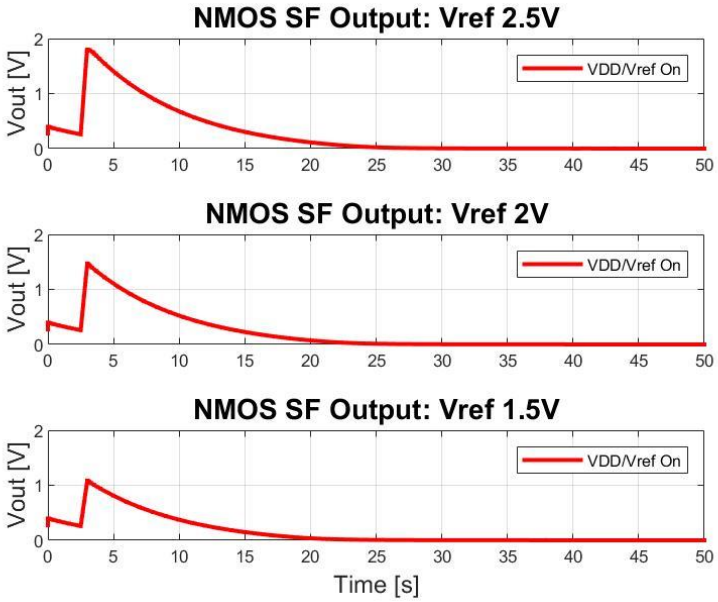


Figure 5.8 Simulation of NMOS SF output response under different V_{refs} using static measurement.

a) Ta_2O_5 Layer CMOS-V1: NPFM-V1

A first batch of CMOS chips underwent the removal of the passivation layer to later deposit Ta_2O_5 on the sensing area and evaluate its performance in terms of the sensitivity and drift of the signal in long-term measurements. This electrochemical characterisation differs from the rest because of the following details: commercial pH buffers were used; no Faraday cage was used; the CMOS chip was fabricated in a different TSMC process; a similar PCB was used for its testing, but it was personalised for this initial design; and no electrical characterisation was performed first, as the

limitations of the pads didn't allow the addition of an extra architecture for this purpose. Figure 5.9 shows the setup at the start of the electrochemical testing.

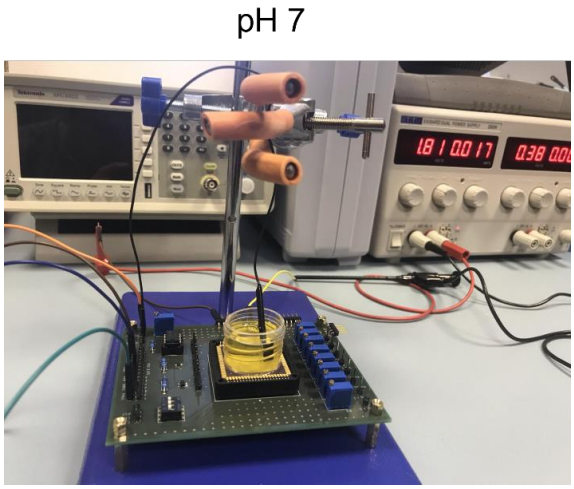


Figure 5.9 Initial setup for first electrochemical characterisation.

The NPFM architecture was tested using the Static Method, shown in Figure 5.5, as an initial reference to evaluate whether the output response matched the simulated data. The PCB required just one power supply of 1.8 V, V_{thres} was set to be 900 mV (half the VDD), V_{bias} was equal to 700 mV, V_{cg} was grounded, and V_{ctrl} and V_{rst} were ON to provide an external threshold voltage and allow the internal bandgap reference to set a fixed current source for the comparator. A V_{ref} of 3 V was supplied to the reference electrode. The initial electrochemical results are shown in Figure 5.10.

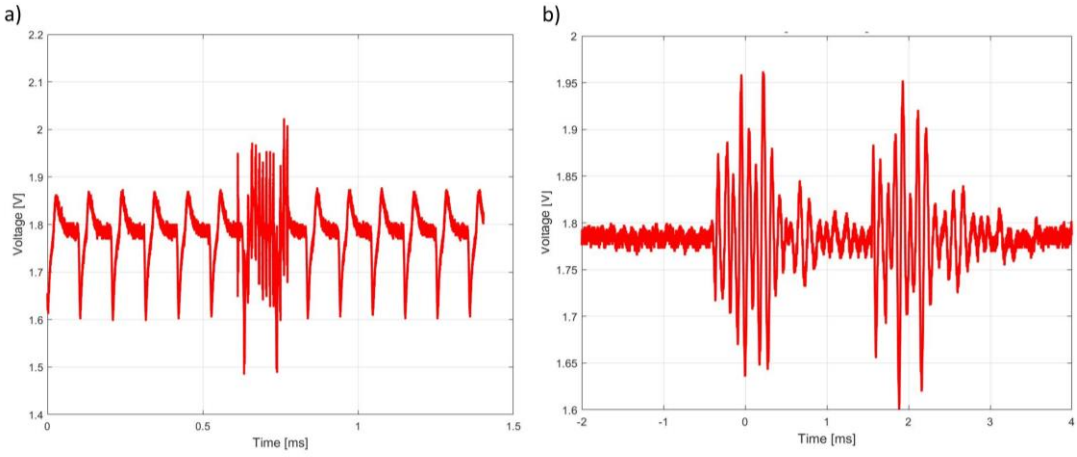


Figure 5.10 NPFM electrochemical characterisation with Ta_2O_5 sensing layer. a) Zoomed-in view with noise interference in the signal; and b) intermittent noise in the signal.

Figure 5.10 a) shows a zoomed-in view of the original signal taken in a lapse of 1.5 ms, giving the first insight into this design's deficiencies. The signal was partially following the expected behaviour, as the design should provide a train of pulses at the output, which frequency changes depending on the voltage at the gate of the ISFET. However, the signal remained stuck between 1.6 V and 1.8 V, meaning the capacitor did not have enough time to fully charge back to VDD before the PMOS switch was turned OFF. The graph also shows sporadic spikes not corresponding to the output signal. Finally, Figure 5.10 b) shows the intermittent noise signal of an undetermined frequency that sometimes overlaps with the output, a sign of electromagnetic interference around the setup.

This electrochemical measurement was the first proof that the chips survived the post-processing technique. The electrical characterisation of this NPFM structure was described in Chapter 3. However, the benefits of the Ta_2O_5 layer could not be demonstrated due to the design flaw of the NPFM-1 architecture described in section 3.4.4. Therefore, this design was not pursued later, and the LPFM overtook the electrochemical characterisation in the following sections.

Furthermore, due to the restrictions put in place during the pandemic period, no further post-processing was done related to the Ta_2O_5 layer in the subsequent designs, as it required the use of cleanroom facilities at different locations.

b) CMOS-V2: NPFM-V2

Due to the promising results obtained from the electrical characterisation of the LFPM architecture and the complex calibration the NPFM required to work, no further electrochemical testing was done on NPFM-V2. This optimised version showed better results in terms of the complete swing from VDD to 0 V every time the capacitor charged up, but the design itself needed to work in a very specific region, making it difficult to manage, even for electrical testing only. Ultimately, the decision was taken to pursue further results with just the LFPM.

c) Unmodified CMOS-V2: LPFM

Before characterising the LPFM circuit, the CMOS-V2 chip was first electrochemically tested for the in-built NMOS source follower (mentioned in

Section 5.3.1). This was done using the same timing diagram as in Figure 5.5. It should be noted that the higher the V_{ref}, the higher the instantaneous initial V_{out}, which means that the reference voltage directly impacts the output voltage, as expected. However, V_{out} tends to zero in as little as approximately 20 seconds, meaning the passivation capacitance might differ between AMS and TSMC technologies. The same behaviour was replicated in simulation by varying the passivation capacitance value. This test was done at pH 7 and repeated with other pH values, but the results showed a similar decay response.

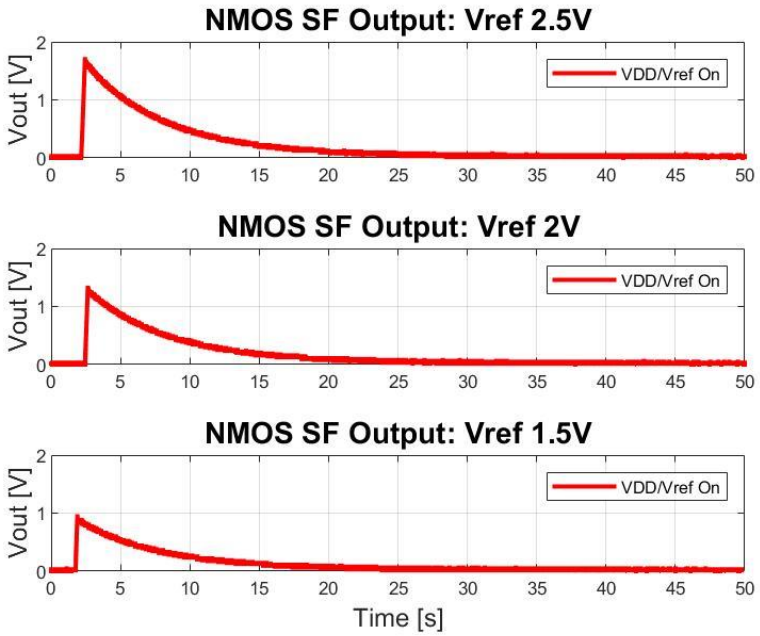


Figure 5.11 Electrochemical characterisation of NMOS SF under different V_{refs} using static measurement.

The equivalent passivation capacitance, made of two dielectric layers, is defined as:

$$C_{pass} = \frac{\epsilon_{Si3N4} * \epsilon_{SiO2}}{\epsilon_{Si3N4} * t_{SiO2} + \epsilon_{SiO2} * t_{Si3N4}} * \epsilon_{0*A_{pass}} \quad (19)$$

The relative permittivity of Si_3N_4 and SiO_2 may vary depending on the specifications of the CMOS technology. For AMS technology, these values correspond to 7.9 and 3.9 respectively [45].

Due to the limited information provided by TSMC, assumptions were made using the AMS technology data to calculate the possible passivation capacitance present in the

design. The information considered for the calculations is included in Table 5-1, using the parameters for AMS technology for the relative permittivities of Si_3N_4 and SiO_2.

ε_{Si3N4}	7.9
ε_{SiO2}	3.9
$\varepsilon_0 (F \times m^{-1})$	$8.85 * 10^{-12}$
SiO_2 *Thickness (µm)*	1.15
Si_3N_4 *Thickness (µm)*	0.6
A_{pass} *(µm)*	125 x 125

Table 5-1 AMS/TSMC technology parameters for C_{pass} calculation.

According to the literature, the resulting passivation capacitance was equal to 0.461 pF, consistent with the range of values where the output decays quicker than expected [170]. A similar electrochemical test was performed on the LPFM architecture using a variety of V_{ref}, from 2.5 V to 12 V, as shown in Figure 5.12, to show the multiple instantaneous output frequencies the design can achieve depending on the initial calibration through V_{ref}. The encapsulation offered good protection against chemical solutions and allowed high voltages to the reference electrode for periods over one minute. However, V_{ref} needed to be contained to a maximum voltage of 6 V to ensure the device maintained the correct functionality for long periods, as a higher leakage current will be present, possibly because of the creation of parasitic current paths between the reference and the bond pads inside the CMOS chip that have been exposed due to damage in the encapsulation, making the architecture fail relatively fast. Therefore, the test shown below was only designed to illustrate the behaviour of the LPFM design over periods under a minute.

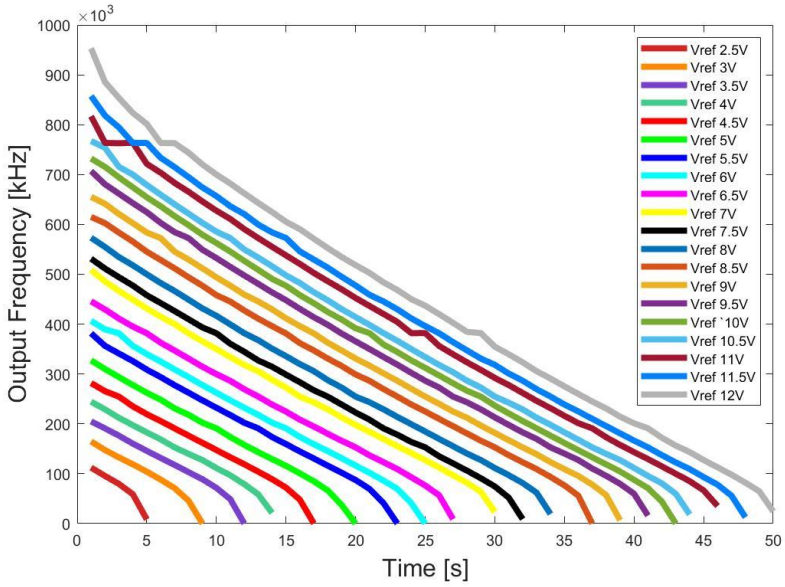


Figure 5.12 Frequency response of LPFM at different reference electrode voltages over time.

The difference between Figure 5.11 and Figure 5.12 decays relies on several factors. First, the instrumentation seems to respond different to the reference electrode voltage. While the NMOS SF requires a relatively low V_{ref} (2.5 V) to reach the maximum output voltage (1.8 V), the LPFM barely reaches approximately 250 mV at the input with the same V_{ref}, so the architectures are working on different regions. The first time the LPFM architecture shows an exponential decay occurs when V_{ref} is equal to 12 V, which represents approximately 1.2 V at the gate input. Another factor is the incorporation of a diode to one end of the programmable gate capacitor, which is directly connected to the floating gate. This diode in reverse biased mode may carry away some charge from the gate as a constant leakage current, becoming the dominant linear part of the decay where the exponential behaviour should start to become less significant.

A third cause might be related to the unique properties of TSMC technology. The effect of the passivation capacitance on how quickly the signal decays were shown through a simulation in Fig. 5.7, but the LPFM instrumentation differs on the addition of a key component like a bank of capacitors for the charging and discharging phase of the system. In TSMC technology for General Purpose, the layers of the capacitors are located between metals 5 and 6, which is the top metal of the process. Ideally, only the extended sensing electrodes should be placed on the most external layer to ensure

that all the ionic interaction occurs in the areas of interest, as it occurs in AMS technology where the capacitors are buried in the middle metals of the process. The impact of this might be a partial factor on how the architectures respond different to the same reference voltages.

Finally, the last part where the LPFM signal suddenly drops is related to the way the instrumentation works. Below 100 mV, the architecture stops working properly, giving this rapid drop to zero that is shown in every graph of Fig. 5.12.

5.3.2 Dynamic Electrochemical Measurements

Given the problem of the Static Measurement protocol, a Dynamic Measurement Method for further electrochemical analysis was developed. The measurement method is detailed in the figure below.

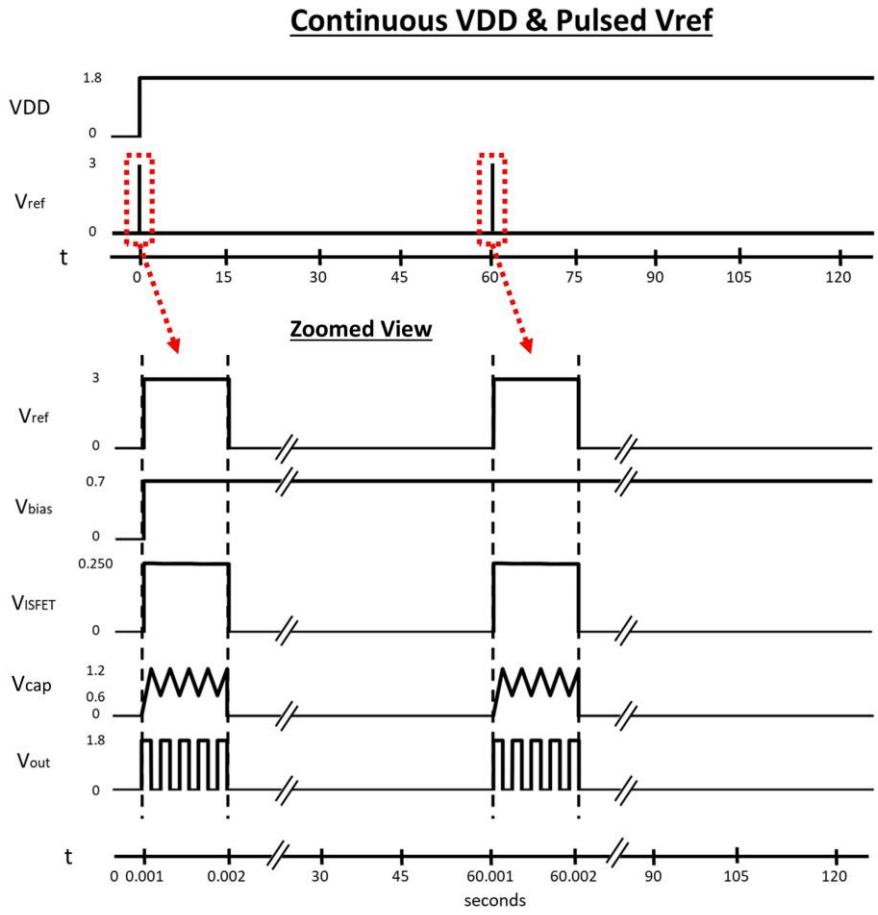


Figure 5.13 Time diagram of dynamic electrochemical measurement: continuous VDD and pulsed V_{ref}.

Within the Dynamic Measurement Method, the VDD and V_{bias} were continuously ON, while the V_{ref} was pulsed (Figure 5.13). The V_{ref} signal was set to its nominal value of 3 V for a short period and then discharged to the ground for a long time. The duty cycle of V_{ref} was kept small since the main interest was the immediate result after it was ON. Keeping V_{ref} ON for an extended period would trigger the undesired decay that was meant to be avoided. This protocol allows the architecture to discharge V_{ref} completely to zero before starting another pulse. The duty cycle was 0.001% or 1 ms every second for short periods and 0.0001667% or 1 ms every minute for long periods. For the LPFM architecture, the short-time V_{ref} generated a series of pulses at a roughly constant frequency, and the instantaneous frequency was taken immediately after V_{ref} was turned ON (Figure 5.14). The instantaneous frequency corresponded to an average frequency of the first 100 µs of the 1 ms pulse every respective period of V_{ref}, either one second or one minute, depending on the case.

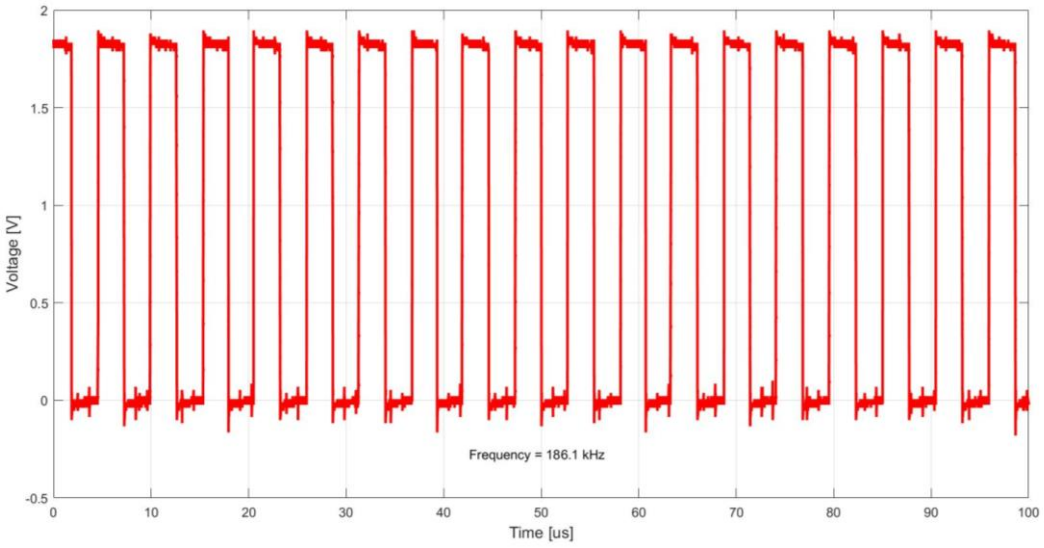


Figure 5.14 Instantaneous frequency of LPFM architecture detected by Picoscope software.

To avoid the collection of vast amounts of data at a maximum average speed of 100 megabits per second (MB/s) up to 1 gigabyte (GB), and to extend the lifecycle of the devices, V_{ref} was set to be ON for 1 ms every minute, and 60 to 90 data points were obtained depending on how long the system was tested under solution for different pH values. These plots were captured using the Picoscope, and the frequency of the short burst of pulses was obtained using the deep measurement feature included in its software.

A further technique was used within the same protocol to discharge all the built-up charges within the electrochemical setup. Here, the VDD and V_{bias} were also pulsed (Figure 5.15). However, this did not change the result further or have any detrimental effect. This protocol could significantly reduce the power consumption of an ISFET sensor, as the circuit is only operating for a very short duty cycle, and the entire interface circuit can be turned OFF for this duration. This will be particularly suitable for implantable applications and environmental sensors with intermittent power supply. Once the dynamic measurement protocol was established, the LPFM architectures was used, along with the various post-processed ISFET devices, for the final testing results using a variety of pH solutions.

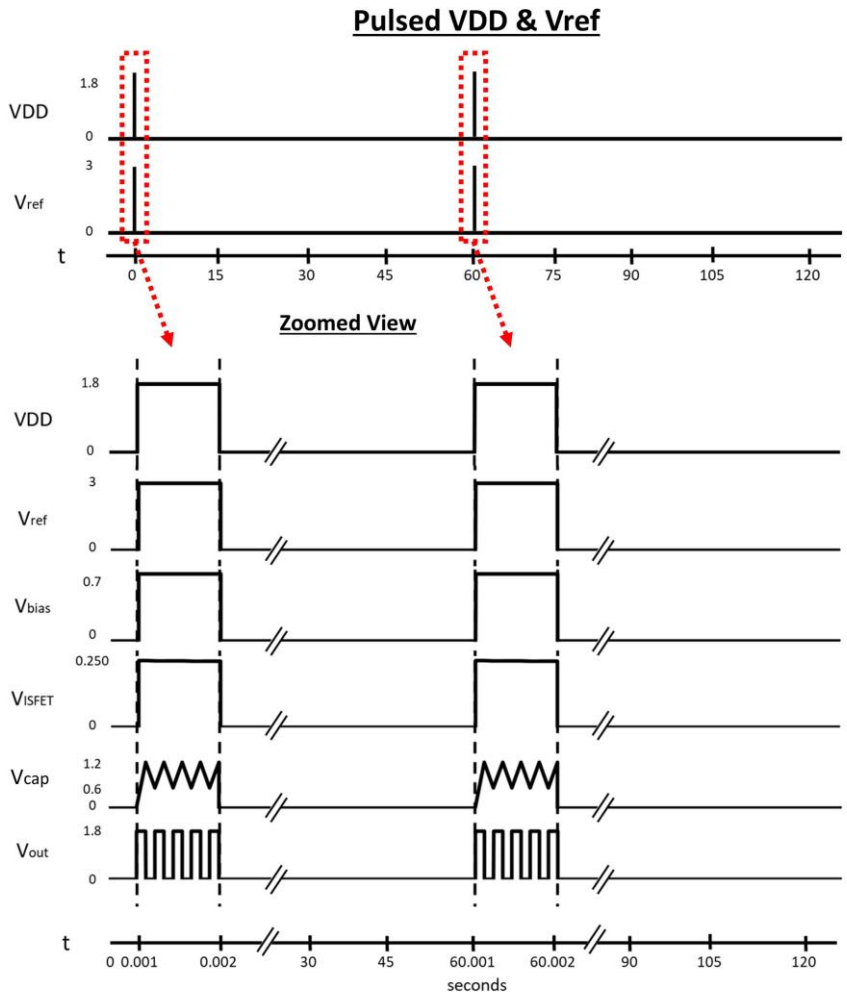


Figure 5.15 Time diagram of dynamic electrochemical measurement: pulsed VDD and pulsed V_{ref}.

The NMOS SF was used again to simulate the behaviour of the readout architecture using the Dynamic Measurement Method. The concept states that the electrical setup should be reset at a regular frequency and the measurement restarted. This method can discharge all the capacitors involved in the signal path. First, the VDD signal was pulsed between 0 V and 1.8 V while V_{ref} was ON. This result, shown in blue (Figure 5.16), did not change the basic nature of the decay. However, when VDD is zero, the output is also zero. Next, only the V_{ref} signal was pulsed between zero and a fixed value. This method would discharge the capacitors and bring their voltage to the ground. The results (green curve) show that the pulsed V_{ref} could eliminate the long-time-constant effects in the measurement setup. The output immediately jumps to the expected voltage when V_{ref} returns to the required value (e.g., 2 V, 2.5 V). Despite an initial decay effect, V_{out} quickly settles into similar behaviour every time V_{ref} is defined in each cycle. Finally, pulsing V_{ref} and VDD together (purple curve) did not change the behaviour very much.

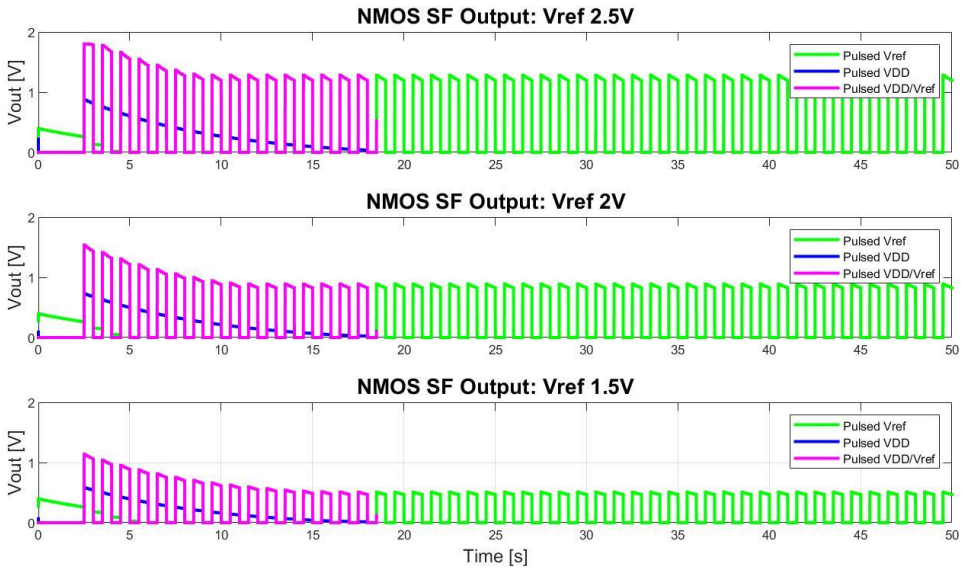


Figure 5.16 Simulation of NMOS SF output response under different V_{refs} using dynamic measurements.

a) Unmodified CMOS-V2: LFPM

The Dynamic Method was first verified by performing the same electrochemical measurement on the NMOS SF architecture, following the timing diagram in Figure 5.13. VDD was kept constant while V_{ref} was pulsed over time. Once again, the higher

the V_{ref}, the higher the instantaneous initial V_{out}, highlighting the impact of V_{ref} over V_{out}, as shown in Figure 5.17. However, this time V_{out} settles to a stable instantaneous value every time V_{ref} is restarted (green curve). The blue curve shows the device's behaviour only when VDD is pulsed, the results of which showed a reduced response, unsuitable for any application. This test was done at pH 7 and repeated with other pH values, and the results showed a similar pulsed response.

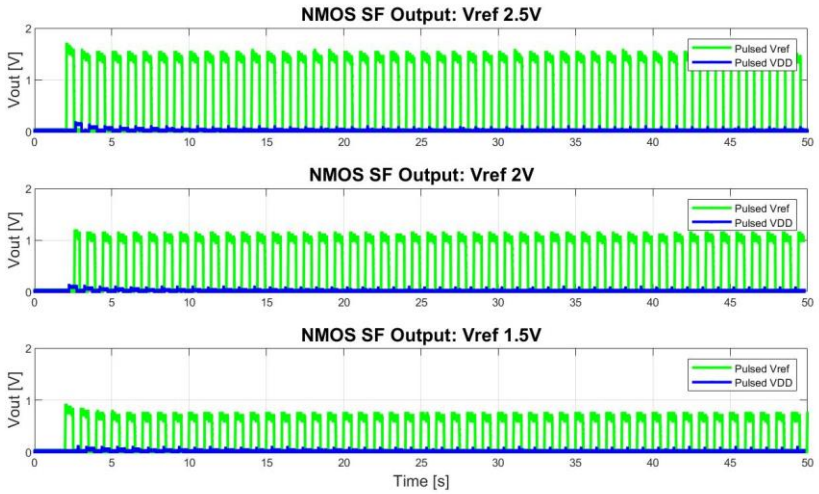


Figure 5.17 Electrochemical characterisation of NMOS SF under different V_{refs} using dynamic measurements.

Finally, the LPFM circuit was electrochemically characterised using the Dynamic Method. This was done for multiple ISFET devices, all fabricated in the CMOS-V2 run. The first ISFET devices did not undergo further post-processing on the sensing layer. Instead, the total thickness of the Si_3N_4 (0.6 µm) was used as the sensing layer. The chip was bonded, encapsulated and attached to a cylindrical plastic chamber. Three pH buffers (4, 7 and 10) were first used to check whether there was reasonable variation between the output frequency that was also consistent over time, as shown in the left graph of Figure 5.18. The frequency output of each measurement cycle was obtained after a 60-minute-long period, and the last 15 minutes are shown, where the signal presented a stability period. The interval between each frequency data point was one minute as a long-term measurement was intended, and a large number of data points were not required to see the expected consistent trend.

Two more pH buffers (2 and 12) were then introduced to the experiment. The whole process was repeated on a different CMOS chip to evaluate the reproducibility of the

results (right graph of Figure 5.18). The last 30 minutes of a 90-minute-long period are shown for this second measurement. Notably, the output frequency varies between different CMOS chips. This is expected due to the mismatch variations between the dies. In the LPFM circuit, ISFETs are paired with a regular MOSFET in the operational amplifier of the V-to-I converter phase. One way to reduce this mismatch would be to use an array of pixels, where the random mismatch error could be eliminated by increasing the number of simultaneous data points.

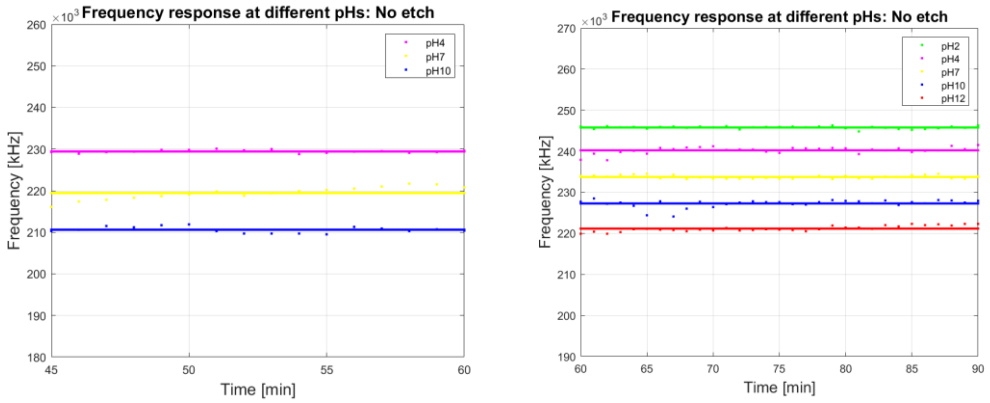


Figure 5.18 Electrochemical measurements of unmodified LPFM architectures. Right: test on LPFM-1 for 60 min, showing the last 15 min. Left: test on LPFM-2 for 90 min, showing the last 30 min.

An average frequency of the last 15/30 minutes was fitted onto a sensitivity graph. The result showed a better consistency than previous static measurement techniques, and the frequency-versus-pH was also linear, as it should be, as shown in Figure 5.19. Similar results were obtained using two different CMOS chips and a greater variety of pH buffers, as shown in the right graph of Figure 5.19. The variation around the mean line was small and showed no time-dependent change. The error bars, which illustrates the variation of the corresponding measurement, represents the standard deviation of the data set. This is a major deviation from various CMOS ISFET measurements reported in the literature. Using the voltage-to-frequency conversion ratio from the electrical measurement, the sensitivity of this device can be calculated as 2.66 kHz/pH or 4.62 mV/pH. This is not unexpected for an unmodified chip with existing foundry-passivation as the sensing layer in TSMC technology. Due to foundry constraints, diodes had to be included in the floating gates to eliminate antenna rule violations that directly affected the sensitivity of the devices [7].

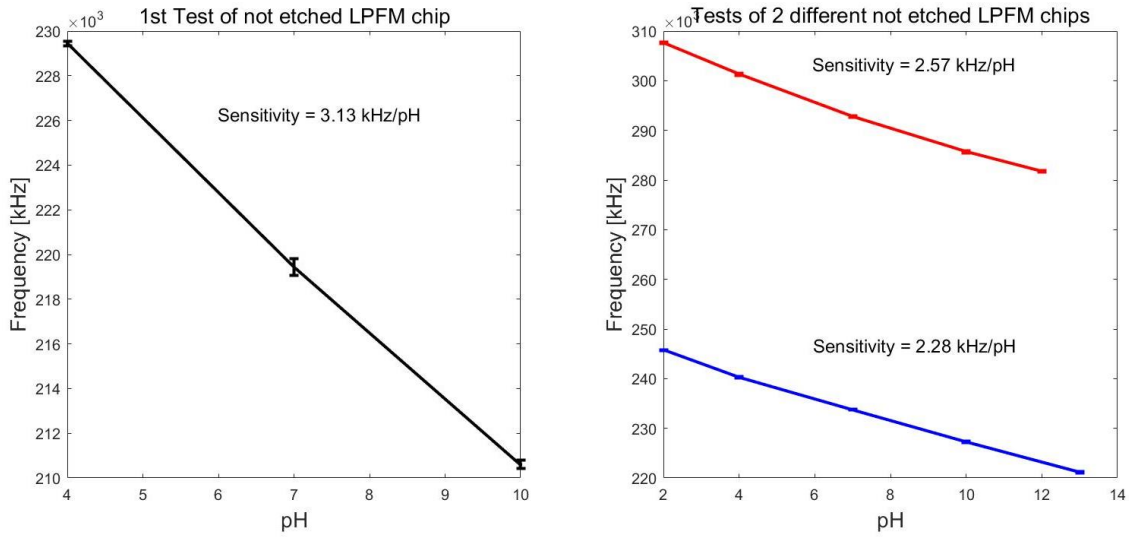


Figure 5.19 Sensitivity of non-etched LPFM architectures for different CMOS chips.

b) Thinned Passivation Layer CMOS-V2: LPFM

The next batch of ISFET devices underwent an etching process where part of the passivation layer was removed to evaluate the impact on the output sensitivity. A one-minute etch was performed, removing an estimated total of 0.248 µm of Si_3N_4. The experiments were repeated using both previous protocols (60 min with three buffers and 90 min with five buffers using three different CMOS chips). Figure 5.20 shows the results using these devices. It is important to highlight that the output frequency difference increased between pH values in all cases compared to the non-etched CMOS chips. However, the results show a higher degree of variation around the mean. The etching used in this work might have impacted the surface roughness of the device. This non-uniformity in the area of interest could have affected the sensitivity of the devices. Roughness increases as a function of the etching time. It also depends on the proposed gas composition, affecting the surface of the sensing area by creating irregularities and leading to variability of the threshold voltage due to deviating gate lengths that will modify the sensitivity [171].

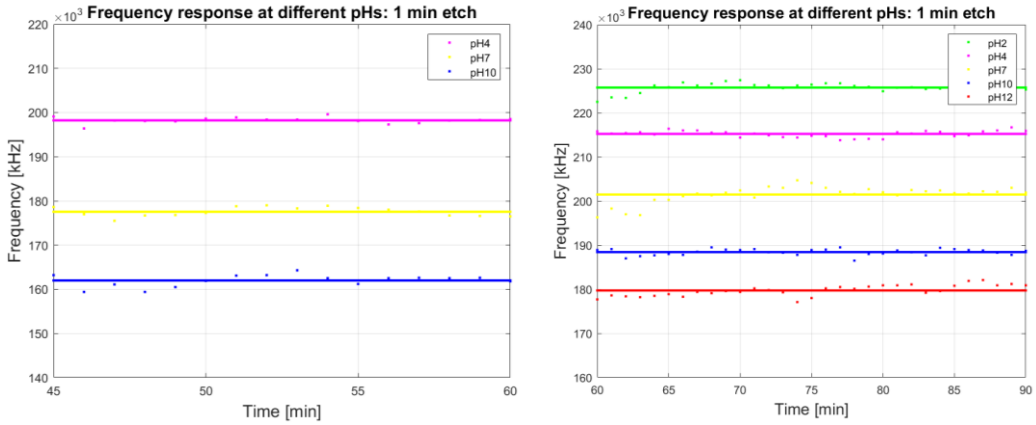


Figure 5.20 Electrochemical measurements of one-minute etched LPFM architectures. Right: test on LPFM-1 for 60 min, showing the last 15 min. Left: test on LPFM-2 for 90 min, showing the last 30 min.

Once again, the average was plotted in a sensitivity graph, as shown in Figure 5.21. The sensitivity of these devices increased to an average of 5.19 kHz/pH or 9.01 mV/pH, confirming the relationship between the passivation thickness and the output sensitivity. However, it was noted that the mean frequency for the same buffer did not match between the experiments (e.g., for pH=4). This can be attributed to the experimental protocol, where the entire electrochemical setup was thoroughly cleaned. Mismatch, post-processing variations between the devices and the time gap between each separate set of measurements might also have affected the results. However, it is acknowledged that the consistency of ISFET characterisation across different setups is still a major problem.

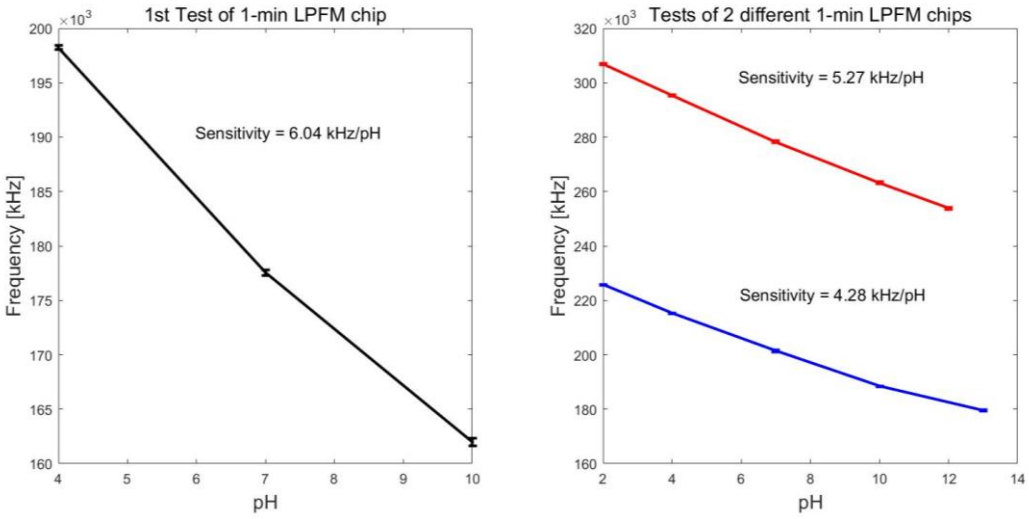


Figure 5.21 Sensitivity of 1-min etched LPFM architectures for different CMOS chips.

Following the same protocols, a third batch of ISFET devices underwent a three-minute etching process, removing an estimated total of 0.478 µm of Si_3N_4. Figure 5.22 shows two of the three measurements done in different CMOS chips. In this case, the output frequency difference is even higher than in the previous case, and the degree of variation around the mean remains consistent between measurements. As expected, the devices show a higher pH sensitivity when the Si_3N_4 layer is thinner.

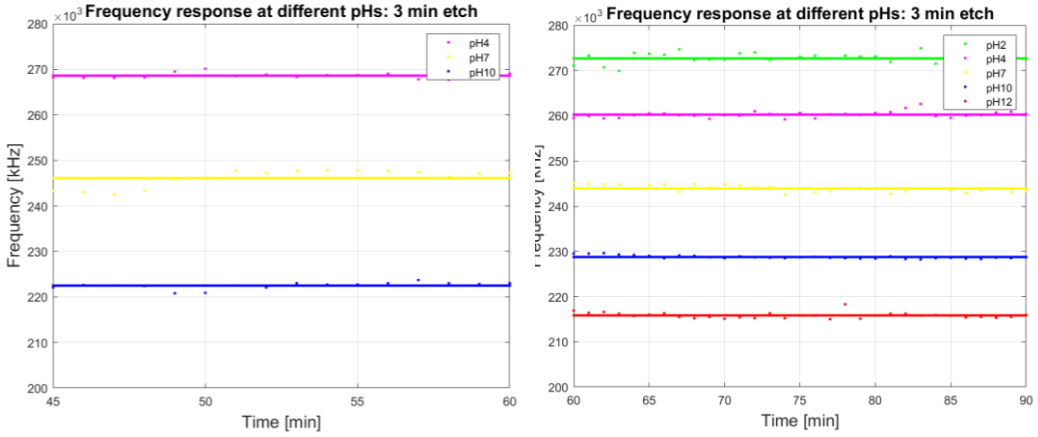


Figure 5.22 Electrochemical measurements of three-minute etched LPFM architectures. Right: test on LPFM-1 for 60 min, showing the last 15 min. Left: test on LPFM-2 for 90 min, showing the last 30 min.

Figure 5.23 illustrates the sensitivity graphs of these cases, indicating an upward trend to an average of 6.7 kHz/pH or 11.62 mV/pH. Again, the same pattern is evident in this scenario, with varying means observed between CMOS chips using identical pH buffers, yet consistency in linearity is maintained across all instances.

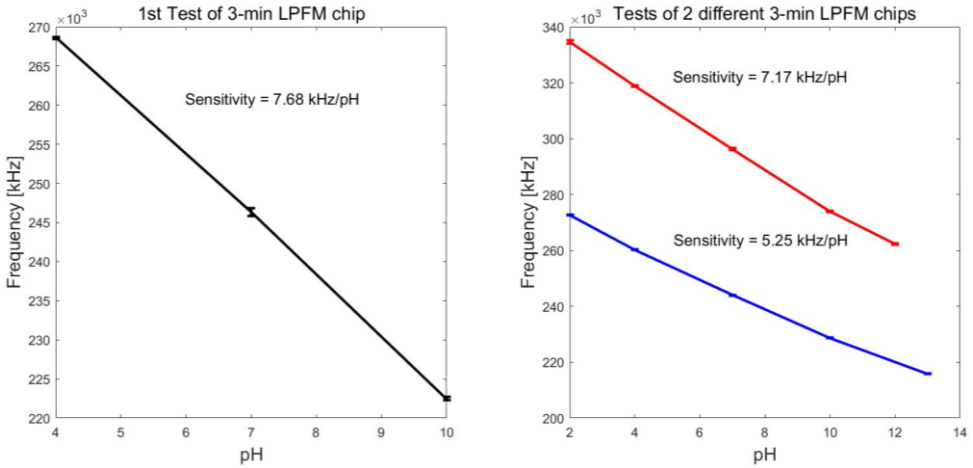


Figure 5.23 Sensitivity of 3-min etched LPFM architectures for different CMOS chips.

Finally, a single ISFET device underwent a five-minute etching process, removing an estimated total of 0.698 µm Si_3N_4, more than 100% of the Si_3N_4 of the passivation layer. In this case, the device started to present an inconsistent behaviour where, although it still detected a mean difference between pH values, the output was not exceptionally stable over time, especially with pH 10. The sensitivity also didn't increase but decreased considerably, even from the initial CMOS chips without etching. This could mean the sensing layer became irregular and insensitive to pH changes. A reasonable explanation could be related to how the etching process works, as it creates a rough surface with varying heights that can become significant with higher etching times. In this CMOS chip, the Si_3N_4 was gone, reaching the SiO_2 of the sensing surface, making it difficult to give reliable results with a non-uniform and insensitive surface due to the post-processing. The results are shown in Figure 5.24.

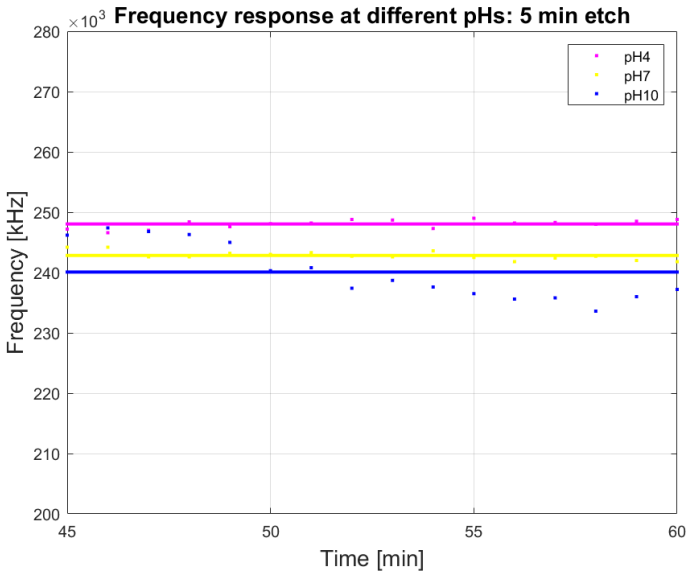


Figure 5.24 Electrochemical measurements of 5-min etched LPFM architectures. Test on LPFM-1 for 60 min, showing the last 15 min.

For this case, the sensitivity graph in Figure 5.25 decreases compared to the previous results, giving an average value of 1.328 kHz/pH or 2.30 mV/pH. The relationship frequency-versus-pH is also less linear than in the previous cases, and the standard errors shown are the highest of all the experiments performed, particularly for pH 10.

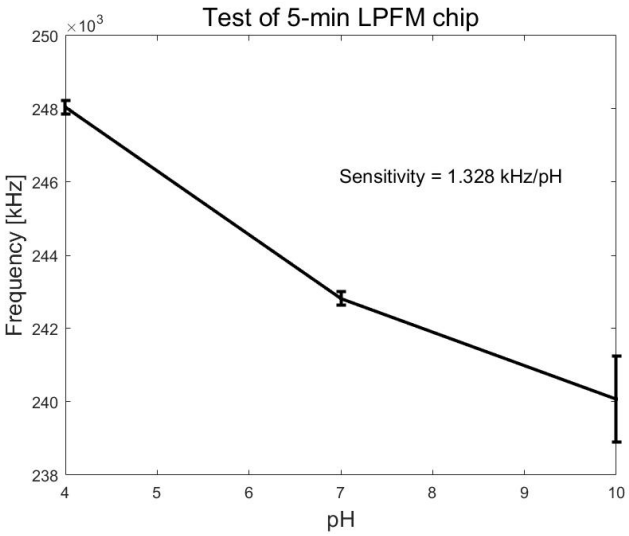


Figure 5.25 Sensitivity of 5-min etched LPFM architecture using a single CMOS chip.

Figure 5.26 summarises the frequency sensitivity against the etching time for different CMOS chips. It is evident from the trend that the sensitivity reaches a maximum for a three-minute etching (0.122 µm of Si_3N_4) and decays significantly after that. For future reference, changes in the etching recipe can be made to perform slower etching processes that will allow for a more detailed evaluation of the etched surface to maximise the sensitivity of the devices.

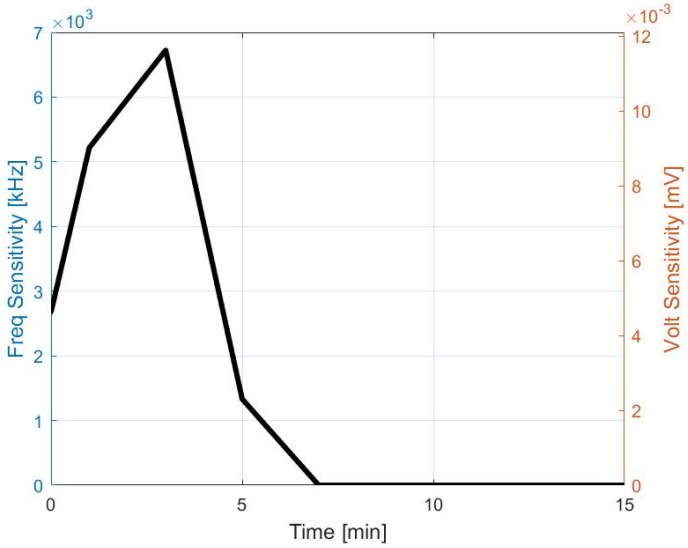


Figure 5.26 Frequency sensitivity against LPFM architecture etching time.

Similarly, Table 5-2 summarises all the information presented throughout the chapter to show the behaviour of the devices in each scenario. Two cases presented here were

not described: seven and 15-minute etches. These cases were discarded because the etching went through the SiO_2, making the devices insensitive to pH variations. Both CMOS chips were tested under solution without any response to either the solution or V_{ref} values, which is consistent with the literature.

Pass layer thickness	Sensitivity (kHz/pH)	Sensitivity (mV/pH)
0 min etch (Si_3N_4 0.6 µm SiO_2 1.25 µm)	2.66	4.62
1 min etch (Si_3N_4 0.352 µm SiO_2 1.25 µm)	5.19	9.01
3 min etch (Si_3N_4 0.122 µm SiO_2 1.25 µm)	6.70	11.62
5 min etch (Si_3N_4 0 µm SiO_2 1.05 µm)	1.33	2.30
7 min etch (Si_3N_4 0 µm SiO_2 0.825 µm) *	0	0
15 min etch (Si_3N_4 0 µm SiO_2 0.730 µm) *	0	0

Table 5-2 Passivation layer thickness and their respective average sensitivity.

Table 5-3 outlines the sensor characteristics compared to several ISFET architectures in the frequency domain. These designs were post-processed and/or tested under solution. It is important to clarify that most of them were manufactured in 0.35 µm technology, and thus have different design rules to follow. The sensitivity and power consumption were measured using a ΔV = 600 mV, but the modularity of the architecture allows a variable dynamic response depending on the setup conditions, with a min-max power consumption of 71.69–223 µW.

The disadvantages of nonlinear architectures are that they require precise calibration to work under a specific working region, making them difficult to handle. The work presented in [82] resembles the proposed design, but it demonstrates a nonlinear frequency behaviour. The main difference relies on the constant discharging phase of the capacitor. The ISFET is also not part of the closed-loop feedback, having a much higher PVT variation.

Regarding the linear architectures, the work in [81] post-processed the surface to remove the passivation layer thin films and left an oxide thickness of approximately 110 nm, increasing the sensitivity with significant PVT variation. Liao et al. [83] presented a similar design with a much higher power consumption due to the simultaneous use of the comparators and adding an extra capacitor to the architecture. This work saves 13 times more power while providing a higher frequency sensitivity

at the output. Compared to the only architecture manufactured in 0.18 µm technology with a linear response [103], this work demonstrates a doubled frequency sensitivity with twice the power consumption, making it clear that compromises need to be made regarding the complexity of the design against the sensitivity required.

	[77]	[80]	[81]	[83]	[82]	[103]	This work
Technology	0.35 µm	0.35 µm	0.35 µm	0.35 µm	0.18 µm	0.18 µm	**0.18 µm**
Sensing Area	n.a.	64 µm x 54 µm	30 µm x 30 µm	Octogonal ring; diameter 250 µm	80 µm x 80 µm	20 µm x 2 µm	**125 µm x 125 µm**
Post-processing	Etching & polishing	Unmodified die	Etching & polishing	Al_2O_3 deposition	Unmodified die*	Unmodified die	**Etching**
Instrumentation	Pulse Frequency Modulator	3-stage ring oscillator	5-stage ring oscillator	Current-controlled oscillator	Current-controlled oscillator	Log domain oscillator	**Current-controlled oscillator**
Supply Voltage	n.a.	1.2 V	n.a.	n.a.	1 V	3.3 V / 1.8 V	**1.4 V - 1.8 V**
pH range	4 - 10	5 - 7	3 - 9	6 - 8	1 - 14	4 - 10	**2 - 12**
Sensitivity	0.070 - 11.6 MHz/pH	6 - 8 kHz/pH	250 kHz/pH	2.2 kHz/pH	≈ 138 kHz/pH	3 kHz/pH	**6.7 kHz/pH**
Power Consumption	n.a.	6 µW	n.a.	1.9 mW	40.2 µW	76 µW	**144.2 µW**

*Table 5-3 Comparison of pH-to-frequency architectures.*Preliminary results of [82] were in agreement with the simulations.*

5.4 Summary

In this chapter, two measurement methods (Static and Dynamic) were described in detail to evaluate the performance of the LPFM architecture. The sections focused on electrochemical characterisation performed in unmodified and thinned CMOS chips using pH buffer solutions. A major challenge was presented for this device in terms of the output response over long periods. The new Dynamic Method was proposed to achieve successful results for this type of design with unknown passivation capacitance. It also demonstrated the etching process' applicability to increase the devices' sensitivity by partially removing the surface of the passivation layer. However, the devices showed lower sensitivity than what has been reported in other technologies (e.g., AMS). This leaves room to assess other variables in the TSMC technology that might have caused noticeable changes in the output sensitivity. The strict DRC/antenna rules and the properties of the metal layers used for the ISFET layout could have a significant contribution.

Chapter 6

Conclusion

6.1 Overview of the CMOS ISFET Designs

In recent decades, the integration and miniaturisation of CMOS electrochemical sensors have focused on developing integrated systems for applications in telecommunications, healthcare and environmental monitoring, among others, taking advantage of their high performance and low fabrication cost. One of the applications of interest is using ISFETs to detect bioanalytical signals, using small-size, low-power devices with high sensitivity. The technology has been extensively researched and demonstrated to be capable of accurately detecting pH levels. This research aims to develop a microchip capable of monitoring biopotential signals, such as pH, by creating a front-end platform that can overcome some of the main challenges of this type of sensor.

After reviewing the current ISFET technology, going from its fundamental principles to the most promising applications of interest, this thesis presented two CMOS front-end architectures: a nonlinear PFM and a linear PFM. The importance of a pH-to-frequency conversion relies on its main advantages, such as a high immunity to noise, less signal processing as it converts the output into a digital signal, and compatibility to provide stable results against supply voltage variations. Both were designed in TSMC technology and electrically characterised before further post-processing. Customised PCB platforms were designed for operating the architectures, and their corresponding output frequencies were analysed. Both designs showed potential for operating a range of interest, but the LPFM were the architecture selected for the next stage of the design.

Several post-processing steps were investigated for suitable microfabrication processes on small 2 × 2 mm CMOS chips. First, the surface was analysed to evaluate the composition of the layers, as well as the corresponding thickness of each of them. The passivation layer was then removed and replaced with Ta_2O_5 in a sputtering process with a thickness of 100 nm. Finally, the original passivation thickness was thinned to

different thicknesses on a different batch using an etching process with different processing times.

An off-chip readout system was developed for data acquisition, and the devices were fully encapsulated for electrochemical testing. The data were obtained using a Static and Dynamic Measurement Method. The difference arises from the time that the voltage supplies remain on, allowing the architecture to give different behaviours of the output responses. The Static Method showed a continuous decay response that tended to zero in a relatively short period. In contrast, the Dynamic Method allowed for recording of the instantaneous frequency by pulsing the input voltages, keeping the duty cycle small for V_{ref} to fully discharge before the next pulse signal is send. The Dynamic Method was then used to record the response of the ISFET devices for long periods in different batches. The data related to the sensitivity of each case was analysed against the thickness of the passivation layer.

This work demonstrates the applicability of two small and low-power analogue front-end architectures to transduce a pH signal into the frequency domain as pH sensing platforms. One in particular, the LPFM architecture with a programmable dynamic range for pH detection showed the best features in terms of power consumption, steady response against power supply variations, high immunity against noise and a rail-to-rail linear response at the output. Microfabrication techniques were applied to improve the sensitivity of the devices. An etching process was done to thin the passivation layer in order to enhance the output response by 250% with an 80% reduction of the Si_3N_4 layer, resulting in a maximum output frequency of 6.7 kHz/pH A new recording method was also proposed to overcome the continuous decay of the signal. The Dynamic Method consisted of recording the instantaneous frequency for the first 100 µs of every minute, while the rest of the time the system remains off. Data showed good stability and repeatability considering all the factors involved in an electrochemical measurement, as well as the variabilities of the CMOS chips depending on their manufacture, which includes layout variations and rules imposed by the technology to comply with antenna violations.

However, while this work has provided valuable insights into the subject matter, is it essential to acknowledge some of the challenges and limitations that have arisen during the process. These issues can be divided as follows:

1. Frequency variability: Although it is true that the results showed some consistency in the variation of frequency between pHs, it is also important to clarify that the actual frequency values were not the same from chip to chip due to mismatch behaviour. The main objective was to first develop a single front-end architecture to then move to an array of pixels so that the average of multiple signals can overcome this problem.
2. Manual frequency counter: One of the main issues to be addressed is related to the way in which the data was handled for further analysis. Because there was no automatic system or adequate internal signal processing, it was decided to take manual measurements based on the capabilities of a Picoscope. This method is less accurate, more time-consuming and sometimes subject to errors due to multiple time frames where the detection system missed the signal because it happened extremely quickly. The decision to use this method was contemplated because the initial interest was to observe the trend that follows to use it as an alternative to the problems encountered with the decaying signal.
3. Etching recipe: The post-processing used for this work was intended to remove the entire passivation layer (both SiO_2 and Si_3N_4) instead of thinning just the most external layer of Si_3N_4. Therefore, the recipe took approximately 5 minutes to remove the entire layer, which is a very short time to analyse different scenarios and its uniformity was not considered as an important factor at the beginning.
4. TSMC technology: Through Chapter 5, the possible impact of the properties of the technology that were used for the fabrication of the CMOS chips was highlighted. Furthermore, the most recent literature showed similar behaviour in another ISFET design where the signal was not as strong as expected in unmodified devices [7], based on other results in different technologies, such as AMS. More research is needed to evaluate whether the limitations of this technology for this type of sensor overshadow its benefits.

5. Common challenges (drift and trapped charge): Finally, some important common challenges are still a matter of subject, as the signal exhibited unexpected behaviour when testing was done in a continuous way. Possible causes were analysed, but it is still necessary to evaluate the impact of the drift and trapped charge on the final outcome of the signal as a whole, contemplating the additional factors that affected the decaying response.

Chapter 7

Future Work

7.1 Introduction

The outcome of this research aimed to showcase the efficacy of a functional sensing platform, proficient in signal transduction from pH levels to frequency, employing a single front-end architecture. However, a spectrum of improvements remains available for refining the functionality of the architecture, considering all the challenges and guidelines learned during the course of the research. This chapter outlines the foremost enhancements in detail.

7.2 Array of CMOS Sensors

A possible future step would be to design an array of CMOS ISFET sensors to improve the noise performance. Noise in a CMOS chip can be divided into three components: thermal noise, flicker noise and shot noise, all with different origins and, therefore, all independent from each other. It has been demonstrated that averaging a signal from an array of small independent sensors has a better signal-to-noise ratio than a single sensor with a large sensing area [172].

Furthermore, one of the main issues of the LPFM architecture is related to the process mismatch present between the two inputs of the V-to-I converter, as one of them is working as an ISFET with the gate exposed, while the other is a regular MOSFET, leading to increased variations between measurements from chip to chip. Large sensing areas can solve this issue together with compensation schemes like a programmable gate capacitor for temporal calibration of the threshold voltage [173]. An array of pixels sharing common measurement units also increases the total in-chip sensing area, making the design more robust against noise and mismatch variations.

7.3 Cancellation of common-mode noise

One approach that has shown good potential in eliminating the common mode noise is by using a differential arrangement consisting of an ISFET and an ion-insensitive structure or reference field-effect transistor (REFET). Therefore, the change in the pH of the solution is measured as a differential voltage, where the ISFET responds to the pH and the REFET does not. In this way, a REFET will get rid of common mode disturbances such as undefined metal-liquid interface, leakage current and temperature effects by subtracting them from the ISFET response [174].

Several REFETs haven been analysed based on different approaches, but the general idea is to create an insensitive layer that blocks the interaction with the ionic concentration. Layers of buffered hydrogel, paralyne, acrylate membranes with an intermediate hydrogel layer and polyvinyl chloride (PVC) are some examples of materials used to create a REFET structure [175]. In this case, one end of the OTA amplifier used for the V-to-I Converter works as a regular MOSFET, thus creating mismatch problems. This MOSFET could be replaced with a REFET by modifying the surface of a regular ISFET to be insensitive to pH with some of the materials reported in the literature.

7.4 Subthreshold operation of an ISFET

ISFETs in subthreshold mode are becoming more common in modern electronics for applications where the power consumption and transconductance efficiency are critical [176]. These devices exhibit enhanced sensitivity to changes in ion concentration due to their logarithmic response characteristic, making them ideal for low-voltage, low-power and high-resolution sensing applications [20]. It allows ISFETs to operate with minimal power consumption while maintaining a high level of precision in ion detection.

In the case of the LPFM architecture, the system partially works under this condition, as it exhibits a rail-to-rail output where the gate needs as minimum as 150 mV to begin working in a linear behaviour. However, an interesting application would be to delimit the working region to work only in subthreshold mode [56], thus making the system

as efficient as possible in terms of power consumption, particularly for applications where the detection of the whole range of pH is not necessary.

7.5 Event-driven (ED) Scheme

Following the progress of neuromorphic vision research, an array of pixels using these architectures would need an event-driven scheme based on address-event representation (AER). This is a communication protocol for transferring the state of an array of analogue time-dependent variables, exploiting the concept of pulse density modulation for coding information. In basic terms, the outgoing pulses from each pixel are encoded based on their physical address and transmitted asynchronously [177].

Since the LPFM architecture creates a signal with a fixed pulse width and variable frequency, an AER-based scheme could be ideal for communicating high-density data from a large array of pH sensors. Each time a pixel generates a pulse (or event), it communicates with the array periphery, and a code or address is placed on an external bus. At the receiver end, the pulses are directed to the pixels whose code or address was on the bus, always showing the same pulse stream on both sides. This protocol also gives channels with high priority more opportunities to transmit their respective pulses [178].

In this case, the output signals will follow the same principle, requiring a protocol that facilitates the transmission of information from an array of pixels with data in the frequency domain. This scheme has several advantages, like fast data acquisition, low communication bandwidth, high-energy efficiency and brain-like processing [179].

7.6 On-chip Signal Processing

One of the main limitations of the current designs is that information needs to be handled externally. The front-end architectures only provide a pulse train at the output, leaving the signal processing as an additional external cycle to get the final data in the desired format. This is done by using the properties of a Picoscope and manually getting the instantaneous frequency per minute through signal recording. The design

requires additional block components that translate the original signal into more concrete data to make a more reliable and independent system.

For instance, considering the work proposed previously, an array of pixels will require row and column decoders to access individual pixels and a frequency counter to present the data of interest in an easier way to manipulate. Concepts like placement optimisation and design metrics for energy efficiency (power consumption) and cost (area) also have an impact on the layout design if additional signal processing blocks are required to get a more robust design [180].

7.7 Further Post-processing: Ta_2O_5 deposition, Microfluidics Channels and Surface Modification

One of the main improvements that can have an impact on the sensitivity of the devices is to complete the Ta_2O_5 deposition that was postponed due to the pandemic restrictions that avoided the corresponding analysis on the latest design of interest. The results showed that the unmodified sensing double layer of SiO_2/Si_3N_4 is slightly sensitive to pH changes, and literature has shown that Ta_2O_5 have better properties than most of the sensing layers used in CMOS devices. Another application of interest is the applicability of these designs as real time readout systems for dynamic measurements. Until now, data have been taken one pH at a time. The CMOS chips go through a cleaning process before another solution of a different pH is deposited into the chamber, making it impossible to record the response of the architectures to a change in pH. Although the pH solution could be modified by adding basic or acidic solutions directly into the chamber, the setup did not have a way to measure the change in pH with another verification method in the background.

The concept of incorporating custom microfluidics channels on the surface of the sensing area will allow the system to change the solution with calibrated pH values without the need to clean the surface every time, providing a clearer picture of the response of the architectures to real-time changes in the pH. Adding these channels will also ensure a uniform fluid flow of the pH solution directly on top of the exposed

gate and provide a more robust controllable delivery setup for more extended pH measurements [181].

Lastly, once the suggested improvements are implemented, the device should be ready for surface modification for the selectivity of various ions depending on the application of interest. It has been demonstrated that these platforms can be used for multiple ion detection [19] as well as that of other molecules, such as enzymes, antibodies and genetic markers, through the immobilisation of binding agents on the sensing area surface. Further work should be done to develop a working system that can be used for specific applications involving medical diagnostics, environmental monitoring and food safety.

References

[1] J. Cortes-Guzman, A. Tsiamis, D. R. S. Cumming, and S. Mitra, ‘Linear Pulse-Frequency Modulator ISFET with a Wide Supply Range’, in *2021 IEEE Sensors*, Sydney, Australia: IEEE, Oct. 2021, pp. 1–4. doi: 10.1109/SENSORS47087.2021.9639752.

[2] R. Scaff, M. B. Fontes, and S. G. Dos Santos Filho, ‘Characterization of an ISFET Device as a pH Sensor for Application in the Industrial, Environmental and Biomedical Fields’, *ECS Trans.*, vol. 9, no. 1, pp. 571–578, Sep. 2007, doi: 10.1149/1.2766931.

[3] M. Golio, ‘Fifty Years of Moore’s Law’, *Proc. IEEE*, vol. 103, no. 10, pp. 1932–1937, Oct. 2015, doi: 10.1109/JPROC.2015.2473896.

[4] C.-S. Lee, S. Kim, and M. Kim, ‘Ion-Sensitive Field-Effect Transistor for Biological Sensing’, *Sensors*, vol. 9, no. 9, pp. 7111–7131, Sep. 2009, doi: 10.3390/s90907111.

[5] R. Goswami and R. Saha, Eds., ‘Contemporary Trends in Semiconductor Devices: Theory, Experiment and Applications’, in *Lecture Notes in Electrical Engineering*, vol. 850. Singapore: Springer Nature Singapore, 2022. doi: 10.1007/978-981-16-9124-9.

[6] P. Bergveld, ‘Development of an Ion-Sensitive Solid-State Device for Neurophysiological Measurements’, *IEEE Trans. Biomed. Eng.*, vol. BME-17, no. 1, pp. 70–71, Jan. 1970, doi: 10.1109/TBME.1970.4502688.

[7] Y. Liu, T. G. Constandinou, and P. Georgiou, ‘Ultrafast Large-Scale Chemical Sensing with CMOS ISFETs: A Level-Crossing Time-Domain Approach’, *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 6, pp. 1201–1213, Dec. 2019, doi: 10.1109/TBCAS.2019.2947167.

[8] S. Sinha and T. Pal, ‘A Comprehensive Review of FET-based pH Sensors: Materials, Fabrication Technologies, and Modeling’, *Electrochem. Sci. Adv.*, vol. 2, no. 5, Oct. 2022, doi: 10.1002/elsa.202100147.

[9] N. Moser, T. S. Lande, C. Toumazou, and P. Georgiou, ‘ISFETs in CMOS and Emergent Trends in Instrumentation: A Review’, *IEEE Sens. J.*, vol. 16, no. 17, pp. 6496–6514, Sep. 2016, doi: 10.1109/JSEN.2016.2585920.

[10] P. Li, G.-H. Lee, S. Y. Kim, S. Y. Kwon, H.-R. Kim, and S. Park, ‘From Diagnosis to Treatment: Recent Advances in Patient-Friendly Biosensors and Implantable Devices’, *ACS Nano*, vol. 15, no. 2, pp. 1960–2004, Feb. 2021, doi: 10.1021/acsnano.0c06688.

[11] R. P. Buck, D. E. Hackleman, and W. R. Kenan, ‘Field-Effect Potentiometric Sensors’, *Anal. Chem.*, vol. 49, no. 14, pp. 2315–2321, Dec. 1977, doi: 10.1021/ac50022a051.

[12] Sah Chih-Tang, ‘Evolution of the MOS Transistor from Conception to VLSI’, *Proc. IEEE*, vol. 76, no. 10, pp. 1280–1326, Oct. 1988, doi: 10.1109/5.16328.

[13] S. Cao *et al.*, ‘ISFET-Based Sensors for (Bio)chemical Applications: A Review’, *Electrochem. Sci. Adv.*, Mar. 2022, doi: 10.1002/elsa.202100207.

[14] T. C. Carusone, D. Johns, K. W. Martin, and D. Johns, *Analog Integrated Circuit Design*, 2nd ed. Hoboken, NJ: John Wiley & Sons, 2012.

[15] D. A. Neamen, *Microelectronics: Circuit Analysis and Design*, 4th ed. New York: McGraw-Hill, 2010.

[16] R. Chaudhary *et al.*, ‘Fabrication and Characterization of Al Gate n-MOSFET, On-Chip Fabricated with Si_3N_4 ISFET’, in *2015 19th International Symposium on VLSI Design and Test*, Ahmedabad, India: IEEE, Jun. 2015, pp. 1–4. doi: 10.1109/ISVDAT.2015.7208083.

[17] D. Welch, S. Shah, S. Ozev, and J. Blain Christen, ‘Experimental and Simulated Cycling of ISFET Electric Fields for Drift Reset’, *IEEE Electron Device Lett.*, vol. 34, no. 3, pp. 456–458, Mar. 2013, doi: 10.1109/LED.2013.2240648.

[18] M. W. Shinwari, D. Zhitomirsky, I. A. Deen, P. R. Selvaganapathy, M. J. Deen, and D. Landheer, ‘Microfabricated Reference Electrodes and their Biosensing Applications’, *Sensors*, vol. 10, no. 3, pp. 1679–1715, Mar. 2010, doi: 10.3390/s100301679.

[19] N. Moser *et al.*, ‘Complementary Metal–Oxide–Semiconductor Potentiometric Field-Effect Transistor Array Platform Using Sensor Learning for Multi-ion

Imaging', *Anal. Chem.*, vol. 92, no. 7, pp. 5276–5285, Apr. 2020, doi: 10.1021/acs.analchem.9b05836.

[20] S. Martinoia, G. Massobrio, and L. Lorenzelli, 'Modeling ISFET Microsensor and ISFET-Based Microsystems: A Review', *Sens. Actuators B Chem.*, vol. 105, no. 1, pp. 14–27, Feb. 2005, doi: 10.1016/S0925-4005(04)00107-8.

[21] P. Zarzycki, R. Charmas, and P. Szabelski, 'Study of Proton Adsorption at Heterogeneous Oxide/Electrolyte Interface. Prediction of the Surface Potential using Monte Carlo Simulations and 1-pK Approach', *J. Comput. Chem.*, vol. 25, no. 5, pp. 704–711, Apr. 2004, doi: 10.1002/jcc.10419.

[22] R. E. G. van Hal, J. C. T. Eijkel, and P. Bergveld, 'A Novel Description of ISFET Sensitivity with the Buffer Capacity and Double-Layer Capacitance as Key Parameters', *Sens. Actuators B Chem.*, vol. 24, no. 1–3, pp. 201–205, Mar. 1995, doi: 10.1016/0925-4005(95)85043-0.

[23] M. Spijkman, E. C. P. Smits, J. F. M. Cillessen, F. Biscarini, P. W. M. Blom, and D. M. de Leeuw, 'Beyond the Nernst-Limit with Dual-Gate ZnO Ion-Sensitive Field-Effect Transistors', *Appl. Phys. Lett.*, vol. 98, no. 4, p. 043502, Jan. 2011, doi: 10.1063/1.3546169.

[24] S. Martinoia and G. Massobrio, 'A Behavioral Macromodel of the ISFET in SPICE', *Sens. Actuators B Chem.*, vol. 62, no. 3, pp. 182–189, Mar. 2000, doi: 10.1016/S0925-4005(99)00377-9.

[25] J.R.K. Marland et al., 'Implantable Microsystems for Personalised Anticancer Therapy' in *CMOS Circuits for Biological Sensing and Processing*, S. Mitra and D. R. S. Cumming, Eds., Cham: Springer International Publishing, 2018. doi: 10.1007/978-3-319-67723-1.

[26] L. Bousse, 'Single Electrode Potentials Related to Flat-Band Voltage Measurements on EOS and MOS Structures', *J. Chem. Phys.*, vol. 76, no. 10, pp. 5128–5133, May 1982, doi: 10.1063/1.442812.

[27] L. Bousse, N. F. De Rooij, and P. Bergveld, 'Operation of Chemically Sensitive Field-Effect Sensors as a Function of the Insulator-Electrolyte Interface', *IEEE Trans. Electron Devices*, vol. 30, no. 10, pp. 1263–1270, Oct. 1983, doi: 10.1109/T-ED.1983.21284.

[28] A. Poghossian and M. J. Schöning, ‘Capacitive Field-Effect EIS Chemical Sensors and Biosensors: A Status Report’, *Sensors*, vol. 20, no. 19, p. 5639, Oct. 2020, doi: 10.3390/s20195639.

[29] W. M. Siu and R. S. C. Cobbold, ‘Basic Properties of the Electrolyte—SiO_2—Si Ssystem: Physical and Theoretical Aspects’, *IEEE Trans. Electron Devices*, vol. 26, no. 11, pp. 1805–1815, Nov. 1979, doi: 10.1109/T-ED.1979.19690.

[30] S Sinha, R Rathore, S K Sinha, R Sharma, R Mukhiya, and V K Khanna, ‘Modeling and Simulation of ISFET Microsensor For Different Sensing Films’, 2014, doi: 10.13140/2.1.2123.4564.

[31] F. Nasir and M. A. Mohammad, ‘Investigation of Device Dimensions on Electric Double Layer Microsupercapacitor Performance and Operating Mechanism’, *IEEE Access*, vol. 8, pp. 28367–28374, 2020, doi: 10.1109/ACCESS.2020.2972080.

[32] T. Kevkić, R. Maity, D. Todorović, B. Vučković, and N. Maity, ‘Analysis of Static Behavior of Ion-Sensitive Field-Effect Transistor for pH Measurements’, *Bull. Nat. Sci. Res.*, vol. 12, no. 1, pp. 21–27, 2022, doi: 10.5937/bnsr12-37850.

[33] D. E. Yates, S. Levine, and T. W. Healy, ‘Site-Binding Model of the Electrical Double Layer at the Oxide/Water Interface’, *J. Chem. Soc., Faraday Trans. 1*, 1974,70, 1807-1818, doi: https://doi.org/10.1039/F19747001807.

[34] C. Hazarika and S. Sharma, ‘Survey on Ion Sensitive Field Effect Transistor from the View Point of pH Sensitivity and Drift’, *Indian J. Sci. Technol.*, vol. 10, no. 37, pp. 1–18, Sep. 2017, doi: 10.17485/ijst/2017/v10i37/118444. [35] M. Waleed Shinwari, M. Jamal Deen, and D. Landheer, ‘Study of the Electrolyte-Insulator-Semiconductor Field-Effect Transistor (EISFET) with Applications in Biosensor Design’, *Microelectron. Reliab.*, vol. 47, no. 12, pp. 2025–2057, Dec. 2007, doi: 10.1016/j.microrel.2006.10.003.

[36] L. Keeble, N. Moser, J. Rodriguez-Manzano, and P. Georgiou, ‘ISFET-Based Sensing and Electric Field Actuation of DNA for On-Chip Detection: A Review’, *IEEE Sens. J.*, vol. 20, no. 19, pp. 11044–11065, Oct. 2020, doi: 10.1109/JSEN.2020.2998168.

[37] P. Georgiou and C. Toumazou, ‘ISFET Characteristics in CMOS and their Application to Weak Inversion Operation’, *Sens. Actuators B Chem.*, vol. 143, no. 1, pp. 211–217, Dec. 2009, doi: 10.1016/j.snb.2009.09.018.

[38] M. J. Milgrew, D. R. S. Cumming, and P. A. Hammond, ‘The Fabrication of Scalable Multi-Sensor Arrays using Standard CMOS Technology’, in *Proceedings of the IEEE 2003 Custom Integrated Circuits Conference, 2003.*, San Jose, CA, USA: IEEE, 2003, pp. 513–516. doi: 10.1109/CICC.2003.1249450.

[39] P. A. Hammond, D. R. S. Cumming, and D. Ali, ‘A Single-Chip pH Sensor Fabricated by a Conventional CMOS Process’, in *Proceedings of IEEE Sensors*, Orlando, FL, USA: IEEE, 2002, pp. 350–355. doi: 10.1109/ICSENS.2002.1037115.

[40] M. J. Milgrew and D. R. S. Cumming, ‘Matching the Transconductance Characteristics of CMOS ISFET Arrays by Removing Trapped Charge’, *IEEE Trans. Electron Devices*, vol. 55, no. 4, pp. 1074–1079, Apr. 2008, doi: 10.1109/TED.2008.916680.

[41] P. Georgiou and C. Toumazou, ‘ISFET Threshold Voltage Programming in CMOS Using Hot-Electron Injection’, *Electron. Lett.*, vol. 45, no. 22, p. 1112, 2009, doi: 10.1049/el.2009.2310.

[42] M. Gantier, M. Kalofonou, and C. Toumazou, ‘A Trapped Charge Compensation Scheme for ISFET Based Translinear Circuits’, in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence: IEEE, May 2018, pp. 1–5. doi: 10.1109/ISCAS.2018.8351615.

[43] N. Moser, L. Petrou, Y. Hu, and P. Georgiou, ‘An ISFET Pixel with Integrated Trapped Charge Compensation using Temperature Feedback’, in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*, Florence: IEEE, 2018, pp. 1–5. doi: 10.1109/ISCAS.2018.8351358.

[44] N. Miscourides and P. Georgiou, ‘Calibrating for Trapped Charge in Large-Scale ISFET Arrays’, *IEEE Sens. J.*, vol. 20, no. 10, pp. 5110–5118, May 2020, doi: 10.1109/JSEN.2020.2968578.

[45] M. Sohbati, ‘Circuits and Systems for DNA Detection by Ion-Sensitive Field Effect Transistor’, Ph.D. dissertation, Electrical and Electronic Engineering Department, Imperial College London, London, 2014.

[46] M. Sohbati and C. Toumazou, ‘Dimension and Shape Effects on the ISFET Performance’, *IEEE Sens. J.*, vol. 15, no. 3, pp. 1670–1679, Mar. 2015, doi: 10.1109/JSEN.2014.2365291.

[47] T. Prodromakis, P. Georgiou, K. Michelakis, and C. Toumazou, ‘Effect of Mobile Ionic-Charge on CMOS Based Ion-Sensitive Field-Effect Transistors (ISFETs)’, in *2009 IEEE International Symposium on Circuits and Systems*, Taipei, Taiwan: IEEE, May 2009, pp. 2165–2168. doi: 10.1109/ISCAS.2009.5118225.

[48] V. K. Khanna, ‘Remedial and Adaptive Solutions of ISFET Non-Ideal Behaviour’, *Sens. Rev.*, vol. 33, no. 3, pp. 228–237, Jun. 2013, doi: 10.1108/02602281311324681.

[49] Y.-J. Huang *et al.*, ‘v’, in *2015 IEEE International Electron Devices Meeting (IEDM)*, Washington, DC, USA: IEEE, Dec. 2015, p. 29.2.1-29.2.4. doi: 10.1109/IEDM.2015.7409792.

[50] A. G. I. Al-Ahdal, ‘Floating Gate ISFET Chemical Inverters: For Semiconductor Based Biomedical Applications’, Ph.D. dissertation, Electrical and Electronic Engineering Department, Imperial College London, London, 2012. [51] P. Woias, L. Meixner, D. Amandi, and M. Schönberger, ‘Modelling the Short-Time Response of ISFET Sensors’, *Sens. Actuators B Chem.*, vol. 24, no. 1–3, pp. 211–217, Mar. 1995, doi: 10.1016/0925-4005(95)85045-7.

[52] L. Bousse, D. Hafeman, and N. Tran, ‘Time-Dependence of the Chemical Response of Silicon Nitride Surfaces’, *Sens. Actuators B Chem.*, vol. 1, no. 1–6, pp. 361–367, Jan. 1990, doi: 10.1016/0925-4005(90)80231-N.

[53] N. Miscourides and P. Georgiou, ‘ISFET Arrays in CMOS: A Head-to-Head Comparison Between Voltage and Current Mode’, *IEEE Sens. J.*, vol. 19, no. 4, pp. 1224–1238, Feb. 2019, doi: 10.1109/JSEN.2018.2881499.

[54] J. C. Chou and Y. F. Wang, ‘Temperature Characteristics of a-Si:H Gate ISFET’, *Mater. Chem. Phys.*, vol. 70, no. 1, pp. 107–111, Apr. 2001, doi: 10.1016/S0254-0584(00)00469-7.

[55] J.-C. Chou, C.-Y. Weng, and H.-M. Tsai, ‘Study on the Temperature Effects of Al_2O_3 Gate pH-ISFET’, *Sens. Actuators B Chem.*, vol. 81, no. 2–3, pp. 152–157, Jan. 2002, doi: 10.1016/S0925-4005(01)00945-5.

[56] S. E. Naimi, B. Hajji, I. Humenyuk, J. Launay, and P. Temple-Boyer, 'Temperature Influence on pH-ISFET Sensor Operating in Weak and Moderate Inversion Regime: Model and Circuitry', *Sens. Actuators B Chem.*, vol. 202, pp. 1019–1027, Oct. 2014, doi: 10.1016/j.snb.2014.06.008.

[57] N. I. M. Noh, K. A. Yusof, A. Z. Abdullah, S. H. Herman, W. Fazlida, and H. Abdullah, 'Light Effect Characterization of ISFET Based pH Sensor with Si_3N_4 Gate Insulator', in *2014 IEEE Symposium on Computer Applications and Industrial Electronics (ISCAIE)*, Penang, Malaysia: IEEE, Apr. 2014, pp. 82–87. doi: 10.1109/ISCAIE.2014.7010214.

[58] Y. Liu, P. Georgiou, T. Prodromakis, T. G. Constandinou, and C. Toumazou, 'An Extended CMOS ISFET Model Incorporating the Physical Design Geometry and the Effects on Performance and Offset Variation', *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4414–4422, Dec. 2011, doi: 10.1109/TED.2011.2168821.

[59] L. Gasparyan, F. Gasparyan, and V. Simonyan, 'Internal Electrical Noises of BioFET Sensors Based on Various Architectures', *Open J. Biophys.*, vol. 11, no. 02, pp. 177–204, 2021, doi: 10.4236/ojbiphy.2021.112006.

[60] X. Huang, H. Yu, X. Liu, Y. Jiang, M. Yan, and D. Wu, 'A Dual-Mode Large-Arrayed CMOS ISFET Sensor for Accurate and High-Throughput pH Sensing in Biomedical Diagnosis', *IEEE Trans. Biomed. Eng.*, vol. 62, no. 9, pp. 2224–2233, Sep. 2015, doi: 10.1109/TBME.2015.2419233.

[61] B. Nemeth, M. S. Piechocinski, and D. R. S. Cumming, 'High-Resolution Real-Time Ion-Camera System Using a CMOS-Based Chemical Sensor Array for Proton Imaging', *Sens. Actuators B Chem.*, vol. 171–172, pp. 747–752, Aug. 2012, doi: 10.1016/j.snb.2012.05.066.

[62] K. Nakazato, M. Ohura, and S. Uno, 'CMOS Cascode Source-Drain Follower for Monolithically Integrated Biosensor Array', *IEICE Trans. Electron.*, vol. E91-C, no. 9, pp. 1505–1515, Sep. 2008, doi: 10.1093/ietele/e91-c.9.1505.

[63] S. Thanapitak and C. Sawigun, 'Flipped Voltage Follower ISFET Readout Circuits', in *2016 5th International Symposium on Next-Generation Electronics (ISNE)*, Hsinchu, Taiwan: IEEE, May 2016, pp. 1–2. doi: 10.1109/ISNE.2016.7543382.

[64] S. Thanapitak, ‘An 1 V - 1 nW Source Follower ISFET Readout Circuit for Biomedical Applications’, in *2015 Science and Information Conference (SAI)*, London, United Kingdom: IEEE, Jul. 2015, pp. 1118–1121. doi: 10.1109/SAI.2015.7237284.

[65] P. Bergveld, ‘Thirty years of ISFETOLOGY What Happened in the Past 30 Years and What May Happen in the Next 30 Years’, *Sens. Actuators B Chem.*, vol. 88, Issue 1, pp. 1-20, 2003, doi: 10.1016/S0925-4005(02)00301-5.

[66] M. M. Uzzal, P. Zarkesh-Ha, J. S. Edwards, E. Coelho, and P. Rawat, ‘A Highly Sensitive ISFET Using pH-to-Current Conversion for Real-Time DNA Sequencing’, in *2014 27th IEEE International System-on-Chip Conference (SOCC)*, Las Vegas, NV, USA: IEEE, Sep. 2014, pp. 410–414. doi: 10.1109/SOCC.2014.6948964.

[67] B. Premanode, W. P. Chan, and C. Toumazou, ‘Ultra-Low Power Precision ISFET Readout Using Global Current Feedback’, *Electron. Lett.*, vol. 42, no. 22, p. 1264, 2006, doi: 10.1049/el:20061690.

[68] D. Ma, P. Georgiou, and C. Toumazou, ‘A Weak Inversion ISFET Current Mirror for Differential Bio-Sensing’, in *2016 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Shanghai, China: IEEE, Oct. 2016, pp. 42–45. doi: 10.1109/BioCAS.2016.7833720.

[69] L. M. Shepherd and C. Toumazou, ‘A Biochemical Translinear Principle with Weak Inversion ISFETs’, *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 52, no. 12, pp. 2614–2619, Dec. 2005, doi: 10.1109/TCSI.2005.857919.

[70] G. Nabovati, E. Ghafar-Zadeh, and M. Sawan, ‘A 64-Pixel ISFET Based Biosensor for Extracellular pH Gradient Monitoring’, in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, Portugal: IEEE, May 2015, pp. 1762–1765. doi: 10.1109/ISCAS.2015.7168995.

[71] Y. Liu, A. Al-Ahdal, P. Georgiou, and C. Toumazou, ‘Minimal Readout Scheme for ISFET Sensing Arrays Based on Pulse Width Modulation’, *Electron. Lett.*, vol. 48, no. 10, p. 548, 2012, doi: 10.1049/el.2011.3847.

[72] N. Moser, T. S. Lande, and P. Georgiou, ‘A Novel pH-to-Time ISFET Pixel Architecture with Offset Compensation’, in *2015 IEEE International Symposium*

on Circuits and Systems (ISCAS), Lisbon, Portugal: IEEE, May 2015, pp. 481–484. doi: 10.1109/ISCAS.2015.7168675.

[73] A. T. Do, J. Minkyu, and K. S. Yeo, 'Improved Inverter-Based Read-Out Scheme for Low-Power ISFET Sensing Array', *Electron. Lett.*, vol. 49, no. 24, pp. 1517–1518, Nov. 2013, doi: 10.1049/el.2013.3025.

[74] R. W. Rochelle, 'Pulse-Frequency Modulation', *IRE Trans. Space Electron. Telem.*, vol. SET-8, no. 2, pp. 107–111, 1962, doi: 10.1109/IRET-SET.1962.5008816.

[75] A. E. Ross, 'Theoretical Study of Pulse-Frequency Modulation', *Proc. IRE*, vol. 37, no. 11, pp. 1277–1286, Nov. 1949, doi: 10.1109/JRPROC.1949.229667.

[76] V. Nerubatskyi, O. Plakhtii, and D. Hordiienko, 'Efficiency Analysis of DC-DC Converter with Pulse-Width and Pulse-Frequency Modulation', in *2022 IEEE 41st International Conference on Electronics and Nanotechnology (ELNANO)*, Kyiv, Ukraine: IEEE, Oct. 2022, pp. 571–575. doi: 10.1109/ELNANO54667.2022.9926762.

[77] C.-F. Chang and M. S.-C. Lu, 'CMOS Ion Sensitive Field Effect Transistors for Highly Sensitive Detection of DNA Hybridization', *IEEE Sens. J.*, vol. 20, no. 16, pp. 8930–8937, Aug. 2020, doi: 10.1109/JSEN.2020.2986461.

[78] P. Tripathi, N. Moser, and P. Georgiou, 'A Neuron-Based ISFET Array Architecture with Spatial Sensor Compensation', in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan: IEEE, May 2019, pp. 1–5. doi: 10.1109/ISCAS.2019.8702711.

[79] P. Zarkesh-Ha, J. Edwards, and P. Szauter, 'Avalanche ISFET: A Highly Sensitive pH Sensor for Genome Sequencing', in *2015 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Atlanta, GA, USA: IEEE, Oct. 2015, pp. 1–4. doi: 10.1109/BioCAS.2015.7348335.

[80] M. Douthwaite, E. Koutsos, D. C. Yates, P. D. Mitcheson, and P. Georgiou, 'A Thermally Powered ISFET Array for On-Body pH Measurement', *IEEE Trans. Biomed. Circuits Syst.*, vol. 11, no. 6, pp. 1324–1334, Dec. 2017, doi: 10.1109/TBCAS.2017.2727219.

[81] C. Lee, Y.-W. Chen, and M. S.-C. Lu, ‘CMOS Biosensors for the Detection of DNA Hybridization in High Ionic-Strength Solutions’, *IEEE Sens. J.*, vol. 21, no. 4, pp. 4135–4142, Feb. 2021, doi: 10.1109/JSEN.2020.3031321.

[82] S. Aslanzadeh, A. Hedayatipour, S. H. Hesari, and N. McFarlane, ‘A Low-Power Voltage-Clamped CMOS pH to Frequency Sensor’, in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan: IEEE, May 2019, pp. 1–5. doi: 10.1109/ISCAS.2019.8702619.

[83] H.-H. Liao, H.-H. Tsai, Y.-Z. Juang, R.-L. Wang, C.-C. Fu, and C. Yu, ‘ISFET with Built-in Gold Electrode and Readout Circuit with Frequency-Adjustable Pulse Output’, in *2013 Seventh International Conference on Sensing Technology (ICST)*, Wellington, New Zealand: IEEE, Dec. 2013, pp. 457–460. doi: 10.1109/ICSensT.2013.6727695.

[84] K. Hu, X. Lian, S. Dai, and J. K. Rosenstein, ‘Low Noise CMOS ISFETs Using In-Pixel Chopping’, in *2019 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Nara, Japan: IEEE, Oct. 2019, pp. 1–4. doi: 10.1109/BIOCAS.2019.8919025.

[85] M. Shojaei Baghini, A. Vilouras, M. Douthwaite, P. Georgiou, and R. Dahiya, ‘Ultra-Thin ISFET-Based Sensing Systems’, *Electrochem. Sci. Adv.*, vol. 2, no. 6, p. e2100202, Dec. 2022, doi: 10.1002/elsa.202100202.

[86] M. Cacho-Soblechero, K. Malpartida-Cardenas, N. Moser, and P. Georgiou, ‘Programmable Ion-Sensing Using Oscillator-Based ISFET Architectures’, *IEEE Sens. J.*, vol. 19, no. 19, pp. 8563–8575, Oct. 2019, doi: 10.1109/JSEN.2019.2921728.

[87] Feng Tan, Xianhe Huang, Wei Wei, and Wei Fu, ‘Analysis of Phase Noise and Timing Jitter in Crystal Oscillator’, in *2007 International Conference on Communications, Circuits and Systems*, Kokura: IEEE, Jul. 2007, pp. 1103–1106. doi: 10.1109/ICCCAS.2007.4348239.

[88] M. Mehri, S. Heidari, and N. Masoumi, ‘The Estimation of EMI-Induced Phase Noise and Jitter on Oscillator/Clock Signals’, in *2017 IEEE 21st Workshop on Signal and Power Integrity (SPI)*, Lake Maggiore, Italy: IEEE, May 2017, pp. 1–4. doi: 10.1109/SaPIW.2017.7944039.

[89] M.-N. Niu, X.-F. Ding, and Q.-Y. Tong, ‘Effect of Two Types of Surface Sites on the Characteristics of Si_3N_4-Gate pH-ISFET’s’, *Sens. Actuators B Chem.*, vol. 37, pp. 13-17, Nov. 1996, doi: 10.1016/S0925-4005(97)80067-6 .

[90] B. Palán, F. V. Santos, J. M. Karam, B. Courtois, and M. Husák, ‘New ISFET Sensor Interface Circuit for Biomedical Applications’, *Sens. Actuators B Chem.*, vol. 57, no. 1–3, pp. 63–68, Sep. 1999, doi: 10.1016/S0925-4005(99)00136-7.

[91] A. M. Dinar, A. M. Zain, and F. Salehuddin, ‘Utilizing of CMOS ISFET Sensors in DNA Applications Detection: A Systematic Review’, *Control Syst.*, vol. 10, 2018.

[92] S.-R. Chang and H. Chen, ‘A CMOS-Compatible, Low-Noise ISFET Based on High Efficiency Ion-Modulated Lateral-Bipolar Conduction’, *Sensors*, vol. 9, no. 10, pp. 8336–8348, Oct. 2009, doi: 10.3390/s91008336.

[93] Y. Hu, N. Moser, and P. Georgiou, ‘A 32 x 32 ISFET Chemical Sensing Array With Integrated Trapped Charge and Gain Compensation’, *IEEE Sens. J.*, vol. 17, no. 16, pp. 5276–5284, Aug. 2017, doi: 10.1109/JSEN.2017.2722043.

[94] C. Panteli, P. Georgiou, and K. Fobelets, ‘Performance Improvement of Commercial ISFET Sensors Using Reactive Ion Etching’, *Microelectron. Eng.*, vol. 192, pp. 61–65, May 2018, doi: 10.1016/j.mee.2018.02.004.

[95] P. A. Hammond, D. Ali, and D. R. S. Cumming, ‘Design of a Single-Chip pH Sensor Using a Conventional 0.6 -μm CMOS Process’, *IEEE Sens. J.*, vol. 4, no. 6, pp. 706–712, Dec. 2004, doi: 10.1109/JSEN.2004.836849.

[96] V. P. Chodavarapu, A. H. Titus, and A. N. Cartwright, ‘Differential Read-Out Architecture for CMOS ISFET Microsystems’, *Electron. Lett.*, vol. 41, no. 12, p. 698, 2005, doi: 10.1049/el:20051044.

[97] M. S. A. Shawkat and N. McFarlane, ‘A Single-Chip ISFET Based pH Sensor’, in *2016 IEEE SENSORS*, Orlando, FL, USA: IEEE, Oct. 2016, pp. 1–3. doi: 10.1109/ICSENS.2016.7808833.

[98] B. Ozansoy Kasap, S. V. Marchenko, O. O. Soldatkin, S. V. Dzyadevych, and B. Akata Kurc, ‘Biosensors Based on Nano-Gold/Zeolite-Modified Ion Selective Field-Effect Transistors for Creatinine Detection’, *Nanoscale Res. Lett.*, vol. 12, no. 1, p. 162, Dec. 2017, doi: 10.1186/s11671-017-1943-x.

[99] V. P. Chodavarapu, A. H. Titus, and A. N. Cartwright, ‘CMOS ISFET Microsystem for Biomedical Applications’, in *IEEE Sensors, 2005.*, Irvine, CA, USA: IEEE, 2005, pp. 109–112. doi: 10.1109/ICSENS.2005.1597648.

[100] M. J. Milgrew, P. A. Hammond, and D. R. S. Cumming, ‘The Development of Scalable Sensor Arrays Using Standard CMOS Technology’, *Sens. Actuators B Chem.*, vol. 103, no. 1–2, pp. 37–42, Sep. 2004, doi: 10.1016/j.snb.2004.03.004.

[101] Y. Hu and P. Georgiou, ‘3-T ISFET Front-End Utilising Parasitic Device Capacitance’, *Electron. Lett.*, vol. 50, no. 21, pp. 1507–1509, Oct. 2014, doi: 10.1049/el.2014.2488.

[102] L. Yang, X. Zhang, Q. Zhang, M. Tan, and Y. Yu, ‘A High-Speed Small-Area Pixel 16 × 16 ISFET Array Design Using 0.35-μm CMOS Process’, *Microelectron. J.*, vol. 79, pp. 107–112, Sep. 2018, doi: 10.1016/j.mejo.2018.03.003.

[103] W. P. Chan, B. Premanode, and C. Toumazou, ‘An Integrated ISFETs Instrumentation System in Standard CMOS Technology’, *IEEE J. Solid-State Circuits*, vol. 45, no. 9, pp. 1923–1934, Sep. 2010, doi: 10.1109/JSSC.2010.2053863.

[104] K. Nakazato, ‘An Integrated ISFET Sensor Array’, *Sensors*, vol. 9, no. 11, pp. 8831–8851, Nov. 2009, doi: 10.3390/s91108831.

[105] Y.-H. Lin, C.-P. Chu, C.-F. Lin, H.-H. Liao, H.-H. Tsai, and Y.-Z. Juang, ‘Extended-Gate Field-Effect Transistor Packed in Micro Channel for Glucose, Urea and Protein Biomarker Detection’, *Biomed. Microdevices*, vol. 17, no. 6, p. 111, Dec. 2015, doi: 10.1007/s10544-015-0020-4.

[106] R.-L. Wang *et al.*, ‘CMOS Pulse-Width-Modulation Readout Circuit with a Wide Modulation Range for Ion-Sensitive FET-Based Sensors’, *Jpn. J. Appl. Phys.*, vol. 54, no. 4S, p. 04DL02, Apr. 2015, doi: 10.7567/JJAP.54.04DL02.

[107] Y.-Z. Juang *et al.*, ‘A Fully Compatible CMOS-Based Hydrogen Ion Sensor Using Natural Forming Sensing Membrane for Urea Detecting Application’, *Procedia Chem.*, vol. 1, no. 1, pp. 1067–1070, Sep. 2009, doi: 10.1016/j.proche.2009.07.266.

[108] A. Ganguli, Y. Watanabe, M. T. Hwang, J.-C. Huang, and R. Bashir, ‘Robust Label-Free microRNA Detection Using One Million ISFET Array’, *Biomed. Microdevices*, vol. 20, no. 2, p. 45, Jun. 2018, doi: 10.1007/s10544-018-0290-8.

[109] C. Duarte-Guevara *et al.*, ‘On-Chip Metal/Polypyrrole Quasi-reference Electrodes for Robust ISFET Operation’, *The Analyst*, vol. 140, no. 10, pp. 3630–3641, 2015, doi: 10.1039/C5AN00085H.

[110] M. S. Andrianova, E. V. Kuznetsov, V. P. Grudtsov, and A. E. Kuznetsov, ‘CMOS-Compatible Biosensor for L-carnitine Detection’, *Biosens. Bioelectron.*, vol. 119, pp. 48–54, Nov. 2018, doi: 10.1016/j.bios.2018.07.044.

[111] C. G. Jakobson, U. Dinnar, M. Feinsod, and Y. Nemirovsky, ‘Ion-Sensitive Field-Effect Transistors in Standard CMOS Fabricated by Post-Processing’, *IEEE Sens. J.*, vol. 2, no. 4, pp. 279–287, Aug. 2002, doi: 10.1109/JSEN.2002.802237.

[112] Haigang Yang *et al.*, ‘pH-ISFET Based Micro Sensor System on Chip Using Standard CMOS Technology’, in *Fifth International Workshop on System-on-Chip for Real-Time Applications (IWSOC’05)*, Banff, Alta., Canada: IEEE, 2005, pp. 180–183. doi: 10.1109/IWSOC.2005.21.

[113] J. Wei, H. Yang, H. Sun, Z. Lin, and S. Xia, ‘A Fully CMOS-Integrated pH-ISFET Interface Circuit’, in *2005 6th International Conference on ASIC*, Shanghai, China: IEEE, 2005, pp. 414–416. doi: 10.1109/ICASIC.2005.1611338. [114] Y.-L. Chin, J.-C. Chou, Z.-C. Lei, T.-P. Sun, W.-Y. Chung, and S.-K. Hsiung, ‘Titanium Nitride Membrane Application to Extended Gate Field Effect Transistor pH Sensor Using VLSI Technology’, *Jpn. J. Appl. Phys.*, vol. 40, no. Part 1, No. 11, pp. 6311–6315, Nov. 2001, doi: 10.1143/JJAP.40.6311.

[115] P.-Y. Kuo, Y.-Y. Chen, W.-H. Lai, and C.-H. Chang, ‘Analysis of CMOS Extended-Gate Field-Effect Transistor With On-Chip Window Based on Uricase/RuO_2 Sensing Film’, *IEEE J. Electron Devices Soc.*, vol. 9, pp. 995–1002, 2021, doi: 10.1109/JEDS.2021.3120759.

[116] B. C. Cheah *et al.*, ‘An Integrated Circuit for Chip-Based Analysis of Enzyme Kinetics and Metabolite Quantification’, *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 3, pp. 721–730, Jun. 2016, doi: 10.1109/TBCAS.2015.2487603.

[117] H. Guliga, W. F. H. Abdullah, and S. H. Herman, ‘Extended-Gate Field-Effect Transistor (EGFET) Integrated Readout Interfacing Circuit for pH Sensing ’, in *2014 2nd International Conference on Electrical, Electronics and System Engineering (ICEESE)*, Kuala Lumpur: IEEE, Dec. 2014, pp. 11–14. doi: 10.1109/ICEESE.2014.7154605.

[118] B. A. McKinley, ‘ISFET and Fiber Optic Sensor Technologies: In Vivo Experience for Critical Care Monitoring’, *Chem. Rev.*, vol. 108, no. 2, pp. 826–844, Feb. 2008, doi: 10.1021/cr068120y.

[119] K.-Y. Park, S.-B. Choi, M. Lee, B.-K. Sohn, and S.-Y. Choi, ‘ISFET Glucose Sensor System with Fast Recovery Characteristics by Employing Electrolysis’, *Sens. Actuators B Chem.*, vol. 83, no. 1–3, pp. 90–97, Mar. 2002, doi: 10.1016/S0925-4005(01)01049-8.

[120] D.-C. Li, P.-H. Yang, and M. S.-C. Lu, ‘CMOS Open-Gate Ion-Sensitive Field-Effect Transistors for Ultrasensitive Dopamine Detection’, *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2761–2767, Oct. 2010, doi: 10.1109/TED.2010.2063330.

[121] M. Cacho-Soblechero, K. Malpartida-Cardenas, C. Cicatiello, J. Rodriguez-Manzano, and P. Georgiou, ‘A Dual-Sensing Thermo-Chemical ISFET Array for DNA-Based Diagnostics’, *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 3, pp. 477–489, Jun. 2020, doi: 10.1109/TBCAS.2020.2978000.

[122] C. Hu, M. A. Al-Rawhani, B. C. Cheah, S. Velugotla, and D. R. S. Cumming, ‘Hybrid Dual Mode Sensor for Simultaneous Detection of Two Serum Metabolites’, *IEEE Sens. J.*, vol. 18, no. 2, pp. 484–493, Jan. 2018, doi: 10.1109/JSEN.2017.2774359.

[123] J. Broomfield *et al.*, ‘Detection of YAP1 and AR-V7 mRNA for Prostate Cancer Prognosis Using an ISFET Lab-On-Chip Platform’, *ACS Sens.*, vol. 7, no. 11, pp. 3389–3398, Nov. 2022, doi: 10.1021/acssensors.2c01463.

[124] G. Alexandrou *et al.*, ‘Detection of Multiple Breast Cancer *ESR1* Mutations on an ISFET Based Lab-on-Chip Platform’, *IEEE Trans. Biomed. Circuits Syst.*, vol. 15, no. 3, pp. 380–389, Jun. 2021, doi: 10.1109/TBCAS.2021.3094464.

[125] J. Zeng, L. Kuang, N. Miscourides, and P. Georgiou, ‘A 128 × 128 Current-Mode Ultra-High Frame Rate ISFET Array With In-Pixel Calibration for Real-Time Ion Imaging’, *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 2, pp. 359–372, Apr. 2020, doi: 10.1109/TBCAS.2020.2973508.

[126] P. Shields, B. Nemeth, R. B. Green, M. O. Riehle, and D. R. S. Cumming, ‘High-Speed Imaging of 2-D Ionic Diffusion Using a 16 x 16 Pixel CMOS

ISFET Array on the Microfluidic Scale', *IEEE Sens. J.*, vol. 12, no. 9, pp. 2744–2749, Sep. 2012, doi: 10.1109/JSEN.2012.2200249.

[127] Y. Imaizumi, T. Goda, A. Matsumoto, and Y. Miyahara, 'Identification of Types of Membrane Injuries and Cell Death Using Whole Cell-Based Proton-Sensitive Field-Effect Transistor Systems', *The Analyst*, vol. 142, no. 18, pp. 3451–3458, 2017, doi: 10.1039/C7AN00502D.

[128] Y. Hong, S.-O. Chung, J. Park, and Y. Hong, 'Portable Soil pH Sensor Using ISFET Electrode', *J. Inf. Commun. Converg. Eng.*, vol. 20, no. 1, pp. 49–57, Mar. 2022, doi: 10.6109/JICCE.2022.20.1.49.

[129] M. Joly, L. Mazenq, M. Marlet, P. Temple-Boyer, C. Durieu, and J. Launay, 'Multimodal Probe Based on ISFET Electrochemical Microsensors for In-Situ Monitoring of Soil Nutrients in Agriculture', in *Proceedings of Eurosensors 2017, Paris, France, 3–6 September 2017*, MDPI, Aug. 2017, p. 420. doi: 10.3390/proceedings1040420.

[130] D. Y. Chen and P. K. Chan, 'An Intelligent ISFET Sensory System with Temperature and Drift Compensation for Long-Term Monitoring', *IEEE Sens. J.*, vol. 8, no. 12, pp. 1948–1959, Dec. 2008, doi: 10.1109/JSEN.2008.2006471.

[131] P. Whig and S. N. Ahmad, 'On the Performance of ISFET-based Device for Water Quality Monitoring', *Int. J. Commun. Netw. Syst. Sci.*, vol. 04, no. 11, pp. 709–719, 2011, doi: 10.4236/ijcns.2011.411087.

[132] J. Orozco, A. Baldi, P. L. Martín, A. Bratov, and C. Jiménez, 'Monitoring of Bentonite Pore Water with a Probe Based on Solid-State Microsensors', *Anal. Chim. Acta*, vol. 579, no. 1, pp. 95–101, Oct. 2006, doi: 10.1016/j.aca.2006.07.030.

[133] C. Jimenez-Jorquera, J. Orozco, and A. Baldi, 'ISFET Based Microsensors for Environmental Monitoring', *Sensors*, vol. 10, no. 1, pp. 61–83, Dec. 2009, doi: 10.3390/s100100061.

[134] J. Alonso, 'Analysis and Identification of Several Apple Varieties Using ISFETs Sensors ', *Talanta*, vol. 59, no. 6, pp. 1245–1252, May 2003, doi: 10.1016/S0039-9140(03)00028-6.

[135] N. Houngkamhang and P. Phasukkit, ‘Portable Deep Learning-Driven Ion-Sensitive Field-Effect Transistor Scheme for Measurement of Carbaryl Pesticide’, *Sensors*, vol. 22, no. 9, p. 3543, May 2022, doi: 10.3390/s22093543.

[136] A. Kuznetsov, M. Andrianova, N. Komarova, V. Grudtsov, E. Kuznetsov, and A. Saurov, ‘Detection of Aroma Compound by ISFET Modified with Aptamer’, in *2017 2nd International Conference on Bio-engineering for Smart Technologies (BioSMART)*, Paris: IEEE, Aug. 2017, pp. 1–3. doi: 10.1109/BIOSMART.2017.8095326.

[137] Y. Jiang *et al.*, ‘A High-Sensitivity Potentiometric 65-nm CMOS ISFET Sensor for Rapid E. coli Screening’, *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 2, pp. 402–415, Apr. 2018, doi: 10.1109/TBCAS.2018.2793861.

[138] L. Campanella, C. Colapicchioni, M. Tomassetti, A. Bianco, and S. Dezzi, ‘A New ISFET Device for Cocaine Analysis’, *Sens. Actuators B Chem.*, vol. 24, no. 1–3, pp. 188–193, Mar. 1995, doi: 10.1016/0925-4005(95)85040-6.

[139] Y. Su, M. Tomassetti, M. P. Sammartino, G. Crescentini, and L. Campanella, ‘A New Salicylate ISFET for the Determination of Salicylic and Acetylsalicylic Acid in Drugs’, *J. Pharm. Biomed. Anal.*, vol. 13, no. 4–5, pp. 449–457, Apr. 1995, doi: 10.1016/0731-7085(95)01320-K.

[140] M. Kalofonou, P. Georgiou, C.-P. Ou, and C. Toumazou, ‘An ISFET Based Translinear Sensor for DNA Methylation Detection’, *Sens. Actuators B Chem.*, vol. 161, no. 1, pp. 156–162, Jan. 2012, doi: 10.1016/j.snb.2011.09.089.

[141] D. Ma, J. Rodriguez-Manzano, S. de Mateo Lopez, M. Kalofonou, P. Georgiou, and C. Toumazou, ‘Adapting ISFETs for Epigenetics: An Overview’, *IEEE Trans. Biomed. Circuits Syst.*, vol. 12, no. 5, pp. 1186–1201, Oct. 2018, doi: 10.1109/TBCAS.2018.2838153.

[142] D. G. Chen, D. Matolin, A. Bermak, and C. Posch, ‘Pulse-Modulation Imaging—Review and Performance Analysis’, *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 1, pp. 64–82, Feb. 2011, doi: 10.1109/TBCAS.2010.2075929.

[143] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 3rd ed. in The Oxford series in electrical and computer engineering. New York ; Oxford: Oxford University Press, USA, 2012.

[144] D.-H. Kwon, ‘Effects of Heat Treatment on Ta_2O_5 Sensing Membrane for Low Drift and High Sensitivity pH-ISFET’, *Sens. Actuators B Chem.*, vol. 34, Issues 1-3, pp. 441-445, 1996, doi: 10.1016/S0925-4005(96)01938-7.

[145] A. M. Dinar, A. S. M. Zain, and F. Salehuddin, ‘Comprehensive Identification of Sensitive and Stable ISFET Sensing Layer High-k Gate Based on ISFET/Electrolyte Models’, *Int. J. Electr. Comput. Eng. IJECE*, vol. 9, no. 2, p. 926, Apr. 2019, doi: 10.11591/ijece.v9i2.pp926-933.

[146] B. Tordoff *et al.*, ‘The LaserFIB: New Application Opportunities Combining a High-Performance FIB-SEM with Femtosecond Laser Processing in an Integrated Second Chamber’, *Appl. Microsc.*, vol. 50, no. 1, p. 24, Dec. 2020, doi: 10.1186/s42649-020-00044-5.

[147] E. S. Kim *et al.*, ‘Facile Fabrication of Micro/Nano-Structured Wrinkles by Controlling Elastic Properties of Polydimethylsiloxane Substrates’, *Polymer*, vol. 212, p. 123087, Jan. 2021, doi: 10.1016/j.polymer.2020.123087.

[148] M. F. Hayles and D. A. M. De Winter, ‘An Introduction to Cryo-FIB-SEM Cross-Sectioning of Frozen, Hydrated Life Science Samples’, *J. Microsc.*, vol. 281, no. 2, pp. 138–156, Feb. 2021, doi: 10.1111/jmi.12951.

[149] T. Zachs *et al.*, ‘Fully Automated, Sequential Focused Ion Beam Milling for Cryo-Electron Tomography’, *eLife*, vol. 9, p. e52286, Mar. 2020, doi: 10.7554/eLife.52286.

[150] L. J. Allen, A. J. D’Alfonso, B. Freitag, and D. O. Klenov, ‘Chemical Mapping at Atomic Resolution Using Energy-Dispersive X-ray Spectroscopy’, *MRS Bull.*, vol. 37, no. 1, pp. 47–52, Jan. 2012, doi: 10.1557/mrs.2011.331.

[151] S. Kumar, K. Rechav, I. Kaplan-Ashiri, and A. Gal, ‘Imaging and Quantifying Homeostatic Levels of Intracellular Silicon in Diatoms’, *Sci. Adv.*, vol. 6, no. 42, p. eaaz7554, Oct. 2020, doi: 10.1126/sciadv.aaz7554.

[152] C.-E. Lue, T.-C. Yu, C.-M. Yang, D. G. Pijanowska, and C.-S. Lai, ‘Optimization of Urea-EnFET Based on Ta2O5 Layer with Post Annealing’, *Sensors*, vol. 11, no. 5, pp. 4562–4571, Apr. 2011, doi: 10.3390/s110504562.

[153] H.-J. Jang and W.-J. Cho, ‘High-Performance Silicon-on-Insulator Based Ion-Sensitive Field-Effect Transistor Using High-k Stacked Oxide Sensing Membrane’, *Appl. Phys. Lett.*, vol. 99, no. 4, p. 043703, Jul. 2011, doi: 10.1063/1.3619831.

[154] A. Tsiamis *et al.*, ‘Comparison of Conventional and Maskless Lithographic Techniques for More than Moore Post-Processing of Foundry CMOS Chips’, *J. Microelectromechanical Syst.*, vol. 29, no. 5, pp. 1245–1252, Oct. 2020, doi: 10.1109/JMEMS.2020.3015964.

[155] I. V. Tudose *et al.*, ‘Chemical and Physical Methods for Multifunctional Nanostructured Interface Fabrication’, in *Functional Nanostructured Interfaces for Environmental and Biomedical Applications*, Elsevier, 2019, pp. 15–26. doi: 10.1016/B978-0-12-814401-5.00002-5.

[156] V. K. Khanna, ‘Fabrication of ISFET Microsensor by Diffusion-Based Al Gate NMOS Process and Determination of its pH Sensitivity from Transfer Characteristics’, *APPL PHYS*, vol. 50, p. 9, 2012.

[157] T.-M. Pan, C.-H. Cheng, and C.-D. Lee, ‘Yb2O3 Thin Films as a Sensing Membrane for pH-ISFET Application’, *J. Electrochem. Soc.*, p. 5.

[158] S. J. Wu, B. Houng, and B. Huang, ‘Effect of Growth and Annealing Temperatures on Crystallization of Tantalum Pentoxide Thin Film Prepared by RF Magnetron Sputtering Method’, *J. Alloys Compd.*, vol. 475, no. 1–2, pp. 488–493, May 2009, doi: 10.1016/j.jallcom.2008.07.126.

[159] T. Mikolajick, R. Kühnhold, and H. Ryssel, ‘The pH-Sensing Properties of Tantalum Pentoxide Films Fabricated by Metal Organic Low-Pressure Chemical Vapor Deposition’, *Sens. Actuators B Chem.*, vol. 44, no. 1–3, pp. 262–267, Oct. 1997, doi: 10.1016/S0925-4005(97)00166-4.

[160] S. J. Darghlou, H. kangarlou, and V. razzazi, ‘Effect of Vertical Deposition Angle on Structural and Optical Properties of Tantalum Oxide Nano Layers Deposited by Electron Gun Evaporation’, *Chin. J. Phys.*, vol. 74, pp. 226–238, Dec. 2021, doi: 10.1016/j.cjph.2021.09.008.

[161] U. Buder, J.-P. von Klitzing, and E. Obermeier, ‘Reactive Ion Etching for Bulk Structuring of Polyimide’, *Sens. Actuators Phys.*, vol. 132, no. 1, pp. 393–399, Nov. 2006, doi: 10.1016/j.sna.2006.04.048.

[162] H. K. Lee, K. S. Chung, and J. S. Yu, ‘Selective Etching of Thick Si_3N_4, SiO_2 and Si by Using CF_4/O_2 and C_2F_6 Gases with or without O_2 or Ar Addition’, *J. Korean Phys. Soc.*, vol. 54, no. 5(1), pp. 1816–1823, May 2009, doi: 10.3938/jkps.54.1816.

[163] F.-L. Jin, X. Li, and S.-J. Park, ‘Synthesis and Application of Epoxy Resins: A Review’, *J. Ind. Eng. Chem.*, vol. 29, pp. 1–11, Sep. 2015, doi: 10.1016/j.jiec.2015.03.026.

[164] J. Xu, B. Ma, W. Mao, and X. Wang, ‘Strength Characteristics and Prediction of Epoxy Resin Pavement Mixture’, *Constr. Build. Mater.*, vol. 283, p. 122682, May 2021, doi: 10.1016/j.conbuildmat.2021.122682.

[165] L. Sudakov-Boreysha, A. Morgenshtein, U. Dinnar, and Y. Nemirovsky, ‘ISFET CMOS Compatible Design and Encapsulation Challenges’, in *Proceedings of the 2004 11th IEEE International Conference on Electronics, Circuits and Systems, 2004. ICECS 2004.*, Tel Aviv, Israel: IEEE, 2004, pp. 535–538. doi: 10.1109/ICECS.2004.1399736.

[166] E. O. Blair *et al.*, ‘Test Structures for the Characterisation of Sensor Packaging Technology’, in *2017 International Conference of Microelectronic Test Structures (ICMTS)*, Grenoble, France: IEEE, Mar. 2017, pp. 1–6. doi: 10.1109/ICMTS.2017.7954279.

[167] J. R. K. Marland *et al.*, ‘Real-Time Measurement of Tumour Hypoxia Using an Implantable Microfabricated Oxygen Sensor’, *Sens. Bio-Sens. Res.*, vol. 30, p. 100375, Dec. 2020, doi: 10.1016/j.sbsr.2020.100375.

[168] K. Hekmat, ‘Interference by Cellular Phones with Permanent Implanted Pacemakers: An Update’, *Europace*, vol. 6, no. 4, pp. 363–369, Jul. 2004, doi: 10.1016/j.eupc.2004.03.010.

[169] R. A. Stevenson, 'Design and application of broadband ceramic feedthrough capacitor EMI filters to cardiac pacemakers and implantable defibrillators,' *Proceedings of the 19th Annual International Conference of the IEEE Engineering in Medicine and Biology Society. 'Magnificent Milestones and Emerging Opportunities in Medical Engineering' (Cat. No.97CH36136)*, Chicago, IL, USA, 1997, pp. 2558-2562 vol.6, doi: 10.1109/IEMBS.1997.756852.

[170] G. Savadjiev, ‘Design and Fabrication of an Ion Sensitive Field Effect Transistor and Readout Circuit using a Commercial TSMC 65nm Process’, M. Eng Thesis, Department of Electrical and Computer Engineering, McGill University, Montreal, 2020, Available: https://escholarship.mcgill.ca/concern/theses/8c97kv817.

[171] S. H. Gerritsen *et al.*, ‘Surface Smoothing by Atomic Layer Deposition and Etching for the Fabrication of Nanodevices’, *ACS Appl. Nano Mater.*, vol. 5, no. 12, pp. 18116–18126, Dec. 2022, doi: 10.1021/acsanm.2c04025.

[172] C. Accarino *et al.*, ‘Noise Characteristics with CMOS Sensor Array Scaling’, *Measurement*, vol. 152, p. 107325, Feb. 2020, doi: 10.1016/j.measurement.2019.107325.

[173] S. B. Prakash and P. Abshire, ‘A Fully Differential Rail-to-Rail CMOS Capacitance Sensor With Floating-Gate Trimming for Mismatch Compensation’, *IEEE Trans. Circuits Syst. Regul. Pap.*, vol. 56, no. 5, pp. 975–986, May 2009, doi: 10.1109/TCSI.2009.2015202.

[174] E. Muller, P. Woias, P. Hein, and S. Koch, ‘Differential ISFET/REFET Pairs as a Reference System for Integrated ISFET-Sensor Arrays’, in *TRANSDUCERS ’91: 1991 International Conference on Solid-State Sensors and Actuators. Digest of Technical Papers*, San Francisco, CA, USA: IEEE, 1991, pp. 467–470. doi: 10.1109/SENSOR.1991.148913.

[175] A. Errachid, ‘A Simple REFET for pH Detection in Differential Mode’, *Sens. Actuators B Chem.*, vol. 60, no. 1, pp. 43–48, Nov. 1999, doi: 10.1016/S0925-4005(99)00242-7.

[176] M. Douthwaite, N. Moser, and P. Georgiou, ‘CMOS ISFET Arrays for Integrated Electrochemical Sensing and Imaging Applications: A Tutorial’, *IEEE Sens. J.*, vol. 21, no. 20, pp. 22155–22169, Oct. 2021, doi: 10.1109/JSEN.2021.3094206.

[177] J. Zhang, J. Wei, and H. Chen, ‘An Address Event Representation Circuits Design with Rotation Priority against Pulse Collision’, in *2019 IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC)*, Xi’an, China: IEEE, Jun. 2019, pp. 1–3. doi: 10.1109/EDSSC.2019.8754504.

[178] A. Linares-Barranco, M. Oster, D. Cascado, G. Jiménez, A. Civit, and B. Linares-Barranco, 'Inter-spike-intervals Analysis of Poisson Like Hardware Synthetic AER Generation.' in *Computational Intelligence and Bioinspired Systems*, vol. 3512, J. Cabestany, A. Prieto, and F. Sandoval, Eds. Lecture Notes in Computer Science, Berlin: Springer, 2005, pp. 502–508, doi: 10.1007/11494669_59

[179] N. Wu, ‘Neuromorphic Vision Chips’, *Sci. China Inf. Sci.*, vol. 61, no. 6, p. 060421, Jun. 2018, doi: 10.1007/s11432-017-9303-0.

[180] K. M. Monica, ‘Design and Study of System on Chip Design for Signal Processing Applications in Terms of Energy and Area’, *Mater. Today Proc.*, p. S221478532105080X, Jul. 2021, doi: 10.1016/j.matpr.2021.07.221.

[181] G. Xu, J. Abbott, and D. Ham, ‘Optimization of CMOS-ISFET-Based Biomolecular Sensing: Analysis and Demonstration in DNA Detection’, *IEEE Trans. Electron Devices*, pp. 1–8, 2016, doi: 10.1109/TED.2016.2582845.

Appendices

Appendix A. Chip Layouts

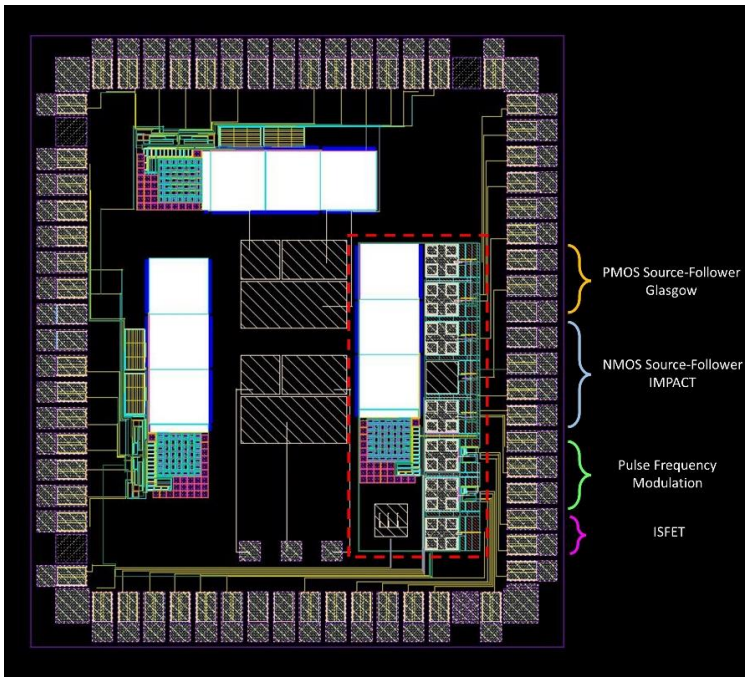


Figure A.1 Chip layout of first tape-out with the NPFM-V1 included.

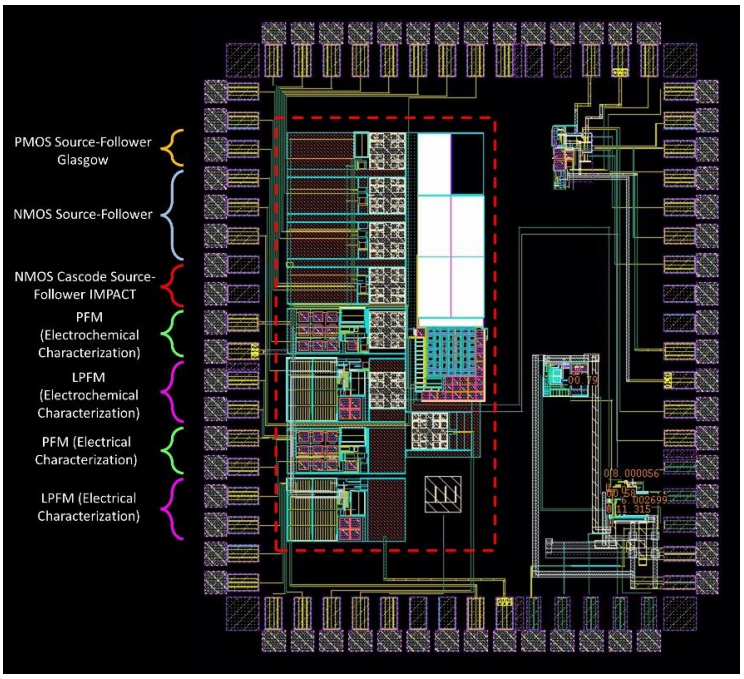
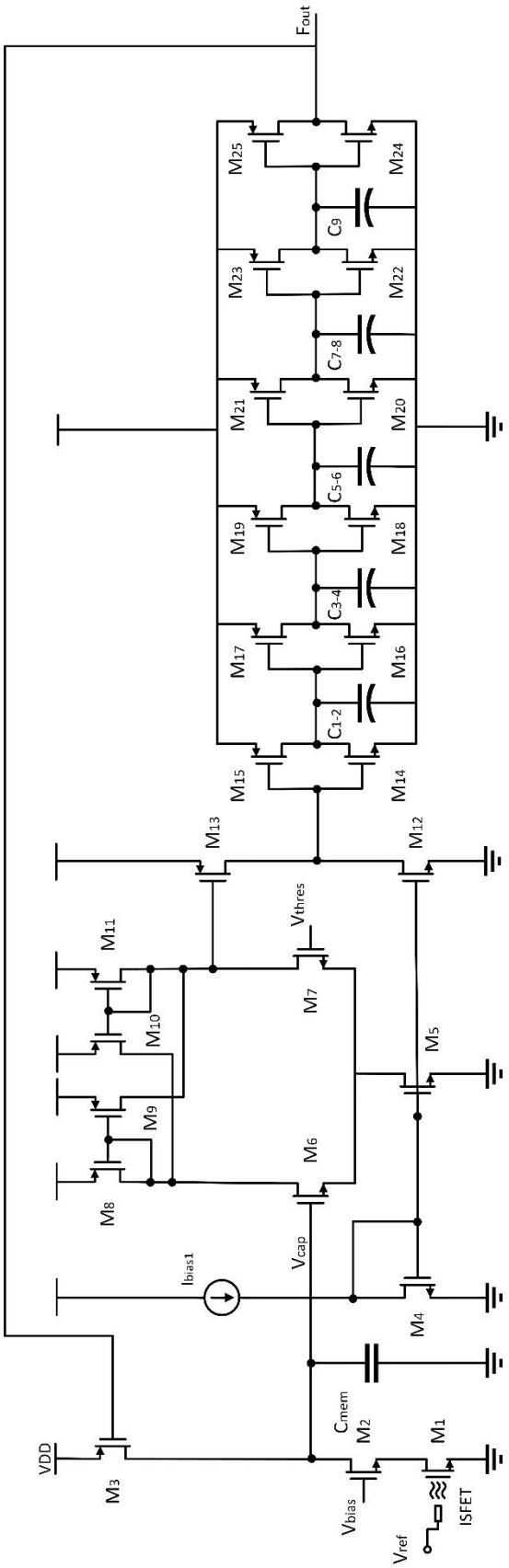


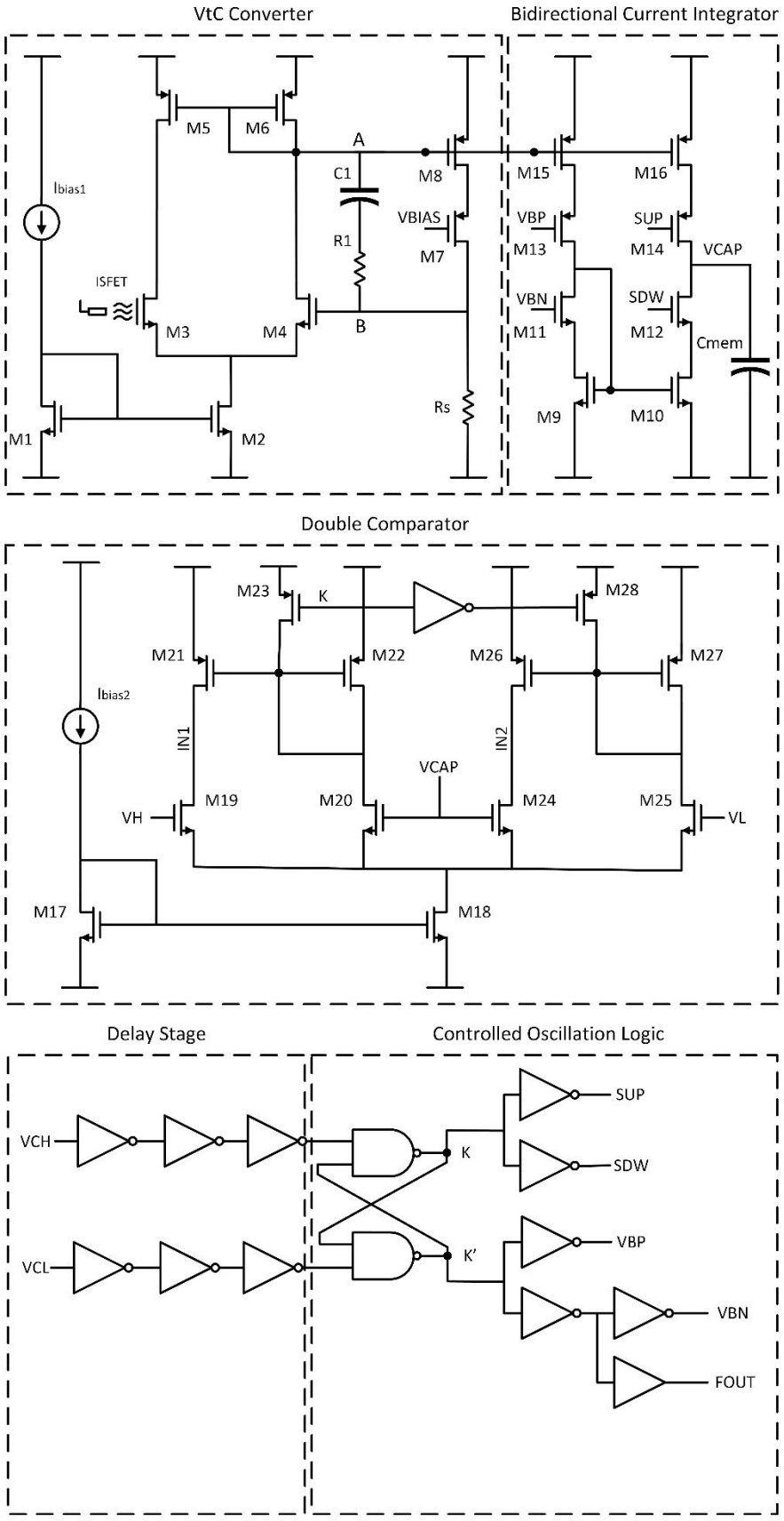
Figure A.2 Chip layout of second tape-out with improved NPFM-V2 and LFPM included.

Appendix B.1 Full View NPFM



Pulse Frequency Modulator									
Component	Aspect ratio/size	Component	Aspect ratio/size	Component	Aspect ratio/size	Component	Aspect ratio/size	Component	Aspect ratio/size
M1	0.5/19.995	M10/M11	10/0.5	M17	0.36/1	M23	0.36/1		
M2/M3	20/0.5	M12	10/0.5	M18	0.22/1	M24	0.22/1		
M4	40/0.5	M13	10/0.5	M19	0.36/1	M25	0.36/1		
M5	10/25	M14	0.22/1	M20	0.22/1	Cmem	1.5p		
M6/M7	10/0.5	M15	0.36/1	M21	0.36/1	C1-9	1.8p		
M8/M9	10/0.5	M16	0.22/1	M22	0.22/1				

Appendix B.2 Full View LPFM



Linear Pulse Frequency Modulator							
Component	Aspect ratio/size	Component	Aspect ratio/size	Component	Aspect ratio/size	Component	Aspect ratio/size
M1	10/1.2	M11/M12	1.65/1.2	M21/M22	20/2	C1	400f
M2	20/1.2	M13/M14	5/1.2	M23	8/1.2	R1	1.12k
M3/M4	1/1.2	M15/M16	5/1.2	M24/M25	20/1.2	Rs	19k
M5/M6	30/1.2	M17	10/1.2	M26/M27	20/2		
M7/M8	50/1.2	M18	40/1.2	M28	8/1.2		
M9/M10	1.65/1.2	M19/M20	20/1.2	Cmem	7.16p		

Appendix C. Experimental Setup

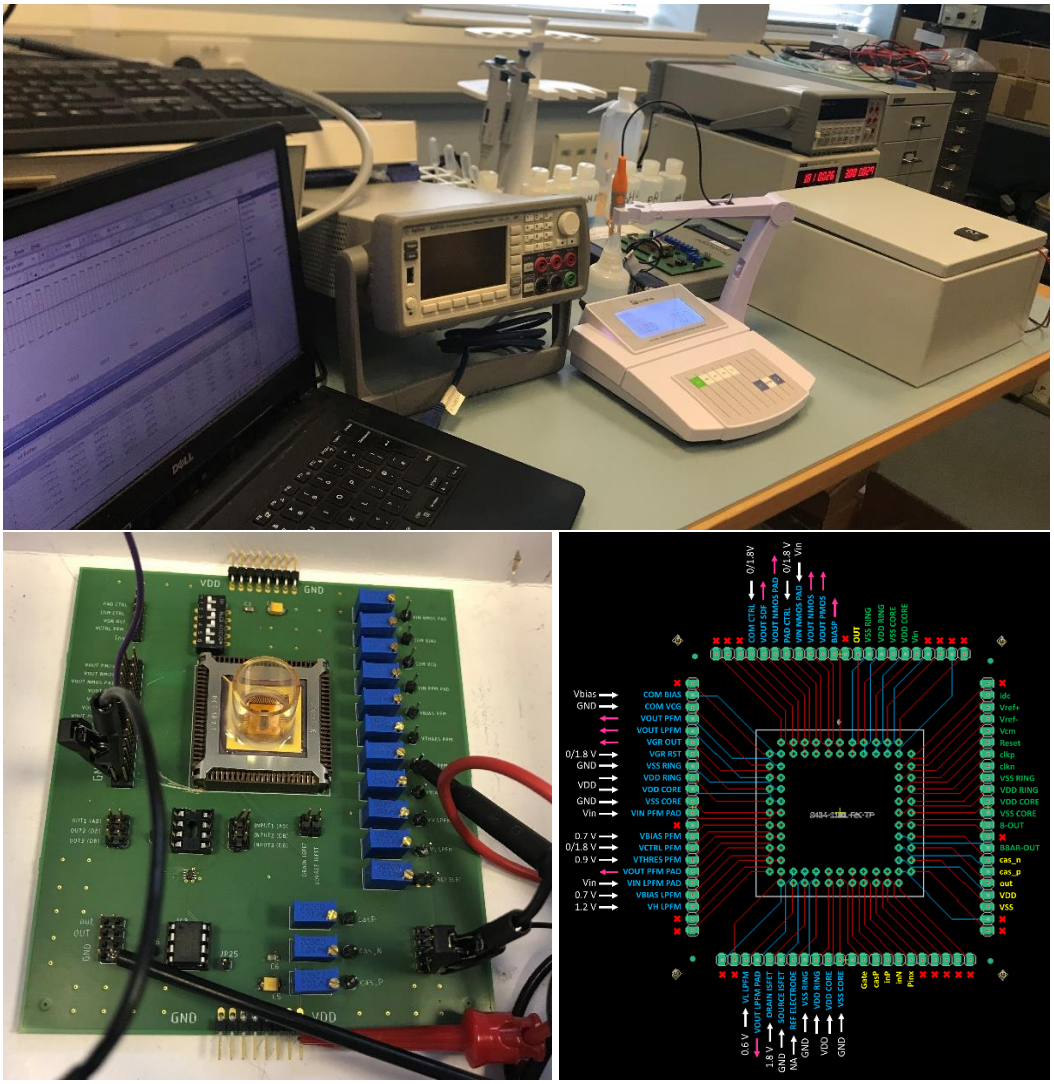


Figure C Experimental setup, which includes a power supply, signal generator, custom PCB inside a Faraday cage, Picoscope, pH meter and a computer for data acquisition.

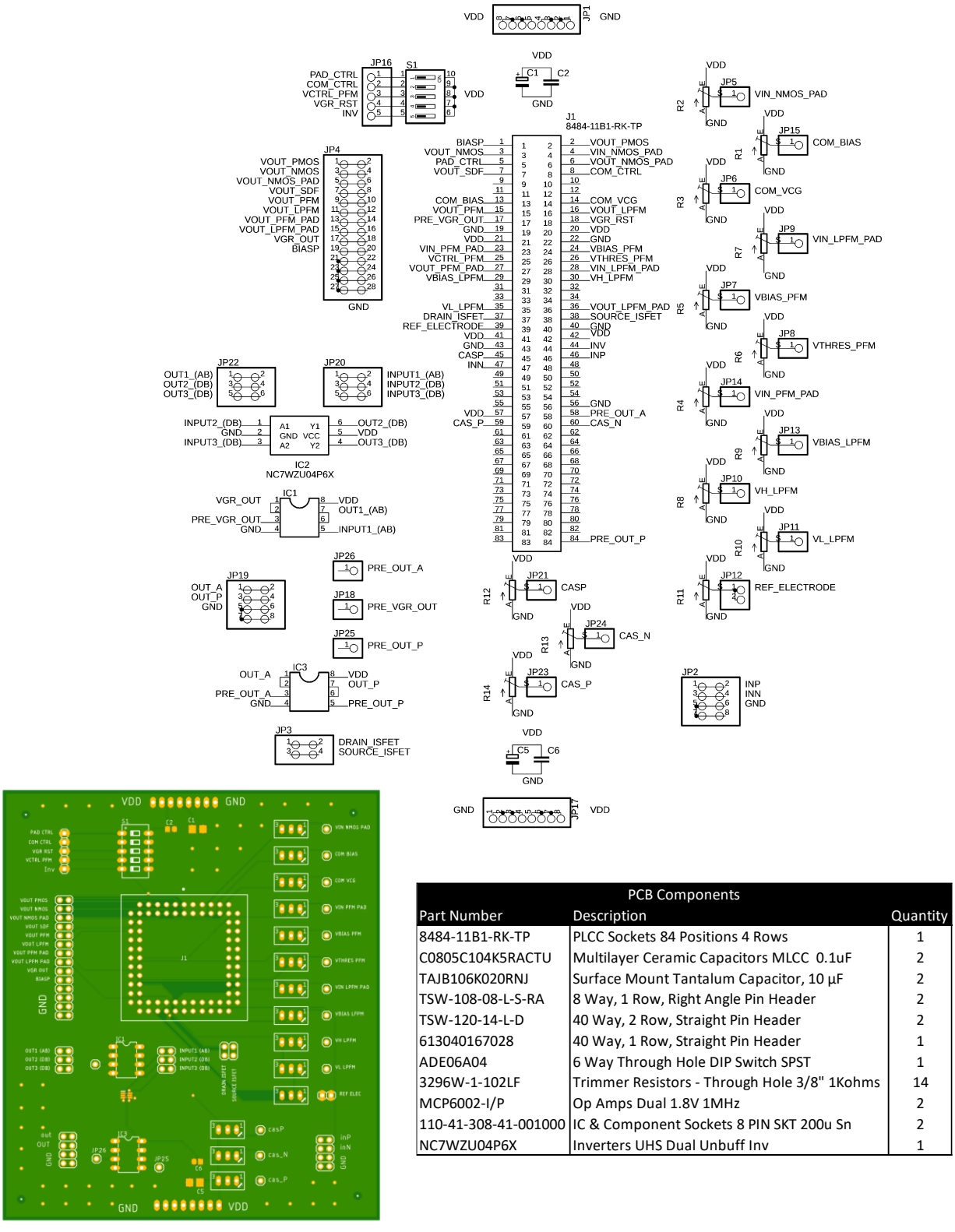
The custom PCB allows for the control of all the independent voltage inputs using potentiometers with just one power supply. It also includes signal processing and control switches for on-chip or off-chip input variables. The same PCB was used for electrical and electrochemical characterisation. The difference is that a chamber was incorporated on top of some CMOS chips for putting the solution in while taking the measurements in real time for the electrochemical testing.

Appendix D. Details of chemical reagent manufacturers.

Table D. Official names and manufacturer details of the reagents used during the post-processing.

Name	Official Name	Manufacturer
SPR 220-7	MEGAPOSIT SPR 2020-7	Rohm and Haas Electronic Materials LLC
HMDS	1,1,1,3,3,3-hexamethyldisilazane 98%	Thermo Scientific
MEK	Methyl Ethyl Ketone >=99%	Fisher Scientific
PGMEA	PGMEA-Thinner	CMC MATERIALS UPC LTD
MF26-A developer	MEGAPOSIT MF-26A Developoer	DuPont
Remover 1165	MICROPOSIT Remover 1165	DuPont
Acetone	Acetone	Thermo Scientific
IPA	Isopropyl alcohol	CMC MATERIALS UPC LTD

Appendix E . PCB Schematic and Layout



PCB Components		
Part Number	Description	Quantity
8484-11B1-RK-TP	PLCC Sockets 84 Positions 4 Rows	1
C0805C104K5RACTU	Multilayer Ceramic Capacitors MLCC 0.1uF	2
TAJB106K020RNJ	Surface Mount Tantalum Capacitor, 10 µF	2
TSW-108-08-L-S-RA	8 Way, 1 Row, Right Angle Pin Header	2
TSW-120-14-L-D	40 Way, 2 Row, Straight Pin Header	2
613040167028	40 Way, 1 Row, Straight Pin Header	1
ADE06A04	6 Way Through Hole DIP Switch SPST	1
3296W-1-102LF	Trimmer Resistors - Through Hole 3/8" 1Kohms	14
MCP6002-I/P	Op Amps Dual 1.8V 1MHz	2
110-41-308-41-001000	IC & Component Sockets 8 PIN SKT 200u Sn	2
NC7WZU04P6X	Inverters UHS Dual Unbuff Inv	1

Figure E. Schematic, layout and list of components for custom PCB.