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Doctor of Philosophy in Engineering

Tuneable Multilevel Capacitance Switching in Hafnium-Based Oxides

by

Deepika Yadav

2026

Contribution

- **D. Yadav**, S. Stathopoulos, T. Prodromakis, et al., "Multibit Ferroelectric Memcapacitor for Non-volatile Analogue Memory and Reconfigurable Filtering," *arXiv preprint*, arXiv:2511.09838v1, 2025. Accepted at *Advanced Functional Materials*.

- **D. Yadav**, H. Levene, T. Prodromakis, et al., "Impedance Spectroscopy of Hafnium Oxide: Memristive and Memcapacitive Switching with Annealing," *IEEE Transactions on Electron Devices*, 2025. doi: 10.1109/TED.2025.3547291.

- S. Kumar, **D. Yadav**, T. Prodromakis, et al., "Electrical Analysis of Atomic Layer Deposited Thin HfO_2 and HfO_2/Ta_2O_5-Based Memristive Devices," *IEEE Transactions on Electron Devices*, 2025. doi: 10.1109/TED.2025.3539256.

- C. Sbandati, X. Jiang, **D. Yadav**, et al., "Neuronal Multi-Unit Activity Processing with Metal Oxide Memristive Devices," *Advanced Electronic Materials*. doi: 10.1002/aelm.202400638.

- D. Guo, **D. Yadav**, S. Wang, et al., "A Multi-Channel Auditory Signal Encoder with Adaptive Resolution Using Volatile Memristors," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, 2025. doi: 10.1109/ISCAS56072.2025.11044000.

- G. Huang, Y. Zhang, **D. Yadav**, et al., "Characterisation and Data-Driven Modelling of Memimpedance," in *Proc. IEEE International Symposium on Circuits and Systems (ISCAS)*, 2025. doi: 10.1109/ISCAS56072.2025.11043853.

Abstract

Memcapacitors are devices exhibiting history-dependent capacitance in response to applied electrical stimuli and have attracted increasing attention as potential building blocks for adaptive, reconfigurable, and energy-efficient electronic systems. Unlike conventional tunable capacitors that rely on continuous biasing or mechanical actuation, memcapacitors offer non-volatile capacitance tuning, enabling circuits that retain their programmed functionality without static power consumption. However, practical implementations that are compact, CMOS-compatible, and capable of reliable multilevel operation remain limited. This thesis therefore investigates memcapacitive behaviour in metal–dielectric–metal device architectures. Hafnium oxides is chosen as the dielectric material due to it's high dielectric constant, ultrathin scalability, and CMOS compatibility, while appropriate compositional modification also enabling ferroelectric behaviour. These versatile properties allow hafnium oxide to be explored across two distinct physical regimes: defect-mediated switching in conventional hafnium oxide and polarisation-driven switching in ferroelectric hafnium zirconium oxide (HZO). This provides a unified framework to study the evolution of memcapacitive behaviour from binary to multilevel operation.

In the first part of the thesis, memcapacitive behaviour is examined in conventional hafnium oxide memristor. Although primarily investigated for resistive switching, the geometry is inherently capacitive, offering an opportunity to study capacitance modulation. Electrical characterisation reveals binary capacitance switching with a capacitance ratio of 1:3 and a memory window of $\sim$3 pF in a 20×20 μm^2 device, programmed using voltage pulses up to 5 V. Scaling the device area increases the absolute capacitance and enhances the capacitive ratio, confirming that the modulation scales with device geometry. Finally, an equivalent circuit model is developed to quantitatively capture the coupled resistive–capacitive behaviour.

Building on this binary baseline, the thesis then investigates ferroelectric HZO capacitors, where capacitance is controlled by switchable polarisation rather than defect dynamics. These devices exhibit a substantially enlarged non-volatile capacitance window of approximately 24 pF and enable access to more than eight stable capacitance states, with endurance $\sim 10^6$ cycles and retention beyond 10^5 s. The states are well separated, with switching behaviour analogous to potentiation–depression, and can be programmed using voltages within $\pm$3 V for a 60×60 μm^2 device size. Area-scaling analysis reveals a progressive reduction of the capacitive memory window with decreasing device size. At 20×20 μm^2, the memory window becomes comparable to that observed in memristive devices, while voltage-dependent analogue switching remains intact.

In this context, a single reconfigurable ferroelectric device can deliver capacitance densities of approximately 27 fF/μm^2, which are competitive with current MIM technologies, while simultaneously providing non-volatile and programmable capacitance states. This combina-

tion offers a pathway to reduce overall capacitor footprint by replacing multiple fixed-value elements with a single tunable memcapacitor. Further studies of frequency-dependent behaviour, dielectric loss, and DC leakage establish the operational limits and practical constraints governing reliable multistate performance. To verify circuit-level integration, the HZO devices were employed in a tunable high-pass filter and a relaxation RC oscillator. The filter cut-off frequency was tuned by 4.4 kHz, while the oscillator frequency was tuned by 6.5 kHz, directly translating non-volatile capacitance states into programmable frequency responses. In addition, complementary electrostatic force microscopy measurements confirm local charge and polarisation modulation, providing microscale evidence of stable multistate capacitive behaviour.

Overall, this thesis presents a comprehensive progression of memcapacitive behaviour in hafnium-based devices, from binary defect-mediated switching to multilevel ferroelectric operation, supported by electrical, microscopic, and circuit-level analyses. The results establish hafnium-based ferroelectric capacitors as a scalable and versatile platform for non-volatile analogue capacitance tuning, with relevance to reconfigurable electronics, adaptive analogue systems, and emerging memory-centric computing architectures.

Lay Summary

Capacitors are essential components in electronic circuits, where they help control signal frequency, timing, and energy flow. As circuit requirements change during operation, it is often desirable for the capacitance value to be adjustable, enabling adaptive tuning of circuit behaviour. Several tunable capacitor technologies already exist, but each comes with important limitations. Some tunable devices are physically large and cannot be integrated directly onto silicon chips, while others require a continuous electrical bias to maintain a chosen capacitance value, leading to constant power consumption. As a result, most capacitors used on chips today have fixed values. When tuning is required, designers must combine many fixed-value capacitors or add additional circuitry, which increases chip area, complexity, and power usage. Therefore, achieving tunable capacitance in a compact, energy-efficient form that can be integrated directly on-chip would address many of these challenges.

This thesis explores a new approach to tunable capacitors using hafnium-based oxide materials, which are already widely used in modern semiconductor manufacturing. By applying controlled electrical signals, the capacitance of a single, very small device can be adjusted across multiple well-defined levels within a simple and scalable device structure. This enables one tunable capacitor to replace multiple fixed-value capacitors typically used in circuits, offering a pathway to reduce overall chip footprint. Importantly, once programmed, the capacitor can retain its tuned value without continuous power. This non-volatile tuning capability not only improves energy efficiency but also enables new forms of adaptive electronics. In particular, the gradual and reversible tuning behaviour resembles how biological synapses adjust their strength, making these devices relevant for future brain-inspired computing systems. The tuning behaviour demonstrated in this work is stable, reproducible, and operates over practical frequency ranges relevant to real electronic systems. The thesis further shows how these tunable capacitors can be directly integrated into simple circuits, where changing the stored capacitance leads to predictable changes in circuit behaviour, such as signal frequency. In this way, the work represents a meaningful step toward practical memcapacitors that combine tunability, scalability, and low-power operation within a single on-chip device.

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Contents

Contribution i

Abstract ii

Lay Summary iv

Acknowledgements v

List of Figures x

List of Tables xiii

Abbrevations xiv

Nomenclature xvii

1 Introduction 1

1.1 Motivation 1

1.2 Aim and Scope of Thesis 3

1.3 Thesis Outline 4

2 Memcapacitors: Memristors to Ferroelectrics 5

2.1 Memristors: Definition, Physical Mechanisms, and Application 5

2.1.1 Definition and Historical Origin of the Memristor 6

2.1.2 Device Structure and working of Memristors 7

2.1.3 Applications and Impact of Memristive Devices 11
2.2 Memcapacitors: Origin and Types of Memcapacitor 13
2.3 The Memristor Memcapacitor 15
2.3.1 Coexistence of Resistive and Capacitive Switching 15
2.3.2 Frequency-Domain Characterisation and Impedance-Based Analysis . 16
2.3.3 Hafnium Oxide: A suitable Dielectric 19
2.4 Ferroelectric Memcapacitor 20
2.4.1 Evolution of Ferroelectric Materials Toward CMOS-Compatible Devices 20
2.4.2 Ferroelectricity in Hafnium-Zirconium Oxide 22
2.4.3 Capacitance-Voltage Hysteresis 24
2.4.4 Multibit Capacitance Switching 25
2.5 Conclusion 27

3 Device Fabrication and Thin film Analysis 28

3.1 Fabrication Overview 28
3.1.1 Lithography 29
3.1.2 Metal Electrode Deposition using Sputterer 31
3.1.3 Dielectric Layer by Atomic Layer Deposition 32
3.1.4 Lift-off, Etching and Annealing 34
3.2 Thin-Film Material Characterisation 34
3.2.1 X-ray Photoelectron Spectroscopy (XPS) 35
3.2.2 X-ray Diffraction (XRD) 36
3.2.3 Atomic Force Microscopy (AFM) 38
3.3 Conclusion 45

4 The Memristor-Memcapacitor 47

4.1 Characterisation Protocol 47
4.1.1 System Calibration and Measurement Setup 48

4.1.2 DC Characterisation 49
4.1.3 AC Characterisation 52
4.2 Impedance Spectroscopy and Analysis 53
4.2.1 Mathematical Aspect 53
4.2.2 Bode Plot 54
4.2.3 Nyquist Plot 56
4.3 Device Analysis 57
4.3.1 Resistive and Capacitive switching 58
4.3.2 Impedance spectroscopy 61
4.4 Conclusion 65

5 The Ferroelectric Memcapacitor 66

5.1 Characterisation Protocol 66
5.1.1 Polarisation-Voltage Measurement 68
5.1.2 Capacitance–Voltage Measurement 70
5.1.3 PUND and Endurance Measurement 71
5.2 HZO:The baseline Device 71
5.2.1 Polarisation-Voltage Analysis 72
5.2.2 Capacitance-Voltage Analysis 73
5.2.3 PUND and Endurance Analysis 77
5.3 Effect of Top Electrode 78
5.4 Material Stack Engineering 80
5.5 Conclusion 82

6 Multibit Ferroelectric Memcapacitor 84

6.1 Voltage dependent Switching 84
6.1.1 Voltage-Dependent P-V 85
6.1.2 Voltage-Dependent C-V 88

6.1.3 Multilstate Capacitance write-read operation 90
6.2 Factors affecting Capacitance 95
6.2.1 Loss Analysis 95
6.2.2 Area Dependence 96
6.2.3 Frequency Dependence 98
6.2.4 C-V Cycle Dependence 99
6.3 Circuit-Level Demonstration: Tunable High-Pass Filter 102
6.4 Conclusion 106

7 Conclusion and Future Work 108

7.1 Key Contributions and Conclusion 108
7.2 Limitations and Challenges 110
7.3 Future Directions 111
7.3.1 Standalone Device Optimisation 111
7.3.2 Array Integration on Wafer and CMOS Chip 112

8 Appendix 116

Bibliography 120

List of Figures

2.1 Symmetry of the four fundamental circuit variables 6
2.2 First experimental memristor Demonstration 7
2.3 Switching behaviour in memristors 8
2.4 Schematic of Electrochemical metallization memory 10
2.5 Schematic of Valence change memory 10
2.6 CMOS bottlenecks and future of computing 12
2.7 Extension of fundamental circuit elements 14
2.8 Non-zero crossing I-V hysteresis 16
2.9 Coupled resistive and capacitive switching 17
2.10 Impedance-derived equivalent circuit and conduction model in HfO_x-RRAM . 18
2.11 Ferroelectricity in doped HfO_2 22
2.12 Ferroelectric polarisation and domains 23
2.13 Landau energy landscape 24
2.14 Capacitive memory window in HZO 25
2.15 Multilevel capacitive potentiation and depression 26

3.1 Mask set used for fabricating the MIM device structures 29
3.2 Overview of the fabrication workflow 30
3.3 Device layout and SEM images of fabricated MIM capacitors. 35
3.4 XPS analysis of HfO_x and HZO films. 37
3.5 Grazing-incidence XRD analysis of HfO_x and HZO films 37

3.6 PFM characterisation of ferroelectric switching in the HZO film 40

3.7 PFM investigation of programming and reproducibility in HZO films 41

3.8 Time-dependent PFM switching behaviour of the HZO film 42

3.9 EFM mapping of charge contrast and multilevel states in HZO 45

4.1 Measurement protocol overview 48

4.2 Possible electroforming outcomes in devices 51

4.3 Impedance spectroscopy framework and equivalent circuit representation . . . 55

4.4 Resistive and capacitive switching of as-deposited and annealed HfO_x devices 58

4.5 AC impedance analysis of as-deposited and annealed HfO_x devices 62

4.6 Equivalent circuit modelling and fitting of impedance data for HfO_x devices . 65

5.1 Overview of the electrical characterisation workflow and device variants investigated in this chapter 67

5.2 Effect of rise–fall time on ferroelectric switching behaviour. 68

5.3 Illustration of common measurement artefacts in polarisation switching . . . 69

5.4 ake-up behaviour of the HfZrO ferroelectric capacitor 72

5.5 Influence of C–V sweep direction on subsequent ferroelectric switching behaviour 74

5.6 C–V characteristics and zero-bias retention in TiN/HZO/TiN capacitors . . 76

5.7 PUND and endurance analysis of TiN/HZO/TiN capacitors 77

5.8 Comparison of TiN/HZO/TiN and Pt/HZO/TiN capacitors 79

5.9 Comparison of stack-engineered HZO capacitors 81

6.1 Voltage-amplitude-dependent polarisation evolution in the HZO-MS capacitor 85

6.2 Switching time analysis using Merz and nucleation-limited models 87

6.3 Voltage-dependent C-V evolution under bipolar sweeping for different initial states 89

6.4 Multistate write-read operation and retention characteristics 91

6.5 Repeated programming behaviour at fixed voltage amplitude 93

6.6 Assessment of dissipative effects in the ferroelectric memcapacitor 96

6.7 Ferroelectric and capacitive behaviour with area scaling 97

6.8 Frequency behavior of HZO-MS memcapacitor 100

6.9 Cycle-dependent degradation of the C-V response in the HZO-MS capacitor 101

6.10 Experimental platforms for circuit-level evaluation 103

6.11 Programmable high-pass filter behaviour 104

6.12 Capacitance-programmable RC oscillator 105

7.1 Wafer-scale 1T1C array mask layout 113

7.2 1T1C crossbar-chip layout 114

8.1 TiOx memristor with only resisitve switching 117

8.2 Volatile TiO_x ALD device 118

8.3 Volatile HfTiO device 119

List of Tables

3.1 Summary of fabricated device stacks used in this work. 30

3.2 Lithography process parameters for the negative-tone (AZ 2035) and positive-tone (SPF 220) photoresists used in this thesis. 31

3.3 Summary of ALD dielectric stacks used in this thesis. 33

4.1 Size comparison for capacitive switching, reproduced from [1] 61

4.2 Electrical Characteristics of As-deposited and Annealed Samples, reproduced [1] 64

6.1 MFM memcapacitor comparison reported in literature and current work. . . . 94

6.2 Expected and measured data values for cut-off and passband 104

6.3 Programmed capacitance states and oscillation frequency in the tunable RC oscillator. 106

8.1 Device material systems, fabrication processes, and electrical behaviour. . . . 116

Abbreviations

1T1C One Transistor One Capacitor.

AC Alternating Current.

AFM Atomic Force Microscopy.

Al Aluminium.

ALD Atomic Layer Deposition.

BE Bottom Electrode.

BST Barium Strontium Titanate.

CIM Compute-In-Memory.

CMOS Complementary Metal–Oxide–Semiconductor.

CMU Capacitance Measurement Unit.

CPE Constant Phase Element.

CV Capacitance–Voltage.

DC Direct Current.

DUT Device Under Test.

ECM Electrochemical Metallization.

EFM Electrostatic Force Microscopy.

FeFET Ferroelectric Field-Effect Transistor.

FRAM Ferroelectric Random Access Memory.

FTJ Ferroelectric Tunnel Junction.

Gd Gadolinium.

HCS High-Capacitance State.

HfO_x Hafnium Oxide.

HfTiO Hafnium Titanium Oxide.

HRS High-Resistance State.

HZO / HfZrO Hafnium Zirconium Oxide.

IGZO Indium Gallium Zinc Oxide.

IS Impedance Spectroscopy.

IV Current–Voltage.

KAI Kolmogorov-Avrami-Ishibashi model.

La Lanthanum.

LCS Low-Capacitance State.

LRS Low-Resistance State.

MEMS Microelectromechanical Systems.

MFIS Metal–Ferroelectric–Insulator–Semiconductor.

MFM Metal–Ferroelectric–Metal.

MIM Metal–Insulator–Metal.

MIS Metal–Insulator–Semiconductor.

MoO_x Molybdenum Oxide.

MOS Metal–Oxide–Semiconductor.

MRAM Magnetoresistive Random Access Memory.

MS Multilayer Stack.

Nb_2O_5 Niobium Pentoxide.

NLS Nucleation-limited switching.

PCM Phase Change Memory.

PFM Piezoresponse Force Microscopy.

Pt Platinum.

PUND Positive-Up-Negative-Down.

PV Polarisation–Voltage.

RF Radio Frequency.

RT Room Temperature.

RTA Rapid Thermal Annealing.

Si Silicon.

SMU Source Measure Unit.

SS Switching Spectroscopy.

TE Top Electrode.

TiN Titanium Nitride.

TiO_x Titanium Oxide.

VCM Valence Change Memory.

W Tungsten.

WO_x Tungsten Oxide.

XPS X-ray Photoelectron Spectroscopy.

ZnO Zinc Oxide.

ZrO_x Zirconium Oxide.

Nomenclature

E Electric field ($\mathrm{V\,m^{-1}}$).

J_{C} Conduction current density ($\mathrm{A\,m^{-2}}$).

J_{D} Displacement current density ($\mathrm{A\,m^{-2}}$).

J_{tot} Total current density ($\mathrm{A\,m^{-2}}$).

P Polarisation ($\mathrm{C\,m^{-2}}$).

P_r Remanent polarisation ($\mathrm{C\,m^{-2}}$).

P_s Saturation polarisation ($\mathrm{C\,m^{-2}}$).

Q Electric charge (C).

R Resistance (Ω).

R_s Series resistance (Ω).

X_c Capacitive reactance (Ω).

Z Complex impedance (Ω).

ϵ_0 Vacuum permittivity ($\mathrm{F\,m^{-1}}$).

ϵ_r Relative permittivity (dimensionless).

ω Angular frequency ($\mathrm{rad\,s^{-1}}$).

ϕ Impedance phase angle (rad).

σ Electrical conductivity ($\mathrm{S\,m^{-1}}$).

$\tan\delta$ Dielectric loss tangent (dimensionless).

τ Characteristic relaxation time (s).

f Frequency (Hz).

f_c Cut-off frequency (Hz).

t Dielectric thickness (m).

Chapter 1

Introduction

1.1 Motivation

Capacitors are essential components in integrated circuits, playing a central role in analog, radio-frequency (RF), and mixed-signal subsystems, where they enable functions such as adaptive circuit operation and frequency reconfiguration. In many of these applications, the ability to tune capacitance dynamically is highly desirable. Several established tunable capacitor technologies have been developed and deployed in practical systems, particularly in RF and microwave applications. One of the most widely used approach is based on microelectromechanical systems (MEMS) capacitors, which utilise electrostatic actuation to modify electrode spacing or overlap area, enabling wide tuning ranges and high quality factors [2]. These characteristics make MEMS capacitors particularly attractive for high-performance RF applications, where low loss and large tuning ranges are critical. However, their reliance on mechanical motion introduces challenges related to reliability, switching speed, fabrication complexity, and device footprint [3]. As a result, MEMS capacitors are typically implemented off-chip, limiting their scalability and suitability for on-chip integration.

Beyond MEMS, tunable capacitance in electronic systems is most commonly realised using semiconductor and ferroelectric varactors. Semiconductor varactors achieve tunability through voltage-controlled modulation of depletion or accumulation regions and are widely used in voltage-controlled oscillators and phase-locked loops due to their fast response, and ease of on-chip integration. However, their tuning range is typically limited and inherently volatile, requiring a continuous direct-current bias to maintain a given capacitance state. In addition, strong voltage-dependent nonlinearity, interface charge accumulation, and bias-induced degradation can degrade performance in precision analog and RF circuits.

An alternative class of electronic varactors is based on ferroelectric materials such as barium strontium titanate (BST), in which capacitance modulation arises from the strong electric-field dependence of the material permittivity [4]. BST-based capacitors can provide large and continuous capacitance tuning within compact thin-film geometries, together with high capacitance density, making them attractive for RF and microwave applications. However, elevated dielectric losses, temperature sensitivity, and materials integration challenges have limited their widespread adoption in standard CMOS system-on-chip platforms.

Owing to the challenges associated with integrating tunable capacitors onto highly scaled semiconductor platforms, modern integrated circuits continue to rely heavily on fixed on-chip metal-insulator-metal (MIM) capacitors for analog and RF functionality. In many system-on-chip implementations, these capacitors occupy a substantial fraction of the analog and RF layout, in some cases accounting for up to approximately 40% of the local circuit area [5]. Hence, despite offering good linearity and low loss, MIM capacitors impose significant area overhead and restrict circuit-level reconfigurability.

Motivated by the limitations of conventional tunable capacitors, a new class of capacitive elements has emerged as an extension of memristive systems, commonly referred to as memcapacitors [6, 7]. In contrast to conventional capacitors, memcapacitors exhibit capacitance values that depend not only on the instantaneous applied voltage but also on the history of electrical excitation, enabling reconfigurable capacitance states without the need for continuous biasing. The development of memcapacitors has been driven by advances in materials and device physics that enable electrically controllable internal states to influence the capacitive response. Several physical mechanisms have been explored to realise memcapacitive behaviour. A prominent class is based on ion migration and redistribution, that is a memristive device architectures, where electrically driven ionic motion modifies internal electric fields and interfacial charge distributions. Such structures are particularly attractive as they can enable coupled resistive and capacitive tuning within a simple device geometry [1, 8, 9, 10].

Charge trapping provides an alternative mechanism for inducing memory effects in capacitive structures and is well established in charge-trap flash memory, where trapped charge is primarily exploited to modulate threshold voltage. When intentionally harnessed to influence internal electric fields, charge trapping can also be used to realise programmable, history-dependent capacitive behaviour, motivating its exploration as a potential memcapacitive mechanism [11, 12, 13].

Finally, ferroelectric polarisation provides a distinct route to memory effects in capacitive structures, where remanent polarisation states modulate the dielectric response and interfacial capacitance. In particular, hafnium-based ferroelectric materials have attracted significant attention due to their compatibility with CMOS processing, scalability to nanometre thicknesses, and ability to sustain stable polarisation switching at low operating voltages. When exploited in capacitor architectures, ferroelectric polarisation enables programmable, history-dependent capacitance states without continuous biasing, motivating their investigation as a platform for non-volatile memcapacitive behaviour. As a result, considerable research effort has been directed toward improving the operating efficiency, stability, and controllability of such devices to enable reliable memcapacitive behaviour, with growing exploration across a range of contexts including RF circuit application, memory elements, and neuromorphic architectures [14, 15, 16].

Taken together, these developments establish memcapacitors as a distinct class of tunable capacitive devices with the potential to overcome key limitations of conventional technologies. However, despite increasing interest, memcapacitive research remains comparatively immature. As a result, the physical origins and practical implications of history-dependent capacitance are not yet fully understood. This motivates a systematic investigation of memcapacitive behaviour to clarify underlying mechanisms and assess their relevance for integrated electronic systems.

1.2 Aim and Scope of Thesis

The aim of this thesis is to establish hafnium-oxide-based capacitors as a recently emerging class of scalable, electrically reconfigurable capacitive elements that overcome the fundamental limitations of existing tunable capacitive technologies. In particular, the thesis seeks to demonstrate that metal–dielectric–metal capacitors based on hafnium oxides can deliver non-volatile, multistate capacitive tuning within a compact, CMOS-compatible platform, enabling direct translation from device physics to circuit-level functionality.

To achieve this, the thesis investigates memcapacitive behaviour arising from two distinct yet complementary physical mechanisms within hafnium-based architectures: defect-mediated internal state modulation in conventional HfO_x devices and polarisation-driven switching in ferroelectric $HfZrO_x$ (HZO) capacitors. In both systems, electrically induced internal states governed respectively by defect dynamics and ferroelectric domain switching give rise to history-dependent capacitance modulation, allowing capacitance to be programmed and retained without continuous biasing.

Beyond identifying the underlying mechanisms, the thesis aims to determine how material processing, device scaling, and electrical excitation conditions can be engineered to widen the capacitive tuning window, stabilise multistate operation, and define practical operating limits relevant to circuits. For memristive HfO_x devices, this involves resolving coupled resistive–capacitive processes through comprehensive electrical characterisation, including impedance spectroscopy, and determining how thermal annealing modifies defect landscapes. For ferroelectric HZO capacitors, the investigation spans micro to macro-scale characterisation, encompassing controlled multistate tuning behaviour, analysis of dielectric losses and stability, and demonstration of device-level functionality relevant to circuit operation, thereby enabling direct correlation between domain-scale switching, charge redistribution, and the resulting capacitive response.

Ultimately, this thesis aims to reposition capacitors from fixed passive components to programmable functional elements. By translating multistate capacitance control into reproducible circuit-level behaviour, the thesis also provides a thorough measurement and analysis framework for hafnium-based memcapacitors, addressing a critical gap in a field where standardised characterisation approaches remain limited. This framework establishes a reproducible reference point for future studies, enabling consistent comparison, validation, and extension of memcapacitive behaviour across materials, devices, and circuit implementations, and positions hafnium-based memcapacitors as viable building blocks for adaptive analogue electronics, reconfigurable RF systems, and emerging memory-centric computing architectures.

1.3 Thesis Outline

This thesis is organised to move from background and methodology to detailed experimental investigation and functional demonstration of memcapacitive behaviour in hafnium-based devices. The progression of chapters reflects the development from fundamental mechanisms to multistate capacitive operation and circuit-level relevance.

Chapter 2 reviews two complementary routes to memcapacitance: ion-mediated, memristor-derived behaviour in HfO_x devices, and ferroelectric polarisation-driven capacitance modulation in HZO capacitors. Prior to introducing memcapacitors directly, the chapter provides a focused discussion of memristive systems from which the memcapacitor concept emerges, followed by a critical literature survey of both approaches.

Chapter 3 describes the experimental workflow used to fabricate and characterise the HfO_x memristors and ferroelectric HZO capacitors studied in this thesis. In addition to device fabrication, thin-film characterisation is presented to establish the relationship between processing conditions, film properties, and subsequent electrical behaviour. This includes structural, chemical, and morphological analysis using techniques such as XPS, XRD, and AFM.

Chapter 4 investigates the electrical behaviour of HfO_x MIM devices, with a focus on the coexistence of resistive and capacitive switching. Beyond conventional resistive metrics, the chapter examines tunable and non-volatile capacitive responses and their evolution with thermal annealing. Impedance spectroscopy is introduced as a central analytical framework to decouple resistive and capacitive contributions and to interpret frequency-dependent behaviour.

Chapter 5 presents a systematic investigation of ferroelectric HZO-based capacitors with the objective of establishing a stable and optimised ferroelectric memcapacitor platform. The chapter examines how polarisation switching governs non-volatile capacitance modulation, beginning with baseline device behaviour and wake-up effects. Electrode and dielectric stack engineering are then explored to enhance switching symmetry, memory window, and endurance, providing the foundation for multistate operation.

Chapter 6 constitutes the core contribution of the thesis, demonstrating multistate, non-volatile memcapacitive behaviour in optimised HZO capacitors. By controlling voltage programming, intermediate ferroelectric states are stabilised, enabling reproducible multibit capacitance levels within a single device. The chapter establishes the role of frequency, device area, and cycle repetition on the memory window, and demonstrates functional relevance through circuit-level integration in a reconfigurable high-pass filter and RF oscillator.

Chapter 7 summarises the main findings of the thesis and discusses the limitations for memcapacitive device design and operation. Directions for future research are outlined, including opportunities to further improve endurance, develop more reliable switching schemes, and reduce dielectric and circuit-level losses. The chapter also discusses the extension of standalone memcapacitor concepts to array-level implementations, demonstrated through an 8×8 one-transistor-one-capacitor architecture realised both at the wafer level and within a 180 nm CMOS platform.

Chapter 2

Memcapacitors: Memristors to Ferroelectrics

This chapter surveys and contextualises the physical mechanisms, material platforms, and device concepts underpinning memcapacitive behaviour in thin-film oxide systems, with particular emphasis on hafnium-based technologies. Two distinct yet complementary routes to memcapacitance are examined. First, memristor-derived memcapacitive behaviour is discussed, where capacitive modulation emerges from defect dynamics and interfacial charge redistribution in HfO_x devices. Second, ferroelectric-based memcapacitors are introduced, focusing on $HfZrO_x$ capacitors in which non-volatile and multilevel capacitance states arise from controlled ferroelectric domain switching. The chapter reviews the key experimental signatures, operating principles, and limitations reported in the literature for both approaches, and identifies open challenges related to memory window stability, multilevel accessibility, and scalability. This framework motivates the experimental investigations presented in the subsequent chapters, which aim to systematically analyse, optimise, and extend multibit capacitive behaviour in hafnia-based memcapacitor devices.

2.1 Memristors: Definition, Physical Mechanisms, and Application

Memristors form the conceptual and experimental foundation from which memcapacitive behaviour was first identified and explored. The earliest physical manifestations of memcapacitive effects emerged naturally from memristive device physics, as defect migration, charge trapping, and interfacial polarisation, processes central to resistive switching that also give rise to history-dependent capacitance. Understanding the definition and physical mechanisms of memristors is therefore essential before addressing memcapacitive behaviour. This section further examines representative memristor applications, not only as examples of resistive memory, but to highlight application domains that are later shown in this chapter to be more efficiently addressed using capacitive, rather than resistiv, memory elements.

2.1.1 Definition and Historical Origin of the Memristor

Electronic systems are traditionally constructed using a small set of fundamental circuit elements, which are broadly classified as either active or passive[17]. Active elements, such as transistors, voltage sources, and current sources, are capable of supplying energy or providing power gain within a circuit. In contrast, passive elements do not generate energy; instead, they dissipate, store, or release energy supplied by external sources. Passive elements such as resistors, capacitors, and inductors form the foundation of classical circuit theory and have long served as the basic building blocks of electronic system design. For several decades, these three elements were regarded as complete and sufficient to describe all passive electrical behaviour.

In 1971, Leon Chua challenged this long-standing view by postulating the existence of a missing fourth fundamental passive circuit element, motivated by the symmetry of the fundamental circuit variables: current, voltage, charge, and magnetic flux, as schematically illustrated in Fig. 2.1. While resistors relate voltage and current, capacitors relate voltage and charge, and inductors relate current and magnetic flux, Chua observed that no circuit element directly related charge and magnetic flux. To complete this symmetry, he proposed *memristor*, an element defined by a constitutive relation between charge and flux, giving rise to a state-dependent resistance termed *memristance* [7]. A defining feature of the memristor is that its instantaneous resistance depends explicitly on the history of electrical excitation applied to the device.

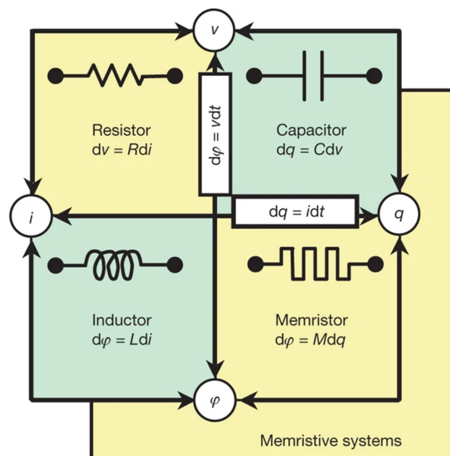

Figure 2.1: **Symmetry of the four fundamental circuit variables**: Current (i), voltage (v), electric charge (q), and magnetic flux (ϕ) and their associated circuit elements. Resistors, capacitors, and inductors relate pairs of variables through differential constitutive relations, while the memristor completes the symmetry by defining a direct relationship between charge and flux. Reproduced from [18]. Copyright © 2008 Springer Nature.

Although Chua's proposal was mathematically rigorous and conceptually elegant, it attracted limited attention at the time due to the absence of a clear physical realisation. As a result, the memristor remained largely a theoretical construct for several decades. During this period, numerous physical systems, particularly thin-film oxides were reported to exhibit history-dependent resistance changes [19, 20, 21, 22, 23, 24]. However, such behaviour was not formally recognised within the framework of a fundamental circuit element and was therefore not identified as manifestations of memory resistance.

A decisive turning point occurred in 2008, when a research team at Hewlett–Packard Laboratories, led by Stanley Williams, reported resistive switching behaviour in nanoscale metal–insulator–metal structures based on titanium dioxide thin films and explicitly identified this behaviour as a physical realisation of Chua's memristor [18]. In this device architecture, a thin TiO_2 layer was sandwiched between metallic electrodes, and resistance modulation was explained through field-driven migration of oxygen vacancies within the oxide. Importantly, this work demonstrated that memristive behaviour can arise naturally in nanoscale systems where electronic transport is coupled to ionic motion under an external electric field. The redistribution of charged atomic species alters the effective conductive region of the device, enabling reversible and non-volatile resistance switching.

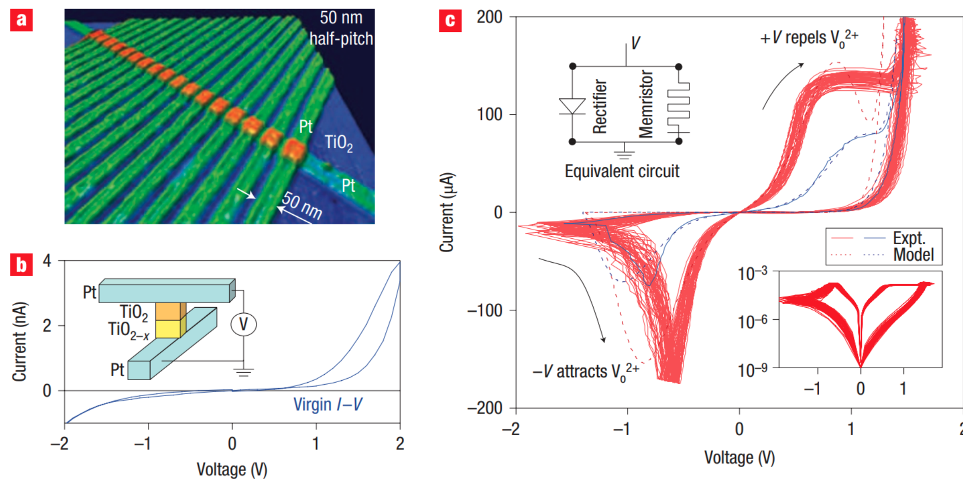

Figure 2.2: **Experimental demonstration of memristive behaviour in nanoscale TiO_{2-x} devices reported by HP Lab.** (a) Atomic force microscopy image of crossbar nano-devices with a Pt/TiO_{2-x}/Pt metal–insulator–metal architecture. (b) Schematic of the device structure and the corresponding current–voltage response of a pristine device. (c) Reproducible bipolar current–voltage characteristics measured over multiple switching cycles, exhibiting a pinched hysteresis loop that passes through the origin. Reproduced from [25]. Copyright © 2008 Springer Nature

The current–voltage characteristics observed in Fig. 2.2 exhibit a distinctive pinched hysteresis loop, which is widely regarded as the defining electrical signature of a memristor. This behaviour reflects the underlying memory effect that distinguishes memristive systems from conventional nonlinear resistive elements lacking state-dependent dynamics, and therefore serves as a practical experimental criterion for identifying memristive behaviour. This 2008 demonstration is widely regarded as the first experimentally convincing validation of the memristor concept and has since served as a foundation for understanding resistive switching phenomena in nanoscale thin-film devices.

2.1.2 Device Structure and working of Memristors

From an electrical characterisation perspective, memristive devices are commonly identified by their nonlinear current-voltage response exhibiting a pinched hysteresis loop, as discussed in the previous section. In practical device operation, this history-dependent behaviour manifests as electrically accessible resistance states that can be reproducibly programmed and read.

Memristors are therefore often described in terms of a high-resistance state (HRS) and a low-resistance state (LRS), with information encoded by switching the device between these states using voltage or current excitation. Depending on the material system, device structure, and programming conditions, this switching may occur abruptly between two well-defined resistance levels or progressively through a series of intermediate states, enabling either binary or analogue operation as schematically illustrated in Fig. 2.3 [26].

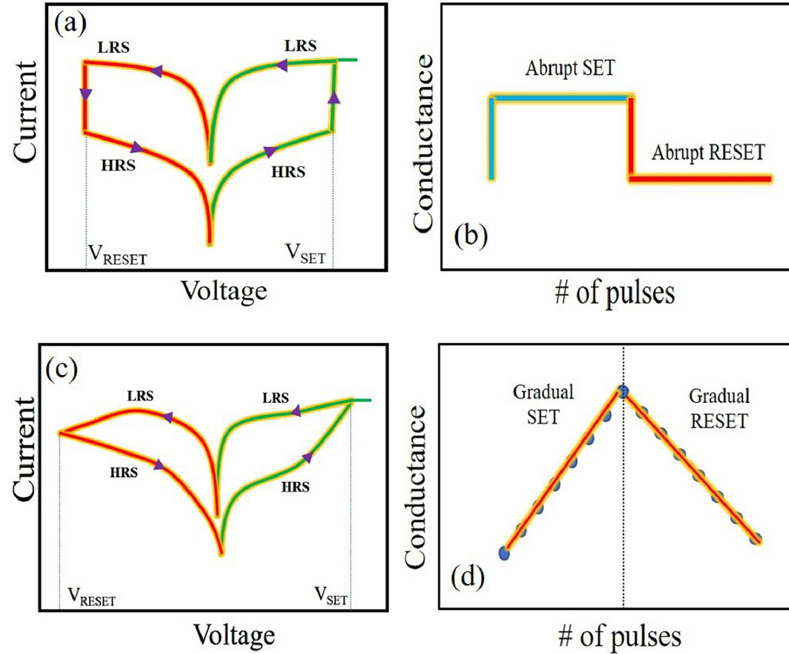

Figure 2.3: **Representative electrical characteristics of memristive devices illustrating binary and analogue switching behaviour.** (a–b) I-V characteristics exhibiting abrupt transitions between the HRS and LRS, together with the corresponding pulse-induced conductance evolution indicative of abrupt switching. (c–d) I-V characteristics with gradual resistance modulation and progressive conductance change under successive voltage pulses, enabling multilevel operation. Reproduced from Ref. [26]. Copyright © 2022 Elsevier.

Memristors are most commonly realised in a metal-insulator-metal (MIM) configuration, in which a thin functional layer is sandwiched between two electrodes. This simple vertical stack serves as a generic platform for a wide range of resistive switching phenomena and underpins the majority of memory-oriented implementations. Although lateral device geometries have also been demonstrated, vertical configurations dominate memory applications. In vertical devices, the electrode separation is defined by the thickness of the active layer, allowing nanometre-scale dimensions, reduced operating voltages, and high integration density, all of which are essential for scalable memory arrays [27].

A wide range of materials have been explored as the active layer in memristor devices, reflecting the diversity of underlying switching mechanisms. Oxide-based materials such as TiO_x, ZrO_x, HfO_x, SiO_x, WO_x, and ZnO are among the most extensively studied, owing to their compatibility with complementary metal-oxide-semiconductor (CMOS) processing [28, 29, 30, 31, 32]. This compatibility arises from their ability to be integrated into standard fabrication flows without interfering with key process steps such as self-aligned salicide formation or introducing contamination to silicon device layers. Beyond conventional oxides, two-dimensional materials including MoS_x, graphene, MXenes, and halide perovskites have

been investigated for flexible and emerging device platforms [33, 34, 35, 36]. Amorphous semiconductors such as indium-gallium-zinc oxide (IGZO) have also been explored for flexible and transparent memristive devices [37].

In most practical implementations, pristine memristor devices initially exhibit a very high resistance and require an electroforming step prior to normal operation, however forming free devices do exist [38]. Forming typically involves the application of a sufficiently large voltage or current stress, which induces irreversible microscopic changes within the active layer, such as defect generation, vacancy redistribution, or local structural modification. This process establishes electrically active conduction pathways and enables subsequent reversible switching between the HRS and LRS at significantly lower operating voltages.

Depending on the dominant physical mechanism responsible for resistance modulation, memristive switching in MIM structures is most commonly classified into electrochemical metallization (ECM) and valence change memory (VCM), which form the focus of the following sections. Other resistive memory technologies, including phase-change memory (PCM) and magnetoresistive random-access memory (MRAM), also employ resistance-based readout. However, they rely on fundamentally different physical mechanisms, such as structural phase transitions and spin-dependent tunnelling, respectively [39, 40]. As these mechanisms fall outside the scope of oxide-based memristive and impedance-driven phenomena, hence they are not considered further in this thesis.

Electrochemical Metallization Memories (ECM)

A typical ECM device consists of an insulating or weakly conducting solid electrolyte sandwiched between an electrochemically active electrode, most commonly silver or copper, and an inert counter electrode such as platinum, tungsten, or TiN [41, 42, 43, 44, 45, 46]. The intermediate layer serves primarily as an ion-conducting medium for metal cations. Upon application of an external bias, metal atoms at the active electrode are oxidised and injected into the insulating layer as mobile cations. These ions migrate under the applied electric field and are reduced near the inert electrode, leading to the nucleation and growth of a metallic filament that progressively bridges the two electrodes. The formation of this conductive filament drives the device into a LRS.

Reversal of the applied polarity or application of a sufficiently large voltage can dissolve or rupture the filament either through electrochemical back-diffusion of metal ions or local Joule heating, thereby restoring the device to a HRS. This filamentary switching mechanism typically results in abrupt resistance transitions and high ON/OFF ratios, and ECM devices are therefore most commonly associated with binary, digital-like switching behaviour as shown in Fig 2.4. In the context of industrial memory development, such devices are often referred to as conductive-bridging random access memory, whereas the term ECM is more commonly used in the scientific literature to emphasise the underlying electrochemical processes. ECM switching has been demonstrated across a wide range of material systems, reflecting the generality of this mechanism.

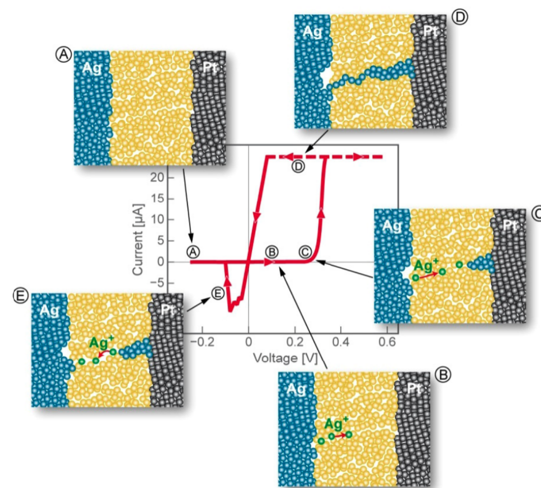

Figure 2.4: **Schematic of the ECM switching in an Ag-based metal-electrolyte-metal device.** The sequence (A–E) correlates the measured current-voltage characteristics with the evolution of Ag ion migration and metallic filament formation leading to the LRS, followed by filament dissolution that restores the HRS. Reproduced from [41]. Copyright © 2011 IOP Publishing.

Valence Change Memories (VCM)

In contrast to ECM, valence change memory (VCM) devices rely on resistive switching mechanisms that are intrinsic to the oxide layer itself. VCM behaviour is most commonly observed in non-stoichiometric transition metal oxides, where the presence and redistribution of oxygen vacancies under an applied electric field play a central role in modulating electrical conduction. These vacancies act as charged defects that locally alter the valence state of neighbouring cations and, consequently, the electronic structure of the oxide [47].

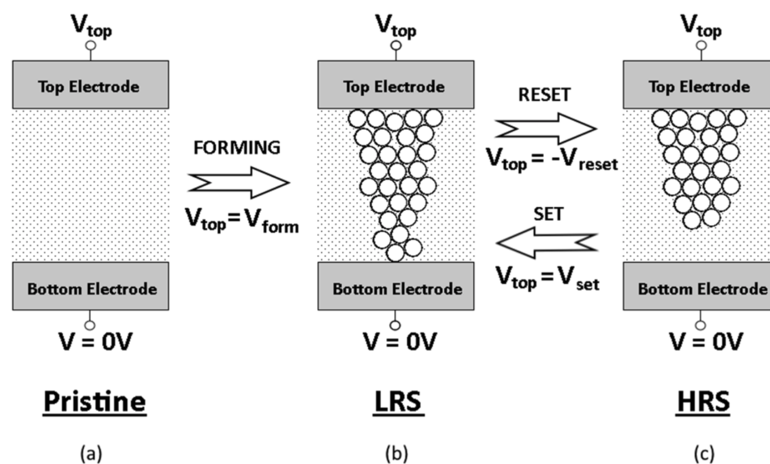

Figure 2.5: **Schematic illustration of the valence change memory.** (a) Pristine device state, where the oxide layer is highly insulating prior to electroforming. (b) LRS formed after the application of a forming voltage. (c) HRS achieved by applying a RESET voltage of opposite polarity, resulting in partial rupture of the conductive filament near the electrode interface. Reproduced from [47]. Copyright © 2015 MDPI .

A typical VCM device adopts MIM architecture, in which an oxide layer is sandwiched between two inert or weakly reactive electrodes. When a suitable voltage is applied, oxygen vacancies migrate within the oxide, leading to local changes in stoichiometry and the formation of regions with enhanced electronic conductivity. While the redistribution of oxygen vacancies governs the change in resistance state, the electrical current itself is carried by electrons through these vacancy-modulated conduction paths. Owing to the gradual and spatially distributed nature of vacancy redistribution, resistance modulation in VCM devices is often continuous, enabling analogue or multilevel switching behaviour [48, 49]. Under certain conditions, however, vacancy accumulation can become sufficiently localised to produce abrupt, binary switching behaviour [50]. In many material systems, such localised vacancy accumulation results in the formation of a conductive filament composed of oxygen-deficient oxide, where cations undergo a reduction in valence state. The formation of this filament drives the device into a LRS, while partial re-oxidation or redistribution of vacancies disrupts the conductive path and restores the HRS. The electronic transport in these resistance states is typically governed by interface and defect-mediated conduction processes, commonly described by Schottky emission at the electrode-oxide interface or Poole-Frenkel conduction through trap states within the oxide [51]. The TiO_x device reported by HP Lab works on similar mechanism [18]. Importantly, VCM switching does not necessarily require the formation of a fully developed filament. In several oxide systems, resistive switching has been shown to be dominated by interfacial effects, where modulation of the Schottky barrier at the electrode-oxide interface governs the resistance state [52]. In such cases, the LRS may scale with device area, indicating a non-filamentary or interface-controlled switching mechanism, or a hybrid behaviour combining both bulk and interfacial contributions.

Owing to its oxide-intrinsic nature, VCM switching offers a more suitable platform for exploring impedance and capacitance-based memory effects. In contrast to ECM devices, where resistance modulation is governed by the formation of metallic conductive bridges that effectively short the dielectric, VCM devices preserve the insulating character of the oxide to a greater extent. This distinction makes VCM-based systems more amenable to capacitive studies, where controlled modulation of dielectric response is essential.

2.1.3 Applications and Impact of Memristive Devices

The strong interest in memristive devices over the past two decades is driven not only by their identification as the long-postulated fourth fundamental circuit element, but more importantly by their potential to address fundamental limitations of modern computing technologies [53, 54, 55, 56]. For several decades, progress in electronics was sustained by Moore's law, whereby shrinking transistor dimensions led to simultaneous improvements in performance, energy efficiency, and integration density. Today, however, transistor scaling has approached atomic limit, and further size reduction no longer yields proportional gains in speed or power efficiency [57]. As a result, continued reliance on conventional CMOS scaling is insufficient to meet the growing demands of data storage and computation. While CMOS transistors remain the fundamental building blocks of both logic circuits and conventional memory technologies, transistor-based memory cells typically require multiple devices per bit or complex charge-storage structures such as floating-gate MOSFETs, which limit achievable storage density and increase circuit complexity.

Beyond device-level scaling limits, the architecture of modern computing systems has itself

become a major source of inefficiency. Most current processors are based on the von Neumann architecture, in which memory and processing units are physically separated [58]. While logic devices have benefited from decades of transistor scaling, improvements in memory access speed and energy efficiency have progressed much more slowly. Also, static random-access memory (SRAM), widely used as on-chip cache, requires six transistors per stored bit to maintain fast and reliable operation, resulting in significant area overhead compared with emerging two-terminal memory devices. As a result, data transfer between memory and compute units rather than the computation itself has become a major source of energy consumption and delay at the system level.

This limitation is especially evident in data-intensive workloads such as artificial intelligence and machine-learning applications, which rely heavily on repeated vector-matrix multiplications and frequent access to large data sets [54]. Although such workloads are typically executed on highly parallel processors such as GPUs, which are designed to accelerate these operations, memory remains physically separate from the compute cores. Consequently, even GPU-based systems incur significant energy and time overhead due to constant data movement between memory and computation units. Recent studies on large-scale AI models have highlighted not only the high financial cost of training and deployment, but also the associated carbon footprint, raising concerns about scalability, sustainability, and suitability for edge or mobile systems [59]. These challenges have intensified the search for alternative computing paradigms that reduce data movement and improve energy efficiency at a fundamental level.

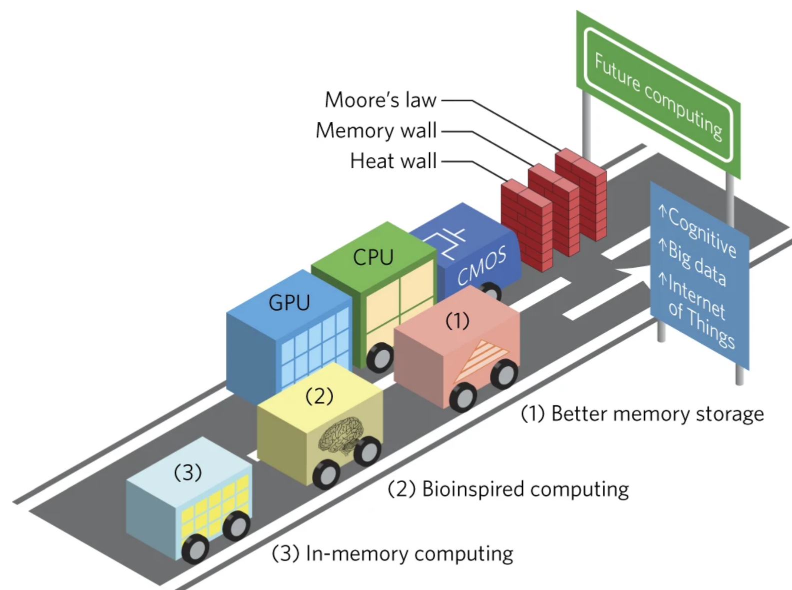

Figure 2.6: **CMOS bottlenecks and future of computing.**Overview of CMOS scaling limits and memory bottlenecks motivating alternative computing approaches, including enhanced memory storage, neuromorphic computing, and in-memory computation provided by memristor. Reproduced from [56].Copyright © 2018 Springer Nature.

In-memory computing and analogue information representation. Memristive devices provide a natural hardware platform for in-memory or compute-in-memory (CIM) computing, in which data storage and computation are co-located within the same physical structure [60, 61]. This architectural feature directly addresses the inefficiencies associated with frequent data transfer between memory and processing units in conventional computing systems. When arranged in crossbar architectures, memristive devices can directly implement

vector-matrix multiplication by exploiting Ohm's law for multiplication and Kirchhoff's current law for summation, enabling massively parallel computation within a single operation. This capability offers a promising route towards energy-efficient acceleration of data-intensive workloads. In addition to their computational role, memristors inherently function as memory elements. Unlike conventional digital memories that store information in strictly binary states, memristive devices can support multiple, continuously tunable resistance levels. This analogue behaviour enables information to be stored with higher density without further device miniaturisation [62]. Although floating-gate MOSFET memories have the potential to provide a variable threshold voltage similar to memristor, but the information is stored as charge within an isolated gate structure and requires complex transistor architectures and high-voltage programming mechanisms. In contrast, memristive devices store information through changes in their internal resistance state within a simple two-terminal device configuration. The ability to combine dense data storage with CIM highlights a key advantage of memristive technologies over traditional memory and logic components.

Neuromorphic computing and artificial intelligence. A particularly influential application domain for memristive devices is neuromorphic computing, which draws inspiration from the structure and operation of biological neural systems [63, 64, 65]. In this framework, memristors act as artificial synapses, where device conductance represents synaptic weight and history-dependent behaviour enables learning and adaptation. Modern artificial intelligence workloads, including artificial neural networks and spiking neural networks, rely heavily on repeated vector-matrix multiplications during both training and inference. GPUs dependence on frequent memory access leads to substantial energy consumption and limits deployment in edge and mobile platforms. Memristive neuromorphic architectures offer an alternative paradigm in which synaptic weights are stored locally and updated in place, reducing data movement and enabling low-power, event-driven computation. In this context, both volatile and non-volatile memristive behaviours have been explored to emulate short-term and long-term synaptic plasticity, respectively, providing a closer functional analogy to biological systems.

Broader applications and motivation for alternative memory modalities. Beyond memory storage, in-memory computing, and neuromorphic systems, memristive devices have been investigated for a wide range of additional applications, including reconfigurable electronics, sensing and optoelectronic systems [66, 67, 68, 69]. These studies highlight the versatility of memristive technologies, but they also reveal important challenges such as device variability, stochastic switching behaviour, limited endurance, and difficulties in achieving precise and stable analogue control. While addressing these challenges remains an active area of research, they motivate continued exploration for improved control over internal state variables.

2.2 Memcapacitors: Origin and Types of Memcapacitor

The concept of the memcapacitor emerged as a natural extension of Chua's theory of memory-enabled circuit elements. While the memristor formalised resistance with memory, Di Ventra and co-workers subsequently demonstrated that memory effects are not inherently restricted to resistive systems, but can be generalised to capacitive and inductive elements as well [6]. Within this broader framework of memory circuit elements, a memcapacitor is defined as a capacitor whose instantaneous capacitance depends on the history of applied electrical excitation through one or more internal state variables. A meminductor is defined

analogously as an inductor whose inductance evolves according to past current or flux. These definitions are formulated at the level of circuit behaviour and are independent of any specific material system or device geometry.

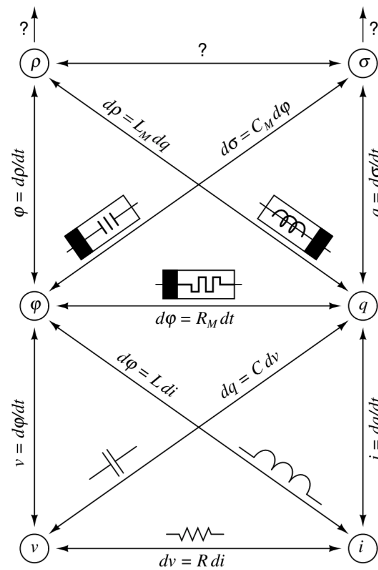

Figure 2.7: **Extension of fundamental circuit elements**Conceptual framework extending the four fundamental circuit variables to include memory-enabled elements. In addition to the resistor, capacitor, and inductor, the diagram illustrates the memristor, memcapacitor, and meminductor as elements whose constitutive relations depend on internal state variables, completing the symmetry of Chua's circuit element taxonomy. Reproduced from [70]. Copyright © 2014 Springer International Publishing.

Importantly, the earliest experimental indications of memory-enabled capacitance emerged in nanoscale memristive devices [8, 71, 8, 72]. This was not because such devices were intentionally designed as memcapacitors, but because the internal physical processes responsible for resistive switching such as charge redistribution, defect motion, and interface polarisation, can also give rise to history-dependent capacitive responses. As a result, memristive systems represent the practical platform in which memcapacitive effects were observed and studied, treated often as a secondary or coupled phenomenon. Beyond memristive systems, a second and conceptually distinct class of memcapacitors is realised in ferroelectric materials [73]. In these systems, polarisation switching leads directly to programmable and hysteretic capacitance, providing an intrinsic form of capacitive memory that does not rely on conductive filament formation or resistive state changes. Ferroelectric memcapacitors therefore represent a more direct physical realisation of the memcapacitor concept, with capacitance serving as the primary state variable.

Capacitive memory effects have also been reported in a range of device stacks that do not rely on resistive switching, including charge-trap dielectrics, nanopores, electrochemical capacitors, and interface-dominated metal–insulator–semiconductor (MIS) and metal–oxide–semiconductor (MOS) structures [74, 75, 76, 77]. In these systems, history-dependent capacitance typically arises from charge trapping, ionic redistribution, or interfacial polarisation rather than from changes in conductive pathways. A substantial body of work continues to explore such effects for sensing, reliability, and memory-related applications.

However, the present thesis focuses on memcapacitive behaviour realised through memristive and ferroelectric material systems. Accordingly, the following sections examine, first, memcapacitive effects that emerge with memristive switching and their identification through frequency-domain and impedance-based characterisation, and second, intrinsically capacitive ferroelectric memcapacitors, which form the foundation for the ferroelectric systems investigated in later chapters.

2.3 The Memristor Memcapacitor

2.3.1 Coexistence of Resistive and Capacitive Switching

Memristive devices are typically realised in MIM architectures, in which a thin dielectric layer is sandwiched between two electrodes. From a purely geometric and electrostatic standpoint, such structures inherently possess capacitance, independent of any memory functionality. As a result, every practical memristor comprises not only a state-dependent resistive element, but also capacitive components arising from the dielectric bulk and electrode interfaces. The central question is therefore not whether capacitance exists in memristive devices, but whether this capacitance itself exhibits history dependence and can act as a memory variable. This raises a related issue: if the defining electrical signature of an ideal memristor is a pinched hysteresis loop in the current–voltage plane, how is this signature modified when a memristive system also possesses a state-dependent capacitive response, and how should such behaviour be experimentally identified and quantified?

One of the earliest and most widely studied demonstrations of resistive-capacitive coexistence was reported in TiO_x/TiO_2-based memristive devices. In these systems, deviations from ideal memristor behaviour were consistently observed in the form of a non-zero crossing in the I–V hysteresis loop [72, 78, 79]. Such behaviour cannot be explained by resistance memory alone. Instead, it arises from transient charge accumulation and release within the device, which introduces a capacitive current component that becomes comparable to the conductive current when the timescale of charge redistribution approaches that of the applied voltage sweep. The resulting superposition of resistive and capacitive currents produces a hysteresis loop that does not pass through the origin, providing indirect but compelling evidence of a capacitive contribution coupled to the memristive state.

Building on this observation, Salaoru *et al.* demonstrated that memristive switching in TiO_x/TiO_2 devices is accompanied by well-defined capacitive switching when probed at appropriate frequencies [72]. Experimental results showed that similar SET and RESET voltages are required to induce both resistive and capacitive transitions, indicating that the LRS/HRS and HCS/LCS states are governed by a shared internal state variable rather than independent processes. In this study, the LRS was found to coincide with the HCS, while the HRS corresponded to the LCS, indicating an inverse correlation between resistance and capacitance. In a subsequent report by the same author, an opposite trend was observed, with HRS and HCS appearing together, as did LRS and LCS. These contrasting behaviours can be rationalised by considering the spatial distribution of crystalline defects such as oxygen vacancies and titanium interstitials, which strongly influence both electrical conductivity and dielectric permittivity in TiO_2. The formation, rupture, or partial dissolution of conductive filaments therefore modifies not only percolative current pathways, but also the effective

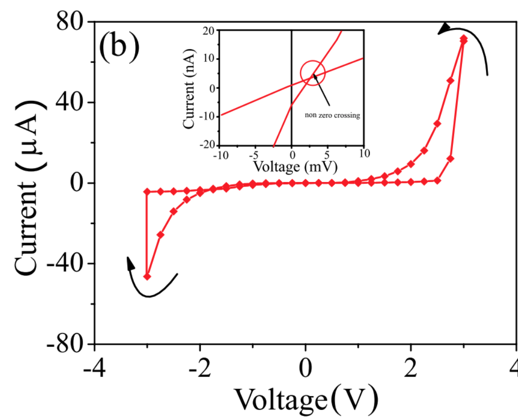

Figure 2.8: **Non-zero crossing I-V hysteresis**Current-voltage characteristics of a TiO_x/TiO_2 memristive device exhibiting bipolar resistive switching with a pronounced non-zero crossing of the hysteresis loop. The inset highlights the offset near the origin, indicating the presence of a capacitive component accompanying resistive switching, evidencing the coexistence of memristive and memcapacitive behaviour. Reproduced from [80].Copyright © 2013 AIP Publishing.

capacitive area and dielectric response of the device.

The coexistence of resistance and capacitance in memristive devices has been further verified through several radio-frequency (RF) applications employing memristors [81, 82]. A representative demonstration is provided by Shuang *et al.*, where a planar memristive device was implemented as a reconfigurable RF switch [83]. In this work, memristive RF switches exploit non-volatile resistance states together with intrinsically low OFF-state capacitance, enabling high cutoff frequencies without continuous power consumption. This application highlights that memristive devices do not operate as purely resistive switches at high frequencies, but instead function as coupled resistive–capacitive systems whose overall impedance is governed by the internal device state. Taken together, these observations demonstrate that memristive devices must be understood as dynamic impedance elements in which resistive and capacitive components are intrinsically linked and jointly governed by the same underlying physical mechanisms.

Importantly, both in RF applications and in previously reported capacitive switching studies, the resistive and capacitive contributions are explicitly treated as parallel elements within the active region, consistent with equivalent circuit models extracted from impedance spectroscopy. This naturally motivated the need for characterisation approaches capable of quantitatively separating and tracking resistive and capacitive contributions, as discussed in the following subsection.

2.3.2 Frequency-Domain Characterisation and Impedance-Based Analysis

Even though the memcapacitor was formally introduced in 2009, for a long time only theoretical application existed [84, 85, 15]. The vast majority of experimental work focused on resistance-based switching identified through direct current (DC) measurements. This emphasis is largely driven by the relative simplicity of DC characterisation, where resistive

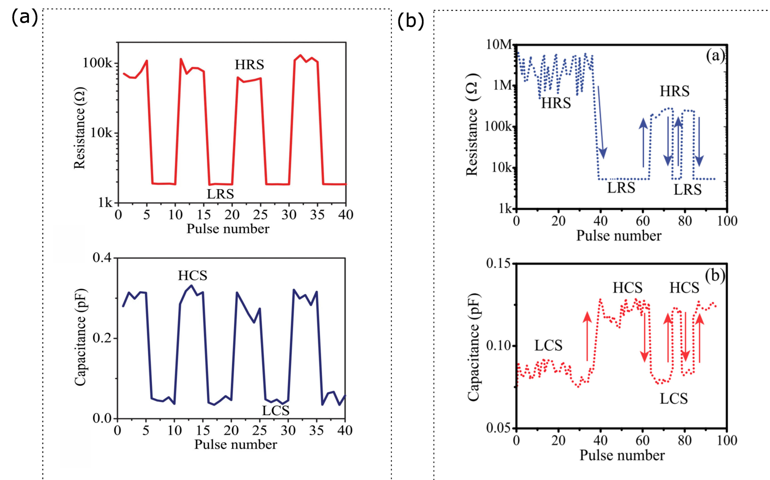

Figure 2.9: Pulse-induced resistive and capacitive switching characteristics illustrating different correlations between resistance and capacitance in TiO_x-based memristive devices. (a) Resistance and capacitance evolution showing correlated switching, where transitions between HRS and LRS are accompanied by corresponding transitions between HCS and LCS. (b) Resistance and capacitance evolution exhibiting an inverse relationship, in which LRS corresponds to HCS and HRS to LCS. Reproduced from [72, 80].Copyright © 2014 SpringerOpen, Copyright © 2013 AIP Publishing.

memory can be readily observed through I-V hysteresis. In contrast, the investigation of capacitance-based memory effects progressed more slowly, as capacitive responses are inherently dynamic, frequency-dependent, and highly sensitive to parasitic contributions arising from measurement setups, interconnects, and interfaces [10]. Distinguishing genuine memory-enabled capacitance from trivial geometric or parasitic effects therefore posed a significant experimental challenge.

Early efforts to explore frequency-dependent behaviour in memristive systems were largely restricted to transient analysis and single-frequency probing. While such approaches provided qualitative indications of LCS and HCS, they did not offer a systematic means of separating resistive and capacitive contributions, nor of quantifying how these evolve with device state. As research interest expanded toward high-frequency, reconfigurable, and analogue electronic applications, as discussed previously, this simplified treatment became increasingly inadequate.

Impedance spectroscopy emerged as a critical tool to address these limitations. By probing both the magnitude and phase of the electrical response over a broad frequency range, it provides direct access to the complex impedance of the device [10, 86]. When represented in the complex impedance plane, commonly referred to as a Nyquist plot, distinct contributions associated with bulk regions, interfaces, and localised conduction pathways can be resolved. This enables the construction of physically meaningful equivalent circuit models and provides insight into the internal kinetics governing memory behaviour. Importantly, impedance spectroscopy does not assume the coexistence of resistive and capacitive elements beforehand, but instead offers experimental validation of their presence. Consequently, a substantial body of literature has focused on extracting equivalent circuit representations, most commonly involving parallel combinations of resistance and capacitance, often augmented by series el-

ements to account for contact effects [87, 78]. A representative device is discussed below to illustrate this behaviour in detail; however, the observed device response is not limited to this example, and a wide range of equivalent circuit representations have been reported in the literature [71, 88, 89, 90, 79].

Device example: Impedance spectroscopy studies of filamentary HfO_x-based RRAM devices reveal that their electrical response cannot be captured by a single, fixed equivalent circuit, as reported by Bai et al. [8]. Temperature and frequency-dependent measurements performed in both the HRS and LRS demonstrated that distinct circuit representations are required across operating regimes, reflecting changes in the dominant conduction microdomains. In the LRS, the impedance response was best described by a parallel RC element in series with an inductive component, whereas in the HRS the response simplified to a dominant RC behaviour. These results highlight that even within a single material system, the effective equivalent circuit and in particular the role of capacitive elements can change substantially with the resistive switching state.

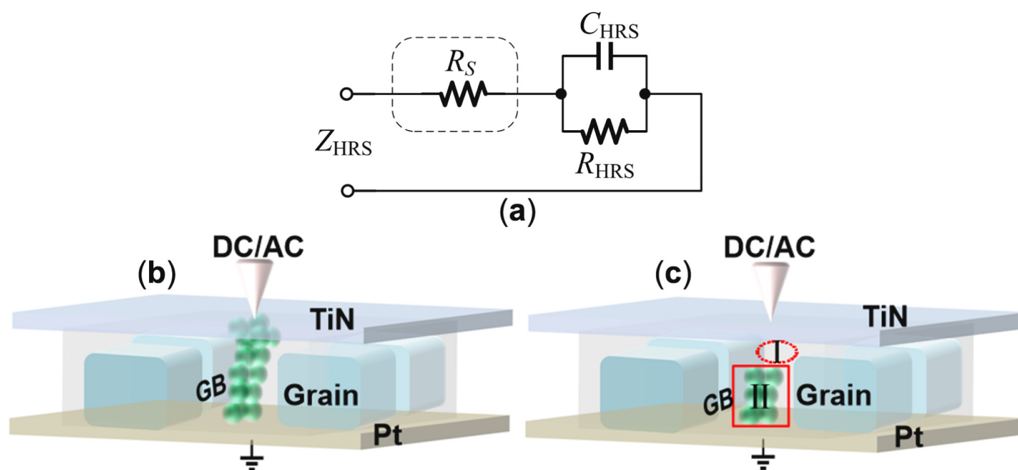

Figure 2.10: Equivalent circuit extracted from impedance spectroscopy and corresponding microscopic conduction model of a HfO_x-based RRAM device. (a) Impedance-derived equivalent circuit in the HRS, comprising a parallel R_{HRS}–C_{HRS} element in series with a contact resistance R_s. (b,c) Schematic illustration of the microscopic conduction pathways under combined DC/AC excitation, showing filamentary conduction in the LRS and grain-boundary-dominated transport in the HRS. Reproduced from [8].Copyright © 2022 Elsevier.

It shows that impedance spectroscopy serves a dual role in the investigation of memory-enabled devices. First, it provides direct insight into the physical origin of capacitive behaviour by resolving contributions from ionic motion, interfaces, and microstructural features. Second, it enables the construction of state-dependent equivalent circuit models that bridge device physics and circuit-level interpretation.

However, despite the widespread identification of capacitive elements in equivalent circuits, relatively few studies explicitly exploit or control capacitive switching as a functional memory variable. In many cases, capacitance is treated as a secondary component rather than as a programmable quantity in its own right [88, 89, 79, 10]. Hence, this thesis focuses not only on impedance spectroscopy as a characterisation tool, but also on the deliberate study of capacitive switching as an active device functionality.

2.3.3 Hafnium Oxide: A suitable Dielectric

From a circuit viewpoint, a practical memcapacitor can be understood as a capacitor that is always accompanied by some finite leakage resistance. In the high-resistance state, the device is expected to store charge and behave predominantly as a capacitive element. However, if the off-state resistance is not sufficiently large, the stored charge gradually leaks away through this resistance. The characteristic timescale for this leakage is given by the product of resistance and capacitance, $\tau = R_{\mathrm{OFF}}C$. As a result, even a large capacitance becomes functionally meaningless if the off-resistance is too low, since the capacitance state cannot be retained long enough to be read or exploited. In the low-resistance state, by contrast, conduction dominates the response and the capacitive contribution becomes secondary. This simple consideration highlights that meaningful memcapacitive behaviour requires not only a large capacitance, but also an adequately high off-state resistance.

This consideration highlights two key material requirements for a functional memcapacitor. First, the switching medium must exhibit a very large resistance ratio between HRS and LRS, ensuring that resistive leakage does not dominate the capacitive response. Second, the material should possess a high dielectric constant to achieve sizable capacitance within a small device footprint. Meeting both requirements simultaneously is intrinsically challenging, as materials that offer a high dielectric constant often do not exhibit sufficiently large resistance ratios, while systems with extreme resistance modulation typically possess relatively low permittivity. For instance, TiO_x can exhibit a high relative permittivity but typically offers a limited resistance ratio, whereas materials such as GeO_x, which demonstrate extremely large resistance ratios, often suffer from low dielectric constants, severely constraining achievable capacitance densities [70]. This intrinsic trade-off motivates careful material selection beyond conventional resistive switching oxides.

Within this context, hafnium oxide (HfO_x) emerges as a particularly attractive platform. HfO_x combines a decent dielectric constant with excellent scalability to nanometre thicknesses, enabling large capacitance densities in compact device geometries [91]. Moreover, post-deposition annealing has been shown to significantly enhance the resistive switching characteristics of HfO_x, leading to improved resistance ratios and switching stability [30, 92]. This provides a favourable pathway for simultaneously strengthening both the resistive and capacitive aspects of device behaviour. In this thesis, annealed HfO_x devices are therefore explored not only for optimised resistive switching, but also as a platform to systematically extend such optimisation toward controlled capacitive switching, as discussed in Chapter 4. In addition, HfO_x benefits from low-power operation, high endurance, and full CMOS compatibility, making it well suited for practical memory and analogue circuit integration [93, 94].

Building upon annealed HfO_x, an additional degree of functionality can be introduced through appropriate annealing and dopants that stabilises a ferroelectric phase in HfO_x [95]. Ferroelectricity provides an intrinsic route to electrically tunable and non-volatile capacitance through a polarisation-dependent dielectric response. This capability enables direct and programmable modulation of capacitance, positioning ferroelectric capacitors as a compelling and technologically viable platform for memcapacitor devices.

2.4 Ferroelectric Memcapacitor

This section reviews the origin and key physical properties of ferroelectric materials with a specific focus on hafnium–zirconium oxide (HZO) as a CMOS-compatible ferroelectric system. The discussion begins with a brief overview of classical ferroelectric materials and the technological limitations that constrained their large-scale integration. The emergence of HZO, is then introduced as a transformative development that has reshaped ferroelectric device research by enabling scalability and compatibility with advanced semiconductor processes. Building on this foundation, the physical origin of ferroelectricity in HZO is examined in terms of crystal structure, domain formation, and polarisation switching. Finally, the manifestation of these ferroelectric processes as non-volatile capacitance modulation is discussed, establishing the conceptual basis for ferroelectric memcapacitors as a recent and distinct device concept within the broader landscape of memory-enabled electronic components.

2.4.1 Evolution of Ferroelectric Materials Toward CMOS-Compatible Devices

Ferroelectric materials belong to the broader class of ferroic systems and are characterised by the presence of a spontaneous electric polarisation that emerges below a critical phase transition temperature. Crucially, the spontaneous polarisation can be reversibly switched between energetically equivalent states by an external electric field, providing an intrinsic mechanism for non-volatile information storage. Although ferroelectricity was theoretically anticipated and experimentally demonstrated in the early twentieth century in materials such as Rochelle salt and potassium dihydrogen phosphate, early ferroelectrics were limited by mechanical fragility, chemical instability, and poor compatibility with device fabrication.

Significant technological progress in ferroelectric devices was achieved with the development of perovskite compounds, most notably barium titanate ($BaTiO_3$), strontium titanate ($SrTiO_3$), lead zirconate titanate (PZT), with few more [96, 97]. These materials became the most widely used classical ferroelectrics owing to their perovskite crystal structure, large dielectric constants, and strong spontaneous and remanent polarisation. As a result, perovskite ferroelectrics enabled a wide range of early applications, including high-energy-density capacitors, sonar systems, electromechanical transducers, and non-volatile ferroelectric memories [98, 99, 100, 101]. In particular, PZT emerged as the material of choice for ferroelectric random-access memories (FRAMs) due to its favourable switching characteristics and reliable polarisation retention, representing a major milestone in the exploitation of ferroelectricity for information storage [102].

Despite their technological impact, perovskite ferroelectrics faced persistent challenges. High crystallisation temperatures, chemical and structural incompatibility with silicon, and degradation during standard CMOS processing steps collectively hindered their integration into advanced technology nodes [103, 104]. Also, PZT-based FRAM capacitors struggled to scale beyond the 130 nm node, while increasing regulatory restrictions on the use of lead further reduced their long-term viability for large-scale semiconductor manufacturing [105]. In parallel with these developments in perovskite ferroelectrics, hafnium and zirconium oxide were being extensively investigated as high-κ dielectrics for gate stacks and dynamic random-access memory capacitors [106, 107]. Their technological relevance stemmed from excellent thermal stability, large bandgaps, CMOS compatibiltity and low leakage currents at aggressively scaled thicknesses. This positioned hafnium and zirconium-based oxides as

materials of interest beyond conventional dielectric applications, enabling exploration of additional functional behaviour within a CMOS-compatible framework.

As part of this broader exploration beyond conventional dielectric functionality, the earliest demonstrations of ferroelectricity in HfO_2 were realised through silicon doping, which enabled stabilisation of a metastable, non-centrosymmetric orthorhombic phase under suitable processing conditions as shown in fig 2.11 [95]. Although this established hafnium oxide as a viable ferroelectric material, ferroelectric Si:HfO_2 remained constrained by its processing requirements. In particular, the stabilisation of the ferroelectric phase relied on relatively high crystallisation temperatures, imposing a large thermal budget that limited process flexibility and posed challenges for back-end-of-line integration [108].

Subsequent studies showed that the ferroelectric orthorhombic phase in hafnium oxide can be stabilised through the incorporation of a range of dopants, including Al, Gd, La, Si, and Zr [109, 108, 110, 111]. While these dopants modify the relative stability of competing structural phases, Gd and La still require comparatively higher crystallisation temperatures. In contrast, zirconium incorporation enables effective stabilisation of the ferroelectric phase at significantly lower crystallisation temperatures, leading to the development of HZO. As a result of this favourable balance between phase stability, process flexibility, and scalability, HZO has emerged as the most robust and technologically versatile hafnia-based ferroelectric [112, 113, 114, 115].

The discovery of ferroelectricity in HZO has revitalised the field of ferroelectric memories and enabled a new generation of CMOS-compatible ferroelectric devices. In contrast to classical perovskite ferroelectrics, hafnia-based materials exhibit robust ferroelectricity at nanometre-scale thicknesses, with ferroelectric phases stabilised in films as thin as $\sim$5–10 nm deposited by atomic layer deposition. These exceptional features have enabled the widespread adoption of HZO across multiple ferroelectric device architectures, including ferroelectric random-access memories (FRAM), ferroelectric tunnel junctions (FTJ), and ferroelectric field-effect transistors (FeFET) [116, 117, 118, 115, 119, 120]. Across these device concepts, information is stored in the orientation of the remanent polarisation within the HZO layer. The way this stored information is read, however, depends on the specific device architecture.

In FRAM, the ferroelectric layer is integrated into a capacitor structure, and the stored information is read out through the polarisation-dependent charge displacement that occurs during switching. This read operation directly senses the remanent polarisation state via the capacitor charge. In FTJ, the HZO layer is sufficiently thin to permit quantum-mechanical tunnelling. Polarisation reversal modifies the interfacial potential profile and effective tunnelling barrier height, resulting in a large change in electrical resistance that can be read without destructive switching. In FeFETs, the ferroelectric HZO layer is incorporated into the gate stack of a transistor. The polarisation state induces a persistent electric field at the semiconductor interface, leading to a non-volatile shift in the channel threshold voltage. Information is therefore stored as distinct transistor operating states and read out through standard current–voltage characteristics.

More recently, research efforts have increasingly focused on exploiting ferroelectricity in HZO for non-volatile capacitance modulation [121, 122]. Although ferroelectric capacitors inherently exhibit history-dependent dielectric responses, systematic investigation of this behaviour as a functional memory mechanism remains at an early stage.

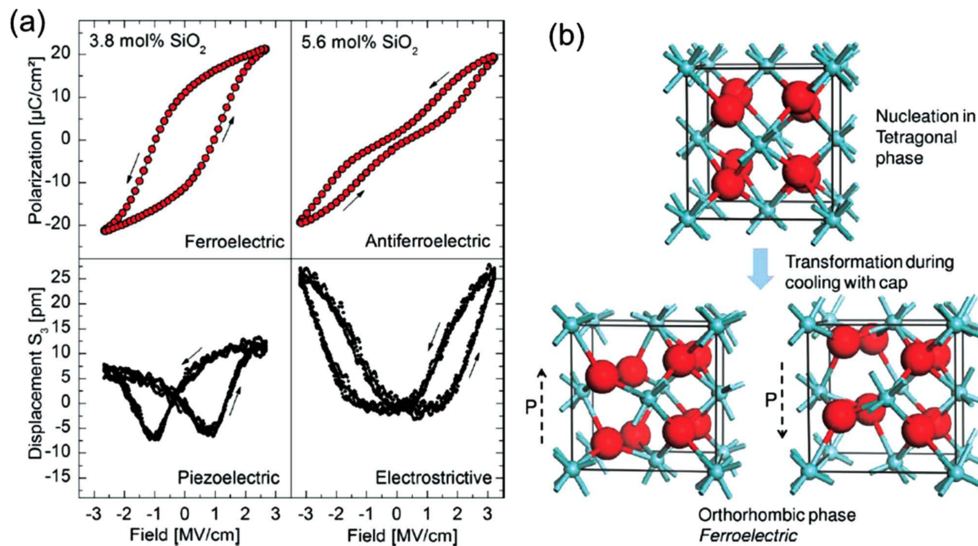

Figure 2.11: **Early demonstration of ferroelectricity in Si-doped HfO_2.** (a) Polarization-electric field and corresponding piezoelectric displacement responses measured from TiN/Si:HfO_2/TiN capacitors with varying SiO_2 concentrations. (b) The proposed phase evolution mechanism, where post-deposition annealing under mechanical confinement stabilises a non-centrosymmetric orthorhombic phase via transformation from the tetragonal phase. Reproduced from [95].Copyright © 2011 AIP Publishing.

2.4.2 Ferroelectricity in Hafnium-Zirconium Oxide

Under equilibrium conditions, bulk HZO crystallises predominantly in centrosymmetric monoclinic and tetragonal phases and does not exhibit ferroelectric behaviour. Ferroelectricity in HZO emerges only when a metastable orthorhombic phase is stabilised, most commonly associated with the non-centrosymmetric $Pca2_1$ space group [114]. In hafnia-based thin films, access to this ferroelectric phase requires careful control of processing conditions, including film thickness, mechanical constraint imposed usually by TiN electrodes, and post-deposition thermal treatment, typically achieved through rapid thermal annealing in the temperature range of approximately 400–600 °C [123, 124]. The orthorhombic phase breaks inversion symmetry through collective atomic displacements within the unit cell, giving rise to a spontaneous polarisation. As a direct consequence of their non-centrosymmetric crystal structure, ferroelectric materials are inherently piezoelectric. This electromechanical coupling underpins a wide range of applications in sensors, actuators, and transducers, and also plays an important role in probing ferroelectric behaviour at the nanoscale.

The non-centrosymmetric orthorhombic $Pca2_1$ phase of HZO supports a spontaneous polarisation along a crystallographic polar axis, with two energetically equivalent orientations of opposite sign. During crystallisation, different regions of the film can adopt either orientation, leading to the formation of polar domains. Ferroelectric behaviour in HZO therefore arises from the field-driven reorientation of these domains as shown in Fig. 2.12. Upon application of an external electric field, domains aligned with the field grow at the expense of oppositely polarised regions through domain nucleation and domain wall motion, resulting in a net macroscopic polarisation [125]. Reversal of the electric field drives switching of the domain orientation, giving rise to a switchable polarisation that is experimentally captured through

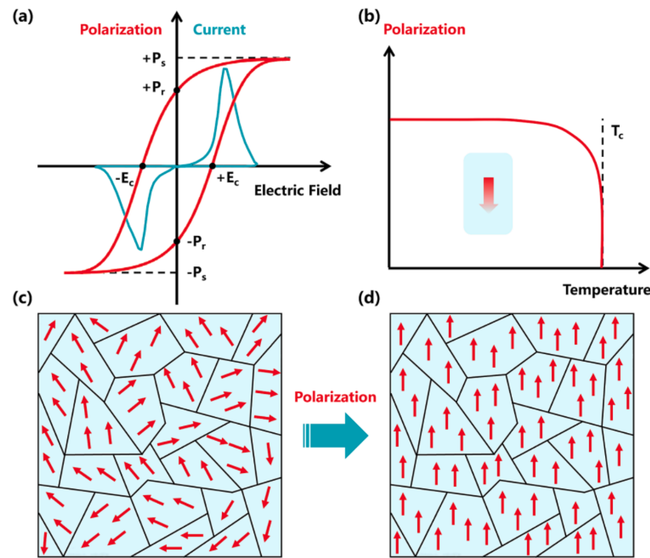

Figure 2.12: **Polarisation switching and domain evolution in ferroelectric materials.** (a) Schematic polarisation–electric field hysteresis loop with corresponding switching current, highlighting remanent polarisation and coercive field. (b) Temperature dependence of polarisation showing the ferroelectric-paraelectric phase transition at the Curie temperature. (c) Randomly oriented ferroelectric domains. (d) Domain alignment under an applied electric field leading to a saturated polarisation state. Reproduced from [125]. Copyright © 2025 Elsevier.

the characteristic polarisation–voltage (P–V) hysteresis response of ferroelectric capacitors.

The thermodynamic origin of this bistable polarisation can be described using Landau theory, in which the Gibbs free energy is expressed as a function of polarisation P as;

$$F(P) = \alpha P^2 + \beta P^4 + \gamma P^6 - EP,$$

where α, β, and γ are Landau expansion coefficients and E is the applied electric field. This free-energy landscape exhibits a double-well profile with two stable minima corresponding to remanent polarisation states [126, 127, 128]. Application of an external electric field tilts the energy landscape, lowering one minimum relative to the other and driving polarisation switching via domain evolution. Since the dielectric permittivity is inversely related to the curvature of the free energy, $\partial^2 F/\partial P^2$, each polarisation state is associated with a distinct capacitance, providing the physical basis for capacitive switching in ferroelectric HZO devices.

Importantly, during the transition between the two stable polarisation states, the energy landscape passes through a sequence of intermediate configurations, as illustrated schematically in Fig. 2.13. These intermediate states correspond to quasi-stable polarisation configurations that arise from partial domain switching and local energy minima in the tilted potential. While conventional ferroelectric memory operation exploits only the two global minima of the energy landscape, this thesis specifically explores the electrical accessibility and stability of these intermediate states and their manifestation as distinct capacitive levels during polarisation evolution

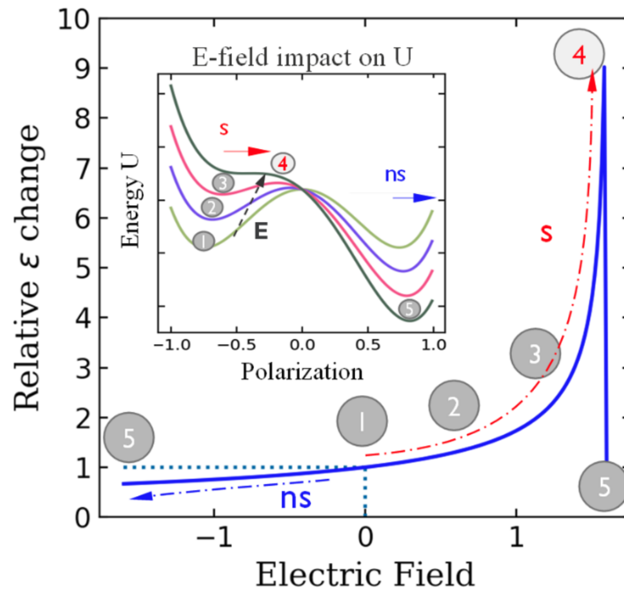

Figure 2.13: **Electric-field-induced evolution of the ferroelectric energy landscape.** The plot shows relative change in dielectric response as a function of applied electric field. The focus here is inset, that shows the potential energy U as a function of polarisation for different electric fields, illustrating the progressive tilting of the double-well landscape under bias. Reproduced from [126]. Copyright © 2022 IEEE.

2.4.3 Capacitance-Voltage Hysteresis

The butterfly-shaped capacitance-voltage (C-V) hysteresis is another characteristic electrical signature of ferroelectric capacitors and directly reflects the field-dependent dielectric response associated with polarisation switching [122, 129]. Peaks in the C-V curve typically occur in the vicinity of the coercive fields, where small changes in electric field induce large variations in polarisation due to active domain nucleation and domain wall motion.

In an ideal, symmetric ferroelectric capacitor with identical top and bottom electrodes and negligible defect influence, the butterfly curve is symmetric with respect to field polarity, and the capacitance values associated with oppositely polarised states merge at zero bias. In practical ferroelectric HZO capacitors, however, interfacial asymmetry, built-in electric fields, or non-uniform space-charge distributions can break this symmetry and give rise to asymmetric C-V characteristics as shown in Fig. 2.14. Such asymmetry shifts the crossing point of the butterfly curves away from zero bias, enabling a finite difference in capacitance between oppositely polarised states that can be read at zero applied voltage. This difference constitutes a non-volatile capacitive memory window and represents a fundamentally different mode of information storage compared to conventional polarisation-based readout, as the stored state can be accessed without state destruction [130]. Importantly, this capacitive memory window is not exclusively governed by defect-related effects. It can also be deliberately engineered through asymmetric electrode stacks, even in the absence of pronounced defect contributions [129, 130].

This capacitive memory window can be accessed in a manner analogous to ferroelectric

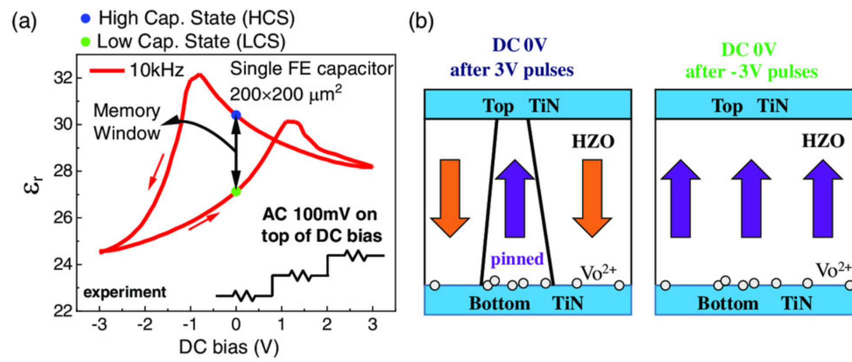

Figure 2.14: **Non-volatile capacitive memory window in ferroelectric HZO capacitors.** (a) Capacitance-voltage hysteresis measured from a single TiN/HZO/TiN ferroelectric capacitor, showing a non-volatile capacitive memory window readable at zero bias. (b) Physical mechanism underlying the capacitive memory window, highlighting asymmetric polarisation configurations. Reproduced from [131]. Copyright © 2022 Wiley.

polarisation itself, which is not intrinsically restricted to two discrete states. Rather than being limited to the two end points corresponding to fully polarised states, the butterfly-shaped C–V response reflects a continuous dielectric landscape that evolves during polarisation reversal, consistent with the Landau framework. As the applied bias is swept between the two coercive fields, the ferroelectric film passes through a series of intermediate domain configurations, each associated with a distinct polarisation distribution and, consequently, a distinct effective permittivity. These intermediate configurations are electrically accessible, enabling multiple, voltage-dependent capacitance states within the same device and giving rise to multilevel, or multibit, capacitive behaviour.

2.4.4 Multibit Capacitance Switching

Recent studies have demonstrated that intermediate capacitance states in ferroelectric HZO capacitors can be accessed using tailored voltage pulse schemes, enabling gradual and repeatable modulation of the capacitive state. Wu *et al.* demonstrated the realisation of eight distinct capacitance levels within a memory window of approximately 20 pF, where the incremental switching behaviour exhibited analog characteristics analogous to synaptic potentiation and depression as shown in Fig. 2.15 [121].

Subsequently, Wang *et al.* reported a wider and continuous capacitive memory window of 7.8 fF μm^{-2}, while Zhang *et al.* demonstrated a total memory window of approximately 40 pF with eight stable and well-separated capacitance states [14, 132]. Importantly, both studies further extended these concepts to array-level demonstrations and highlighted the relevance of ferroelectric memcapacitors for neuromorphic computing applications.

In comparison to resistive memory elements, capacitive devices offer several fundamental advantages that make them attractive for both neuromorphic and in-memory computing applications [133, 134]. Where resistive devices rely on steady-state current flow and therefore incur static power consumption, ferroelectric memcapacitors store information in programmable capacitance states that can be accessed at zero DC bias. As a result, power consumption in capacitive devices is predominantly dynamic, eliminating static leakage currents during read operations. In addition, the open-circuit nature of capacitors inherently

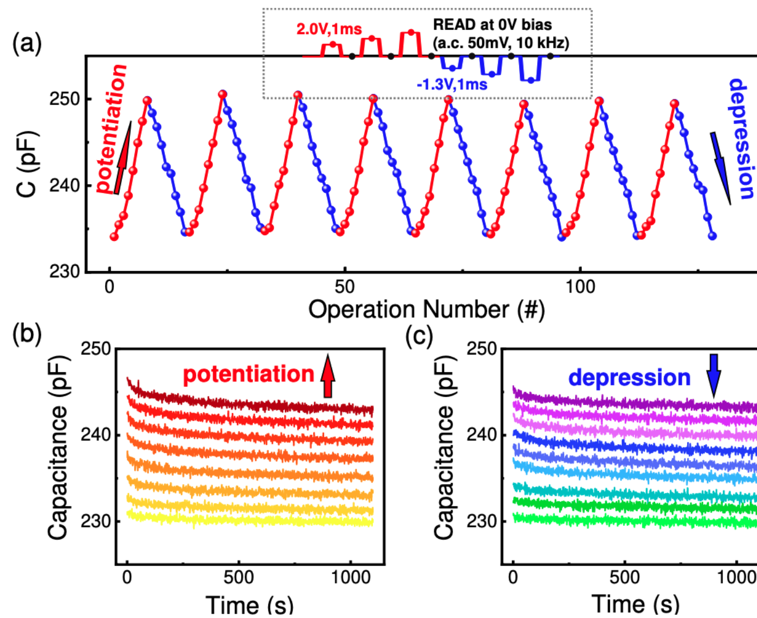

Figure 2.15: **Multilevel capacitive potentiation and depression in ferroelectric HZO capacitors.** (a) Reversible and repeatable modulation of capacitance under successive voltage pulse sequences, demonstrating potentiation (red) and depression (blue) with non-destructive readout at zero DC bias using a small AC signal. (b and c) Time evolution of multiple stable capacitance states accessed during potentiation and depression. Reproduced from [121].Copyright © 2024 AIP Publishing.

suppresses DC sneak-path currents and mitigates IR drop along interconnects, challenges that commonly limit the scalability and energy efficiency of resistive crossbar architectures [135]. Capacitive arrays therefore enable selector-free operation while maintaining stable and non-destructive readout of stored states. Together, the combination of low static power consumption, immunity to sneak paths, and compatibility with dense integration positions memcapacitor or specifically ferroelectric memcapacitors as a promising alternative to resistive devices for energy-efficient computing paradigms.

However, translating the intrinsic advantages of ferroelectric capacitors into reliable device operation remains challenging. At the material and device level, intrinsic ferroelectric phenomena such as wake-up, imprint, and fatigue strongly influence polarisation switching behaviour and can lead to temporal evolution of the dielectric response [136, 137]. From the perspective of capacitive switching, the existing literature remains comparatively limited. While a small number of recent studies have demonstrated the existence of a non-volatile capacitive memory window and the feasibility of accessing intermediate capacitance states, systematic investigations linking macroscopic C-V behaviour to microscopic domain configurations and local dielectric response are still scarce. In particular, the relationship between domain-scale switching processes, dielectric nonlinearity, and the stability of multilevel capacitance states has not yet been fully established. This gap motivates a systematic investigation of the underlying material and device-level issues, with the aim of elucidating and stabilising multilevel capacitive behaviour in ferroelectric HZO devices.

2.5 Conclusion

This literature review has established that memcapacitive behaviour can be realised through two distinct yet complementary physical pathways. The first arises from resistive switching systems, where memristive devices based on HfO_x exhibit history-dependent capacitive responses in addition to resistance modulation. Prior studies indicate that appropriate material and process engineering, particularly post-deposition annealing, can enhance the capacitive memory window and enable access to multiple capacitance states. These observations motivate a systematic investigation of memristor-based memcapacitors, with an emphasis on understanding the physical origin of capacitive switching, the number of accessible states, and the feasibility of developing equivalent circuit models that capture the coupled resistive-capacitive behaviour.

The second pathway is based on ferroelectric capacitors, enabled by the discovery of robust ferroelectricity in CMOS-compatible HZO. In contrast to resistive systems, ferroelectric capacitors provide a purely capacitive mechanism for non-volatile memory, where polarisation-controlled dielectric permittivity gives rise to a programmable capacitance landscape. The existing literature highlights the strong potential of HZO ferroelectric capacitors for multilevel operation through engineered capacitive memory windows. This motivates a focused investigation of ferroelectric memcapacitors, addressing how the capacitive memory window can be controlled, expanded, and reliably accessed for multiple states. Collectively, the studies reviewed in this chapter define the foundation for the experimental investigations presented in the subsequent chapters, which aim to establish a unified understanding of memcapacitive behaviour across both memristive and ferroelectric platforms.

Chapter 3

Device Fabrication and Thin film Analysis

This chapter outlines the complete experimental workflow used to fabricate and analyse the thin-film devices examined in this thesis, namely hafnium oxide (HfO_x) memristors and ferroelectric hafnium-zirconium oxide (HZO) capacitors. Section 3.1 introduces the fabrication framework, beginning with the lithographic mask set and proceeding through the sequence of metal and dielectric depositions, pattern transfers, and post-deposition annealing steps. Section 3.2 presents the thin-film analysis performed to verify that the deposited layers possess the structural and chemical integrity required for reliable device operation. These measurements establish the effect of post deposition annealing on the phase, stoichiometry, and functionality at film level. Together, the fabrication and film analysis presented in this chapter establish the link between processing conditions, resulting film structure, and the functional electrical behaviour explored in the subsequent chapters.

3.1 Fabrication Overview

All devices fabricated in this thesis follow a metal–insulator–metal (MIM) architecture, comprising a patterned bottom electrode (BE), an ultrathin dielectric layer, and a top electrode (TE). The lithographic mask set used to realise these structures, pre-designed and available within the research group for device fabrication, is shown in Fig. 3.1. It consists of three chromium-on-quartz masks, one for each device layer, and supports a wide range of device geometries with area 1×1 μm^2, 2×2 μm^2, 5×5 μm^2, 10×10 μm^2, 20×20 μm^2, 30×30 μm^2, 40×40 μm^2, 50×50 μm^2, and 60×60 μm^2. This mask design enables a unified fabrication platform capable of producing both HfO_x memristors and ferroelectric HZO capacitors. Table 3.1 summarises all device types fabricated using this mask set, including their material stacks and electrode configurations.

An overview of the complete fabrication workflow is illustrated in Fig. 3.2. In brief, three sequential lithography steps are used to define (i) the bottom electrode, (ii) the dielectric layer, and (iii) the top electrode. Between these patterning steps, material deposition is performed using sputtering and atomic layer deposition, followed by lift-off or etching as appropriate. Although Fig. 3.2 provides the overall process sequence, each individual step is

discussed in detail in subsequent subsections.

All devices were fabricated on 200 nm thermally grown SiO_2 on Si, produced by dry oxidation at 1050°C. This oxide thickness provides robust electrical isolation from the silicon substrate, eliminating parasitic leakage pathways and unwanted capacitive coupling that could otherwise interfere with the intrinsic electrical behaviour of the fabricated MIM structures.

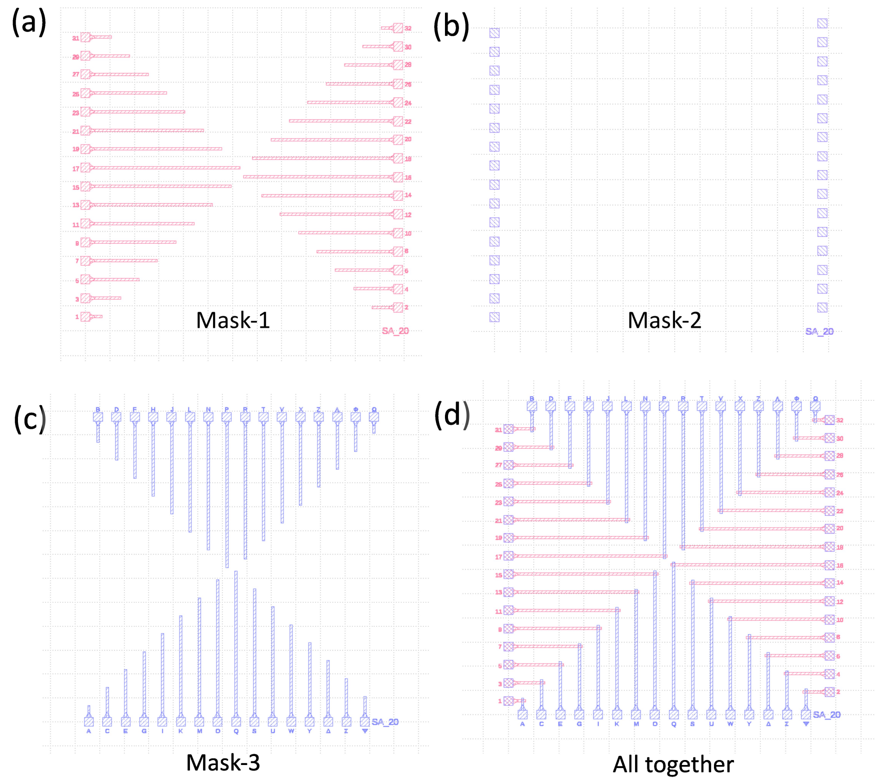

Figure 3.1: **Mask set used for fabricating the MIM device structures.** (a) Bottom electrode mask used to pattern the contact pads and define the bottom electrode extensions. (b) Middle-layer mask used to open the bottom electrode contact pads after dielectric deposition. (c) Top electrode mask, similar in design to the bottom electrode mask. (d) Overlay of all three masks showing the complete device layout. Each die contains 32 standalone MIM devices with varying line lengths and resistances.

3.1.1 Lithography

Lithography is the central pattern-definition step in the fabrication of all devices presented in this thesis [138]. It enables selective transfer of the mask design onto the wafer surface by using a photosensitive polymer called photoresist, a controlled ultraviolet (UV) exposure dose, and a corresponding alkaline developer solution. The fundamental role of the developer is to selectively dissolve regions of the resist whose chemical structure has been modified during UV exposure. The resulting patterned openings define where metals or dielectric layers will subsequently be deposited or removed.

Two classes of photoresists are used in microfabrication: positive and negative resists. Their

Table 3.1: Summary of fabricated device stacks used in this work.

Device ID	Bottom Electrode	Dielectric Layer	Top Electrode
D1	TiN	HfO_x (7nm)	TiN
D2	TiN	$Hf_xZr_yO_z$ (10nm)	TiN
D3	TiN	$Hf_xZr_yO_z$ (10nm)	Pt
D4	TiN	$Hf_xZr_yO_z$-MS (10nm)	TiN
D5	TiN	$Hf_xZr_yO_z$-Al (11nm)	TiN
D6	TiN	$Hf_xTi_yO_z$ (10nm)	TiN

MS denotes multilayer-stacked dielectric structures, while Al indicates Al-doped $Hf_xZr_yO_z$ films. The TE and BE electrodes are all 50nm in thickness.

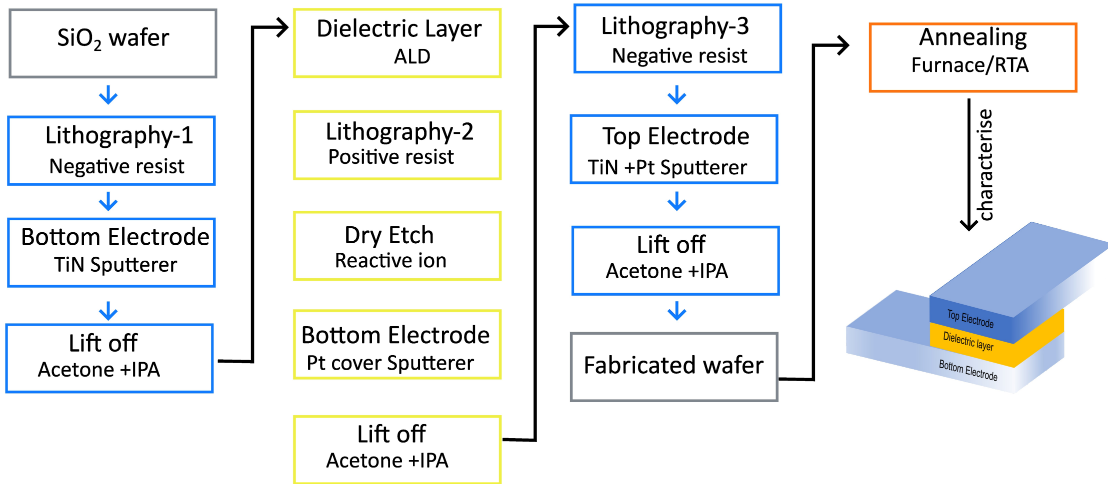

Figure 3.2: **Overview of the fabrication workflow used to realise the MIM device structures.** This flow illustrates the common backbone used for both HfO_x memristors and ferroelectric HZO capacitors, with differences arising in stack conditions and annealing conditions.

behaviour under UV illumination differs fundamentally. In a positive resist, UV exposure generates chemical fragments that increase solubility in the developer, meaning the illuminated regions are removed after development. Negative resists undergo cross-linking upon exposure, which decreases solubility, and therefore the unexposed regions are dissolved instead. The choice between these chemistries depends on the required feature size, the desired undercut profile, and the lift-off behaviour needed for subsequent metallisation. Positive resists generally provide superior resolution and more vertical profiles, whereas negative resists naturally form an undercut, which is advantageous for metal lift-off but introduces additional care in exposure optimisation to avoid pattern broadening.

In this thesis, both positive and negative photoresists were used depending on the layer being patterned. The negative resist AZ 2035 was selected for electrode definition, as its inherent sidewall profile provides a controlled undercut that improves lift-off reliability for sputtered titanium nitrate (TiN). For the patterning of HfO_x and HZO layers deposited by ALD, the positive resist SPF 220.3 was used and is discussed in detail in later section. All lithography exposures were performed using a Karl Suss mask aligner equipped with a mercury lamp that emits a broadband spectrum containing both the I-line (365 nm) and G-line (436 nm). The

tool allows installation of I-line or G-line filters when a narrower spectral band is required for improved process control. The lithographic workflow was tailored to the thermal, chemical, and optical constraints of each resist system, and the corresponding spin speeds, exposure doses, and development conditions are summarised in Table 3.2. These parameters were experimentally optimised to ensure consistent pattern fidelity across all device sizes, with the smallest features defining the overall process window. Together, these lithography protocols define all three levels required for device fabrication with high dimensional accuracy.

Table 3.2: Lithography process parameters for the negative-tone (AZ 2035) and positive-tone (SPF 220) photoresists used in this thesis.

Process Step	**AZ 2035 (Negative)**	**SPF 220.3 (Positive)**
Spin coating	3500 rpm	3500 rpm
Pre-exposure bake	100°C for 60 s	115°C for 90 s
UV exposure dose	45 s at 365 nm	15 s at 365 nm
Post-exposure bake	100°C for 60 s	115°C for 90 s
Development	AZ 726 MIF, 60 s	MF 26A, 90 s

3.1.2 Metal Electrode Deposition using Sputterer

Sputtering is a plasma-based physical vapour deposition process in which energetic ions from an ionised gas are accelerated towards a target material, resulting in the ejection of target atoms through momentum transfer. These ejected atoms subsequently travel through the chamber and condense on the substrate to form a thin film. In most thin-film deposition processes, argon (Ar) is used as the sputtering gas due to its chemical inertness, low cost, and atomic mass comparable to that of many technologically relevant metals, enabling efficient momentum transfer during ion bombardment. The ion energy is primarily determined by the potential drop between the plasma and the target surface, which governs the sputtering yield and film growth characteristics. Depending on the electrical properties of the target material and the desired film morphology, the plasma may be sustained using DC or RF excitation, while reactive sputtering employs the introduction of a reactive gas to enable compound film formation [139].

TiN films in this work are deposited using reactive DC sputtering, where nitrogen gas is introduced alongside Ar. Nitrogen reacts with Ti atoms ejected from the target, forming a TiN compound layer directly on the substrate. This enables precise control of film stoichiometry, electrical conductivity, and stress, all of which are critical for the performance of MIM structures. TiN electrodes are deposited at a working pressure of 2 mTorr, 600 W power, and a nitrogen flow of 20 sccm with Ar as the sputtering gas. Platinum (Pt) films were deposited using RF sputtering rather than DC sputtering. Although Pt is a conductive metal, DC sputtering of Pt can lead to plasma instability, target heating, and micro-arcing due to its high atomic mass and relatively low sputter yield, particularly under the low-pressure and low-rate conditions required for thin electrode layers. RF sputtering mitigates these effects by sustaining a stable plasma through an alternating electric field, enabling improved control over ion bombardment energy and deposition rate. In this work, RF-sputtered Pt was employed as a thin capping layer on TiN to suppress oxidation during subsequent high-temperature annealing steps. The 10 nm Pt layer was deposited using RF sputtering at a power of 200 W in an Ar ambient with a flow rate of 25 sccm and a chamber pressure of 30 mTorr.

3.1.3 Dielectric Layer by Atomic Layer Deposition

Atomic layer deposition (ALD) is used to grow ultrathin HfO_x and HZO dielectric layer with precise control over thickness, uniformity, and chemical composition. ALD operates through a sequence of discrete, self-limiting surface reactions, allowing the film to be constructed one molecular layer at a time. Each ALD cycle consists of a precursor exposure, a purge, an oxidant exposure, and a second purge. During the first half-cycle, the metal precursor is introduced into the reactor and chemisorbs onto surface hydroxyl groups through ligand-exchange reactions. Chemisorption continues only until all available reactive sites become saturated, at which point further adsorption is not possible. The chamber is then purged with an inert carrier gas to remove unreacted precursor molecules and volatile ligand by-products, thereby preventing any gas-phase reactions that would break the self-limiting nature of the process. In the second half-cycle, an oxidant such as water vapour is pulsed into the chamber. The oxidant reacts with the chemisorbed precursor fragments, replacing the organic ligands and forming metal–oxygen bonds. This reaction also regenerates hydroxyl groups on the surface, restoring the chemical functionality required for subsequent cycles. A final purge removes excess oxidant and reaction products, ensuring that each phase of the cycle remains limited by surface chemistry rather than the gas-phase environment. Because both half-reactions terminate naturally upon surface saturation, the amount of material deposited per cycle remains nearly constant. This behaviour enables sub-nanometre thickness precision, excellent conformality, and highly uniform deposition, even across topographically varied device features [140].

ALD processes can be implemented in several forms depending on how the oxidant is activated. In thermal ALD, the precursor and oxidant react solely through thermally driven surface chemistry, yielding smooth films with well-controlled stoichiometry. Plasma-enhanced ALD replaces the molecular oxidant with a plasma, increasing the reactivity of the surface reactions and enabling deposition at lower temperatures, although the presence of energetic ions can introduce defects or alter bonding environments in ultrathin oxide layers. Ozone-assisted ALD uses O_3 as a highly reactive oxidant that enhances ligand removal and improves film density; however, its strong oxidising behaviour can modify local bonding configurations in mixed-metal systems such as hafnium–zirconium oxides. Among these variants, thermal ALD was used for thin film deposition.

There are four metal precursors used in this thesis: tetrakis(dimethylamido)hafnium (IV) (TDMAHf), tetrakis(dimethylamido)zirconium (IV) (TDMAZr), tri(methyl)aluminium (TMA), and tetrakis(dimethylamido)titanium (TDMAT). TDMAHf, TDMAZr and TDMAT are delivered from heated bubblers maintained at approximately 75°C to ensure sufficient vapour pressure and stable precursor flow. In contrast, TMA is introduced at room temperature bubbler because it is intrinsically highly volatile and reacts readily even without additional thermal activation; heating would raise its vapour pressure to a level that would compromise safety measures. All dielectric films are deposited at a substrate temperature of 250°C, which lies within the optimal ALD temperature window for stable self-limiting growth. This temperature is primarily determined by the thermal stability and reaction kinetics of the metal-organic precursors used during film growth. Higher deposition temperatures can lead to precursor decomposition, increased film roughness, enhanced defect formation, and may induce partial crystallisation of the film. In contrast, amorphous films are preferred at the deposition stage to allow controlled crystallisation during the subsequent annealing step. Higher temperatures may also favour the formation of the non-ferroelectric monoclinic phase in HZO, which is

undesirable. It is also worth noting that the Curie temperature of ferroelectric HZO lies in the range of ∼400–600°C; however, since the as-deposited films are initially amorphous and become ferroelectric only after rapid thermal annealing, this does not impose a constraint on the deposition temperature [141].

For HfO_x-based devices, the dielectric layer is deposited using TDMAHf and H_2O precursors, forming uniform amorphous HfO_x films that serve as the functional dielectric in memristive devices. Ferroelectric capacitors employ HZO as the functional dielectric and are realised in three principal configurations: a baseline HZO stack, a multilayer HZO-MS stack, and an Al_2O_3-modified HZO-Al stack. The baseline HZO film is realised using a supercycle scheme in which HfO_x and ZrO_x sublayers are alternated to achieve the target composition. A typical implementation employs a 1:1 sequence of HfO_x:ZrO_x cycles, repeated until the desired thickness is reached. This approach ensures atomic-scale mixing while preserving the composition known to stabilise the ferroelectric orthorhombic phase upon rapid thermal annealing. The supercycle methodology further enables direct control over the Hf:Zr ratio without reliance on co-injection or plasma activation, improving reproducibility across wafers and fabrication runs.

In the HZO-MS configuration, the film is constructed from repeated blocks of HfO_x and ZrO_x, for example five cycles of HfO_x followed by five cycles of ZrO_x. This nanolaminate architecture introduces additional internal interfaces that may influence crystallisation pathways, internal stress, domain formation, and defect distribution, allowing systematic examination of how nanoscale layering affects ferroelectric switching behaviour, endurance, and wake-up effects. The HZO-Al variant incorporates an ultrathin Al_2O_3 layer, approximately 1 nm thick, inserted near the centre of the HZO stack. This is achieved by introducing a short TMA/H_2O ALD sequence within the main HZO supercycle. The Al_2O_3 insertion locally modifies the internal electric-field distribution and defect landscape, providing an additional degree of control over wake-up behaviour, polarisation stability, and long-term retention.

In addition to HfO_x and HZO, hafnium-titanium oxide (HTO) films were fabricated as part of process development. As these structures are not incorporated into the memristive or ferroelectric devices analysed in this thesis, their fabrication details and preliminary characterisation are presented separately in the Appendix along with a few other fabricated devices. A summary of all dielectric stacks and their corresponding ALD schemes is provided in Table 3.3. While exact cycle counts and film thicknesses may vary between fabrication runs, the precursor chemistry, supercycle methodology, and overall design strategy remain consistent across all wafers.

Table 3.3: Summary of ALD dielectric stacks used in this thesis.

Stack	Precursors	Cycle / supercycle scheme
HfO_x	TDMAHf + H_2O	cycle for desired thickness
HTO	TDMAHf, TDMAT + H_2O	(HfO_x:TiO_x) supercycles (1:1)
HZO	TDMAHf, TDMAZr + H_2O	(HfO_x:ZrO_x) supercycles (1:1)
HZO-MS	TDMAHf, TDMAZr + H_2O	(HfO_x:ZrO_x) supercycles (5:5)
HZO-Al	TDMAHf, TDMAZr, TMA + H_2O	HZO (1:1)/ Al_2O_3 (1 nm) / HZO (1:1)

3.1.4 Lift-off, Etching and Annealing

Lift-off: Lift-off is an essential post-deposition process used to remove the photoresist layer together with any metal or dielectric material deposited on top of it, thereby revealing the patterned features underneath. After metal deposition, the wafer is immersed sequentially in acetone and isopropyl alcohol (IPA), each for approximately five minutes in a room-temperature ultrasonic bath. The solvent penetrates the resist–film interface and dissolves the photoresist, while ultrasonic agitation accelerates the detachment of the overlying material. Following the lift-off step, the wafer is rinsed with DI water and dried with nitrogen to ensure that no residue remains in the patterned areas.

Etching of ALD dielectric films: Unlike sputtered dielectrics, ALD films are fully conformal and coat not only the intended areas but also the resist sidewalls and the regions intended to remain open. For this reason, ALD films cannot be removed through a standard solvent lift-off procedure. Instead, a blanket ALD deposition is first performed across the entire wafer, and the dielectric is subsequently patterned by etching. To access the bottom electrode post ALD film, a positive photoresist is patterned using the mask-2 in the lithography. In this configuration, the photoresist protects the dielectric everywhere except above the intended contact pads. The exposed dielectric was then removed using a CHF_3/Ar-based reactive ion etching (RIE) process operated at 100 W power, with a CHF_3 flow rate of 20 sccm, and a chamber pressure of 25 mTorr. This process selectively removes the oxide layer, exposing the underlying metal electrode while leaving the resist-protected regions intact. Once the etching step is complete, the photoresist is stripped using the same solvent lift-off procedure described above. This etch-back strategy provides a reliable method to access the electrode surfaces beneath conformal ALD films while maintaining the integrity of the dielectric in the active device areas.

Post-deposition annealing: Two annealing approaches are used in this work, depending on the targeted device behaviour and material composition. For HfO_x devices, furnace annealing is employed to induce crystallisation or partial ordering within the dielectric film. The wafer is annealed in a nitrogen ambient using a slow temperature ramp of 5 °C/min up to 400 °C, where it is held for 1 minute. After the dwell step, the sample remains in the furnace until the temperature passively cools to approximately 200 °C before removal. In contrast, HZO films intended for ferroelectric capacitors require rapid thermal annealing (RTA) to stabilise the non-centrosymmetric orthorhombic phase responsible for ferroelectricity. RTA is carried out at 500 °C for 30 s in an ambient nitrogen environment, providing a high-temperature spike of sufficiently short duration to drive the desired phase transformation while suppressing the formation of competing monoclinic or tetragonal phases.

3.2 Thin-Film Material Characterisation

The intrinsic material properties of the deposited dielectric and ferroelectric films were examined using X-ray photoelectron spectroscopy (XPS), X-ray diffraction (XRD), and atomic force microscopy (AFM), each providing a distinct but complementary insight into film behaviour. XPS and XRD were performed on both HfO_x and $HfZrO_x$ films, whereas AFM-based measurements were carried out only on the ferroelectric HZO films. In addition to thin-film material analysis, the structural fidelity of the fabricated devices was verified through optical

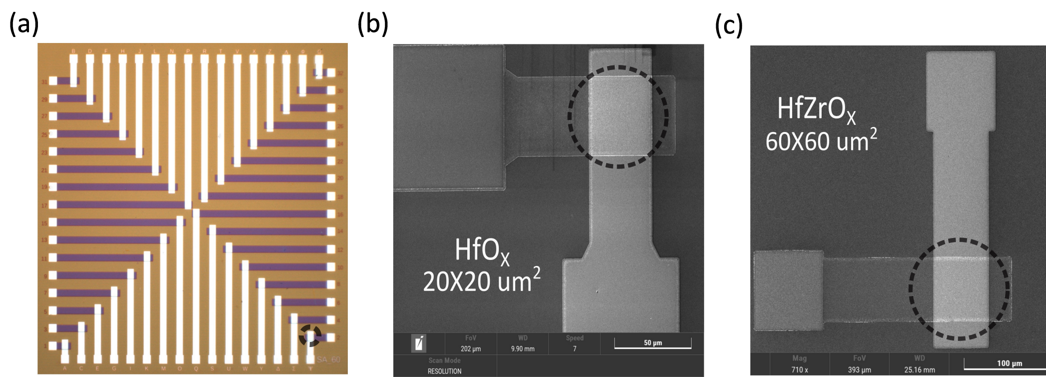

Figure 3.3: **Device layout and SEM images of fabricated MIM capacitors.** (a) Optical micrograph of the full MIM test structure used for electrical characterisation. (b) SEM image of a fabricated HfO_x capacitor (20×20 μm^2), showing the top-electrode pad and underlying device region. (c) SEM image of a fabricated $HfZrO_x$ capacitor (60×60 μm^2) with the same overall geometry. In both structures, the capacitor area (dashed circle) and contact routing are clearly defined, confirming uniform pattern transfer and successful electrode formation.

microscopy and SEM imaging (Fig. 3.3). These images confirm uniform pattern transfer, clean electrode definition, and well-resolved device geometries across both HfO_x and HZO stacks, providing confidence that the electrical measurements presented later arise from intrinsic material behaviour rather than fabrication artefacts. All measurements were performed on test samples consisting of a TiN bottom electrode and dielectric layers with the same thickness as specified in Table 3.1.

3.2.1 X-ray Photoelectron Spectroscopy (XPS)

XPS was used to assess the stoichiometry and chemical bonding environments of the dielectric films before and after annealing. Measurements were performed using a Thermo Scientific NEXSA G2 system equipped with a monochromated Al Kα source (1486.7 eV). Owing to the limited escape depth of photoelectrons, XPS probes the near-surface region of the film, typically corresponding to an information depth of approximately 8–10 nm. This depth is commonly described in terms of the effective attenuation length (λ) of the emitted electrons, where roughly 60% of the signal originates from the top $\sim \lambda$ of the material and about 95% from within $\sim 3\lambda$. Prior to spectral acquisition, a gentle surface-cleaning step was carried out using an argon cluster ion beam (4 keV, 1000 atoms, 30 s) to minimise surface carbon contamination without significantly altering the near-surface chemistry. Survey spectra and high-resolution scans were collected to analyse the elemental composition and chemical states of Hf, Zr, and O.

HfO_x: For HfO_x thin films, XPS was used to determine whether thermal treatment alters the oxygen coordination or cation bonding environment in a manner that could influence memristive behaviour. Figure 3.4(a,b) shows the Hf 4f spectra, which exhibit the characteristic spin–orbit doublet corresponding to the Hf $4f_{7/2}$ and Hf $4f_{5/2}$ states, separated by 1.66 eV. This splitting is slightly lower than reported values for fully stoichiometric Hf–O bonding, suggesting subtle variations in local bonding configuration or the presence of mildly

sub-stoichiometric regions. The O 1s spectra can be deconvoluted into two components separated by 1.99 eV, corresponding to lattice oxygen and non-lattice oxygen states. Notably, the relative intensities and binding energies of these components remain essentially unchanged after furnace annealing, indicating that annealing at 400 °C does not significantly modify the overall film stoichiometry. As carbon-related features are reduced following the cluster-cleaning step while other peak characteristics remain unchanged, any differences in electrical behaviour between as-deposited and annealed HfO_x films can be attributed primarily to microstructural evolution rather than changes in chemical composition.

HZO: For HZO-based films, XPS was employed to evaluate cation stoichiometry, oxidation states, and oxygen bonding environments, as shown in Figure 3.4(c–f). As XPS probes only the top few nanometres of the surface, the measured composition primarily reflects the near-surface region of the ALD-grown film. Because the HZO-MS nanolaminate and baseline HZO films share the same global Hf:Zr ratio and differ only in stacking order, both architectures yield equivalent XPS signatures in the absence of sputter-depth profiling. Consequently, a single representative HZO film is analysed to characterise the chemical state of all HZO variants. The extracted Hf:Zr quantitative fitting is close to 1:1 ratio, as shown in Figure 3.4(c), consistent with the intended ALD supercycle design. This composition is widely regarded as optimal for stabilising the orthorhombic ferroelectric phase in HZO upon annealing. The Hf 4f spectrum exhibits a sharp spin–orbit doublet with a splitting of approximately 1.6 eV, comparable to that observed in HfO_x films. Similarly, the Zr 3d core-level spectrum shows well-defined Zr $3d_{5/2}$ and Zr $3d_{3/2}$ peaks separated by 2.4 eV, characteristic of the Zr^{4+} oxidation state.

The O 1s spectrum for HZO shows a dominant lattice-oxygen peak with a weaker defect-related shoulder, closely resembling the line shape observed in HfO_x films. This similarity is expected, as oxygen in HZO occupies comparable coordination environments to those in pure HfO_x, and the incorporation of Zr does not substantially shift the O 1s binding energy. Consistent with the cation spectra, the O 1s peak positions remain unchanged after RTA (500 °C, 30 s), indicating that annealing preserves overall stoichiometry while primarily driving the structural transition toward the ferroelectric orthorhombic phase.

3.2.2 X-ray Diffraction (XRD)

XRD enables distinction between amorphous and crystalline films by revealing Bragg diffraction peaks associated with long-range crystallographic order. As such, it complements the XPS analysis by revealing how crystallographic phases evolve upon annealing. Measurements were performed using a Panalytical Empyrean diffractometer operated in grazing-incidence mode with Co Kα radiation (λ = 1.7886 Å). Grazing-incidence XRD (GIXRD) enhances surface sensitivity by suppressing substrate contributions, making it particularly suitable for ultrathin films.

HfOx: For HfO_x films, XRD is employed to examine the structural evolution before and after thermal annealing. As shown in Fig. 3.5(a), the as-deposited films exhibit no discernible diffraction peaks, confirming a predominantly amorphous structure and the absence of long-range atomic order immediately after deposition. Following post-deposition annealing, the emergence of distinct but relatively broad diffraction features indicates the onset of crystalli-

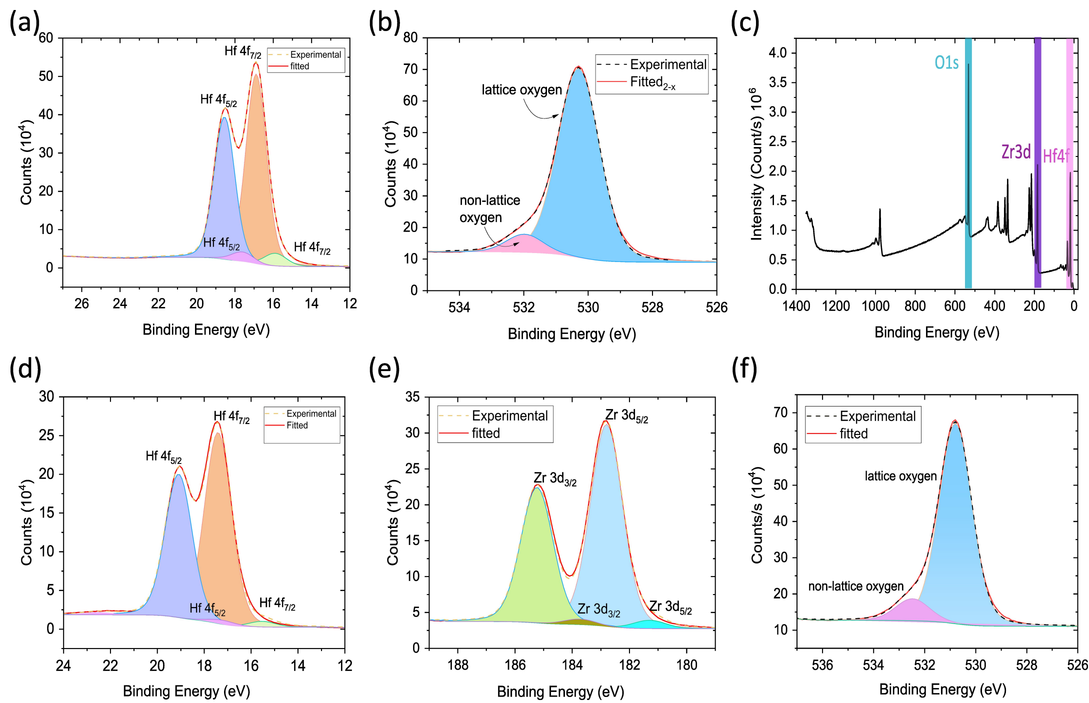

Figure 3.4: **XPS analysis of HfO_x and HZO films.** (a–b) High-resolution Hf 4f and O 1s spectra for as-deposited and annealed HfO_x, showing the characteristic Hf 4f doublet and lattice/non-lattice oxygen components. (c) Survey scan of an HZO film identifying 1:1 cation ratio and oxygen. (d–f) High-resolution Hf 4f, Zr 3d and O 1s spectra for HZO, confirming respective oxidation states, and lattice-oxygen dominated bonding with a minor defect-related contribution.

sation within the film. The broad peak widths suggest that the annealed films do not undergo complete crystallisation, but instead consist of a heterogeneous microstructure comprising nanocrystalline regions embedded within an amorphous matrix.

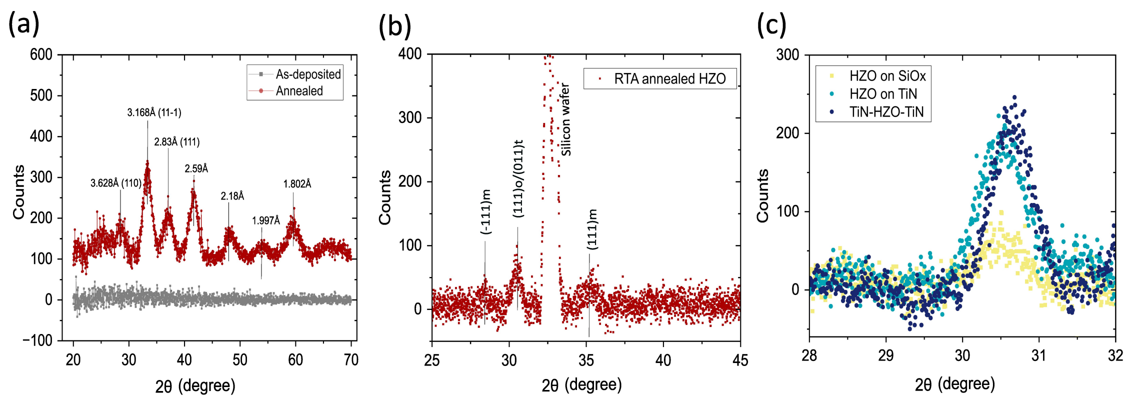

Figure 3.5: **Grazing-incidence XRD analysis of HfO_x and HZO films.** (a) XRD patterns of as-deposited and annealed HfO_x showing crystallisation into the monoclinic phase after annealing. (b) RTA annealed HZO exhibiting the characteristic orthorhombic ferroelectric peak. (c) Influence of substrate-electrode stack on orthorhombic phase formation for HZO.

The dominant diffraction feature corresponds to the $(11\bar{1})$ reflection associated with monoclinic HfO_2, is the thermodynamically stable phase at room temperature and is therefore

expected to form preferentially upon annealing [30, 142]. While signatures of tetragonal or orthorhombic phases have also been reported in similarly processed films [143], their contribution here appears secondary and insufficient to define the overall structural response. The coexistence of multiple diffraction features, together with peak broadening and reduced peak intensity, points toward a mixed-phase or structurally disordered film rather than a well-defined single crystalline phase. This mixed amorphous-crystalline nature can be effectively described using composite structural models, such as those proposed by Yamazaki *et al.* [144], where nanocrystalline inclusions are embedded within an amorphous host. From a device perspective, such structural inhomogeneity is particularly relevant, as it can influence defect distribution, local electric fields, and charge transport pathways. Consequently, the structural changes induced by annealing are expected to play a key role in governing the electrical and memcapacitive behaviour discussed in subsequent chapters.

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HZO: In contrast to HfO_x, XRD analysis of HZO films serves a broader purpose. Beyond verifying crystallisation, it enables identification of the ferroelectric orthorhombic phase and allows assessment of how substrate choice, electrode materials, and device geometry influence phase stability. As such, XRD provides a direct structural link between processing conditions and the ferroelectric properties discussed later in this thesis. Figure 3.5(b) shows the GIRXD pattern of HZO films subjected to RTA. A weak but clearly identifiable diffraction feature appears near 30.5°, corresponding to the $(111)_o/(001)_t$ family of reflections associated with the non-centrosymmetric orthorhombic $Pca2_1$ phase [145, 146]. Although the peak intensity is modest, as expected for ultrathin HZO films, its presence confirms that a fraction of the film transforms into the ferroelectric orthorhombic phase upon annealing. The simultaneous presence of monoclinic, tetragonal, and orthorhombic contributions indicates a mixed-phase microstructure, consistent with prior reports.

To investigate the role of substrate and electrode boundary conditions, HZO films were deposited on three different stacks: (i) SiO_x, (ii) TiN bottom electrode only, and (iii) symmetric TiN/HZO/TiN capacitors. The corresponding evolution of the orthorhombic peak intensity is shown in Fig. 3.5(c). A systematic increase in peak intensity is observed when progressing from SiO_x to TiN-supported films, with the strongest orthorhombic signature obtained for the fully symmetric TiN/HZO/TiN stack. This trend can be attributed to a combination of factors, including mechanical confinement imposed by TiN electrodes, stress arising from thermal expansion mismatch during annealing, and favourable interface energetics at the TiN/HZO boundary. Together, these effects promote stabilisation of the orthorhombic phase while suppressing relaxation into the monoclinic ground state. This behaviour is consistent with literature reports demonstrating that metal electrodes, particularly TiN bottom layers, enhance ferroelectric phase formation by imposing in-plane stress [147]. Consequently, the XRD results provide direct structural evidence linking phase composition to device-level ferroelectric and memcapacitive performance.

3.2.3 Atomic Force Microscopy (AFM)

AFM was employed to probe the nanoscale functional behaviour of HZO films using two specialised modes: piezoresponse force microscopy (PFM) and electrostatic force microscopy

(EFM). PFM enables spatially resolved mapping of ferroelectric switching behaviour, while EFM is used to examine the stability and tuneability of stored charge. Together, these techniques provide a nanoscale perspective on the mechanisms underlying memcapacitive behaviour.

Measurements were carried out using a Park Systems NX20 atomic force microscope equipped with a conductive PPP-CONTSCPt probe. All measurements were performed on samples prepared in a half-stack configuration consisting of the TiN bottom electrode and the HZO film. To ensure a well-defined electrical pathway for PFM and EFM operation, one side of the sample was selectively etched to expose the TiN bottom electrode, which was subsequently connected to the metallic sample holder using conductive silver paste.

Both PFM and EFM measurements were performed using the instrument's internal lock-in amplifier. The AC excitation frequency was set to 17 kHz, well below the mechanical modulation frequency, with a time constant of 100 ms and a sensitivity setting of 0.1 V. An AC drive amplitude of 10 V was used throughout. This value was found to be essential for reliable signal acquisition, as lower AC voltages produced weak or no observable contrast in both amplitude and phase, whereas a 10 V excitation ensured a sufficiently strong electromechanical and electrostatic response while avoiding excessive perturbation of the written domains. All measurements were performed under identical conditions to enable consistent comparison across different biasing protocols and switching experiments.

Piezoresponse Force Microscopy (PFM)

For PFM measurements, a conductive tip applies a combined DC and AC voltage to the sample surface, and the resulting electromechanical deformation arising from the piezoelectric effect is detected through the cantilever deflection. The applied tip voltage can be written as;

$$V(t) = V_{\text{DC}} + V_{\text{AC}} \cos(\omega t), \tag{3.1}$$

where V_{DC} is the static bias used to switch the material and V_{AC} is the probing bias applied at angular frequency ω. The sample deformation at the driving frequency produces an oscillatory cantilever signal that can be expressed as

$$A(t) = A_0 + A_1 \cos(\omega t + \phi), \tag{3.2}$$

where A_0 is the static surface displacement, A_1 represents the amplitude of the voltage-induced deformation, and ϕ is the phase shift between the driving voltage and the sample response [148, 149]. In PFM, the amplitude A_1 provides information on the magnitude of the local electromechanical coupling, while the phase ϕ reflects the polarisation orientation. Oppositely polarised domains exhibit phase values differing by approximately 180°, enabling nanoscale mapping of remanent ferroelectric states. All ferroelectrics exhibit a piezoelectric response, hence the detection of a switchable electromechanical signal by PFM provides direct nanoscale evidence of ferroelectricity within the film.

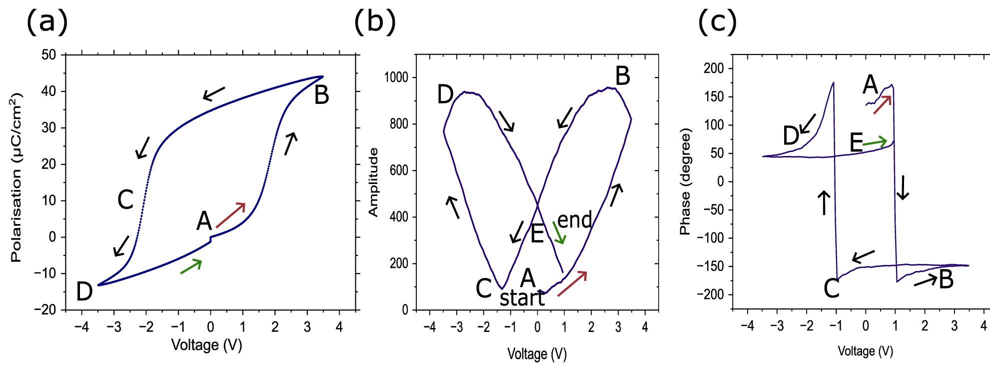

Figure 3.6: **PFM characterisation of ferroelectric switching in the HZO film.** (a) Schematic polarisation–voltage (P–V) loop illustrating the ferroelectric switching pathway, with labelled points (A–D) indicating key stages of domain evolution during the voltage sweep. (b) SS-PFM amplitude–voltage loop showing the characteristic butterfly response, with minima near the coercive voltages corresponding to domain switching. (c) Corresponding phase–voltage loop exhibiting a sharp $\sim 180°$ phase reversal between the two remanent polarisation states. The labelled points (A–D) are consistently marked across all panels to highlight the progression of switching and enable direct correlation between polarisation, amplitude, and phase responses.

Ferroelectric Switching Response To establish the intrinsic switching characteristics, amplitude–voltage and phase–voltage hysteresis loops were acquired using Switching Spectroscopy (SS) PFM mode. The amplitude in Fig. 3.6(b) shows the characteristic butterfly-shaped response of a ferroelectric material, with two high-amplitude regions corresponding to saturated polarisation states and a minimum near the coercive field where domain reversal occurs. The phase loop in Fig. 3.6(c) displayed an abrupt $\sim$180° reversal, confirming two stable and switchable remanent states. On the positive sweep, the phase flipped sharply at the coercive voltage but changed slightly as the bias approached its maximum value. A similar behaviour occurred on the negative sweep, where the phase decreased after switching instead of remaining constant. This gradual phase evolution arises from built-in field asymmetry and bias-dependent electrostatic screening, which modify the energy landscape and tip–sample environment even after switching. The effect is more prominent on the negative-bias side. Importantly, this drift does not indicate further switching; rather, it reflects a continuous change in electromechanical coupling under large bias.

Programming and reproducibility: The robustness of the written ferroelectric states was further evaluated by repeating write-read sequence multiple times. Figures 3.7(a) and 3.7(b) show three consecutive PFM amplitude and phase readouts, with the entire write-read procedure repeated three times. The persistence of both amplitude and phase contrast across repeated reads and rewrites demonstrates that the nanoscale ferroelectric domains are non-volatile and reproducible under the applied biasing conditions.The apparent fluctuations observed in the PFM amplitude traces arise from the pulsed measurement mode used in this experiment, where the applied bias is incremented in discrete steps of 0.1 V rather than swept continuously. This stepwise excitation introduces small variations in the measured amplitude response, giving rise to the observed wiggles. In contrast, measurements performed using a continuous bias sweep used in Fig. 3.6 exhibit comparatively smoother amplitude behaviour, indicating that the fluctuations primarily originate from the measurement protocol rather

than instability of the ferroelectric state.

To assess whether multiple programmable states can coexist within a single scan area, a standard box-in-box writing protocol was employed. In this scheme, two regions were written sequentially and read simultaneously at the end of the process. As shown in Fig. 3.7(c), clear contrast is observed between the written regions. The outer region written at −4 V corresponds to a high-capacitance state (HCS), while the inner region written at +3.5 V yields a low-capacitance state (LCS). Both written regions are clearly distinguishable from the unwritten background, in agreement with the macroscopic electrical measurements. The higher bias required to access the HCS reflects the intrinsic electrical asymmetry observed in these devices. The relatively weak contrast, even for the −4 V write, is attributed to a combination of electrostatic charge screening and the high AC read voltage, which can partially bias domains toward the LCS during measurement. Despite this limitation, the statistical distributions extracted from the PFM signal (Fig. 3.7(d)) clearly separate the written regions from each other and from the unwritten background.

Together, these results confirm that HZO supports reproducible, non-volatile nanoscale ferroelectric programming, with multiple stable states that can be written, distinguished, and reliably read.

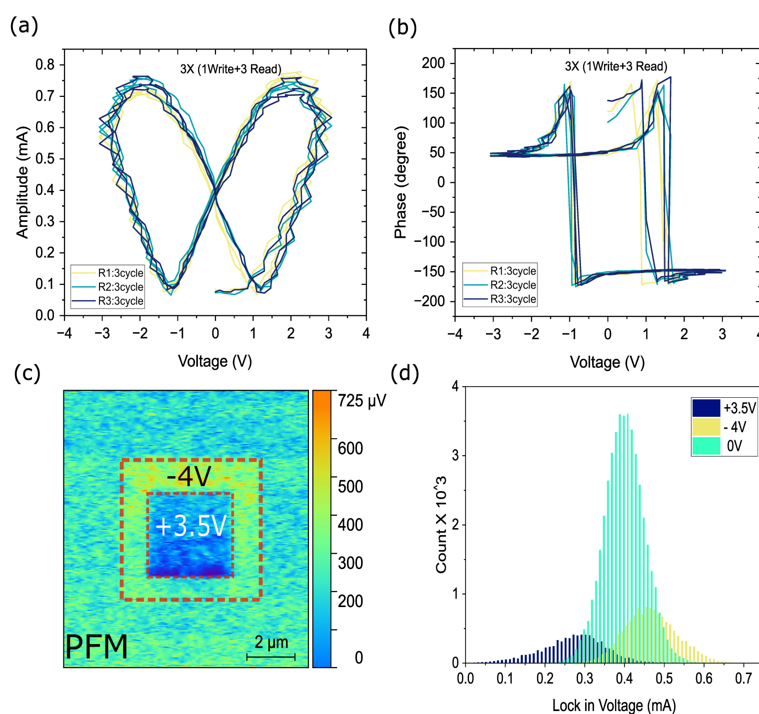

Figure 3.7: **PFM investigation of programming and reproducibility in HZO films.** (a) PFM amplitude and (b) phase images acquired after repeated write–read cycles, demonstrating stable and reproducible nanoscale ferroelectric domains. (c) PFM response following a box-in-box writing protocol, where the outer region was written at −4 V and the inner region at +3.5 V, producing domains with opposite polarisation states. (d) Statistical distribution of the PFM signal showing clear separation between the written regions and the unwritten background.

Time-Dependent Switching Dynamics While the preceding experiments establish that ferroelectric states can be written reproducibly and remain non-volatile, they do not reveal how rapidly these states can be formed or how sensitive the switching process is to the timescale of the applied bias. Since ferroelectric switching proceeds through time-dependent domain nucleation and growth, the stability and completeness of switching are expected to depend strongly on the duration and rate of the applied voltage. To probe these kinetic effects, the temporal dependence of switching was investigated using two complementary approaches: (i) varying the sweep period of the DC voltage during SS-PFM measurements, and (ii) employing discrete write and read voltage pulses with controlled pulse widths.

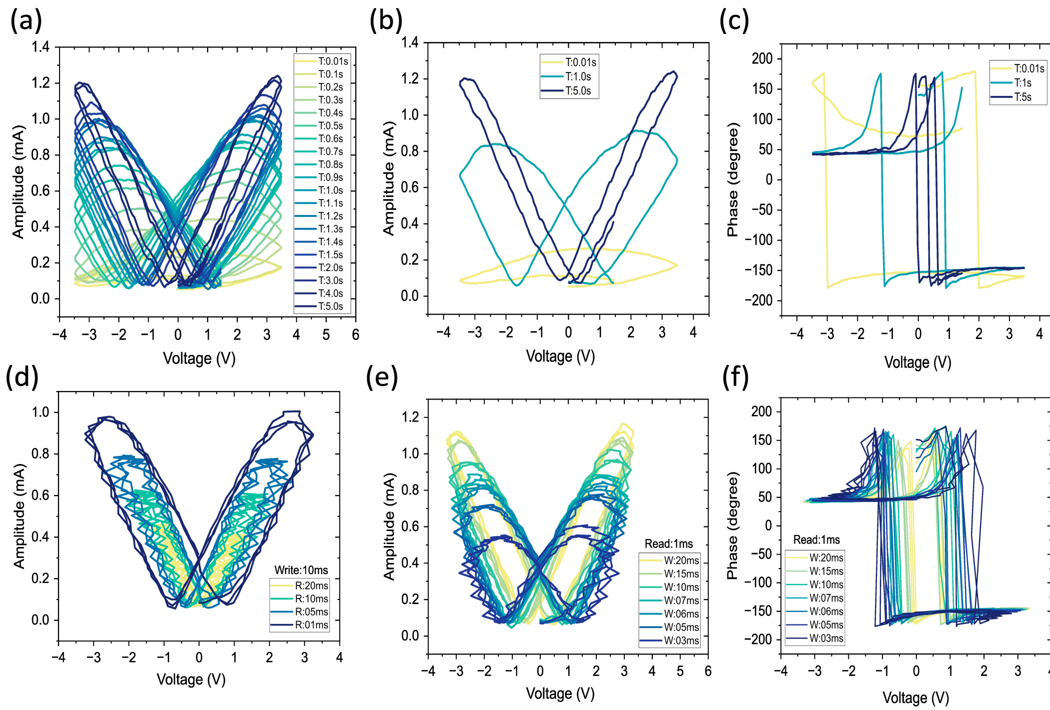

Figure 3.8: **Time-dependent PFM switching behaviour of the HZO film.** (a–c) SS-PFM amplitude and phase loops measured for varying voltage-sweep periods, showing the transition from rate-limited switching at short periods (0.01 s) to well-defined ferroelectric hysteresis at long periods (5 s). (d) Influence of read-pulse duration on the measured amplitude for a fixed write pulse. (e,f) Amplitude and phase loops as a function of write-pulse duration for read at 1 ms, illustrating the minimum pulse width needed for complete and stable switching.

To study the characteristic switching timescales, the sweep period was varied from 0.01 s to 5 s, as shown in Fig. 3.8 (a-c). At a sweep period of 0.01 s, the amplitude nearly vanished and the butterfly loop was barely resolved, although the phase still reversed over a broad voltage range, indicating slow and incomplete domain switching, as shown in Fig. 3.8 (b) by the yellow trace. At intermediate sweep periods (around 1 s), the butterfly loop became well defined with sharper phase transitions, reflecting complete domain reversal (Fig. 3.8(b), green trace). At 5 s, the amplitude reached its maximum and the butterfly loop narrowed (Fig. 3.8 (b), blue trace). These trends mirror device-level behaviour, where fast sweeps yield broadened, rate-limited switching, while slow sweeps recover the equilibrium coercive field.

To independently examine the write and read timescales of ferroelectric switching, a pulse-based protocol was employed. Unlike sweep-based PFM measurements, where only the

duration of the voltage sweep is varied, the pulse protocol allows independent control over the write-pulse and read-pulse durations. This approach also enables repeated readout of the same written location, as demonstrated previously in the volatility and reproducibility tests.

For the pulse-based experiments, the read-pulse duration was first varied, as shown in Fig. 3.8(d). Short read pulses produced a stronger and more reliable piezoresponse, with the maximum amplitude observed for a read duration of 1 ms. In contrast, longer read pulses progressively suppressed the measured amplitude. This reduction is attributed to tip-induced biasing and enhanced electrostatic screening during prolonged readout, rather than loss of the written ferroelectric state. These results indicate that the read process itself can perturb the domain configuration if the read pulse is too long, highlighting the importance of short, minimally invasive read conditions.

Next, the write-pulse duration was varied. Long write pulses resulted in saturated amplitude and clean 180° phase reversals, indicating complete and stable domain switching. Shorter write pulses led to weaker amplitude and incomplete switching, reflecting insufficient time for domain nucleation and growth. Below approximately 3 ms, the butterfly loop largely collapsed, while a change in phase could still be detected, indicating the presence of partial or unstable switching. This behaviour is consistent with the sweep-time analysis discussed earlier, where fast voltage sweeps similarly suppressed the amplitude response while retaining a phase evolution due to incomplete domain growth. Together, these observations identify a minimum pulse width of approximately 3 ms for deterministic switching and demonstrate that ferroelectric switching in HZO is governed by the kinetics of domain formation and stabilisation, with distinct timescale requirements for reliable write and read operations. It should be noted that the switching times extracted from SS-PFM measurements do not represent the intrinsic speed limit of the ferroelectric material. At the material level, ferroelectric switching in HZO can occur on sub-nanosecond timescales, with reported switching events approaching a few hundred picoseconds [150]. In such cases, the switching dynamics are primarily limited by domain-wall motion and device area. The much longer timescales observed in the present PFM measurements arise from the experimental geometry, where local switching under the AFM tip involves additional delays associated with nucleation, tip–sample contact conditions, and the limited bandwidth of the measurement system.

Electrostatic Force Microscopy (EFM)

EFM was employed to probe how different written polarisation states translate into distinct surface charge distributions and, consequently, different local capacitance states. EFM maps the electrostatic landscape above the surface and determines whether regions written with different voltages stabilise distinct levels of stored charge. If such charge contrast can be resolved reliably between neighbouring areas, it provides direct nanoscale evidence for multiple, non-volatile capacitive states in the HZO memcapacitor.

In EFM, the same tip bias $V(t)$ from Eq. 3.1 is applied, given by $V(t) = V_{DC} + V_{AC}\cos(\omega t)$. However, rather than detecting the resulting piezoelectric deformation, the measurement here focuses on the electrostatic force generated by this voltage. The force between the tip and sample is given by

$$F_{\text{es}}(t) = \frac{1}{2}\frac{\partial C}{\partial z}V(t)^2, \tag{3.3}$$

where $\partial C/\partial z$ is the gradient of the tip–sample capacitance. As the HZO films studied here are relatively smooth, variations in $\partial C/\partial z$ are negligible. Expanding $V(t)^2$ yields a static component and oscillatory components at the drive frequency ω and its second harmonic 2ω:

$$F_{\text{es}}(t) = \frac{1}{2}\frac{\partial C}{\partial z}\left[V_{\text{DC}}^2 + \frac{1}{2}V_{\text{AC}}^2 + 2V_{\text{DC}}V_{\text{AC}}\cos(\omega t) + \frac{1}{2}V_{\text{AC}}^2\cos(2\omega t)\right]. \tag{3.4}$$

$$V_{\text{DC}} = V_{\text{tip}} - V_{\text{surface}}, \tag{3.5}$$

where V_{surface} is the local surface potential. This definition is central to EFM, as the surface potential encodes the net bound, screening, and trapped charges associated with each written polarisation state. Any modification in the local charge distribution alters V_{surface} and therefore changes the effective V_{DC} sensed by the tip.

In Eq. 3.4, the static DC terms and the components proportional to V_{AC}^2 and $\partial C/\partial z$ do not contribute to charge mapping, as the lock-in amplifier selectively detects only the force modulation at the drive frequency corresponding to the ω term. The component oscillating at ω is proportional to $V_{\text{DC}}V_{\text{AC}}$ and therefore directly reflects variations in the local surface potential beneath the tip. This ω term forms the basis of charge mapping in EFM: the lock-in amplifier isolates it with high sensitivity and produces a spatial map of stored charge or surface potential. As the differences in surface potential between written regions are significant, the ω channel provides much clearer contrast than PFM when probing remanent ferroelectric states.

For EFM measurements, a similar box-in-box write-read scheme was employed to examine the electrostatic signatures associated with the written states. The inner region was written at +3.5 V and the outer region at −4 V. The resulting EFM image reveals a clear surface-potential contrast between the two regions, confirming that the two write voltages stabilise distinct, non-volatile charge states.

To investigate the existence of multi charge state, a three-level writing sequence was subsequently applied using −4 V, +1.5 V, and +3.5 V. The intermediate write voltage of +1.5 V was selected based on electrical measurements to lie within the tunable capacitance window. The resulting EFM map resolves three neighbouring regions with different surface potentials, and the corresponding histograms display three well-separated peaks. These results demonstrate the existence of stable and distinguishable nanoscale charge states, providing direct spatial evidence of multistate behaviour consistent with the device-level memcapacitive characteristics.

Finally, to verify that the observed contrast originates from electrostatic charge rather than surface morphology, EFM measurements were overlaid with topography and a line-scan analysis was performed. The topographic line scan across the written regions remained smooth, with an RMS roughness of approximately 0.9 nm, while the corresponding EFM line profile exhibited three discrete potential plateaus (C_0, C_1, and C_2) associated with the three written states. This confirms that the EFM contrast arises from differences in local surface potential rather than from topographic effects.

Taken together, the PFM and EFM results provide a coherent nanoscale picture of the

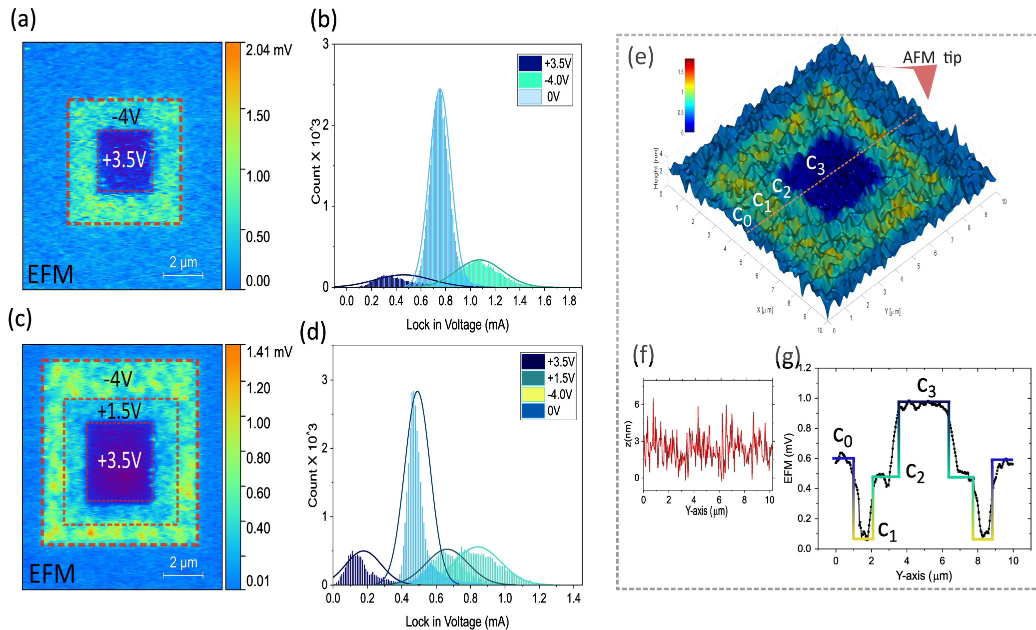

Figure 3.9: **EFM mapping of charge contrast and multilevel states in HZO.** (a) EFM box-in-box map showing clear potential contrast between regions written at –4 V and +3.5 V.(b) Histogram confirming two distinct charge levels. (c) Three-level writing experiment using –4 V, +1.5 V, and +3.5 V. (d) Histogram showing three separated electrostatic states. (e–f) Topography and line-scan height profile. (g) Corresponding EFM line profile resolving three charge plateaus, verifying that the contrast arises from surface potential rather than morphology.

memcapacitive behaviour in HZO. PFM identifies switchable ferroelectric domains through their piezoresponse, while EFM reveals the corresponding non-volatile charge states and their multilevel nature. The ability of EFM to resolve three distinct and stable potential levels provides direct nanoscale evidence of multistate memcapacitive behaviour, consistent with the macroscopic electrical characteristics discussed in later chapters.

3.3 Conclusion

This chapter presented the complete fabrication workflow and thin-film characterisation of HfO_x and HZO-based devices used throughout this thesis. XPS analysis revealed no significant change in stoichiometry upon annealing for either HfO_x or HZO films, indicating chemically stable oxide formation across all samples. In contrast, XRD highlighted clear structural evolution following annealing. Both materials exhibited partial crystallisation; however, HfO_x showed more pronounced monoclinic phase signatures, whereas HZO demonstrated the emergence of orthorhombic diffraction peaks associated with ferroelectricity, with TiN electrodes shown to be critical for phase stabilisation.

For HZO, AFM-based analysis further linked structure to nanoscale functionality. PFM measurements verified piezoelectric activity through characteristic butterfly-shaped amplitude loops and near-180° phase switching. Time-dependent write–read studies revealed distinct

timescale requirements, with write pulses exceeding 3 ms required for stable domain formation, while shorter write pulses led to suppressed amplitude response. Finally, multistate behaviour was demonstrated using box-in-box writing schemes and EFM mapping, which resolved multiple stable and distinguishable charge states at the nanoscale. Overall, this chapter establishes a comprehensive materials, structural, and nanoscale foundation for understanding memcapacitive behaviour in both defect-driven HfO_x systems and ferroelectric HZO devices, forming the basis for the electrical investigations presented in the following chapters.

Chapter 4

The Memristor-Memcapacitor

This chapter presents a comprehensive investigation of the electrical behaviour of HfO_x metal–insulator–metal (MIM) devices, focusing on both as-deposited and post-deposition annealed structures. In addition to conventional resistive switching, the central objective of this chapter is to establish tunable and non-volatile capacitive states and to examine how these capacitive responses evolve alongside resistive switching. While HfO_x has been extensively studied as a memristive material, the coexistence and controllability of resistive and capacitive switching within the same device remain less explored.

The motivation for examining annealed HfO_x devices is established in Chapter 2, where prior studies have shown that thermal processing can significantly enhance resistive switching characteristics, including increased switching window, improved stability, and access to new functional phases. However, existing literature predominantly emphasises resistive behaviour, and the influence of annealing on capacitive switching and frequency-dependent response has received limited attention. This chapter therefore extends the electrical investigation of annealed HfO_x beyond resistive metrics to include capacitive tunability and dynamic impedance behaviour. Finally, impedance spectroscopy is introduced as a key analytical framework to deconvolute the coupled resistive and capacitive processes by mapping the measured response onto an equivalent electrical circuit.

Hence, the chapter is structured in three parts. First, the electrical characterisation protocol is presented, outlining the DC and AC measurement methodologies used to probe static switching behaviour and small-signal frequency response. Second, explain the impedance spectroscopy and anlaysis. Finally, the validated framework is applied to compare the electrical behaviour of as-deposited and annealed HfO_x devices, enabling detailed interpretation of their tunable resistive-capacitive states and frequency-dependent performance.

4.1 Characterisation Protocol

This section introduces the electrical characterisation protocol commonly used in memristive device studies and employed in this work to investigate the behaviour of HfO_x MIM devices systematically. The protocol is designed to probe both static and dynamic electrical responses and to ensure consistency and comparability between as-deposited and annealed devices. An

overview of the complete measurement sequence is provided in Fig. 4.1, which illustrates the logical flow from initial system calibration through DC-AC measurements and impedance analysis.

The electrical characterisation protocol begins with calibration of the measurement setup to minimise parasitic capacitance and ensure reliable extraction of device-intrinsic responses. DC characterisation is then carried out to establish the baseline resistive behaviour of the devices, including activation of switching and evaluation of state stability. Subsequently, AC characterisation is performed to probe voltage-dependent capacitance modulation and the frequency-dependent dynamic electrical response of the devices under small-signal excitation.

Each stage of the electrical characterisation protocol outlined above is discussed in detail in the following subsections.

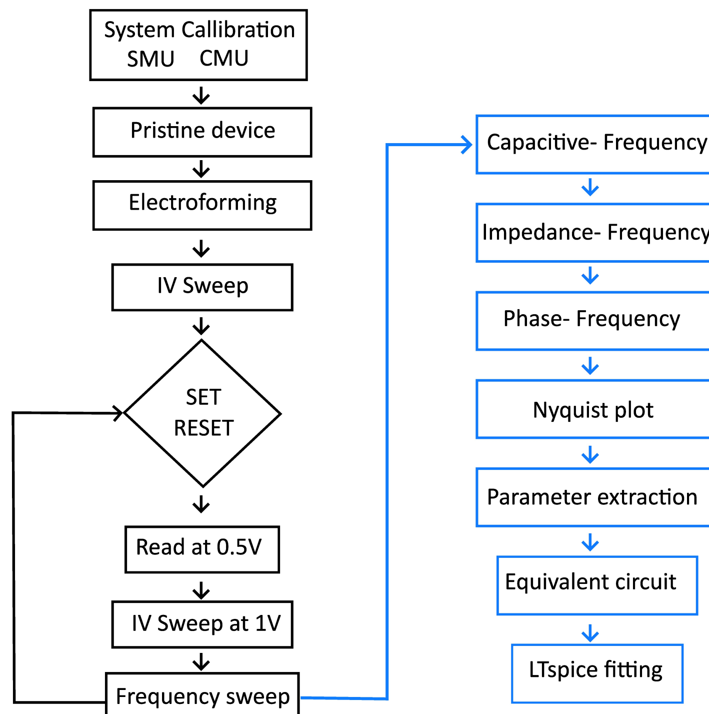

Figure 4.1: **Measurement protocol overview.** Schematic overview of the measurement protocol, illustrating the logical progression from system calibration and electroforming to DC I-V measurements and frequency-dependent impedance analysis, leading to equivalent circuit extraction and LTspice fitting.

4.1.1 System Calibration and Measurement Setup

All electrical measurements were carried out using a Keithley 4200 Semiconductor Characterization System, which integrates precision Source Measure Units (SMUs) and Capacitance Measurement Units (CMUs). The system enables accurate current–voltage (I–V) and impedance measurements over a wide frequency range from 1 kHz to 10 MHz, allowing comprehensive assessment of both resistive and reactive components of the device response.

At these measurement scales, particularly for low current DC measurements and high frequency AC characterisation, parasitic contributions from the measurement setup can significantly influence the extracted electrical parameters. Parasitic capacitances arising from probe pads, cables, and probe tips, as well as series resistances and inductive effects associated with interconnects and contacts, can distort both magnitude and phase of the measured response. Accurate removal of these extrinsic contributions is therefore essential to ensure that the measured characteristics reflect the intrinsic behaviour of the device rather than artefacts of the measurement environment. To address this, systematic calibration of both the SMU and CMU paths was performed prior to all electrical measurements.

The SMU calibration primarily corrects for internal offsets, leakage currents, and voltage measurement drifts that can affect low-current precision. Unlike the CMU path, the SMU does not require a manual open–short sequence; instead, the system performs an internal auto-zero and leakage compensation routine. This process measures the instrument's intrinsic bias and offset when no external device is connected, storing those values to be subtracted automatically during I–V measurements. This ensures that the voltage applied to the top electrode and the current measured from the device accurately reflect the true behavior of the Device-Under-Test (DUT), free from instrument-induced deviations.

Following SMU calibration, the CMU was calibrated to remove frequency-dependent parasitic effects arising from cables, probe tips, and contact pads. This step includes a open and short compensation sequence as recommended by the instrument manufacturer. First, the effective cable length and propagation delay are determined to correct for phase and impedance errors at high frequencies. The open-circuit compensation is then performed with the probe tips lifted above the DUT to measure and store the baseline stray capacitance and reactance of the measurement setup. Subsequently, the short-circuit compensation is executed by shorting the probe tips together, allowing the system to quantify residual series resistance, inductance, and contact effects. These two datasets are used internally to subtract the measurement path contributions from all subsequent impedance spectra, isolating the true response of the DUT.

The combined SMU and CMU calibration ensures that all subsequent current, voltage, and impedance measurements are representative of the intrinsic device behavior, independent of extrinsic parasitics.

4.1.2 DC Characterisation

DC characterisation constitutes the first stage of electrical evaluation performed on the fabricated HfO_x devices, and serves to establish their fundamental resistive switching functionality before advancing to dynamic and frequency-dependent studies. As discussed in Chapter 2, HfO_x-based memristive devices are known to exhibit resistive switching behaviour; however, practical device operation often involves additional steps to activate, stabilise, and verify this behaviour. Accordingly, DC characterisation is employed to determine whether the devices are forming-free or require an initial electroforming step. For devices that do not exhibit intrinsic switching, electroforming is applied to activate conductive pathways within the dielectric through controlled high-voltage stress. Following activation, I–V cycling is performed to examine high resistive state (HRS) and low resistive state (LRS), switching polarity, and reproducibility. Post-switching measurements are then used to assess the stability and volatil-

ity of the programmed states.

A bipolar voltage sweep is used to electroform and conduct I-V, starting from 0 V, ramping to a positive maximum bias, reversing to a negative bias, and finally returning to 0 V, thereby completing a full electrical cycle. This back-and-forth traversal of the electric field is essential to capture the hysteretic current with voltage.

Together, these DC measurements establish the operational voltage window, identify non-functional or unstable devices, and confirm the robustness of the resistive states. Only devices that exhibit repeatable and non-volatile DC switching behaviour are subsequently selected for AC characterisation and impedance spectroscopy, as this is a necessary condition for meaningful frequency-domain analysis. The individual steps of the DC characterisation protocol are described in detail in the following subsections.

Electroforming

Electroforming is a commonly required activation step for HfO_x-based devices, as pristine films typically exhibit highly insulating behaviour due to the absence of pre-existing conductive pathways. While forming-free HfO_x devices have been reported, such behaviour is comparatively less common and is often associated with specific processing conditions, defect engineering strategies, or ultrathin film geometries. Prior to applying any forming voltage, initial low-bias voltage sweeps were performed to assess the pristine electrical response of each device and to identify non-functional samples.

Devices exhibiting abnormally high current even at low bias, corresponding to an effective resistance below approximately 5 kΩ and a linear I–V response, were classified as dead or burnt devices. Such behaviour indicates a permanent ohmic short between the top and bottom electrodes, likely arising from local dielectric rupture, pinhole defects, or processing-induced damage. These devices do not exhibit memristive or memcapacitive behaviour and were discarded immediately.

Devices that retained very high resistance, typically in the GΩ range, under low-bias sweeps were classified as forming-required. For these devices, controlled electroforming was subsequently performed to activate conductive pathways within the HfO_x dielectric. Electroforming was achieved by applying a sequence of voltage sweeps with gradually increasing maximum amplitude, while strictly limiting the current using a compliance setting to avoid catastrophic hard breakdown. A successful forming event is characterised by a sudden increase in current followed by stabilisation into a reproducible conduction regime, indicating the occurrence of a controllable soft breakdown.

During this incremental biasing process, three outcomes are typically observed: (i) devices that fail catastrophically and transition into a permanent short, (ii) devices that undergo soft breakdown and enter a stable resistive switching regime, and (iii) devices that remain highly insulating regardless of the applied voltage and never form. Only devices belonging to the second category, those that successfully formed and exhibited a measurable resistive window were retained for further DC, AC, and impedance analysis. Devices in the remaining categories were excluded at this stage. In general, approximately 75–80 percent of the fabricated devices fall into the second category and are therefore suitable for further characterisation and investigation of the switching properties.

A schematic representation of the all possible categories identified during the electroforming stage are provided in Fig. 4.2. Importantly, all examples shown in Fig. 4.2 correspond to measured electrical data obtained from HfO_x devices fabricated under identical conditions, comparing as-deposited and post-annealed films.

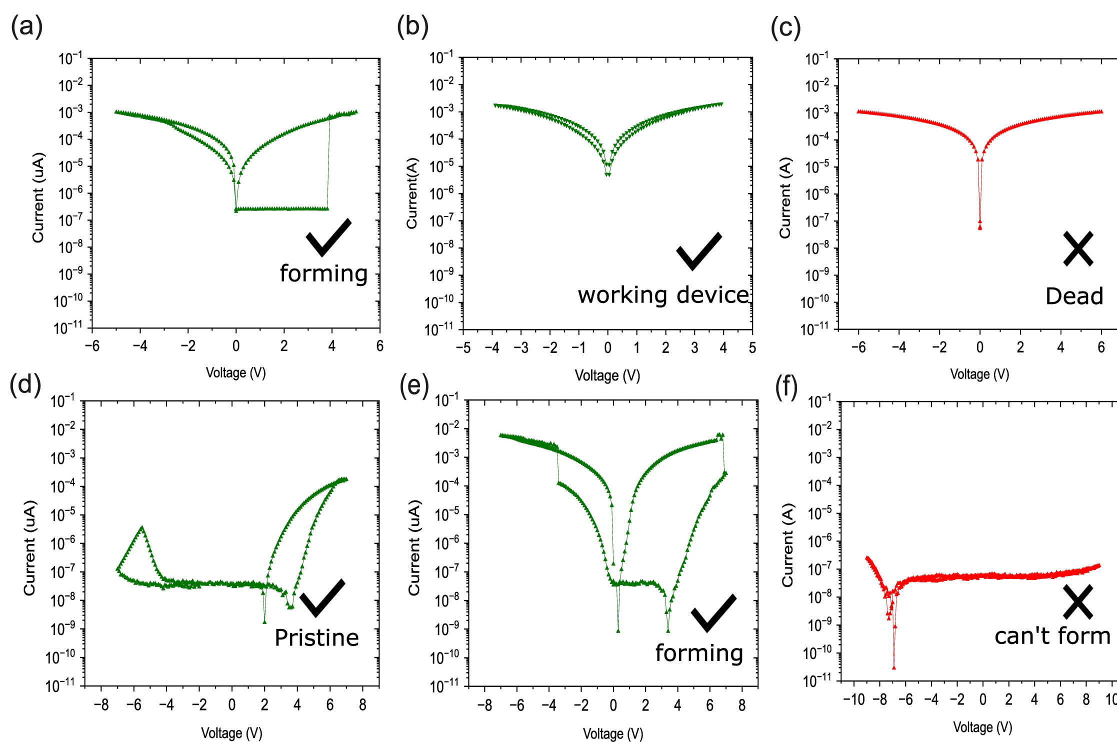

Figure 4.2: **Possible electroforming outcomes in devices.**Panels (a)-(c) show data from as-deposited HfO_x devices. (a) successful forming of an as-deposited device, (b) stable post-forming operation of the same device, and (c) a dead device exhibiting permanent shorting. Panels (d)-(f) show corresponding behaviour in annealed HfO_x devices, including (d) pristine insulating response, (e) successful electroforming, and (f) devices that remain insulating and fail to form.

I–V Cycling and Resistance Stabilisation

After successful forming, each device was subjected to multiple I–V sweeps within the operational voltage window to assess repeatability and state stability. To estimate the safe working voltage range, voltage sweeps with amplitudes approximately half of the forming voltage were applied and progressively increased to expand the resistive window until the device exhibited a short-circuit failure. This preliminary step helps determine the reliable voltage operating limits of the memristive stack and is performed only once per batch to define the typical working range. Once the working voltage range was established, a new pristine device was selected and formed for subsequent electrical characterisation.

The formed device is then tested for infant mortality, which refers to the tendency of some devices to lose their switching functionality within the first few electrical cycles due to unstable conductive pathways or weakly formed defect configurations. To identify such behaviour, a small number of initial I–V sweeps were applied to examine whether the resistive window

remained consistent or progressively shrank. During the initial sweeps, minor fluctuations in current were observed as the defect distribution and interface states stabilised under repeated bias stress. When the I–V curves became reproducible with consistent threshold voltages and hysteresis shape, the device was considered electrically stable and suitable for data acquisition. Such screening ensured that only robust and representative devices were used for subsequent AC measurements.

Before proceeding to AC measurements, a retention test was performed on each stabilised device to confirm the non-volatility of its resistive state. The test involved programming the device into a chosen resistance level and periodically reading the current at a small voltage selected such that it does not perturb the stored state of the device. The choice of read voltage is inherently device-dependent; in this work, a value of 0.5 V was used. The resistance was monitored over one minute to identify any drift or relaxation. If the resistance remained constant over extended durations without significant decay, the device was classified as non-volatile and suitable for impedance analysis. This retention verification is crucial because AC impedance characterisation assumes that the device remains in a steady resistive state throughout the frequency sweeps. Any instability would introduce uncontrolled variations in the extracted capacitance or phase response.

4.1.3 AC Characterisation

AC characterisation was performed to probe the frequency-dependent response of the HfO_x devices and to provide the impedance dataset required for subsequent impedance spectroscopy analysis. In contrast to DC measurements, which primarily establish static conduction states and resistive switching behaviour, AC measurements resolve the dynamic components of the device response, including capacitive behaviour and interfacial contributions that govern the overall complex impedance.

To ensure that the measured response reflects the intrinsic behaviour of a programmed state rather than additional switching events, all AC measurements were conducted in the small-signal regime. This was achieved by superimposing a sinusoidal excitation of 30 mV on a fixed DC bias of 0.5 V. The small AC amplitude keeps the device within its linear, non-switching regime, such that the applied perturbation probes the differential response of the system without inducing resistive state change. If the AC amplitude is increased significantly, unintended partial switching or nonlinear conduction can occur, leading to distortion of the measured impedance. Conversely, excessively small amplitudes reduce the signal-to-noise ratio and compromise measurement reliability. The selected value of 30 mV therefore represents a balance between maintaining linear response and achieving sufficient measurement sensitivity.

The applied DC bias fixes the device at a well-defined operating point corresponding to a programmed resistance state, HRS or LRS. Maintaining a constant DC bias during frequency sweeps ensures that the measured impedance reflects the response of a single, stable state. This requirement highlights the necessity of non-volatile and repeatable DC switching prior to AC characterisation, as any state instability would invalidate the small-signal assumption and lead to ambiguous frequency-domain data. Under these conditions, impedance magnitude and phase were extracted over a frequency range from 1 kHz to 10 MHz.

For each device, impedance and capacitance were first measured in the as-programmed

state. The device was then deliberately switched between HRS and LRS using the DC voltage levels established during I-V characterisation, and the AC measurement was repeated under identical small-signal conditions. This workflow establishes a direct link between the programmed resistive state and the corresponding capacitive and impedance response of the device. A schematic overview of the combined DC programming and AC frequency-sweep sequence is already mentioned in Figure 4.1. The frequency-dependent data obtained through this protocol are subsequently analysed using impedance spectroscopy technique, which is introduced in the following section.

4.2 Impedance Spectroscopy and Analysis

Impedance spectroscopy is employed in this work as an analytical framework to decouple the resistive and capacitive responses observed during DC and AC characterisation. While DC measurements establish the presence of resistive switching and AC measurements reveal voltage-dependent capacitance modulation, neither approach alone can unambiguously determine how these processes are electrically coupled within the device. Impedance spectroscopy addresses this limitation by resolving the complex, frequency-dependent response of the system and enabling its interpretation in terms of an equivalent electrical circuit. Originally developed to study electrochemical interfaces, impedance spectroscopy has also been extended to solid-state electronic systems, including memristors and memcapacitors, where defect-mediated transport and interfacial charge dynamics play a dominant role. In such oxide-based devices, the technique provides a powerful means to probe bulk conduction, interfacial effects, and relaxation phenomena through their distinct frequency signatures.

The applicability of impedance spectroscopy relies on the device operating in a linear, time-invariant regime, such that the measured response reflects intrinsic material and interface properties rather than field-driven switching events. For this reason, impedance measurements are performed under small-signal AC excitation superimposed on a fixed DC bias, as described in the preceding section.

In the following subsections, the impedance analysis begins with the mathematical formulation of the complex impedance, which forms the basis for interpreting the frequency-dependent response of the device. This formulation is then used to explain the construction and physical meaning of the Bode and Nyquist representations. From these plots, the relevant electrical parameters are extracted and subsequently used to fit an equivalent-circuit model using impedance spectrum analysis tool. This stepwise approach enables quantitative correlation between the measured impedance response and the underlying electrical behaviour of the device.

4.2.1 Mathematical Aspect

As described earlier in chapter 2, the fabricated memristor stack can be modeled as a parallel network consisting of a resistor and a capacitor. This simplified model captures both the bulk transport through the oxide layer and interfacial effects from the electrodes. The validity of this assumption will be verified later through experimental fitting and comparison with equivalent-circuit models. According to this representation, the complex impedance of the

equivalent circuit can be expressed as:

$$Z(\omega) = R_s + \frac{RX_C}{R + X_C}, \tag{1}$$

$$X_C = \frac{1}{j\omega C}, \tag{2}$$

Here, $Z(\omega)$ represents the complex impedance of the circuit, R_s corresponds to the series or contact resistance, R denotes the parallel resistive channel within the device, and C represents the capacitive contribution arising from charge accumulation across the dielectric. X_C is the reactance of the capacitor and $\omega = 2\pi f$ is the angular frequency of the applied signal.

Substituting Eq. (2) into Eq. (1) and simplifying yields:

$$Z(\omega) = R_s + \frac{R}{1 + \omega RC} - i\frac{\omega R^2 C}{1 + (\omega RC)^2}. \tag{3}$$

This expression can be rearranged into the contour form where $Z'(\omega)$ and $Z''(\omega)$ denote the real and imaginary impedance, respectively.:

$$\left[Z'(\omega) - \left(R_s + \frac{R}{2}\right)\right]^2 + [Z''(\omega)]^2 = \left(\frac{R}{2}\right)^2, \tag{4}$$

which is analogous to the standard equation of a circle, $(x - a)^2 + (y - b)^2 = r^2$, where the center (a, b) corresponds to $\left(R_s + \frac{R}{2}, 0\right)$ and the radius r equals $R/2$. When the impedance is plotted on the complex plane, this relationship produces a semicircular arc characteristic of an ideal parallel RC network with a series resistance.

Equations (1) and (4) therefore form the analytical foundation for impedance analysis in this work. Equation (1) defines the composite impedance of the device, while Eq. (3) expresses its frequency-dependent real and imaginary components. Together, they provide the mathematical basis for constructing the Bode and Nyquist plots, which translate experimental impedance measurements into physically interpretable signatures. In particular, Eq. (4) is critical for understanding how measured parameters can be represented on the complex plane to extract resistive, capacitive, and interfacial contribution, forming the basis of the detailed analyses presented in the following subsections.

4.2.2 Bode Plot

The Bode plot represents the experimentally measured frequency-dependent response of the device through two quantities: the impedance magnitude $|Z(\omega)|$ and the phase angle $\angle Z(\omega)$, both plotted as a function of logarithmic frequency. In the present analysis, the bode representation serves two essential purposes. First, it provides direct physical insight into the transition between resistive and capacitive dominance through the identification of a characteristic cut-off frequency. Second, it forms the experimental basis from which the Nyquist plot is constructed by converting magnitude and phase information into real and imaginary impedance components.

As shown in Fig. 4.3, at low frequencies ($\omega RC \ll 1$), the capacitive branch behaves as an open circuit and the current primarily flows through the resistive channel (R). In this regime, the impedance magnitude approaches a constant value equal to ($R_s + R$), and the phase angle remains close to 0°, indicating that voltage and current are nearly in phase, characteristic of ohmic conduction. As the frequency increases, the capacitive reactance decreases according to $X_C = 1/(\omega C)$, progressively allowing current to flow through the capacitive pathway. In the high-frequency limit ($\omega RC \gg 1$), the capacitive contribution dominates and the impedance magnitude asymptotically approaches R_s, corresponding to the residual series resistance associated with electrodes and contacts. Concurrently, the phase angle shifts toward −90°, consistent with ideal capacitive behaviour.

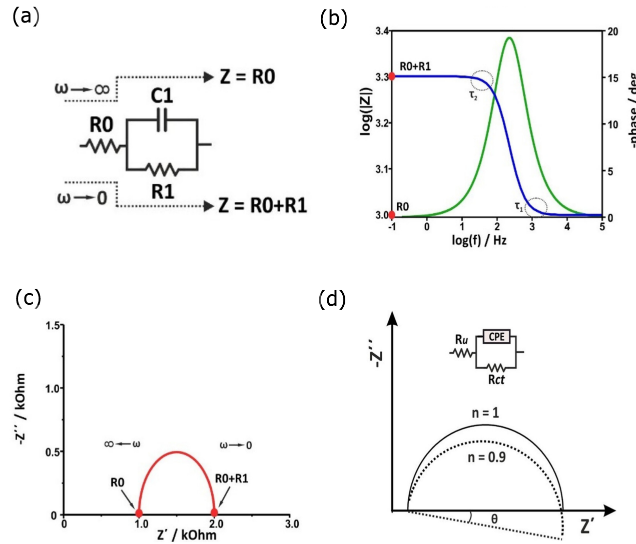

Figure 4.3: **Impedance spectroscopy framework and equivalent circuit representation.** (a) Randles equivalent circuit model illustrating the low- and high-frequency impedance limits, (b) corresponding Bode magnitude and phase plots, (c) Nyquist representation highlighting the extraction of resistive components, and (d) schematic illustration of the effect of a constant phase element (CPE) on the Nyquist response. Reproduced from [151]. Copyright © 2023 American Chemical Society.

The transition between these two regimes occurs at the characteristic or cut-off frequency, defined as

$$f_c = \frac{1}{2\pi RC}. \tag{5}$$

At this frequency, the resistive and capacitive contributions are equal in magnitude and the impedance magnitude decreases to $1/\sqrt{2}$ of its low-frequency value. This relation provides a first-order estimate of the device capacitance via $C = 1/(2\pi R f_c)$ and offers an independent consistency check for parameters obtained from equivalent-circuit fitting.

Beyond identifying the cut-off frequency and effective bandwidth, the Bode plot also enables construction of the Nyquist representation. Using the measured impedance magnitude and phase at each frequency point, the real and imaginary components of the complex impedance are obtained as

$$Z'(\omega) = |Z|\cos\phi, \qquad Z''(\omega) = |Z|\sin\phi, \tag{6}$$

where $Z'(\omega)$ and $Z''(\omega)$ correspond to the resistive and reactive components, respectively.

Equation (6) provides the direct transformation from experimentally measured Bode spectra to the Nyquist representation. When plotted on the complex plane, these data points follow the contour described by Eq. (4), enabling quantitative extraction of the equivalent circuit parameters (R_s, R, and C). The Nyquist analysis, which explicitly exploits this contour representation, is discussed in detail in the following section.

4.2.3 Nyquist Plot

As mentioned in the previous section, the Nyquist plot reorganises the experimentally measured impedance magnitude and phase onto the complex plane, where the impedance response must satisfy the contour relation derived earlier. This representation provides a direct means to analyse the resistive–capacitive coupling in the device and enables both quantitative parameter extraction and identification of non-ideal capacitive behaviour. In the ideal case, the impedance contour follows a perfect semicircle corresponding to a parallel RC network with a series resistance as shown in Fig. 4.3 (d). However, departures from this ideal contour are commonly observed in practical devices and carry important physical information. In particular, deviations from the ideal semicircle directly reflect non-ideal capacitance arising from distributed relaxation processes within the dielectric and at the interfaces. The Nyquist representation therefore serves not only as a tool for extracting circuit parameters but also as a diagnostic framework for assessing the degree of capacitive non-ideality inherent to the device.

Parameter Extraction from Nyquist Plots: The Nyquist plot represents the complex impedance on the Z'–Z'' plane. According to Eq. (4), the impedance response of an ideal parallel RC circuit with a series resistance R_s traces a perfect semicircle in this representation. The high-frequency intercept of the semicircle corresponds to R_s, while the low-frequency intercept represents $(R_s + R)$. Frequency increases clockwise along the arc, and the apex of the semicircle (maximum $|Z''|$) occurs at $\omega = 1/RC$, corresponding to the characteristic relaxation time $\tau = RC$ of the system. This behaviour can be verified analytically by examining the limiting cases of $Z'(\omega)$ in Eq. (4). In the high-frequency limit, the capacitive reactance becomes negligible, yielding

$$\lim_{\omega\to\infty} Z'(\omega) = R_s,$$

whereas in the low-frequency limit, current flows predominantly through the resistive pathway,

$$\lim_{\omega\to 0} Z'(\omega) = R_s + R.$$

Accordingly, the diameter of the semicircle equals R, and its centre is located at $R_s + R/2$ along the real axis. These parameters serve as the initial inputs for equivalent-circuit fitting, where the experimentally obtained impedance spectra are modeled using circuit-analysis software. The capacitance values estimated independently from the Bode cut-off frequency are cross-verified during this fitting procedure to ensure internal consistency.

Non-Ideal Capacitive Behaviour and Constant Phase Element: In practice, experimental Nyquist plots obtained from memristive and memcapacitive devices rarely exhibit a perfect semicircle. Instead, the impedance arc is systematically depressed below the real axis, reflecting non-ideal behaviour arising from interfacial roughness, spatially distributed trap states, compositional inhomogeneity, and local variations in electric field. To account for this non-

ideal response, the ideal capacitive element is replaced by a constant phase element (CPE), which introduces a fractional phase relationship between voltage and current. The impedance of a CPE is expressed as

$$Z_{\text{CPE}} = \frac{1}{(j\omega)^n Q}, \tag{8}$$

where Q is a pseudo-capacitance and $0 < n \leq 1$ quantifies the deviation from ideal capacitive behaviour. When $n = 1$, the CPE reduces to an ideal capacitor, whereas decreasing values of n lead to increasing depression of the Nyquist arc, indicative of a broader distribution of relaxation times, shown in Fig. 4.3 (d). Importantly, the Nyquist contour is constrained to lie on or below the ideal semicircle as the value of n cant exceed 1. The parameter Q does not represent a true capacitance but rather a frequency-dependent pseudo-capacitance.

Equivalent-Circuit Modelling and Validation: Equivalent-circuit modelling is carried out by fitting the experimentally obtained impedance spectra using impedance analysis software (EIS Spectrum Analyser). The software allows the user to construct a trial equivalent circuit by selecting individual electrical elements, assigning initial parameter values, and iteratively refining these parameters to minimise the deviation between the simulated and experimental impedance response. During this process, physical constraints are imposed on the parameters to ensure meaningful solutions, such as enforcing positive resistances and restricting the CPE exponent to the range $0 < n \leq 1$.

The fitting procedure is initiated using a simple R–C model corresponding to an ideal parallel resistive–capacitive network with a series resistance. When this model fails to accurately reproduce the experimental Nyquist contour particularly the depressed semicircular response, the ideal capacitor is replaced by CPE. The choice between a capacitive or CPE-based model is therefore guided by the quality of fit and the ability of the circuit to capture the observed frequency-dependent behaviour. This fitting procedure therefore establishes the validity of the proposed equivalent-circuit representation for HfO_x devices. Together with the DC and AC characterisation steps described earlier, this completes the electrical analysis framework adopted in this chapter. This provides the foundation for interpreting the device-specific results discussed in the following section.

4.3 Device Analysis

The device-level electrical behaviour is analysed using HfO_x MIM devices with a fixed lateral area of $20 \times 20\ \mu\text{m}^2$, which serves as the reference geometry throughout this section. The discussion begins with the resistive and capacitive switching characteristics of as-deposited devices, establishing the baseline response and identifying the extent of capacitive tunability. This behaviour is then compared with that of post-deposition annealed devices, where changes in electrical performance are interpreted in relation to the film morphology and structural evolution discussed earlier. The analysis is subsequently extended to impedance spectroscopy and equivalent-circuit modelling, with LTspice simulations used to validate the extracted electrical configuration.

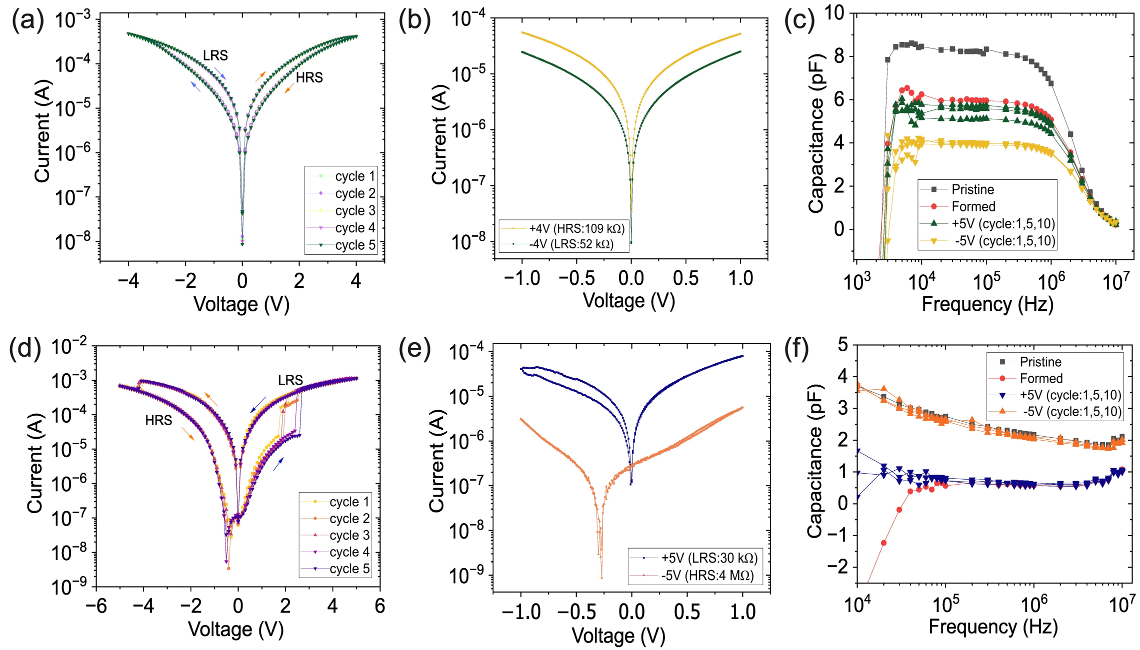

Figure 4.4: **Resistive and capacitive switching of as-deposited and annealed HfO_x devices.** (a-c) Electrical behaviour of as-deposited devices and (d-f) for annealed. Figure (a,d) shows semilogarithmic I-V characteristics over repeated switching cycles, demonstrating reproducible SET/RESET behaviour, (b,e) low-voltage I-V response highlighting the distinct low and high-resistance states, and (c,f) frequency-dependent capacitance for pristine and formed states, including cyclic stability over multiple switching events. Reproduced from the author's own work [1].

4.3.1 Resistive and Capacitive switching

As-deposited: As-deposited HfO_x devices exhibit resistance in the GΩ range, together with a capacitance of approximately 8 pF measured at 10 kHz, indicative of an intact dielectric response prior to any field-induced modification of the oxide. Following electroforming at ±5 V, the devices transition into a stable operating regime characterised by a substantial reduction in resistance to the range of 50–500 kΩ. This behaviour indicates the establishment of a percolative conduction network within the HfO_x film, consistent with defect-mediated transport in amorphous oxides [152]. Simultaneously, the measured capacitance decreases to approximately 6 pF. As no geometric change in electrode area or film thickness occurs during forming, this reduction cannot be attributed to capacitive scaling effects. Instead, it indicates a modification of the effective dielectric response, arising from redistribution of the internal electric field and localised screening associated with the newly formed conductive pathways.

Figures 4.4 (a) and (b) present the resistive switching behaviour of the formed as-deposited devices. Figure 4.4 (a) shows semi-logarithmic I-V characteristics recorded over five consecutive cycles, demonstrating reproducible bipolar switching. The resistive switching ratio remains modest, with values close to 2, and the SET and RESET transitions evolve gradually rather than abruptly, suggesting that switching is governed by distributed defect rearrangement rather than sharply localised filament formation. To verify the robustness of the programmed resistive states, each state was subsequently probed using low-voltage I-V

sweeps, as shown in Fig. 4.4 (b). Measurements performed at ±1 V do not induce any observable change in resistance, confirming that the resistive states are non-volatile and stable under low-field interrogation. This observation validates the use of a 0.5 V read voltage in subsequent AC and impedance measurements, ensuring that the device remains within the small-signal regime without perturbing the stored state.

In addition to resistive switching, the as-deposited devices exhibit clear capacitive switching behaviour, as shown in Fig. 4.4 (c). Two discrete non-volatile capacitance states are observed: a low-capacitance state (LCS) of approximately 4 pF and a high-capacitance state (HCS) of approximately 6 pF. These states are accessed reproducibly through voltage programming, confirming the coexistence of memristive and memcapacitive behaviour within the same device. Notably, despite the analogue nature of the resistive switching, the capacitive response remains largely binary, with the device switching between two well-defined capacitance levels rather than exhibiting a continuous analogue evolution. Independent of the polarity or magnitude of the programming voltage beyond threshold, the device consistently stabilises into one of these two capacitance states. While this behaviour limits multilevel capacitive tunability, the presence of reproducible and non-volatile binary capacitance states is nevertheless highly significant from a device perspective.

The LRS corresponds to the LCS, while the HRS corresponds to the HCS. From a simple geometric viewpoint, enhanced conduction might be expected to reduce the effective dielectric thickness and increase capacitance. The trend observed here indicates that the capacitive response is governed not by geometry but by voltage-history-dependent redistribution of defects, interfacial charge accumulation, and local permittivity modulation within the oxide. In addition, the capacitive switching exhibits pronounced state-dependent variability, with significantly larger fluctuations observed in the HCS. This behaviour suggests that the high-capacitance configuration corresponds to a less energetically stable defect landscape, where stochastic vacancy motion and distributed relaxation processes dominate [153]. The frequency dependence of the capacitance further reveals important limitations of the device. As frequency increases, the distinction between HCS and LCS progressively diminishes, and beyond a characteristic cut-off frequency the capacitance values converge. This convergence reflects the inability of defect and interface mediated mechanisms to respond at higher frequencies.

Overall, the as-deposited HfO_x devices demonstrate clear coexistence of resistive and capacitive memory effects, with analogue resistive switching accompanied by robust binary capacitive switching. While the limited resistive window, modest capacitance contrast, and reduced frequency retention impose constraints on performance, the presence of reproducible non-volatile binary capacitance states highlights the potential of these devices as tunable binary capacitors. These observations provide a critical baseline for assessing how post-deposition annealing will modify the defect landscape, as discussed in the following subsection.

Annealed devices: Post-deposition annealing substantially modifies the electrical behaviour of the HfO_x devices, resulting in qualitatively different switching characteristics compared to the as-deposited case. While the pristine resistance of annealed samples remains comparable to that of as-deposited devices, the forming voltage increases to approximately ±7 V. This increase is indicative of a reduced density of electrically active defects and a more robust oxide network, consistent with annealing-induced defect reorganisation and partial structural ordering [92, 154]. In addition, the pristine capacitance decreases to approximately 3 pF, reflecting a reduction in the effective dielectric constant associated with structural reorgani-

sation of the film during annealing [155, 144].

Following electroforming, annealed devices exhibit a pronounced enhancement in resistive switching performance. As shown in Fig. 4.4 (d), the semi-logarithmic I-V characteristics display a significantly enlarged resistive window, with resistive ratios reaching values on the order of 100 consistent with previous reports [30, 51]. This behaviour indicates the formation of more sharply defined and spatially confined conduction pathways, in contrast to the diffused vacancy networks observed in as-deposited films. The switching polarity remains bipolar however, the I-V characteristics are no longer symmetric about the origin. This is clealry visible in the low voltage I-V at HRS, shown in Fig. 4.4 (e).

The analogue nature of the resistive switching is also modified by annealing. While gradual switching is still observed, particularly during the RESET transition from LRS to HRS, the SET transition becomes comparatively sharper and more abrupt. This behaviour highlights a key trade-off introduced by annealing, although the resistive window becomes substantially larger and more stable, the degree of analogue tunability is partially reduced. From a processing perspective, annealing introduces additional constraints related to thermal budget and CMOS compatibility. Temperatures approaching 500 °C are generally considered incompatible with back-end-of-line integration. For this reason, the annealing temperature in this work was limited to 400 °C, as discussed in Chapter 3. This choice represents a deliberate balance between achieving enhanced electrical performance and maintaining compatibility with practical device integration requirements.

The capacitive behaviour of annealed devices, presented in Fig. 4.4 (f), shows a clear improvement over as-deposited samples. Two well-separated non-volatile capacitance states are observed, with a capacitive switching ratio of approximately 3. Importantly, these states remain nearly constant up to frequencies approaching 10 MHz, indicating enhanced frequency retention and reduced dielectric relaxation. Compared to as-deposited devices, the capacitance states in annealed films exhibit significantly reduced variability, reflecting a more energetically stable defect and interface configuration. The reduced dispersion in the high-capacitance state suggests that annealing suppresses stochastic vacancy motion contributing to the dielectric response.

Overall, annealing drives the HfO_x devices into a regime characterised by large and stable resistive switching windows, improved capacitive state separation, and enhanced frequency retention. While some analogue tunability is sacrificed relative to as-deposited devices, the emergence of robust, well-defined resistive and capacitive states establishes annealed HfO_x as a promising platform for stable memristive–memcapacitive device operation.

Area dependence: While the capacitive switching ratio of annealed 20×20 μm^2 devices represents a clear improvement, it remains limited for applications requiring a larger window. To address this limitation and to evaluate the scalability of the memcapacitive response, the effect of device area on capacitive switching behaviour was investigated. Increasing the device area to 40 μm^2 leads to a substantial enhancement in capacitive switching window. In as-deposited devices, the increase in area primarily results in a higher absolute capacitance without a corresponding improvement in capacitive switching ratio. In contrast, annealed devices exhibit a pronounced increase in capacitive switching ratio, reaching values close to 10. This behaviour indicates that the mechanisms responsible for memcapacitive switching in annealed HfO_x scale favourably with device area, enabling access to a wider and more stable capacitance window.

It is important to note that this area-scaling study is intended to demonstrate the feasibility of enhancing the capacitive switching window through geometric scaling. For the remainder of this chapter, detailed electrical and impedance characterisation is still performed on the smaller 20×20 μm^2 devices, as reduced device dimensions are preferable for integration density and space-constrained circuit applications. The observed area dependence nevertheless confirms that the memcapacitive behaviour is not limited by intrinsic material constraints and can be further optimised through device design.

Table 4.1: Size comparison for capacitive switching, reproduced from [1]

Sample	Device size (µm)	Pristine capacitance (pF)	Formed capacitance (pF)	Capacitive states (pF)
As-deposited	20	10	7	HCS: 6 LCS: 4
	40	30	20	HCS: 20 LCS: 10
Annealed	20	3	1	HCS: 3 LCS: 1
	40	10	1	HCS: 10 LCS: 1

4.3.2 Impedance spectroscopy

As-deposited devices: Figures 4.5(a)-(c) present the impedance response of as-deposited HfO_x devices measured in the two programmed states. The impedance magnitude Bode plot shown in Fig. 4.5(a) exhibits a characteristic low-pass filter behaviour, where the impedance remains approximately constant at low frequencies and rolls off beyond a well-defined cut-off frequency. In this regime, low-frequency signals are transmitted with minimal attenuation, while higher-frequency components are progressively suppressed. Such a response indicates that the small-signal dynamics of the device are governed by a coupled resistive–capacitive interaction, rather than by purely resistive or purely capacitive transport.

A key observation is that electrical programming results in two distinct impedance profiles, each associated with a different cut-off frequency. The high-impedance state (HIS) exhibits a lower cut-off frequency, whereas the low-impedance state (LIS) extends the passband to higher frequencies. This behaviour demonstrates that voltage programming enables direct and reversible control over the frequency response of the device. Rather than acting solely as a resistive memory element, the as-deposited device functions as a voltage-tunable impedance element whose effective bandwidth can be modulated through switching. Importantly, this tunability arises from the collective modification of both resistive and capacitive contributions, highlighting their coupled evolution following electrical programming.

Further insight into this coupling is provided by the corresponding phase Bode plot shown in Fig. 4.5(b). At low frequencies, the phase remains close to zero, indicating resistive-dominated transport. As frequency increases, the phase progressively shifts towards negative values, reflecting the increasing contribution of capacitive charging processes. The phase reaches its maximum deviation in the vicinity of the cut-off region identified in the magnitude plot, confirming that the transition between resistive- and capacitive-dominated response occurs over the same frequency range. At higher frequencies, the phase partially recovers as dielectric relaxation mechanisms are unable to respond to rapid excitation, leading to a

suppression of capacitive contributions.

To directly assess the validity of the assumed equivalent-circuit description, the same impedance data are reorganised into the complex plane and presented as Nyquist plots in Fig. 4.5(c). Both programmed states form semicircular arcs, providing experimental verification that the impedance response of the as-deposited devices is consistent with a Randles-type equivalent circuit comprising a parallel resistive-capacitive element in series with a contact resistance, as introduced in the previous section. The high-frequency intercept corresponds to the series resistance R_s, while the span of the arc reflects the effective parallel resistance associated with the programmed state, which are listed in Table 4.2. The emergence of semicircular contours therefore confirms that resistive and capacitive contributions act predominantly in parallel within the device. Although the Nyquist arcs are not perfectly ideal and exhibit a measurable downward depression, their overall geometry closely follows the contour relation derived earlier.

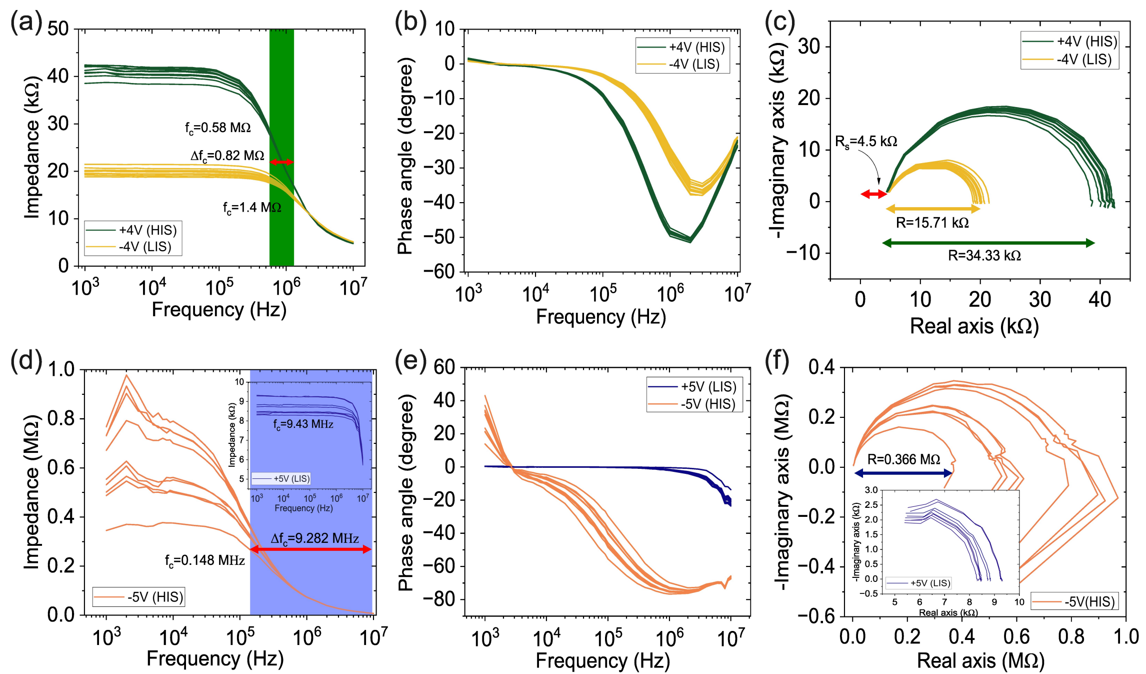

Figure 4.5: **AC impedance analysis of as-deposited and annealed HfO_x devices.** (a-c) As-deposited devices and (d-f) annealed devices. Panels (a,d) show the impedance magnitude as a function of frequency, highlighting the cut-off frequencies of the respective resistance states and the resulting tunable frequency band indicated by shaded green and blue regions in the respective plots. Panels (b,e) present the corresponding phase Bode plots. Panels (c,f) display Nyquist plots exhibiting depressed semicircular behaviour for both resistance states, from which the resistance (R) and series resistance (R_s) values are extracted. Reproduced from the author's own work [1].

It is important to emphasise that the resistance values extracted from impedance spectroscopy are systematically lower than the corresponding resistances obtained from low-bias DC measurements. This discrepancy reflects the fundamentally different physical regimes being probed. While DC measurements capture the static, quasi-equilibrium conduction through bulk defect pathways, the resistance extracted from Nyquist analysis represents a dynamic, frequency-dependent response governed by interfacial transport, charge redistribution, and

dielectric relaxation processes [156, 157]. Despite the difference in absolute magnitude, the relative resistance contrast between the two programmed states remains largely preserved under AC excitation, summarised in Table 4.2. These observations establish a clear baseline against which the impact of post-deposition annealing on resistive–capacitive coupling and dynamic frequency response is examined in the following subsection.

Annealed devices: The impedance response of annealed HfO_x devices differs qualitatively from that of as-deposited devices. Figures 4.5 (d)–(f) present the impedance magnitude, phase, and Nyquist representations measured in the two programmed states.

The impedance magnitude Bode plot shown in Fig. 4.5(d) retains a low-pass filter like profile. However, the cut-off frequency shifts over a much wider range between the two programmed states than in as-deposited devices, allowing expanded tunability. The corresponding phase Bode plots, shown in Fig. 4.5(e), provide further insight into the dynamic response. Annealed devices exhibit a markedly enhanced capacitive dominance, with the maximum phase angle approaching 80°. In contrast, the phase in as-deposited devices does not exceed 55°, even in the high-resistance state. This pronounced phase shift indicates that the capacitive contribution exerts stronger control over the total impedance in annealed devices across a broad frequency range. Notably, this occurs despite the lower absolute capacitance measured in annealed films. This behaviour arises from the substantially higher dynamic resistance introduced by annealing, which suppresses the resistive branch of the parallel RC network and allows the capacitive response to dominate over longer timescales. As a result, capacitive relaxation processes persist to higher frequencies, consistent with the improved frequency retention of the programmed capacitive states observed earlier.

Nyquist plots for annealed devices, shown in Fig. 4.5(f), reveal a pronounced asymmetry between the two impedance states. The HIS forms a well-defined but downward-depressed semicircular arc, similar to as-deposited. However, at higher frequencies shows a slight extension into the positive imaginary region. While such features are sometimes associated with inductive effects in electrochemical systems, the present data do not provide sufficient evidence to conclusively attribute this behaviour. Consequently, this low-frequency deviation is noted but not explicitly modeled. In contrast, the LIS does not exhibit a complete semicircular arc within the measured frequency window. Only the initial portion of the Nyquist contour is observed, suggesting that the characteristic relaxation frequency of the LIS lies beyond the upper limit of the measurement range. The absence of a closed semicircle in this state reflects instrumental bandwidth limitations rather than a breakdown of the assumed equivalent-circuit description.

Overall, the impedance response of annealed HfO_x devices demonstrates that thermal processing not only enhances resistive switching contrast but also fundamentally reshapes the dynamic resistive–capacitive coupling. These characteristics establish a clear functional distinction between as-deposited and annealed devices and provide a solid experimental basis for the equivalent-circuit modelling and parameter extraction discussed in the following section.

Equivalent circuit and Spice Model

The resistance (R) and series resistance (R_s) values extracted from the Nyquist analysis were subsequently used to construct an equivalent-circuit representation of the HfO_x devices,

Table 4.2: Electrical Characteristics of As-deposited and Annealed Samples, reproduced [1]

Sample	State	R_{dc} (kΩ)	C (pF)	Bode plot f_c (MHz)	Nyquist plot τ (μs)	Nyquist plot R (kΩ)	Equivalent circuit elements R (kΩ)	Equivalent circuit elements Q (10^{-12})	Equivalent circuit elements n
As deposited	**SET**	52	4	1.4	0.159	15.7	15.67	8.814	0.993
	RESET	109	6	0.58	0.265	34.3	33.92	9.29	0.99
Annealed	**SET**	30	1	9.43	–	4	–	–	–
	RESET	4×10^3	3	1.48	0.79	357	373	3.81	0.94

as illustrated in Fig. 4.6 (a)-(c). For both as-deposited and annealed devices, accurate reproduction of the experimental impedance spectra requires the replacement of an ideal capacitor with a CPE. As demonstrated by the close agreement between experimental data and fitted curves in Fig. 4.6 (b,c), the inclusion of a CPE is essential to account for the non-ideal, distributed nature of the capacitive response. The necessity of a CPE confirms that the impedance behaviour cannot be described by a single, well-defined relaxation process and instead reflects intrinsically non-ideal capacitive dynamics.

The extracted CPE exponent n serves as a quantitative indicator of deviation from ideal RC behaviour. Annealed devices consistently exhibit lower values of n compared to as-deposited samples, indicating a stronger departure from ideal capacitive behaviour. This reduction in n implies a broader distribution of relaxation times and points to increased heterogeneity in the dielectric landscape following thermal treatment. Such behaviour is consistent with structural reorganisation during annealing, including the formation of grain boundaries, modified electrode–oxide interfaces, and spatially varying defect environments.

To further validate the physical relevance of the extracted parameters, circuit-level simulations were performed using LTspice covered in Fig. 4.6 (d-f). When the experimentally derived equivalent-circuit topology is implemented, the simulated impedance response reproduces the key features of the measured spectra, confirming the validity of the extracted R and R_s values. However, because LTspice does not natively support CPE elements, simulations employing an ideal capacitor of equivalent nominal capacitance exhibit clear discrepancies relative to experiment, particularly in the phase response. As shown in Fig. 4.6 (e-f), the ideal RC model fails to capture the experimentally observed phase evolution across the frequency range, providing direct evidence that ideal capacitive descriptions are insufficient for these devices. From a physical perspective, the presence of a CPE implies fractional-order capacitive dynamics, arising from spatially distributed relaxation pathways within the oxide [158]. The more pronounced fractional behaviour observed in annealed devices suggests that annealing enhances the complexity of the internal relaxation landscape rather than simplifying it. This insight is particularly relevant for neuromorphic and bio-inspired hardware, where fractional-order elements have been shown to more accurately reproduce biologically relevant temporal dynamics [158].

Overall, the equivalent-circuit analysis demonstrates that the electrical behaviour of HfO_x memristor–memcapacitor devices is governed by intrinsically non-ideal capacitive dynamics. The stronger CPE behaviour observed in annealed devices underscores the role of structural reorganisation in shaping frequency response and relaxation behaviour, and establishes the necessity of modeling approaches that extend beyond ideal RC descriptions. These findings complete the electrical characterisation framework developed in this chapter and provide a robust physical basis for the conclusions drawn in the following section.

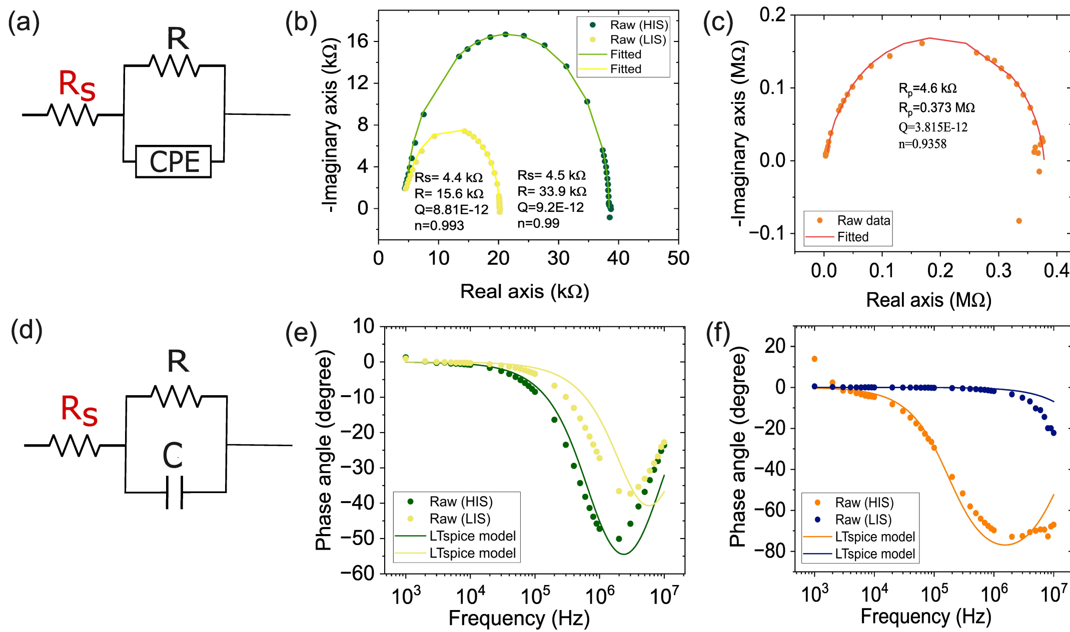

Figure 4.6: **Equivalent circuit modelling and fitting of impedance data for HfO_x devices.** (a) Randles-type equivalent circuit to fit the experimental impedance data. (b,c) Nyquist plots showing raw and fitted impedance responses for as-deposited and annealed devices, respectively, with extracted circuit parameters indicated. (d) Idealised R–C equivalent circuit employed for LTspice-based fitting to evaluate deviations from ideal capacitive behaviour. (e,f) Comparison between experimental phase–frequency characteristics and LTspice simulations for as-deposited and annealed devices, respectively. Reproduced from the author's own work [1].

4.4 Conclusion

This chapter has established the coupled memristive and memcapacitive behaviour of HfO_x devices through systematic DC, AC, and impedance spectroscopy, and validated an equivalent-circuit framework. As-deposited devices exhibit analogue resistive switching accompanied by reproducible binary capacitive switching, while annealed devices show enhanced resistive and capacitive ratio, stronger capacitive dominance, and extended frequency retention arising from a modified defect and interfacial landscape. Although the capacitive response in both cases is predominantly binary, the clear and reproducible separation of capacitance states represents a critical enabling step toward voltage-programmable capacitive elements. Impedance analysis further reveals intrinsically non-ideal, fractional-order capacitive dynamics, particularly in annealed devices. At the same time, the absence of stable intermediate capacitance states highlights a key challenge. Binary capacitive switching is sufficient to demonstrate functional tunability; however, advanced applications such as reconfigurable electronics and adaptive systems require access to multiple, independently addressable capacitance levels. This limitation motivates the transition to ferroelectric systems, where intrinsic polarisation switching provides a natural route to stable multistate capacitive behaviour, forming the focus of the following chapter.

Chapter 5

The Ferroelectric Memcapacitor

This chapter presents a comprehensive investigation of ferroelectric HZO based capacitors, with the objective of establishing a stable and optimised ferroelectric memcapacitor platform. Building on the oxide-based memcapacitor behaviour examined in previous chapter, the emphasis here shifts from defect-mediated dielectric effects to polarisation-driven capacitance modulation enabled by ferroelectric HZO. Unlike non-ferroelectric HfO_x devices, where capacitive changes are often inseparable from resistive conduction pathways, ferroelectric HZO provides a fundamentally different mechanism in which polarisation reversal directly modifies the internal electric field and effective permittivity. This chapter concentrates on how polarisation switching manifests electrically in practical device stacks and governs the non-volatile capacitive response. Understanding this polarisation-capacitance relationship is essential before pursuing the multistate memcapacitive functionality presented in the following chapter.

Hence, the current chapter is divided into four sections. First, an electrical characterisation framework is established to probe ferroelectric switching, capacitance modulation, and cycling behaviour. This framework is then applied to a baseline HZO device to analyse wake-up behaviour, polarisation evolution, and the resulting capacitive memory window. Subsequently, electrode engineering is investigated to understand how contact material influences switching symmetry and internal field distribution. Finally, dielectric stack engineering is explored as an independent pathway to enhance polarisation stability, memory window, and endurance, thereby defining a robust ferroelectric memcapacitor platform that underpins the multistate investigations presented in the subsequent chapter.

5.1 Characterisation Protocol

All ferroelectric characterisation in this work was carried out using a Keithley 4200-SCS parameter analyser equipped with the Pulse Measurement Unit (PMU) and Remote Pulse Module (RPM). This integrated platform provides a dedicated ferroelectric measurement environment, enabling precise voltage waveform generation and high-speed, time-resolved current acquisition within a single system. Crucially, it supports a suite of built-in characterisation protocols that together allow comprehensive evaluation of ferroelectric capacitors, spanning large-signal switching, small-signal dielectric response, and long-term cycling behaviour.

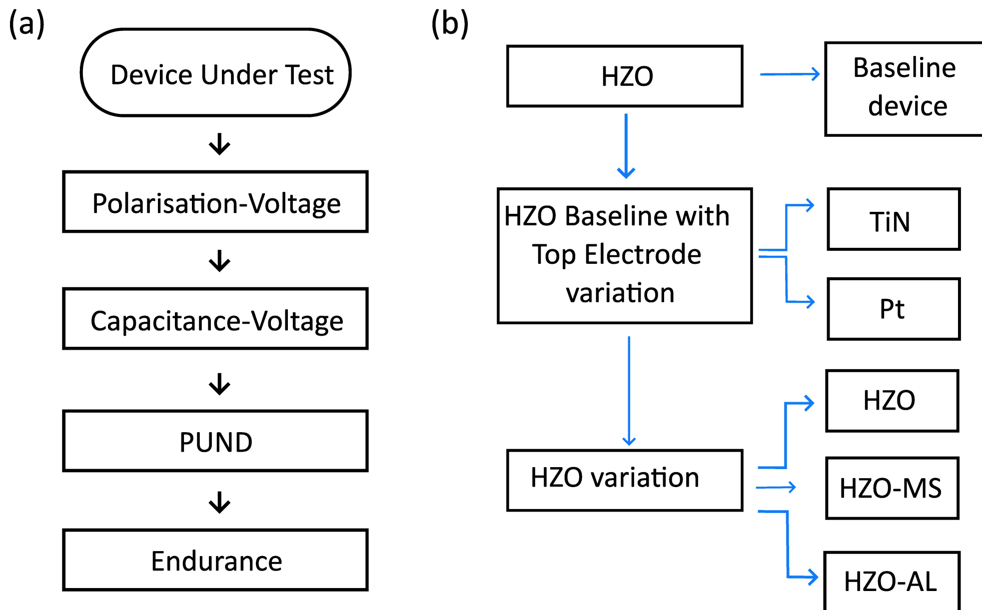

Figure 5.1: **Overview of the electrical characterisation workflow and device variants investigated in this chapter.** (a) Sequential ferroelectric characterisation protocol applied to each device under test. (b) Device hierarchy studied in this work, starting from a baseline HZO capacitor, followed by top electrode variation, and subsequently dielectric stack engineering through modified HZO structures.

A key advantage of this configuration is that it eliminates the need for external Sawyer-Tower circuitry, which has traditionally been used to extract ferroelectric polarisation. In the Sawyer-Tower method, the ferroelectric capacitor is connected in series with a large reference capacitor, and the polarisation is inferred indirectly from the voltage developed across this element. While widely adopted, this approach relies on voltage division and small signal amplitudes, making it susceptible to parasitic capacitances, leakage currents, and limited temporal resolution, particularly problematic for thin-film HZO devices with low switching charge. In contrast, the PMU/RPM system directly measures current and voltage synchronously at high sampling rates, enabling time-domain integration of the switching current to extract polarisation without series reference elements. This direct measurement capability is essential for resolving fast, low-amplitude switching events and for reliably linking polarisation dynamics to the accompanying capacitive response.

Accordingly, four complementary electrical characterisation protocols are employed in this study as shown in Fig. 5.1 and are discussed in the following subsections. First, the fundamental polarisation-voltage (P-V) characteristics and switching current evolution. Second, small-signal capacitance-voltage (C-V) capturing dielectric response and domain reconfiguration. Third, Positive–Up–Negative–Down (PUND) measurements to decouple true ferroelectric switching from non-switching and leakage contributions. Finally, endurance testing that evaluates the stability of polarisation under repeated cycling. Together, these techniques establish a complete picture of large-signal polarisation dynamics, small-signal permittivity modulation, and device reliability.

5.1.1 Polarisation-Voltage Measurement

The first step in ferroelectric characterisation is to establish the presence of genuine polarisation switching and to distinguish functional ferroelectric devices from non-ideal or defective structures. This is achieved using large-signal voltage excitation to directly probe domain reversal and the associated displacement current. In this work, polarisation behaviour is evaluated using triangular voltage pulse measurements, which provide a robust and widely adopted method for extracting the fundamental *P–V* characteristics of ferroelectric capacitors. In addition to revealing intrinsic switching behaviour, this measurement serves as a screening tool to identify devices suitable for further electrical analysis.

Ferroelectric hysteresis loops were recorded using a symmetric triangular voltage waveform. The linear voltage ramp ensures a constant dV/dt, allowing the measured current to be directly integrated over time to obtain the total charge according to $Q(t) = \int I(t)\,dt$. By sweeping the applied voltage continuously between positive and negative extremes, the electric field is driven through both polarisation states within each cycle, enabling direct extraction of remanent polarisation (P_r), coercive voltage (V_c), and saturation polarisation (P_s) from the resulting charge-voltage response.

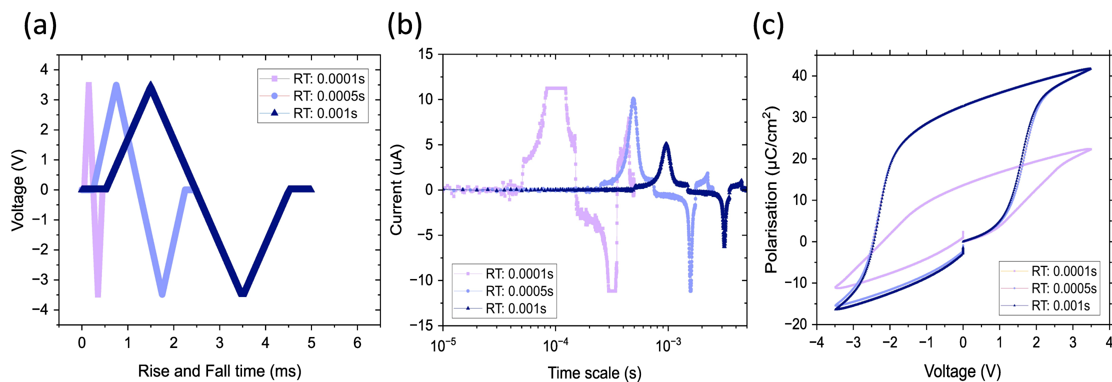

Figure 5.2: **Effect of rise–fall time on ferroelectric switching behaviour.** (a) Applied bipolar waveforms with rise/fall times of 100 μs, 500 μs, and 1 ms. (b) Corresponding switching currents showing sharper, higher transients for fast ramps and broadened, lower-amplitude peaks for slow ramps. (c) Resulting P-V loops, where fast ramps yield well-defined ferroelectric hysteresis and slower ramps produce constricted loops due to reduced switching efficiency. Reproduced from authors work [159].

The ability to resolve a clear ferroelectric switching response depends critically on the duration of the applied voltage ramp. Figure 5.2 illustrates the influence of rise and fall time on the measured switching behaviour. When the voltage is ramped too rapidly (e.g. 0.0001 s), the electric field changes faster than the ferroelectric domains can respond, leading to distorted current peaks and incomplete polarisation reversal. As the ramp duration increases, domains are given sufficient time to reorient, resulting in well-defined displacement current peaks and closed *P–V* hysteresis loops. Beyond a threshold rise/fall time of approximately 0.0005 s in the present system (corresponding to a ramp frequency of $\sim$2 kHz), the total switched charge saturates. Further increases in ramp duration broaden the current transient but do not increase the integrated charge, indicating that full polarisation reversal has already been achieved.

Based on these observations, a triangular waveform with a rise/fall time of 0.001 s was

selected for all subsequent polarisation measurements. Representative device responses obtained under identical pulse conditions are shown in Figure 5.3. Four characteristic behaviours were identified:

(a) The first type shows highly noisy and unstable current transients, resulting in scattered or open charge–voltage loops. Such behaviour is attributed to poor electrical contact or intermittent leakage pathways, which limits ferroelectric response.

(b) The second type exhibits distorted or asymmetric current peaks with significantly lower current magnitude compared to the ferroelectric case. The corresponding charge loops are irregular and weakly polarised, suggesting non-uniform interfaces or dipolar contributions rather than domain switching. As the switching current is several orders of magnitude lower than in a genuine ferroelectric device, repeated cycling does not lead to any wake-up or improvement in the loop shape.

(c) The third type displays nearly rectangular current waveforms and diamond-shaped charge voltage loops, indicative of purely capacitive or resistive behaviour with negligible remanent polarisation, typically corresponding to shorted or non-ferroelectric structures.

(d) In contrast, the fourth type shows sign of displacement current peaks of opposite polarity and a closed hysteresis. It does require wakeup cycles discussed in further section to reach maximum polarisation but does confirm genuine ferroelectric switching.

Only the devices exhibiting the fourth behaviour were selected for detailed analysis, as they demonstrate reproducible polarisation reversal under triangular voltage excitation.

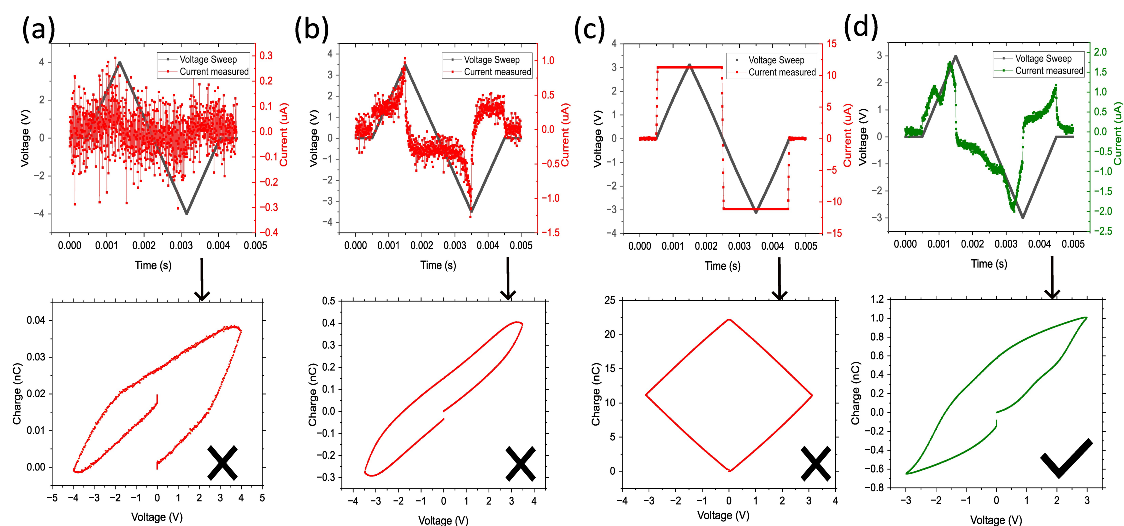

Figure 5.3: **Illustration of common measurement artefacts in polarisation switching.** (a–c) Three incorrect charge-integration cases showing noisy current, incomplete switching, or distorted waveforms leading to invalid P-V loops. (d) Correct measurement producing a clean displacement current and a physically meaningful ferroelectric loop.

5.1.2 Capacitance–Voltage Measurement

While the triangular waveform discussed earlier captures the large-signal polarisation switching behaviour, C–V measurements provide complementary insight into the field-dependent dielectric response of the same ferroelectric capacitors. The C–V technique is particularly useful for examining local permittivity changes associated with domain alignment, internal bias, and interfacial asymmetry, thereby enabling direct correlation between dielectric tunability and the underlying polarisation state. As described by Equation (5.1), the capacitance of a ferroelectric layer can be expressed as

$$\frac{C}{A} = \frac{\varepsilon_0 \varepsilon_r}{t} \left(1 + \frac{1}{\varepsilon_0 \varepsilon_r} \frac{dP_f}{dE} \right), \tag{5.1}$$

where t is the film thickness, ε_r is the intrinsic dielectric constant, and dP_f/dE represents the differential change in ferroelectric polarisation with the applied electric field [160]. The first term corresponds to the linear dielectric contribution, while the second term reflects the field-dependent component arising from domain dynamics. In ferroelectric capacitors, this coupling gives rise to the characteristic "butterfly" C–V profile, with capacitance maxima appearing near the coercive voltages due to enhanced differential polarisation (dP/dE). The central region of the loop corresponds to the low-field dielectric state, while the peaks reflect partial domain reorientation during switching.

The C–V measurements were performed using a slowly swept DC bias with a superimposed small-signal AC excitation. The AC perturbation probes the differential permittivity at each bias point without inducing additional domain switching, while the DC bias gradually modifies the domain configuration. In this work, a 30 mV, 10 kHz AC signal was selected to ensure linear small-signal operation: the amplitude is sufficiently low to avoid depolarising or moving domain walls, yet large enough to provide a stable capacitance signal above the noise floor. The DC bias was swept between ±3.5 V and ±3 V using a step size of 0.1 V.

The voltage range used for C–V measurements was slightly reduced relative to the P–V characterisation to account for the slower nature of the DC sweep, during which the device experiences sustained electric fields at each bias point. Extended dwell times can promote leakage-driven degradation or dielectric breakdown, particularly in larger-area capacitors. A finer voltage step of 0.01 V was also evaluated but led to premature failure in several devices, whereas smaller-area capacitors exhibited greater resilience under the same conditions. Devices showing irreversible leakage or degradation at this stage were excluded from further analysis.

To evaluate the non-volatile capacitance associated with individual programmed polarisation states, a two-step measurement protocol was adopted. Each state was first programmed using a controlled DC bias sweep with a step size of 0.1 V. Following programming, the capacitance was measured at zero DC bias using the same 30 mV, 10 kHz AC excitation. The AC readout was maintained for approximately one minute to obtain a stable, time-averaged capacitance value representative of the programmed dielectric state. This post-sweep readout scheme enables direct correlation between the applied programming voltage and the resulting non-volatile capacitance, forming the basis for subsequent multistate analysis.

5.1.3 PUND and Endurance Measurement

The PUND test and endurance cycling were performed to isolate the genuine ferroelectric switching response and evaluate its stability under repeated electrical stress. The PUND sequence consists of four unipolar voltage pulses: Positive (P), Up (U), Negative (N), and Down (D). The first pulse of each polarity (P or N) reverses the domain orientation relative to the previous state, thereby generating a transient displacement current associated with polarisation switching. The subsequent pulse of the same polarity (U or D) produces only the background dielectric response, as the domains are already aligned in that direction. A well-behaved ferroelectric capacitor therefore exhibits sharp, symmetric switching peaks during the P and N pulses, superimposed on the dielectric current, followed by low and stable dielectric currents during the U and D pulses. Hence, the actual switching current can be extracted from the difference between the P-U and N-D current profiles.

When a time-varying electric field is applied across the ferroelectric layer, the total current density can be described as

$$J_{\text{tot}} = J_{\text{C}} + J_{\text{D}} = \sigma E + \frac{\partial D}{\partial t} = \sigma E + \varepsilon_0 \frac{\partial E}{\partial t} + \frac{\partial P}{\partial t}, \tag{5.2}$$

where σE represents the leakage current, $\varepsilon_0 \frac{\partial E}{\partial t}$ is the reversible dielectric contribution, and $\frac{\partial P}{\partial t}$ corresponds to the time-dependent ferroelectric polarisation switching term [161]. The large transient peaks observed during the P and N pulses occur when $\frac{\partial P}{\partial t}$ dominates, while the background current during the U and D pulses is primarily dielectric. By monitoring how these transient and background components evolve with cycling, true ferroelectric switching can be distinguished from non-switching processes.

Endurance testing extends this concept to long-term electrical stress. Alternating bipolar voltage pulses of fixed amplitude and timing were applied continuously, ensuring that all domains undergo repeated reversal. Periodically, the individual P, U, N, and D responses were recorded to track their evolution as a function of cycle count. In the initial stages, many devices exhibit characteristic wake-up behaviour, manifested as an increase in polarisation with cycling, arising from the redistribution of oxygen vacancies, depinning of trapped charges, and stabilisation of the orthorhombic phase. At higher cycle numbers, gradual degradation may occur due to defect generation, interfacial charge build-up, or partial domain pinning, leading to reduced polarisation and asymmetric switching currents.

Overall, the combined PUND and endurance protocol provides a comprehensive picture of ferroelectric reliability, capturing both the transient switching dynamics and their long-term stability.

5.2 HZO:The baseline Device

The electrical characterisation was first performed on TiN/HZO/TiN capacitors annealed at 500 °C with a dielectric thickness of 10 nm, which serves as the reference device for subsequent comparisons.

5.2.1 Polarisation-Voltage Analysis

Polarisation-voltage measurements confirm that the TiN/HZO/TiN capacitors exhibit ferroelectric switching behaviour. Figure 5.4 shows the evolution of switching current and polarisation under consecutive bipolar triangular voltage sweeps. The progressive change in the hysteresis response with repeated cycling is commonly referred to as the wake-up effect, a characteristic feature of HZO-based ferroelectrics, in which the remanent polarisation gradually increases during early electrical cycling [137, 162].

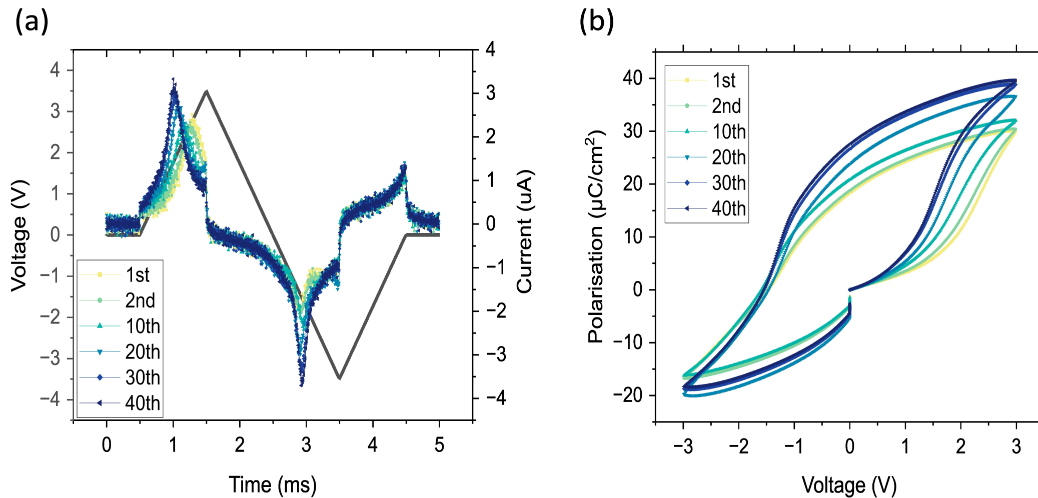

Figure 5.4: **Wake-up behaviour of the HfZrO ferroelectric capacitor.** (a) Evolution of the switching current over successive bipolar cycles, showing progressive sharpening of the transient peaks. (b) Corresponding P-V loops, illustrating the increase in remanent polarisation as wake-up proceeds.

In the first run, the polarisation hysteresis loop is narrow and the switching current peaks are broad and shallow, indicating that only a limited fraction of the film participates in polarisation reversal during the first cycle. This reduced initial response arises from two primary factors. First, annealed HZO films exhibit a heterogeneous phase composition, in which ferroelectric orthorhombic grains coexist with non-ferroelectric monoclinic and tetragonal phases, as confirmed by XRD analysis. Since only the orthorhombic phase supports ferroelectric switching, the initial cycle reflects polarisation reversal within a sparse and spatially non-uniform population of active grains. Second, the pristine film contains a non-equilibrium distribution of oxygen vacancies and trapped charges that generate local internal electric fields. These fields distort the ferroelectric double-well energy landscape and immobilise clusters of domains, further suppressing their contribution to the initial switching response [137, 162].

As the device undergoes repeated bipolar cycling, the switching peaks sharpen and the hysteresis loop progressively expands, typically saturating after ∼30–40 cycles. This increase in switchable polarisation reflects the gradual activation of previously inactive regions and constitutes the wake-up process. This enhancement reflects the gradual removal of structural and defect-related constraints that limit ferroelectric switching in the pristine state [163, 115].

Starting with defect-driven depinning, the wake-up process is strongly influenced by interfa-

cial effects. In TiN/HZO stacks, the TiN electrode possesses a finite oxygen affinity and forms a thin TiON interlayer at the interface. During bipolar cycling, field-assisted redox interactions partially equilibrate the interfacial oxygen vacancy concentration, reducing interfacial asymmetry and lowering the depolarising field. This redistribution of oxygen vacancies away from the HZO/TiN interface into the bulk, together with depopulation of shallow trap states, reduces local internal bias fields that initially pin ferroelectric domains. As these regions become switchable, both the switching current and the remanent polarisation increase, producing the characteristic sharpening of the displacement current peaks. Oxygen vacancies play a multifaceted role in this process, contributing to spontaneous polarisation while simultaneously acting as sources of leakage current [163, 115].

In addition to defect-mediated effects, repeated electrical cycling promotes partial conversion of metastable tetragonal grains into the orthorhombic ferroelectric phase [137]. Grain regions initially locked in mixed-phase configurations also undergo subtle structural rearrangements, increasing the overall volume fraction of switchable orthorhombic material. This phase evolution explains why wake-up increases the effective switching volume, rather than merely improving the mobility of domains that were already ferroelectric.

Overall, the wake-up process can be regarded as a reversible forming phenomenon, analogous to the forming step in memristive devices. Unlike filamentary forming in resistive memories, wake-up in ferroelectrics is non-destructive and instead reorganises the internal defect landscape and phase distribution to activate the full switchable polarisation. In most devices, the polarisation stabilises after wakeup cycles, beyond which further cycling induces little additional change. This stabilised, fully awakened state defines the baseline condition for interpreting the capacitance–voltage behaviour discussed in the next section, where the C–V sweep interacts strongly with the same defect dynamics.

5.2.2 Capacitance-Voltage Analysis

The C-V characteristics of the TiN/HZO/TiN ferrroelectric capacitors exhibit the expected butterfly-shaped C-V profile; however, the measured capacitance behaviour extends beyond this conventional signature. In particular, the applied DC voltage sweep does not merely probe the dielectric response, but actively modifies the internal ferroelectric state in a manner that depends strongly on the sweep direction and the underlying defect configuration.

Accordingly, the discussion of the C-V behaviour is structured in two stages. First, the influence of sweep direction on the resulting C-V profile and its correlation with the subsequent P-V response is examined. This analysis establishes the appropriate sweep protocol used throughout the remainder of the thesis and highlights the role of bias direction in programming the ferroelectric state. Building on this understanding, the following subsection presents a detailed analysis of the C-V characteristics, focusing on peak asymmetry, non-zero capacitance crossing at zero bias, the resulting capacitance memory window, and the stability of the programmed capacitive states. Together, these observations form the basis for identifying and quantifying non-volatile capacitive states in the ferroelectric memcapacitor.

Sweep-Direction Dependence

Figure 5.5 compares the C-V characteristics obtained when the voltage sweep is initiated from positive and negative polarity. Although both traces exhibit the expected butterfly-shaped profile, the overall symmetry, peak amplitudes, and crossing voltage differ markedly depending on the starting polarity. These differences directly influence the subsequent P-V response and therefore provide insight into the internal defect landscape of the TiN/HZO/TiN stack.

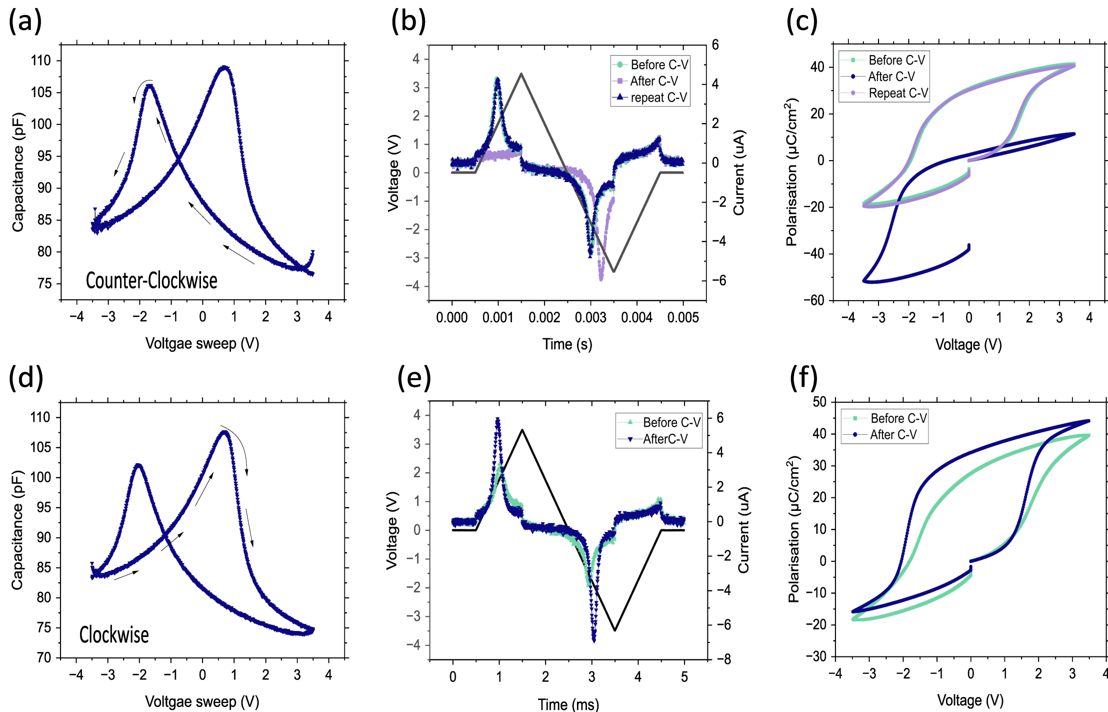

Figure 5.5: **Influence of C–V sweep direction on subsequent ferroelectric switching behaviour.** (a–c) Counter-clockwise C–V cycling with relatively symmetric CV, leaving the device in the opposite polarity polarisation. (d–f) Clockwise C–V cycling produces asymmetric butterfly peaks and a shifted crossing point, which subsequently modify the displacement current and increased polarisation window.

When the sweep begins from the positive side as shown in Fig. 5.5 (a), the resulting C-V curve appears comparatively symmetric, with capacitance maxima of similar magnitude at both polarities. The triangular *P–V* loop measured immediately afterwards shows an oppositely polarised state, and with repeated *P–V* cycling the response returns to the original state, Fig. 5.5 (b-c). No noticeable change is observed in the polarisation curve, indicating that most switchable domains were already activated during the earlier triangular-pulse wake-up cycling, and that the positive-start sweep does not significantly perturb the existing defect distribution or structural state of the film.

A noticeable different response occurs when the sweep is initiated from the negative side, shown in 5.5 (d-f). The P-V loop recorded after this sweep shows a substantial increase in saturation polarisation. It is larger than what 100s of triangular-pulse cycles alone can achieve. This enhancement indicates that there were domains that were still pinned. One plausible interpretation could be that a negative-start sweep begins with the polarisation oriented against the residual internal field, forcing a more aggressive rearrangement of oxy-

gen vacancies and defect dipoles in order to stabilise the polarisation in that unfavourable direction. This early redistribution depins inactive domains and promotes a more uniform orthorhombic ferroelectric phase. By the time the sweep reaches positive bias, the device has already been "reset" into a more activated state, which explains the enhanced P-V saturation. In contrast, a positive-start sweep initially reinforces the preferred internal dipole orientation. During this initial segment, defects and traps experience little driving force to migrate or relax, so the internal configuration remains close to its pre C-V state. This interpretation is supported by the corresponding C-V characteristics, where the butterfly curve becomes more asymmetric, one capacitance peak becomes higher than its counterpart, and the crossing point of the forward and reverse branches shifts further away from zero bias. In conclusion, a negative-start sweep activates more domains and increases the polarisation, but because the quasi-static dwell times also allow oxygen vacancies and trapped charges to drift, the resulting internal bias becomes stronger, making the C–V loop more asymmetric even though the ferroelectric response is enhanced.

The asymmetry and peak distortion observed in the negative-start C-V curves therefore reflect a reconfiguration of the internal electrostatic and structural landscape of the HZO layer. A larger capacitance peak on one branch signifies that a greater fraction of domains participates in switching for that polarity, while the peak shift indicates the presence of a residual, partially relaxed internal bias. As the negative-start configuration yields the highest saturation polarisation and most complete activation of domain switching, all subsequent C-V measurements in this chapter are performed using this sweep direction.

Non-zero Crossing Point and Memory Window

In an ideal symmetric TiN/HZO/TiN capacitor, the forward and reverse branches of the C-V loop would intersect precisely at zero bias, indicating that equal external fields are required to switch the polarisation in the positive and negative directions. However, as shown in Fig. 5.6 (a), the crossing point is displaced toward negative voltage. This displacement reflects a residual built-in field inside the film, arising from a non-uniform distribution of oxygen vacancies, asymmetric interfacial dipoles, and differences in local interface chemistry between the top and bottom TiN electrodes [122, 163, 164]. Although the wake-up process discussed earlier reduces the dominant component of this internal field, it does not eliminate all sources of asymmetry. These residual contributions shift the effective double-well potential and bias the capacitor toward one polarisation orientation, causing the C-V branches to cross at a non-zero voltage. Importantly, such asymmetry is not merely a parasitic effect but a necessary condition for enabling a non-zero capacitance memory window, as discussed in Chapter 2.

Beyond the crossing point, the positions of the capacitance maxima provide further information about the coercive field. The peaks occur near the voltages where the $\mathrm{d}P/\mathrm{d}E$ is largest, around -2 V and $+0.5$ V in Fig. 5.6 (a). These values correspond closely to the current peaks observed in triangular P–V measurements; however, a slight mismatch in voltage is expected. The triangular waveform probes the moment of maximum $\mathrm{d}P/\mathrm{d}t$, whereas the C–V sweep probes the maximum $\mathrm{d}P/\mathrm{d}E$. Both therefore identify the coercive region, but through different dynamical pathways.

Figure 5.6(b) shows that the baseline TiN/HZO/TiN capacitor exhibits a clear capacitance memory window (CMW) at zero DC bias. The two capacitive states defining the extrema of

this window are accessed by applying bias sweeps of opposite polarity, analogous to the write operation in resistive memories. As illustrated in Fig. 5.6(c), a positive programming sweep ramps the voltage from $0 \rightarrow +3 \rightarrow 0$, while a negative sweep ramps from $0 \rightarrow -3 \rightarrow 0$. Although both sweeps span the same voltage range, they prepare the ferroelectric in opposite remanent polarisation states upon returning to zero bias. As a result, the capacitor relaxes into one of two stable dielectric configurations, corresponding directly to the two branches observed in the zero-bias CMW in Fig. 5.6(b).

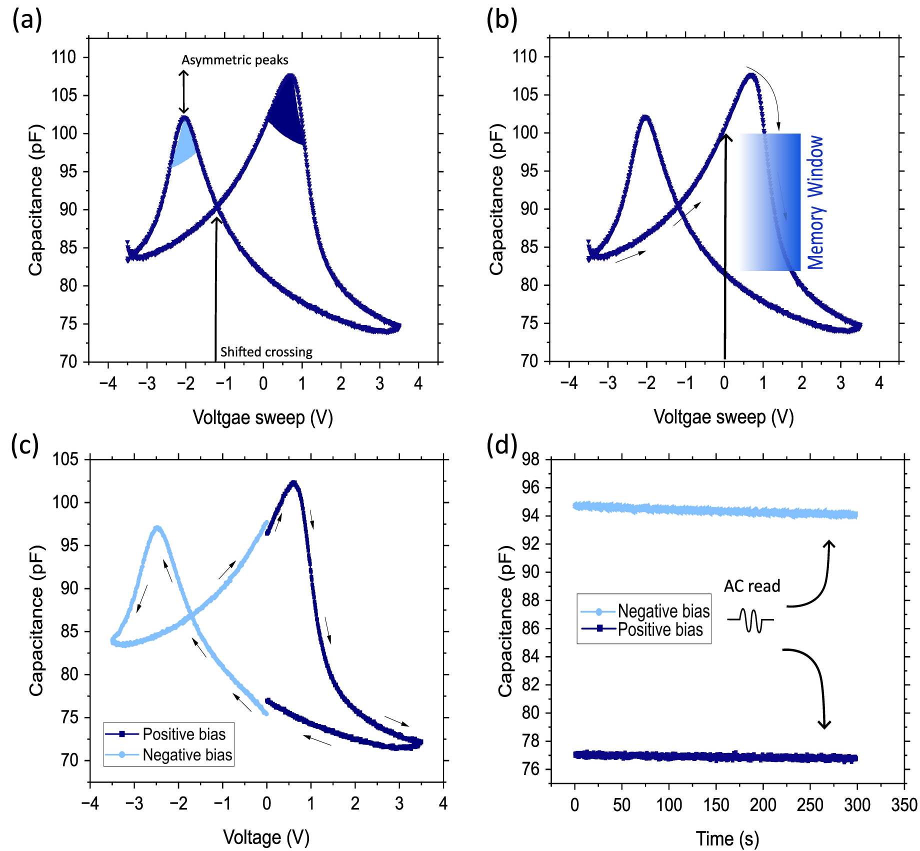

Figure 5.6: **C–V characteristics and zero-bias retention in TiN/HZO/TiN capacitors.** (a) Full C–V sweep showing asymmetric peak amplitudes and a crossing point shifted away from 0 V, indicating internal-field asymmetry. (b) Illustration of the resulting capacitance memory window (CMW) obtained from the vertical separation of the two branches at zero bias. (c) Programming sweeps using positive and negative bias, demonstrating the preparation of two distinct remanent capacitance states through sweep-direction–dependent switching. (d) Non-destructive AC reads confirming stable zero-bias retention of the two programmed states, establishing a clear non-volatile capacitance window.

The programmed states are subsequently read non-destructively at zero bias using a 30 mV, 10 kHz AC probe mentioned before and as shown in Fig. 5.6(d). The measured capacitance remains stable over time, with only minor initial relaxation, confirming that the observed contrast is non-volatile rather than a transient dielectric softening effect. For the representative baseline device, the two zero-bias states differ by approximately 16 pF, establishing a robust CMW. Importantly, because both states are retained at zero applied DC field, no static power is required to store information. This zero-bias retention forms the foundation for non-volatile memcapacitor operation. The following sections therefore focus on completing

the remaining characterisation protocols required to establish the robustness and reliability of device before tuning into mutlibit.

5.2.3 PUND and Endurance Analysis

Figure 5.7 presents the PUND response of the baseline TiN/HZO/TiN capacitor and its evolution under repeated cycling. The presence of sharp, well-defined current transients exclusively during the P and N pulses, accompanied by substantially weaker U and D responses, provides direct confirmation that the observed switching originates from genuine ferroelectric polarisation rather than dielectric or leakage effects. The cycle evolution of the same reveals that the four components do not degrade uniformly. While the U current remains small and nearly constant with cycling, the D current exhibits a markedly different evolution, indicating that the background current is influenced by an internal-field landscape rather than being purely dielectric.

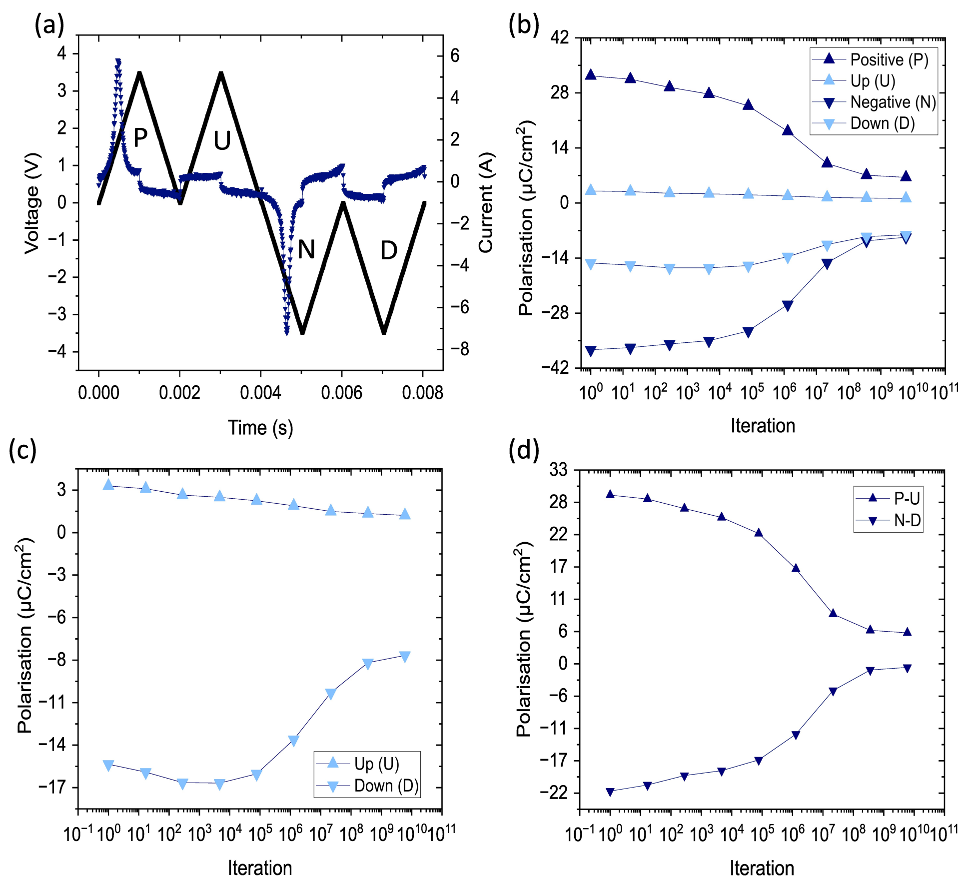

Figure 5.7: **PUND and endurance analysis of TiN/HZO/TiN capacitors.** (a) Applied PUND waveform and corresponding current transients, showing clear switching peaks during P and N and smaller non-switching currents in U and D. (b) Evolution of all four PUND components over cycling, revealing gradual reduction in switchable polarisation and asymmetry in the non-switching currents. (c) Separate plot of U and D components, highlighting their unequal magnitudes and cycle-dependent relaxation. (d) Extracted switchable charge (P–U and N–D), showing progressive fatigue and polarity-dependent degradation.

In an ideal symmetric ferroelectric capacitor, the U and D currents would be nearly identical. In real HZO-based devices, however, the non-switching current contains several contributions:

$$J_{U,D}(t) = \varepsilon_0 \frac{\partial E}{\partial t} + \sigma E + J_{\text{defect}}(t), \tag{5.3}$$

where $\varepsilon_0 \frac{\partial E}{\partial t}$ represents the reversible dielectric current, σE the leakage contribution, and $J_{\text{defect}}(t)$ accounts for slow defect-related processes such as oxygen vacancy drift, trapped charge relaxation, and internal-field redistribution.

As shown explicitly in Fig. 5.7 (c), the U and D components evolve very differently with cycle count. The U current remains weak and decreases only slightly, whereas the D current is initially much larger and decays substantially with cycling. This asymmetry reflects the fact that defect and vacancy motion responds asymmetrically to the applied electric field. In the TiN/HZO/TiN stack, the built-in internal field biases the film toward one polarisation orientation. Consequently, the U pulse, which aligns with this internal bias, induces minimal defect redistribution, while the D pulse, which opposes the built-in field, drives significant defect relaxation currents that gradually diminish as the vacancy distribution evolves toward equilibrium.

After subtraction of the non-switching background, the extracted switchable components (P−U) and (N−D) are shown in Fig. 5.7(d). Both components decrease gradually with cycle count, indicating the onset of ferroelectric fatigue under repeated electrical stress, with measurable degradation initiating at relatively low cycle counts on the order of 10^3 cycles. The decay is smooth rather than abrupt, suggesting progressive degradation rather than catastrophic breakdown of the ferroelectric response. Despite this reduction, ferroelectric switching remains observable beyond this regime, confirming functional endurance of the baseline device. Notably, even after background subtraction, a clear asymmetry persists between the (P−U) and (N−D) branches. This residual difference demonstrates that the asymmetry is intrinsic to the ferroelectric stack rather than an artefact of non-switching current contributions. The unequal convergence of the two switching branches reflects a built-in internal-field environment imposed by the asymmetric TiN/HZO interfaces, which biases the stability and reversibility of the two polarisation states differently.

Together with the *P–V* and *C–V* results, these observations establish the baseline TiN/HZO/ TiN device as a functional ferroelectric memcapacitor capable of non-volatile capacitance switching. While the HZO capacitor demonstrates a reproducible capacitance memory window, its magnitude remains modest for advanced multistate applications, and long-term cycling stability is limited by leakage-assisted degradation and interfacial asymmetry. To address these limitations, two optimisation routes are explored: electrode engineering and dielectric stack variation. The physical rationale for each approach and its impact on device behaviour are discussed in the respective sections.

5.3 Effect of Top Electrode

Platinum (Pt) is frequently employed in ferroelectric HZO studies owing to its chemical inertness and its ability to suppress wake-up and reduce leakage current [146]. Motivated by this report, Pt was introduced as the top electrode in the present study to evaluate whether a symmetric, low-defect interface could improve the polarisation and capacitance

behaviour of the device. The bottom TiN electrode, however, plays a critical role in stabilising the orthorhombic ferroelectric phase in HZO and was therefore retained. Figure 5.8 (a)-(b) compares the displacement current and P-V characteristics of TiN/HZO /TiN and Pt/HZO/TiN (Pt(TE)) devices. The Pt(TE) device exhibits noticeably broader and lower switching peaks, which translate into a wider, softer hysteresis loop with reduced saturation polarisation. Additionally, the coercive voltages shift slightly to higher value, reflecting changes in the internal-field landscape. Although previous works do not explicitly report such coercive-field variations, the behaviour is complex and difficult to interpret solely from the *P-V* loop.

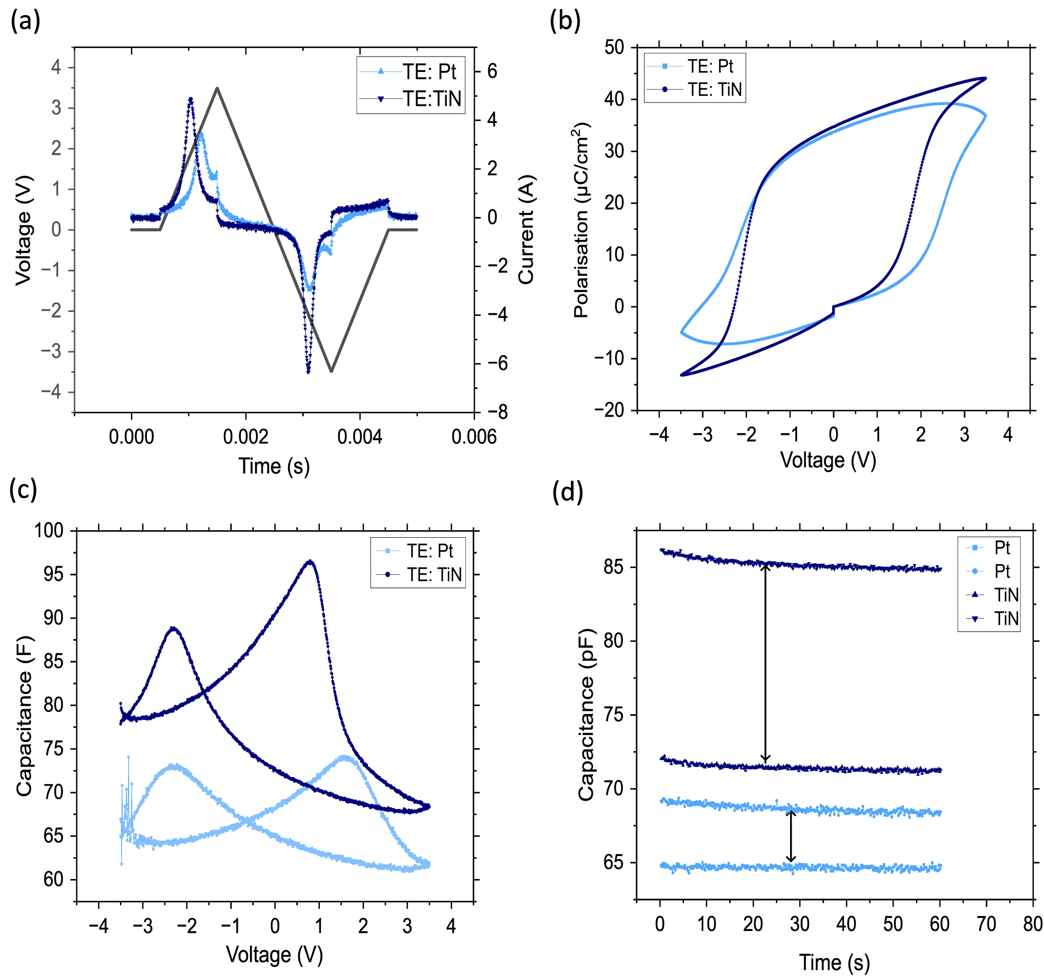

Figure 5.8: **Comparison of TiN/HZO/TiN and Pt/HZO/TiN capacitors.** (a) Displacement-current response showing broader, lower switching peaks for the Pt device. (b) Corresponding *P–V* loops, where Pt exhibits reduced saturation and altered coercive voltages. (c) Quasi-static *C–V* curves: Pt shows significantly lower capacitance, symmetric peak amplitudes, and a crossing point near 0 V, unlike the higher-tunability, asymmetric TiN device. (d) Zero-bias AC reads after programming, highlighting the much smaller memory window in the Pt stack.

However, the corresponding C-V data provide a clearer insight. The contrast becomes more striking in the C-V characteristics shown in Fig. 5.8 (c) -(d). The Pt device exhibits (i) much lower absolute capacitance, (ii) nearly symmetric butterfly peaks, and (iii) a crossing

point shifted much closer to 0 V relative to the TiN device. This behaviour is consistent with a reduced internal field arising from the chemically inert Pt/HZO interface. Unlike TiN, which can scavenge oxygen during deposition or during early cycling, Pt does not promote vacancy migration, thereby suppressing the strong built-in fields typically associated with oxygen-reactive TiN and leading to more symmetric peak amplitudes. However, despite the improved symmetry, the overall capacitance tuneability collapses. The Pt device shows only a narrow variation of ∼65-72 pF, in contrast to the much larger tunability of ∼80-96 pF obtained with TiN.

This significant reduction in capacitance doesn't follow the P-V as devices with Pt (TE) still produces comparable polarisation magnitudes. Instead, the lower capacitance is attributed to the formation of a thin, low-permittivity interfacial dead layer at the Pt/HZO boundary. Because Pt does not scavenge oxygen from HZO, it forms a relatively inert interfacial layer, often described as a "dead" interface [165].Such interfacial layers, extensively reported in nanoscale capacitors, act as an additional series capacitor and reduce the measured capacitance even when the ferroelectric bulk remains unchanged. Hence, the observed capacitance can be written as;

$$\frac{1}{C_{\text{observed}}} = \frac{1}{C_{\text{bulk}}} + \frac{1}{C_{\text{dead layer}}}. \tag{5.4}$$

Even a few angstorm of a low-ε interfacial oxide at the Pt/HZO interface can dominate the total capacitance, sharply reducing the observed C-V swing and the resulting memory window. This explains why the Pt/HZO device displays extremely small tunable range. Furthermore, the programmed and read capacitance state in Fig. 5.8 (d) confirm that the Pt device retains low capacitive contrast, yielding a memory window too small for reliable tuning.

In summary, Pt electrodes can be beneficial in applications where symmetric switching and reduced built-in fields are desirable. However, in the present context, a certain degree of built-in asymmetry is essential for achieving large, stable capacitance contrast, and Pt suppresses this beneficial asymmetry while simultaneously introducing an interfacial dead layer. For this reason, TiN remains the preferred top electrode for achieving strong, non-volatile memcapacitive behaviour.

5.4 Material Stack Engineering

Beyond electrode engineering, dielectric stack modification provides an additional route to tailor ferroelectric HZO capacitors. In this work, two modified dielectric configurations were fabricated and benchmarked against the baseline single-layer HZO device: (i) a multi-stack structure (HZO-MS) composed of alternating HfO_2/ZrO_2 sublayers (5:5 supercycles), and (ii) a bilayer configuration (HZO-Al) incorporating a nominally 1 nm Al-rich layer positioned at the centre of the HZO film, as described in Chapter 3. The multi-stack design is motivated by reports that HfO_2/ZrO_2 superlattices enhance the orthorhombic phase fraction through interfacial strain and composition modulation, leading to higher remanent polarisation and improved endurance [166, 167, 130]. By contrast, ultrathin Al_2O_3 or Al-rich interlayers have been proposed as a means to tailor wake-up behaviour and leakage current, although their impact on ferroelectric phase stability remains strongly dependent on thickness and position

within the stack. Figure 5.9(a) compares the *P-V* characteristics of the three devices. The baseline HZO device shows the expected hysteresis. The HZO–MS device exhibits a modest but consistent enhancement of both P_r and P_s, together with slightly steeper switching near the coercive field. This behaviour is consistent with earlier superlattice studies, where the repeating HfO_2/ZrO_2 interfaces stabilise the orthorhombic phase and promote more uniform domain switching across the film thickness [166, 167].

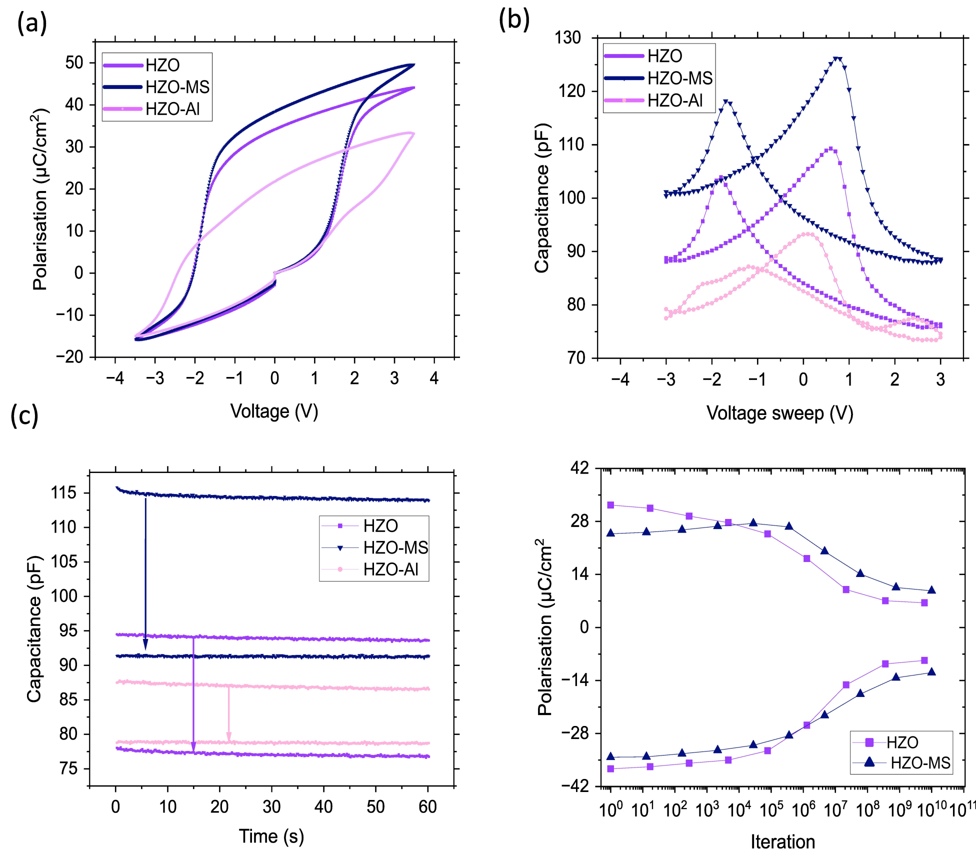

Figure 5.9: **Comparison of stack-engineered HZO capacitors.** (a) P-V loops for HZO, HZO-MS, and HZO-Al devices, showing enhanced switching in HZO-MS and suppressed ferroelectricity in HZO-Al. (b) Corresponding C-V characteristics, where HZO-MS exhibits the largest capacitance swing and memory window, while HZO-Al loses the butterfly response. (c) Zero-bias read-capacitance traces confirming stable non-volatile contrast in HZO and HZO-MS, but strongly reduced window in HZO-Al. (d) Endurance evolution of the switchable polarisation for HZO and HZO-MS, demonstrating improved cycling stability in the multi-stack structure. Reproduced from authors own work [159]

In contrast, the HZO-Al device exhibits a markedly slimmer loop, reduced P_r, and a more slanted shape, indicating that the effective ferroelectric volume is reduced and that a larger fraction of the film responds as a high–κ dielectric rather than a switchable ferroelectric. Since the Al-rich layer is embedded in the middle of the stack rather than at the metal interface, it likely interrupts the continuity of orthorhombic grains and introduces a non-ferroelectric region that screens part of the depolarising field, thereby suppressing long-range domain correlation. The corresponding *C-V* characteristics in Fig. 5.9 (b), together with the zero-bias capacitance traces in Fig. 5.9 (c), reinforce this picture and, importantly, reveal a direct correlation between polarisation and capacitance across all three stacks. The HZO-MS

capacitor displays higher peak capacitance, a broader butterfly response, and the largest non-volatile capacitance window of 24 pF among the three devices. In sharp contrast, the HZO-Al stack exhibits both reduced absolute capacitance and a strongly distorted *C-V* profile, with the butterfly shape suppressed and the memory window nearly vanishing. This indicates that the central Al-rich layer does not act as a benign dopant reservoir; instead, it behaves as a low-polarisation, lower-permittivity layer in series with the ferroelectric film, reducing the net tunability.

Unlike the Pt-electrode case discussed previously, where the polarisation remained relatively high while the capacitance collapsed due to a dead interfacial layer, here the trends in polarisation and capacitance evolve in tandem across all stacks. The HZO-MS device exhibits both enhanced P_r and an enlarged *C-V* swing, whereas the HZO-Al device shows simultaneously suppressed polarisation and capacitance. This behaviour is consistent with the Landau framework, in which changes in the switchable polarisation are directly mirrored by corresponding variations in the field-dependent permittivity. From a device perspective, this coupling is favourable: the stack that offers the strongest ferroelectric switching also delivers the largest capacitance memory window, making it the most promising candidate for memcapacitive operation.

Since dielectric stack engineering directly modifies defect distribution and internal field profiles, these differences in switching behaviour are expected to strongly influence long-term cycling stability. Endurance measurements up to 10^{10} cycles, summarised in Fig. 5.9 (d), therefore provide a critical comparison between the baseline HZO and the HZO–MS configurations. The HZO-MS device retains a slightly higher remanent polarisation than the baseline HZO up to 10^6 cycles and exhibits a slower onset of fatigue, in agreement with reports that superlattice-type stacks can redistribute oxygen vacancies and reduce local field concentration at individual interfaces [166, 130]. The standard HZO device shows moderate fatigue but remains functional over the same cycling range.

Overall, the comparative study in Fig. 5.9 demonstrates that multi-stack dielectric engineering (HZO-MS) is a more effective route to performance enhancement than the insertion of an Al-rich mid-layer. The HZO-MS architecture simultaneously improves remanent polarisation, enlarges the capacitance memory window, and enhances cycling stability, whereas the HZO-Al stack undermines both ferroelectric and memcapacitive responses. For this reason, the HZO-MS configuration is selected as the optimised platform for the subsequent chapter, where its multilevel capacitive states and circuit-level operation are explored in detail.

5.5 Conclusion

This chapter established the core electrical behaviour of HZO-based ferroelectric capacitors using a unified electrical characterisation framework. The investigation first examined the fundamental processes governing ferroelectric operation using TiN/HZO/TiN capacitors as a baseline platform. Clear ferroelectric switching and non-volatile capacitance modulation were demonstrated in the baseline device. A finite zero-bias capacitance memory window of approximately 16 pF was observed, together with a pronounced dependence on sweep direction arising from vacancy-mediated internal bias. While these results confirm the feasibility of ferroelectric memcapacitance in HZO, the baseline stack exhibited limited endurance, with degradation initiating at relatively low cycle counts. This behaviour highlighted the need to

systematically examine the role of electrode interfaces and dielectric stack design in order to improve both the magnitude and long-term stability of the memcapacitive response.

Systematic electrode and dielectric engineering revealed that interface chemistry is a central determinant of memcapacitor performance. The introduction of a platinum top electrode effectively reduced built-in fields and suppressed internal asymmetry; however, this came at the cost of capacitance tunability due to the formation of a dead-layer-like interfacial response. In contrast, dielectric stack modification via the HZO-MS architecture enhanced the effective ferroelectric volume while maintaining TiN electrodes at both interfaces. This approach led to increased remanent polarisation, an enlarged zero-bias capacitance memory window of approximately 24 pF, and substantially improved endurance. The HZO-MS devices retained stable ferroelectric and memcapacitive behaviour up to 10^6 switching cycles, representing a clear and quantitative improvement over the baseline configuration that start degrading after 10^3 cycles. By comparison, insertion of an Al-rich interlayer disrupted ferroelectric continuity, suppressing both polarisation switching and capacitance tunability.

Overall, the results of this chapter demonstrate that achieving stable and practically useful ferroelectric memcapacitance in HZO requires maximising the switchable ferroelectric volume while carefully controlling defect transport and interfacial asymmetry. Among the structures investigated, the TiN/HZO–MS/TiN stack provides the most favourable balance of polarisation strength, capacitance tunability, and endurance. This optimised platform establishes a robust and well-understood foundation for the following chapter, which builds upon this device architecture to explore controlled multilevel capacitance states and their circuit-level implications.

Chapter 6

Multibit Ferroelectric Memcapacitor

This chapter presents the central theme of the thesis, wherein the optimised HZO-MS capacitor is shown to operate as a multistate, non-volatile memcapacitive device. While the previous chapter established binary capacitive memory and identified the interfacial and stack-level conditions required for stable operation, the present chapter leverages this framework to experimentally access and control intermediate states, enabling multibit capacitive behaviour within a single ferroelectric capacitor. Accordingly, the evolution of polarisation with applied voltage is analysed alongside the corresponding capacitance response, establishing a direct and reproducible link between ferroelectric domain energetics and discrete, non-volatile capacitance levels. The chapter further examines practical operating constraints, including device area scaling, frequency-dependent behaviour, and dissipative effects such as dielectric loss and DC leakage. Finally, the functional relevance of multibit memcapacitance is demonstrated through circuit-level integration, where the device is employed in representative analogue functions, including a tunable high-pass filter and a relaxation-based RC oscillator, to realise programmable frequency control.

6.1 Voltage dependent Switching

The multistate behaviour of a ferroelectric memcapacitor arises from the intrinsic structure of its Landau free-energy landscape, in which electrical bias can be used to continuously reshape the stability of polarisation states as discussed in chapter 2. By varying the amplitude of the applied voltage, the energy profile is progressively tilted, allowing the system to stabilise in intermediate, quasi-stable configurations rather than switching directly between the two fully polarised states. As a result, partial domain switching enables access to multiple internal states that are encoded in both the polarisation and the capacitive response of the device.

This section applies this theoretical framework to the optimised HZO-MS capacitor, using voltage programming as a control parameter to tune internal states in a deterministic manner. The section first examines the voltage-dependent evolution of ferroelectric polarisation, before analysing how these intermediate configurations manifest in the capacitance response. This combined analysis provides a unified physical picture linking polarisation, capacitance, and multibit memcapacitive behaviour within a single device.

6.1.1 Voltage-Dependent P-V

To understand how voltage amplitude gives access to intermediate polarisation states, a series of pulses with increasing peak amplitude were applied to the HZO-MS capacitor. The resulting displacement current transients and P–V characteristics provide direct insight into the dynamics of domain activation and redistribution under electrical bias, as shown in Fig. 6.1(a) and (b). Within the Landau framework introduced in Chapter 2, increasing voltage amplitude progressively tilts the ferroelectric free-energy landscape, enabling the stabilisation of intermediate configurations through partial domain switching rather than abrupt reversal between fully polarised states.

At low voltage amplitudes (≤ 1.5 V), switching current peaks appear only near the maximum of the applied waveform, indicating that the electric field remains close to the activation threshold for most of the cycle and that only a limited fraction of domains undergo reversal near the field apex. As the voltage amplitude increases, the instantaneous field exceeds the activation threshold earlier in the rising edge of the waveform, causing the switching peaks to shift progressively towards earlier times. This behaviour reflects increasingly rapid engagement of domains at higher applied fields and a corresponding increase in the switching current. These switching kinetics directly shape the evolution of the P-V loops in Fig. 6.1(b). With increasing amplitude, a nested sequence of loops emerges, accompanied by a smooth increase in remanent polarisation towards saturation. This gradual evolution confirms that polarisation reversal in the HZO film proceeds through progressive domain activation rather than binary switching, consistent with a Landau energy landscape that supports a continuum of metastable intermediate states. In HZO, the relatively large critical nucleation volume and high domain-wall energy tend to stabilise intermediate configurations, allowing voltage amplitude to incrementally redistribute the domain population rather than inducing abrupt collective switching [168, 169].

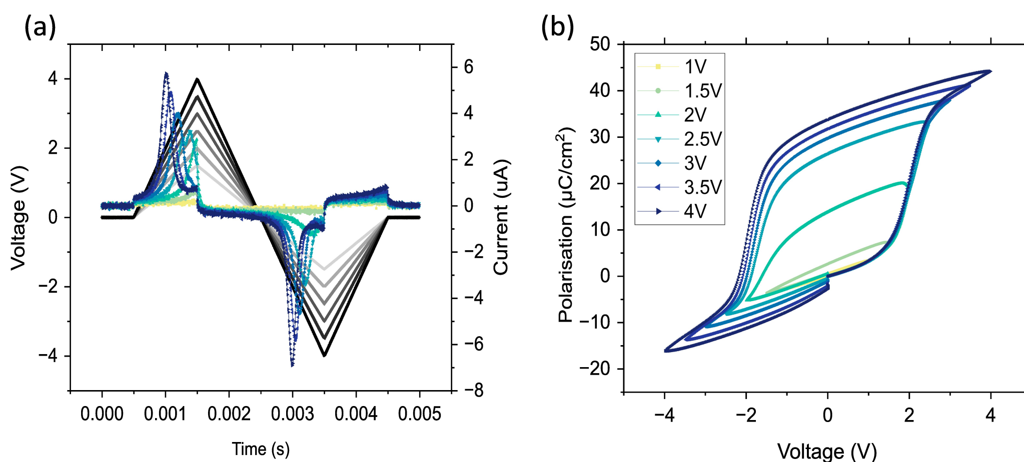

Figure 6.1: **Voltage-amplitude-dependent polarisation evolution in the HZO-MS capacitor.** (a) Applied triangular voltage waveforms with increasing peak amplitude and the corresponding displacement current transients, showing the evolution of switching dynamics with bias amplitude. (b) Measured polarisation-voltage characteristics for increasing voltage amplitudes, exhibiting nested minor loops and progressive development of remanent polarisation associated with partial domain switching. Reproduced from authors own work [159]

Domain-switching Kinetics Beyond confirming the accessibility of intermediate polarisation states, Fig. 6.1 raises a central question addressed extensively in ferroelectric literature: what physical mechanisms govern the kinetics of gradual domain redistribution under electrical bias. The switching dynamics of ferroelectric materials are commonly interpreted using three established frameworks, namely the Kolmogorov–Avrami–Ishibashi (KAI) model, nucleation-limited switching (NLS), and Merz-type field-activated switching, each of which emphasises a different rate-controlling process [126, 127, 170, 171]. The KAI model describes switching as a process initiated by random nucleation events followed by unrestricted lateral domain growth. However, ultrathin HZO films do not satisfy the assumptions underlying this framework. Their polycrystalline microstructure, heterogeneous defect landscape, and strong pinning at grain boundaries severely restrict lateral domain expansion, resulting in switching that proceeds through many spatially confined events rather than the growth of a few large domains. The smooth, non-abrupt evolution of polarisation observed in Fig. 6.1(b) is therefore incompatible with KAI-type behaviour, indicating that this model does not provide an appropriate description of switching kinetics in the present devices.

In contrast, NLS captures the role of nucleation statistics in determining the switching delay. Within this framework, the formation of a critical nucleus represents a key activation barrier, leading to a stochastic and strongly field-dependent onset of switching. This behaviour is commonly described by the Du-Chen expression for the nucleation waiting time,

$$t_{\text{nucleation}} = t_0 \exp\left(\frac{\alpha}{k_{\text{B}} T} \cdot \frac{1}{V_{\text{sw}}^2} \right), \tag{6.1}$$

which highlights the strong exponential dependence of nucleation delay on the inverse square of the applied voltage. Hence, NLS describes the rate-limiting role of nucleation in initiating polarisation reversal. Once nucleation has occurred, the subsequent evolution of switched regions is influenced by domain-wall propagation through a heterogeneous energy landscape. This field-assisted motion is commonly described by the Merz relation,

$$t_{\text{wall}} = t_0 \exp\left(\frac{E_{\text{a}}}{E} \right), \tag{6.2}$$

which reflects the lowering of activation barriers for domain-wall depinning and motion under applied electric field. This mechanism dominates when domain walls encounter strong pinning from grain boundaries, oxygen vacancies, and local structural inhomogeneities, such that increasing field facilitates depinning and accelerates polarisation reversal following nucleation.

As widely reported in the literature, polarisation switching in hafnium-based ferroelectrics is not governed by a single microscopic process, but instead reflects the combined influence of nucleation and domain-wall propagation. Although domain-wall motion necessarily follows nucleation, these processes can contribute differently to the overall switching time depending on the applied electric field and material landscape. The experimentally measured switching time can therefore be expressed as the sum of two contributions,

$$t_{\text{sw}} = t_{\text{nucleation}} + t_{\text{wall}}, \tag{6.3}$$

where $t_{\text{nucleation}}$ represents the delay associated with the formation of a critical nucleus and t_{wall} captures the subsequent propagation of domain walls through the ferroelectric film.

To assess the relative contributions of these two processes in the present devices, the experimentally extracted switching time t_{sw}, obtained from the position of the switching current

peak within triangular voltage waveforms, was analysed using linearised representations associated with NLS and Merz-type field-activated scaling. Comparison of these fits allows identification of the rate-limiting contribution over the experimentally accessible voltage range, without implying the absence of the complementary mechanism.

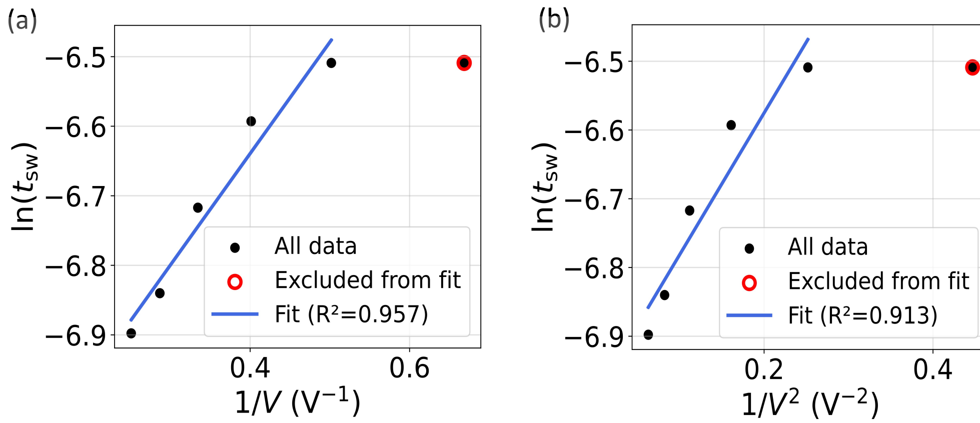

Figure 6.2: **Switching time analysis using Merz and nucleation-limited models.** (a) $\ln(t_{sw})$ plotted as a function of $1/V$, corresponding to Merz-type field-activated switching. (b) $\ln(t_{sw})$ plotted as a function of $1/V^2$, corresponding to nucleation-limited switching. The switching time t_{sw} is extracted from the position of the displacement current peak under triangular voltage excitation. The lowest-voltage data point is excluded from the fits. Reproduced from authors own work [159]

Figure 6.2 compares $\ln(t_{sw})$ plotted against $1/V$ and $1/V^2$. Since the horizontal axis is expressed in inverse voltage, the rightmost data point corresponds to the lowest applied voltage amplitude. This near-threshold point was excluded from the fits because switching in this regime is highly stochastic and the current transient is weak and broadened, rendering the extracted peak position sensitive to noise, bandwidth, and incomplete switching. It is also noted that additional mechanisms may influence switching behaviour in this low-field regime, which are not explicitly captured by the present models and are beyond the scope of this study. Excluding this near-threshold point, both representations exhibit approximately linear trends, indicating that field-dependent activation plays an important role in the switching dynamics over the experimentally accessible range. Although the correlation with Merz-type scaling is marginally stronger than with NLS scaling, the proximity of the fits suggests that the switching kinetics cannot be uniquely attributed to a single idealised mechanism. Instead, the results are consistent with a composite switching response in which nucleation and domain-wall propagation contribute concurrently, with their relative influence varying smoothly with applied voltage. Further experimental investigation across extended voltage and time scales would be required to fully understand these contributions, which lies beyond the scope of this thesis.

Overall, these results demonstrate that polarisation reversal in HZO is neither abrupt nor governed by a single activation pathway. Instead, switching evolves through a continuous, field-tunable redistribution of domain fractions, with nucleation, depinning and interface-mediated processes contributing across different voltage regimes. This gradual and cumulative switching response underpins the reproducible intermediate polarisation states observed here and forms the physical foundation for the multilevel capacitance behaviour examined in the following sections.

6.1.2 Voltage-Dependent C-V

Having established how ferroelectric polarisation evolves progressively with increasing voltage amplitude, the same framework is now applied to the capacitance response of the HZO-MS capacitor. Importantly, the evolution of capacitance with applied voltage amplitude is examined in the context of the device's prior state, enabling assessment of how history-dependent domain configurations influence the C-V response.

As discussed in Chapter 5, a positive bias drives the capacitor into a low-capacitance state (LCS), whereas a negative bias stabilises a high-capacitance state (HCS). To understand how capacitance evolves under increasing voltage excitation, C-V measurements were therefore performed starting explicitly from both LCS and HCS. In all cases, the voltage sweeps were initiated from negative polarity and applied in a clockwise direction, such that each measurement cycle spans both positive and negative bias. As a result, the applied waveform first drives the device towards LCS under positive bias and subsequently pull towards HCS with negative bias, as illustrated in Fig. 6.3.

When the device begins from the LCS, the domain configuration already corresponds to a minimum-capacitance state. The positive half-cycle reinforces the existing domain alignment, while the negative half-cycle remains insufficient to overcome the coercive field required for reorientation. As the voltage amplitude is increased, the negative-going bias eventually approaches the coercive regime, allowing the system to escape the low-capacitance well and initiate partial domain reversal. Upon reversal, the subsequent positive-going bias drives the device back towards the low-capacitance branch. This sequence results in a progressive increase followed by a decrease in capacitance within each cycle, giving rise to the gradual emergence of the characteristic butterfly-shaped C-V response. Thus, when starting from the LCS, the negative polarity primarily governs the transition towards the high-capacitance branch, and significant modulation occurs only once a sufficient negative amplitude is reached.

A complementary behaviour is observed when the device begins from the HCS. In contrast to the LCS case, even modest positive voltage amplitudes act against the established polarisation and begin to drive the device towards the low-capacitance branch, while the negative polarity reinforces the initial high-capacitance configuration. As a result, capacitance modulation appears at substantially lower positive voltages than in the LCS case. This asymmetry, whereby positive bias induces an earlier response while negative bias requires larger amplitudes, directly reflects the polarity-dependent coercive fields and internal imprint effects discussed in Chapter 5.

Despite the pronounced differences in early-stage evolution, both initial conditions converge as the voltage amplitude increases. At sufficiently large amplitudes, each cycle sequentially drives the device through both low and high-capacitance configurations, causing the C-V trajectories to follow similar butterfly loops. These amplitude-dependent and history-dependent C-V trajectories establish how biasing conditions govern access to different capacitance branches. However, while this analysis clarifies how capacitance evolves under continuous sweeping, it does not yet reveal how discrete, stable capacitive states look like. Hence, the accessibility of these capacitive states are examined in the following section.

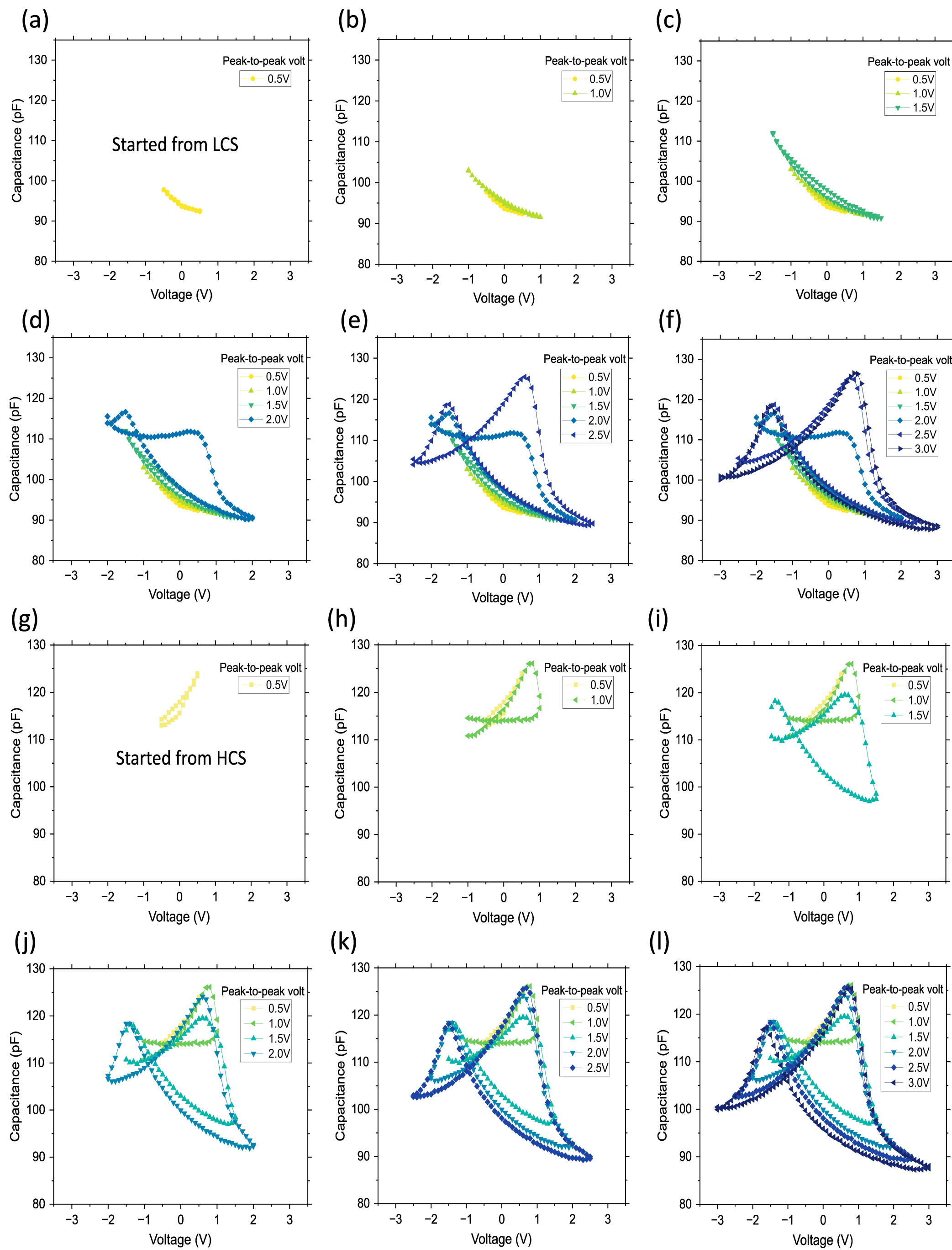

Figure 6.3: **Voltage-dependent C-V evolution under bipolar sweeping for different initial states.** (a-f) C-V characteristics measured with increasing voltage amplitude starting from the low-capacitance state. (g-l) Corresponding C-V characteristics starting from the high-capacitance state. In all cases, the voltage sweep is applied in a clockwise direction, spanning both positivand negative bias within each cycle, revealing trajectory and history-dependent capacitance evolution.

6.1.3 Multilstate Capacitance write-read operation

Having established how capacitance evolves under continuous voltage sweeping, the next step is to determine whether these changes can be harnessed for controlled, non-volatile multilevel operation. A write-read programming scheme was implemented in which voltage polarity is used selectively to push or pull the device away from its initial capacitance state. When the device is initialised from LCS, only negative programming voltages are applied in order to progressively increase the capacitance. Conversely, when the device is in HCS, only positive programming voltages are used to gradually reduce the capacitance. In this manner, each polarity is employed exclusively to drive the device along a single monotonic branch. The capacitance read was done after each programming step. Increasing programming amplitudes were applied sequentially to incrementally redistribute the ferroelectric domain population, while the read operation probed the resulting steady-state capacitance without perturbing the stored configuration.

Figure 6.4(a) shows the capacitance evolution when the device is initialised in the HCS and subjected to a sequence of positive programming voltages. Each trace corresponds to the capacitance measured during the read phase following a single programming sweep. A clear ladder of quasi-stable levels emerges, where low programming amplitudes induce only minor changes, while larger amplitudes progressively depress the capacitance towards the LCS. Beyond approximately 2–2.4 V, the incremental change diminishes, reflecting the finite population of remaining switchable domains as the system approaches saturation.

An analogous behaviour is observed when the device is initialised in the LCS and driven by increasingly negative programming sweeps, as shown in Fig. 6.4(b). In this case, the capacitance initially exhibits a weak response, consistent with the C-V evolution discussed in the previous section, followed by a steep transition region as marginally stable domains are activated in larger numbers, and finally saturates as the HCS is reached. Importantly, the full tuning window spans approximately 24 pF, with 8-9 intermediate non-volatile capacitance states that can be reliably accessed through amplitude programming.

Hence, the resulting capacitive states exhibit three distinct regimes: (i) a weak-response regime at low programming voltage, where only the most weakly pinned domains contribute to switching; (ii) a steep transition regime between approximately 0.8–2.0 V for positive programming or −1.6–−3.0 V for negative programming, where a large fraction of marginal domains becomes energetically accessible; and (iii) a saturation regime, in which further increases in amplitude produce only minor changes in capacitance due to the depletion of remaining switchable domains.

To visualise the correspondence between the applied programming voltage and the resulting capacitive state, the steady-state capacitance values extracted from Fig. 6.4(a) and (b) are combined in Fig. 6.4(c), enabling direct comparison of write amplitude and readout response. The combined curves form a characteristic potentiation-depression response. The positive voltage progressively depress the capacitance, while negative voltage potentiate it. This bidirectional, amplitude-dependent evolution is directly analogous to synaptic plasticity in biological neural networks, where synaptic weights evolve gradually in response to the magnitude and history of incoming stimuli. Unlike resistive switching elements commonly used as synapses in neuromorphic architectures, memcapacitors encode the synaptic state in a capacitive variable, enabling passive storage with intrinsically low leakage making them much more energy efficient than memristors [133, 14, 121, 132]. In the present ferroelectric

implementation, the HZO dielectric enables multilevel capacitive programming in a thin-film, low-voltage, and CMOS-compatible platform. Together, these attributes position the HZO–MS capacitor as a compact and energy-efficient analogue synaptic element suitable for future neuromorphic circuits.

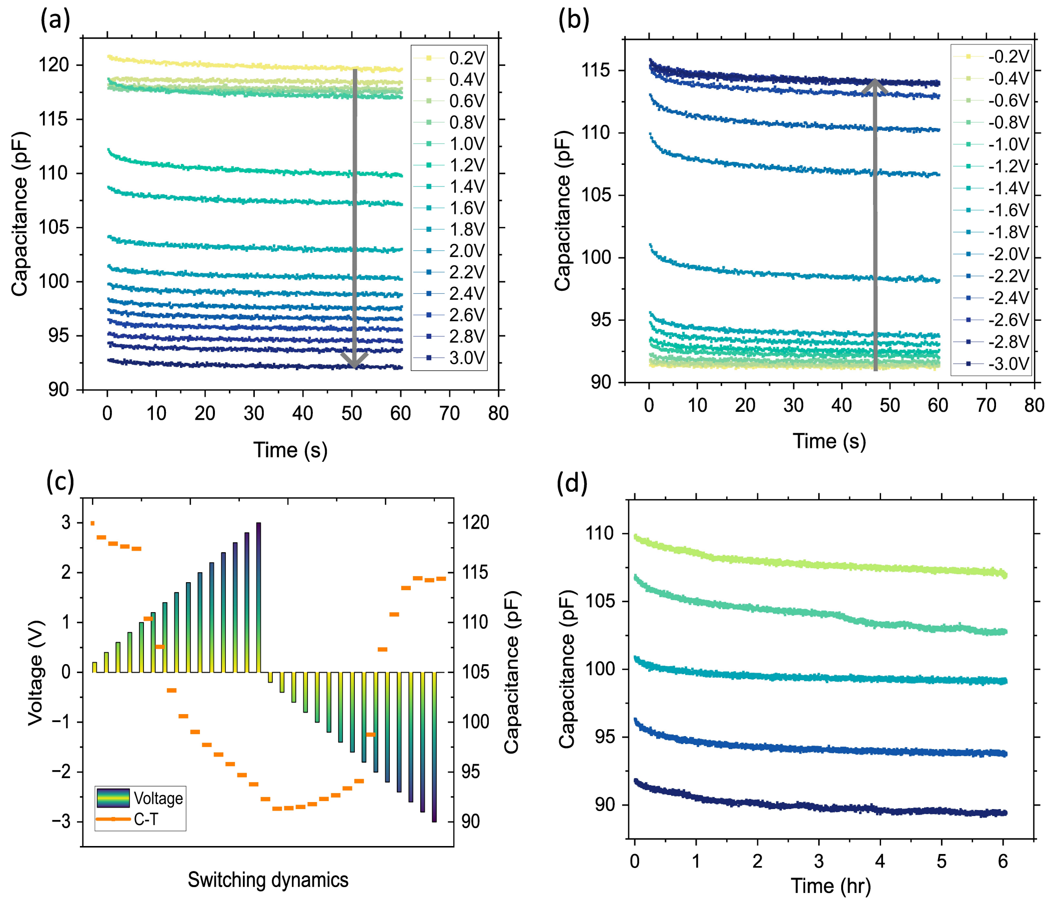

Figure 6.4: **Multistate write-read operation and retention characteristics.** (a) Capacitance readout following positive programming sweeps of increasing amplitude, starting from the HCS. (b) Capacitance readout following negative programming sweeps of increasing amplitude, starting from LCS. (c) Correlation between the applied programming voltage sequence and the resulting steady-state capacitance, illustrating bidirectional potentiation and depression. (d) Long-term retention of selected intermediate capacitance states under small-signal, zero-bias read conditions, confirming non-volatile multilevel behaviour. Reproduced from authors own work [159]

Having established controllable multistate write-read operation, the temporal stability of the programmed capacitance levels is examined. In the preceding experiments, capacitance was read over a time window of approximately 60 s, during which all intermediate states were found to be stable and well separated. To assess longer-term stability, selected programmed capacitance levels were monitored over extended durations of six hours, as shown in Fig. 6.4(d). While the present measurements directly confirm state stability over six hours, long-term retention is commonly assessed using accelerated thermal testing. In such methods, the programmed states are monitored at elevated temperatures (typically ∼80–100 °C over 8–10 hours) and the resulting relaxation behaviour is extrapolated to room temperature using a thermally activated retention model. In the present measurements, all intermediate

levels remain clearly distinguishable over time, exhibiting only minor relaxation without convergence or state collapse. This confirms that the accessed domain configurations correspond to genuinely non-volatile states under small-signal, zero-bias read conditions.

Programming Asymmetry and Window Drift A subtle but important asymmetry emerges when comparing the two programming directions. While positive programming reliably drives the device towards the LCS, negative programming does not fully recover the maximum high-capacitance state observed when the device is initially prepared in the HCS, as shown in Fig. 6.4(a-b). This indicates that the multistate write process is not strictly reversible in terms of absolute capacitance extrema, even though monotonic tuning along each programming branch remains well controlled.

Furthermore, when the device is repeatedly programmed back and forth between LCS and HCS, a gradual downward shift of the entire capacitance window is observed. Importantly, the width of the tuning window and the number of accessible intermediate states remain largely preserved, but the absolute capacitance levels drift to lower values over successive cycles. Also, the HCS falls at larger rate than LCS, that also weakens the memeory window. This behaviour suggests a cumulative modification of the internal electrical boundary conditions, likely associated with interfacial charge trapping or imprint effects induced by repeated voltage stress. This highlights a key limitation and underscores the need for improved write schemes that minimise cumulative interfacial perturbation. Addressing this effect represents an important direction for future work, particularly for applications requiring long-term bidirectional weight updates.

Domain-Switching Statistics The multilevel capacitance behaviour of the HZO–MS capacitor can be understood without invoking any specific switching kinetics by considering how the ferroelectric domain population is progressively redistributed under electrical programming. From this perspective, the applied programming amplitude does not determine how fast domains switch, but rather how many domains become energetically accessible for reorientation. The resulting capacitive state is therefore governed by the distribution of domains between the two stable orientations, rather than by the temporal details of the switching process.

Let f_n denote the fraction of domains aligned in the high-capacitance orientation after the n-th programming pulse. Following a subsequent programming sweep of amplitude V_{prog}, the domain fraction in the $(n+1)$th state consists of two contributions: domains that were already aligned in the high-capacitance orientation (f_n), and a subset of the remaining unswitched domains $(1 - f_n)$ that become energetically favourable to reorient under the applied field. The influence of the programming amplitude is captured by a monotonic, polarity-dependent accessibility function $p(V_{\text{prog}})$, which represents the fraction of marginally stable domains that can be activated at a given voltage. The evolution of the domain fraction can therefore be written phenomenologically as

$$f_{n+1} = f_n + (1 - f_n)\, p(V_{\text{prog}}). \tag{6.4}$$

Within this formulation, polarity dependence arises naturally from the interfacial asymmetry of the HZO–MS stack. A positive programming sweep experiences a different effective electric field within the ferroelectric than an equally strong negative sweep, leading to distinct accessibility functions $p_+(V)$ and $p_-(V)$. This asymmetry directly gives rise to the experimen-

tally observed potentiation and depression branches without requiring different microscopic switching mechanisms.

Importantly, this domain-fraction description also explains the non-uniform spacing of the programmed capacitance states. The incremental change in domain fraction can be written as;

$$\Delta f_n = f_{n+1} - f_n = (1 - f_n)\, p(V_{\text{prog}}), \tag{6.5}$$

that depends explicitly on both the history-dependent availability of unswitched domains $(1-f_n)$ and the voltage-dependent accessibility $p(V_{\text{prog}})$. As a result, successive programming steps do not produce equal changes in capacitance.

At low programming amplitudes, $p(V_{\text{prog}})$ is small, so only a limited fraction of marginal domains is accessible, leading to closely spaced capacitance states. At intermediate amplitudes, a much larger population of domains becomes energetically accessible while a substantial fraction of domains remains unswitched, resulting in larger state-to-state transitions. As saturation is approached, the pool of remaining unswitched domains diminishes, reducing Δf_n even as the applied voltage increases. Consequently, the capacitance states are intrinsically non-uniformly spaced, reflecting the progressive redistribution of domain fractions rather than any kinetic limitation.

Repeated programming behaviour While amplitude programming establishes access to multiple discrete capacitance states, it remains to be understood whether a given programming amplitude uniquely defines a single internal configuration or instead permits a range of nearby metastable states that can be accessed through repeated excitation.

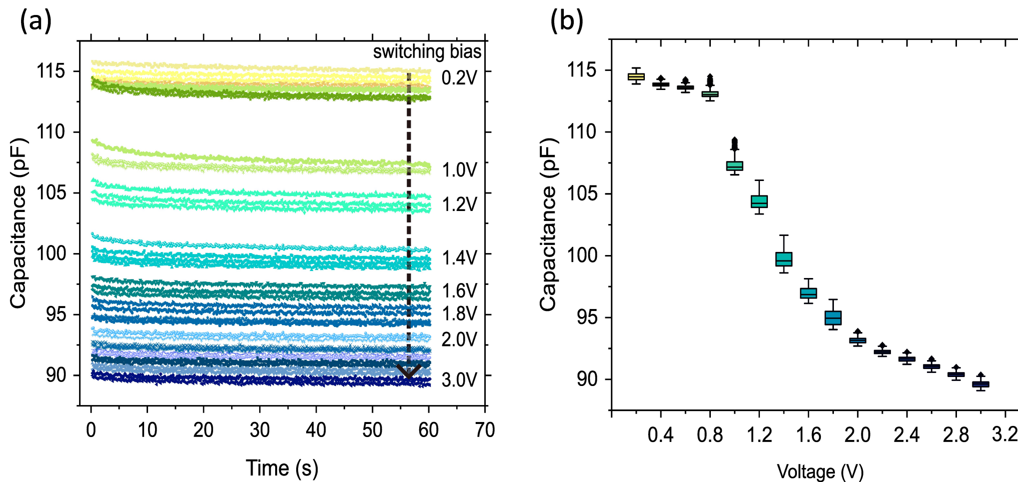

Figure 6.5: **Repeated programming behaviour at fixed voltage amplitude.** (a) Capacitance readout as a function of time following repeated positive programming sweeps of identical amplitude, starting from the high-capacitance state, showing convergence within a finite window of accessible states. (b) Steady-state capacitance values extracted from (a) as a function of programming voltage, illustrating the voltage-dependent width and position of the accessible capacitance window. Reproduced from authors own work [159]

To probe the structure of the intermediate capacitance levels beyond single-shot programming, a complementary experiment was performed in which the device was initialised in the

HCS and subjected to repeated positive programming sweeps of identical voltage amplitude until no further systematic change was observed. After each sweep, the capacitance was read using the same non-perturbative AC probe.

This repeated-programming experiment reveals that a fixed programming amplitude does not map to a single discrete capacitance value, but rather to a finite window of accessible states as shown in Fig. 6.5. At low programming amplitudes, this window is narrow because only a small subset of weakly pinned domains can be activated. As the amplitude increases, the window broadens and reaches a maximum in the intermediate voltage range, where the distribution of local switching barriers is widest. At still higher amplitudes, the window narrows again as the pool of remaining switchable domains diminishes and the system approaches saturation.

Taken together, these observations demonstrate that voltage amplitude and repetition play complementary roles in controlling the domain redistribution. The programming amplitude defines the range of energetically accessible configurations, while repeated application allows the device to incrementally explore and stabilise states within that range. This behaviour is consistent with the domain-fraction framework introduced earlier and also highlights the analogue nature of the ferroelectric memcapacitive rather than just 8-9 fixed states..

Comparison with existing MFM stacks The optimised HZO-MS device investigated in this work exhibits a capacitive memory window of approximately 24 pF, as established in the preceding analysis. To place the present results in context, Table 6.1 compares representative HfZrO-based MFM capacitors, highlighting variations in device geometry, electrode configuration, read frequency, endurance, and retention performance. Notably, the switching behaviour in the present device is asymmetric which contrasts with several previously reported MFM and MFIM ferroelectric memcapacitors, where the accessible capacitance states are largely symmetric and more uniformly spaced [132, 121, 14, 73].

Table 6.1: MFM memcapacitor comparison reported in literature and current work.

Ferroelectric film	**Electrode (BE / TE)**	**Area (μm^2)**	T_{ann} **(°C)**	**CMW**	**Read frequency**	**Cap states**	**E (cycles)**	**R (s)**
HZO [164]	TiN/ TiN	50 × 50	450	$\sim 2\varepsilon_0$	10kHz	2	$> 10^4$	10^8 s
La:HZO [129]	Mo+MoO$_x$ / TiN	–	400	4.71 ε_0	10kHz	2	–	10^8 s
HZO [135]	TiN / TiN	100 × 100	450	$\sim 5\ \varepsilon_0$	10kHz	2	10^3	$> 10^8$ s
Nb_2O_5 / La:HZO [172]	TiN+MoO$_x$ / TiN	60 × 80	400	8.7 ε_0	10kHz	2	10^7	10^{11} s
HZO-MS [130]	W / W	–	500	$\sim 11pF$	-	2	–	–
HZO [121]	TiN/Pt	100 × 100	500	$\sim 15pF$	10kHz	8	10^7	$> 10^3$ s
HZO-MS [132]	Pt/W	π (100 × 100)	550	40pF	10kHz	8	10^{10}	$> 10^4$ s
HZO [14]	TiN / MoO$_x$	100 × 100	400	78pF	1kHz	> 8	10^9	$> 10^8$ s
This work HZO-MS	TiN / TiN	60 × 60	500	$\sim 24pF$	10kHz	> 8	10^6	$> 10^5$ s

All devices are programmed using comparable electric fields, typically in the range of 2.5–3 MV/cm, therefore, switching voltage is not explicitly included. Reported capacitance windows correspond to measurements at zero DC read bias. E: endurance; R: retention time.

A direct comparison of capacitive memory window can be misleading, as the reported memory

window is strongly influenced by both device area and measurement conditions. In particular, larger capacitor footprints and lower read frequencies naturally yield higher absolute capacitance values, independent of the intrinsic tunability of the ferroelectric layer. When the capacitance memory window of the present device is considered relative to its active area and read frequency, the achieved modulation is of the same order as the highest values reported for comparable HZO-based MFM structures. As discussed in the following section, this behaviour directly reflects the role of device scaling and readout frequency. The apparent disparity in absolute capacitance window therefore arises primarily from differences in measurement conditions rather than a fundamental limitation of the HZO-MS architecture.

It is further noted that several prior studies employing tungsten or molybdenum based electrodes report enhanced endurance and retention characteristics. While such electrodes can promote favourable switching behaviour, they are also associated with increased fabrication complexity and potential interfacial instability. Previous systematic investigations have shown that TiN electrodes offer a balanced trade-off between ferroelectric phase stabilisation, defect management, and CMOS process compatibility [173]. In this context, the demonstration of a competitive multilevel capacitive memory window using a simple TiN/HZO/TiN stack represents a meaningful result. At the same time, the comparatively limited endurance observed in the present device highlights endurance optimisation as a key challenge and an important direction for future work.

6.2 Factors affecting Capacitance

The functional relevance of a multistate ferroelectric memcapacitor is determined not only by its ability to access and retain discrete capacitance levels, but also by how these states scale, persist, and remain reproducible under realistic device and measurement constraints. Beyond demonstrating multilevel programmability, it is therefore essential to examine the design and implementation level factors that govern practical usability.

Several aspects are particularly important in this regard. First, dissipative mechanisms such as dielectric loss and DC leakage must be sufficiently low to preserve signal amplitude, phase integrity, and stability when the device is embedded in analogue and frequency dependent circuits. Second, understand the memory window scaling with device area, directly influencing circuit footprint, signal levels, and integration density. Third, the capacitance of ferroelectric thin films is inherently frequency dependent, and understanding how multistate behaviour evolves across frequency is critical for analogue, and RF operation. Finally, programming repeatability assesses the ability to reliably reaccess the same capacitance state across successive write–read cycles, a key requirement for stable analogue computation and long-term circuit functionality.

6.2.1 Loss Analysis

To evaluate the impact of dissipative processes on circuit-level operation, the loss behaviour of the ferroelectric memcapacitor was examined under small-signal read conditions. Figure 6.6(a) presents the measured phase response as a function of frequency, obtained using a low-amplitude AC excitation superimposed on a DC read bias of 0.5 V. At lower frequen-

cies, up to approximately 100 kHz, the phase angle remains close to $-90°$, indicating that the device response is dominated by reversible polarisation and displacement current, with negligible resistive contribution.

As the excitation frequency increases, a gradual reduction in the phase magnitude is observed, reflecting the increasing influence of dissipative mechanisms within the dielectric. The dielectric loss tangent was extracted from the phase response using $\tan\delta = \tan(90° - |\phi|)$. Based on this analysis, $\tan\delta$ increases from approximately 0.04 at 10 kHz to around 0.07 at 100 kHz. At higher frequencies approaching the MHz regime, the phase departs more substantially from the ideal capacitive limit (for example, $\phi \approx -69.25°$ at 1 MHz), indicating that dielectric losses increasingly shape the small-signal impedance response.

In addition to frequency-dependent dissipation, the steady-state conduction behaviour of the device was assessed through time-resolved DC leakage current measurements using a constant bias of 3 V, as shown in Fig. 6.6(b). A transient increase in current is observed, which rapidly decays as the system approaches equilibrium. After this initial relaxation, the current stabilises at values below 2 pA for the remainder of the measurement. The low steady-state leakage corresponds to an effective DC resistance in the gigaohm range, confirming that charge transport through the dielectric is strongly suppressed under static bias conditions. Together with the measured loss tangent, these results indicate that while dissipative effects are non-negligible, they remain compatible with reliable operation of the ferroelectric memcapacitor in frequency-dependent circuit applications.

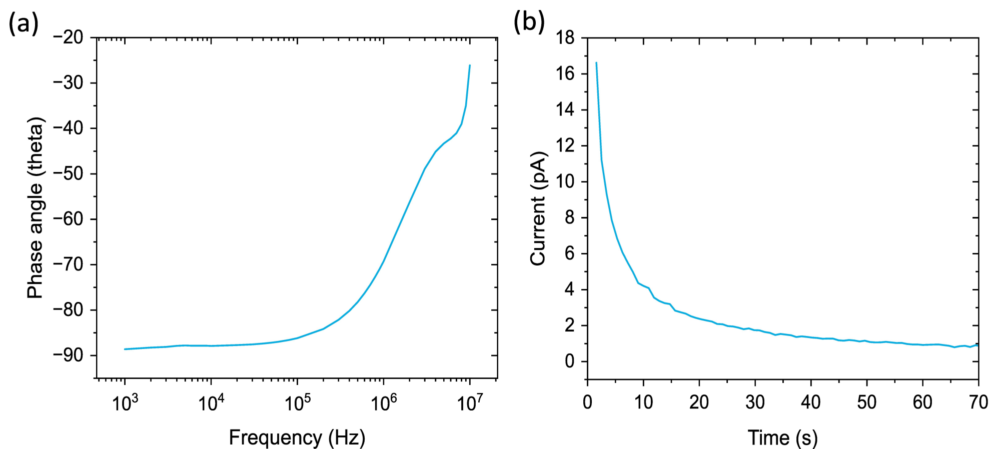

Figure 6.6: **Assessment of dissipative effects in the ferroelectric memcapacitor.** (a) Frequency-dependent phase response obtained using small-signal AC measurements at a DC read bias of 0.5 V. (b) Time-resolved DC leakage current measured under a constant bias of 3 V, illustrating transient relaxation and steady-state conduction behaviour.

6.2.2 Area Dependence

To assess how device geometry influences ferroelectric switching and the resulting multistate capacitance, capacitors with lateral dimensions ranging from 2×2 to 60×60 μm^2 were fabricated and characterised under identical measurement conditions. The corresponding P-V and C-V characteristics, shown in Fig. 6.7, reveal a clear and systematic dependence on device area. For a parallel-plate geometry, the small-signal capacitance is expected to scale

linearly with electrode area. This behaviour is confirmed in the measured C–V loops, where the absolute capacitance increases proportionally with A, accompanied by a corresponding increase in the accessible capacitance memory window.

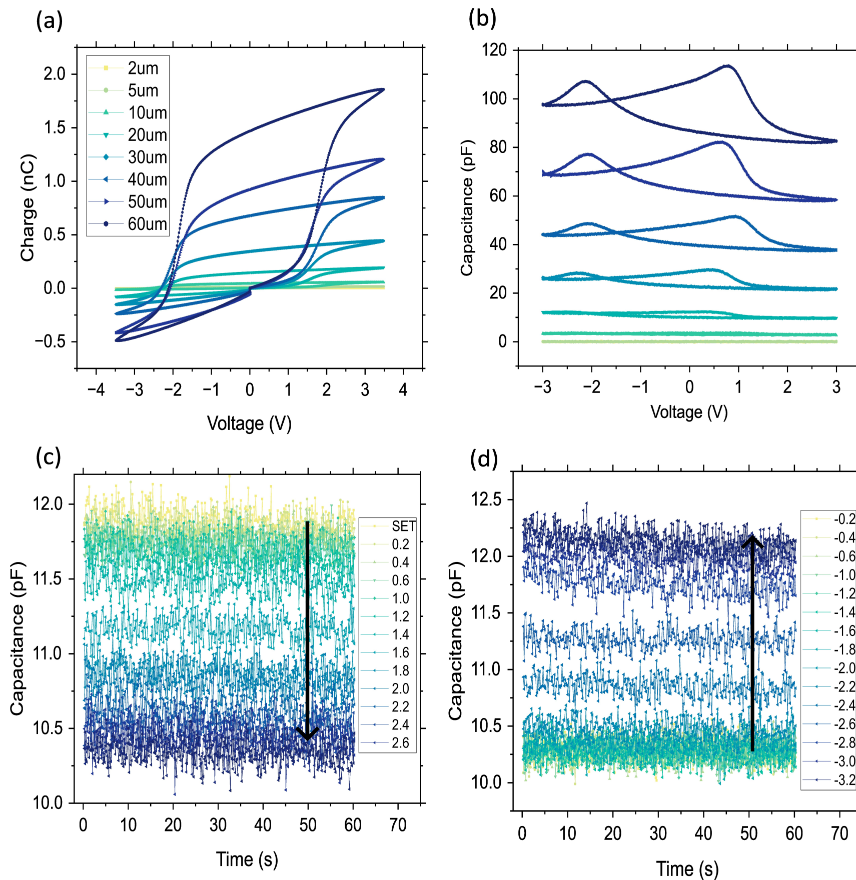

Figure 6.7: **Ferroelectric and capacitive behaviour with area scaling.** (a) P-V characteristics measured for device size ranging from 2×2 to 60×60 μm^2, showing increasingly smooth and well-defined ferroelectric switching. (b) Corresponding C-V characteristics, where larger devices exhibit clearer butterfly-shaped responses. (c,d) Time-resolved capacitance evolution measured for a 20×20 μm^2 device, demonstrating stable and repeatable switching between discrete capacitance states within a memory window of approximately 2 pF. The colour scale indicates the applied programming voltage (in volts) used to access the different capacitance states.

Devices with areas below approximately 10×10 μm^2 exhibit incomplete hysteresis, significant cycle-to-cycle variability, and noisy C–V characteristics. In this regime, the number of ferroelectric grains and active nucleation sites is sufficiently small that individual domain-switching events produce large fluctuations in the measured signal. As a result, the capacitance states are poorly separated and a well-defined memory window is not established. As the device area increases beyond 20×20 μm^2, the switching curves evolve into smooth and well-defined hysteresis loops. Larger capacitors effectively average over many grains and nucleation events, suppressing local variability and enabling reproducible access to intermediate polarisation states. The 60×60 μm^2 devices exhibit widest P-V loops and C-V characteristics with maximum memory window, allowing reliable extraction of multiple capacitance states across the window.

This observed dependence on device area also highlights an important physical constraint on the number of achievable analogue states, namely the discrete nature of ferroelectric domain switching. Although the device exhibits analogue capacitance modulation at the macroscopic level, the number of achievable states is not unbounded. Each intermediate state arises from a finite distribution of switched and unswitched ferroelectric regions, i.e, the apparent analogue response is the collective average of many discrete domain-switching events. The minimum switching increment is therefore constrained by the smallest stable ferroelectric region and by the discreteness of domain-wall motion. First-principles studies of $HfZrO_2$ further suggest that domain growth is intrinsically quantized, proceeding unit-cell-by-unit-cell in one lateral direction and in half-unit-cell quanta in another, depending on crystallographic orientation [174]. Consequently, the practical number of distinct states is limited not only by this microscopic discreteness, but also by device area, domain-wall pinning, cycle-to-cycle variability, retention, and the experimental ability to resolve adjacent states without overlap.

The observed area dependence also has direct implications for system-level design. Larger capacitors provide improved signal-to-noise ratio and robust state separation, making them suitable for circuit blocks requiring stable analogue modulation or coarse tuning. Although the lateral dimensions of the largest devices studied here may initially appear substantial, it is important to recall that on-chip metal–insulator-metal (MIM) capacitors, introduced in Chapter 2, are reported to consume a significant fraction of the total chip area in analogue and mixed-signal systems, in some cases approaching ~40% of the overall layout. Moreover, achieving the required capacitance values typically demands capacitance densities exceeding $\sim$10 fF/μm^2 [5]. In this context, the HZO-MS capacitors demonstrate that a single reconfigurable ferroelectric device can deliver capacitance densities with an average of $\sim$27 fF/μm^2 in 60×60 μm^2 devices, while simultaneously providing non-volatile and programmable capacitance states unavailable in conventional MIM technologies. This combination offers a pathway to reduce overall capacitor footprint by replacing multiple fixed-value elements with a single tunable component.

6.2.3 Frequency Dependence

To assess how the multistate capacitive response of the HZO-MS memcapacitor evolves with signal frequency, the device was first programmed into a fixed capacitance state and subsequently characterised under small-signal AC excitation across frequencies ranging from 10 kHz to 10 MHz. These measurements probe the same internal domain configuration at different excitation rates, allowing the intrinsic frequency response of the programmed states to be isolated from any write-induced effects.

Figure 6.8(a) shows the capacitance measured as a function of time for a fixed programmed state at different excitation frequencies. Across the full frequency range, the capacitance remains stable over the measurement window, confirming that the AC read operation is non-disturbing and does not modify the stored domain configuration. As the frequency increases, the absolute capacitance associated with each state decreases systematically. This reduction reflects the intrinsic frequency dispersion of the dielectric response: at higher excitation rates, only a small fraction of bound and interfacial charge is able to respond within each cycle, resulting in a lower effective capacitance.

Motivated by this observation, the evolution of the programmed capacitance states with frequency was examined more directly. Figure 6.8(b) shows the capacitance measured across frequency for multiple pre-programmed states, similar to previously observed reports [175]. In addition to the overall reduction in absolute capacitance, the separation between adjacent states progressively decreases with increasing frequency, indicating a contraction of the accessible capacitance window.

Further insight is obtained by examining the C-V characteristics at different frequencies. At low to intermediate frequencies (100–600 kHz), shown in Fig. 6.8(c), the *C–V* curves retain a pronounced butterfly shape. This response indicates that reversible domain-wall motion and polarisation dynamics are still able to follow the AC excitation and contribute significantly to the measured capacitance. A qualitative transition occurs as the frequency is increased beyond this range. Between approximately 600 and 700 kHz, the butterfly curvature collapses and the *C–V* response becomes inverted, as shown in Fig. 6.8(d). Similar inverted characteristics have been reported in hafnia-based ferroelectrics and are attributed to the dominance of dielectric contributions once ferroelectric domain-wall motion becomes kinetically limited [122]. In this high-frequency regime, the measured capacitance is governed primarily by lattice permittivity, interfacial field redistribution, and dielectric nonlinearity rather than by reversible polarisation switching. As the frequency increases further toward the megahertz range, the inverted response strengthens. Together, these measurements conclude a clear transition from a ferroelectric-dominated regime at low frequencies to a dielectric-dominated regime at high frequencies. This transition defines the effective operational bandwidth over which reversible domain-wall motion contributes meaningfully to the multistate response of the HZO-MS memcapacitor.

6.2.4 C-V Cycle Dependence

Since the multistate write protocol employed in this chapter relies on voltage sweeps of increasing amplitude to redistribute the ferroelectric domain population, it is instructive to examine how the device responds under sustained C-V cycling. Repeated C-V characterisation represents an extreme case of voltage-sweep–based operation, analogous to endurance testing but with slow, continuous voltage ramps rather than discrete triangular pulses. This approach allows the impact of prolonged sweep-induced electrical stress on the ferroelectric memcapacitor to be isolated and assessed.

Endurance measurements presented in Chapter 5 demonstrate that the optimised HZO-MS stack sustains stable ferroelectric switching up to approximately 10^6 cycles under dynamic triangular voltage pulses. In addition, as shown in Fig. 6.9(a,b), repeated P-V measurements are highly reproducible and show no noticeable drift. In contrast, repeated C-V sweeps exhibit a progressive shift and lead to rapid degradation of the ferroelectric response, with the characteristic butterfly-shaped C-V behaviour collapsing after only $\sim$60 cycles. This accelerated degradation originates from the fundamentally different electrical stress imposed during C-V measurements. Unlike triangular pulses, which apply brief high-field excursions, a C-V sweep exposes the device to a slowly varying voltage that dwells near sub-coercive and near-coercive fields for extended durations. As a result, the HZO layer experiences millisecond-scale electric-field exposure during each sweep. Such conditions promote slow relaxation processes, including oxygen-vacancy migration, interfacial charge trapping, and progressive pinning of ferroelectric domain walls, all of which are known to accelerate degradation in

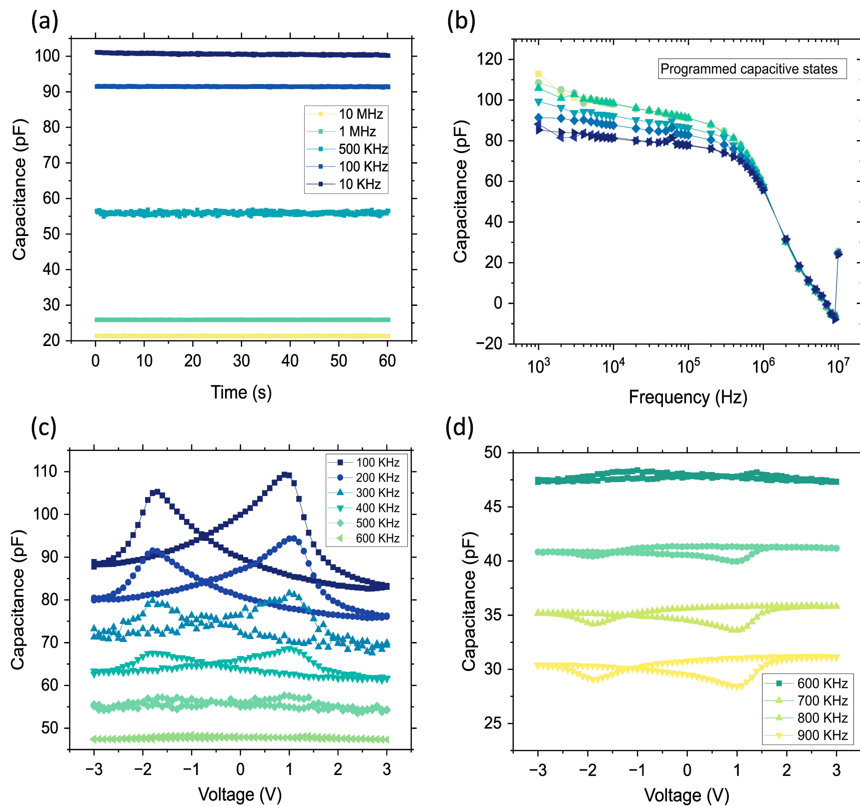

Figure 6.8: **Frequency behavior of HZO-MS memcapacitor.** (a) Capacitance stability measured as a function of time for a fixed programmed state under small-signal AC excitation at different frequencies. (b) Capacitance measured as a function of frequency for several programmed capacitance states, showing a gradual reduction in absolute capacitance and contraction of the tunable window with increasing frequency. (c) C-V characteristics measured at low to intermediate frequencies (100-600 kHz), where the characteristic butterfly shape is preserved. (d) C-V characteristics at higher frequencies (600-900 kHz), where the butterfly curvature collapses and an inverted response emerges.

hafnia-based ferroelectrics.

Following approximately 60 C-V sweeps, the butterfly loop collapses almost entirely and the capacitance response transitions into a largely monotonic voltage dependence as shown in Fig. 6.9 (e). The post-cycling characteristic retains only a narrow capacitance modulation window of approximately $\sim$ 6 pF and a small P-V loop, indicating that the dominant ferroelectric contribution has been strongly suppressed while a small residual voltage dependence persists. Notably, this distorted C-V response qualitatively resembles the behaviour reported for metal-ferroelectric-insulator-semiconductor (MFIS) stacks, where the measured capacitance is governed primarily by electrostatic field redistribution across the ferroelectric, interfacial dielectric layer, and semiconductor rather than by reversible ferroelectric domain switching [73]. The C-V response in such systems arises from a combination of interfacial depletion, charge screening, and residual polarisation.

Hence, these observations highlight an important limitation of voltage-sweep–based operation in ferroelectric memcapacitors, similar to the behaviour observed during multistate programming. While amplitude-controlled sweeps provide a convenient means to access and

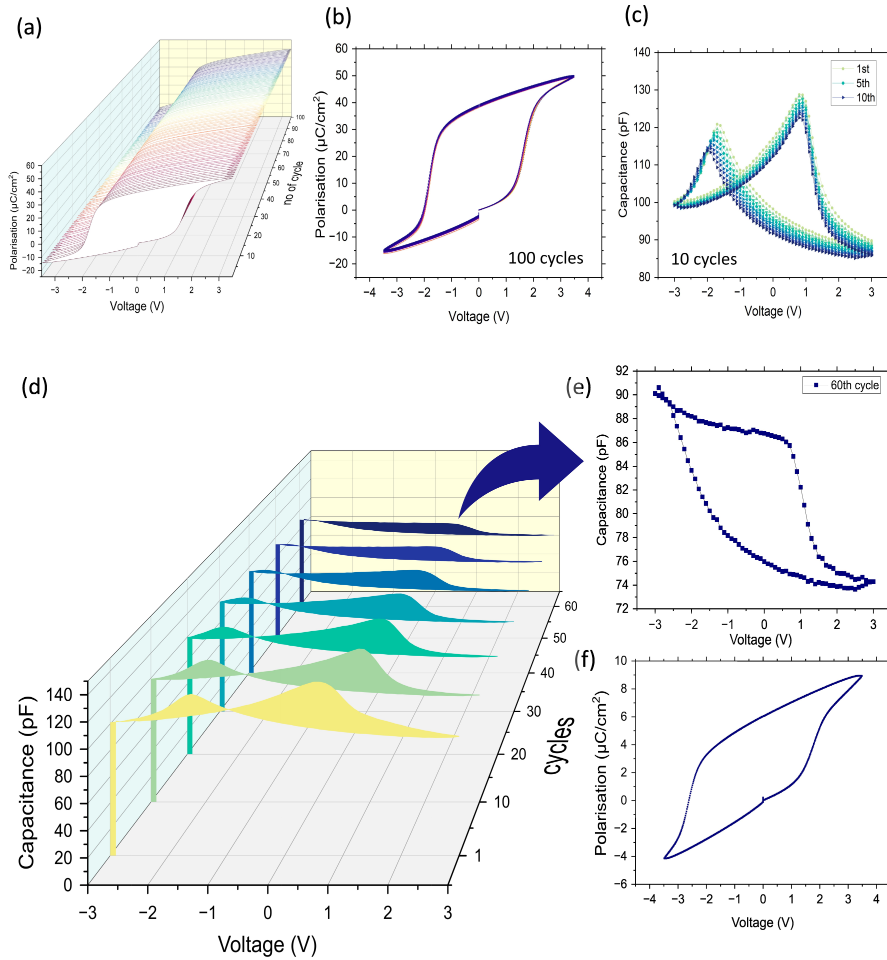

Figure 6.9: **Cycle-dependent degradation of the C-V response in the HZO-MS capacitor.** (a) Three-dimensional representation of consecutive P-V loops. (b) Two-dimensional projection of the same set of P-V loops, highlighting reprogrammability. (c) C-V characteristics measured showing a gradual shift of the capacitance window with repeated sweeps. (d) Extended C-V cycling over a larger number of voltage sweeps, revealing the progressive suppression of the butterfly-shaped response with increasing cycle count. (e) C-V curve after the 60th sweep, showing a largely monotonic capacitance–voltage dependence with a strongly reduced memory window. (f) Representative P-V loop of the same device.

characterise multistate behaviour, they also introduce cumulative electrical stress through repeated traversal of sub-coercive and near-coercive fields. In the multistate regime, this stress manifests as gradual drift and asymmetry of the capacitance window, whereas under repeated C-V cycling, it accelerates into a rapid suppression of the ferroelectric contribution and a transition toward an interface-dominated capacitance response. Hence, developing stress-aware write protocols represents an important direction and forms a key motivation for the future research directions discussed in the following chapter.

6.3 Circuit-Level Demonstration: Tunable High-Pass Filter

Having established the key electrical characteristics of the ferroelectric memcapacitor, the next step is to examine how these properties translate into practical circuit functionality. This serves two purposes: (i) to verify that the programmed capacitance states can be used directly in a passive circuit without any DC bias, and (ii) to demonstrate that the device can realise discrete, non-volatile configurations of a signal-processing block, allowing its behaviour to be evaluated at the system level. Two circuit implementations are considered in this section: a tunable high-pass filter and a tunable RC oscillator. The high-pass filter is analysed in detail as a primary benchmark for analogue operation. In parallel, a relaxation-RF oscillator is demonstrated as a complementary application, illustrating the direct mapping of non-volatile capacitance states to programmable oscillation frequency.

Figure 6.10 (a) shows the experimental platform used to realise the tunable high-pass filter, with the main components marked. The platform consists of a custom PCB interfaced with the packaged HZO-MS devices and external measurement instrumentation. A microcontroller module provides the digital control signals required to configure the on-board MEMS switching elements. In the present configuration, signal routing is performed using two MEMS-based 4-to-1 multiplexers, enabling selection of the desired device. Electrical access to the packaged memcapacitor and the filter output is provided through SMA connectors. Although the PCB includes additional circuitry for pulse driving and analogue switching, these elements are not active during filter operation.

Figure 6.10 (b) shows the RC oscillator implemented as a second circuit-level demonstration of memcapacitor functionality. The oscillator circuit is assembled on a stripboard and electrically interfaced with the filter PCB to provide access to the programmed memcapacitor, supply rails, and signal routing via SMA connections. In this configuration, the memcapacitor serves as the timing element that directly controls the oscillation period. For the Schmitt trigger circuitry, a linear voltage regulator is used to step down the 5 V supply to 1.8 V. This reduced supply voltage ensures stable operation of the comparator while simultaneously limiting the maximum voltage stress applied to the memcapacitor. As a result, the upper and lower switching thresholds are constrained to remain low, as higher voltages are not suitable for reliable operation of these memcapacitors. Although multiple Schmitt trigger footprints are present on the board, only a single device is used in the present implementation. The Schmitt trigger provides the hysteresis necessary for relaxation oscillation, repeatedly charging and discharging the memcapacitor through a fixed resistor of 200 kΩ. Mechanical relays located on the lower section of the board are included to enable manual routing and isolation during testing.

High Pass Filter: For filter experimentation, five capacitance states between 100 and 120 pF were programmed on-chip using the voltage-sweep protocol described previously. For an ideal RC high-pass filter, the cutoff frequency is given by

$$f_c = \frac{1}{2\pi RC}. \tag{6.6}$$

Using $R = 15$ kΩ and $C = 100$–120 pF, the expected cutoff frequency ranges from 106.1 kHz down to 88.4 kHz.

Figure 6.11(b) shows the measured magnitude response of the tunable high-pass filter for five

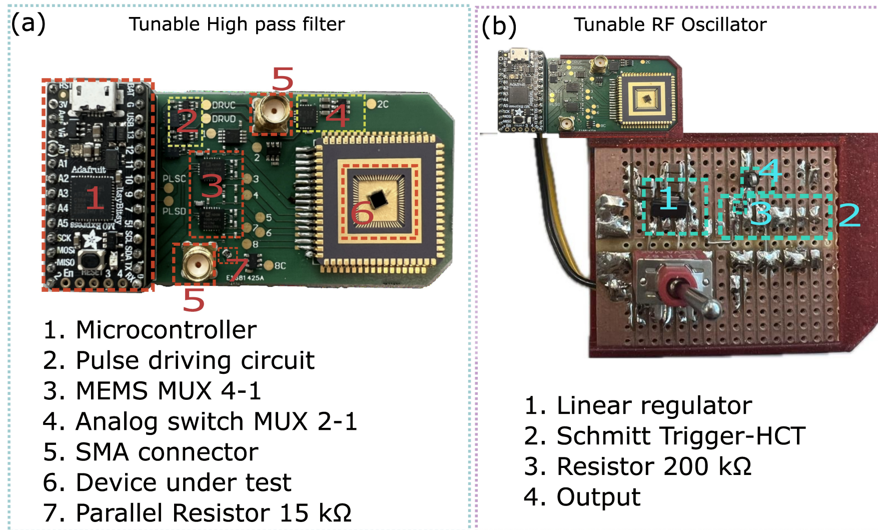

Figure 6.10: **Experimental platforms for circuit-level evaluation.** (a) Experimental platform used to implement a tunable high-pass filter based on a packaged HZO–MS device, with key components marked and labelled. (b) Tunable RC relaxation oscillator interfaced with the same memcapacitor platform, with the main functional elements indicated, demonstrating programmable oscillation frequency.

programmed capacitance states. As the stored capacitance increases from 100 to 120 pF, the cutoff frequency shifts monotonically from 45.5 kHz to 41.1 kHz, following the expected qualitative trend for a first-order RC network. However, two clear deviations from ideal behaviour are observed: the cutoff frequencies are systematically lower than those predicted for an ideal filter, and the pass-band gain does not approach unity but instead saturates at approximately −7 dB across all capacitance states, with some variations as listed in table 6.2. These features indicate the presence of non-ideal elements that only become apparent when the device is embedded in a circuit environment.

The loss mechanisms intrinsic to the ferroelectric memcapacitor, discussed in the preceding section, are insufficient to account for the observed magnitude of pass-band attenuation. Although the dielectric loss tangent increases with frequency, the measured pass-band gain remains largely unchanged across the operating range of the filter, indicating that dielectric loss does not set the absolute level of attenuation. Similarly, the extremely low DC leakage current implies that steady-state conduction through the dielectric does not play a significant role under the small-signal read conditions employed. Instead, intrinsic losses primarily contribute to phase lag and energy dissipation without introducing a strong frequency-dependent reduction in gain.

The dominant contribution to the reduced pass-band gain and downward shift in cutoff frequency is therefore attributed to resistive elements introduced at the circuit level. These include series resistance associated with metal interconnects, contact interfaces, bond wires, packaging, and other parasitic contributions within the measurement setup. Collectively, these effects can be represented by an effective series resistance, R_s, which adds to the nominal filter resistance such that;

$$R_{\text{eff}} = R + R_s,$$

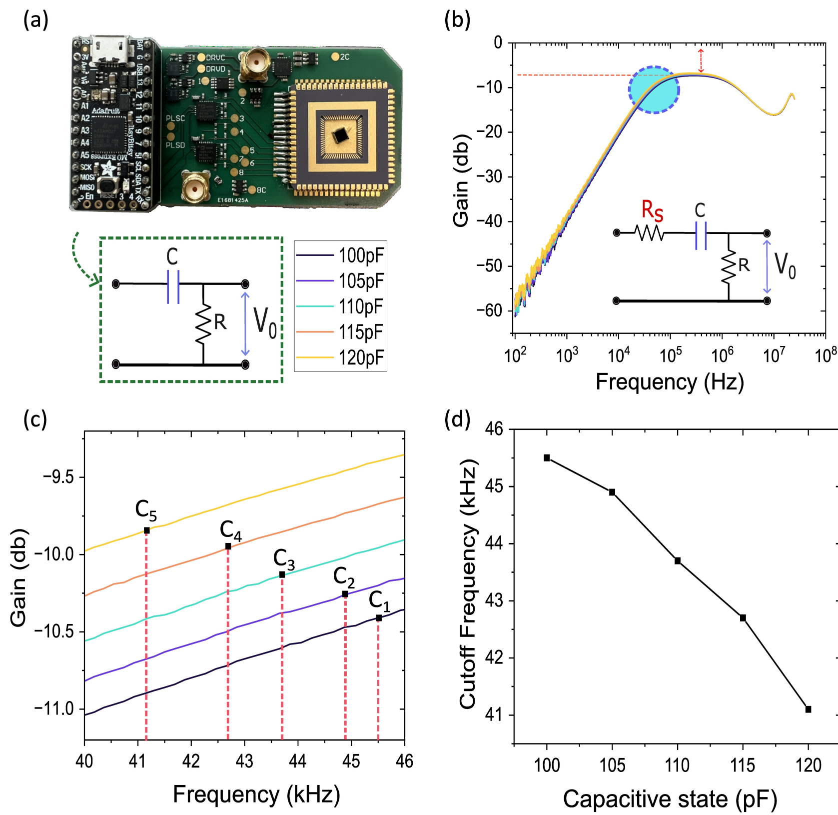

Figure 6.11: **Programmable high-pass filter behaviour.** (a) Experimental filter platform and the corresponding RC high-pass filter configuration employing the HZO-MS device. (b) Measured gain response of the filter for multiple programmed capacitance states, with the equivalent non-ideal RC model indicated. (c) Expanded view of the pass-band region highlighting the relative shift in response for different capacitance states. (d) Extracted cutoff frequency as a function of the programmed capacitance state, demonstrating monotonic tunability. Reproduced from authors own work [159]

Table 6.2: Expected and measured data values for cut-off and passband

Capacitance (pF)	Measured f_c (kHz)	Expected f_c (kHz)	Pass Band (dB)
120	41.1	88.5	-6.85
115	42.7	92.3	-6.96
110	43.7	96.2	-7.1
105	44.9	101.3	-7.3
100	45.5	106.1	-7.4

thereby increasing the RC time constant and lowering the measured transition frequency. At the same time, the presence of R_s limits the transmitted signal amplitude, giving rise to the observed pass-band plateau. From the measured pass-band attenuation, the effective series resistance is estimated to be $R_s \sim$ 18–20 kΩ. Despite these parasitic effects, the filter characteristics remain highly reproducible and exhibit monotonic, well-separated cutoff frequencies for each programmed capacitance state. The states are fully non-volatile, require no external bias to maintain, and are preserved across repeated programming cycles. This robustness is reflected in the smooth progression of cutoff frequencies in Fig. 6.11(c) and

the capacitance–frequency relation in Fig. 6.11(d).

The trend in Fig. 6.11(d) is expected to follow the hyperbolic dependence $f_c \propto 1/C$. In principle, equal changes in capacitance should produce progressively smaller shifts in cutoff frequency as C increases. However, because the measured capacitance range (100–120 pF) spans only a narrow window, the corresponding variation in f_c covers a similarly restricted interval. Over such a limited range, a hyperbolic curve appears almost linear, which explains the near-linear behaviour observed experimentally. The underlying inverse relationship remains consistent with the RC model, and the monotonic decrease in cutoff frequency confirms that each programmed capacitance state maps onto a distinct circuit response.

RF Oscillator A Schmitt-trigger-based RC relaxation oscillator provides a simple and robust platform for translating capacitance modulation into frequency tuning. In this architecture, oscillation arises from the periodic charging and discharging of a capacitor through a resistive path, with the switching thresholds of the Schmitt trigger defining the upper and lower voltage limits of the oscillation cycle. The oscillation period is therefore directly governed by the RC time constant, making such circuits highly sensitive to variations in the capacitance value. When a non-volatile memcapacitor is used as the timing element, the oscillation frequency becomes programmable through the stored capacitance state, without the need for continuous biasing or active tuning circuitry. This makes the relaxation oscillator suitable experiment for assessing the circuit-level impact of multistate capacitance tuning.

Figure 6.12(a) illustrates the operating principle of the Schmitt-trigger RC oscillator employed in this work, that is explained before, while Fig. 6.12(b,c) show the experimental implementation and measured output waveform, respectively. Five distinct capacitance states were programmed into the HZO-MS device and subsequently used to control the oscillation frequency. Due to device-to-device variability and the gradual evolution of the capacitance window discussed earlier, the accessible capacitance range in this oscillator differs slightly from that used in the filter demonstration. Despite this, a clear and monotonic tuning behaviour is observed.

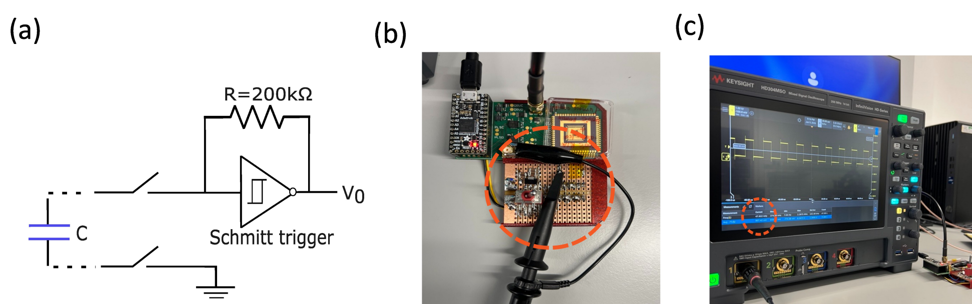

Figure 6.12: **Capacitance-programmable RC oscillator.** (a) Schematic of the Schmitt-trigger-based RC relaxation oscillator, with the memcapacitor acting as the timing element. (b) Experimental oscillator implementation interfaced with the memcapacitor platform. (c) Representative output waveform measured from the oscillator, illustrating stable oscillation under programmed capacitance states.

As the programmed capacitance is increased from approximately 95 pF to 115 pF, the oscillation frequency decreases correspondingly from about 53 kHz to 47 kHz, listed in table 6.3. This inverse relationship between capacitance and frequency is consistent with the expected

RC relaxation behaviour and confirms that the ferroelectric memcapacitor functions effectively as a programmable timing element. Although the present implementation is intended as a proof-of-concept demonstration, it clearly illustrates the potential of ferroelectric memcapacitors for reconfigurable frequency control in compact oscillator architectures and adaptive analogue or mixed-signal systems.

Table 6.3: Programmed capacitance states and oscillation frequency in the tunable RC oscillator.

State	Capacitance (pF)	Frequency (kHz)
C_1	95	53.4
C_2	100	52.2
C_3	105	50.5
C_4	110	49.2
C_5	115	46.9

6.4 Conclusion

This chapter represents the central functional demonstration of the thesis, establishing that the engineered HZO-MS ferroelectric capacitor can operate as a multistate, non-volatile memcapacitive device with a capacitive memory window of approximately 24 pF. Through controlled voltage programming, more than eight stable and well-separated capacitance states were reproducibly accessed with endurance approaching 10^6 cycles and retention exceeding 10^5 s. In addition to discrete multistate operation, the device exhibits the capability for more gradual capacitance modulation and achieves performance comparable to existing reports in the literature while occupying one of the smallest device footprints. The observed capacitive switching behaviour closely mirrors synaptic potentiation and depression, positioning the HZO-MS capacitor as a physically grounded analogue synaptic element for neuromorphic and adaptive electronic systems.

Beyond demonstrating multibit operation, the chapter systematically examined the practical constraints governing device functionality. Area-scaling studies revealed that reliable capacitive memory behaviour requires device dimensions of at least $20 \times 20\ \mu m^2$, with the accessible memory window scaling with active area. At the same time, the achieved capacitance densities are competitive with conventional on-chip MIM capacitors, highlighting the potential of ferroelectric memcapacitors to replace multiple fixed-value elements with a single reconfigurable component and thereby reduce overall circuit footprint. Frequency-dependent measurements further clarified the operational bandwidth of the device, identifying a transition from ferroelectric-dominated behaviour at low frequencies to dielectric-dominated response at higher frequencies, accompanied by moderate but non-negligible dissipative losses.

Crucially, the chapter extended beyond standalone device characterisation to demonstrate circuit-level functionality. Integration of the HZO–MS device into a tunable high-pass filter directly translated discrete capacitance states into monotonic and well-separated cutoff frequencies spanning approximately 4.4 kHz, while simultaneously revealing circuit-level non-idealities that are not apparent from device measurements alone. A complementary RC relaxation oscillator further demonstrated non-volatile frequency programmability over a tun-

ing range of approximately 6.5 kHz, confirming that the memcapacitor can function as a reconfigurable timing element in compact analogue circuits. Together, these demonstrations establish a clear and direct link between ferroelectric switching physics and practical circuit behaviour.

Taken together, the results presented in this chapter provide a comprehensive assessment of multistate ferroelectric memcapacitors from the device to the circuit level. By connecting domain-scale switching processes to system-relevant functionality, this chapter establishes HZO–MS capacitors as a viable platform for non-volatile analogue capacitance tuning and sets the stage for a broader discussion of reliability challenges and future optimisation strategies in the following chapter.

Chapter 7

Conclusion and Future Work

The work presented throughout this thesis establishes a coherent and experimentally grounded foundation for understanding and exploiting memcapacitive behaviour in hafnium-based systems, spanning materials, devices, and circuit-level functionality. While the results demonstrate clear progress toward non-volatile, multistate capacitive elements compatible with modern semiconductor technologies, they also reveal important constraints that must be addressed to enable reliable and scalable deployment. Accordingly, this chapter first summarises the key conclusions, then offers a critical reflection on the challenges identified, and finally outlines realistic future research directions that are already in progress.

7.1 Key Contributions and Conclusion

This thesis has established a comprehensive understanding of memcapacitive behaviour in hafnium-based devices by providing meaningful insight on materials characterisation, device-level electrical behaviour, nanoscale functionality, and circuit-level performance. In doing so, the thesis also defines a structured characterisation protocol that enables a clear distinction between robust and unstable memcapacitive behaviour, providing a practical reference framework for future studies.

Thin-film analysis confirms that device performance and long-term stability are governed by oxide chemistry and phase evolution rather than isolated electrical metrics. XPS verifies chemically stable hafnium-based oxides across all investigated stacks, while XRD reveals annealing-induced structural evolution. These results provide a consistent baseline for interpreting device behaviour and validate assumptions commonly made in the hafnium oxide literature. Beyond these standard techniques, AFM analysis significantly extends the functional interpretation of the materials. PFM provides direct evidence of non-volatility and write-read reproducibility at the nanoscale. In parallel, EFM enables spatial resolution of multiple stable charge configurations using box-in-box writing schemes, demonstrating nanoscale multistate behaviour that is rarely addressed in existing memcapacitor studies. In this sense, the material characterisation meaningfully extends the application of established techniques to extract deeper functional insight.

At the device level, the thesis demonstrates that conventional hafnium oxide memristors in-

herently exhibit coupled memristive and memcapacitive behaviour. While analogue resistive switching is achievable, the associated capacitance modulation is shown to be predominantly binary. For devices with an active area of 20×20 μm^2, a reproducible capacitance memory window of approximately 3 pF is observed, with clear separation between low and high-capacitance states. Scaling the device area to 40×40 μm^2 increases the absolute capacitance and yields an effective capacitive ratio approaching 10, confirming that capacitive modulation scales with device geometry. These findings highlight an important and often overlooked conclusion: devices designed for resistive switching may not possess a fixed capacitance and can exhibit history-dependent capacitive behaviour that influences circuit operation. Although the binary nature of the capacitive response limits the suitability of HfO_x memristors as multistate tunable capacitors, the results emphasise that any application employing memristive devices must consider the possibility of capacitive tunability, either as a functional attribute or as a non-ideal effect.

The thesis further establishes ferroelectric hafnium zirconium oxide capacitors as a fundamentally effective platform for memcapacitive functionality. Robust multistate capacitive behaviour is realised, which is not achievable in defect-mediated systems. Devices with an area of 20×20 μm^2 exhibit a similar memory window as memristor while enabling analogue switching behaviour under voltage control. With increasing device area, for example 60×60 μm^2, a capacitance memory window of approximately 24 pF is achieved, together with stable operation approaching 10^6 switching cycles and retention exceeding 10^5 s. These results clearly demonstrate that ferroelectric polarisation switching provides a scalable and reliable physical mechanism for multistate memcapacitance, surpassing the intrinsic limitations observed in conventional HfO_x devices. Beyond performance enhancement, the thesis addresses several critical aspects of ferroelectric memcapacitors. Switching asymmetry, although frequently reported, is examined here explicitly in terms of its impact on capacitive state accessibility and programming voltage requirements, revealing its direct influence on state recovery and long-term stability. In parallel, analysis of read frequency and dissipative losses defines the practical operating envelope of ferroelectric memcapacitors. Reliable multistate behaviour is shown to require device dimensions of at least 20×20 μm^2, while frequency-dependent measurements reveal a transition from ferroelectric-dominated behaviour at low frequencies to dielectric-dominated response at higher frequencies, accompanied by moderate but non-negligible loss tangents.

Crucially, by packaging the optimised memcapacitors and integrating them into simple analogue circuits, discrete non-volatile capacitance states are directly translated into predictable circuit responses. Although the absolute tuning ranges are modest, approximately 4.4 kHz in a tunable high-pass filter and 6.5 kHz in an RC relaxation oscillator, these demonstrations confirm that multistate memcapacitance can be harnessed reliably in practical circuit environments. At the same time, the observed deviations from ideal behaviour expose circuit-level non-idealities that are not apparent from device-only measurements, reinforcing the necessity of system-level validation when assessing emerging memcapacitive technologies.

7.2 Limitations and Challenges

Having established ferroelectric HZO capacitors as a viable platform for non-volatile, multistate memcapacitive functionality, it is important to reflect on the broader implications and limitations revealed through this work. A central insight emerging from this thesis is that the practical relevance of memcapacitive devices is determined not only by the existence of history-dependent capacitance, but by how reliably such behaviour can be accessed, preserved, and interpreted under realistic electrical and circuit-level conditions.

From a materials and processing perspective, the thesis highlights several constraints that currently limit the translation of hafnium-based memcapacitors toward large-scale integration. In particular, the reliance on high-temperature post-deposition annealing to stabilise the ferroelectric phase poses a challenge for back-end-of-line CMOS compatibility. Although such processing is acceptable for exploratory device studies, future implementations will require either reduced thermal budgets or alternative process flows that preserve ferroelectric functionality while remaining compatible with advanced integration schemes.

Closely related to processing constraints is the issue of device endurance under repeated multistate operation. While the optimised ferroelectric devices demonstrate stable behaviour approaching 10^6 switching cycles, this endurance remains limited when compared to other reported ferroelectric capacitors. The observed degradation under prolonged operation indicates that further optimisation of electrode interfaces and defect populations will be essential to suppress cumulative degradation mechanisms. These findings underscore the importance of film optimisation for improving both device endurance and retention.

One of the most critical insights revealed by this thesis is the strong dependence of memcapacitor reliability on the applied voltage waveform. While dynamic pulse-based switching preserves ferroelectric functionality over 10^5–10^6 cycles, repeated C–V voltage sweeps were found to rapidly suppress the ferroelectric contribution, driving the device toward an interface-dominated response. Even within the functional multistate operating window, repeated bidirectional programming induces a gradual downward drift of the absolute capacitance window and incomplete recovery of the states. These observations indicate that prolonged voltage exposure, particularly under sub-coercive sweep conditions, introduces cumulative modifications to the internal electrical boundary conditions. Consequently, conventional slow-sweep-based characterisation and write schemes are not suitable for sustained multistate operation, and stress-aware programming strategies must be regarded as an essential requirement for reliable long-term memcapacitive functionality.

Finally, the thesis highlights an inherent trade-off between electrically reconfigurable capacitance and low-loss performance. While the measured dielectric loss tangent is compatible with proof-of-concept analogue and frequency-dependent circuit operation, it remains higher than that of conventional fixed MIM capacitors [176]. This reflects a fundamental compromise between achieving strong, programmable internal polarisation dynamics and maintaining ultra-low dissipation. Understanding and managing this trade-off will be critical when targeting specific application domains, particularly in RF and analogue systems, where loss directly impacts performance.

Overall, this thesis does not claim to deliver a fully optimised or deployment-ready memcapacitor technology. Instead, it provides a coherent and reproducible framework for understanding,

characterising, and interpreting memcapacitive behaviour in hafnium-based systems, demonstrating competitive capacitance memory windows within a minimal device footprint. In a field where standardised measurement protocols remain limited and results are often difficult to compare, this reflective assessment defines both the opportunities and the constraints of programmable capacitance, offering a clear reference point for future research and technological development.

7.3 Future Directions

Building on the findings of this thesis, future research is planned along two complementary directions. The first focuses on further improvements at the material and device level, with the aim of enhancing endurance, reducing thermal processing constraints, and minimising dissipative losses. The second direction addresses the extension of memcapacitive functionality from standalone devices to array-level integration. To assess the true scalability and system-level relevance of memcapacitive behaviour, it is essential to move beyond isolated devices and investigate operation under dense integration. In this context, array configurations represent a natural and necessary next step, as they expose interaction effects, device-to-device variability, and access constraints that fundamentally determine practical applicability.

7.3.1 Standalone Device Optimisation

A major pathway toward improving ferroelectric memcapacitor performance lies in materials research and device-stack optimisation. A key advantage of this approach is that it can directly leverage the extensive process knowledge developed for hafnium-based FeFET and translate these strategies to ferroelectric memcapacitors [177, 178, 179, 159]. In FeFET technology, challenges related to endurance degradation, thermal budget constraints, and interfacial stability have been intensively investigated, resulting in multiple demonstrated routes toward low-temperature processing and enhanced cycling robustness. The strong overlap in materials systems and switching physics makes this body of work a natural and well-founded starting point for advancing ferroelectric memcapacitors beyond the limitations identified in this thesis.

To simultaneously address thermal budget, endurance, and dissipative loss, future work will investigate annealing-free and low-temperature ferroelectric stabilisation strategies that have proven effective in FeFETs. These include compositional engineering of HZO, such as selective dopant incorporation to promote orthorhombic phase formation at reduced temperatures, as well as surface and interface energy engineering to stabilise ferroelectricity without conventional high-temperature post-metallisation annealing. When adapted to metal-ferroelectric-metal capacitor geometries, such approaches are expected to improve cycling endurance by reducing defect-assisted degradation, while also offering potential pathways toward reducing dielectric loss, which remains to be explored in detail.

7.3.2 Array Integration on Wafer and CMOS Chip

Beyond standalone device optimisation, a key requirement for translating ferroelectric memcapacitors into system-relevant technologies is their integration into dense array architectures capable of scalable and parallel operation. This requirement is particularly evident in neuromorphic and memory-centric computing, where dense arrays enable high storage density, parallel computation, and energy-efficient vector-matrix operations. In this context, several recent studies have already demonstrated ferroelectric memcapacitor arrays for neuromorphic inference and in-memory computing, establishing array-level operation as a critical benchmark for practical relevance [16, 180].

Crossbar arrays provide a compact and scalable geometry in which memory elements are located at the intersections of orthogonal word and bit lines. While capacitive crossbar networks are not new as a concept and have long been employed in applications such as touch sensing and display technologies, their use as programmable memory or computing elements is comparatively recent. In memory-centric architectures, the crossbar topology is particularly attractive as it naturally supports collective state updates and analogue multiplication-accumulation operations, making it a foundational structure for emerging in-memory and neuromorphic computing systems. Extending memcapacitive functionality from single devices to array-level integration is therefore a necessary step toward system-relevant implementation.

However, array integration introduces challenges that are not apparent in standalone device measurements. In dense crossbar configurations, unintended current pathways can form through unselected cells during read or write operations, commonly referred to as sneak-path effects. These parasitic conduction paths distort the effective readout signal, reduce programming selectivity, and lead to increased energy consumption, with the severity of these effects scaling unfavourably as array size increases. Additional complications arise from parasitic coupling between neighbouring cells and device-to-device variability, further degrading read accuracy and increasing peripheral circuit complexity. In memristor-based crossbar arrays, sneak-path currents are particularly problematic due to the inherently conductive nature of resistive switching elements, which results in high write and read currents and increased energy consumption at the array level. To ensure reliable addressing and suppress unintended current paths, practical memristive arrays therefore incorporate access devices such as transistors or diodes at the cell level, leading to one-transistor-one-resistor (1T1R) architectures. The selector device electrically isolates unselected cells during read and write operations, enabling controlled programming and readout. While effective, this configuration introduces additional dynamic power consumption associated with current-driven operation and selector biasing, and imposes area and circuit overheads that influence overall array density and energy efficiency. These considerations motivate the exploration of alternative array concepts that retain scalability while reducing current-driven power dissipation.

Memcapacitor-based arrays offer a complementary approach to resistive memories, since capacitive state modulation intrinsically operates at low current levels and enables near-zero static power consumption. These characteristics directly address the current-driven energy penalties identified in resistive crossbar architectures and make memcapacitors especially attractive for energy-efficient memory and computing systems, both with and without selector devices [133]. As a first step toward scalable integration, wafer-level 8×8 memcapacitor arrays are proposed as a compact platform for investigating array-level behaviour. Two complementary array architectures will be explored in parallel. Capacitor-only crossbar arrays will be used to probe the intrinsic behaviour of memcapacitors under dense integration, enabling

direct assessment of array-level interactions and understand working mechanisms in the absence of selector. In contrast, one-transistor–one-capacitor (1T1C) architectures introduce an explicit selector device for each memcapacitor cell, enabling individual addressing, controlled programming, and reproducible readout. A direct comparison between capacitor-only and 1T1C configuration, therefore, allows intrinsic memcapacitive behaviour to be decoupled from access-device-assisted operation, clarifying the trade-offs between array density, electrical control, and reliability.

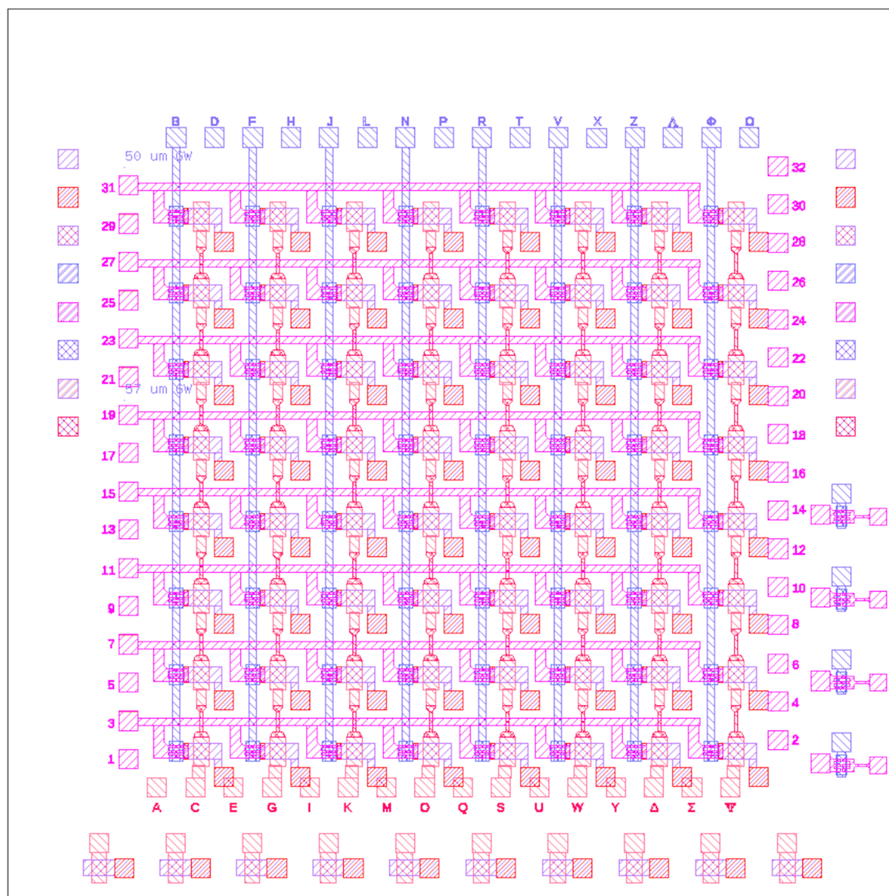

Figure 7.1: **Wafer-scale 1T1C array mask layout.** Mask layout of a wafer-scale 8 × 8 one-transistor–one-capacitor (1T1C) array designed using KLayout. The layout realises a crossbar architecture in which ferroelectric memcapacitors are individually accessed through dedicated transistor selectors, enabling controlled programming and readout at the array level.

Figure 7.1 illustrates the layout of the proposed 1T1C array, which also incorporates standalone devices for independent benchmarking. For the selector device, amorphous indium–gallium–zinc oxide (IGZO) transistors will be investigated due to their low off-state leakage, compatibility with low-temperature processing, and suitability for back-end-of-line integration. IGZO-based access devices have been extensively studied in ferroelectric memory and FeFET technologies, providing a well-characterised and reliable foundation for array development. These attributes align closely with the thermal budget constraints identified in this thesis and make IGZO a promising candidate for integration with ferroelectric memcapacitors [181]. By evaluating array behaviour with and without selector devices, and by mapping performance across the wafer, this approach will enable systematic identification of the limits

imposed by array density and access-device design.

In parallel, chip-level integration is also being pursued through the tape-out of a dedicated 8×8 1T1C crossbar integrated circuit, as shown in Fig. 7.2. The test chip has been implemented in a commercially available 180 nm CMOS technology and is specifically intended to evaluate the back-end-of-line (BEOL) integration of in-house ferroelectric memcapacitors. The array is built on a custom nMOS selector device substrate, enabling controlled electrical access to individual cells while supporting BEOL-integrated capacitors with lateral dimensions extending up to $100 \times 100\ \mu m^2$.

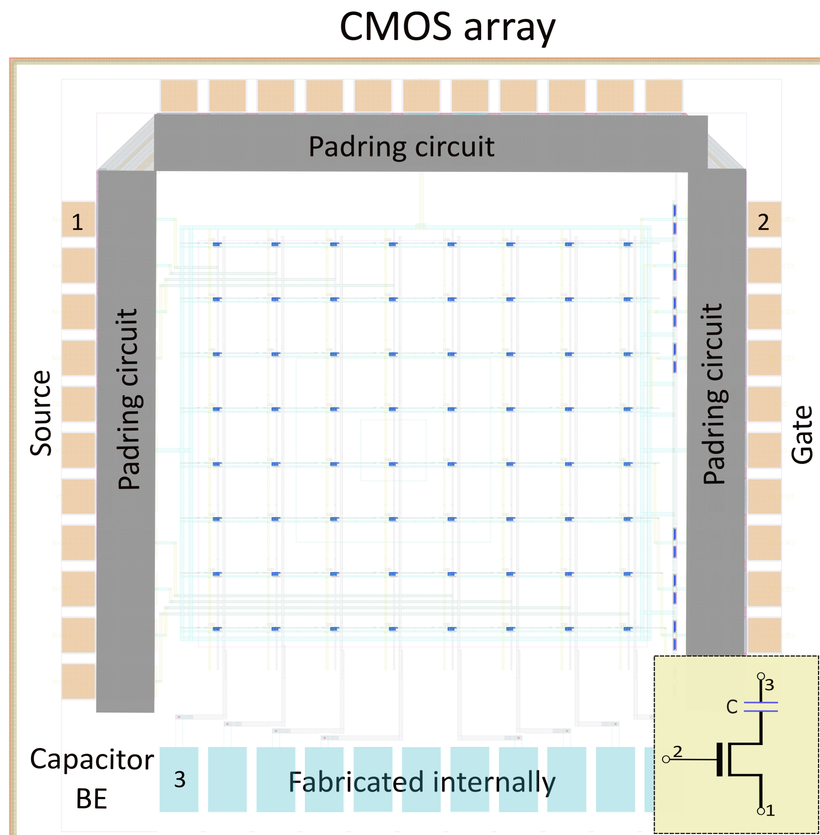

Figure 7.2: **1T1C crossbar-chip layout.** Top-level layout of the chip-level 8 × 8 one-transistor–one-capacitor (1T1C) crossbar array implemented in a commercial CMOS technology. The layout shows the central array region with orthogonal word and bit-line routing, surrounded by peripheral circuitry and bonding pads for electrical access. This design serves as a platform for evaluating back-end-of-line integration of ferroelectric memcapacitors and array-level electrical behaviour under realistic on-chip conditions. The inset shows the corresponding 1T1C electrical circuit schematic.

In this design, the transistor elements, including the source and gate terminals, are fabricated at the foundry, while the capacitor bottom electrodes are intentionally left unpatterned during CMOS processing to enable subsequent in-house fabrication. The inset in Fig. 7.2 illustrates a single 1T1C configuration, in which the selector transistor enables addressing and selection of individual capacitors. Hence, arranged in a crossbar architecture, multiple capacitive elements can be accessed and programmed for array-level operation. In addition, an emulator chip incorporating fixed on-chip capacitors has also been designed. This emulator provides

a reference platform for functional validation of the CMOS circuitry and array addressing scheme, ensuring correct chip operation prior to, and independent of, BEOL ferroelectric capacitor integration.

The primary objective of this chip-level platform is not immediate application deployment, but systematic technology evaluation under realistic on-chip conditions. In particular, it enables assessment of ferroelectric capacitor deposition, patterning, electrical interfacing, and device-to-device variability when integrated directly above CMOS circuitry. The conventional 1T1C crossbar topology further provides a flexible and widely adopted framework that can be readily extended toward diverse proof-of-concept demonstrations, including memory operation and computing-oriented primitives. By establishing this controlled on-chip test, this work creates a critical bridge between wafer-scale studies and future system-level implementations of memcapacitive technologies.

Once integration challenges at both wafer and chip levels are sufficiently understood, these platforms can be extended toward application-oriented demonstrations, including adaptive analogue circuits, reconfigurable RF building blocks, and memory-centric or neuromorphic computing primitives. In this way, the array-level research directions outlined here build directly upon the experimental framework and insights developed in this thesis, defining a clear and realistic pathway from single-device memcapacitors toward scalable, CMOS-compatible system-level array implementations.

Chapter 8

Appendix

In addition to the device structures discussed in the main chapters of this thesis, several other material systems and device variants were fabricated and electrically characterised during the course of this work. While these devices were explored as potential candidates for non-volatile capacitive tuning, a range of practical and physical limitations including highly resistive behaviour, volatile switching, and the absence of stable and reproducible impedance states makes them unsuitable for the targeted memcapacitor applications. The table summarises these device systems and the corresponding DC and AC electrical behaviour observed. In addition, selected examples of device behaviour are discussed in detail.

Table 8.1: Device material systems, fabrication processes, and electrical behaviour.

Material	**Dep.**	**Temp.**	**BE/TE**	**DC behaviour**	**AC / Impedance response**
TiO_x (20 nm)	E-beam	RT	Pt/Pt	Repeatable resistive switching.	No switching
TiO_x (10 nm)	ALD	100	Pt/Pt	Highly resistive; no observable switching.	Not suitable
TiO_x (10 nm)	ALD	200	Pt/Pt	Volatile resistive switching.	States not reproducible
TiO_x/Al_2O_3 (9/1 nm)	ALD	200	Pt/Pt	Near-ohmic response; no stable switching.	Not suitable
HfO_x (7 nm)	ALD	100	TiN/TiN	Highly resistive; no observable switching.	Not suitable
$HfTiO_x$ (10 nm)	ALD	250	TiN/TiN	Volatile resistive switching.	Negligible phase switching

TiO_x E-beam: Motivated by previous literature reports suggesting the possibility of capacitive switching in TiO_x systems, TiO_x was selected as the first material platform for investigation for this thesis [72, 80]. The e-beam deposited TiO_x devices exhibited stable and reproducible current-voltage characteristics, as shown in Fig. 8.1 (a), with repeatable switching behaviour observed over multiple voltage cycles. XPS analysis, shown in Fig. 8.1 (b), confirmed the formation of non-stoichiometric TiO_x films with mixed titanium oxidation states. The presence of Ti^{3+} and Ti^{4+} components is consistent with oxygen-deficient TiO_x and supports defect-mediated conduction mechanisms commonly associated with resistive switching in this material system. Despite the well-behaved DC characteristics, impedance spectroscopy measurements revealed no discernible change in the impedance response between the different resistive states, as shown in Fig. 8.1 (c) and Fig. 8.1 (d). Both the impedance magnitude and phase remained largely unchanged across the measured frequency range. This indicates that the observed switching is predominantly resistive in nature, with only marginal changes in resistance that do not significantly perturb the effective capacitive contribution of the device. As a result, these devices were not suitable for further investigation as memcapacitors.

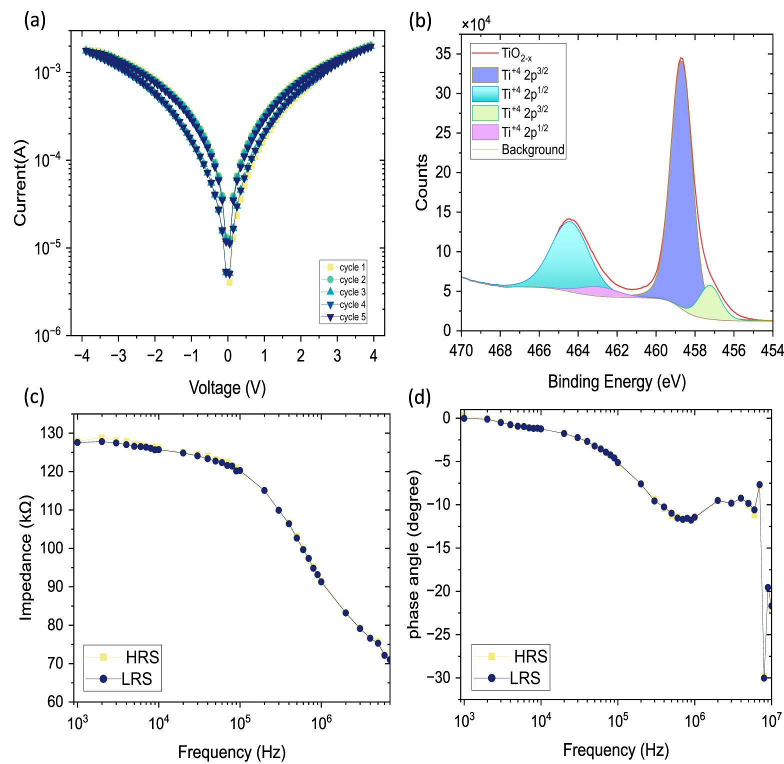

Figure 8.1: **Electrical and material characterisation of e-beam deposited TiO_x devices.** (a) Current-voltage characteristics demonstrating repeatable resistive switching over multiple voltage cycles. (b) Ti 2*p* XPS spectrum indicating mixed titanium oxidation states consistent with non-stoichiometric TiO_x. (c-d) Impedance magnitude and phase as a function of frequency for HRS and LRS overlapping.

TiO_x-ALD: TiO_x films deposited by ALD at 200°C shows a different current-voltage characteristics as shown in Fig. 8.2 (a), but exhibit clear switching behaviour with a characteristic pinched hysteresis, indicating electrically active devices capable of repeated DC operation. However, the switching behaviour of these devices was found to be volatile in nature. This volatility becomes particularly evident in the impedance spectroscopy data shown in Fig. 8.2(b). The impedance spectra exhibit significant variability between identical resistive states, and repeated programming and measurement cycles fail to reproduce consistent impedance trajectories. In several cases, states accessed during an initial measurement could not be reliably recovered upon subsequent testing. This behaviour suggests that the switching mechanism in ALD-deposited TiO_x at elevated growth temperatures is governed by unstable or weakly confined defect configurations that relax on timescales comparable to the impedance measurement itself.

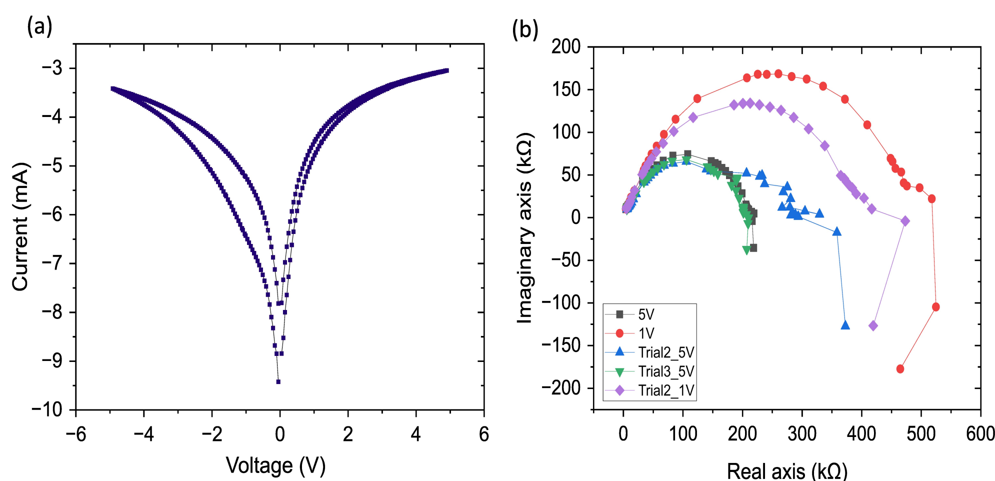

Figure 8.2: **Volatile TiO_x device deposited by ALD.** (a) Current–voltage characteristics showing resistive switching behaviour. (b) Nyquist plots measured after repeated programming, demonstrating significant variability and lack of reproducibility between identical resistive states, indicating unstable impedance behaviour.

$HfTiO_x$-ALD: The $HfTiO_x$ device exhibits repeatable current–voltage characteristics with clear resistive switching behaviour, as shown in Fig. 8.3(a). However, the switching is volatile, with the programmed low-resistance state (LRS) relaxing towards the high-resistance state (HRS) over time, as shown in the time-dependent resistance measurement in Fig. 8.3(b). In contrast to the ALD-deposited TiO_x devices discussed earlier, the impedance spectra of the $HfTiO_x$ device appear comparatively more stable. As shown in Fig. 8.3(c) and Fig. 8.3(d), repeated impedance measurements following SET and RESET operations do not exhibit large variations in either impedance magnitude or phase, despite the underlying volatility observed in the DC characteristics.

However, it is important to note that the $HfTiO_x$ devices operate in a highly resistive regime. As a result, any subtle impedance changes associated with volatile state relaxation may fall below the sensitivity of the impedance spectroscopy measurement. Moreover, the phase response shows minimal separation between the HRS and LRS across the measured frequency range, indicating that the capacitive contribution remains largely unchanged between states. This observation implies that any capacitance modulation in the device is negligible. Consequently, despite the relatively well-behaved impedance spectra, the absence of a measurable

and state-dependent phase response confirms that $HfTiO_x$ devices do not exhibit meaningful capacitive tuning. Furthermore, the volatile nature of the switching makes it difficult to unambiguously decouple intrinsic impedance behaviour from time-dependent resistance relaxation, limiting the reliability of impedance-based state discrimination in this system.

Nevertheless, the same characteristics that limit the suitability of $HfTiO_x$ devices for memcapacitor applications makes them attractive for alternative use cases. In particular, these devices operate at low switching voltages, exhibit forming-free behaviour, and maintain high resistance levels. Accordingly, the HfTiO device investigated here was employed as the active element in a multi-channel auditory signal encoder with adaptive resolution based on volatile memristors, where volatility and dynamic state evolution are desirable features [182].

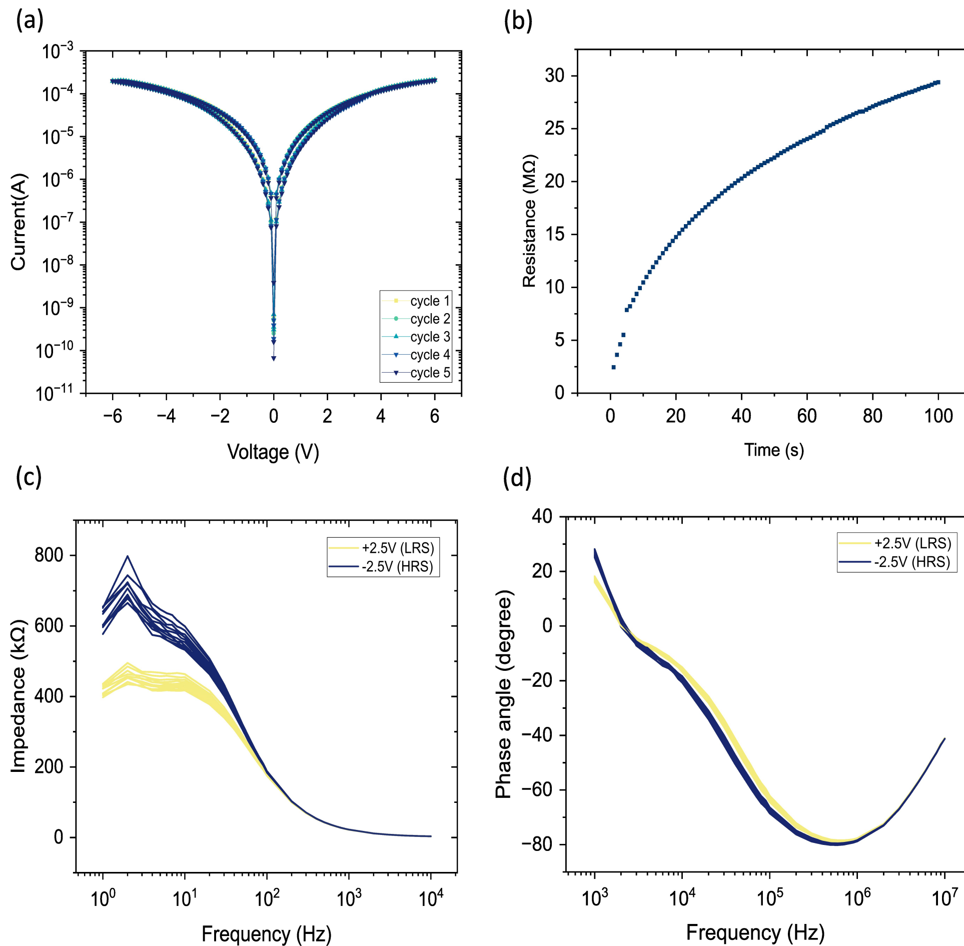

Figure 8.3: **Volatile HfTiO device with state-dependent impedance response.** (a) Current-voltage characteristics showing repeatable resistive switching behaviour. (b) Time-dependent resistance evolution indicating volatile relaxation of the programmed low-resistance state. (c) Impedance magnitude as a function of frequency for the HRS and LRS. (d) Corresponding phase response, showing minimal phase separation between states and indicating negligible capacitive modulation.

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