Digital Parametric Testing

Thesis submitted by
Derek Ward
for the degree of
Doctor of Philosophy

Edinburgh Microfabrication Facility,
Department of Electrical Engineering,
University of Edinburgh,
Edinburgh,
Scotland.

February 1991

Abstract

As minimum geometries of VLSI processes continue to shrink there have been two main effects on the field of parametric test. Firstly, structures must be able to characterise these smaller geometries and secondly the space for test structures has become more limited due to the requirement for them to be located in the scribe channel. The work of this thesis investigates methods of increasing the efficiency of test structure implementation to alleviate these problems.

This work has demonstrated SPICE parameter extraction from test transistors accessed via a digitally addressed multiplexer: firstly using test circuits, to analyse pass transistor effects, then on a test chip using multiplexed access. The technique allows SPICE parameters to be extracted from transistor arrays with a large saving in the number of probe pads and hence overall silicon area.

Digital misalignment structures have been implemented for the characterisation of small geometry processes. Use of such structures is demonstrated in this thesis using both a shift register output and a novel 'diode vernier' scheme. One of the main drawbacks of using shift register structures has been the requirement for a large amount of functional circuitry. The diode vernier introduced in this thesis is a simply designed structure that can be easily tested with standard parametric test equipment and requires only one diode per test structure element.

Finally, a digital process control chip has been fabricated to integrate the ideas presented in this thesis. This uses multiplexers to access both test transistors and diode vernier structures. It demonstrates the feasibility of using a digital approach to parametric test chip design which has the potential to signficantly reduce the area required for test structures.

Acknowledgements

Firstly I would like to thank my supervisor Dr A.J. Walton for his invaluable enthusiasm, help and support throughout this project.

I am grateful to the many technical staff of the EMF, both past and present, who have processed masks and wafers for me and without whom this project would not have been possible: John Laurie, Joe Gow, Alec Ruthven, Brian Neilson, Catherine McGuigan, Dave Hope, Jock Fraser and many others, who I hope I have not offended by forgetting or not mentioning individually. I would like to thank the following staff for special praise: Mr Alan Gundlach for his continual good cheer in providing help and advice on processing, Mr Bill Gammie for his advice and help on design, test structures and interfacing with RAL Prime F, Dr J.T.M. Stevenson for producing stepper reticles and Dr R.D. Mackie for use of his DAS functional test system and instructions in its operation.

Mention should also be made of my industrial supervisor Dr H.D. Coltman for his help and interest, Dr A. Aitken and Elizabeth Aitken, especially the latter, for proof reading parts of this thesis and all the EMF PhD students, too numerous to mention, for mutual support, help, understanding and advice, friendly or otherwise!

I would like to acknowledge the Science and Engineering Research Council for their grant assistance and GEC Hirst Research Centre for their CASE sponsorship of this project.

To my mother

Margaret Kennedy Goodlet Ward

1929-1980

Contents

Chapter 1

Introduction

1.1. Introduction

The beginnings of the semiconductor industry as a manufacturing technology for the fabrication of large transistor arrays became feasible in 1957 when Texas Instruments developed the first IC using the silicon planar process. This began the era of the large scale production of silicon wafers capable of having multiple similar devices. This brought economies of scale to the semiconductor industry as did the subsequent introduction of automation. These advances continue today, where for example increased wafer size allied to reductions in minimum device geometries make the production of silicon circuits a highly complex manufacturing process. As a result, increased control of the fabrication process is required to successfully manufacture ICs. Silicon processing has unique properties which pose problems for its control which are not encountered in traditional manufacturing environments. Of these problems the question of scale is most pronounced in contrast with these traditional industries. For example a single silicon chip may be $5mm \times 5mm$ yet contain several tens of thousands of transistors. In this case simple visual checks or spot measurements which are adequate for checking macro-sized objects are no longer appropriate. Allied to this there is the added difficulty that the electrical properties of the silicon devices must be controlled to tight tolerances to ensure optimum circuit performance.

This control of the fabrication process falls into two distinct categories; in-line checking after individual process steps and off-line analysis. The latter consists of electrical checks at the end of the process on test structures. These wafers have undergone the complete processing cycle although in some cases they may only have been processed for a subset of the full process. "Parametric testing" describes the part of the control methodology involving off-line electrical testing of test structures and provides information which can be used by the fabrication engineer to monitor and control the process. Therefore parametric test is an important and integral part of the full silicon fabrication sequence due to its

ability to aid process control of both physical and electrical parameters. It achieves this by not only helping to identify drifts in measured parameters but as a quality control aid to weed out 'bad' wafers before full functional testing. A 50% saving in cost is a commonly quoted industry statistic for a bad wafer being screened out at the parametric, rather than at the functional test stage. The latter being a time consuming and expensive part of the fabrication sequence as each die on all wafers must be tested for correct functionality against specifications [1].

Parametric testing is thus a valuable tool but if it is to be seen to remain a useful part of the fabrication sequence it must continue to be capable of making accurate, meaningful measurements at the geometries of the processes it is aiming to control. As process geometries have shrunk the consequence has been that tighter tolerances are placed on functional devices characteristics. This task of producing devices to these characteristics has become more and more demanding and hence parametric test structures must also be capable of making measurements of these tighter tolerances.

With this problem in mind this project was developed to help allow parametric test continue as a useful contributor to process control.

1.2. Objectives

The primary objective of the project was to demonstrate the feasibility of using on-chip switching for parametric testing. This objective could be broken down into three subsidiary parts. The first of these was was to place part of the test chip measurement system onto the chip itself. This involved replacing part of the switching matrix of the parametric test system with circuitry on-chip which would achieve the same function. This has the advantage that faster switching times are possible since transistor switches are used rather than the electro-mechanical relays in the tester's switching matrix [2]. The second was to investigate the use of transistors as switches. This is of major importance when the analogue characteristics of the device under test (DUT) are being measured. The final one was to use non-analogue, digital measurement structures in the above situation where the switch characteristic is of less importance.

1.3. Thesis Structure and Chapter Outlines

This section gives a summary of the contents of each of the subsequent chapters of this thesis.

Chapter 2 reviews the silicon fabrication sequence and breaks it down into its component parts. The relevance of control for each individual process step is shown and both in line and electrical parametric methods are discussed.

Chapter 3 reviews the history of process control chips (PCCs) and then details the design and use of individual test structures for resistivity, linewidth and misalignment measurement. The use of other structures such as MOS capacitors and other specialised devices are mentioned as are test transistors used for circuit and device parameter extraction. Area test structures for yield, reliability and design rule checking are then described. Finally parametric test systems, their evolution and history, along with a description of existing systems is presented.

Chapter 4 introduces the concept and use of on-chip switching, gives previous uses of on-chip switching, and highlights the advantages of such an approach. The aim of the work is detailed and the results of SPICE analysis of the switching circuitry given. The objectives of the test chips designed are discussed along with their measurement and suitability for SPICE parameter extraction.

Chapter 5 concerns the work involved with digital vernier structures and describes their concept together with previous implementations. In particular the design and implementation of a U-shaped toothed vernier is explored. Analysis of the previously developed 'shift register vernier' is presented and reasons for its non-functioning suggested. A new design of its output circuit is presented and a test chip with X and Y verniers for three different layer to layer misalignments implemented using this circuit. The failure of this new shift register design is discussed in detail and a subsequent redesign presented which resulted in a fully functional dynamic shift register. The use of a novel accessing scheme for verniers, as an alternative to shift register use, is presented together with its application to many parametric test structures.

Chapter 6 outlines the design of the final, fully digital PCC which integrates the work presented in chapters 4 and 5. The layout and structures are described and the results discussed.

Chapter 7 gives the conclusions of the project and outlines several possibilities for future work to exploit the work of the thesis.

Appendix 1 is a run sheet for the standard EMF 6μm NMOS process that was used for all designs made for this thesis project.

Appendix 2 defines the SPICE (level 3) parameters and their meaning.

Appendix 3 gives a list of published papers relevant to this thesis.

References

1. D. Martin, "Parametric Testing," *SERC School on Microfabrication 1988*, pp. 16.1-16.17, Edinburgh, April 1988.

2. A.J. Walton, J.M. Robertson, R. Holwill, and B. Moore, "On Chip Switching for DC Parametric Testing," *Electronics Letters*, vol. 21, no. 10, pp. 422-423, May 1985.

Chapter 2

Wafer Processing and its Control and Measurement

2.1. Introduction

This chapter summarises the main physical processes for MOS device fabrication and the relation between them necessary to produce completed circuits.

Since the development of the integrated circuit and the silicon planar process, development has continually been towards smaller device geometries. This has been reflected by the use of more sophisticated processing techniques and equipment and has resulted in the need for these advanced processes to be ever more accurately characterised since much tighter tolerances are necessary for small geometry processes. Hence in recent years the control of the process has become significantly more important.

Although the individual process steps and processing tools have changed with diminishing minimum process geometries the fabrication process has remained at heart, an essentially cyclical process, with several iterations through the layer deposition (growth)/ion implant, photolithography and etch cycle. This cycle is illustrated by figure 2.1. The number of iterations is dependent on the technology but is typically six for a simple NMOS process and eight for an equivalent CMOS one. However the mask count can range from 5-20 depending on the process with the trend toward higher numbers for increasingly more complicated processes. An example of an NMOS process runsheet showing the various process steps is given in appendix 1. This runsheet is for the standard EMF $6\mu m$ NMOS process which was employed for all the test chips fabricated for the work contained in this thesis.

2.2. Wafer Production

The silicon used for wafer manufacturing is produced from electronic grade silicon (EGS) which is a high quality silicon with a very low level of residual impurities. This is especially true for the major doping elements boron and phosphorus whose concentrations

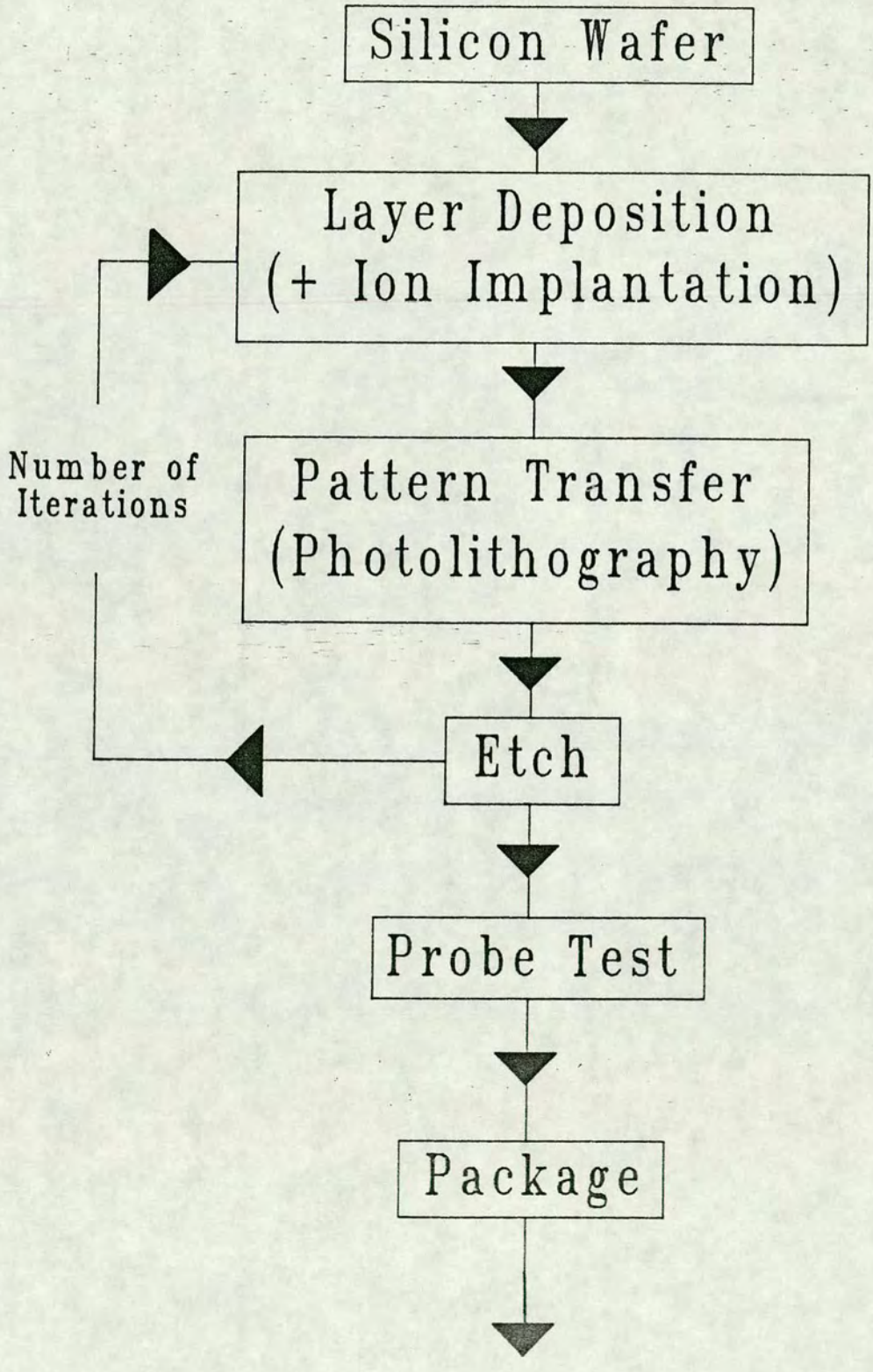


Figure 2.1. The silicon fabrication cycle.

are in the parts per billion range [1]. Virtually all silicon for VLSI production is prepared by the Czochralski technique and the single crystal silicon growers used are known more commonly as 'pullers' due to the method employed [1]. In this technique EGS is melted in a crucible with crystal growth occurring from a seed crystal held above the melt which is slowly pulled and rotated upwards in tempo with the growing crystal of silicon [1]. The complete, grown crystal is referred to as an 'ingot' or 'boule' and tests are made on it at this stage for any defects. These include four point resistivity measurements as well as crystallographic tests on sectioned parts.

The production of wafers from this boule then requires several further operations involving sectioning, chemical etching and polishing [1]. During this process X-ray analysis of the boule is required to locate the crystallographic planes so that the primary and secondary flats can be ground onto the wafers. (The primary flat is located relative to a known crystallographic axis while the secondary position relative to the first identifies the substrate doping and orientation). At the end of the wafer production process the finished wafers are again tested with the electrical, mechanical and crystallographic properties characterised before shipment to customers.

2.3. Layer Growth and Deposition

2.3.1. Oxidation

Thermally grown layers of SiO_2 form both the important gate oxide of the MOS transistor and the field oxide which forms part of the physical device isolation. As final device performance is dependent upon gate oxide quality it is very important that a high degree of process control is exercised.

Silicon has a high affinity for oxygen and an oxide layer rapidly forms when it is placed in an oxidising ambient. Silicon oxidation can take place in either a dry or a wet oxidising ambient. In the former, oxygen alone reacts with the silicon,

$$Si\,(solid) + O_2 \rightarrow SiO_2\,(solid) \tag{2.1}$$

In wet oxidation, water vapour reacts with the silicon to form the oxide

$$Si\,(solid) + 2H_2O \rightarrow SiO_2\,(solid) + 2H_2 \tag{2.2}$$

In both cases the growth of the SiO_2 layer proceeds by the diffusion of the oxidising species

through the oxide layer, the oxide growth occurring at the $Si-SiO_2$ interface. A model of this growth was first proposed in 1965 by Deal and Grove who proposed two growth regimes [2]. For a time (t) which is large the oxide thickness (x_0) is described by the following equation,

$$x_0^2 = Bt \tag{2.3}$$

where B is the parabolic rate constant. If t is small then the oxide thickness is given by,

$$x_0 = \frac{B}{A}(t + \tau) \tag{2.4}$$

where $\frac{B}{A}$ is the linear rate constant and τ the time to create an oxide of thickness x_i in any previous oxidation step [3,4]. The physical processes which control these two equations are diffusion and reaction controlled respectively with equations 2.3 and 2.4 valid for both wet and dry oxidation. For dry oxidation the constant τ in equation 2.4 is such that the product $\frac{B}{A}\tau$ gives the equivalent of approximately 200-250$\mathring{A}$ oxide at $t=0$, whereas for wet oxidation the constant is zero [3].

Several physical processes effect oxidation rates which are obviously reflected in the two rate constants. Most notable amongst these are Si substrate orientation, substrate doping and the presence of chlorination in the feed gas [3,4]. These change either the linear rate constant for those associated with surface effects (substrate orientation and doping) or the parabolic constant for diffusion effects (chlorination).

Oxidation is normally performed in furnace tubes at temperatures ranging from 750-1250°C with a temperature control of better than ± 0.5°C which ensures uniformity [4]. Wafers are cleaned and dried and then placed vertically in a slotted paddle or boat. They are then placed in a furnace which may be 'idling' at a low temperature (750-800°C). The furnace temperature is then ramped up to the oxidation temperature for the desired period before ramping down and unloading. Furnace liners, wafer boats and paddles are normally made of quartz for low contamination, although recent interest has also focussed on the possible use of other materials such as silicon or silicon carbide. Newer techniques such as the use of vertical furnaces and cantilevered wafer loading systems have been investigated and have found use. Processing gases are regulated by electronic mass flow controllers which are themselves under microprocessor control which can easily be used to store, develop and run process 'recipes'.

The choice between wet and dry oxidation depends on the thickness and properties required of the oxide. Gate oxides which are relatively thin and need a low interface charge are grown typically in dry oxygen, most usually with HCl to reduce mobile ion contamination. Thick field oxides normally utilise wet oxidation to facilitate rapid growth.

The SiO_2 and the $Si-SiO_2$ interface have associated charges, generally classified into four types and labelled as shown in figure 2.2 [3,4]. These charges are important for device operation as they can induce charges in the underlying silicon channel region and can also affect yield and reliability.

Q_f, sometimes described as Q_{ss}, is a charge (usually positive) fixed in the oxide near the $Si-SiO_2$ interface. Substrate orientation, oxidation and annealing conditions are the main factors influencing values of this charge. Q_m is due to mobile electronic charges in the bulk oxide and is caused by ionic contamination during processing. The most common contaminants are positive sodium and potassium or heavy metal ions. Q_{ot} is the oxide trapped charge caused by electrons or holes contained in the bulk oxide. Radiation, avalanche injection or oxide currents are the main causes of these charges. Finally Q_{it} is the charge trapped at the $Si-SiO_2$ interface. A number of explanations such as oxidation defects and metallic impurities have been suggested as causing this.

2.3.2. Chemical Vapour Deposition (CVD)

Deposition of layers is an important part of the MOS fabrication process and apart from oxide growth and some forms of metal deposition most layers are produced by CVD. The requirements of such layers are good adhesion, thickness uniformity and step coverage with constant film composition and no material aggregation or accumulation [5,6]. MOS processing utilises CVD for the deposition of silicon nitride, polysilicon, silicon dioxide (for insulating layers) and some metals. The chemical vapour deposition systems which are in use today are mostly of the low pressure, hot wall (LPCVD) or cold wall plasma assisted (PECVD) type. Atmospheric pressure CVD is no longer a method of choice due to comparatively low wafer throughput and poor layer thickness uniformity although some older processes still use this for depositing a SiO_2 overglaze [5].

A typical LPCVD system is shown in figure 2.3. The hot wall system consists of a three zone furnace with quartz tube and wafer holders. Reactant gases are pumped along the tube at pressures between 30 to $250Pa$ at temperatures ranging from 300-900°C.

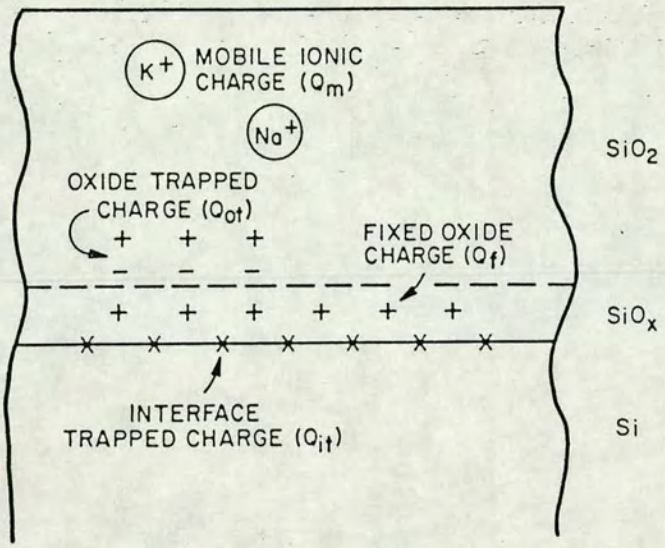


Figure 2.2. Charges in thermally oxidised silicon. After [3].

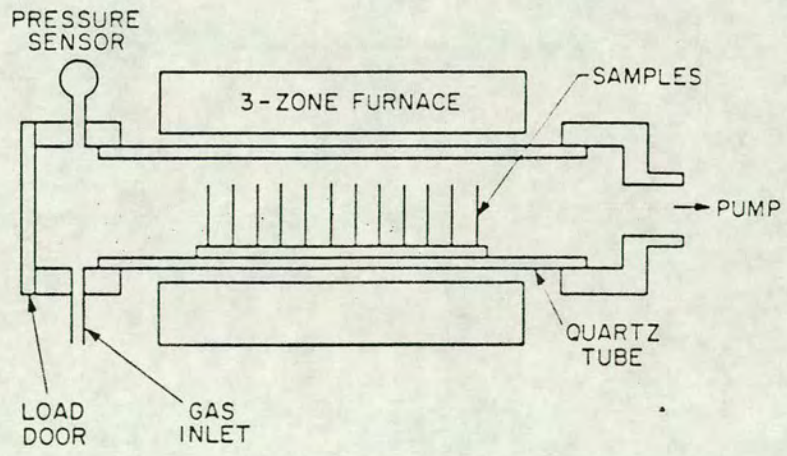


Figure 2.3. Schematic of hot-wall LPCVD reactor. After [5].

LPCVD systems are capable of taking large multi-batch loads and give layer uniformities of $\pm 5\%$ [5].

Polysilicon is formed in an LPCVD tube by pyrolisis of SiH_4 between 600 and 650°C. It is used as the gate electrode in MOS devices and in its undoped state as a high value resistor in SRAMs. It is used for interconnect although doped polysilicon has a higher sheet resistivity than metal interconnect. In its function as interconnect it is normally highly (n^+) doped with phosphorus. Various methods of introducing dopants into polysilicon can be used. Lowest track resistances may be obtained by diffusion doping although the high temperature drive in may not be compatible with VLSI processing. Implantation with subsequent transient anneal is one potential solution to this problem [5].

LPCVD is used to produce silicon nitride (Si_3N_4) by the reaction of silane and ammonia at 700-900°C. Silicon nitride is used as an oxidation mask to define active areas in LOCOS structures but as it is a good barrier to both oxygen and water diffusion these properties also make it a useful material for use as a passivation material. In this application the silane/ammonia reaction occurs at too high a temperature for a final passivation layer so plasma enhanced deposition (PECVD) of silicon nitride must be used. At temperatures of around 300°C, the plasma discharge gives energy for the dissociation of the feed gases into radicals which combine on the heated wafer substrate to form silicon nitride. PECVD can also be used for SiO_2, Al_2O_3, polysilicon and silicon carbide deposition [5].

Deposited silicon dioxide can fulfill a number of roles. In an undoped form it can be used as an insulating layer between conducting layers, an implant or diffusion mask or a capping layer to prevent outdiffusion from doped layers during high temperature steps. Doped silicon dioxide is used as an insulator between metal layers, as a diffusion source and as a final passivation layer. Both phosphorus and boron can be used in this role, although the former is more common. The phosphorus is formed by reacting phosphine with oxygen and is deposited simultaneously with the SiO_2. Concentrations of up to 8% phosphorus are used in this application and a high temperature reflow step used to improve step coverage (a potential reliability hazard) into contact holes. The reaction used to form SiO_2 for insulation between metallisation layers and for device passivation, (where low temperature deposition is necessary) involves reacting silane with oxygen, below 500°C. Better step coverage and uniformity can be achieved at higher temperatures. where two

possible reactions are the decomposition of tetraethyl orthosilicate (TEOS), at around $700°C$, and the reaction of dichlorosilane and nitrous oxide at approximately $900°C$ [5].

Silicide formation through deposition of refactory metals such as tungsten (W), molybdenum (Mo), tantalium (Ta) and titanium (Ti) may also be achieved by CVD. The use of silicide as a gate and interconnect material is becoming more important as VLSI circuits require to minimise their RC delay time [5].

2.3.3. Measurement of Layer Thickness and Quality

Layer thicknesses can be measured by interference techniques or ellipsometers. These are used routinely in a production situation with test or product wafers being used. The ellipsometer can also be used to determine layer refractive index. If the layer under test has undergone a subsequent etch stage then layer thickness can also be measured by using stylus profiling equipment. Test wafers are preferred for this as the stylus method could potentially damage the wafer. In addition to monitoring the thickness of polysilicon its sheet resistivity is also of importance and may be measured in-line by the four-point probe method or by using a specially laid out electrical test structure: the Greek cross [7-9]. Measurement and control of layer thickness and quality are crucial for gate oxide growth. Electrical measurements of this oxide are centered on capacitance-voltage measurements from which a number of parameters (mainly oxide related) can be derived [10-13]. Table 2.1 gives some of the parameters which can be derived from these measurements; for example oxide thickness, substrate doping, threshold voltage, flat-band voltage and concentration of both surface charge and mobile ions [14]. C-V measurement is comparatively slow, requires expensive, specialised equipment and is not suited for testing and wafer mapping of a large numbers of sites. An electrical test structure to measure oxide quality which does not require C-V measurement has been devised which quantifies oxide integrity by measuring pinholes in grown oxides [15].

2.4. Dopant Introduction

2.4.1. Diffusion

The property of impurity diffusion is used to form transistor source and drain regions, dope polysilicon and wells in MOS technology. These dopant atoms can be introduced in a

Technique	Calculated Parameters
Low frequency (quasistatic)	Oxide thickness Threshold voltage
High Frequency	Oxide thickness Threshold voltage Flatband capacitance Flatband voltage Substrate impurity concentration Doping profile Q_{ss}
High frequency (high-low temperature)	Mobile ions Traps Activation energy Capture cross section concentration Interface states
C-t	Effective minority carrier generation lifetime Surface generation velocity

Table 2.1. Some C-V measurement techniques and the parameters which may be evaluated.

number of ways including solid, liquid or gaseous sources, doped oxide layers and ion implantation, although the latter is now the most common method as it gives very precise control over junction depths and total dosage. Once implanted though, redistribution of layers will occur by diffusion at any further high temperature steps including any anneal used to electrically activate an implant.

Diffusion takes place at elevated temperatures, normally in excess of $900°C$, in furnace tubes which have similar specifications to those for oxidation and LPCVD, i.e. temperature control of $\pm 0.5°C$ in a three zone furnace with quartz liners, boats and pushrods.

Mathematically one dimensional flow of impurities can be described by Fick's simple diffusion equation [16,17],

$$\frac{\partial C(x,t)}{\partial t} = D\frac{\partial^2 C(x,t)}{\partial x^2} \tag{2.5}$$

where C, the impurity concentration (a function of position (x) and time (t)), is in units of $atoms\ cm^{-3}$ and D, the diffusion coefficient (assumed constant), is in units of cm^2h^{-1} or μm^2h^{-1}. This equation has been solved for various commonly found practical situations, such as constant surface concentration and constant total dopant [16]. The equation can

also be solved in an iterative fashion by process simulators for more complex situations. Equation 2.5 is a simplified representation of diffusion and several factors have not been considered. One such factor is concentration dependent diffusion which causes deviations at high concentrations from profiles predicted by equation 2.5. This necessitates the use of a concentration dependent diffusion coefficient for model purposes [16]. The diffusion coefficient is also a function of temperature and can be similarly modelled [16]. Enhancement of the rate of diffusion also occurs when silicon is being oxidised for which rate enhancement coefficients of 1.8 for dry and 3.3 for wet oxidation have been found [16].

2.4.2. Ion Implantation

Furnace based dopant introduction systems (e.g. solid source) give little control over the form of the impurity distribution and doping concentrations tend to be high ($10^{17}-10^{22}cm^{-3}$) making the shallow junctions required for VLSI difficult to produce [18]. Ion implantation gives accurate dopant profiles and easily produces shallow junctions with concentrations of dopants in the range 10^{14} to $10^{18}cm^{-3}$, thus is now the main method of introducing dopant into silicon [19]. Further advantages of implantation include small lateral dopant spread, low temperature wafer processing and a high purity of the implanted species. From a practical point of view several materials such as photoresist, silicon dioxide, nitrides and polysilicon can all be used as implant masks. Disadvantages of implantation are principally concerned with the cost, complexity and reliability of the equipment.

A generalised diagram of an ion implanter system is given in figure 2.4. The ion source contains the appropriate implant material. Solid sources are used due to the volatility and toxicity of other sources. Feed gases are produced from these solid sources by vapourisation at high temperatures. Common feed gases are BF_3 for boron, PF_3 for phosphorus and AsF_3 for arsenic. Ions are produced by forming a plasma of the feed gas from which the ion species of interest is then selected by an analyser magnet and then accelerated to the target chamber via a beam tube. In essence it is very similar to the action of a mass spectrograph. Low and medium current implanters commonly use an electrostatic scan system and employ a load lock system which allows single wafer processing. For high current implanters wafer heating becomes a problem and batch systems with large target chambers and physical scanning of some form are necessary.

Numerous models exist to describe the ion distribution profile in silicon after implantation [18,19], the simplest description of which is a Gaussian with the impurity concentration ($n(x)$) as a function of position given as,

$$n(x) = n(R_p) \cdot \exp\left[-\frac{(x - R_p)^2}{2\Delta R_p^2}\right] \tag{2.6}$$

where the peak concentration is at $x = R_p$ and ΔR_p is the standard deviation or 'straggle' of the distribution. Integrating over all x will give the total ion dose (ϕ) from which the maximum concentration can be approximated,

$$n(R_p) = \frac{\phi}{\sqrt{2\pi}\Delta R_p} \approx 0.4\frac{\phi}{\Delta R_p} \tag{2.7}$$

More accurate models exist. One of these, the double Gaussian, models the 'skewness' which is observed in practice. This model matches two Gaussians with the same peak concentration but different ΔR_p. A 'four-moment' approach known as the Pearson IV model gives further accuracy and ascribes four parameters to the distribution. First and second moments are the range (R_p) and straggle (ΔR_p). The third moment is a measure of the distribution skewness (γ) and measures the distribution asymmetry; a positive value for this parameter putting the distribution peak nearer the surface than R_p. The fourth moment describes how flat the top of the distribution is and is known as the kurtosis (β).

After implantation it is necessary to electrically activate the implanted species by thermally annealing the wafers. This places implanted ions into the silicon lattice and also repairs some of the lattice damage. Annealing has the undesirable side effect of causing diffusion of the implanted species which for VLSI circuits may be a problem as this results in an undesirable increase in source/drain junction depths. Reducing the annealing time alleviates this problem hence the use of rapid thermal annealing (RTA) involving the rapid heating of the silicon which keeps diffusion to a minimum. RTA can be accomplished by use of electron or ion beam, lasers or high intensity lamps.

2.4.3. Junction Depth and Profile Analysis

Dopant introduction and control of subsequent diffusion is essential for device operation. Diffusion may occur as either a deliberately introduced step (e.g. CMOS well production) or as a side effect of a high temperature processing step (e.g. annealing). Diffusion affects device operation as lateral diffusion of dopant from source and drain

regions shortens the effective length of a transistor from its drawn length (L_d). Measurement of lateral diffusion (L_{del}) can be achieved either by physical cross section of the device followed by chemical stain and SEM inspection or derived electrically. The latter requires a minimum of two transistors each with the same drawn gate width. A plot of L_d against $1/\beta$ (where β is the device transconductance) yields a straight line graph whose X axis intercept is $2L_{del}$.

Junction depth measurements can be made in a number of ways [20]. Bevel and stain in conjunction with interferometry measurements can attain an accuracy of $\pm 0.05 \mu m$. Other common methods include the groove and stain method [21]. The measurement of sheet resistance can be used to derive junction depth since it is related to the junction depth and the impurity distribution. This relation has been calculated for different impurity distributions (Gaussian, erfc) and are known as Irvins' curves [16].

Profile measurements rather than simple depth measurements are required in many situations. A simple electrical technique for this exists which requires only a four terminal MOSFET as outlined by Buehler [22]. Examples of the many other possible profiling techniques are C-V measurements [10,11,16], spreading resistance [12,16], secondary ion mass spectroscopy (SIMS) [16,23] and Rutherford backscattering spectroscopy (RBS) [23].

2.5. Layer Definition and Patterning

2.5.1. Lithography

Lithography is the transfer of geometric shapes onto the surface of the silicon wafer. In current production practice photolithography at UV wavelengths is the dominant method of achieving this with X-ray and electron beam lithography being mostly limited to the research environment. The transfer of pattern information to the wafer requires the use of a photomask ('mask') or reticle, a lithography tool to transfer the pattern from mask to wafer and the use of a photo-sensitive material to delineate that pattern on the wafer. The transfer procedure is achieved by firstly covering the silicon wafer in a photo-sensitive layer of a complex polymer (known as photoresist). A positive photoresist when exposed to UV light and developed has the exposed regions removed whereas a negative resist does the opposite of this with non-exposed regions removed after exposure. The areas not covered with photoresist are subject to the relevant processing step before the resist is stripped and

the cycle repeated. Immediately after spinning on the resist the wafers are 'soft baked', the increased temperature driving off the resist solvent and promoting adhesion of the resist to the underlying layer. A post exposure 'hard bake' at a temperature just below the resist flow point ensures the adhesion and stability of the remaining photoresist for further processing [24]. This sequence is illustrated by figure 2.5.

For whole wafer systems (contact, proximity and projection printing) maskmaking follows the route shown in figure 2.6. Design data information, typically from a CAD system, is fed to a pattern generator (after conversion to a suitable format such as David Mann) which converts the design into a photographic plate known as a reticle. This reticle is produced larger than the 'on silicon' die size (10× or 4× for example). Electron-beam machines are used for reticle production (or direct production of a mask) because throughput is not such a significant consideration when maskmaking. The reticle is then stepped across another photo-plate to make what will become the master copy of a whole wafer mask for that layer of the design. Working masks are made by contact prints of this master copy. Silicon patterning using step and repeat cameras works directly from a reticle thereby eliminating the the need to produce whole wafer masks from the above procedure.

Photolithography tools can be split into three categories of equipment - contact, proximity and projection printing, but, for any lithography tool, the three key parameters are,

(1) resolution - minimum feature size that can be developed in resist.

(2) registration - how closely a mask can be accurately aligned to previous layers.

(3) wafer throughput - the number of wafer exposures per hour.

Contact printing was originally the most popular lithography method in use due to the low cost of machinery and high throughput compared with other methods [25]. It has the advantage that the optical contrast is close to 100% so that any pattern on a mask can be printed onto the wafer. The main disadvantage of this method is that direct contact is required between wafer and mask giving rise to mask damage due to silicon dust caught between wafer and mask. This causes subsequent wafers to be printed with the now damaged mask causing a drop in yield. Although this is not of significance for circuits of small area it is for VLSI circuits. Yield equations can be used to show that contact printing is best used for small die with large dimensions [25].

Proximity printing reduces mask damage by maintaining a small air gap between mask and wafer although there is a loss of resolution due to diffraction effects. Proximity

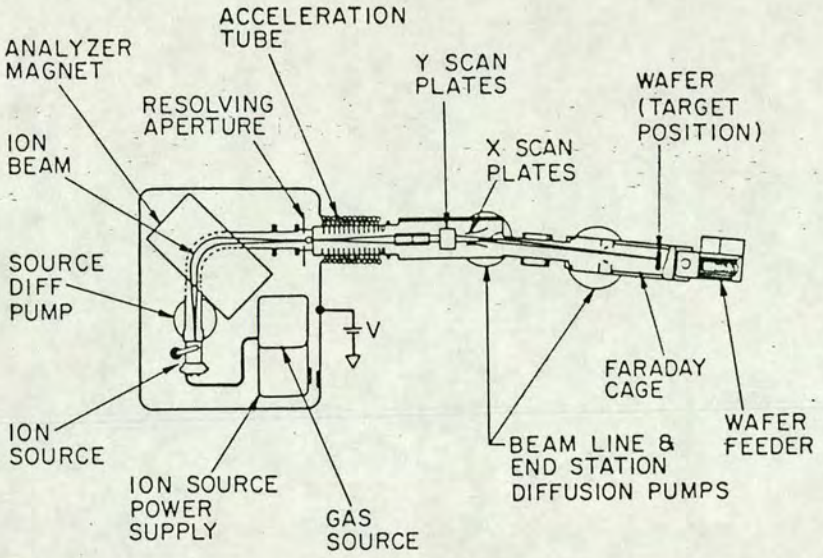


Figure 2.4. Schematic of a typical ion implanter. After [19].

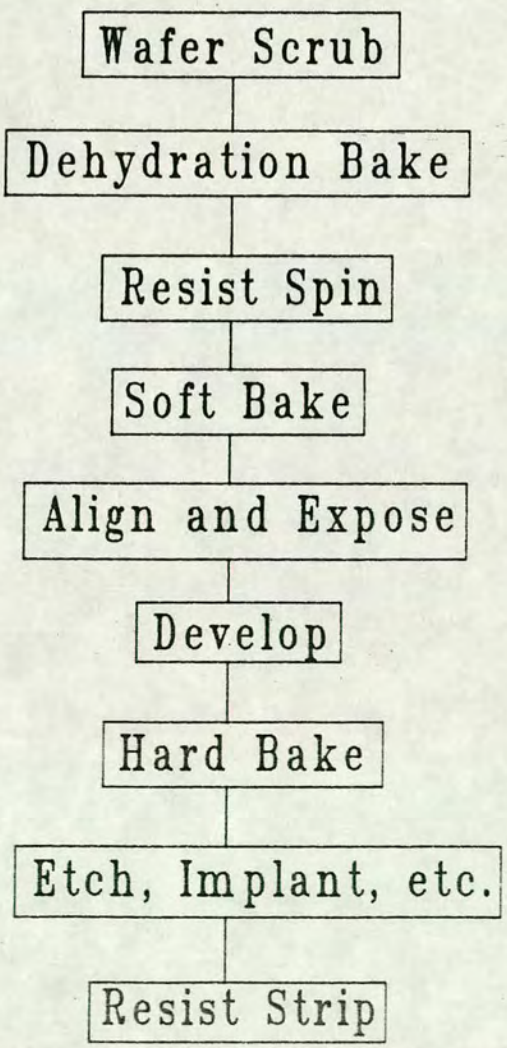


Figure 2.5. Route of wafer through photolithography.

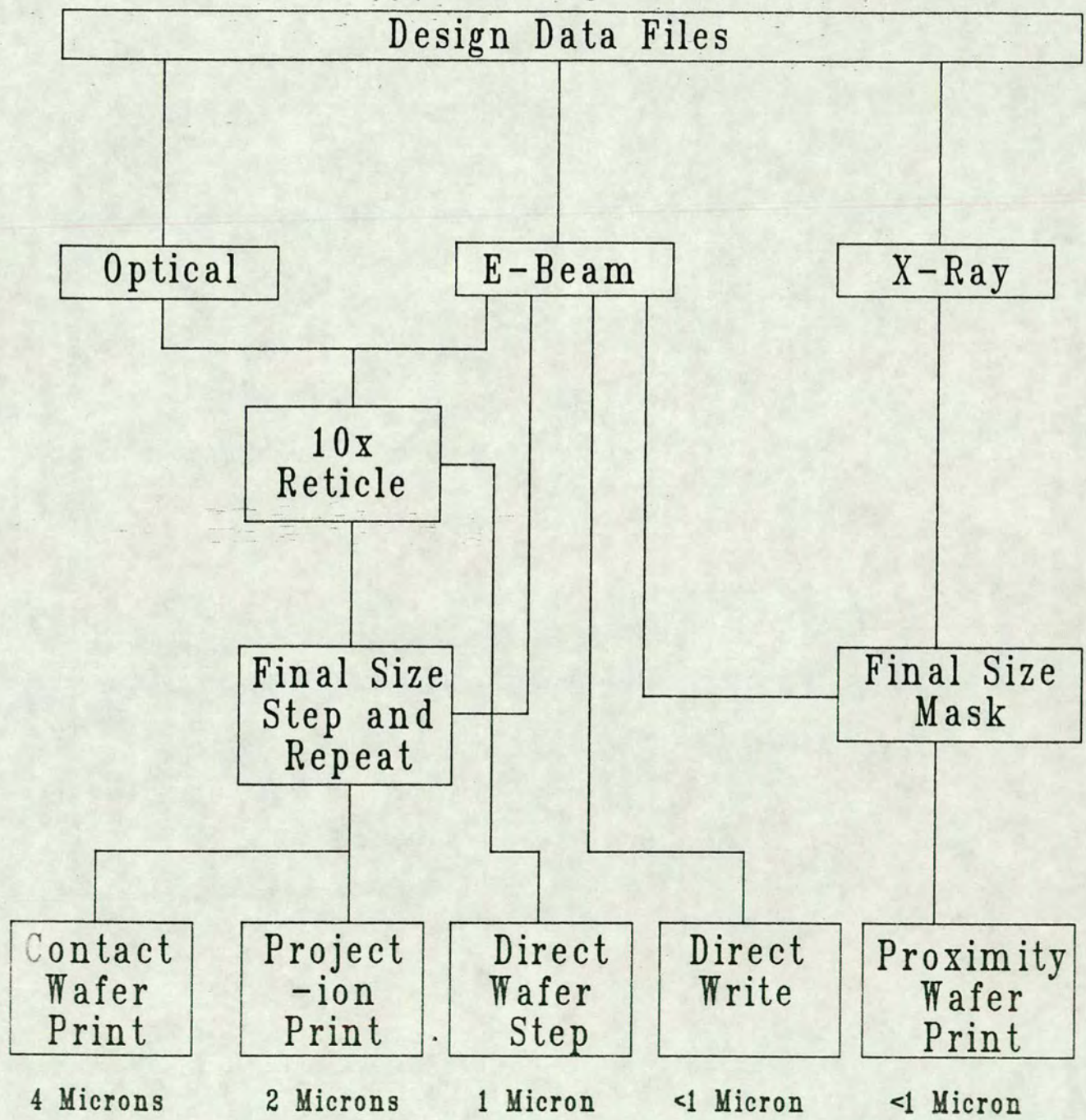


Figure 2.6. Possible routes from wafer design to exposure.

printing is limited by both the wafer and mask flatness. So for effective dimensional control it is necessary to use larger wafer to mask gaps (15 - 20μm) [25].

Projection printing tools fall into two categories; whole wafer (1:1 printing) and direct step and repeat systems. Both rely on optical projection of the mask (the object plane) onto a wafer (the image plane) therefore circumventing the problems of proximity printing.

Projection aligners use whole wafer masks with the wafer and mask held in different planes. The mask pattern is cast onto the wafer by a series of mirrors and lenses. System complexities mean that when the wafer is exposed to UV a curved section is scanned across the wafer. Projection aligners have better resolution than proximity printing and none of the yield problems of contact printers with mask lifetime being potentially infinite [25]. Mask lifetime can be aided by use of a pellicle, a thin transparent film, added a few millimetres off the patterned surface of the mask so that dust particles will not be focused on the wafer surface.

Step and repeat systems ('steppers') use a reticle with the pattern for a single or small number of die on it which is projected via the system optics onto the wafer. Reticles are made at 1×, 5× or 10× final size depending on stepper type. As with whole wafer printing mask life is potentially infinite as no wafer to die contact is made. Advantages over projection printing can be summarised as follows [25],

(1) Resolution of the image is superior.

(2) Mask defects are reduced due to demagnification (1× steppers trade this off with increased throughput).

(3) Fine control of CDs is possible.

(4) Reduction of misalignment and runout between mask and wafer (due to distortion during processing) as only a small area of the wafer is exposed at one time and alignment and focus can be corrected at each site.

Drawbacks to stepper systems include low throughput when compared with whole wafer systems and higher cost and complexity of machinery. For small geometry processes steppers are essential if realistic yield levels are to be achieved.

The benefits and drawbacks of the various lithographic tools discussed are summarised in table 2.2.

	Wafer Stepper 10×	Projection 1:1	Proximity	Contact
Resolution	1.0μm	2-3μm	3-5μm	1.0μm
Alignment (2σ)	$\pm$0.14μm	$\pm$0.7μm	$\pm$1.0μm	$\pm$1.0μm
Overlay (2σ)	$\pm$0.3μm	$\pm$1.2μm	$\pm$1.5μm	$\pm$1.5μm
Throughput (75mm)	10-40w/hr	60w/hr	100w/hr	100w/hr
Mask Induced Defects (Hard)	0	$3in^{-2}$	$10in^{-2}$	
Sensitivity to Soft Defects	5μm	0.5μm	0.5μm	0.5μm
CD on SiO_2 (Perfect Mask)	$\pm$0.1μm	$\pm$0.25μm	$\pm$0.5μm	$\pm$0.25μm
CD on SiO_2 (Mask Induced)	0	$\pm$0.25μm	$\pm$0.5μm	$\pm$0.5μm
Yield	Best	Fair	Poor	Worst
Mask Life	Infinite	Infinite	$\ll$Infinite	Short
Mask Cleaning	*Infrequent*	3-4*hours*	2*hours*	10*exposures*
Wafer Size Capability	50-125mm	75-100mm	75-100mm	50-100mm
Price (1982)	650K$	300K$	50K$	50K$

Table 2.2. Lithography comparisons. After [25].

Advanced lithographic tools such as electron beam and X-ray lithography both offer several potential advantages over photolithography, but at present economic constraints have mainly limited their use to research and development facilities.

2.5.2. Etching

Etching is that part of the semiconductor process where layers of material are removed by various means to define either masked areas for implant/diffusion or circuit areas in metal/polysilicon. The masking is formed using a resist mask by the photolithography process and removal of the unmasked area is achieved by the chosen etch method. Two methods of etching are in common use, wet and dry etching. The latter is by far the most prevalent process used as wet etching is incompatible with VLSI processing needs.

Three parameters can define any etch process and these are selectivity, anisotropy and uniformity and are defined as follows [26],

$$Selectivity\ (S) = \frac{E_f}{E_s} \tag{2.8}$$

where E_f is the film etch rate and E_s the substrate etch rate. The substrate layer is defined as the layer underneath the one being etched,

$$Anisotropy\ (A) = \frac{vertical\ etch\ rate}{lateral\ etch\ rate} \tag{2.9}$$

$$Uniformity\ (U) = \frac{Max. - Min.}{Max. + Min.} \tag{2.10}$$

Max. and *Min.* can refer to either the etch rate or the film thickness depending on which is being measured.

Wet etching is normally a batch process, and requires exposure of the wafers in the etchant (hydrofluoric acid for example) for the appropriate time. Wet etching is normally isotropic (vertical etch rate = lateral etch rate ; $A = 1$). Figure 2.7a) illustrates the isotropic with figure 2.7b) the anisotropic case ($A = \infty$). However some silicon etches have different etch rates for different crystallographic planes, giving the ability for trench like structures to be created. Wet etch processes have the advantages of low cost, as only relatively cheap chemicals are required and associated equipment is simple to operate and maintain. Control parameters are few (concentration of etchant, temperature of etch, agitation and time) and as a batch process throughput is high. Its disadvantage is the inherently isotropic nature of the process so for VLSI, where narrow linewidths and small pitch lines and spaces are required, it is no longer viable [26].

Dry etching is now the predominant technology for VLSI. The use of the term 'dry etching' has become synonymous with that of 'plasma assisted etching' in which the formation of an ionised gas above a wafer, in a sealed chamber etches layers either by physical or chemical means or some combination of both depending on the configuration of the electrodes, gas composition and other system variables. This process has the very important advantages of good resolution and linewidth control. This is despite the capital cost, complexity and maintenance costs of the machinery, high energy damage to the wafer, the use of hazardous gases and the high number of etch control parameters many of which are not fully understood.

Plasmas used for etching in the semiconductor process are AC plasmas with the most normal applied frequency being $13.56MHz$. The potential distribution within the plasma, shown by figure 2.8, is such that both electrodes are negative relative to the plasma [27, 28]. The extra voltage on the powered electrode is due to the blocking capacitor in the RF feed and the area difference between electrodes. This potential distribution gives rise to two possible system configurations. By placing wafers on the grounded electrode, chemical etching will predominate, with the plasma acting as a source of reactive ion species.

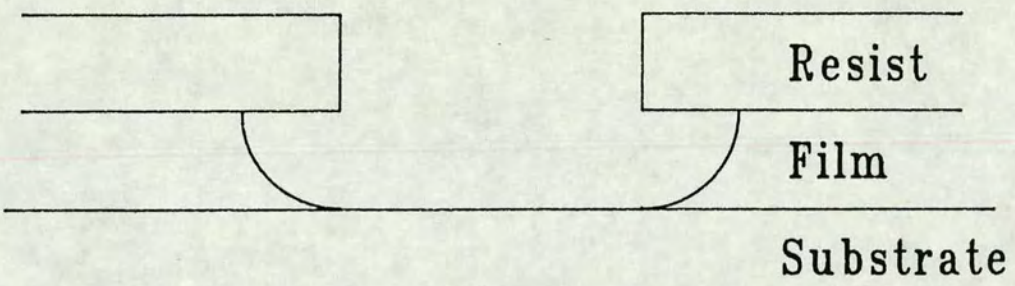


Figure 2.7.a) Isotropic etch (A=1).

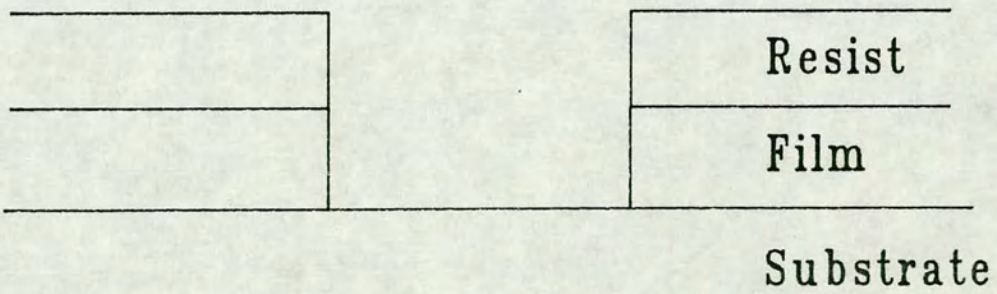


Figure 2.7.b) Anisotropic etch (A=∞).

Alternatively by putting wafers on the powered electrode a high degree of physical etching can be achieved with ions being accelerated across the potential difference over the ion sheath next to the electrode before impacting on the wafer. By altering the plasma potential relative to the wafers various ratios of chemical to physical etching can be achieved.

These physical plasma properties are employed in two different types of plasma etchers. The barrel etcher is used with an oxygen plasma to strip resist and relies on a mostly chemical etch. The planar etcher is used for layer (polysilicon, SiO_2, Si_3N_4 and metal) etching and normally relies on a large physical etch component. Both types of etcher can operate in either batch or single wafer mode with the trend being towards the latter and incorporating cassette to cassette operation for fully automated processing.

2.5.3. Lithography and Etch Control

The critical lithographic parameter which must be monitored is layer to layer registration. This can be measured using both optical and electrical measurement structures. Optical structures range from the simple optical vernier which must be measured by an operator to fully automated systems which work by image analysis of specifically designed patterns on the wafer [29]. Advances on this technique using electron beam sensitive structures for evaluating this parameter are also being investigated [30, 31]. Optical systems can measure photoresist layers which electrically systems cannot achieve but unfortunately are more difficult and expensive to automate. Electrical structures can measure layer to layer registration and a number of structures have been devised to measure this, most notably those used by Buehler [32] and Perloff [33, 34]. These are both based on analogue sheet resistance measurements and recent interest has moved to the use of digital structures for small geometry processes. Lithography tools can also be evaluated using these control structures [35]. For example linewidth uniformity can be a function of the lithography tool in use due to variations in the photomask or projection optics [36].

Measurement of physical etching parameters such as anisotropy and selectivity can best be determined by detailed examination of the silicon wafer, such as in cross section under an SEM. These properties should be relatively stable as they are based on the physical properties of the materials and not primarily dependent on the processing parameters. When etching layers it is essential that a small amount of overetch be allowed

to ensure that all lines clear due to layer thickness variations and topography considerations. 'Snake' structures such as comb resistors can be used to check whether etching can clear lines between parallel conductors [37, 38]. These lines can either be flat or over some topographical step. By having a series of test structures with varying pitch between the conductors a given etch process can be evaluated and minimum design rules devised [39]. Linewidths and etch quality and routinely checked in-line by use of CD (Critical Dimension) structures. CDs for each mask layer are normally placed on each die. These are normally a set of lines of differing widths which are measured by optical inspection, for each layer. Comparison of the mask with the measured CD dimensions gives etch information. A number of sites per wafer and wafers per batch are monitored this way in a production environment. Overetch can be measured electrically in conducting layers using the cross-bridge structure and has been used to characterise variations in etch processes [40, 41].

2.6. Metallisation

The interconnection of devices must fulfill a number of criteria such as low resistance, simple deposition, ohmic contact with silicon and simple pattern definition. Aluminium fits these properties and is widely used although more 'exotic' metals and mixtures such as silicides are becoming more common. Metallisation can potentially take up an area on a chip larger than the devices themselves so with increasing chip size, schemes utilising double and triple layers of metal interconnect have become necessary. This has increased the necessity of accurate control of the metallisation process to eliminate problems such as hillocks, step coverage and junction spiking.

Metal can be deposited by a number of different methods such as evaporation, sputtering, magnetron sputtering or LPCVD. Of these methods the latter two are the most relevant for present day processing requirements. Sputtering relies on the physical process of sputter etching. A low pressure gas (argon is the most common choice) is ionised by the application of a high voltage. The net result of this is that ionised argon atoms are accelerated towards the metal target. Momentum transfer ejects metal ions from the target towards the wafer where a metal film is formed. As this is a very slow process, magnetron sputtering is used to speed it up. This involves the ionised gas being contained by a magnetic field, increasing the plasma density and consequently the metal deposition rate [42]. Metal deposition by LPCVD has the advantage over the previously described

methods as step coverage is conformal with no shadowing effects. At present applications of this method have been limited mainly to silicide deposition.

Good metal step coverage is important because metal thinning, as depicted by figure 2.9, can occur encouraging electromigration effects. Many factors affect step coverage but deposition technique, substrate motion and source geometry are considered the first order effects [43]. Optimisation of source wafer geometry as well as substrate heating to increase film mobility during deposition are two solutions to improve coverage, the latter reducing the possibility of cracks in the metal in corner regions. Problems still exist if small geometry contact holes are to be filled. The steep vertical walls of these give a geometry such that the potential for poor step coverage exists. The option of a high temperature reflow of the underlying phosphorus doped silicon dioxide to give shallower sidewalls cannot be tolerated in a VLSI process while taper etching of the contact holes can take up too much area. In practice these problems are likely be overcome by a compromise between coverage and side wall slope.

Hillocks as their name implies are protrusions of metal above the normal metal film height. They are formed to relieve mechanical stress in the metal layer and are a reliability hazard for two reasons. Firstly hillock formation can leave associated voids which could cause open circuits. Secondly they cause problems with subsequent coverage by a dielectric layer, possibly causing metal to metal shorts for a multi-layer metal process or an ingress for contaminants if the dielectric forms the final passivation layer. Suppression of hillock growth can be achieved with low levels of an alloying compound in the metal film such as copper at 0.5% [42].

Electromigration in metal layers is characterised by the material transport of the layer due to the momentum transfer from the electrons moving in an electric field to the positive metal ions [43]. The effect is dependent on the current density in the metal track, with densities of $10^9 - 10^{10} Am^{-2}$ being sufficient for momentum transfer to take place. The degree to which electromigration occurs is measured by determining the lifetime of conductor lines when current is being passed through them. Equation 2.11 expresses the median time to failure (MTF) (time for 50% of the tracks to fail) [43],

$$MTF = \frac{constant}{J^2} \cdot \exp\left(\frac{E_a}{kT}\right) \qquad (2.11)$$

where J is the current density, E_a is the activation energy and T the temperature in

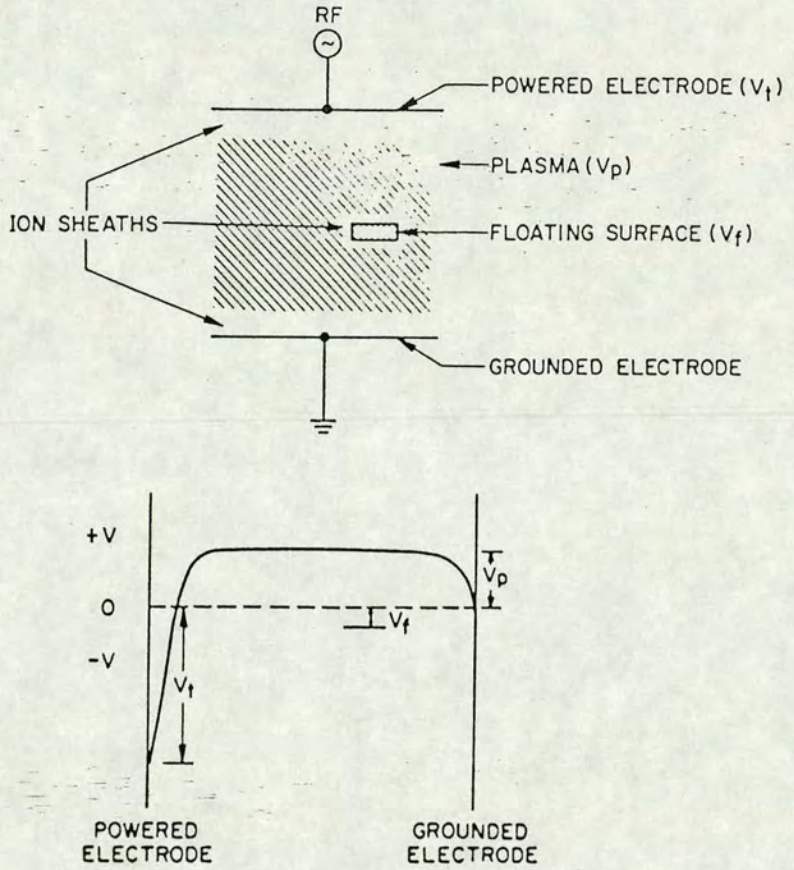


Figure 2.8. Schematic of potential distribution in plasma. After [28].

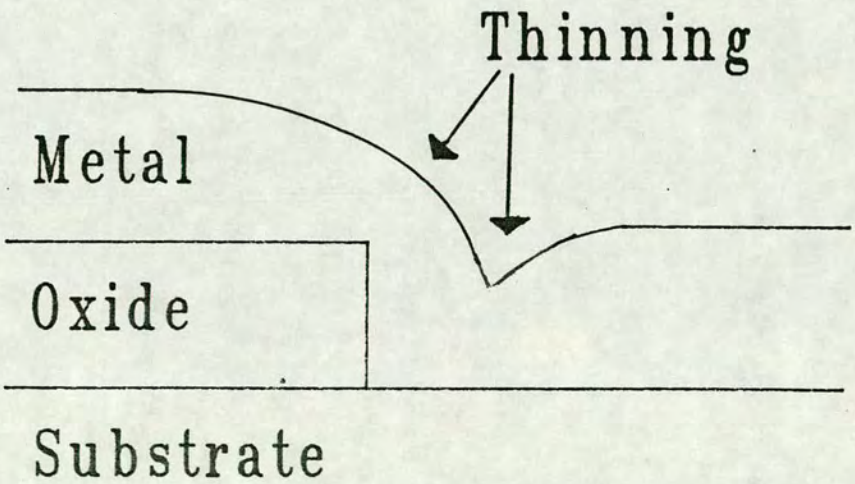


Figure 2.9. Cross-section showing metal thinning over oxide step.

Kelvin. The constant is material and current density dependent. Equation 2.11 is useful for accelerated life testing where high temperature and current densities are used to simulate extended operating periods under normal conditions. The MTF may be improved by the addition of small quantities of alloying elements (around 4% copper, for example), to prevent electromigration. The alloying material segregates at the grain boundaries reducing the aluminium mobility [44].

Junction spiking is a penetration of a p-n junction by a 'spike' of aluminium [43]. The cause of this is the diffusion of silicon into the aluminium during metallisation anneal and subsequent processing. The amount of dissolution is dependent on the temperature and the amount of aluminium available. Spiking becomes an increasing problem with VLSI circuits because of the shallow junctions used. One solution to this problem is the use of a proportion of silicon in the aluminium while another is to use silicides as diffusion barriers at contacts [44].

Metallisation is the most critical step of the silicon fabrication process both in processing and long term reliability terms. The quality of the metallisation can measured in many ways. Step coverage can be evaluated by yield structures such as serpentine resistors [37,38]. Here the number of step 'failures' per number of steps can give a prediction of device yield. Comb resistors may be used to evaluate the metal etch process while contact chains may give a measure of contact resistance and contact step coverage.

2.7. Summary

The MOS silicon process details have been presented briefly in this chapter and the means of controlling each of these steps has been illustrated. Detailed process monitoring requires both the use of in-line structures and measurements and end of line derived information. Some parameters are more easily derived by non-electrical means, for example film thickness, and in general these can be conducted by in-line measurements. As well as being able to monitor purely electrical parameters parametric test structures can, by use of specialised structures, also monitor physical process parameters. Electrical testing, although requiring specialised test structures has the advantage that large numbers of structures can be accessed in a short time span. This enables the measured parameter to be mapped across both a wafer and across a complete batch if required. Trends which would not be apparent from other forms of testing can be monitored. Parametric testing forms a

complementary part to in-line testing in the monitoring of the fabrication process.

References

1. C.W. Pearce, "Crystal Growth and Wafer Preparation," in *VLSI Technology*, ed. S.M. Sze, McGraw-Hill. 1st Edition
2. B.E. Deal and A.S. Grove, "General Relationship for the Thermal Oxidation of Silicon," *J. Appl. Phys.*, vol. 36, p. 3770, 1965.
3. L.E. Katz, "Oxidation," in *VLSI Technology*, ed. S.M. Sze, McGraw-Hill. 1st Edition
4. A.M. Gundlach, "Oxidation," in *SERC School on Microfabrication 1985*, University of Edinburgh, Dept. of Elec. Eng., April 1985.
5. A.C. Adams, "Dielectric and Polysilicon Film Deposition," in *VLSI Technology*, ed. S.M. Sze, McGraw-Hill. 1st Edition
6. R. Holwill, "CVD," in *SERC School on Microfabrication 1985*, University of Edinburgh, Dept. of Elec. Eng., April 1985.
7. L.J. van der Pauw, "A Method of Measuring the Resistivity and Hall Coefficient on Lamellae of Arbitrary Shape," *Philips Technical Review*, vol. 20, no. 8, pp. 220-224, 1958/59.
8. L.J. van der Pauw, "A Method of Measuring Specific Resistivity and Hall Effect of Discs of Arbitrary Shape," *Philips Research Reports*, vol. 13, no. 1, pp. 1-9, February 1958.
9. M.G. Buehler and W.R. Thurber, "An Experimental Study of Various Cross Sheet Resistor Test Structures," *J. Electrochem. Soc.*, vol. 125, no. 4, pp. 645-650, April 1978.
10. K.H. Zaininger and F.P. Weiman, "The C-V Technique as an Analytical Tool: Part 1," *Solid State Technology*, pp. 49-56, May 1970.
11. K.H. Zaininger and F.P. Weiman, "The C-V Technique as an Analytical Tool: Part 2," *Solid State Technology*, pp. 46-55, June 1970.
12. U. Kaempf, "Automated Parametric Testers to Monitor the Integrated Circuit Process," *Solid State Technology*, pp. 81-87, September 1981.

13. J.M. Robertson, "C-V," in *SERC School on Microfabrication 1985*, University of Edinburgh, Dept. of Elec. Eng., April 1985.

14. I. McGillvary, *PhD Thesis,* Edinburgh University, 1986.

15. M.G. Buehler, B.R. Blaes, C.A. Pina, and T.W. Griswold, "Pinhole Array Capacitor for Oxide Integrity Analysis," *Solid State Technology*, pp. 131-137, November 1983.

16. J.C.C. Tsai, "Diffusion," in *VLSI Technology*, ed. S.M. Sze, McGraw-Hill. 1st Edition

17. R. Holwill, "Diffusion," in *SERC School on Microfabrication 1985*, University of Edinburgh, Dept. of Elec. Eng., April 1985.

18. R. Holwill, "Implantation," in *SERC School on Microfabrication 1985*, University of Edinburgh, Dept. of Elec. Eng., April 1985.

19. T.E. Seidel, "Ion Implantation," in *VLSI Technology*, ed. S.M. Sze, McGraw-Hill. 1st Edition

20. C.A. Aley and R.S. Turner, "Junction Depth Measuring Methods: The Pros and Cons," *Semiconductor International*, May 1980.

21. B. McDonald and A. Goetzberger, "Measurement of the Depth of Diffused Layers in Silicon by the Grooving Method," *J. Electrochem. Soc.*, vol. 109, no. 2, pp. 141-144, February 1962.

22. M.G. Buehler, "Dopant Profiles Determined from Enhancement-mode MOSFET dc Measurements," *Appl. Phys. Lett.*, vol. 31, no. 12, pp. 848-850, December 1977.

23. R.B. Marcus, "Diagnostic Techniques," in *VLSI Technology*, ed. S.M. Sze, McGraw-Hill. 1st Edition

24. J.T.M. Stevenson, "Resists," in *SERC School on Microfabrication 1985*, University of Edinburgh, Dept. of Elec. Eng., April 1985.

25. J.T.M. Stevenson, "Lithography," in *SERC School on Microfabrication 1985*, University of Edinburgh, Dept. of Elec. Eng., April 1985.

26. A. Belka, "Etching," in *SERC School on Microfabrication 1985*, University of Edinburgh, Dept. of Elec. Eng., April 1985.

27. J.L. Vossen, "Glow Discharge Phenomena in Plasma Etching and Plasma Deposition," *J. Electrochem. Soc.*, vol. 126, no. 2, pp. 319-324, February 1979.

28. C.J. Mogab, "Dry Etching," in *VLSI Technology*, ed. S.M. Sze, McGraw-Hill. 1st Edition

29. C. Murray, "Measurement Tools for Overlay Registration," *Semiconductor International*, pp. 62-68, February 1987.

30. K.L. Harris, S. Miyauchi, and T. Namae, "Applications of a High-speed, High-resolution Metrology System," *Microelectronic Manufacturing and Testing*, pp. 54-55, May 1987.

31. E.J. Sprogis, "An Overlay Vernier and Process Bias Monitor Measured by Voltage Contrast SEM," *Proc. of the 1989 International Conference on Microelectronic Test Structures (ICMTS)*, vol. 2, no. 1, pp. 129-132, Edinburgh, March 1989.

32. M.G. Buehler, "The Use of Electrical Test Structures Arrays for Integrated Circuit Process Evaluation," *J. Electrochem. Soc.*, vol. 127, no. 10, pp. 2284-2290, October 1980.

33. D.S. Perloff, "A Four-point Electrical Measurement Technique for Characterizing Mask Superposition Errors on Semiconductor Wafers," *IEEE Journal of Solid-State Circuits*, vol. SC-13, no. 4, pp. 436-444, August 1978.

34. D.S. Perloff, "A Van Der Pauw Resistor Structure for Determining Mask Superposition Errors on Semiconductor Slices," *Solid-State Electronics*, vol. 21, pp. 1013-1018, 1978.

35. T.F. Hasan, S.U. Katzman, and D.S. Perloff, "Automated Electrical Measurements of Registration Errors in Step-and-Repeat Optical Lithography Systems," *IEEE Trans. on Electron Devices*, vol. ED-27, no. 12, pp. 2304-2312, December 1980.

36. D. Yen, L.W. Linholm, and M.G. Buehler, "A Cross-bridge Test Structure for Evaluating the Linewidth Uniformity of an Integrated Circuit Lithography System," *J. Electrochem. Soc.*, vol. 129, no. 10, pp. 2313-2318, October 1982.

37. P. Gill and K. Dillenbeck, "Using Snake Patterns to Monitor Defects and Enhance VLSI Device Yields, Part One," *Microcontamination*, pp. 23-60, February 1989.

38. P. Gill and K. Dillenbeck, "Using Snake Patterns to Monitor Defects and Enhance VLSI Device Yields, Part Two," *Microcontamination*, pp. 33-60, March 1989.

39. M.G. Buehler, "Microelectronic Test Chips for VLSI Electronics," in *VLSI Electronics : Microstructure Science*, ed. G.B. Larrabee, vol. 6, pp. 529-576,

Academic Press, 1983. Chapter 9

40. R. Patrick and B. Arden, "Plasma Etch Characterization Using Electrical Linewidth Measuring Techniques," *SPIE*, vol. 775, Integrated Circuit Metrology, Inspection and Process Control, pp. 210-216, 1987.

41. R. Patrick and B. Arden, "Using Electrical Linewidth Metrology To Characterize Plasma Etching," *Microelectronic Manufacturing and Testing*, pp. 25-26, May 1987.

42. R. Holwill, "Metal Deposition," in *SERC School on Microfabrication 1985*, University of Edinburgh, Dept. of Elec. Eng., April 1985.

43. D.B. Fraser, "Metallization," in *VLSI Technology*, ed. S.M. Sze, McGraw-Hill. 1st Edition

44. F. Fantini and G. Soncini, "MOS Integrated Circuits Reliability," *Proc. of EMF International Vacation School on VLSI Fabrication*, Edinburgh, 2-13th April 1984.

Chapter 3

Parametric Testing: a Review of Structures, Testers and Methodology

3.1. Introduction

Parametric test is performed at the end of the fabrication process to confirm that engineering parameters are within specification. This test is performed on specially designed chips which are commonly referred to a process control chips (PCC), process monitor chips (PMC) or test chips, but which will have undergone all the same process steps as product devices. In the development of a new process wafers containing nothing but test chips are fabricated although in production it is more normal to replace small numbers of product chip sites with PCCs [1,2]. With the advent of wafer stepper technology it has become more common to locate the test structures in the scribe channel (or kerf area as it is sometimes otherwise known) [3]. This change was simply the result of throughput considerations since the use of devices in the scribe channel does not require the changing of stepper reticles which would be required for the more conventional 'drop-in'.

PCCs have been used in the semiconductor industry since its beginning in the early 1960's, but their role has now expanded from that of simple process characterisation to process control, equipment and operator performance evaluation and yield predictors. They can be used to help isolate yield problems which may be difficult or time consuming to determine from product circuits, or by other methods such as physical analysis. With the increasing complexity and processing cost of integrated circuits, parametric testing of PCCs can give an early indication of a yield problem. This can avoid the requirement for functional testing of bad batches, as well as helping locate the cause of the problem. The requirement for this in a production environment is chiefly financial since the full functional testing of devices at final test is both slow and expensive so it is desirable to optimise functional tester time [4].

Figure 3.1 shows how all process measurement information interacts with the control and improvement of the fabrication sequence. Although PCCs are a major source of information for process control they are complemented by other forms of information gathering chips. For example 'in process' measurements on test wafers and functional yield data help to give a complete picture of the process. Figure 3.2 illustrates this. From all these sources a data base can be built up over a period of time and used to help diagnose processing problems [5].

PCCs are consequently an important component in the quest to increase reliability and reduce the cost of the final product.

3.2. History of Process Control Chips

One of the earliest test chips reported was designed by Barone and Myers in 1968 which they used for device characterisation, process control as well as circuit reliability purposes [6]. It had 44 probe pads and was used to aid development of a bipolar 8-bit adder product circuit. The test chip had eleven test structures; a bipolar transistor, base resistor, base-under-emitter resistor, step coverage resistor, metal sheet resistor, base collector diode with buried layer, buried layer resistor, metal-semiconductor contact resistor array, metal-metal contact resistor array, multi-emitter transistor and MOS capacitor.

Other early test chip designs, by Schnable and Keen [7] in 1969 and Sahni [8] in 1970, used their chips as reliability monitors. In both these cases the chips were packaged and subjected to thermal stress tests. These early test chips were not intended to be probed automatically and were only used as a 'spot check' to check that the process was under control.

These test chips were of limited use as they were, typically, not comprehensive having frequently been hastily designed by process engineers with limited experience. The resulting designs, without any consistency, were often poorly laid out for automatic testing. As a result skilled technicians would have to spend significant amounts of time manually probing, testing and analysing data from these chips [9].

As technology advanced through the 1970's the size of product circuits increased. As a consequence the PCC became larger since its size is dictated by the product chip dimensions. This increase in area enabled a considerably larger number of test structures to be incorporated. These more comprehensive PCCs made the routine use of parametric test

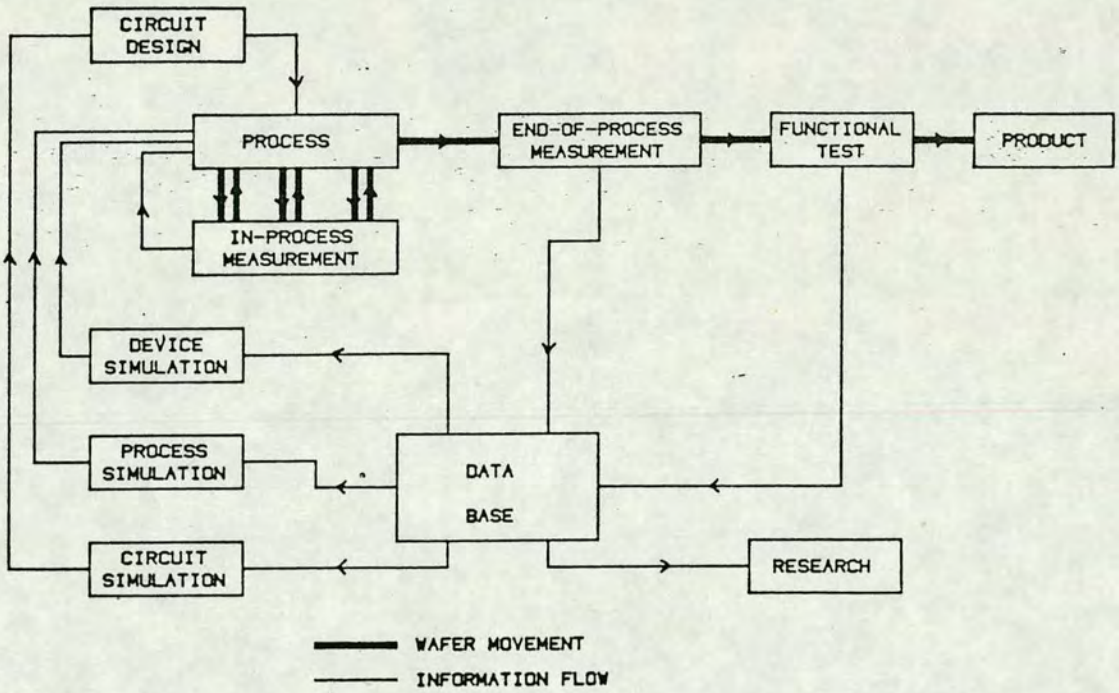


Figure 3.1. The flow of information for process control. After [15]

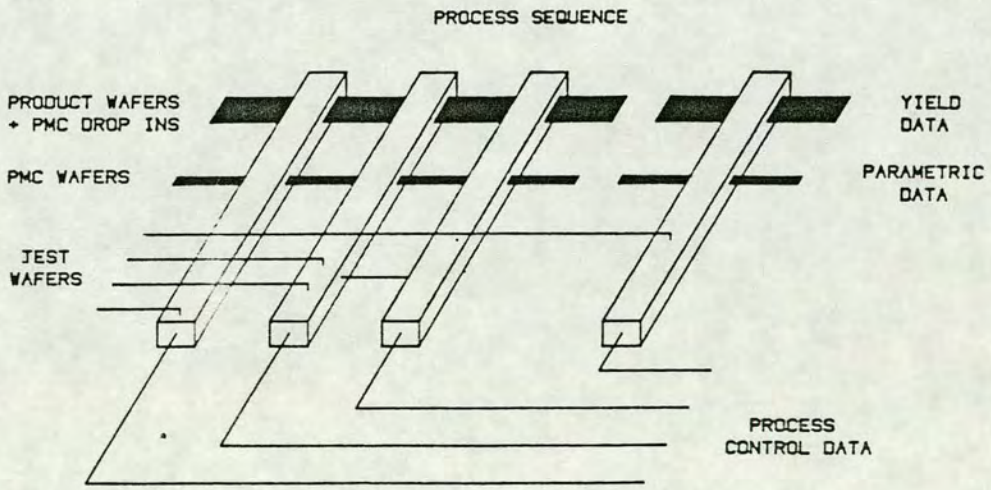


Figure 3.2 The types of processed wafers and the information they give for process monitoring. After [15].

considerably more attractive. This led to the development of dedicated parametric testers becoming available around 1975. A consequence of the increase in the number of test structures was an increase in the number of probe pads. As a result if a PCC were to be measured in a single pass a large switching matrix would be required. Test chips also tended to be structured similarly to product wafers with probe pads around the periphery of the chip, necessitating the use of a new probe card for every new test chip. These problems can be avoided by the design of test chips in a 2 × N probe pad array [10]. Figure 3.3 shows a chip organised so as to be probed by a 2 × N array probe card. Only a single 2 × N probe card is required which can be stepped internally across the test chip. This has several advantages. Namely only one probe card is required so time consuming card interchange is avoided, the structures are isolated so there is no interference between them, the chip design will be modular, i.e. each of the 2 × N sections can be stored in a CAD library and can be 'called up' when required by a new design. Optimum size for probe pads in a 2 × N array size and the need for good probing methodology to reduce errors caused by bad probing has also been investigated [11].

An area where PCCs are playing an increasingly important role is in acceptance or rejection of wafers from silicon foundries. Normally only a small number of wafers will be produced and each wafer may have a number of different designs so PCCs are routinely used to help define wafer acceptance criteria.

The growth of the importance of parametric test and process control has been reflected by the growing availability of specialised parametric test equipment. Over the years this equipment has graduated from hand probing using curve tracers to today's specialised parametric testers, automatic probers and computerised databases. Articles about specific topics within the sphere of parametric test are now common in the literature as are more general review papers [4,12-18]. Conferences have sessions devoted to the subject and there is now a conference solely devoted to the design and measurement of test structures. †

† International Conference on Microelectronic Test Structures (ICMTS). 1988-Long Beach, California. 1989-Edinburgh, Scotland. 1990-San Diego, California.

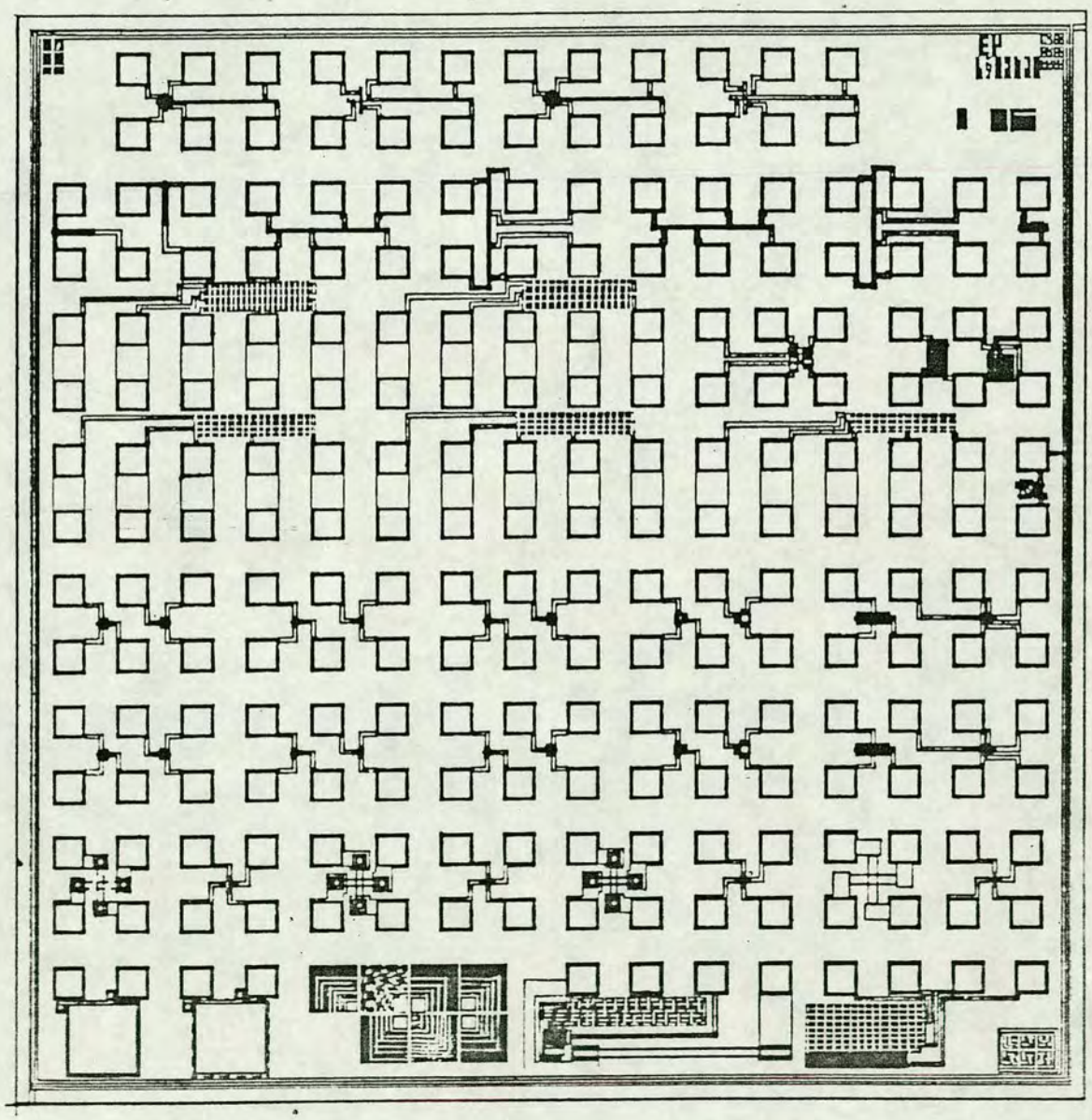


Figure 3.3. A test chip designed to be probed by a 2 × 10 probe card. After [15].

3.3. PCC Test Structures

Test structures can be employed for a number of different purposes some of which are given below,

(1) Device parameter extraction.

(2) Design rule checking.

(3) Process parameter extraction.

(4) Random fault analysis.

(5) Reliability analysis.

(6) Circuit parameter extraction.

Of these, those under the headings of process, device and circuit parameter extraction are by far the most frequently used.

Numerous test structures have been devised through the years to fulfil the above listed functions with many finding use in more than one of these categories. Whatever the function of the test structure though its design should obey the circuit layout rules of the process and where possible should be liberalised so only features under test show layout rule dependence.

Over the years these structures have been assembled into many test chips for many different technologies. These chips may perform a particular function or may analyse a particularly new process or technology [19-25]. Attempts have been made to rationalise test chip design by stating which structures should be included in a test chip [26,27] or by mooting a standard test chip methodology [28].

3.3.1. The Greek Cross

The Greek cross structure shown in figure 3.4 has several applications in PCCs. At a simple level it allows simple four terminal Kelvin measurements of the sheet resistance of appropriate structures made from polysilicon, diffusion or bulk silicon [29]. Four terminal measurement is preferred over two as the Kelvin structure eliminates contact and probe needle resistance from the measured resistance. The measured resistance of the structure is that of the area at the heart of the cross which can be made as small as the process allows. Use of a Greek cross structure is included in some of the structures used to measure linewidth and misalignment, where sheet resistance found from the Greek cross forms part

of the measurement.

The theory underpinning this structure was formulated by van der Pauw [30,31] who proposed a formula which allowed the resistivity of an arbitrary shaped, hole free, lamina to be calculated. It uses four point contacts on the edge of that lamina as shown in figure 3.5.

If a current (i_{MN}) is forced between contact M and N, of figure 3.5, the potential difference (V) between P and O can be measured. We can define resistance (R) in the following manner,

$$R_{MN,OP} = \frac{V_P - V_O}{i_{MN}} \tag{3.1}$$

$$R_{NO,PM} = \frac{V_M - V_P}{i_{NO}} \tag{3.2}$$

Van der Pauw's theorem states there is a relationship between these two values such that,

$$\exp\left[-\frac{\pi d}{\rho} R_{MN,OP}\right] + \exp\left[-\frac{\pi d}{\rho} R_{NO,PM}\right] = 1 \tag{3.3}$$

With d the lamina thickness and ρ its resistivity. It can be subsequently shown that,

$$\rho = \frac{\pi d}{\ln 2} \cdot \frac{R_{MN,OP} + R_{NO,PM}}{2} \cdot f \tag{3.4}$$

where f is an asymmetry factor, a measure of the lamina asymmetry.

For a sample with a line of symmetry, e.g. with M and O on the line of symmetry and N and P placed symmetrically with respect to that line (as illustrated by figure 3.6) then,

$$R_{MN,OP} = R_{NO,PM} = R \tag{3.5}$$

with equation 3.4 becoming,

$$\rho = \frac{\pi d}{\ln 2} \cdot R \tag{3.6}$$

$$\rho_{sheet} = \frac{\pi}{\ln 2} \cdot R \tag{3.7}$$

Van der Pauw's theory did not fully consider the problem of finite contacts and the effect they would have on the measured resistivity.

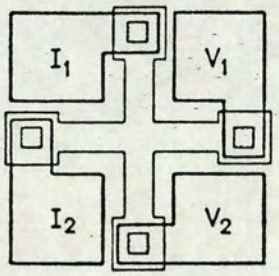


Figure 3.4. The Greek cross structure. After [33].

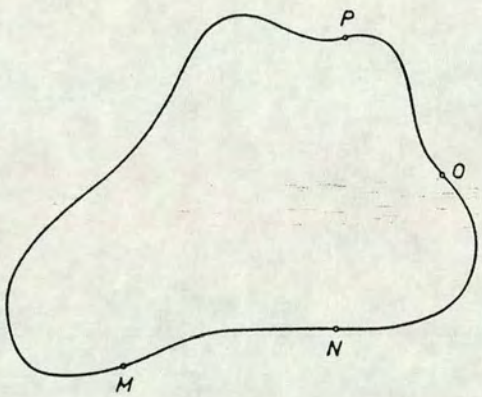


Figure 3.5. A flat lamina of arbitrary shape with four point contacts on the periphery. After [31].

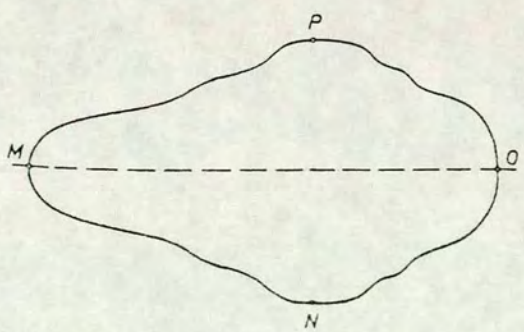


Figure 3.6. A symmetrical flat lamina. After [31].

This problem was initially tackled by Chwang *et al.* [32] who conducted experiments on a square electrolytic tank and developed a resistor analogue model of the lamina. His results, given by figure 3.7, show that his model fitted the data well and that for small contacts (compared to the lamina size) only a small deviation from the van der Pauw formula is observed. The resistor analogue model was extended by David and Buehler to numerically analyse different resistor test structures and to quantify the deviation from equation 3.4 for each one [33]. They analysed the quadrate cross test structure (shown by figure 3.8), the offset quadrate test structure (figure 3.9) and a limiting case of the latter, the Greek cross (figure 3.10).

For these structures the true sheet resistance (ρ_{sheet}) is related to the calculated sheet resistance (as found by the symmetrical van der Pauw equation (equation 3.7)) by,

$$\rho_{sheet} = \frac{\rho_{sheet}\ (calculated)}{1 - E} \tag{3.8}$$

where E is the normalised error between the two resistance values. For the Greek cross structure E has been found to be,

$$E = 0.590\ .\ \exp\left[\ 6.23\ .\ \frac{A}{S}\ \right] \tag{3.9}$$

where A and S are defined in figure 3.10.

From this an error of less than 0.1% between true and calculated resistance values can be achieved for $A/S \geq 1.02$ which can be easily achieved in practice. This numerical analysis approach was confirmed by a theoretical treatment of the Greek cross structure by Versnel in which conformal transformation is used [34].

The Greek crosses validity has been verified experimentally with cross structures as small as $6.4\mu m$ in width giving sheet resistance values within 0.5% of conventional van der Pauw sheet resistors as large as $762\mu m$ in diameter [35]. Problems can arise if large surface leakage currents occur and this results in sheet resistance values higher than expected. To reduce this problem it was found that the arm length should be as short as possible (given the constraint of the arm length to width ratio (A/S of figure 3.10)), a channel stop implant should be used and if possible the use of a peripheral biased gate [35]. As linewidths in the van der Pauw structure can be very narrow and the current needed to force 'detectable' voltages may in some cases be very high, joule heating can be a problem. Where feasible the use of large width arms can reduce this effect [35].

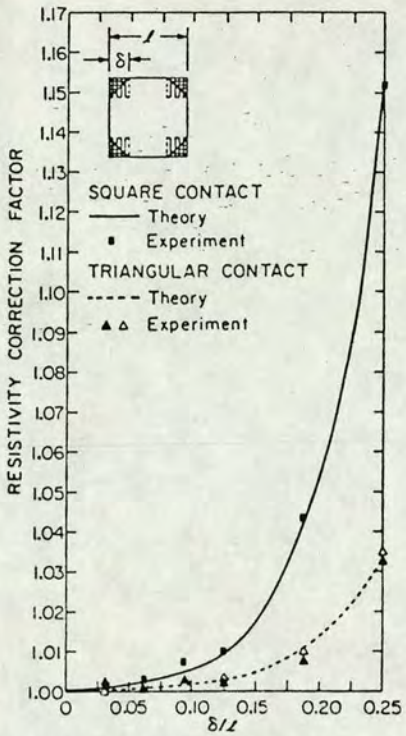


Figure 3.7. Results showing the effect of finite size contacts on a van der Pauw type lamina. After [32].

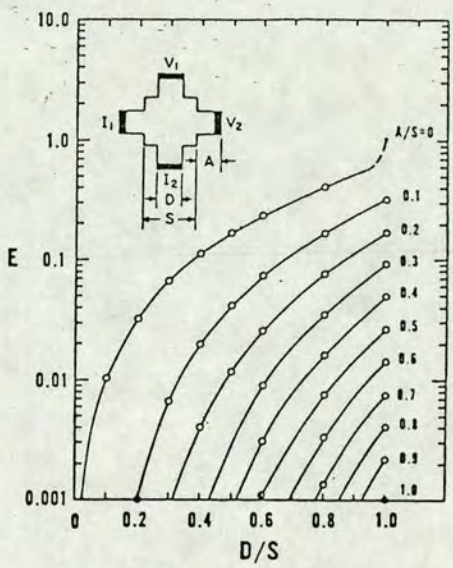


Figure 3.8. Normalised sheet resistance error (E) due to width and length of contact arms for quadrate cross structure. After [33].

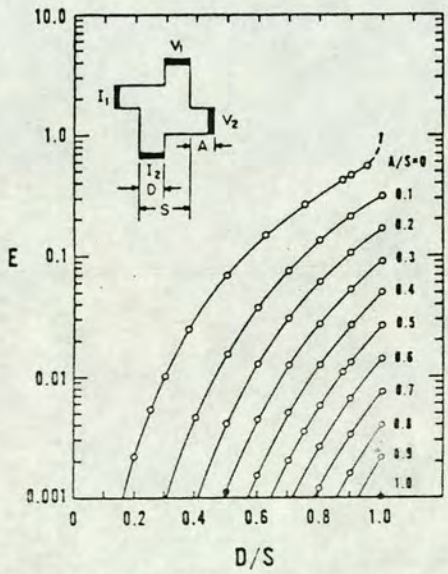


Figure 3.9. Normalised sheet resistance error (E) due to width and length of contact arms for offset quadrate cross structure. After [33].

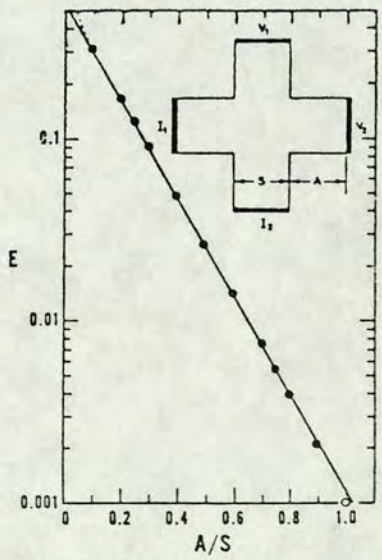


Figure 3.10. Normalised sheet resistance error (E) for a special case of the offset quadrate cross with $\frac{D}{S}=1$, the Greek cross. After [33].

Van der Pauw type sheet resistance measurements have also been compared with those derived by the four point probe method [29,36,37]. These showed that the results were compatible and that the van der Pauw structure was suitable for measuring resistance variations over a whole wafer.

The resistance of a Greek cross can be calculated most accurately in practice as follows. A current is forced between pads A and B (I_{AB}), of the Greek cross shown in figure 3.11, and the voltage between D and C measured (V_{DC}). The current is then reversed (I_{BA}) and the voltage between C and D measured (V_{CD}). The incremental resistance ($R_0\circ$) is then calculated,

$$R_0\circ = \frac{V_{DC} - V_{CD}}{I_{AB} - I_{BA}} \tag{3.10}$$

The process is repeated at 90° to the above by forcing current through B and C and measuring voltages between A and D,

$$R_{90}\circ = \frac{V_{AD} - V_{DA}}{I_{BC} - I_{CB}} \tag{3.11}$$

R in equation 3.7 is then given as

$$R = \frac{R_0\circ + R_{90}\circ}{2} \tag{3.12}$$

3.3.2. Linewidth

The measurement of linewidth is a useful tool in the monitoring of layer etching processes and as such is an important parameter. For example in circuit design the value of diffused or implanted resistors is determined partly by knowledge of the linewidth and the source-drain current is directly dependent upon transistor gate dimensions.

First methods of linewidth analysis involved both optical [38] and electrical techniques. The latter commonly employed the double-bridge method [39] which required fabrication of two different width bridge sheet resistors. Measurement of this structure required a differential method involving the subtraction of two nearly equal quantities. As this method is prone to error a more accurate method of linewidth determination was proposed by Buehler, Grant and Thurber [40]. They combined a bridge with a van der Pauw structure [30,31] that could be combined into one single structure. This the cross-bridge resistor structure is shown in figure 3.12.

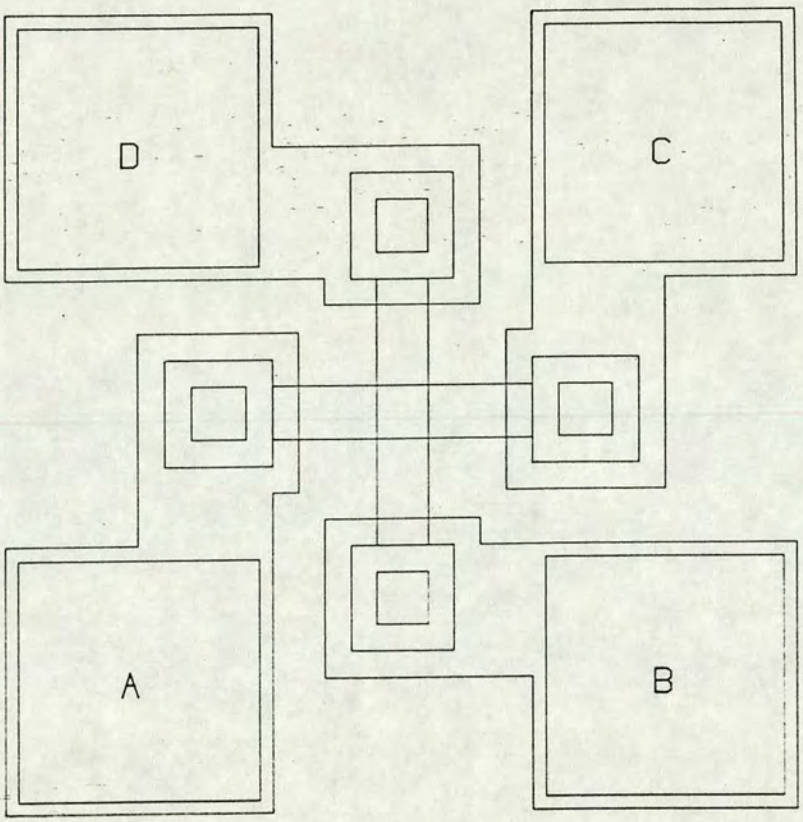


Figure 3.11. The Greek cross. After [15].

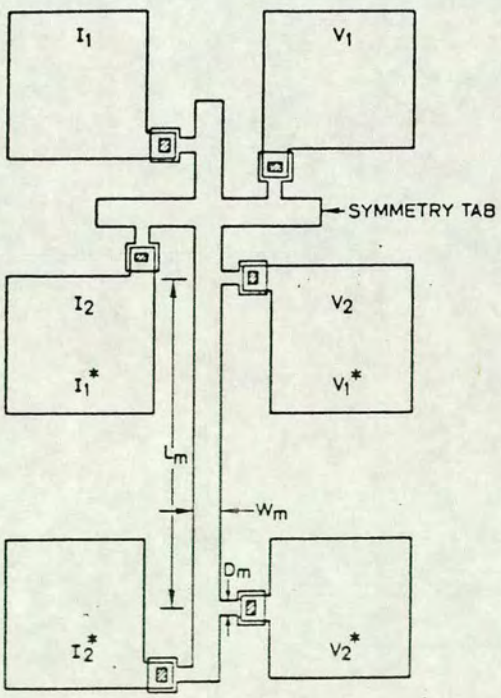


Figure 3.12. The cross-bridge structure used to measure linewidth. After [40].

This structure can be used to measure the linewidth of conducting layers (metal, poly, diffusion) and is essentially a bridge resistor with integral Greek cross. The Greek cross being designed so that the van der Pauw correction factor f (equation 3.4) can be assumed to be unity since the asymmetry factor (F_a) is less than 10% [35]. To find the linewidth (W_e) it is first necessary to determine the sheet resistance (R_s) of the conducting layer. The Greek cross is used for this with pads I_1, I_2, V_1, V_2 of figure 3.2 being utilised and the incremental resistance method employed (equations 3.10-3.12). Linewidth is then determined using the pads labelled I_1^*, I_2^*, V_1^*, V_2^* and the following equation,

$$W_e = \frac{R_s L_m}{R^*} \tag{3.13}$$

where L_m is the drawn linewidth between the voltage taps V_1^* and V_2^* and R^* is the incremental resistance determined by forcing a current in opposite directions through I_1^* and I_2^*,

$$R^* = \frac{V^*(+I) - V^*(-I)}{I^*(+I) - I^*(-I)} \tag{3.14}$$

With $+I$ and $-I$ denote the forward and reverse currents respectively.

To confirm their results Buehler *et al.* [40] compared results obtained from this structure with both optical and double-bridge structures and indicated comparable results with the cross-bridge structure. Linewidth variations of the order of $\pm 0.1 \mu m$ were monitored.

Various layout structures can be devised using this cross-bridge structure. One example utilised by Prometrix showing a central van der Pauw structure and six bridge resistors is shown in figure 3.13 [41].

These linewidth structures can be easily designed and used in any PCC. An example of its application is examination of linewidth variations across wafers and within a chip itself [1]. Similarly variations in linewidth can be used to characterise lithography tools by delineating a single layer cross-bridge in metal and then suitably analysing the inter and intra chip variations [2,42]. Analysis of individual process steps and their effect on linewidth are also possible. For example the effect of plasma descumming on the linewidth uniformity of metal lines has been investigated for linewidth control of small geometry processes [42]. Monitoring of plasma etching itself is another application for linewidth structures. In one such study wafers were subjected to similar lithographic processes but

were processed with different plasma compositions and pressures with linewidths measured using a cross-bridge like structure [43,44]. Dimensional anisotropy of the lithography/process system can be investigated by having orthogonally orientated linewidth structures such as that depicted in figure 3.14.

As in common with other parameters data from linewidth measurements can be collated on disk, wafer contour plots produced as well as attempting to correlate variations with other parameters [46].

Optical measurement of linewidth can be made 'in line', by use of CD structures, and this is still a routine part of the fabrication sequence which gives early warning of possible problems [47-50]. These systems have the advantage that measurements of non-conductive layers such as photoresist can be measured, but unless automated they will not produce as comprehensive a data base as electrical methods.

3.3.3. Mask Misalignment

3.3.3.1. Introduction

When an integrated circuit is fabricated the various layers must be correctly aligned. This overlay registration is crucial in achieving higher packing densities for ICs and the amount which can be tolerated reduces with smaller geometry processes. The tolerance is roughly in proportion with the geometry decrease with, for example, a $5\mu m$ process with $1\mu m$ overlay tolerance becoming $0.2\mu m$ for a $1\mu m$ process [51]. Thus with these small features overlay capabilities of lithography tools becomes more critical and the ability to measure misalignment, commensurately more important. Alignment between layers is achieved by aligning subsequent masks to alignment 'targets' on previously processed layers. These targets can take a number of shapes of which the more common are; cross in a box, box in a box, 'L' and 'V' shapes. Masks may be aligned by an operator or may be fully automatic. Operator alignment is more common with older whole wafer mask exposure technology (contact printing for example) whereas step and repeat mask systems are normally automatic. Although step and repeat systems are automated using a die by die alignment system, some form of operator pre-alignment of each wafer may still be required.

Misregistration can be broken down into five types of errors as follows (depicted in figure 3.15.) [51],

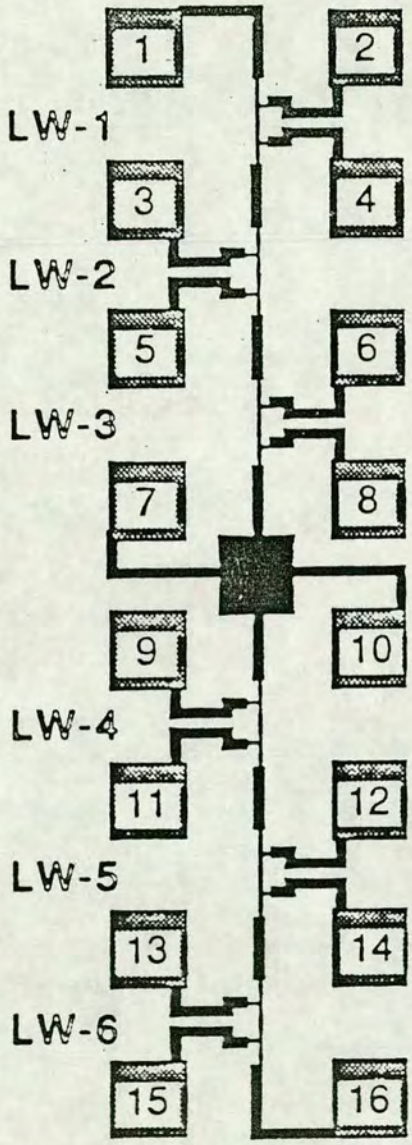


Figure 3.13. Prometrix 'linewidth module' with central van der Pauw structure and six bridge resistors. After [56].

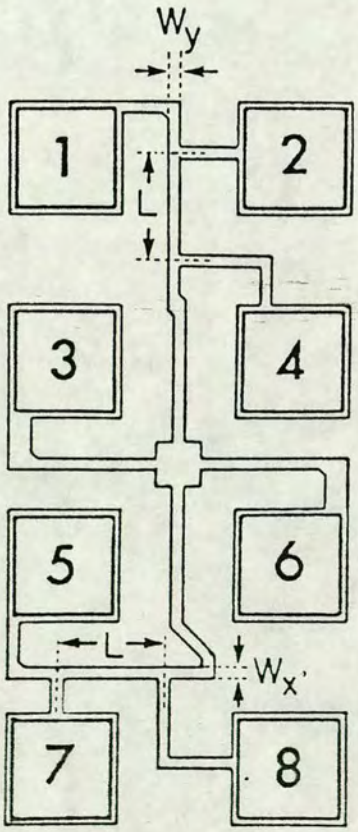


Figure 3.14. Test structure to measure linewidth in both X and Y directions. After [5].

(1) Translation - an offset of the top layer in the $X-Y$ plane.

(2) Rotation - a clock/anti-clockwise shift in the top layer.

(3) Magnification - the overlying layer is larger or smaller than intended.

(4) Trapezoid - a magnification error at one end and a miniaturisation error at the other caused by the mask/reticle being tilted out of its proper plane.

(5) Distortion - lens related problems affecting shape reproduction accuracy on the wafer.

The first three of these can be analysed mathematically using the 'six parameter' model where the X and Y components of the vector misalignment (d'_x and d'_y) can be represented by two linear equations [52,53]

$$d'_x = T_x - \theta_x y + E_x x \tag{3.15}$$

$$d'_y = T_y + \theta_y x + E_y y \tag{3.16}$$

Where $\theta \equiv \frac{(\theta_x + \theta_y)}{2}$ and the components are as shown in figure 3.16.

3.3.3.2. Measurement

Both in-line and off-line measurement of misregistration can be measured with optical, SEM and electrical structures. Perhaps the simplest structure used to measure this parameter is the optical vernier an example of which is shown in figure 3.17 [51]. To measure the misalignment a graduated scale is printed on each of the two layers between which the misregistration is to be measured. The pitch between the tick marks is slightly different and the human eye (via a microscope) is used to gauge which of the two lines on the scales are colinear and this point corresponds to the degree of misalignment. This is reasonably simple as the human eye is better at estimating co-linearity than measuring offsets but the method has a number of disadvantages. Measurement by this method is to some extent operator dependent and the speed of measurement is slow and as a result only a few structures across a wafer can viably be measured. Optical systems can be automated and one method of achieving this is by the use of 'box-within-a-box' structures illustrated by figure 3.18. This system operates by the software first identifying the edges of both boxes then the centroids of each structure. The offsets in the X and Y directions are then calculated. In these systems differing amounts of operator interaction are needed to initiate the measuring process depending on the sophistication of the automation for the instrument

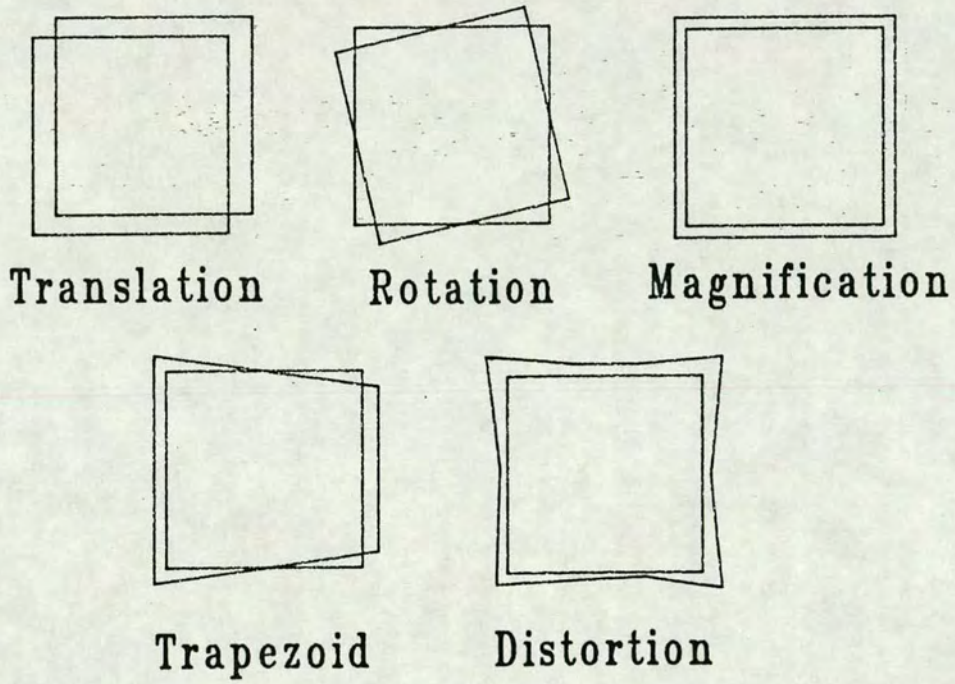


Figure 3.15. Five types of misregistration error.

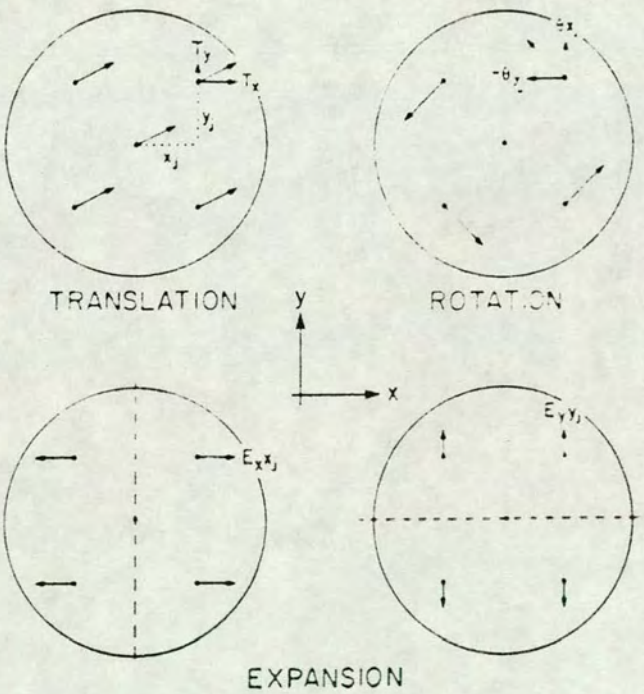


Figure 3.16. Schematic representation of the manner in which translation, rotation and expansion contribute to the X and Y components of mask superposition error. After [51].

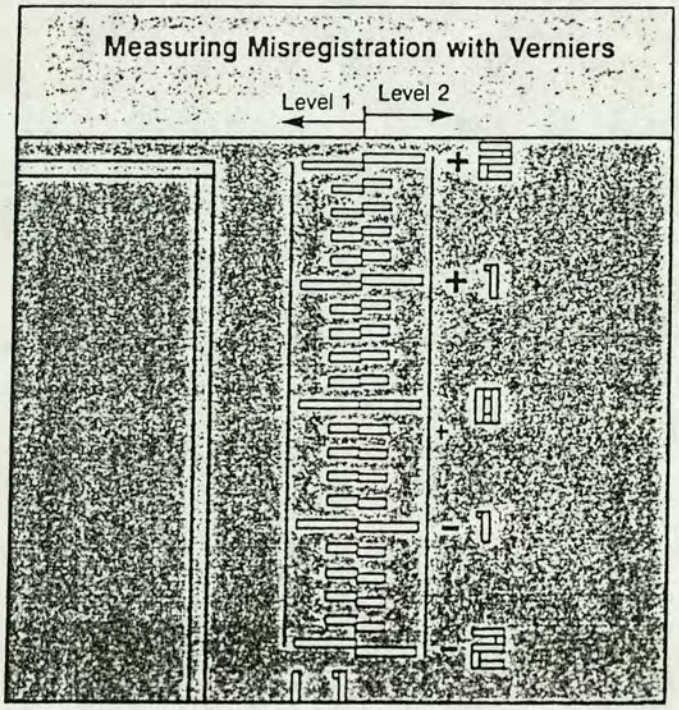


Figure 3.17. An optical vernier for measuring layer misregistration. After [50].

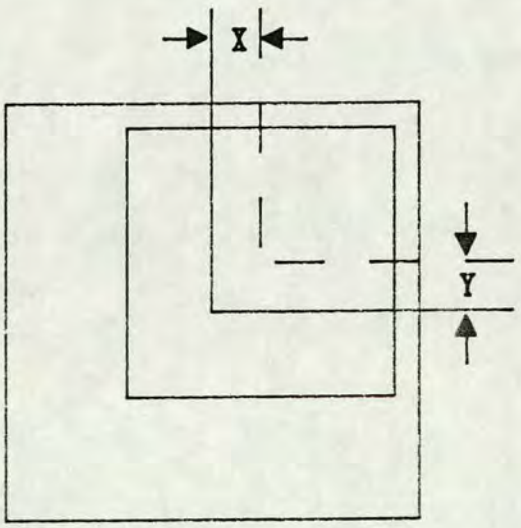


Figure 3.18. The 'box-within-a-box' structure used for automated optical misalignment measurements.

in use [51].

To enhance misalignment measurement it is possible to use an SEM or other e-beam type in place of the optical systems mentioned above. These systems give enhanced resolution but at a reduced wafer throughput and higher equipment costs [54]. SEM analysis may consist of inspection of verniers, similar to the optical type, or by use of more advanced specially designed structures suitable for exclusive SEM use. For example the use of the voltage contrast method in conjunction with a stepped vernier structure has been demonstrated [55].

Although electrical measurements are not as amenable to in-line measurement as optical systems they make up for this by accuracy, repeatability and the ability to generate quickly a large amount of process characterisation information. The structures themselves can take numerous forms and several different designs exist. Most commonly used structures for misalignment have been the simple analogue ones in which the basic measuring process involves forcing a current along a conducting bar and misalignment measured by the relative positioning, and hence voltage drop, between voltage taps [56]. An analogy is to view this structure as a kind of potentiometer with the voltage difference between the sliding contact (the central voltage tap) and the ends of the potentiometer determining the misalignment. With zero misalignment the voltage drops in both arms will be the same.

The simplest structure of this type is shown by figure 3.19 which depicts a combined structure for both X and Y misalignment determination [1,56]. The vertical or Y misalignment is determined by forcing a current between the pads labelled I_1 and I_2 and measuring the voltage differences V_{12}, V_{23}, V_{34}. The displacement of the contact window at point V_3 from the midpoint between between taps V_2 and V_4 is given by,

$$L_y = \frac{L_{12}(V_{34} - V_{23})}{2V_{12}} \tag{3.17}$$

where L_{12} is the distance between taps V_1 and V_2. The X misalignment is determined in a similar manner by forcing the same current used in the Y case between the pads labelled I_2 and I_3 and measuring V_{56} and V_{67}. The X alignment is then,

$$L_x = \frac{L_{12}(V_{67} - V_{56})}{2V_{12}} \tag{3.18}$$

The X and Y alignments can then be combined to form a vector representing the total

mask displacement at the test structure site.

Many variations of this simple bridge structure exist. A production incompatible (in the sense that a special test wafer must be used) variation is used by Prometrix [41]. The first exposure forms a layer as depicted on the left hand side of figure 3.20. The same mask is then shifted to the left, an alignment performed so that the structure on the right of figure 3.20 lies 'exactly' over that of the left. A second exposure is then performed before etching of the clear areas takes place. This results in two sets of opposing bridge structures, one for each of the X and Y directions. The overlay error in X and Y is thus respectively,

$$dx = \frac{(W_1 - W_2)}{2} \tag{3.19}$$

$$dy = \frac{(W_3 - W_4)}{2} \tag{3.20}$$

where W_i $(i = 1 - 4)$ are found using the linewidth finding formula, equations 3.17 and 3.18.

The idea of using the modulated width of parallel conducting tracks has also been evolved for the production compatible structure shown in figure 3.21 [57,58]. The central area, for example polysilicon, modulates the width of two conducting tracks, an implanted 'source-drain' in this example. Misalignment is calculated from the difference in the two track widths from the nominal and is calculated by using equation 3.19. Separate X and Y structures give the complete misalignment vector.

A structure which has found much use, although it is another example which is production incompatible , is that developed by Perloff [52,59,60] and utilised to measure errors in step and repeat lithography systems [53] and monitoring of process uniformity [5]. The structure measures the displacement of contact arms from their central position with information for X and Y direction coming from the same single structure. Mask layer one $(M1)$ delineates the sensor square body and sensor arms 2 , 4 , 6 , 8 as labelled in figure 3.22. The second mask $(M2)$ is aligned to $M1$ such that arms 1 , 3 , 5 , 7 are added to the structure at the mid-points of sides 82 , 24 , 46 and 68 if $M1$ and $M2$ have been perfectly superimposed. These arms overlap the body of the structure by a distance greater than any anticipated mask supposition error. The structures are made electrically active by an ion implant and anneal cycle. The misalignment is calculated as follows. If mask $M2$ has not been superimposed correctly with respect to $M1$ then arm 5 will be

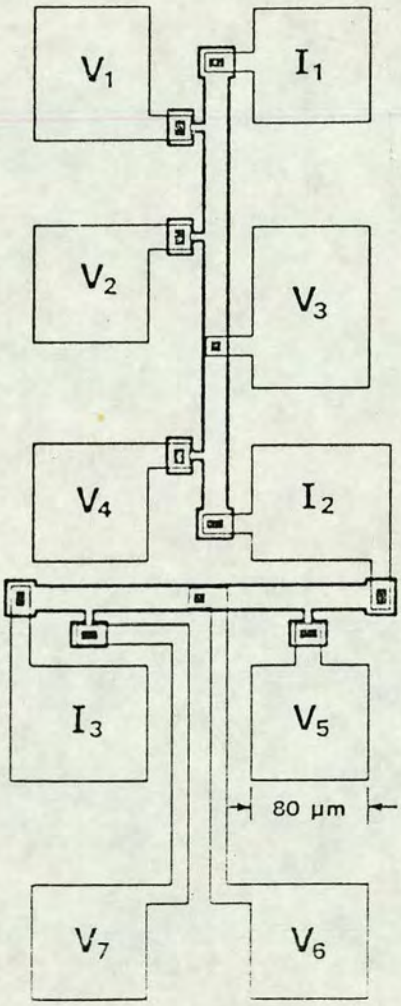


Figure 3.19. A production compatible test structure for measurement of both X and Y misalignment. After [10].

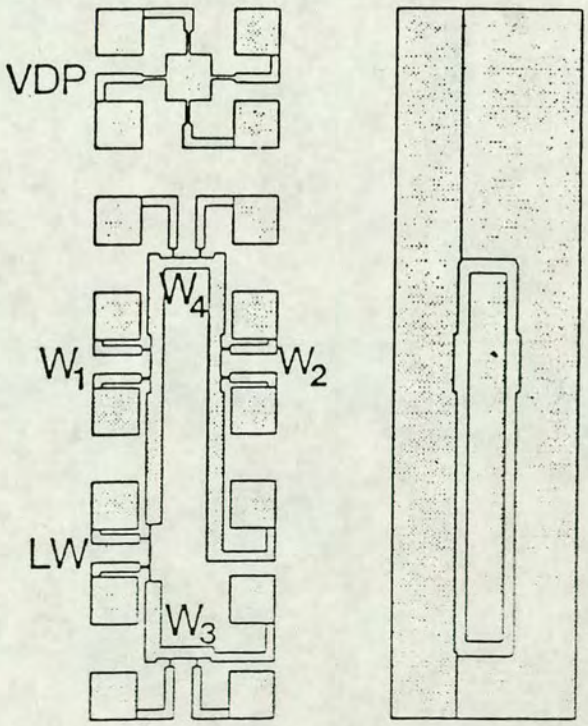


Figure 3.20. Structure used by Prometrix for measuring misalignment. After [56].

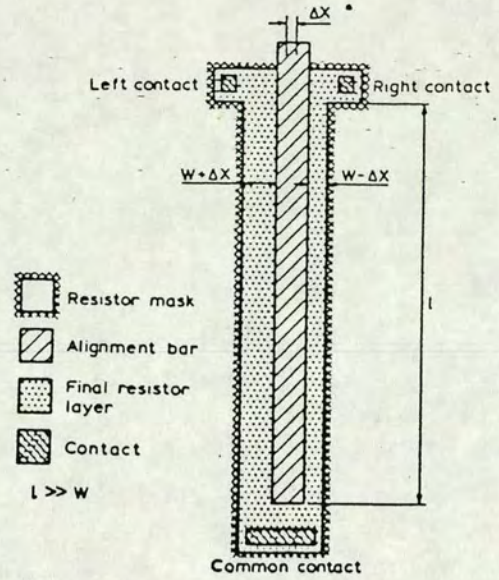


Figure 3.21. Misalignment structure based on the width of two conducting tracks. After [57].

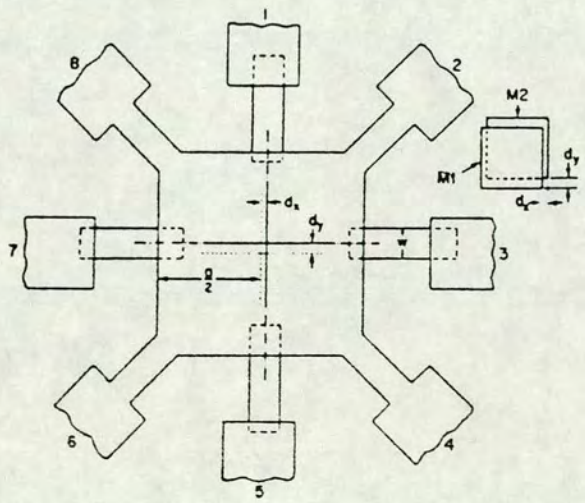


Figure 3.22. Misalignment structure developed by Perloff. After [59].

displaced a distance d_x from the midpoint of side 46 and arm 3 a distance d_y from the midpoint of side 24. From use of conformal transformation the following can be found,

$$d_x = \frac{a}{2} \cdot K(m) \cdot \sin^{-1}(Y_x) \tag{3.21}$$

where a is the side of the body square, $Y(m)$ is a Jacobian elliptic function and $K(m)$ is evaluated in terms of the complete elliptic integral of the first kind and is equal to 1.5826. $Y(m)$ can be approximated as follows,

$$Y_x = \frac{R'_x - R''_x}{R'_x + R''_x} \tag{3.22}$$

with $R'_x = \frac{V_{65}}{I_{82}}$ and $R''_x = \frac{V_{54}}{I_{82}}$.

Similar equations hold for the Y direction viz,

$$d_y = \frac{a}{2} \cdot K(m) \cdot \sin^{-1}(Y_y) \tag{3.23}$$

$$Y_y = \frac{R'_y - R''_y}{R'_y + R''_y} \tag{3.24}$$

with $R'_y = \frac{V_{43}}{I_{68}}$ and $R''_y = \frac{V_{32}}{I_{68}}$.

The sheet resistance, ρ_{sheet} can be found using equation 3.4

$$\rho_{sheet} = \frac{\pi}{\ln 2} \cdot \frac{R_I + R_{II}}{2} \cdot f\left(\frac{R_I}{R_{II}}\right) \tag{3.25}$$

where $R_I = R'_x + R''_x$ and $R_{II} = R'_y + R''_y$.

The factor $f\left(\frac{R_I}{R_{II}}\right)$ can be approximated to unity with an error $<0.1\%$ as the body of the structure is square. Structures with deliberate offsets gave excellent agreement to the electrically derived values and an accuracy of $\pm 0.1 \mu m$ was found with this technique [52,59].

The performance of the bridge and the modified van der Pauw structure has been compared for wafers where deliberate offsets were introduced between the measuring layers [61]. Limitations of misregistration structures were identified as variations in the sheet resistance, nonuniform tap delineation, nonuniform etching of the channel width, errors in the electrical instrumentation and variations in the current and contact resistance. Larger errors were found in the bridge structures and were attributed to their larger size which

make them more sensitive to sheet resistance variations.

A different approach to measuring misalignment, particularly polysilicon to active area is the use of transistors with specially patterned gates [62,63]. The gates of these devices in both cases are tapered and by analysis of the drain current equation for this gate shape, misalignment values can be calculated. Figure 3.23 shows the schematic view of the device used by Lozano *et al.*

All the structures described to here rely on analogue measurements, usually based on a sheet resistance measurement where non-uniformity of linewidth, film thickness and layer homogeneity can cause errors. Digital misalignment structures have been developed to overcome some of these problems. These digital structures all work in a broadly similar manner utilising an electrical vernier approach. The electrical vernier typically has an array of similar elements each of which has the critical test feature offset by the vernier step distance between adjacent elements. In all cases the digital structure's measurement resolution is only limited by the resolution of the lithography equipment because the pitch and range of the vernier can be chosen to suit the particulars of the process required.

Digital measurement structures can take a number of forms and an early example is the tapered comb structure demonstrated by Yamaguchi *et al.*, depicted by figure 3.24. Each tooth of the comb has a fixed step to its adjacent tooth and the registration error between the two layers is found from the difference between the number of teeth connected on either side due to the misalignment of the central contact,

$$Registration\ Error = (N_R - N_L) \cdot \frac{S}{2} \tag{3.26}$$

where N_R and N_L are the contact numbers on the right and left respectively and S the fixed step size. A similar structure is required for each of the X and Y directions to give a complete misalignment vector. The data from each tooth was loaded into a shift register and clocked out. The measurement of one structure took $500\mu s$ a considerable speed increase over analogue structures as no instrument switching or settling time is required.

A variation of this structure is shown by figure 3.25 and has been used to measure contact to polysilicon alignment although its main function was to measure contact hole size [65,66]. Misalignment is measured as for the toothed comb structure with the contact size measured as follows,

$$W_c = D_c - W_p \tag{3.27}$$

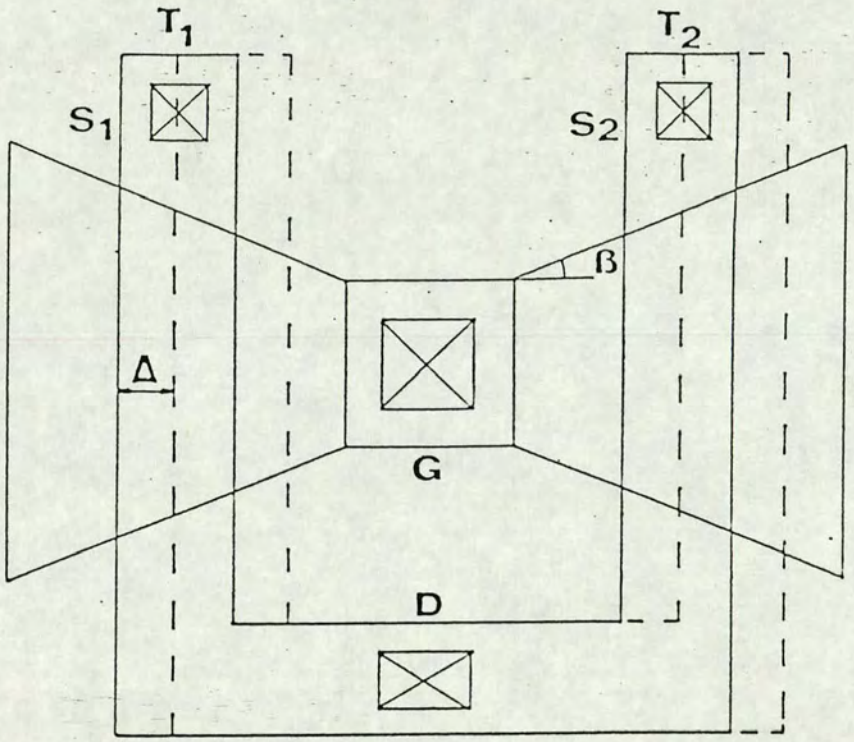


Figure 3.23. Triangular gated MOSFETs used to measure polysilicon to active area misalignment. After [63].

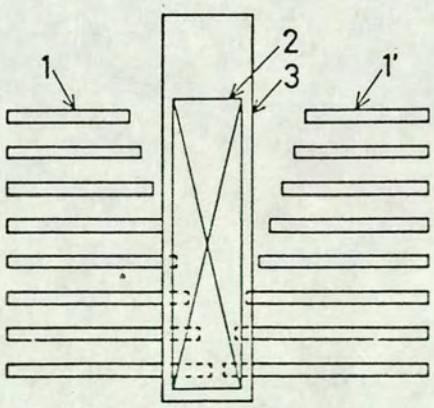


Figure 3.24. The tapered comb structure used for digital misalignment measurements. Areas 1 and 1′ are the comb elements, area 2 the contact hole and area 3 metallisation. After [64].

where W_c and W_p are the width of the contact and polysilicon respectively and D_c the design distance between the two contacts whose inside edges are measured to coincide most closely with the polysilicon edge.

As with the analogue structures polysilicon to diffusion misalignment can be found by the use of a transistor-based structure. This is shown by figure 3.26. The gates of transistors are stepped so that at a region in the centre of the array of transistors an area where the transistors are off exists, figure 3.27. Due to current flow around the edge of the gate regions those at the end of the array of transistors will be on. Data can be loaded to a shift register and clocked out, the position of the off transistors allowing calculation of the misalignment.

The approach which was the basis for the work of this thesis was the use of a U-shaped tooth with a bar as the digital measuring structure, the bar being the stepped feature [68,69]. From the relative position and width of the central region of 'open circuits' between the tooth and bar both the misalignment and overetch respectively between two layers can be determined. By choice of bar and tooth and careful design various different layers can be investigated. Again separate verniers are required to obtain a complete misalignment vector.

3.3.4. Contact Resistance

Simple contact resistance may be measured by use of a two terminal structure such as a contact chain with a number of contacts. This does not give a fully Kelvin measurement and so for more accurate metrology other structures must be used. Contact resistance can be measured using the structure shown in figure 3.28. By solving simultaneous equations the sheet resistance (R_s) and contact resistance (R_c) can be found as follows (see figure 3.28 for notation) [70],

$$R_s = \frac{(R_1 - R_2)}{L_1 - L_2} \cdot W \tag{3.28}$$

$$R_c = \frac{R_2 L_1 - R_1 L_2}{2(L_1 - L_2)} \tag{3.29}$$

These equations are valid if,

$$R_c - R_f = \frac{(R_s \rho_c)^{1/2}}{W} \tag{3.30}$$

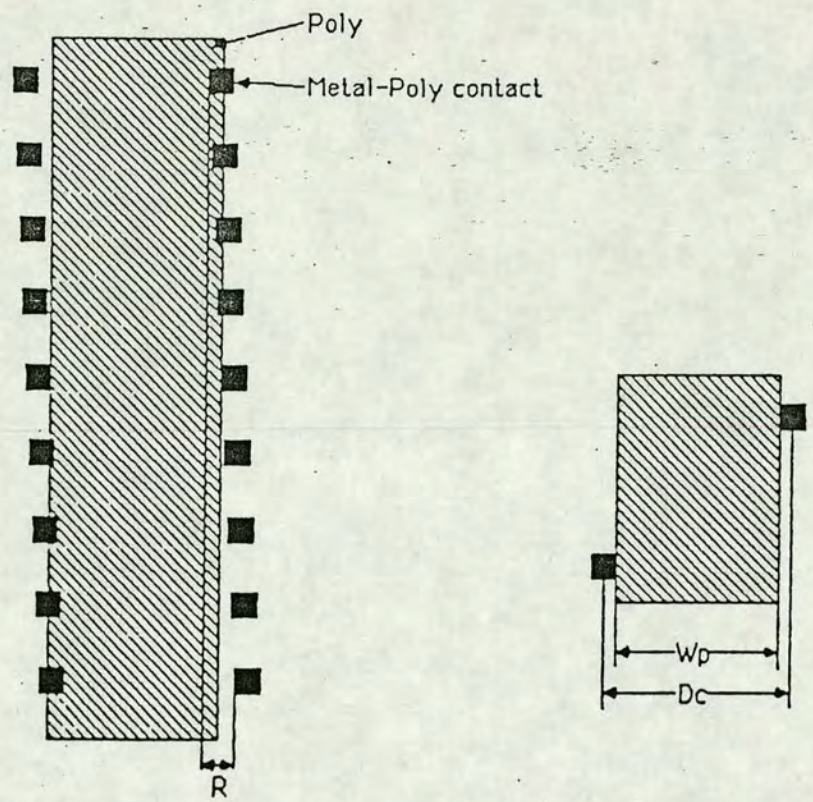


Figure 3.25. A digital test structure used to measure contact hole size but also capable of polysilicon to contact misalignment measurements. After [65].

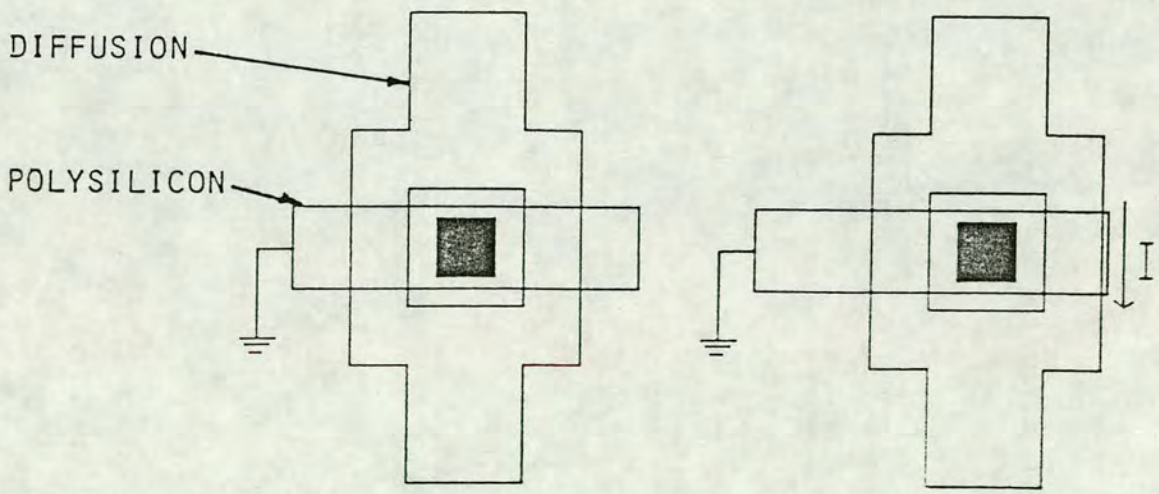


Figure 3.26. Principle of operation of transistors used for a digital polysilicon to active area misalignment structure. These show a non-conducting (left) and conducting transistor (right). After [67].

with ρ_c the specific contact resistivity and R_f the front contact resistance. This approximation holds for $W \geq 5\mu m$.

At the rear of the contact there remains a voltage drop V_e. This defines another parameter, the end resistance (R_e), see figure 3.29, where,

$$R_e = \frac{V_e}{I_i} = \frac{Z}{Sinh(\alpha d)} \tag{3.31}$$

with $\alpha = (R_s/\rho_c)^{1/2}$ and Z the minimum value of contact resistance as the length increases.

There is a difference between the resistance of a loaded (R_c) and unloaded contact (R'_c) and this measurement can be made as shown by figure 3.29. The difference between these two values also gives R_e [71],

$$R_e = \Delta R_c = R_c - R'_c \tag{3.32}$$

The problem of the above structure is that the the measurement of R_c depends upon subtraction of two large numbers. It also includes the effect of parasitic resistances and cannot take into account the change of resistivity of diffused layers underneath contacts. The Kelvin four terminal structure of figure 3.30 overcomes some of these problems and is used to find the interfacial contact resistance (R_i) with,

$$R_i = \frac{\rho_c}{A} \tag{3.33}$$

where A is the contact area.

The six terminal structure depicted in figure 3.31 can be used to measure R_e directly. To find R_e current is forced between pads 1 and 3 and voltage measured between pads 4 and 5. The front contact resistance (R_f) and the sheet resistivity underneath the contact (R_e) can be obtained from the following equations [71],

$$R_e = \frac{(R_{SD}\,\rho_c)^{1/2}}{W} \cdot Cosch\left[\left(\frac{R_{SD}}{\rho_c}\right)^{1/2} \cdot d\right] \tag{3.34}$$

$$R_f = R_e \cdot Cosh\left[\left(\frac{R_{SD}}{\rho_c}\right)^{1/2} \cdot d\right] \tag{3.35}$$

With R_{SD}, w and d the sheet resistance of the diffused layer directly under the contact, the contact window width and the contact window length respectively.

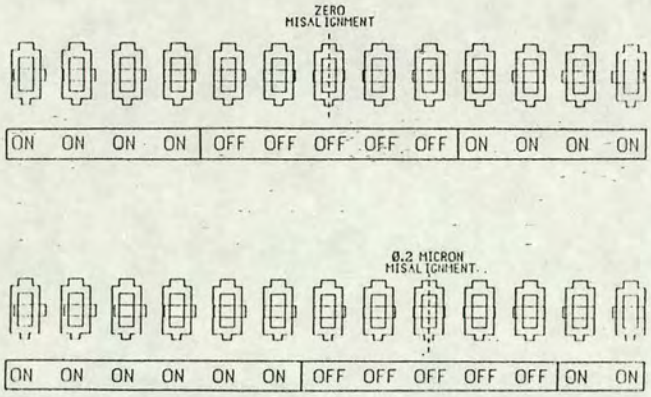
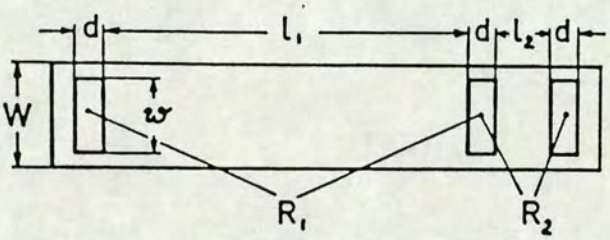


Figure 3.27. Array of transistors used to measure misalignment showing zero (top) and $+0.2\mu m$ (bottom) misalignment. After [67].



$$R_S = (R_1 - R_2) \cdot \frac{W}{l_1 - l_2} \qquad (8)$$

$$R_C = \frac{R_2 \cdot l_1 - R_1 \cdot l_2}{2\,(l_1 - l_2)} \qquad (9)$$

Figure 3.28. Structure to measure contact resistance. After [70].

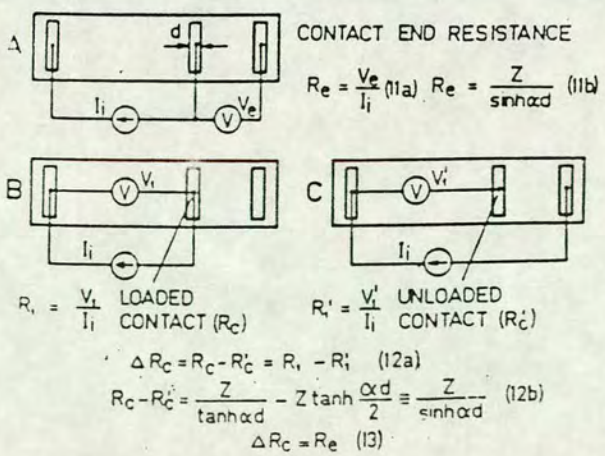


Figure 3.29. Measurement of contact end resistance. After [70].

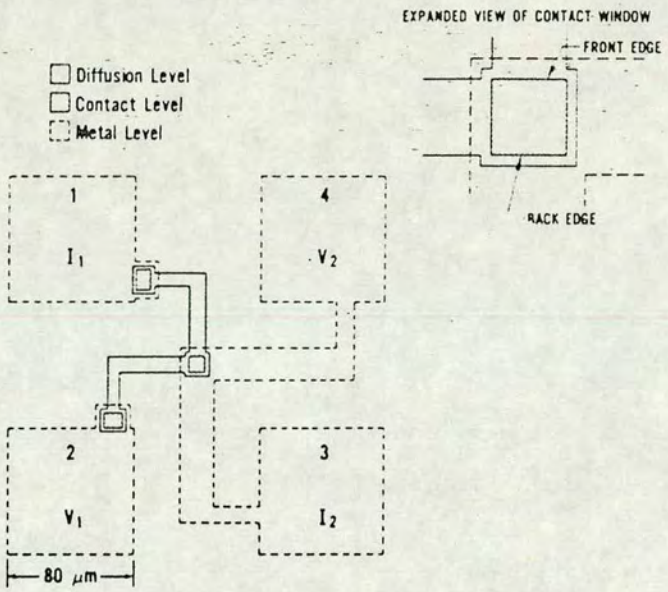


Figure 3.30. Four terminal structure for measuring contact resistance. After [71].

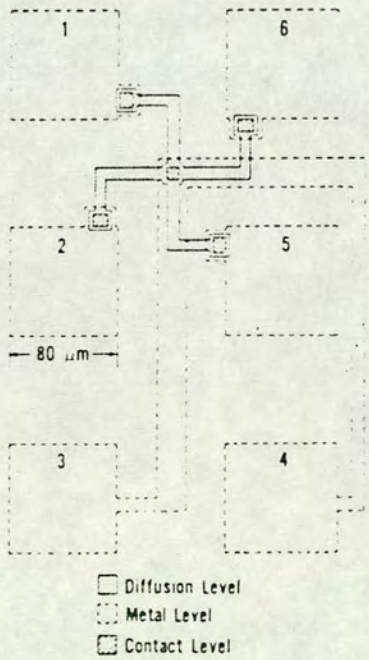


Figure 3.31. Six terminal structure for measuring contact resistance. After [71].

3.4. Other Structures for Process Parameter Extraction

As well as sheet resistance, linewidth, misalignment and contact resistance structures other devices which can be used or adapted to yield processing information include MOS capacitors from which oxide thickness, interface state measurements, flat band voltages and dopant density information can be derived. These measurements would most simply and quickly be achieved by using C-V measurements of a type which would require the use of specialised C-V equipment [72,73]. Diodes may be included to assess leakage currents as may MOSFETs for dopant profile examination [74].

3.5. Transistors

Individual transistors are commonly included on test chips. These can be used to find threshold voltages, breakdown voltages and transistor transconductance. If a number of transistors are included these may be used to extract more generalised parameters which will predict functional circuit performance such as SPICE [75,76]. Many programs exist to extract these parameters examples being SIMPAR [77], SUXES [78], TECAP [79], MOSFIT [80], TOPEX [81] and PARAMEX [82] although there are many more and almost every producer of parametric test equipment utilises a different software package for such work. For example TECAP by Hewlett Packard, MOSFIT by Keithley, TOPEX by TMA.

Extraction of transistor parameters can be both time consuming and can use up large areas of silicon if a transistor array is used. Speeding up testing is possible by taking a limited number of data points and fitting a polynomial of appropriate degree to these points, as indicated by Hamer [83]. Extraction of SPICE level 3 parameters by this method has shown that as little as 28 data points may be needed to extract a full parameter set [84].

To address arrays of MOSFETs addressable decoders have been used to access individual transistors [22,85-87] and a contribution to this subject area is reported in this thesis.

3.6. Area Structures

3.6.1. Introduction

Area structures can be utilised for a number of different purposes. These include reliability, design rule and random fault/yield analysis. Some area test structures may be used in more than one of these categories depending on the application. For example a comb resistor structure might be used for evaluating feature to feature spacing (design rules), in evaluating etch quality (random fault) or electromigration (reliability).

3.6.2. Reliability Analysis Structures

The main reliability problems in MOS devices have been stated as the following [88],

(1) Interconnect and contact failures (corrosion, electromigration and contact failures).

(2) Gate oxide failure (intrinsic breakdown, time dependent breakdown and hot-electron trapping).

(3) Substrate related failures (radiation induced logic errors and latch-up).

Structures are used to identify failure mechanisms that occur from physical changes to test circuits which can then be correlated to functional circuits. All of these structures measure the change in a parameter after a certain period of environmental overstress has been placed on the device. Overvoltage, high temperature, humidity and radiation can all cause device aging and/or failure and can be tested for using these structures. Overstressing a device can simulate long term device operation in a shorter period and obviously depends on a good physical model of the failure mechanism existing. Dielectric breakdown can be investigated by a large area MOS capacitor [12]. Other oxide properties can be investigated using MOSFETs including properties such as charge injection, surface charge spreading and ion migration [12]. Serpentine and comb resistor structures as depicted in figure 3.32 can be used to investigate metalisation faults such as electromigration and corrosion [12].

3.6.3. Yield Structures

These structures are designed to locate and identify physical faults due to processing errors, before the test circuit is subject to normal operating stress [89]. Structures which have been used for this purpose include serpentine resistors for metal step coverage analysis, comb resistors for looking at the etch quality between polysilicon and metal lines [90,91],

MOS capacitors for oxide integrity [92] and addressable arrays of MOSFETs (SRAMs) [93] for accumulation of fault statistics. A problem of all area test structures is that the fault the structure is designed to detect may not be the reason that the structure gives a 'fail' when tested. For example the serpentine resistor which is intended to 'fail' due to an open circuit of a metal step may also give a fail due to an error in layer definition (lithography error) or by poor probe contact during testing. This can only be circumvented by visual inspection of each failure, but this is time consuming especially for the large arrays necessary for this work. To reduce the amount of work required for this an addressable MOSFET array was developed, shown by figure 3.33, which had 100 MOSFETs in an array each with the gate connected to the drain. This structure has the advantage that that the fault locations are pinpointed and searching of large areas for faults is not required. The disadvantage is that testing time is much longer and a smaller number of elements can be examined for a given area, as well as a large number of pads being required. The number of elements, the speed of testing and the area of chip tested can all be improved by the use of decoders to address each individual transistor [86]. The corollary of this is that the decoder must be shown to work before any meaningful results can be taken. To ensure this the decoders must be designed with very conservative design rules.

3.6.4. Design Rule Structures

Structures to evaluate the geometrical rules which govern the layout for circuit design are essentially adaptations of structures which have been outlined already [96]. Linewidth and misalignment information must be incorporated into design rules and any of the structures outlined in the respective sections, on measurement of these parameters, may be used. Feature to feature spacing is another parameter present in the design rules and this can be investigated using comb resistors. Optimisation of a design rule parameter can be achieved by designing a set of structures with a crucial design rule parameter varied and then investigating the yield and reliability of the differing structures.

3.7. Circuit Parameter Extraction

Test circuits can also be included to check that the process is capable of producing a functional circuit [19]. A common circuit to include is a ring oscillator which gives an idea of the potential stage delay and circuit oscillation frequency. An inverter circuit may be included to determine inverter gain, threshold and noise immunity. Full characterisation of

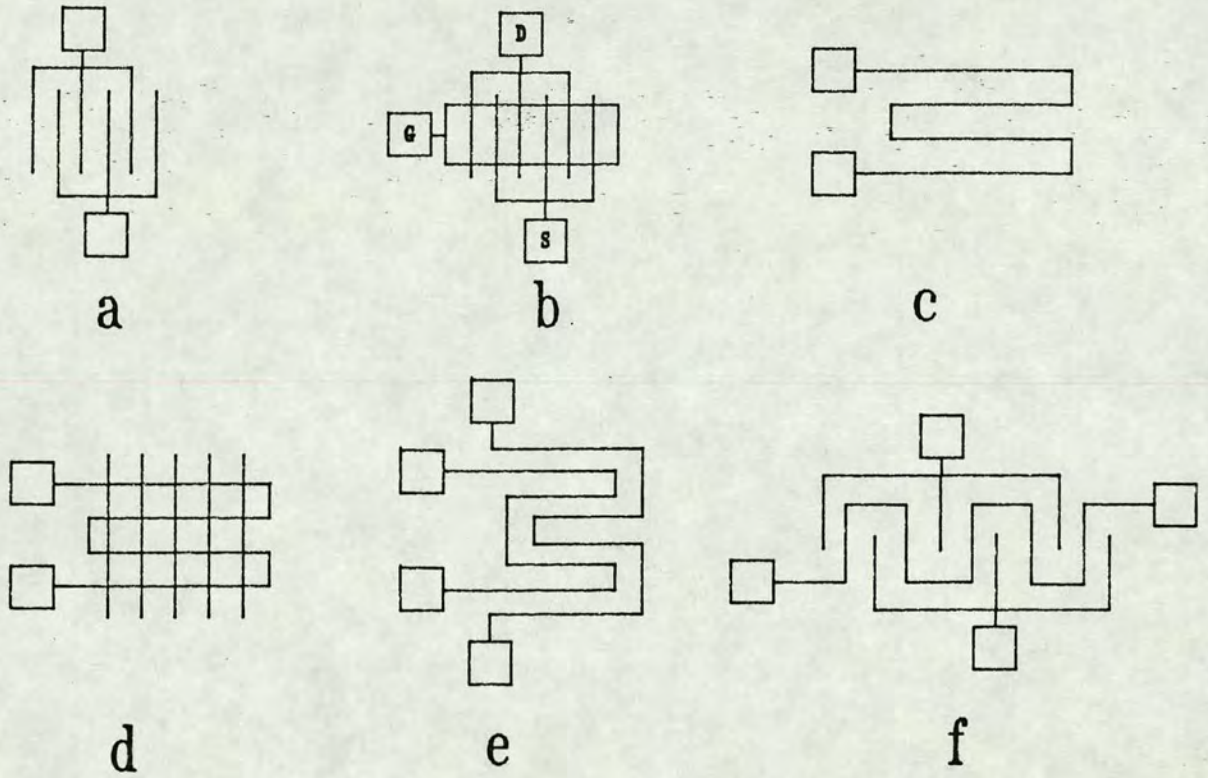


Figure 3.32. Schematic diagrams of comb and serpentine resistors showing a) comb resistor, b) comb MOSFET, c) serpentine resistor, d) serpentine step coverage resistor, e) serpentine comb resistor and f) serpentine comb resistor.

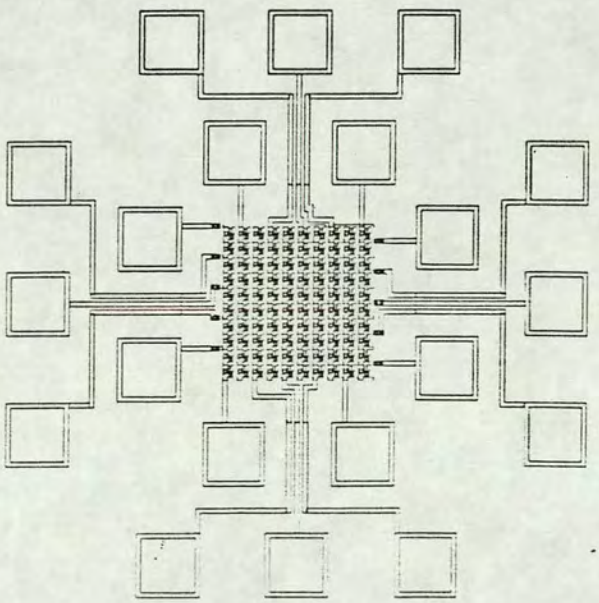


Figure 3.33. An addressable MOSFET array. After [15].

any test circuits might include evaluation of parameters such as power dissipation, maximum clock frequency and fan out. Addressable circuit elements have also been recently developed for this application, specifically for CMOS inverters [97] and for measuring circuit delay time [98].

3.8. Parametric Testers

3.8.1. Evolution of Test Systems

Before the mid seventies there were few commercially available automatic parametric testers. Measurements on PCC test structures were made manually on home made equipment or by using 'add-ons' to functional testers. These techniques were limited in speed and flexibility so few measurements could be made per die per batch [99]. The first parametric test system was marketed in 1975. This was the by the Lomac Corporation and was the Lomac LM-80 model, a single user system running on an 8-bit microprocessor. Data collection was at the rate of 1 to 10 results per second and mass storage of these took place on floppy disc. Although the potential of these machines was clear they were still thought of as 'automated curve-tracers' [100]. As engineers saw the benefits of these dedicated testers, more and better test systems became available to fulfil their needs as Keithley Instruments and Accutest entered the market in the late 1970's. Second generation parametric test equipment became available around 1980. These ran on 16 bit minicomputers with multi-task, multi-user capability and measurement speed was increased by an order of magnitude. In 1983 the Eaton Corporation and Hewlett-Packard also entered the now rapidly expanding market.

Since then updates in microcomputer power have increased tester speed and data handling ability, but the essentials of a test system have not changed drastically. The essentials of a parametric test system were espoused as early as 1978 by Howard and Nahourai and consisted of the following [101],

(1) Sources: voltage, current.

(2) Measuring Instruments: voltage, current (today a capacitance meter would be included).

(3) Switching matrix.

(4) CPU.

(5) I/O terminal.

(6) Operator console.

(7) Disk storage.

(8) Comprehensive software.

These were organised as depicted in figure 3.34. The instrumentation system must be capable of applying voltage and current sources to any pins of the device under test (DUT) and of connecting the voltage, current and capacitance meters similarly. For MOS device analysis three voltage sources and one current source is the normal configuration while bipolar work requires two sources of each kind. The instruments are connected to the DUT via a fully Kelvin switching matrix which, along with shielding and guarding of wiring, reduces errors due to voltage drops and noise. All these elements (instruments and matrix) are under the control of a microcomputer which, as well as running data extraction software, can be used for data analysis, storage and retrieval. These system 'essentials' have been taken on board by many manufacturers each of whom produces their own test system and choice between rival systems can be difficult. Over the years several authors have tried to evaluate systems and to rationalise user requirements, although these are obviously subjective choices and dependent on user needs [102-105].

Today parametric testers are currently most used in the spheres of process monitoring and device measurement. This is due to the increasing emphasis on quality and reliability of the final product which requires ever tighter processing and device parameters for smaller process geometries. Parametric testing is also following the trends of the semiconductor industry as a whole and is moving towards increased automation within that environment. One example of this is the use of 'expert systems' to analyse data from test chips thereby excluding the need for data inspection and analysis by a human 'expert' [106-108]. This area promises the 'ultimate' solution to yield management, where a computerised monitor would analyse all parametric test data for consistencies and inconsistencies, indicate where potential problems lie, and make correlations between the test data, device structure, processing steps and processing equipment. It would then offer advice as to possible causes of problems and suggested solutions to these. This was stated simply by Cresswell who stated "(the expert system) emulates what the human engineer is doing, but it's emulating it much more quickly and has a much higher capacity memory"

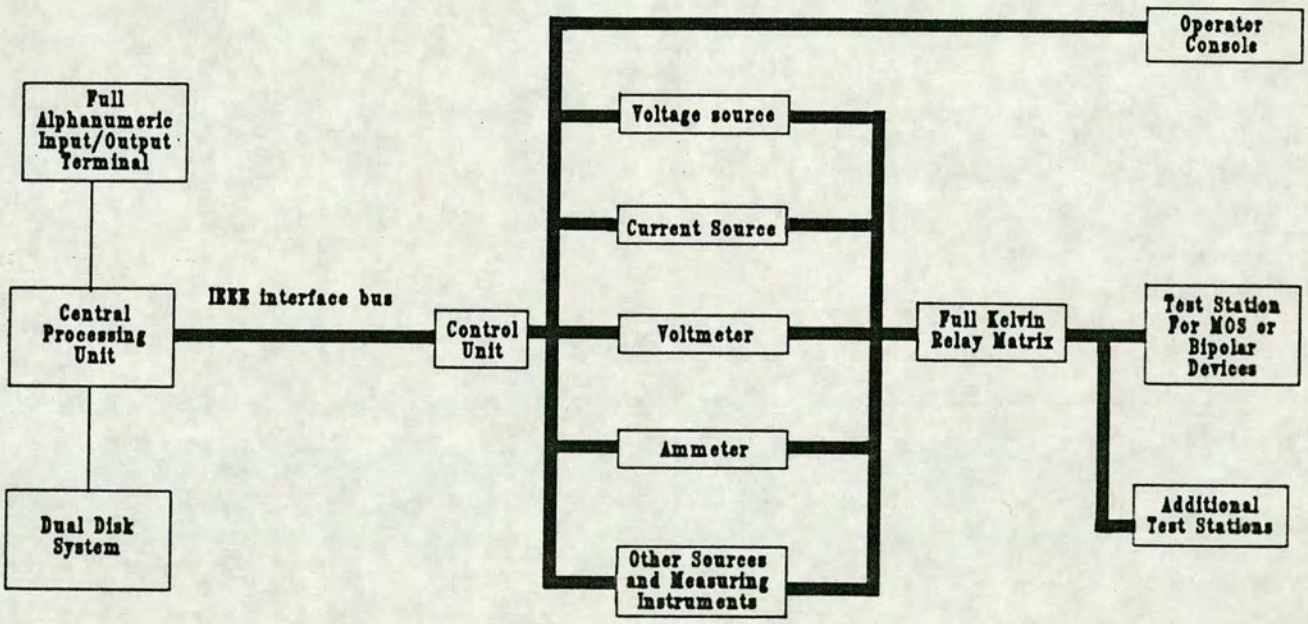


Figure 3.34. Organisation of parametric test system essential components.

[109]. Parametric test data is also well suited for incorporation into a complete computer integrated manufacturing system (CIM), which allows test data to be sent to a central CIM computer where comparisons with other, particularly process, data can speed information feedback for the engineer [110-112]. Yield problems can then be quickly related to process problems by product engineers.

3.8.2. Existing Test Systems

System specifications for parametric testers have not radically changed since first generation testers and consist of test instruments, switching matrix, test head/wafer prober (for packaged devices/wafers) perhaps incorporating a hot/cold chuck, test computer, software library and computer peripherals.

Instrument performance for a standard parametric tester has been stated by Jorgenson of Accutest as follows [105]. Voltage forcing instruments must be capable of forcing from several hundred *Volts* down to around $1mV$ with voltage measurement extending down to the few μV level. Current forcing must extend from a few hundred mA to below $1nA$ with measurements down to a pA or less. Resolution and accuracy of about 0.1% of the measured values is sufficient for most applications. The instruments and matrix should be sufficiently flexible to allow all instruments to be accessed by all the pins.

Improvements in tester hardware have improved throughput in response to the need to acquire more data in a shorter period. This has been achieved by the increase in speed and power of computer controllers and the shorter data acquisition times of the instruments due to the faster speeds of the A/D and D/A converters that they use. Major improvements in computer systems have been reflected in the choice of computer to act as system controller. These have generally been one of a small number of PC/small workstations which have been configured to work in the parametric test environment [113]. Prior to 1986 the typical parametric test system would have been configured with one of the following PCs, IBM PC, HP 9000/236 or PDP-11. These have been superseded by those including the Apollo DOMIAN series 3000, COMPAQ 386, IBM PC-XT, IBM PC-AT, HP 9000/310, MicroVAX II and SUN 3/100 series workstations. The controller used in any given system will depend on the desired use of the computer although most systems come semi dedicated with a computer. Factors such as speed of operation, ease of program writing and need for multi-station testing are all important. Tester manufacturers normally supply certain low

level software routines for instrument connection and data analysis which can be built up by the user to form more complex programs, e.g. to extract threshold voltage.

3.8.3. Integrated Parametric Testers

These offer a cheaper and less costly method of extracting parametric data than from a 'full' test system. These testers have an integrated form incorporating instrumentation, computer hardware/software and switching matrix in one 'box'. They are capable of certain low level measurements and data storage but can normally be configured so that they may be controlled by an external PC/workstation if required. An example of this type of tester is the HP 4145. This may be used as a simple 'stand alone' tester or may be operated under PC control for more sophisticated tasks.

Wafer probers are another, often overlooked, aspect of the hardware of a test system [114]. Probing speed can affect throughput, but modern probers are now generally fast enough so that mechanical scanning takes only a small percentage of the testing time. A large number of manufacturers supply probers and the user can choose an appropriate prober ranging from the simple to the fully automated.

3.8.4. Data Processing

This is perhaps the most important aspect of parametric testing. As stated by Lukasek of Stanford University, "Automated parametric testers can just drown you in numbers" [109]. Hence it is seen that the evaluation and swift analysis of the data accumulated is of paramount importance if parametric test is to have a meaningful role [5,115]. Handling of data can be difficult as parameters are location dependent. Difficulties occur in averaging results, in identifying outliers and in correlating parameters. This can be a problem especially if production wafers only have a few test chips not all of which may be tested, resulting in insufficient data being collected to see problems. To address this statistical evaluation of test data has been performed, particularly to try and evaluate test chip sample size (4-5 per wafer) with the spread of a parameter across a wafer [116,117]. Although the number of die required to accurately measure a parameter will depend on its spread across a wafer, this in turn ultimately being process dependent.

Data acquired may have a limited amount of manipulation done locally on the parametric tester, before being sent to either the CAM database (if one exists) or to some

other computer capable of data analysis. Analysis of data can take many forms and easy interpretation of results is of obvious importance for the engineer. Analysis may use wafer and vector maps, scatter plots, trend charts, histograms, box plots, 3-D plots and control chart generation.

References

1. M.G. Buehler, "The Use of Electrical Test Structures Arrays for Integrated Circuit Process Evaluation," *J. Electrochem. Soc.*, vol. 127, no. 10, pp. 2284-2290, October 1980.
2. D. Yen, L.W. Linholm, and M.G. Buehler, "A Cross-bridge Test Structure for Evaluating the Linewidth Uniformity of an Integrated Circuit Lithography System," *J. Electrochem. Soc.*, vol. 129, no. 10, pp. 2313-2318, October 1982.
3. C. Alcorn, D. Dworak, N. Haddad, W. Henley, and P. Nixon, "Kerf Test Structure Designs for Process and Device Characterization," *Solid State Technology*, pp. 229-235, May 1985.
4. D. Martin, "Parametric Testing," *SERC School on Microfabrication 1988*, pp. 16.1-16.17, Edinburgh, April 1988.
5. D.S. Perloff, T.F. Hasan, and E.R. Blome, "Real-time Monitoring of Semiconductor Process Uniformity," *Solid State Technology*, pp. 81-86, February 1980.
6. F.J. Barone and C.F. Myers, "Getting Beneath the Surface of Multilayer Integrated Circuits," *Electronics*, vol. 41, p. 84, July 1968.
7. G.L. Schnable and R.S. Keen, "Failure Mechanisms in Large-Scale Integrated Circuits," *IEEE Trans. on Electron Devices*, vol. ED-16, no. 4, pp. 322-332, April 1969.
8. R.J. Sahni, *Proc. of Reliability Phys. Symp.*, vol. 8, p. 226, 1970.
9. R.G. Tingley and D.W. Johnson, *Circuits Manufacturing*, vol. 17, p. 30, April 1977.
10. M.G. Buehler, "Comprehensive Test Patterns with Modular Test Structures: The 2 by N Probe-pad Array Approach," *Solid State Technology*, pp. 89-94, October 1979.
11. R.L. Mattis and M.R. Doggett, "A Microelectronic Test Pattern for Analyzing Automated Wafer Probing and Probe Card Problems," *Solid State Technology*, pp. 76-79, November 1978.

12. M.G. Buehler, "Microelectronic Test Chips for VLSI Electronics," in *VLSI Electronics : Microstructure Science*, ed. G.B. Larrabee, vol. 6, pp. 529-576, Academic Press, 1983. Chapter 9

13. U. Kaempf, "Automated Parametric Testers to Monitor the Integrated Circuit Process," *Solid State Technology*, pp. 81-87, September 1981.

14. A.J. Walton, "Process Monitoring and Control," *Proc. of EMF International Vacation School on VLSI Fabrication*, Edinburgh, 2-13th April 1984.

15. A.J. Walton, "Process Control Evaluation and Simulation - Part I," *Proc. Fourth Brazilian Workshop on Microelectronics*, pp. 1-14, Campinas, SP, Brazil, February-March 1983.

16. A.J. Walton, "Process Control Evaluation and Simulation - Part II," *Proc. Fourth Brazilian Workshop on Microelectronics*, pp. 121-135, Campinas, SP, Brazil, February-March 1983.

17. A.J. Walton, "Parametric Test as a Tool for Increasing Engineering Yield," *Proc. of International Workshop on Designing for Yield*, pp. A2/1-A2/10, Oxford, June-July 1987.

18. A.J. Walton and A. Gribben, "A Review of Parametric Testing," *Proc. of Semiconductor International Conference*, pp. 39-63, Birmingham, 29th September-1st October 1987.

19. R.T. Jerdonek, H.F. Bare, and G.J. Fromen, "The Use of a Silicon-gate C-MOS/SOS Test Vehicle to Evaluate Technology Maturity," *IEEE Trans. on Electron Devices*, vol. ED-25, no. 8, pp. 873-878, August 1978.

20. D. Takács, W. Müller, and U. Schwabe, "Electrical Measurement of Feature Sizes in MOS Si^2-Gate VLSI Technology," *IEEE Trans. on Electron Devices*, vol. ED-27, no. 7, pp. 1368-1373, August 1980.

21. R. Zucca, B.M. Welch, C-P. Lee, R.C. Eden, and S.I. Long, "Process Evaluation Test Structures and Measurement Techniques for a Planar GaAs Digital IC Technology," *IEEE Trans. on Electron Devices*, vol. ED-27, no. 12, pp. 2292-2298, December 1980.

22. M.G. Buehler, B.T. Moore, and R.H. Nixon, "Parameter Extraction from Spaceborne MOSFETs," *IEEE Trans. on Nuclear Science*, vol. NS-32, no. 6, pp.

4237-4243, December 1985.

23. T. Ekstedt, K. Cham, T. Harms, V. Konrad, H.Sugawara, G. Modrell, U. Kaempf, and J. Nowell, "A Parametric Test/Analysis System for VLSI Process Development," *Proc. IEEE VLSI Workshop on Test Structures*, pp. 529-535, Long Beach, California, February 1986.

24. T.J. Russell, D.B. Maxwell, C.T Reimann, and M.G. Buehler, "A Microelectronic Test Pattern for Measuring Uniformity of an Integrated Circuit Fabrication Technology," *Solid State Technology*, pp. 71-74, February 1979.

25. M.G. Buehler, L.W. Linholm, V.C. Tyree, R.A. Allen, B.R. Blaes, G.A. Jennings, and K.A. Hicks, "CMOS Process Monitor," *Proc. of the 1988 International Conference on Microelectronic Test Structures (ICMTS)*, vol. 1, no. 1, pp. 164-168, Long Beach, California, February 1988.

26. M.G. Buehler, T.W. Griswold, C.A. Pina, and C. Timoc, "Test Chips for Custom ICs," *Circuits Manufacturing*, vol. 22, pp. 36-42, June 1982.

27. D.S. Perloff, F.E. Wahl, C.L. Mallory, and S.W. Mylroie, "Microelectronic Test Chips in Integrated Circuit Manufacturing," *Solid State Technology*, pp. 75-80, September 1981.

28. M.G. Buehler and L.W. Linholm, "Toward a Standard Test Chip Methodology for Reliable, Custom Integrated Circuits," *Proc. of 1981 Custom Integrated Circuits Conference*, pp. 142-146, May 1981.

29. M.G. Buehler and W.R. Thurber, "A Planar Four-probe Test Structure for Measuring Bulk Resistivity," *IEEE Trans. on Electron Devices*, vol. ED-23, no. 8, pp. 968-974, August 1976.

30. L.J. van der Pauw, "A Method of Measuring Specific Resistivity and Hall Effect of Discs of Arbitrary Shape," *Philips Research Reports*, vol. 13, no. 1, pp. 1-9, February 1958.

31. L.J. van der Pauw, "A Method of Measuring the Resistivity and Hall Coefficient on Lamellae of Arbitrary Shape," *Philips Technical Review*, vol. 20, no. 8, pp. 220-224, 1958/59.

32. R. Chwang, B.J. Smith, and C.R. Crowell, "Contact Size Effects on the Van Der Pauw Method for Resistivity and Hall Coefficient Measurement," *Solid-State*

Electronics, vol. 17, pp. 1217-1227, 1974.

33. J.M. David and M.G. Buehler, "A Numerical Analysis Of Various Cross Sheet Resistor Test Structures," *Solid-State Electronics*, vol. 20, pp. 539-543, 1977.

34. W. Versnel, "Analysis of the Greek Cross, a Van der Pauw Structure with Finite Contacts," *Solid-State Electronics*, vol. 22, pp. 911-914, 1979.

35. M.G. Buehler and W.R. Thurber, "An Experimental Study of Various Cross Sheet Resistor Test Structures," *J. Electrochem. Soc.*, vol. 125, no. 4, pp. 645-650, April 1978.

36. F.M. Smits, "Measurement of Sheet Resistivities with the Four-point Probe," *The Bell System Technical Journal*, May 1958.

37. D.S. Perloff, F.E. Wahl, and J. Conragan, "Four-point Sheet Resistance Measurements of Semiconductor Doping Uniformity," *J. Electrochem. Soc.*, vol. 124, no. 4, pp. 582-590, April 1977.

38. D.A. Swyt, *Solid State Technology*, vol. 19, p. 55, April 1976.

39. W.E. Ham, *Semiconductor Measurement Technology : NBS Special Publication*, no. 400-15, pp. 25-34, January 1976.

40. M.G. Buehler, S.D. Grant, and W.R. Thurber, "Bridge and van der Pauw Sheet Resistors for Characterizing the Line Width of Conducting Layers," *J. Electrochem. Soc.*, vol. 125, no. 4, pp. 650-654, April 1978.

41. Prometrix, "An Overview of Lithography Characterization," in *Prometrix Lithomap User Manual, Chapter 2*.

42. D. Yen, "Electrical Test Methods for Evaluating Lithographic Processes and Equipment," *Proc. of SPIE*, vol. 342, Integrated Circuit Metrology, pp. 73-81, 1981.

43. R. Patrick and B. Arden, "Using Electrical Linewidth Metrology To Characterize Plasma Etching," *Microelectronic Manufacturing and Testing*, pp. 25-26, May 1987.

44. R. Patrick and B. Arden, "Plasma Etch Characterization Using Electrical Linewidth Measuring Techniques," *SPIE*, vol. 775, Integrated Circuit Metrology, Inspection and Process Control, pp. 210-216, 1987.

45. F.E. Wahl and D.S. Perloff, "Techniques for the Evaluation and Display of VLSI Process Uniformity," *Proc. Microelectronics Measurement Technology Seminar*, San Jose, California, February 1979.

46. D.S. Perloff, F.E. Wahl, and J.D. Reimer, "Contour Maps Reveal Non-uniformity in Semiconductor Processing," *Solid State Technology*, pp. 31-42, February 1977.

47. P.H. Singer, "Life on the Edge: Measuring Critical Dimensions," *Semiconductor International*, pp. 84-87, December 1988.

48. R. Stein, D.H. Cummings, and J.A. Schaper, "Calibrating Microscopic Linewidth Measurement Systems," *Semiconductor International*, pp. 132-136, April 1986.

49. N.E. David and H.L. Stover, "Optical Test Structures for Process Control Monitors, Using Wafer Stepper Metrology," *Solid State Technology*, pp. 131-141, June 1982.

50. V.J. Coates, "Computerized Optical System for Precision Line Width Measurements," *Proc. Microelectronics Measurement Technology Seminar*, San Jose, California, February 1979.

51. C. Murray, "Measurement Tools for Overlay Registration," *Semiconductor International*, pp. 62-68, February 1987.

52. D.S. Perloff, "A Four-point Electrical Measurement Technique for Characterizing Mask Superposition Errors on Semiconductor Wafers," *IEEE Journal of Solid-State Circuits*, vol. SC-13, no. 4, pp. 436-444, August 1978.

53. T.F. Hasan, S.U. Katzman, and D.S. Perloff, "Automated Electrical Measurements of Registration Errors in Step-and-Repeat Optical Lithography Systems," *IEEE Trans. on Electron Devices*, vol. ED-27, no. 12, pp. 2304-2312, December 1980.

54. K.L. Harris, S. Miyauchi, and T. Namae, "Applications of a High-speed, High-resolution Metrology System," *Microelectronic Manufacturing and Testing*, pp. 54-55, May 1987.

55. E.J. Sprogis, "An Overlay Vernier and Process Bias Monitor Measured by Voltage Contrast SEM," *Proc. of the 1989 International Conference on Microelectronic Test Structures (ICMTS)*, vol. 2, no. 1, pp. 129-132, Edinburgh, March 1989.

56. T.J. Russell, T.F. Leedy, and R.L. Mattis, "A Comparison of Electrical and Visual Alignment Test Structures for Evaluating Photomask Alignment in Integrated Circuit Manufacturing," *IEDM Technical Digest*, pp. 7A-7F.

57. I J. Stemp, K.H. Nicholas, and H.E. Brockman, "Automatic Testing and Analysis of Misregistrations Found in Semiconductor Processing," *IEEE Trans. on Electron Devices*, vol. ED-26, no. 4, April 1979.

58. K.H. Nicholas, I.J. Stemp, and H.E. Brockman, "Measurement and Identification of Distortion, Alignment and Mask errors in IC Processing," *J. Electrochem. Soc.*, vol. 128, no. 3, pp. 609-614, March 1981.

59. D.S. Perloff, "A Van Der Pauw Resistor Structure for Determining Mask Superposition Errors on Semiconductor Slices," *Solid-State Electronics*, vol. 21, pp. 1013-1018, 1978.

60. D.S. Perloff, "Four-point Sheet Resistance Correction Factors for Thin Rectangular Samples," *Solid State Electronics*, vol. 20, pp. 681-687, 1977.

61. J.M. Dikeman and K.P. Roenker, "A Performance Comparison of the Alignment Resistor and Modified Van der Pauw Misregistration Test Structures," *Proc. of IEEE VLSI Workshop on Test Structures*, pp. 51-66, Long Beach, California, February 1986.

62. M. Jian, "A Test Structure to Measure the Misalignment Between Poly-Si and Diffusion Layers," *Proc. of the 1988 International Conference on Microelectronic Test Structures (ICMTS)*, vol. 1, no. 1, pp. 204-206, Long Beach, California, February 1988.

63. M. Lozano, C. Cané, E. Cabruja, I. Gràcia, and E. Lora-Tamayo, "Measurement of Misalignment Using a Triangular MOS Transistor," *Proc. of the 1989 International Conference on Microelectronic Test Structures (ICMTS)*, vol. 2, no. 1, pp. 139-142, Edinburgh, March 1989.

64. R. Yamaguchi, K. Komatsu, S. Moriya, and K. Harada, "Integrated Electrical Vernier to Measure Registration Accuracy," *IEEE Electron Device Letters*, vol. EDL-7, no. 8, pp. 463-464, August 1986.

65. G. Freeman and W. Lukaszek, "An Electrical Test Structure for Measuring Contact Size," *Proc. of the 1988 International Conference on Microelectronic Test Structures (ICMTS)*, vol. 1, no. 1, pp. 9-14, Long Beach, California, February 1988.

66. G. Freeman, W. Lukaszek, T.W. Ekstedt, and D.W. Peters, "Experimental Verification of a Novel Electrical Test Structure for Measuring Contact Size," *IEEE Trans. on Semiconductor Manufacturing*, vol. 2, no. 1, pp. 9-15, February 1989.

67. A.J. Walton, W.R. Gammie, R. Holwill, and B.M.M. Henderson, "Digital Measurement of Polysilicon to Diffusion Misalignment for a Silicon Gate MOS Process," *Electronics Letters*, vol. 20, no. 23, pp. 951-952, 8th November 1984.

68. B.M.M. Henderson, A.M. Gundlach, and A.J. Walton, "Integrated-circuit Test Structure Which Uses a Vernier to Electrically Measure Mask Misalignment," *Electronics Letters*, vol. 19, no. 21, pp. 868-869, 13th October 1983.

69. B.M.M. Henderson and A.J. Walton, "A Complete Digital Vernier Tool for the Measurement of Mask Misalignment," *Proc. of IEEE VLSI Workshop on Test Structures*, pp. 34-49, Long Beach, California, February 1986.

70. H.H. Berger, "Contact Resistance And Contact Resistivity," *J. Electrochem. Soc.*, vol. 119, no. 4, pp. 507-514, April 1972.

71. S.J. Proctor, L.W. Linholm, and J.A. Mazer, "Direct Measurements of Interfacial Contact Resistance, End Contact Resistance, and Interfacial Contact Layer Uniformity," *IEEE Trans. of Electron Devices*, vol. ED-30, no. 11, pp. 1535-1542, November 1983.

72. K.H. Zaininger and F.P. Weiman, "The C-V Technique as an Analytical Tool: Part 1," *Solid State Technology*, pp. 49-56, May 1970.

73. K.H. Zaininger and F.P. Weiman, "The C-V Technique as an Analytical Tool: Part 2," *Solid State Technology*, pp. 46-55, June 1970.

74. M.G. Buehler, "Dopant Profiles Determined from Enhancement-mode MOSFET dc Measurements," *Appl. Phys. Lett.*, vol. 31, no. 12, pp. 848-850, December 1977.

75. L.W. Nagel, "SPICE 2 : A Computer Program to Simulate Semiconductor Circuits," *Memo. No. UCB/ERL M510*, Electronics Research Laboratory, College of Engineering, University of California, Berkley, May 1975.

76. A. Vladimirescu and S. Liu, "The Simulation of MOS Integrated Circuits Using SPICE 2," *Memo. No. UCB/ERL MBO/7*, Electronics Research Laboratory, College of Engineering, University of California, Berkley, February 1980.

77. W. Maes, K. De Meyer, and L. Dupas, "SIMPAR: A Parameter Extraction Program to be used for any User-defined Analytical Expression in the Field of Process and Device Modelling," *Proc. of 15th European Solid State Device Research Conference, ESSDERC 85*, pp. 153-154, Aachen, September 1985.

78. K. Doganis and D.L. Scharfetter, "General Optimization and Extraction of IC Device Model Parameters," *IEEE Trans. Electron Devices*, vol. ED-30, no. 9, pp. 1219-1228, September 1983.

79. E. Khalily, P. Decher, and A. Darell, "TECAP 2: An Interactive Device Characterization and Model Development System," *Hewlett Packard Technical Data*, 1985.

80. A.L. Silburt, "Automated Parameter Extraction and Modelling of the MOSFET below Threshold," *Proc. of 15th European Solid State Device Research Conference, ESSDERC 85*, pp. 160-161, Aachen, September 1985.

81. C.A. Bloom, *1986 Product Seminar,* TMA, Palo Alta, 26th August 1986.

82. A. Gribben, J.M. Robertson, and A.J. Walton, "Accurate Physical Parameter Extraction for Small Geometry Devices," *Proc. of Semiconductor International Conference (SEMICON)*, pp. 186-202, Birmingham, 1986.

83. M.F. Hamer, "First Order Parameter Extraction on Enhancement Silicon MOS Transistors," *IEE Proc.*, vol. 133, no. 2, pp. 49-54, April 1986.

84. P. Tuhoy, A.J. Walton, and J.M. Robertson, Fast Extraction of Level 3 SPICE Parameters, University of Edinburgh, Dept. of Elec. Eng., Internal Report.

85. M.G. Buehler, "JMOSFIT : A MOSFET Transistor Parameter Extractor," *Proc. of IEEE VLSI Workshop on Test Structures*, pp. 475-496, Long Beach, California, February 1986.

86. A.J. Walton, J.M. Robertson, R. Holwill, and B. Moore, "On Chip Switching for DC Parametric Testing," *Electronics Letters*, vol. 21, no. 10, pp. 422-423, May 1985.

87. A. Nishimura, S.S. Mahant Shetti, J. Givens, E. Born, R. Haken, R. Chapman, and P. Chaterjee, "Multiplexed Test Structure ; A Novel VLSI Technology Development Tool," *Proc. of IEEE VLSI Workshop on Test Structures*, pp. 336-355, Long Beach, California, February 17-18, 1986.

88. F. Fantini and G. Soncini, "MOS Integrated Circuits Reliability," *Proc. of EMF International Vacation School on VLSI Fabrication*, Edinburgh, 2-13th April 1984.

89. M.A. Mitchell, "Defect Test Structures for Characterization of VLSI Technologies," *Solid State Technology*, pp. 207-213, May 1985.

90. P. Gill and K. Dillenbeck, "Using Snake Patterns to Monitor Defects and Enhance VLSI Device Yields, Part One," *Microcontamination*, pp. 23-60, February 1989.

91. P. Gill and K. Dillenbeck, "Using Snake Patterns to Monitor Defects and Enhance VLSI Device Yields, Part Two," *Microcontamination*, pp. 33-60, March 1989.

92. M.G. Buehler, B.R. Blaes, C.A. Pina, and T.W. Griswold, "Pinhole Array Capacitor for Oxide Integrity Analysis," *Solid State Technology*, pp. 131-137, November 1983.

93. H.G. Parks, C.E. Logan, and C.A. Fahrenz, "Use SRAMs and Test Structures as Yield Monitors," *Semiconductor International*, pp. 132-135, April 1989.

94. L.W. Linholm, "The Design, Testing and Analysis of a Comprehensive Test Pattern for Measuring CMOS/SOS Process Performance and Control," *Semiconductor Measurement Technology : NBS Special Publication*, no. 400-66, August 1981.

95. M.G. Buehler and L.W. Linholm, "Role of Test Chips in Coordinating Logic and Circuit Design and Layout Aids for VLSI," *Solid State Technology*, pp. 68-74, September 1981.

96. C. Kooperberg, "Circuit Layout and Yield," *IEEE Journal of Solid-state Circuits*, vol. 23, no. 4, pp. 887-892, August 1988.

97. M.G. Buehler and H.R. Sayah, "Addressable Inverter Matrix for Process and Device Characterisation," *Solid State Technology*, pp. 185-191, May 1985.

98. B.R. Blaes, "CMOS Timing Sampler Array for Measuring Circuit Delays," *Proc. of IEEE VLSI Workshop on Test Structures*, pp. 208-227, Long Beach, California, February 1986.

99. G.G. Evans, "Semiconductor Parametric Testing : Yesterday, Today and Tomorrow," *Semiconductor Production*, pp. 8-17, April/May 1982.

100. G. Evans, "Parametric Testing for LSI/VLSI," *Microelectronic Manufacturing and Testing*, pp. 24-25, January 1983.

101. J.S. Howard and J. Nahourai, "Production Using an Automated Parametric Test System," *Solid State Technology*, pp. 48-52, July 1978.

102. C. Chrones, "Parametric Test Systems for Wafer Processing," *Semiconductor International*, pp. 113-122, October 1980.

103. C. Chrones, "Parametric Testers Evaluate Wafer Processing," *EDN*, pp. 117-122, 15th April 1981.

104. M. Levis, "System Comparisons can Simplify Selection of Parametric Tester," *Electronics*, January 1984.

105. P.H. Singer, "Parametric Test System Update," *Semiconductor International*, pp. 84-90, September 1983.

106. J.Y.-C. Pan and J.M. Tenenbaum, "PIES: An Engineer's Do-it-yourself Knowledge System for Interpretation of Parametric Test Data," *AI Magazine*, vol. 7, no. 4, pp. 62-71, Fall 1986.

107. M.W. Cresswell, L.R. Lowry, and M.H. Hanes, "Generating Expert-system Diagnostic Rules from Parametric Test-structure Data," *Microelectronic Manufacturing and Testing*, pp. 16-18, May 1988.

108. M.E. Zaghloul, D. Khera, L.W. Linholm, and C.P. Reeve, "A Machine-learning Classification Approach for IC Manufacturing Control Based on Test Structure Measurements," *IEEE Trans. on Semiconductor Manufacturing*, vol. 2, no. 2, pp. 47-53, May 1989.

109. P.H. Singer, "Analyzing Parametric Test Structures," *Semiconductor International*, pp. 74-79, June 1987.

110. J. Gililland and A. Ligtenberg, "Automated Semiconductor Wafer Processing," *Microelectronic Manufacturing and Testing*, pp. 46-47, April 1983.

111. O. Melstrand, E. O'Neill, G.E. Sobelman, and D. Dokos, "A Data Base Driven Automated System for MOS Device Characterization, Parameter Optimization and Modeling," *IEEE Trans. on Computer-Aided Design*, vol. CAD-3, no. 1, pp. 47-51, January 1984.

112. J. Harvey and E. Dyatlovitsky, "Automation of Parametric Testing in Semiconductor IC Manufacturing," *Microelectronics Manufacturing and Testing*, pp. 11-13, March 1988.

113. D.A. Angst and J. Domitrowich, "Trends in Parametric Test Systems," *Semiconductor International*, pp. 173-177, September 1987.

114. A. Weiss, "Update on Wafer Probing Systems and Accessories," *Semiconductor International*, pp. 67-78, May 1982.

115. J.M. Charles and M.W. Lantz, "Applications of High-Speed Data Acquisition for Bipolar Device-yield Analysis," *IEEE Trans. on Electron Devices*, vol. ED-27, no. 12, pp. 2299-2303, December 1980.

116. J.S. Suehle, L.W. Linholm, and K. Kafadar, "Minimum Test Chip Sample Size Selection for Characterizing Process Parameters," *IEEE Trans. on Electron Devices*, vol. ED-31, no. 2, February 1984.

117. L.W. Linholm, R.L. Mattis, R.C. Frisch, and C.P. Reeve, "Characterising and Analysing Critical Integrated Circuit Process Parameters," in *Semiconductor Silicon 1981*, ed. Y. Takeishi, pp. 906-920, Princeton, New Jersey.

Chapter 4

On-chip Switching: an Investigation

4.1. Introduction

As minimum geometries have shrunk and chip sizes increased the potential number of test structures on a typical PCC has also increased considerably. The main problem with this is that an increased area of silicon is required to accommodate the large number of extra probe pads. This increased number of probe pads also sets a requirement for a larger switching matrix on associated parametric test hardware which in turn increases tester cost and complexity. The use of a modular test structure design concept using a 2 × N pad array can help reduce this problem but at the cost of increased test chip area and testing time [1]. A more recent approach to this problem has been suggested whereby part of the switching process is placed on-chip and measurements are made using a hybrid digital parametric tester. Placing some of the switching on-chip also allows a significant improvement in speed. This is because the relay settling time in a parametric tester is typically of the order of milliseconds considerably slower than any transistor-based, on-chip system. The switching matrix structure can be thought of as a digital assist to an analogue measurement.

This idea has found a few previous exponents. The various approaches taken are now outlined.

4.2. Some Approaches to On-chip Switching

Placing switching elements on-chip and the use of addressable test structures has its origin in functional circuits such as random access memories (RAMs) and programmable logic arrays where such elements are routinely used to access a small part of an array of elements. Hence it was a natural progression to try to incorporate these ideas into the scope of parametric test and test structure layout. One of the first test structure designs to do this involved accessing clusters of transistors where the rows and columns were connected to individual probe pads [2]. This layout is illustrated by figure 4.1. The

addressing of each transistor is performed off-chip by the parametric tester's mechanical switching matrix. The number of transistors which can be accessed in this form is limited by the number of probe points accessible in one pass. For a typical 2 × 10 probe card this gives 100 (i.e. 10^2) possible elements or N^2 for a 2 × N card. The use of an addressable matrix increases the number of accessible elements for a given number of pads. Assuming that the addressing is performed digitally there is a large increase in number of probeable elements using this scheme. That number of elements being 2^n where n is the number of pads available for digital addressing. Table 4.1 illustrates this, assuming that six pads are required for the relevant voltage and current rails.

Number of Pads	Number of Probe Points	
	Row/Column Access	Multiplex Access
10	25	16
12	36	64
14	49	256
16	64	1024
18	81	4096
20	100	16384

Table 4.1. Comparison of number of probe points accessible for a given number of pads. Figures for both row/column and multiplex access are given.

One of the first applications of use of an on-chip decoder was a test chip design which made yield evaluations for contact chains and transistor arrays [3]. Figure 4.2 shows the layout for this chip. This only required quantitative measurements (i.e. an on/off measurement). The switching was achieved using two digitally addressed decoder units accessed via a hybrid digital parametric tester. The decoder circuitry was designed in a deliberately conservative manner so as to reduce the possibility of failure due to defects in the decoder to a minimum.

Arrays of CMOS inverters have also been investigated using multiplexed access [4]. This design consisted of an array of 222 inverters each accessible with the aid of a shift register stage. Each row of inverters could be accessed by one of the shift register stages and the commoned output from each column accessed by a separate pad. Both the measured DC characteristics of the inverters and the effect of several different processing faults were described. In particular the effect of undersize n-channel transistor widths and of open contacts were reported.

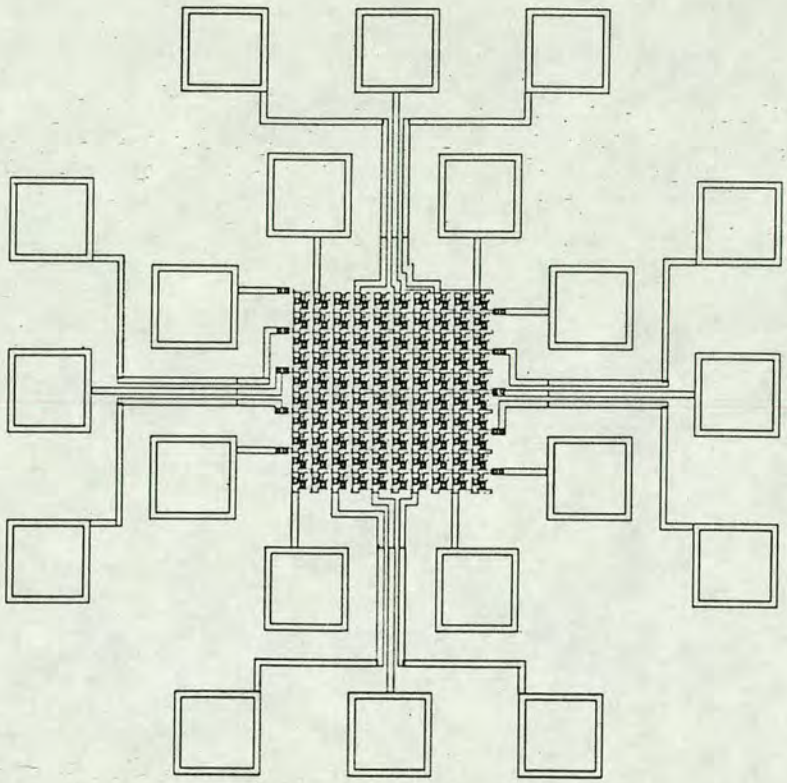


Figure 4.1. Array of 100 MOSFETs with row and column access via individual probe pads. After [2].

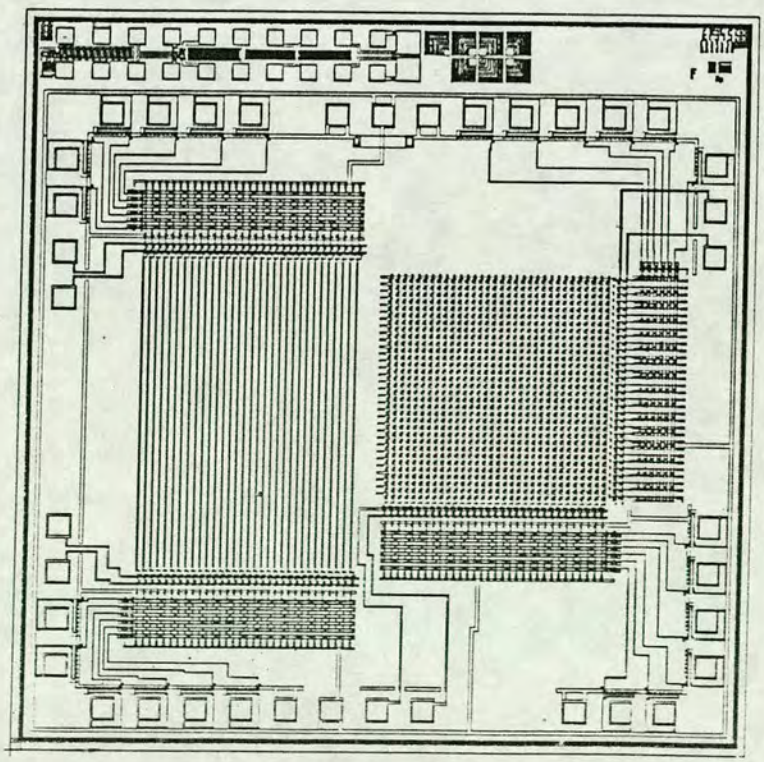


Figure 4.2. Chip by Moore with on-chip decoding to access test structures. After [3].

Addressable structures have also been featured in a CMOS timing sampler array for measuring circuit delays [5]. The timing sampler was used to measure circuit delays in a manner different from the 'traditional' ring oscillator. This allowed the circuit to respond to externally generated timing events (transitions) rather than to the internally generated oscillations of a ring oscillator circuit. The sampler consisted of 120 inverter chains each of which had a unique transistor geometry (i.e. length and width). Each inverter was again accessed via a multiplexer which itself was addressed digitally.

Some typical process control structures have been incorporated into addressable arrays. Nishimura *et al.* used row and column decoders to access several different types of commonly used test structures [6]. These included digital alignment structures in both X and Y directions, process maturity and design rule checker structures, contact chains, comb and serpentine resistors and a number of transistors (used to measure transistor uniformity). In all 1024 test sites could be accessed with both digital and analogue measurements performed. The latter being resistance measurements from contact chains and transistor current measurements.

Addressable row and column decoders have also been used by Buehler to help assess the circuit performance of transistors and to evaluate their radiation 'hardness' [7, 8]. Analogue measurements of the transistors were made via the decoding matrix. These measurements were for a specially derived transistor model which used a degree of optimisation to make the model parameters fit the extracted curves. Results reported gave good correlation between transistors tested individually and those accessed via the decoder.

4.3. Aim and Outline of Work

The work from which this thesis work developed was demonstrated by Moore [3]. As outlined in the section above this used decoders to make on/off measurements on transistors and contact chains. As depicted in figure 4.2 the left-hand side of the chip contains 32 contact chains and the multiplexers which allow access to a particular one of these are situated at the top and bottom of these chains. The right-hand side contains the array of 1024 diode connected MOSFETs. Again these are accessed by multiplexer of the same design. Each decoder address output line controls the gates of two pass transistors. One forms the test element connection to a current force/sense line, the other to a voltage force/sense line. Schematically the layout of this chip is depicted by figure 4.3. Access of a

contact chain or a MOSFET required the correct digital address for that element to be set on both decoder units inputs. All the decoder outputs except that for the element under test will be set low. A current can then be forced between the two current access pads and the voltage across the voltage pads measured and electrical continuity established.

The measurements discussed above are essentially of an on/off type. The aim of the work to be described was to develop this theme to enable analogue measurements to be made and, in particular, to obtain measurements from transistors. This involves accessing the transistors via decoders/multiplexers addressed digitally. The main problem associated with this idea is that the pass transistors, which are necessary to allow access to individual test transistors, will affect the measurements in some way. This work addresses and attempts to quantify the problem to allow meaningful analogue transistor measurements to be made. The object of the investigation was to extract SPICE parameters from the transistors. This gives a very sensitive measurement of both the test transistor and how the inclusion of the pass transistors effects those measurements. Although investigation of transistors accessed via pass transistors has been explored by others [7, 8] the extraction of SPICE parameters [9, 10], as attempted here, has not.

SPICE parameters are widely used for circuit simulation purposes and in appropriate cases for process control. Several routines exist for the extraction of SPICE parameters but almost all rely on some degree of numerical optimisation of the parameters to give close fitting of the parameter derived curves to the real, extracted ones [11-15]. The chosen software was PARAMEX [16] since it does not rely on any such optimisation and hence all the extracted parameters have an attributable physical meaning. The SPICE model used for this work was the '2G' version with level 3 parameters. The level 3 model gives a more complete, and hence more accurate, device model than the 'simple' level 1 model since factors such as saturation slope, mobility degradation and threshold shift with drain voltage are taken into account.

The method of investigation was that SPICE parameters would be extracted directly from test transistors and compared with those extracted via the switching transistors. The effect of the switching circuitry could then be evaluated. The pass transistor size would vary as would electrical variables such as its gate voltage.

The layout of a suitable test chip would require some basic knowledge of the pass transistor switching circuitry. Hence the investigation would begin by using SPICE *as a*

tool for circuit simulation as described in the following section.

4.4. Analysis of Switching Circuitry

Before any test chips for investigating on-chip switching were designed, the switching performance of transistors was first analysed using SPICE. The starting point for this was the circuit considered by Moore but in this case it was evaluated for analogue measurements [3]. That circuit used by Moore with decoders is shown fully in figure 4.3. For simulation purposes the decoders can be ignored because only the pass transistors they switch will have any affect on the analogue characteristics of the circuitry. This gives the effective circuit for transistor testing, with the pass transistors, as that shown by figure 4.4. SPICE was then used to investigate how the inclusion of the pass transistors would affect voltage and current measurements at the external terminals of the test circuit (of figure 4.4), and these were then compared with direct measurement of the test transistor.

Analysis of this circuit revealed that it could be considered in two parts. The first part has the transistors labelled $T1$ and $T2$ in a current limiting position where they effectively control the source-drain current through the device under test. This meant the circuit of figure 4.5, with the relevant transistors, could be used to look at current flow through the test transistor and voltage drops across it. Further simplification to insure that only the pass transistor effects were investigated saw the use of a $10k\Omega$ resistor representing the test transistor. The second part has the transistors $T3$ and $T4$ as part of the voltage sensing arms and the circuit of figure 4.6 can be used to look at characteristics of this circuit.

All simulations were performed on these circuits using SPICE. The SPICE level 1 parameters used were those derived for the EMF NMOS process and these parameters are given in table 4.2. These are the enhancement device parameters because only these devices needed to be considered.

4.5. SPICE Simulations

The voltage sensing circuitry was investigated by first using the simplified circuit of figure 4.6 which concentrates solely on the voltage sensing arms with the voltmeter represented with a high value resistor ($10M\Omega$). Simulations were then performed for a number of different gate voltages on the pass transistors ($T3$ and $T4$), which both had an

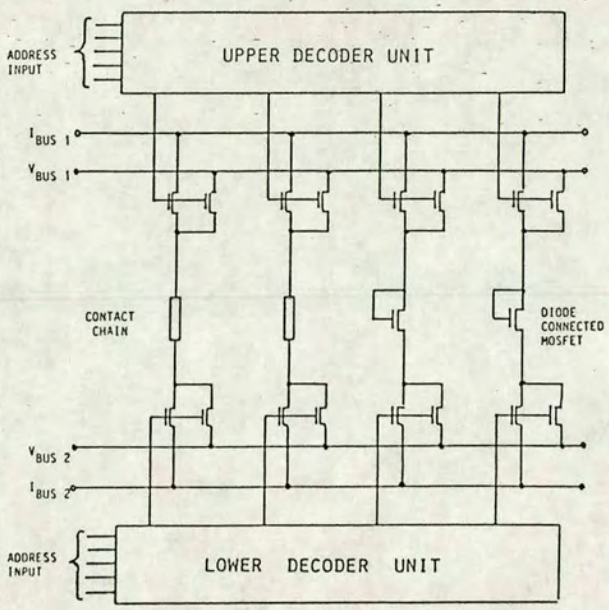


Figure 4.3. Schematic diagram of chip shown in figure 4.2. After [3].

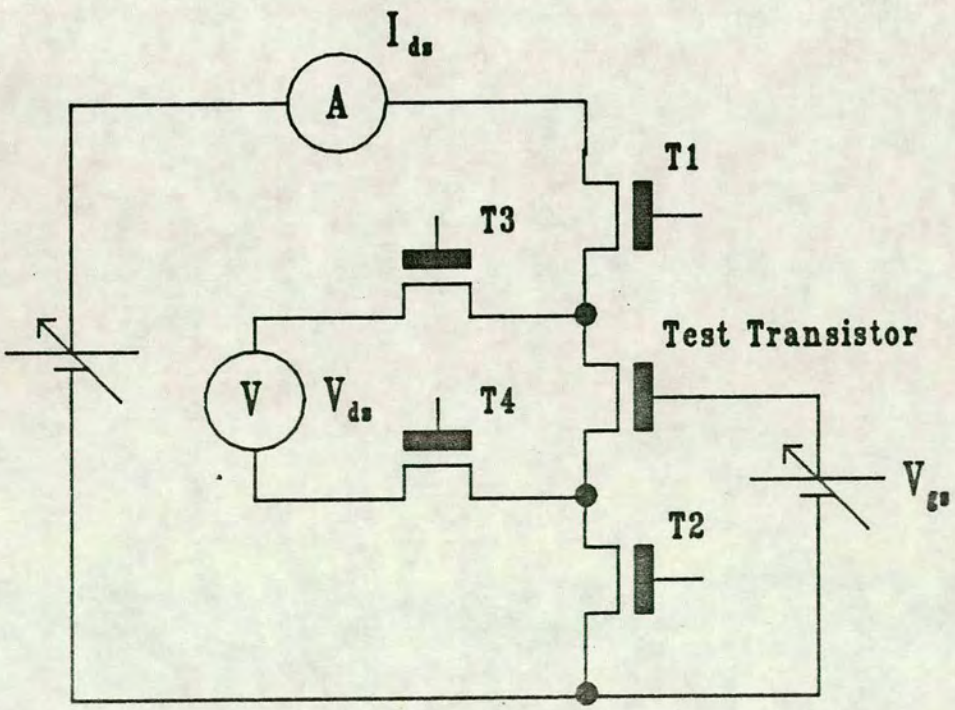


Figure 4.4. Effective circuit for on-chip switching investigation.

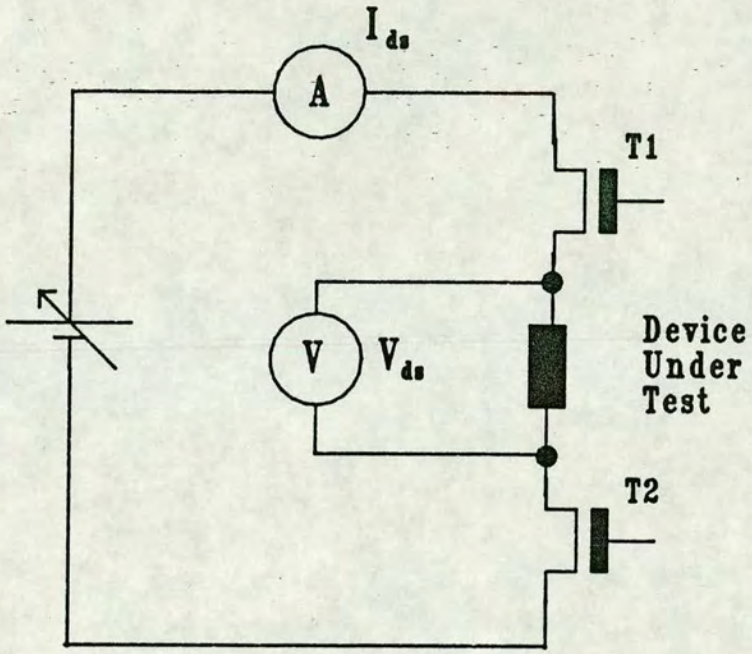


Figure 4.5. Circuit used for current flow (SPICE simulation) experiments.

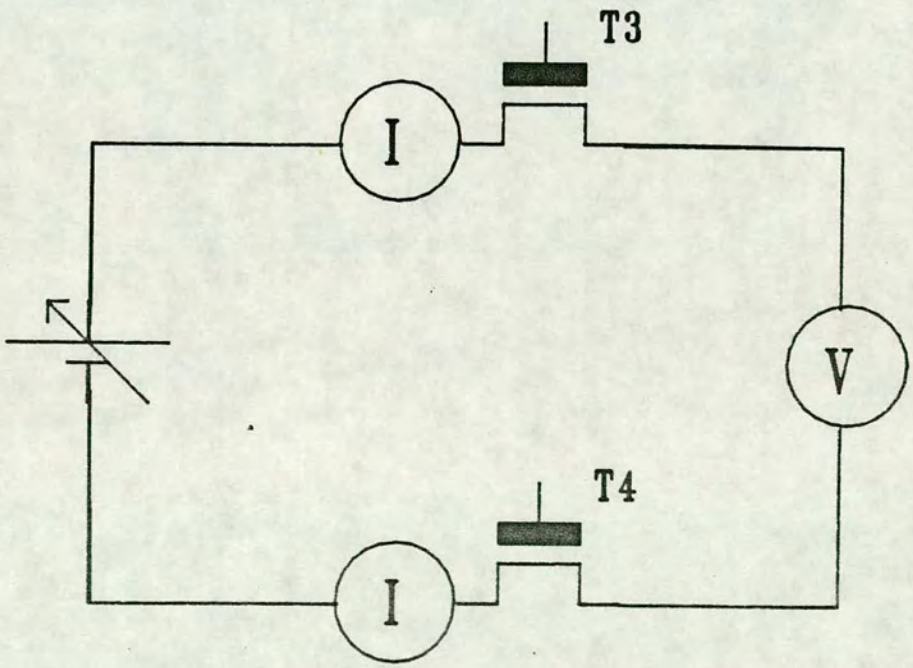


Figure 4.6. Circuit used for voltage sensing (SPICE simulation) experiments.

SPICE Parameter	Numerical Value	SPICE Parameter	Numerical Value
V_{t0}	1.05	μ_0	500
γ	0.3	C_{gso}	4.5×10^{-10}
t_{ox}	8.5×10^{-8}	C_{gdo}	4.5×10^{-10}
C_j	1.0×10^{-4}	C_{jsw}	1.0×10^{-9}
J_s	1.0×10^{-7}	L_{del}	1.93×10^{-6}
X_{qc}	0.4	θ	0.01

Table 4.2. Level 1 SPICE parameters, derived from the EMF 6μm process, used for pass transistor simulations.

aspect ratio of 1:1, where the voltage source was incrementally stepped at $0.1V$ intervals. The voltage drop across the voltmeter was then noted and compared with the supply voltage. Table 4.3 summarises the parameters varied for this simulation and the results are depicted by figure 4.7. These indicate that the voltage drop at the voltmeter terminals would be very close to that at the measurement terminals, provided that the voltage at each measurement terminal was at least V_t (for that pass transistor) below the gate voltage on that same transistor.

Pass Transistor Aspect Ratio	Voltmeter, Z	Pass Transistor V_g
1:1	$10M\Omega$	5,6,7,8,9,10V

Table 4.3. Summary of simulation details.

Thus by increasing the pass transistor gate voltage higher voltages could be measured by the voltmeter. The results are consistent with the explanation that the 'on' resistance of the two pass transistors ($\approx 10k\Omega$ each) is small compared with the resistance of the voltmeter ($\approx$ several $M\Omega$ for a typical meter). Since the current flow in the sensing circuit is very small little voltage is dropped across the pass transistors and the measured voltage at the voltmeter terminals will be very close to that at the measurement points. For this to be true though the pass transistors must retain at least a threshold voltage difference greater between the gate and one input terminal. Thus if a voltage at the measurement points (the pass transistor input voltage) is above $V_g - V_t$ for the pass transistor then this input voltage will not be sensed accurately by the voltmeter.

The effect of varying the pass transistor aspect ratio on the voltage drop across it, for a given gate voltage, was also investigated. The simulations attempted are summarised by table 4.4 and the results for pass transistors ($T3$ and $T4$), with $5V$ gate voltage, is shown by

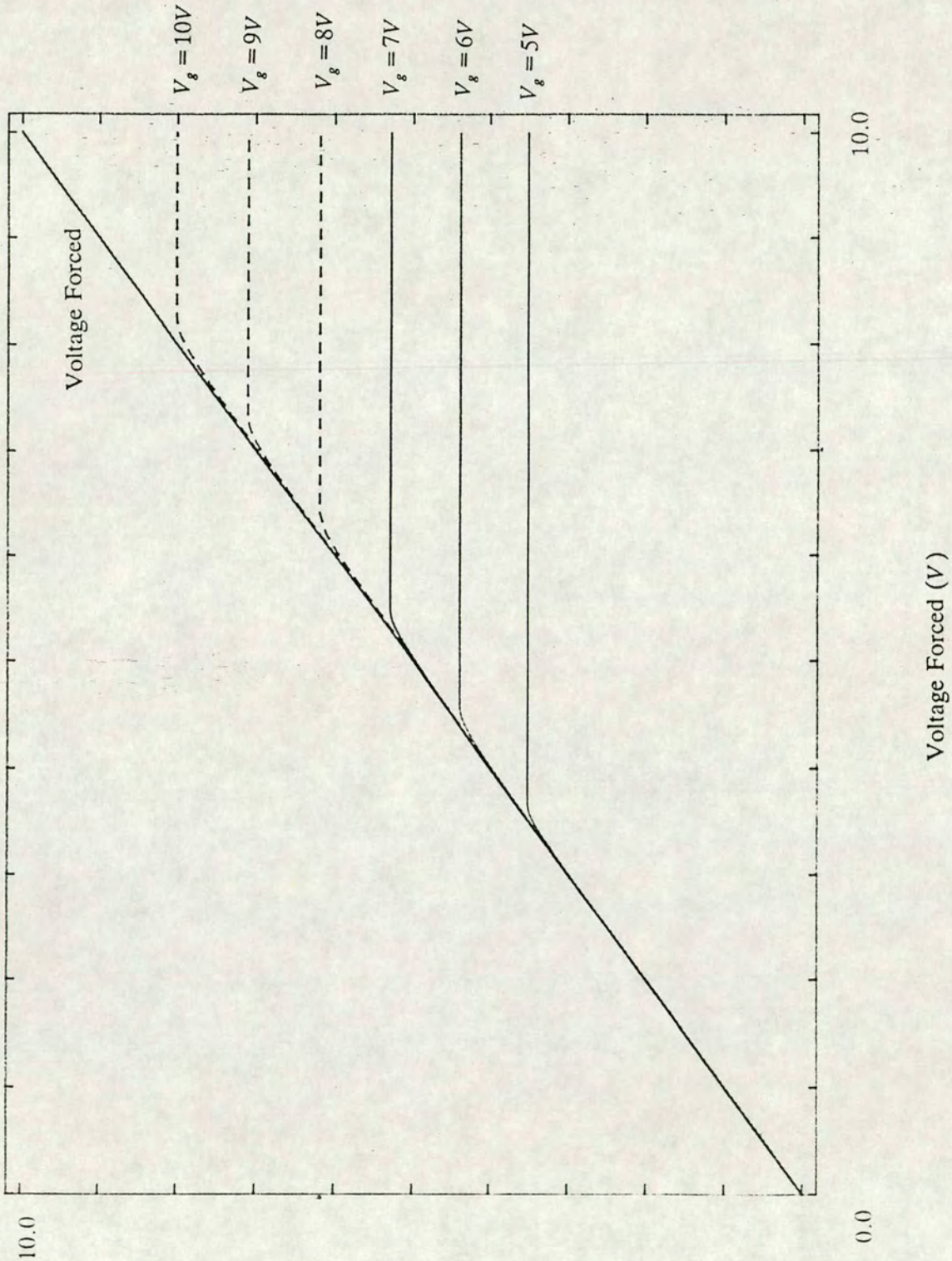


Figure 4.7. Simulation result showing the effect the pass transistor gate voltage (V_g of T3 and T4) has on the voltage measured at the voltmeter.

figures 4.8 and 4.9 respectively.

Pass Transistor Aspect Ratios	Voltmeter, Z	Pass Transistor V_g
1:1 1:4 1:10 10:10 4:4 4:1 10:1	$10M\Omega$	$5V$

Table 4.4. Summary of simulation details.

It can be seen from these that although the voltage drops in each case were small, there was a pronouncedly lower drop for larger W/L ratio transistors. From the first order I_{ds} equation (equation 4.1) this is to be expected,

$$I_{ds} = \beta \left[(V_{gs} - V_t)V_{ds} - \frac{V_{ds}^2}{2} \right] \tag{4.1}$$

where $V_{gs} = V_g - V_s$, $V_{ds} = V_d - V_s$ and β is the transistor gain factor. For a given I_{ds} it can be deduced that V_{ds} will be smaller for a larger W/L.

The effect of different effective impedances of the voltmeter for a given aspect ratio of pass transistor and gate voltage was also examined. Circuit simulations were performed with a $5V$ gate voltage and pass transistor with a 1:1 aspect ratio. These simulations are summarised in table 4.5 and the results for these are shown by figure 4.10.

Pass Transistor Aspect Ratio	Voltmeter, Z	Pass Transistor V_g
1:1	10, 20, 30, $50M\Omega$	$5V$

Table 4.5. Summary of simulation details.

From this it can be seen that, although the voltage drops in each case were small a 'better' (higher impedance) voltmeter results in a lower voltage being dropped across the pass transistor. This is simply due to the lower current flow in the voltage measuring arms for higher impedance voltmeters.

To investigate the role of pass transistors in the current forcing situation, the modified circuit of figure 4.5 was used. This only has the transistors essential for controlling current flow in the DUT. A fixed gate voltage was placed on both the pass transistors ($T1$ and $T2$) and the ammeter simulated by a low value resistor. Simulations were then performed where the voltage forced was varied. The effect of this is shown in figure 4.11 which shows the source-drain voltage for 20:1 pass transistors, both with a gate voltage of $5V$. It was

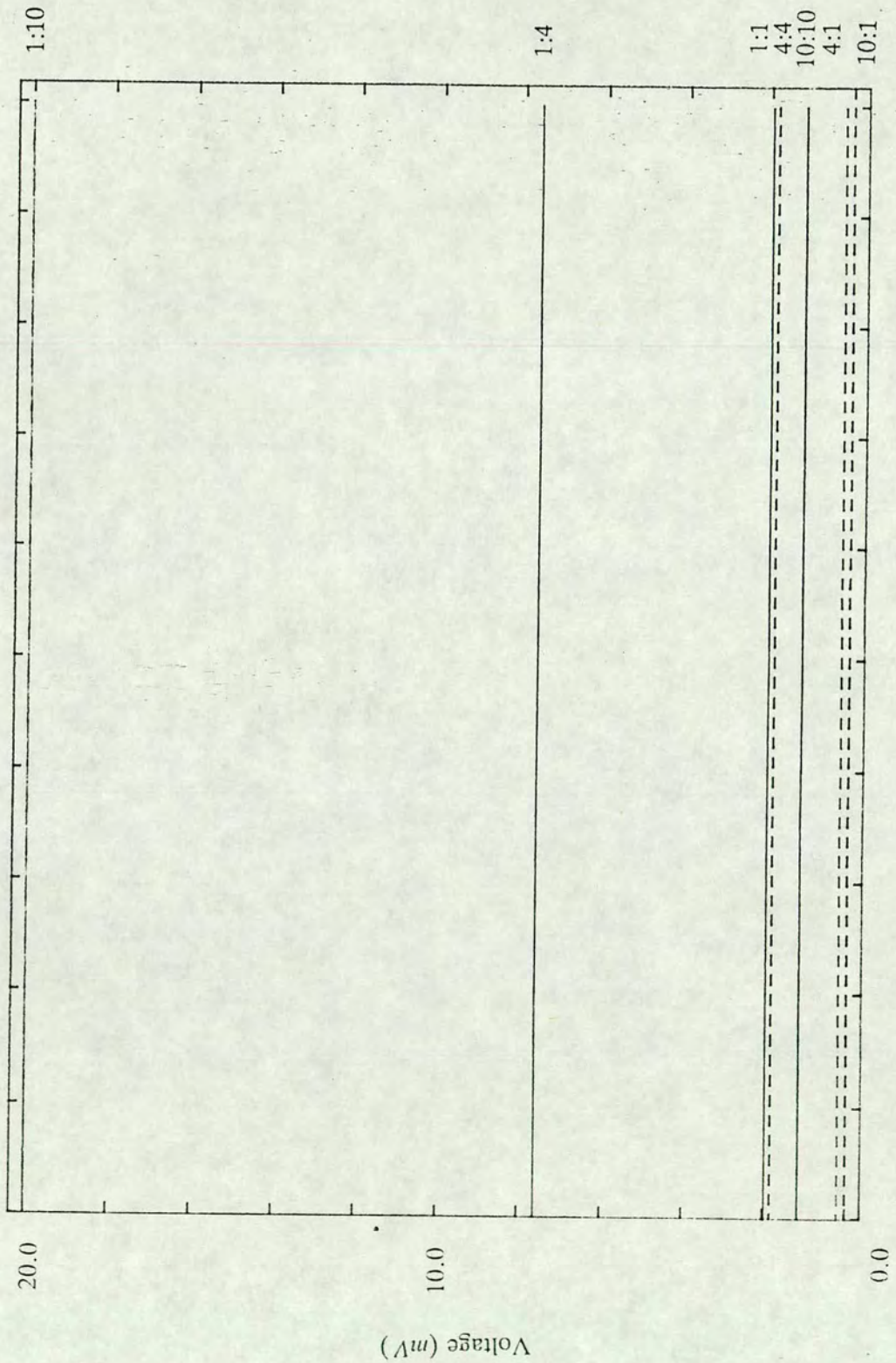


Figure 4.8. Simulation result showing the effect the pass transistor aspect ratio (for T3) has on the voltage dropped across it.

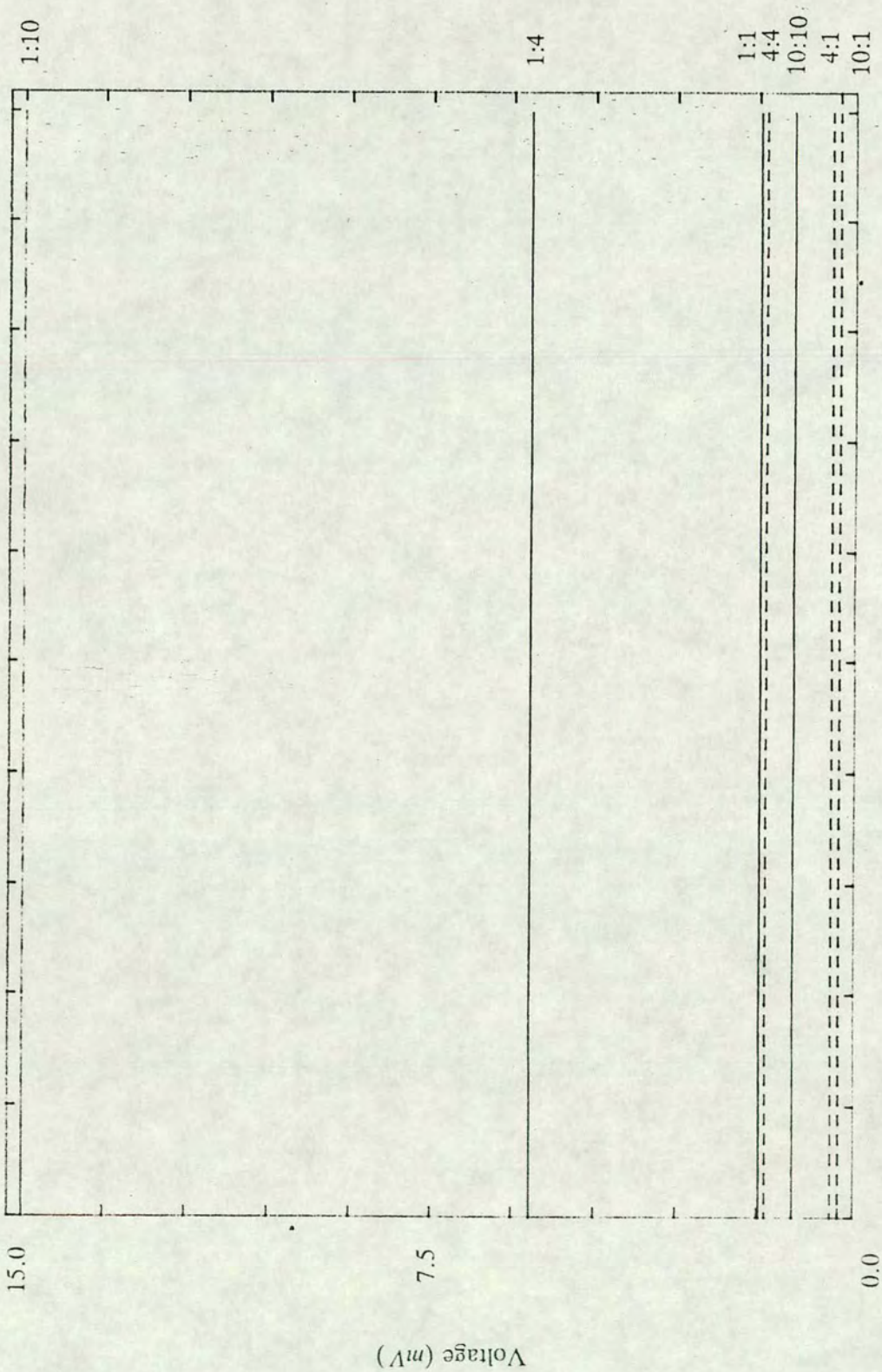


Figure 4.9. Simulation result showing the effect the pass transistor aspect ratio (for T4) has on the voltage dropped across it.

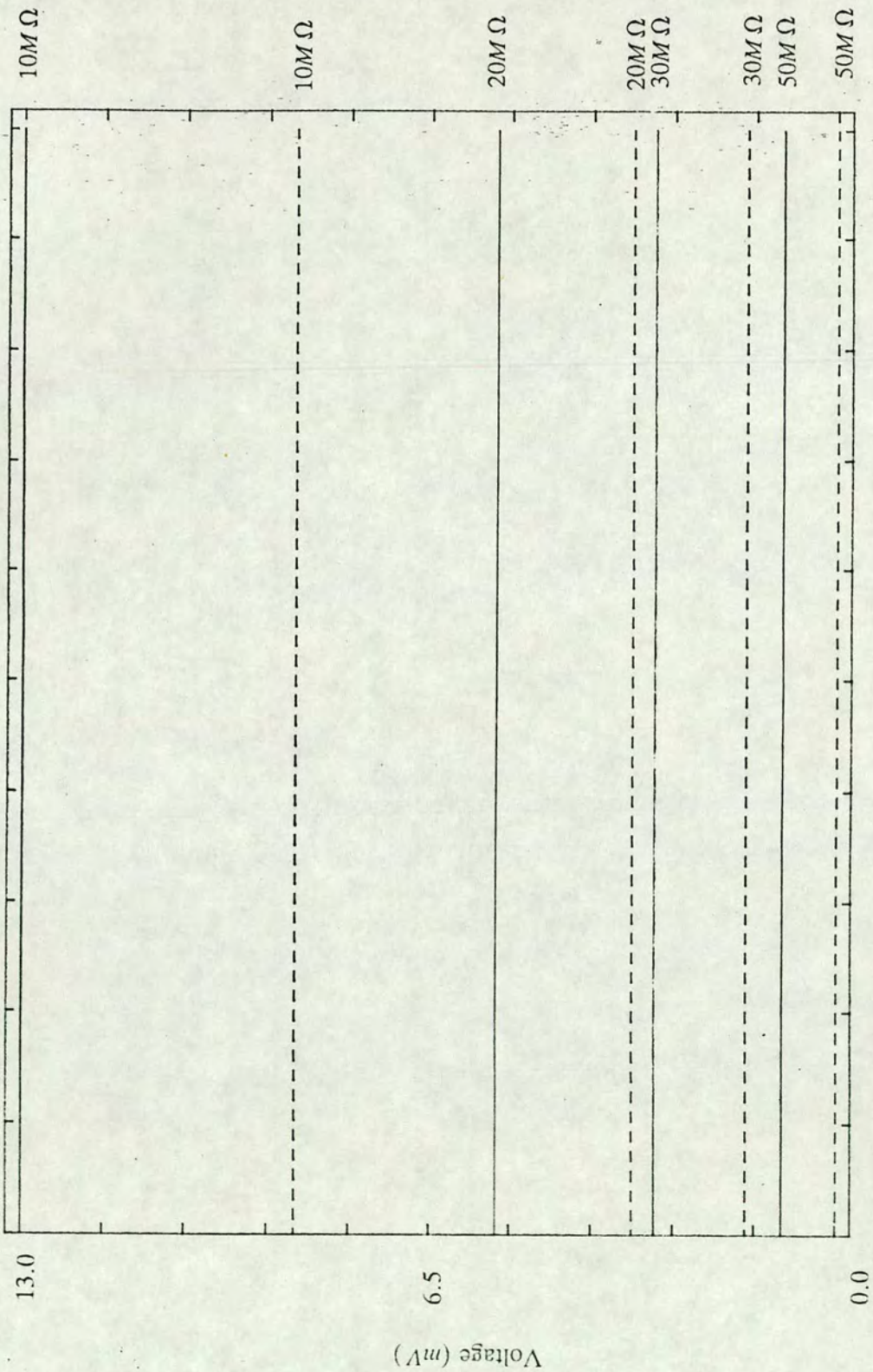


Figure 4.10. Simulation result showing the effect the voltmeter impedance has on the voltage dropped across T3 (solid) and T4 (dotted lines).

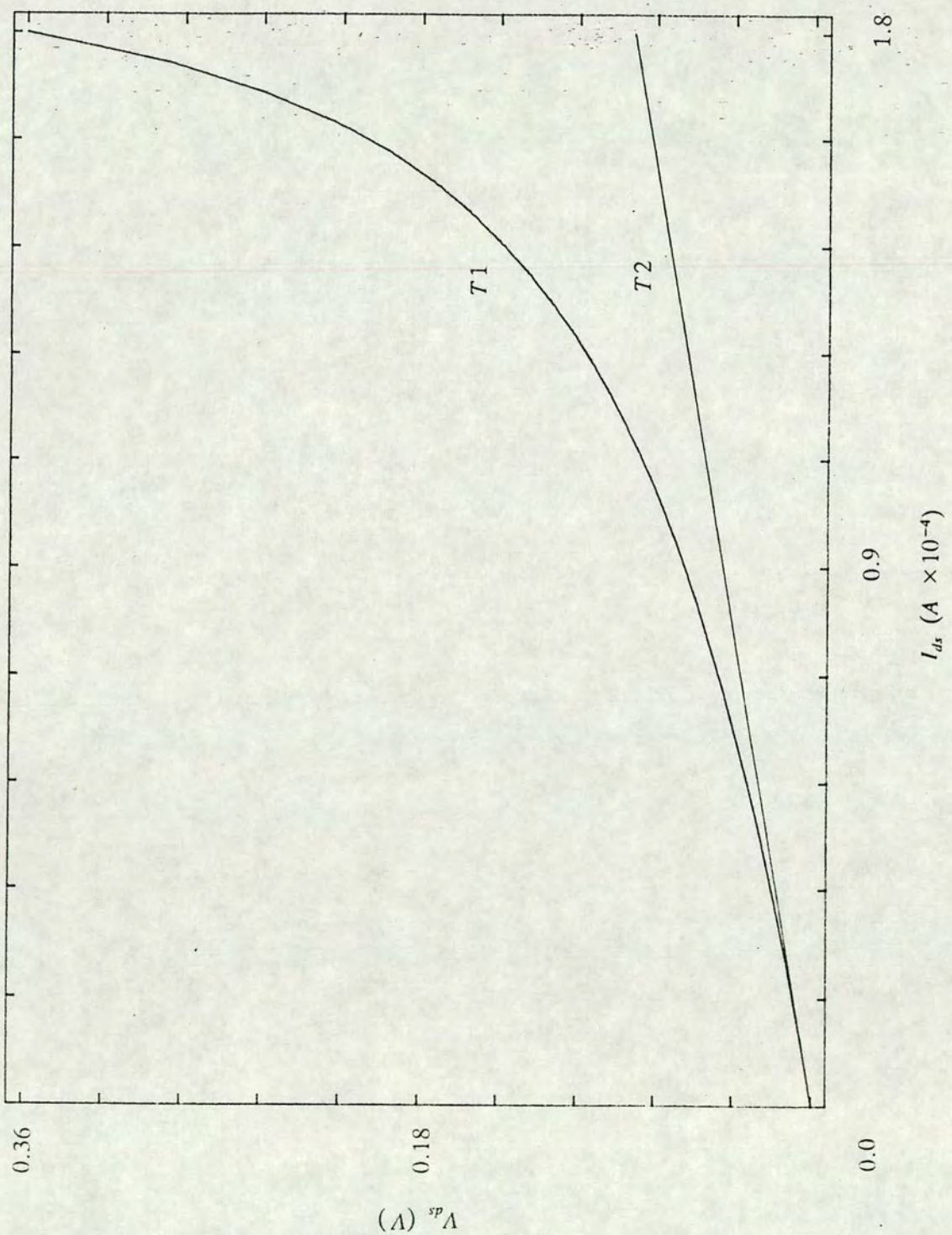


Figure 4.11. Simulation result showing V_{ds} as a function of I_{ds} for T1 and T2. The current limiting effect of T1 is seen.

found that the current flowing in the circuit was limited by transistor $T1$. This saturated at a low I_{ds} while $T2$ was still firmly in the linear region. This can be explained by the non-zero drain voltage of $T1$, due to the combined voltage drop over $T2$ and the test transistor. This non-zero drain voltage of $T1$ with rising current flow is shown by figure 4.12. Similarly V_s and V_{gs} for this transistor is shown by figure 4.13. Here, for $T1$, an increase in V_s occurs where both V_{gs} and V_{ds} will be lower than if V_s is zero. From an appreciation of the simple first order I_{ds} drain equation (equation 4.1) it is clear that this indeed is what would be expected as a lower V_{gs} and V_{ds} will result in a lower I_{ds}. Thus only increasing the W/L ratio or increasing V_g will allow a higher current to flow.

Taking the results of all the simulations into consideration it appeared that there are only minor problems in the use of pass transistors in voltage sensing circuitry. However it has been demonstrated that the use of pass transistors as 'current gates' can only be made by either increasing the transistor size or increasing the pass transistor gate voltage.

4.6. Test Chip Design

To further investigate these results, two test chips were designed, $E\mu$ 640 and $E\mu$ 641. These chips were laid out using the GAELIC design language as implemented on the Rutherford Appleton Labs (RAL) PRIME F computer, accessed locally via a PAD link. The two chips were both processed on a single wafer using the standard EMF $6\mu m$ NMOS process. Since depletion transistors were not used, no depletion implant (layer 2) or buried contact (layer 3) masks were required. For ease of probing a standard 2×10 pad layout of the designs was used throughout both chips [1]. These designs contained a number of different measurement configurations, with a range of pass and test transistor geometries. These different configurations were were used with the idea that at least one would illustrate characteristics favourable for transistor measurement.

Figures 4.14a) to e) shows the five basic transistor configurations used in the designs and are shown in schematic form. The configurations depicted by figure 4.14f) and g) have a similar transistor layout to a) and d) respectively but without some of the intermediate access pads.

Configuration 1 (figure 4.14a)) was essentially that used for the initial circuit simulations, previously outlined, and that used by Moore [3]. The test transistor in configuration 1 was a minimum geometry 1:1 enhancement transistor. The pass transistors

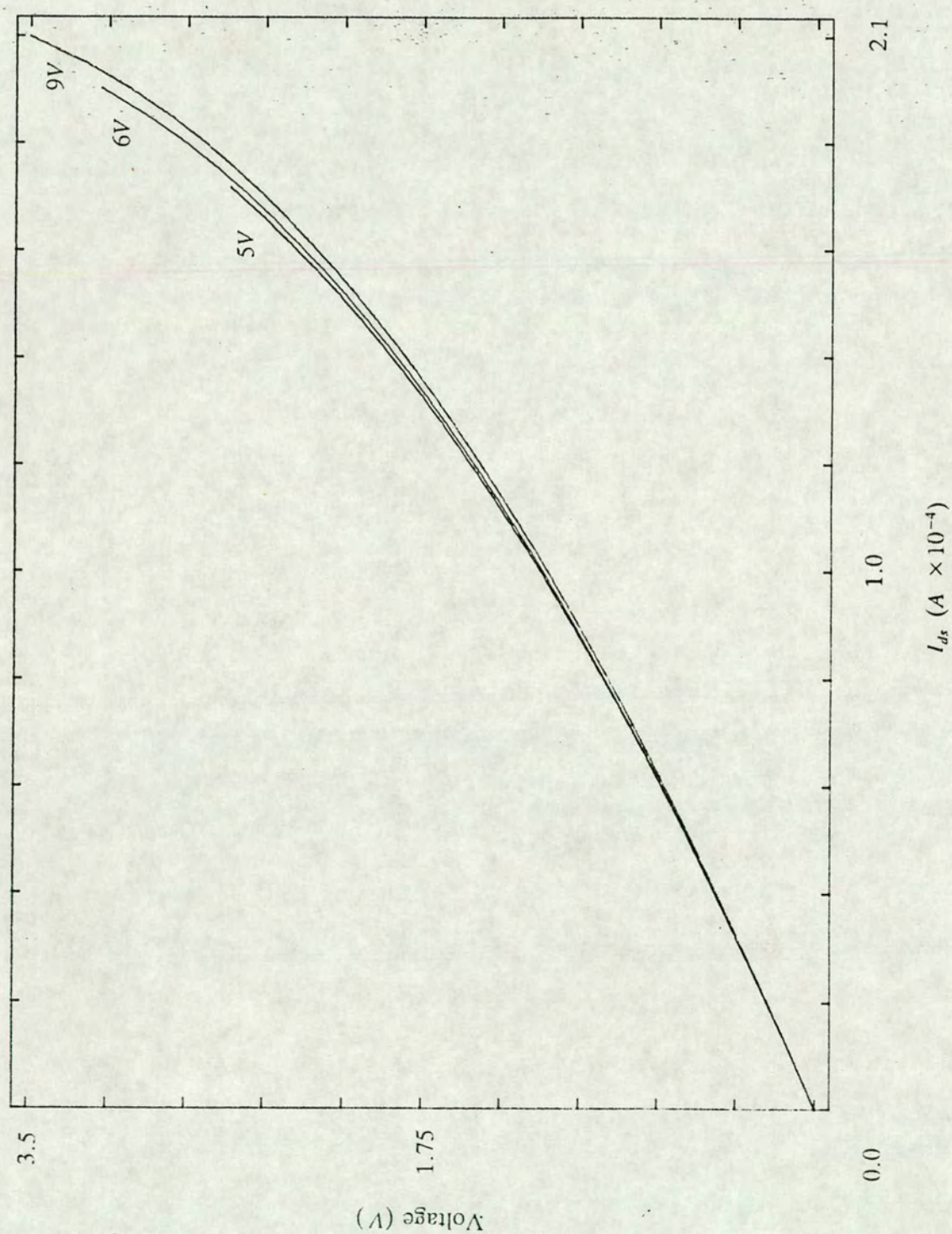


Figure 4.12. Simulation result showing the non-zero drain voltage of T1 with increasing I_{ds} at the indicated V_{gs}.

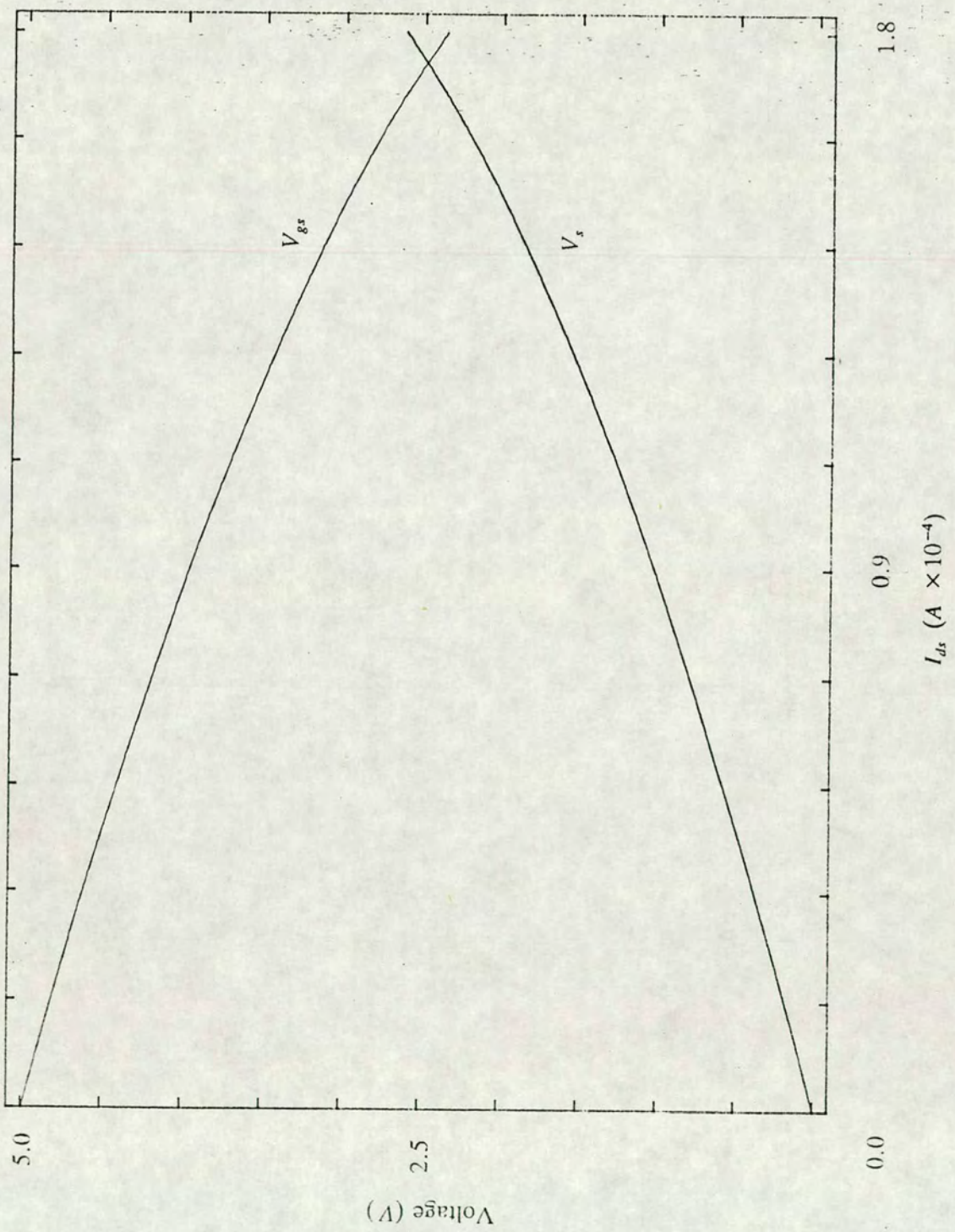


Figure 4.13. Simulation result showing V_s and V_{gs} for T1.

in the sense arms were both 10:1 enhancement devices with a common gate. A number of different aspect ratio current pass transistors were laid out. The layout details for configuration 1 are summarised in table 4.6.

Test Transistors		Pass Transistors
Module	Size	Size
A	1:1	5:1
B	1:1	8:1
C	1:1	10:1
D	1:1	12:1
E	1:1	15:1
F	1:1	20:1
G	1:1	40:1
H	1:1	4:4

Table 4.6. Transistor composition of configurations 1 and 7.

Configuration 7 (figure 4.14f)) has the same transistor configuration as 1 but with a number of the intermediate pads removed. Thus for configuration 1 a total of ten pads were required as opposed to eight pads for 7. Test, sense and force transistors dimensions were the same as 1.

Configuration 2 (figure 4.14b)) has two test transistors per 2 × 10 module and twelve potential pass transistors. Each test transistor had separate source, gate and drain connections while the pass transistors had common gate and drain connections. Each of the 2 × 10 module had the same set of pass transistors but different sets of test transistors. This is summarised by table 4.7.

Test Transistors		Pass Transistors
Module	Size	Size
A	1:1 4:1	1:1 2:1 3:1 4:1 5:1 8:1 10:1 15:1 20:1 30:1 10:10 4:4
B	1:4 4:4	1:1 2:1 3:1 4:1 5:1 8:1 10:1 15:1 20:1 30:1 10:10 4:4
C	8:1 15:1	1:1 2:1 3:1 4:1 5:1 8:1 10:1 15:1 20:1 30:1 10:10 4:4

Table 4.7. Transistor composition of configuration 2.

Configuration 3 (figure 4.14c)) is similar to that of 2 but has a second row of pass transistors in each 2 × 10 module identical to the first. Table 4.8 gives the layout details for this.

Configuration 4 (figure 4.14d)) used the same layout of test and pass transistors as configuration 6 (figure 4.14g)) but the latter had some intermediate pads removed. The

Test Transistors		Pass Transistors
Module	Size	Size
A1	1:1 4:1	1:1 2:1 3:1 4:1 5:1
B1	1:1 4:1	8:1 10:1 12:1 15:1 20:1
C1	1:1 4:1	30:1 40:1 4:4 10:10 20:1
A2	1:4 4:4	1:1 2:1 3:1 4:1 5:1
B2	1:4 4:4	8:1 10:1 12:1 15:1 20:1
A3	8:1 15:1	1:1 2:1 3:1 4:1 5:1
B3	8:1 15:1	8:1 10:1 12:1 15:1 20:1

Table 4.8. Transistor composition of configuration 3.

sense transistors in both these configurations were 10:1 aspect ratio enhancement transistors. Table 4.9 summarises the layout details.

Test Transistors		Pass Transistors	Test Transistors		Pass Transistors
Module	Size	Size	Module	Size	Size
A1	1:1	4:1	A2	4:1	4:1
B1	1:1	8:1	B2	4:1	8:1
C1	1:1	10:1	C2	4:1	10:1
D1	1:1	12:1	D2	4:1	12:1
E1	1:1	15:1	E2	4:1	15:1
F1	1:1	20:1	F2	4:1	20:1

Table 4.9. Transistor composition of configurations 4 and 6.

Configuration 5 (figure 4.14e)) is similar to that of 4 but only has a single transistor in each of the sense and force arms. The sense transistors are of a 10:1 aspect ratio in each case and the complete layout is detailed in table 4.10.

Test Transistors		Pass Transistors	Test Transistors		Pass Transistors
Module	Size	Size	Module	Size	Size
A1	1:1	1:1	A2	4:1	1:1
B1	1:1	2:1	B2	4:1	2:1
C1	1:1	3:1	C2	4:1	3:1
D1	1:1	4:1	D2	4:1	4:1
E1	1:1	5:1	E2	4:1	5:1
F1	1:1	8:1	F2	4:1	8:1
G1	1:1	10:1	G2	4:1	10:1
H1	1:1	12:1	H2	4:1	12:1
I1	1:1	15:1	I2	4:1	15:1
J1	1:1	20:1	J2	4:1	20:1
K1	1:1	4:4	K2	4:1	4:4

Table 4.10. Transistor composition of configuration 5.

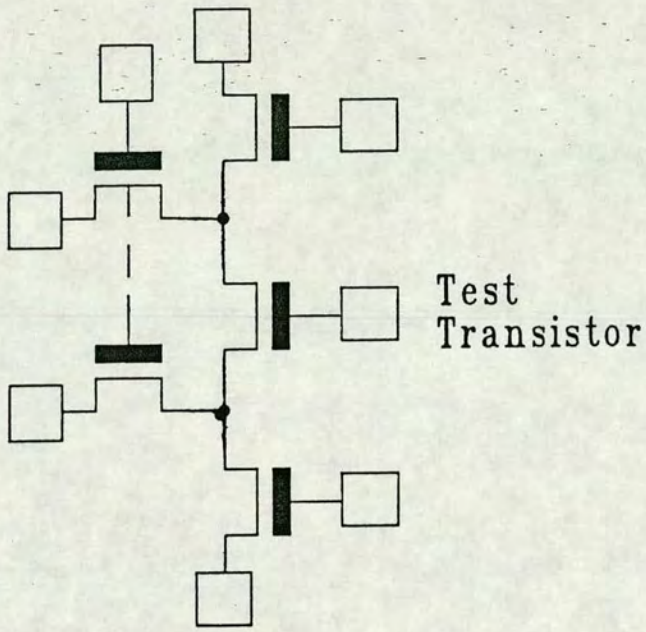


Figure 4.14a) Test and pass transistors for configuration 1.

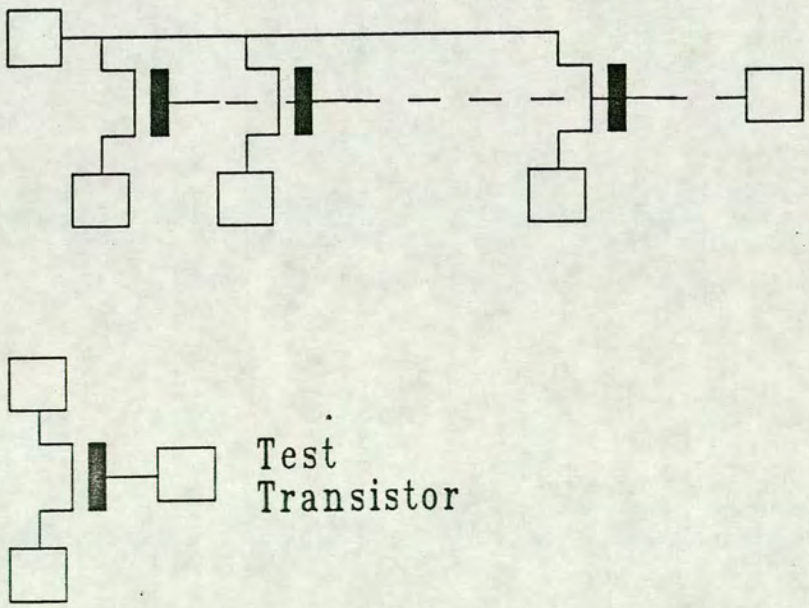


Figure 4.14b) Test and pass transistors for configuration 2.

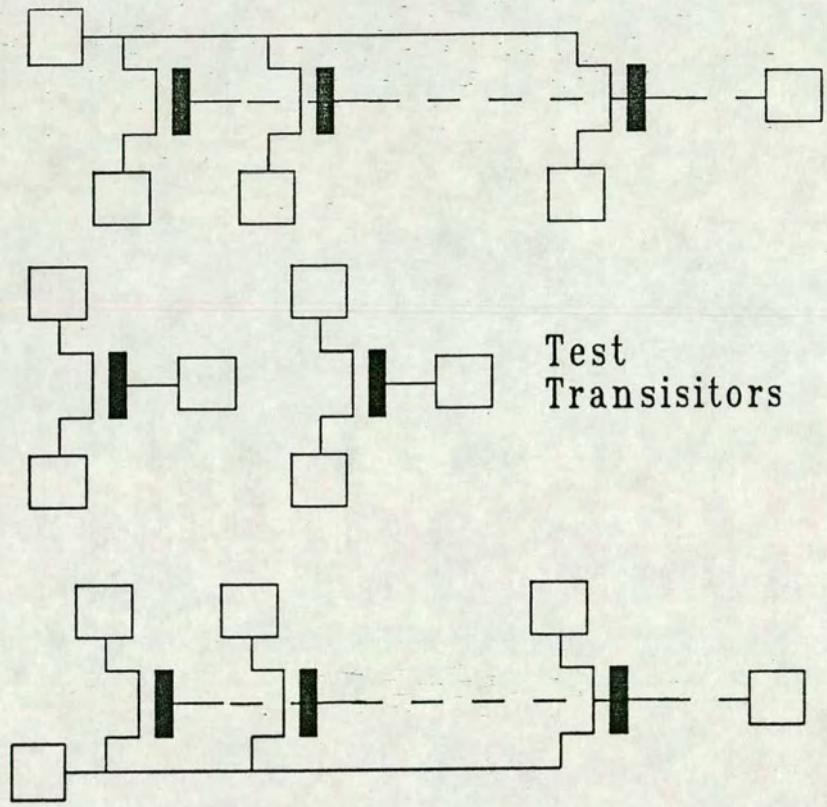


Figure 4.14c) Test and pass transistors for configuration 3.

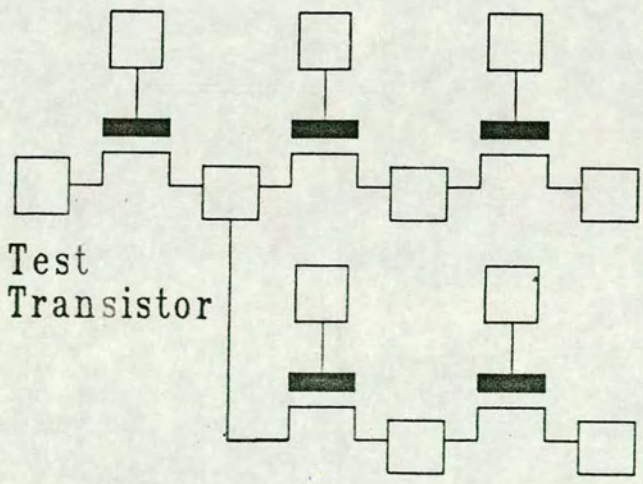


Figure 4.14d) Test and pass transistors for configuration 4.

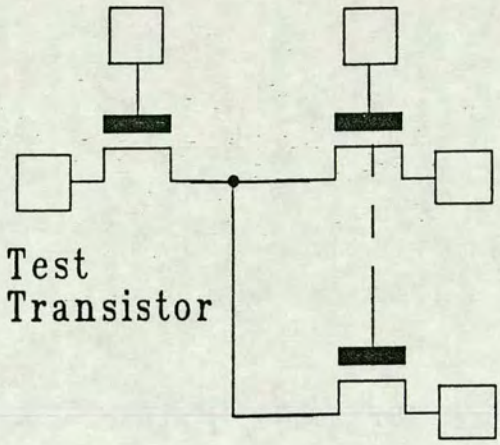


Figure 4.14e) Test and pass transistors for configuration 5.

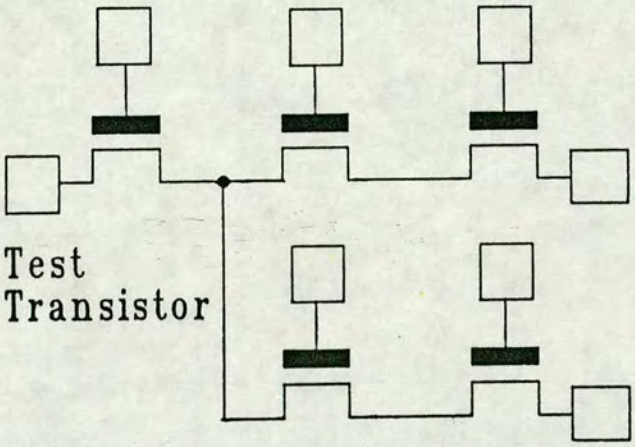


Figure 4.14f) Test and pass transistors for configuration 6.

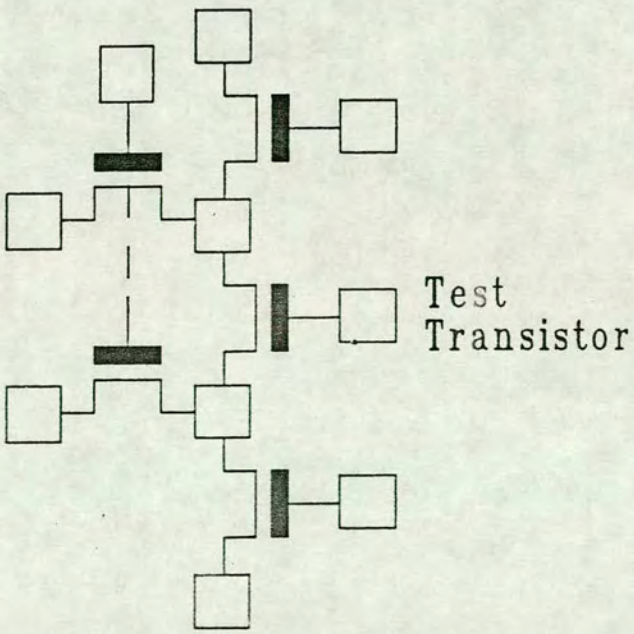


Figure 4.14g) Test and pass transistors for configuration 7.

All these test circuits were assembled into two test chips. The floorplan and layout for $E\mu 640$ is shown, respectively, by figures 4.15 and 4.16. Similarly figures 4.16 and 4.17 show $E\mu 641$.

4.7. Transistor Measurements

The simplest design to be evaluated experimentally is shown in figure 4.19 and used the transistors of configuration 2. From the simulations it was expected that this configuration would show all the problems inherent in the use of accessing test transistors for analogue measurements. It has a common drain and a single pass transistor in the voltage measuring arm and one in the current arm. The test transistor gate could be controlled separately as could the pass transistor gates. The test transistor was chosen as a minimum geometry ($6 \times 6\mu m$) device. Initial experiments investigated obtaining sets of $I_{ds} : V_{ds}$ curves both by measuring the test transistor directly and via the pass transistor circuitry. This process was repeated for various geometries of pass transistor, $T1$ of figure 4.19, with the gate voltage fixed at $5V$. This is summarised in table 4.11 and the results for this are indicated in figure 4.20. This figure shows curves measured at the terminals as well as those obtained with the different sizes of pass transistors.

Pass Transistor Aspect Ratios	Pass Transistor V_g
6:1 8:1 10:1 20:1 30:1	$5V$

Table 4.11. Summary of experimental set up for measurement of $6 \times 6\mu m$ test transistor using different size pass transistors.

As can be seen the transistor characteristics in the linear region are less sensitive to the pass transistor dimension since transistor $T1$ does not limit the current. In the saturated region this is not the case and a larger width of pass transistor helps obtain a better representation of the device under test. This is simply due to the increase in current capability as the transistor width is increased. To compare these curves qualitatively the PARAMEX software was modified to allow the RMS errors between any two sets of $I_{ds} : V_{ds}$ curves to be evaluated. Thus the RMS error of the measured curves made via the pass transistors were compared with those made directly. This is shown by table 4.12 for selected pass transistors and these figures confirm the observations made after visual inspection of the

<table>
<tr><td colspan="8">Test Strip</td></tr>
<tr><td colspan="2">7 H</td><td colspan="2">7 G</td><td colspan="2">7 F</td><td colspan="2">7 E</td></tr>
<tr><td colspan="2">7 A</td><td colspan="2">7 B</td><td colspan="2">7 C</td><td colspan="2">7 D</td></tr>
<tr><td colspan="4">3 A3</td><td colspan="4">3 B3</td></tr>
<tr><td colspan="4">3 B2</td><td colspan="4">3 A2</td></tr>
<tr><td colspan="4">3 B1</td><td colspan="4">3 C1</td></tr>
<tr><td colspan="4">3 A1</td><td colspan="4">2 C</td></tr>
<tr><td colspan="4">2 A</td><td colspan="4">2 B</td></tr>
<tr><td colspan="2">1 H</td><td colspan="2">1 G</td><td colspan="2">1 F</td><td colspan="2">1 E</td></tr>
<tr><td colspan="2">1 A</td><td colspan="2">1 B</td><td colspan="2">1 C</td><td colspan="2">1 D</td></tr>
</table>

Figure 4.15. Chip floorplan of Eμ640.

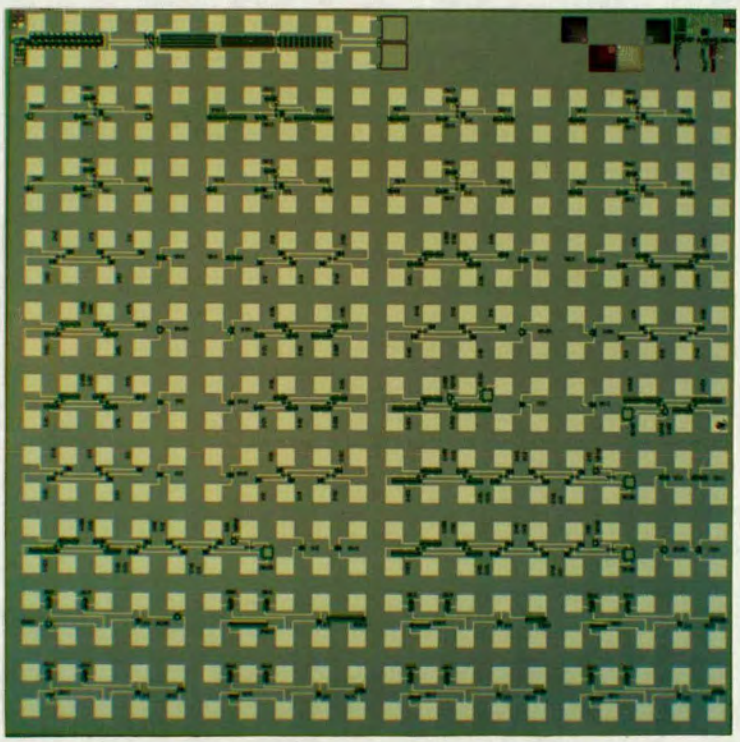


Figure 4.16. Layout of Eμ640.

Test Strip											
5 A2	5 B2	5 C2	5 D2	5 E2	5 F2	5 G2	5 H2				
5 I2	5 J2	5 K2	5 L2	5 L1	5 K1	5 J1	5 I1				
5 A1	5 B1	5 C1	5 D1	5 E1	5 F1	5 G1	5 H1				
4 E2		6 E2		4 F2		6 F2					
4 D2		6 D2		4 C2		6 C2					
4 A2		6 A2		4 B2		6 B2					
4 E1		6 E1		4 F1		6 F1					
4 D1		6 D1		4 C1		6 C1					
4 A1		6 A1		4 B1		6 B1					

Figure 4.17. Chip floorplan of Eμ641.

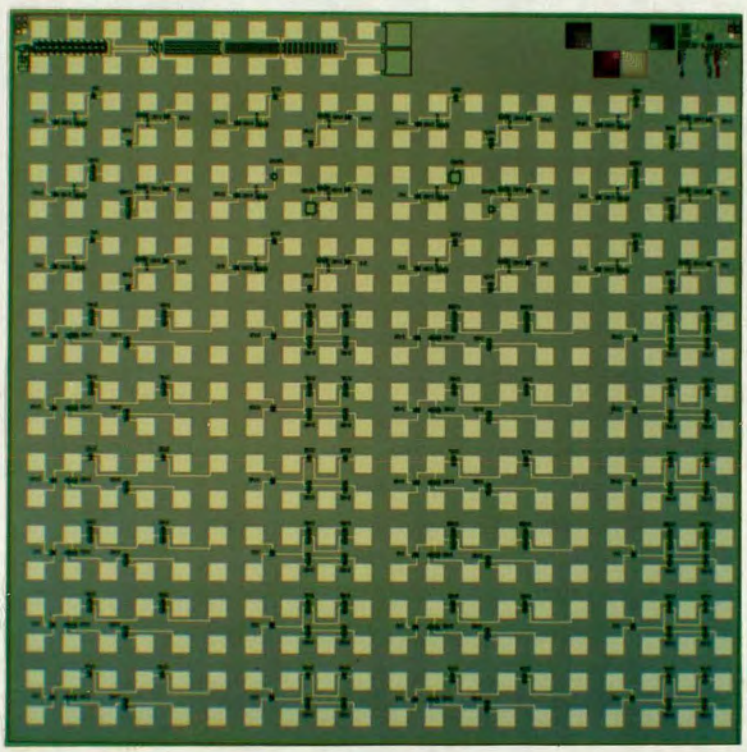


Figure 4.18. Layout of Eμ641.

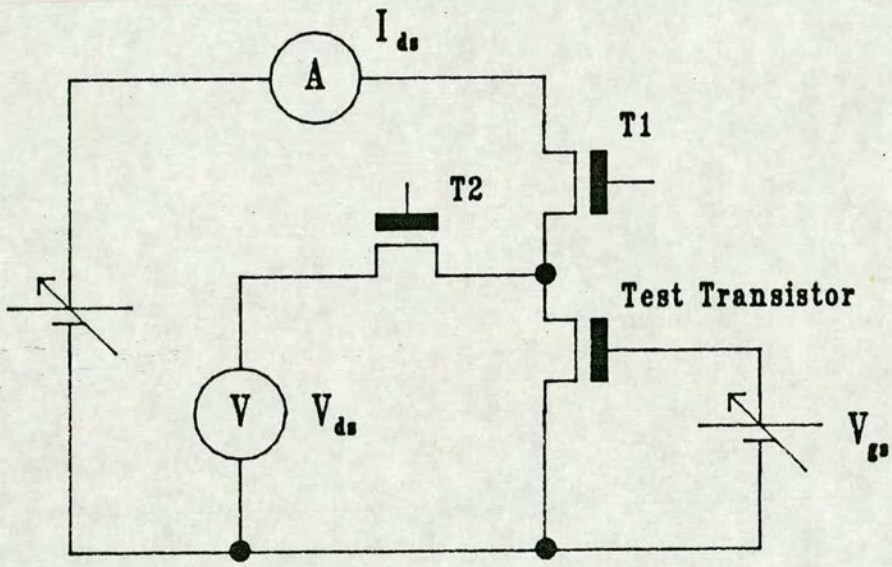


Figure 4.19. Circuit used for experimental measurements.

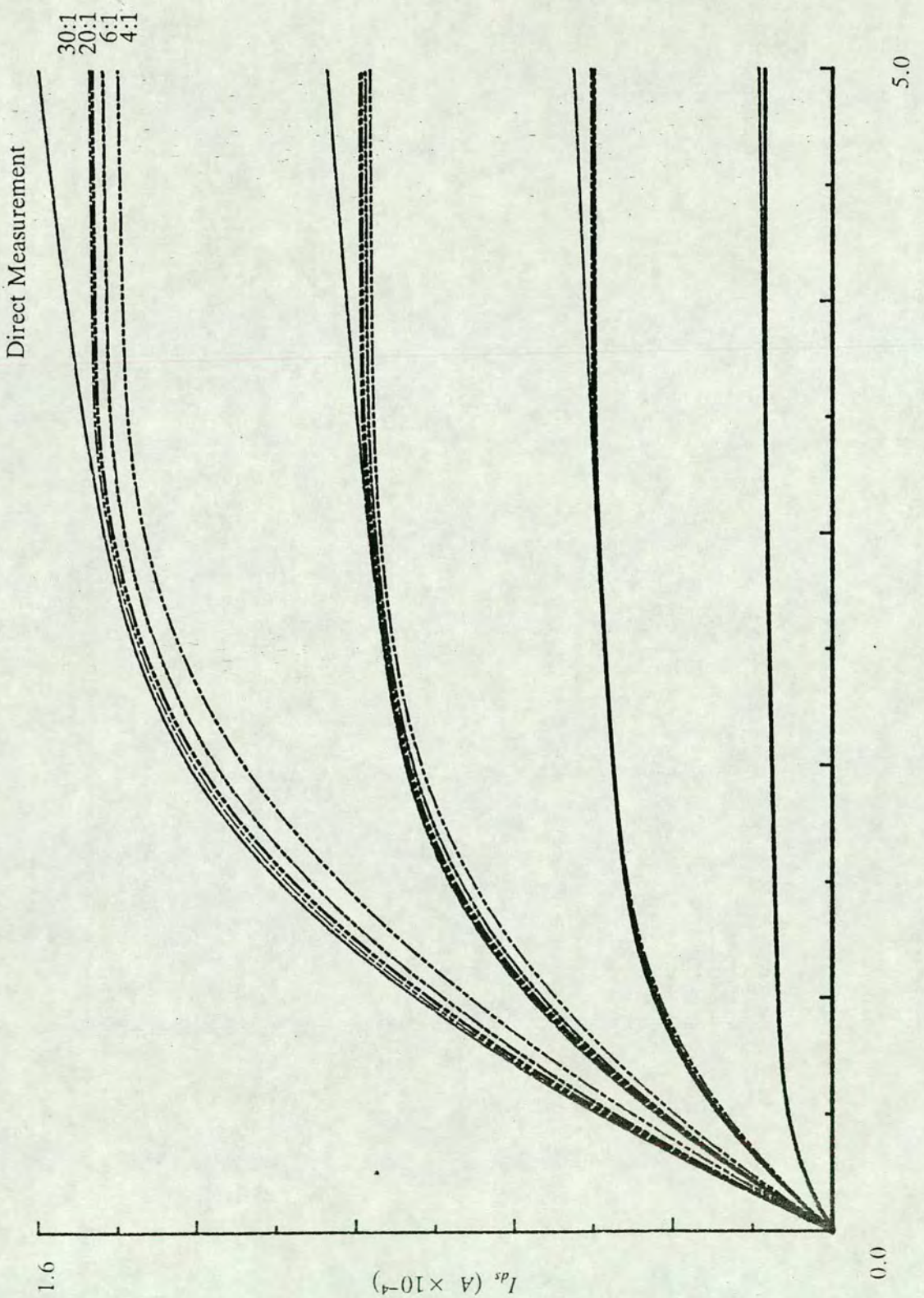


Figure 4.20. Plot of I_{ds} : V_{ds} for 6 × 6μm test transistor measured directly and through the indicated pass transistors.

extracted curves.

V_{gs} (*Volts*)	Average RMS % Error from the Direct Measured Characteristic	
	Pass Transistor Size (μm)	
	24 × 6	180 × 6
2.0	2.4	1.5
3.0	4.0	1.5
4.0	6.7	1.8
5.0	10.6	2.2

Table 4.12. Showing the RMS % error from the directly measured I_{ds} : V_{ds} curves for two different pass transistors geometries at different V_{gs}.

To make more qualitative measurements on the circuit SPICE parameters were extracted for the test transistor and compared with those made via the pass transistors. The SPICE parameters were intended to give an accurate indication of the sensitivity of the measurement system. The SPICE extraction program PARAMEX [16] was used for this purpose and the extracted level 3 SPICE parameters from this circuit are shown in table 4.13.

SPICE Parameters	Measured at the Transistor Terminals	Measured Through the Pass Transistors				
		Pass Transistor Size (μm)				
		24 × 6	48 × 6	60 × 6	120 × 6	180 × 6
N_{fs} (m^{-2})	1.0×10^{15}	2.83×10^{15}	2.83×10^{15}	2.77×10^{15}	2.78×10^{15}	2.83×10^{15}
V_{t0} (V)	1.06	1.03	1.04	1.05	1.05	1.05
γ $(\sqrt{V})$	0.65	0.61	0.55	0.65	0.62	0.64
L_{del} (m)	1.35×10^{-6}	1.35×10^{-6}	1.35×10^{-6}	1.35×10^{-6}	1.35×10^{-6}	1.35×10^{-6}
ΔW (m)	1.32×10^{-6}	1.32×10^{-6}	1.32×10^{-6}	1.32×10^{-6}	1.32×10^{-6}	1.32×10^{-6}
μ_0 $(m^2V^{-1}s^{-1})$	0.079	0.078	0.081	0.079	0.079	0.079
θ (V^{-1})	0.060	0.116	0.093	0.061	0.074	0.066
V_{max} (ms^{-1})	4.59×10^5	*	7.42×10^5	4.67×10^5	5.97×10^5	5.06×10^5
η	0.151	0.049	0.053	0.120	0.038	0.039
δ	0.358	0.377	0.542	0.361	0.411	0.382
κ	0.437	0.006	0.295	0.454	0.213	0.185

* = No significant carrier velocity found.
t_{ox} $(m) = 8.5 \times 10^{-8}$ and X_j $(m) = 1.0 \times 10^{-6}$ (non-measured parameters used)

Table 4.13. SPICE parameters measured directly at test transistor terminals and those measured via the indicated pass transistor.

From these parameters the resimulated curves obtained by using the SPICE parameters in the SPICE equations were generated, figure 4.21. The RMS errors for the these curves against those of direct measurement of the test transistor are shown in table 4.14.

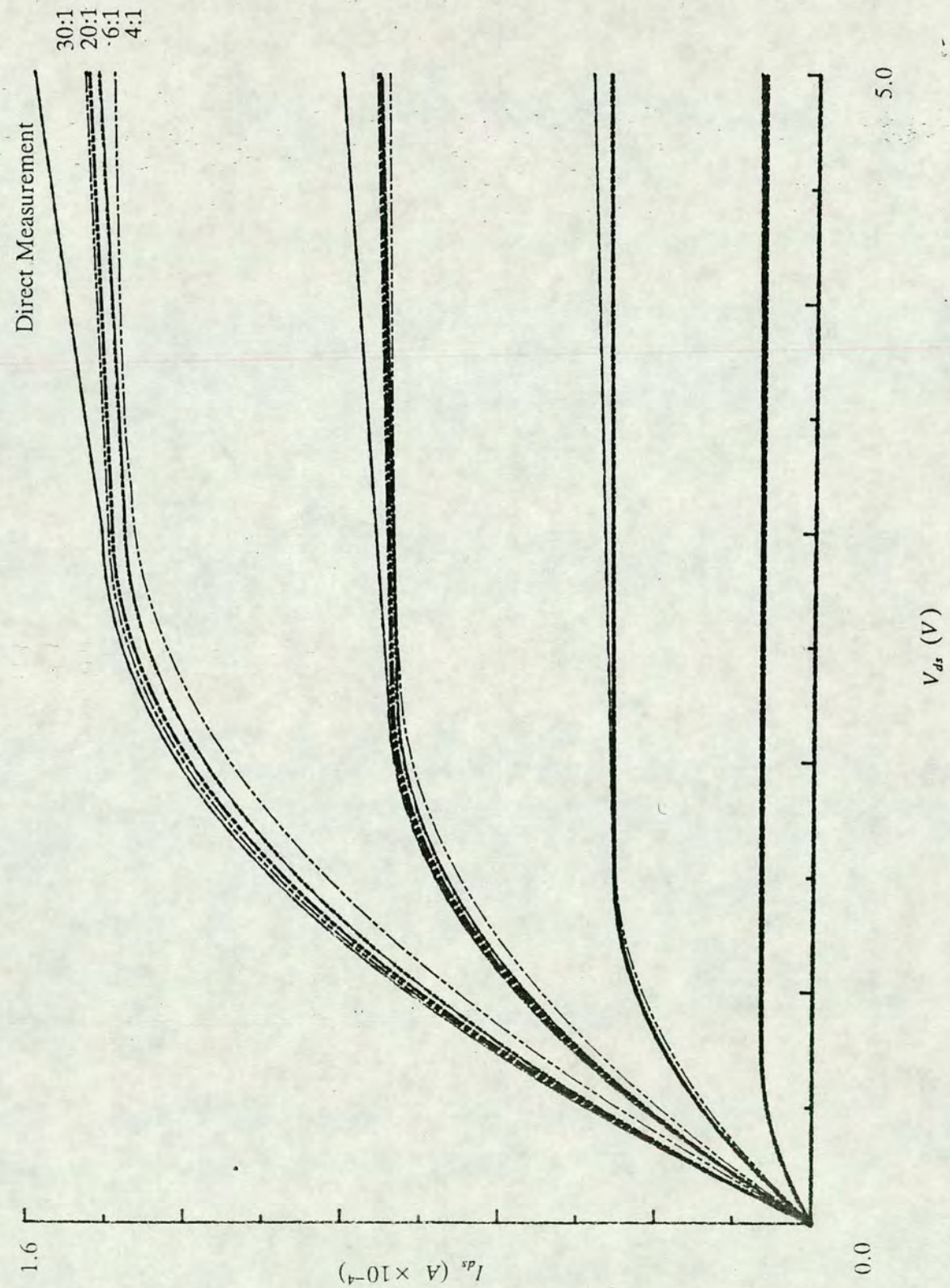


Figure 4.21. Plot of resimulated curves of I_{ds} : V_{ds} for 6 × 6μm test transistor using parameters derived by direct measurement and those derived via the indicated pass transistors.

V_{gs} (*Volts*)	Average RMS % Error of the Simulated from the Measured Characteristic		
	Terminal Measurement	Pass Transistor Size (μm)	
		24 × 6	180 × 6
2.0	13.6	13.1	16.1
3.0	6.5	10.4	9.2
4.0	2.5	9.1	5.0
5.0	0.8	9.3	2.8

Table 4.14. RMS % error of the resimulated curve with the measured curve for direct measurement and via the shown pass transistor size at the given V_{gs}.

Table 4.13 indicated that most of the first order SPICE parameters (i.e. V_{t0}, γ, L_{del}, ΔW) are well matched even when derived through the pass transistor. As can be seen from table 4.14 it is clear that a better representation of the I_{ds} : V_{ds} curves is gained by using a larger geometry pass transistor. Table 4.14 also shows that direct terminal measurement itself will not give ideal matching between measured and SPICE generated curves (column marked 'Terminal Measurement'). Increasing the size of the pass transistor *ad infinitum* is not a viable solution to the measurement problem, since area is obviously at a premium. As had been demonstrated by simulation the current through the test device is limited because V_{gs} of the pass transistor never reaches $5V$ because of the voltage drop across the device being measured. One possible solution to this is to increase the gate voltage on the pass transistor. This was investigated, again using the circuit in figure 4.19, with a minimum geometry ($6 \times 6\mu m$) test transistor. Sets of I_{ds} : V_{ds} curves were then obtained for gate voltages between $5V$ and $9V$ on the current pass transistor. Characteristics were obtained for both a $48 \times 6\mu m$ and a $120 \times 6\mu m$ pass transistor. This is summarised by table 4.15. The results for the $48 \times 6\mu m$ and $120 \times 6\mu m$ transistors are shown by figures 4.22 and 4.23, respectively, with the RMS percentage errors of the measured curves from those found by direct measurement given by tables 4.16 and 4.17.

Pass Transistor Aspect Ratios	Pass Transistor V_g
8:1	5,6,7,8,9V
20:1	5,6,7,8,9V

Table 4.15. Summary of experimental set up for measurement of 6 × 6μm test transistor with different pass transistor gate voltages.

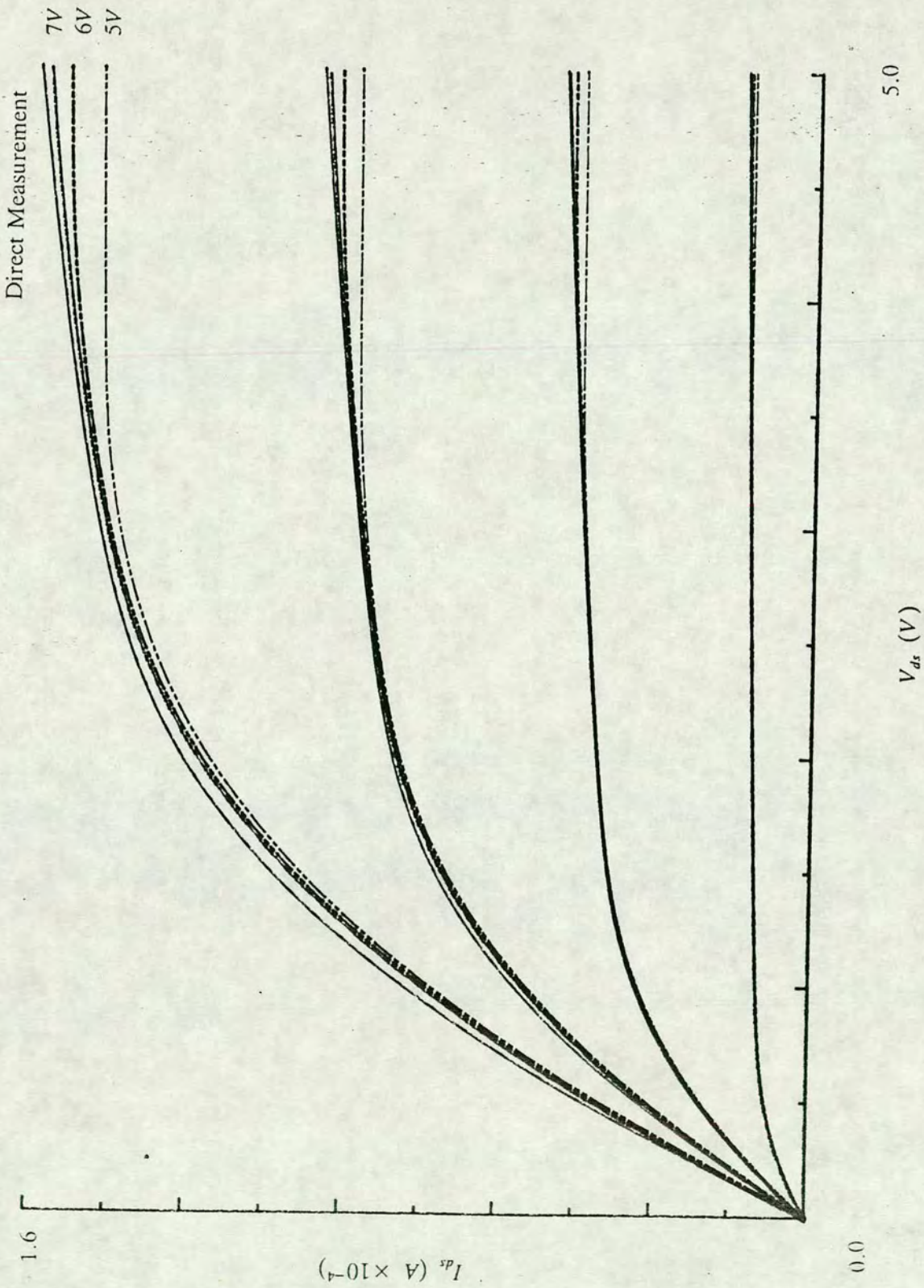


Figure 4.22. Plot of I_{ds} : V_{ds} for 6 × 6μm test transistor measured directly and through the 48 × 6μm pass transistor at the indicated gate voltages.

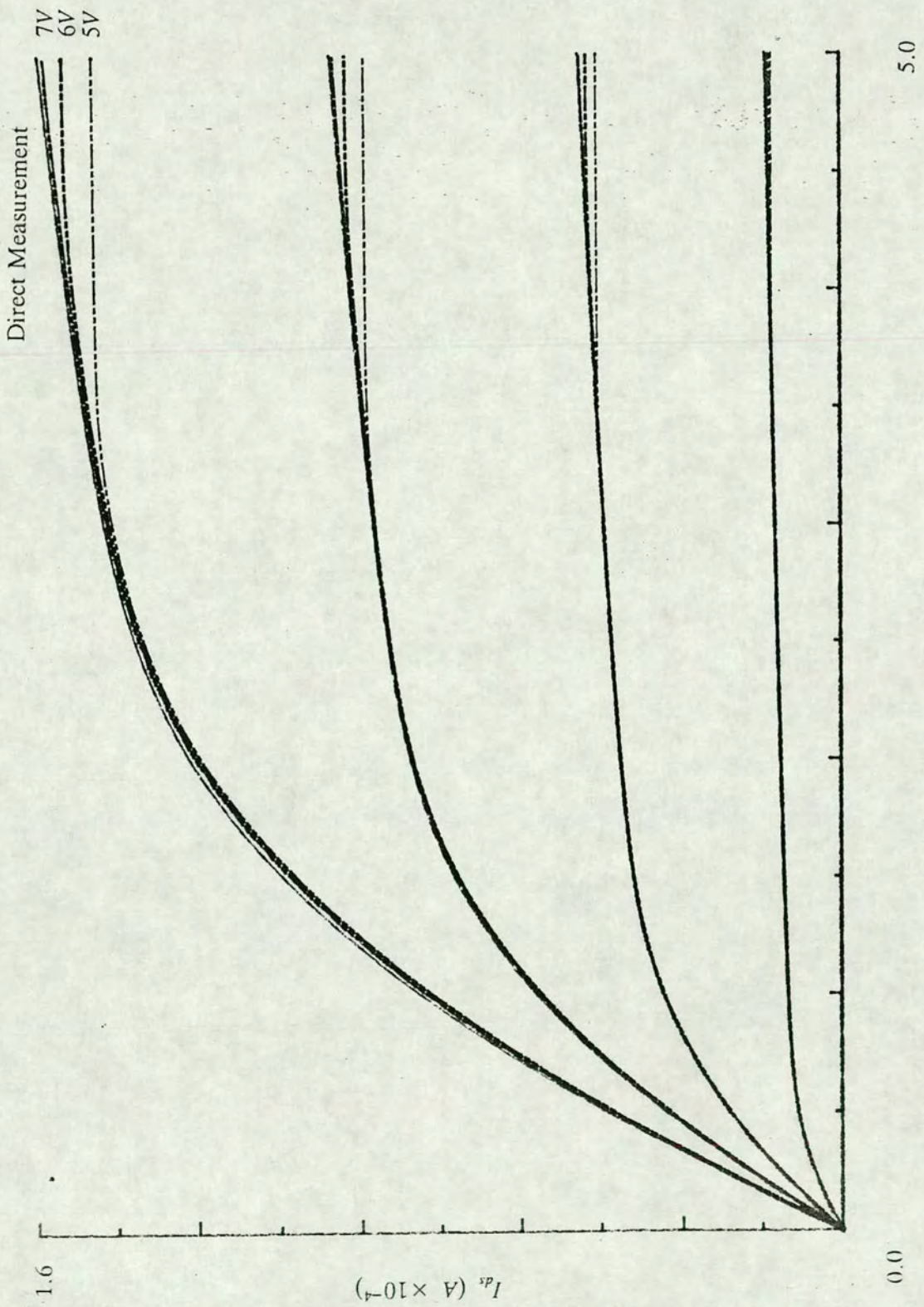


Figure 4.23. Plot of I_{ds} : V_{ds} for 6 × 6μm test transistor measured directly and through the 120 × 6μm pass transistor at the indicated gate voltages.

V_{gs} (*Volts*)	Average RMS % Error from the Measured Characteristic				
	Pass Transistor Gate Voltage				
	5V	*6V*	*7V*	*8V*	*9V*
2.0	2.2	0.8	0.4	0.4	0.4
3.0	2.6	1.2	0.7	0.6	0.5
4.0	3.8	2.2	1.5	1.2	1.2
5.0	5.5	3.4	2.5	2.1	2.0

Table 4.16. RMS % error from directly measured I_{ds} : V_{ds} curves for those measured through 48 × 6μm pass transistor for the indicated gate voltage and V_{gs}.

V_{gs} (*Volts*)	Average RMS % Error from the Measured Characteristic				
	Pass Transistor Gate Voltage				
	5V	*6V*	*7V*	*8V*	*9V*
2.0	1.7	0.4	0.3	0.2	0.1
3.0	1.6	0.6	0.4	0.1	0.2
4.0	2.2	1.0	0.7	0.4	0.5
5.0	3.0	1.6	1.1	0.8	0.8

Table 4.17. RMS % error from directly measured I_{ds} : V_{ds} curves for those measured through 120 × 6μm pass transistor for the indicated gate voltage and V_{gs}.

SPICE parameters for the test transistor were extracted at each of these pass transistor gate voltages and are shown in tables 4.18 and 4.19 for the 48 × 6μm and 120 × 6μm pass transistor cases respectively. These were then used to generate characteristic curves for the transistors. Figures 4.24 and 4.25 show the simulated curves for measurements made directly and through the pass transistors at various gate voltages for the respective 48 × 6μm and 120 × 6μm cases. The RMS errors for these simulated, SPICE derived curves and the real, directly measured curves are given by tables 4.20 and 4.21. From these results it can be observed that a higher gate voltage on the pass transistor partly seems to alleviate the problem with the voltage drop across the test transistor. As the gate voltage on the pass transistor is increased these measurements approach those made by direct measurement on the test transistor. A closer examination of the extracted SPICE parameters, in particular the SPICE parameter κ, supported this. As described in appendix 2 κ is the SPICE parameter which characterises the slope of the I_{ds} : V_{ds} curve in the saturation region. Figure 4.26 plots this variation of κ with pass transistor gate voltage. It

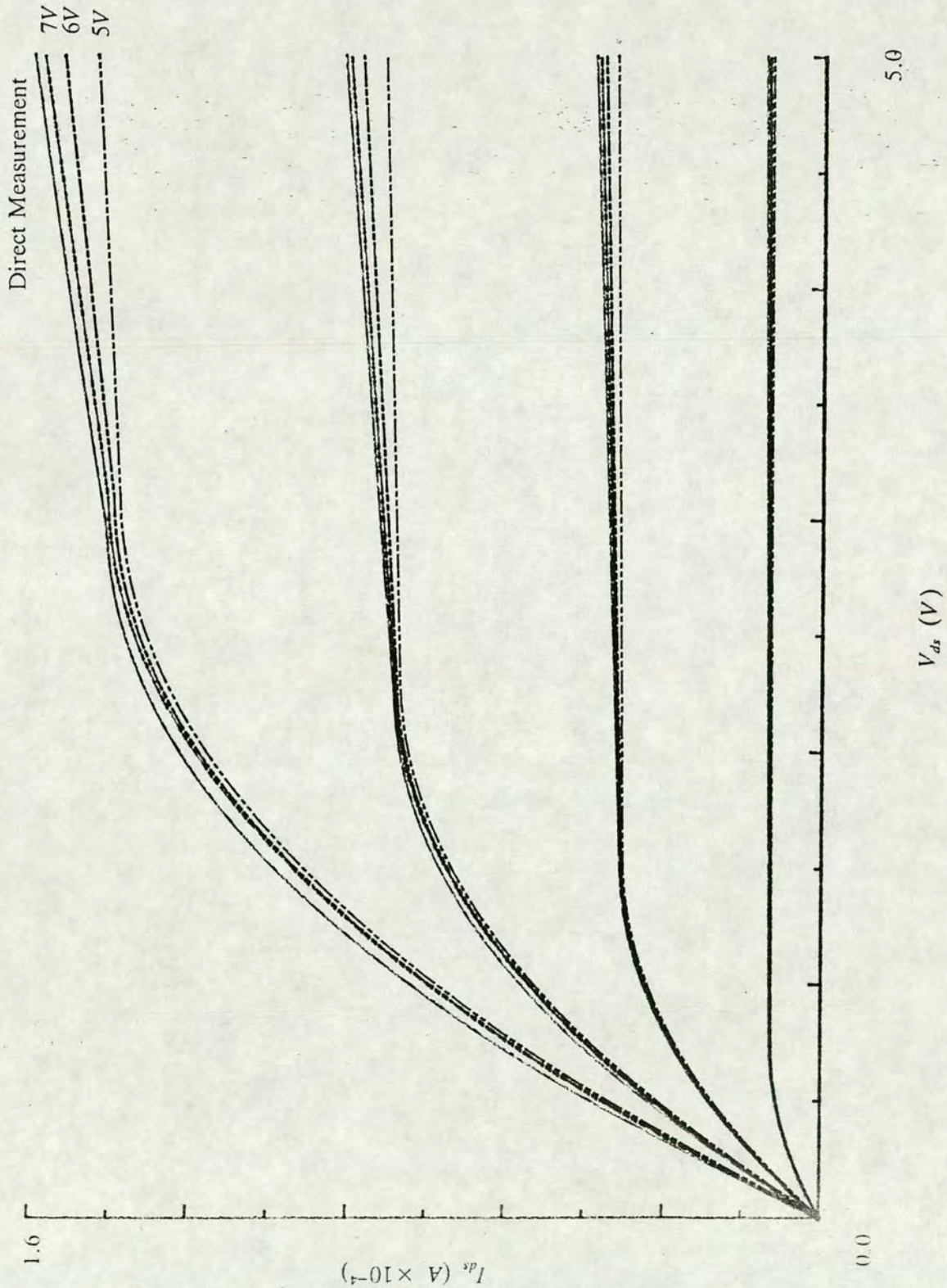


Figure 4.24. Plot of resimulated curves of I_{ds} : V_{ds} for 6 × 6μm test transistor using parameters derived by direct measurement and those derived via the 48 × 6μm pass transistor at the indicated gate voltages.

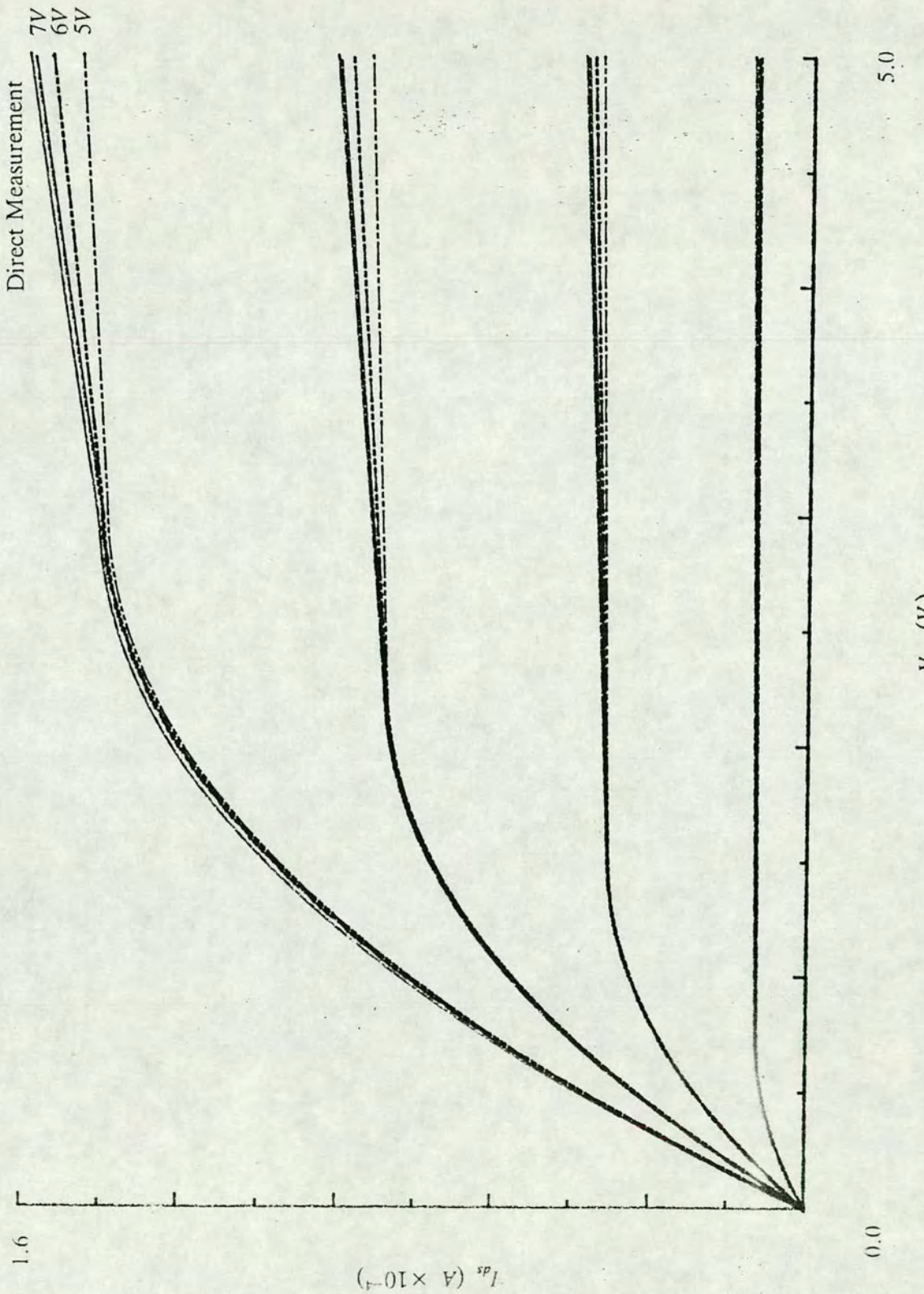


Figure 4.25. Plot of resimulated curves of I_{ds} : V_{ds} for 6 × 6μm test transistor using parameters derived by direct measurement and those derived via the 120 × 6μm pass transistor at the indicated gate voltages.

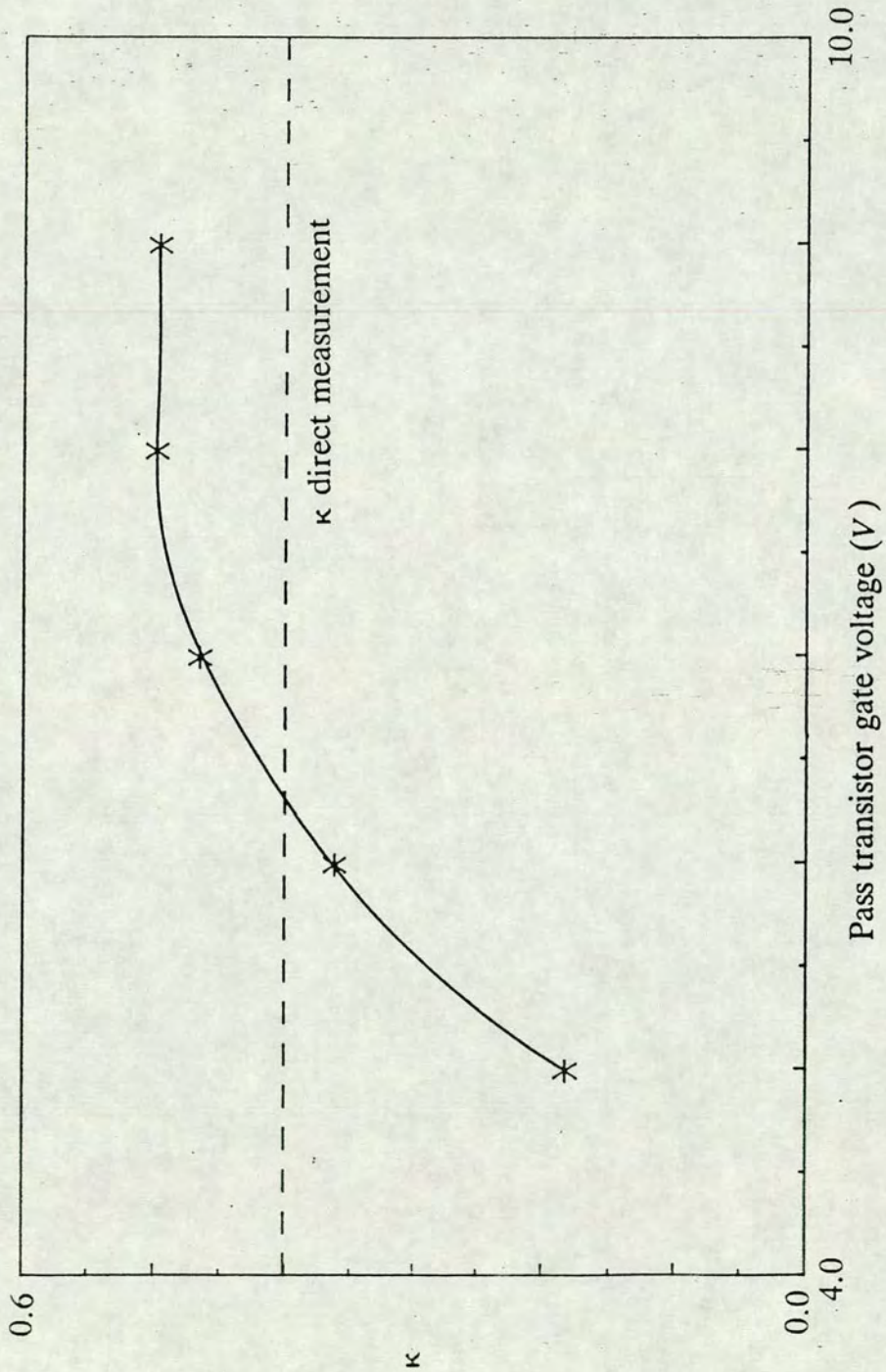


Figure 4.26. The effect of pass transistor gate voltage on SPICE parameter κ.

SPICE Parameters	Measured at the Transistor Terminals	Measured Through the Pass Transistors				
		Pass Transistor Gate Voltage				
		5V	6V	7V	8V	9V
N_{fs} (m^{-2})	1.0×10^{15}	2.72×10^{15}	2.66×10^{15}	2.81×10^{15}	2.56×10^{15}	2.80×10^{15}
V_{t0} (V)	1.03	1.05	1.06	1.06	1.06	1.06
γ $(\sqrt{V})$	0.65	0.53	0.60	0.59	0.60	0.61
L_{del} (m)	1.35×10^{-6}	1.35×10^{-6}	1.35×10^{-6}	1.35×10^{-6}	1.35×10^{-6}	1.35×10^{-6}
ΔW (m)	1.47×10^{-6}	1.47×10^{-6}	1.47×10^{-6}	1.47×10^{-6}	1.47×10^{-6}	1.47×10^{-6}
μ_0 $(m^2V^{-1}s^{-1})$	0.085	0.087	0.087	0.087	0.088	0.087
θ (V^{-1})	0.051	0.088	0.083	0.081	0.080	0.078
V_{max} (ms^{-1})	4.28×10^5	8.06×10^5	7.14×10^5	8.22×10^5	6.81×10^5	7.68×10^5
η	0.159	0.066	0.106	0.132	0.136	0.141
δ	0.367	0.478	0.365	0.392	0.386	0.358
κ	0.402	0.240	0.456	0.643	0.595	0.642

t_{ox} $(m) = 8.5 \times 10^{-8}$ and X_j $(m) = 1.0 \times 10^{-6}$ (non-measured parameters used)

Table 4.18. SPICE parameters measured directly at the test transistor terminals and those measured via the 48 × 6μm pass transistor for the noted gate voltages.

SPICE Parameters	Measured at the Transistor Terminals	Measured Through the Pass Transistors				
		Pass Transistor Gate Voltage				
		5V	6V	7V	8V	9V
N_{fs} (m^{-2})	1.0×10^{15}	3.08×10^{15}	2.97×10^{15}	2.97×10^{15}	2.77×10^{15}	2.93×10^{15}
V_{t0} (V)	1.03	1.05	1.06	1.06	1.06	1.06
γ $(\sqrt{V})$	0.65	0.60	0.59	0.60	0.62	0.62
L_{del} (m)	1.35×10^{-6}	1.35×10^{-6}	1.35×10^{-6}	1.35×10^{-6}	1.35×10^{-6}	1.35×10^{-6}
ΔW (m)	1.47×10^{-6}	1.47×10^{-6}	1.47×10^{-6}	1.47×10^{-6}	1.47×10^{-6}	1.47×10^{-6}
μ_0 $(m^2V^{-1}s^{-1})$	0.085	0.088	0.088	0.088	0.087	0.087
θ (V^{-1})	0.051	0.072	0.071	0.070	0.068	0.067
V_{max} (ms^{-1})	4.28×10^5	5.15×10^5	5.44×10^5	5.23×10^5	5.79×10^5	5.69×10^5
η	0.159	0.068	0.099	0.121	0.137	0.134
δ	0.367	0.375	0.402	0.386	0.339	0.329
κ	0.402	0.181	0.361	0.464	0.497	0.495

t_{ox} $(m) = 8.5 \times 10^{-8}$ and X_j $(m) = 1.0 \times 10^{-6}$ (non-measured parameters used)

Table 4.19. SPICE parameters measured directly at the test transistor terminals and those measured via the 120 × 6μm pass transistor for the noted gate voltages.

would be expected that κ would increase rapidly between $5V$ and $6V$ and, as the gate voltage on the pass transistor increased further, approach the value extracted from direct measurement on the test transistor. This was found to be the case although there is a small overshoot which can be attributed to variations in other parameters offsetting the slightly increased value of κ.

V_{gs} (*Volts*)	Average RMS % Error of the Simulated from the Measured Characteristic					
	Terminal Measurement	Pass Transistor Gate Voltage				
		5*V*	6*V*	7*V*	8*V*	9*V*
2.0	11.4	16.9	14.4	13.9	13.3	13.4
3.0	6.3	10.2	8.0	7.3	6.5	6.8
4.0	2.5	6.9	4.9	4.1	3.5	3.5
5.0	0.6	5.6	3.8	3.0	2.5	2.4

Table 4.20. RMS % error of the resimulated curve with the measured curve for direct measurement and via a 48 × 6μm pass transistor for the noted gate voltages and V_{gs}.

V_{gs} (*Volts*)	Average RMS % Error of the Simulated from the Measured Characteristic					
	Terminal Measurement	Pass Transistor Gate Voltage				
		5*V*	6*V*	7*V*	8*V*	9*V*
2.0	11.4	15.7	14.9	14.0	13.4	13.5
3.0	6.3	8.9	7.6	6.7	6.5	6.5
4.0	2.5	5.2	3.9	3.0	2.9	2.8
5.0	0.6	3.4	2.2	1.6	1.4	1.3

Table 4.21. RMS % error of the resimulated curve with the measured curve for direct measurement and via a 120 × 6μm pass transistor for the noted gate voltages and V_{gs}.

4.8. Conclusions

The results obtained have shown that it is feasible to implement a switching matrix on-chip through which transistor characteristics can be measured. The extraction of SPICE parameters provides a realistic use and it has been demonstrated that these parameters can be extracted with an accuracy comparable to those derived using conventional techniques. This makes it possible to measure process control chips with equipment without a switching matrix. Individual devices are addressed through pass transistors and, with fewer pads required, these test chips can be designed to occupy a reduced area.

References

1. M.G. Buehler, "Comprehensive Test Patterns with Modular Test Structures: The 2 by N Probe-pad Array Approach," *Solid State Technology*, pp. 89-94, October 1979.

2. L.W. Linholm, "The Design, Testing and Analysis of a Comprehensive Test Pattern for Measuring CMOS/SOS Process Performance and Control," *Semiconductor*

Measurement Technology : NBS Special Publication, no. 400-66, August 1981.

3. A.J. Walton, J.M. Robertson, R. Holwill, and B. Moore, "On Chip Switching for DC Parametric Testing," *Electronics Letters*, vol. 21, no. 10, pp. 422-423, May 1985.

4. M.G. Buehler and H.R. Sayah, "Addressable Inverter Matrix for Process and Device Characterisation," *Solid State Technology*, pp. 185-191, May 1985.

5. B.R. Blaes, "CMOS Timing Sampler Array for Measuring Circuit Delays," *Proc. of IEEE VLSI Workshop on Test Structures*, pp. 208-227, Long Beach, California, February 1986.

6. A. Nishimura, S.S. Mahant Shetti, J. Givens, E. Born, R. Haken, R. Chapman, and P. Chaterjee, "Multiplexed Test Structure ; A Novel VLSI Technology Development Tool," *Proc. of IEEE VLSI Workshop on Test Structures*, pp. 336-355, Long Beach, California, February 17-18, 1986.

7. M.G. Buehler, B.T. Moore, and R.H. Nixon, "Parameter Extraction from Spaceborne MOSFETs," *IEEE Trans. on Nuclear Science*, vol. NS-32, no. 6, pp. 4237-4243, December 1985.

8. M.G. Buehler, "JMOSFIT : A MOSFET Transistor Parameter Extractor," *Proc. of IEEE VLSI Workshop on Test Structures*, pp. 475-496, Long Beach, California, February 1986.

9. L.W. Nagel, "SPICE 2 : A Computer Program to Simulate Semiconductor Circuits," *Memo. No. UCB/ERL M510*, Electronics Research Laboratory, College of Engineering, University of California, Berkley, May 1975.

10. A. Vladimirescu and S. Liu, "The Simulation of MOS Integrated Circuits Using SPICE 2," *Memo. No. UCB/ERL MBO/7*, Electronics Research Laboratory, College of Engineering, University of California, Berkley, February 1980.

11. W. Maes, K. De Meyer, and L. Dupas, "SIMPAR: A Parameter Extraction Program to be used for any User-defined Analytical Expression in the Field of Process and Device Modelling," *Proc. of 15th European Solid State Device Research Conference, ESSDERC 85*, pp. 153-154, Aachen, September 1985.

12. K. Doganis and D.L. Scharfetter, "General Optimization and Extraction of IC Device Model Parameters," *IEEE Trans. Electron Devices*, vol. ED-30, no. 9, pp. 1219-1228, September 1983.

13. E. Khalily, P. Decher, and A. Darell, "TECAP 2: An Interactive Device Characterization and Model Development System," *Hewlett Packard Technical Data*, 1985.

14. A.L. Silburt, "Automated Parameter Extraction and Modelling of the MOSFET below Threshold," *Proc. of 15th European Solid State Device Research Conference, ESSDERC 85*, pp. 160-161, Aachen, September 1985.

15. C.A. Bloom, *1986 Product Seminar,* TMA, Palo Alta, 26th August 1986.

16. A. Gribben, J.M. Robertson, and A.J. Walton, "Accurate Physical Parameter Extraction for Small Geometry Devices," *Proc. of Semiconductor International Conference (SEMICON)*, pp. 186-202, Birmingham, 1986.

Chapter 5

Electrical Verniers and Output Circuitry

5.1. Introduction

Measurement of layer to layer misregistration in silicon wafers has until recently mainly been achieved using analogue structures. Typical of these being the tap structure utilised by Buehler, figure 5.1 [1,2] and the van der Pauw structures developed by Perloff, figure 5.2 [3,4]. In both cases measurement relies on the homogeneity of width, thickness and conduction of an area of material formed by a single conducting layer. As minimum geometries and absolute dimensions shrink the control of these variables becomes more problematical. This is because smaller absolute tolerances are required which leads to larger potential measurement inaccuracies.

This has led directly to the interest in use of digital measurement structures for layer to layer misregistration measurements. Irrespective of their specific design these digital structures all have several aspects in common. They have a number of elements, each of which has the critical test feature with an incrementally increasing pitch. Depending on the total number of such elements, the 'window' of misalignment (the total range of measurement) which it is capable of measuring is given by the number of elements and their pitch. As an example if a pitch of $0.05\mu m$ is chosen between adjoining elements and the complete structure consists of 41 elements then the misalignment window is $2\mu m$. Assuming a zero offset for the central element then the measurement of misalignment is in the range of $\pm 1\mu m$. This can be expressed as follows,

$$pitch \times (number\ of\ elements - 1) = window \tag{5.1}$$

The subtraction of one from the number of elements allows for the central element. Substituting values for the example given above gives,

$$0.05 \times (41 - 1) = 2\mu m = \pm 1\mu m \tag{5.2}$$

The advantage of digital measurement structures is that the pitch, number of elements and central offset can all be chosen at the design stage. The only parameter limiting the

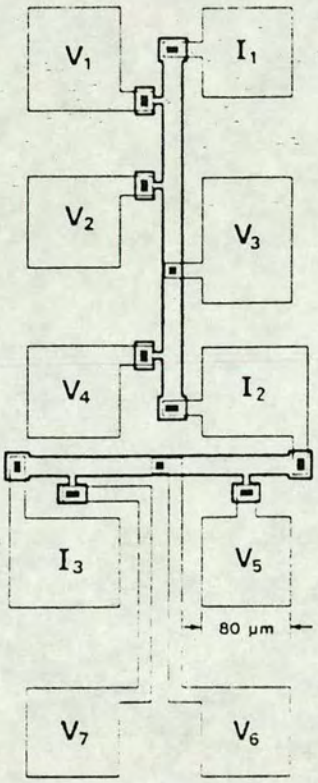


Figure 5.1. Analogue misalignment measuring structure developed by Buehler. After [1].

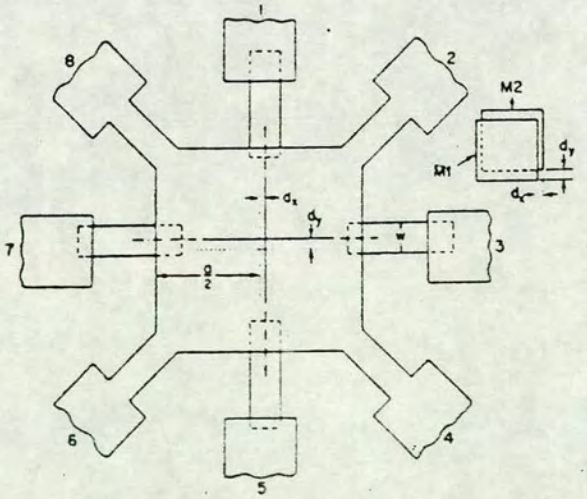


Figure 5.2. Analogue misalignment measuring structure developed by Perloff. After [3].

performance of these test structures is its minimum dimensions defined by the lithography. Other process variables which limit analogue structures are not applicable. The pitch can be chosen as small as deemed necessary at the design stage and, with a suitable choice of number of elements per structure, can characterise misalignment to the required resolution. The main obstacle to using digital structures is that a single misalignment structure, which may have only required six pads for an analogue measurement, would now appear to require a larger number of output pads. A structure which had N digital elements requires a minimum of N + 1 pads, when all its inputs are discrete and all outputs commoned. Figure 5.3 shows this schematically. Obviously a structure with this number of pads would not be feasible, so a solution involving interface circuitry is required to reduce the potential number of pads to a usable number.

5.2. The Origins of Digital Structures

Electrically measured vernier structures for misalignment measurement are a development from the use of optical verniers for a similar purpose. Optical verniers must be manually measured hence data acquisition is slow and repeatability may be questioned. A conventional optical vernier, shown by figure 5.4, has two sets of interleaved teeth of differing periodicity. When misalignment occurs one set of these is displaced relative to the other and the displacement of the 'just touching' tooth from its designed place, is the component of misalignment in that direction. Unfortunately this will only work if there is no relative over/underetch between the two layers. If this occurs then a false reading will result. This is illustrated by figure 5.5 which shows a conventional vernier which *could* be electrically tested by sequentially checking each vernier element for continuity. Figure 5.5a) shows this vernier with no overetch and zero misalignment while figure 5.5b) shows how this same vernier would give a false reading of $0.4\mu m$ misalignment where both layers have been overetched by $0.2\mu m$. To overcome this it is necessary to utilise a vernier design which will account naturally for any such relative over/underetching between layers.

One of the first uses of digital structures outlined in the literature was a digital vernier structure for measuring layer to layer misalignment [5]. Figure 5.6 shows this structure which allowed compensation for overetching between layers with output achieved by using a parallel load shift register. A ten pad 'footprint' was required with separate structures needed to derive the X and Y misalignment components. This vernier structure formed the basis for the work of this chapter and hence its detailed operation is described later.

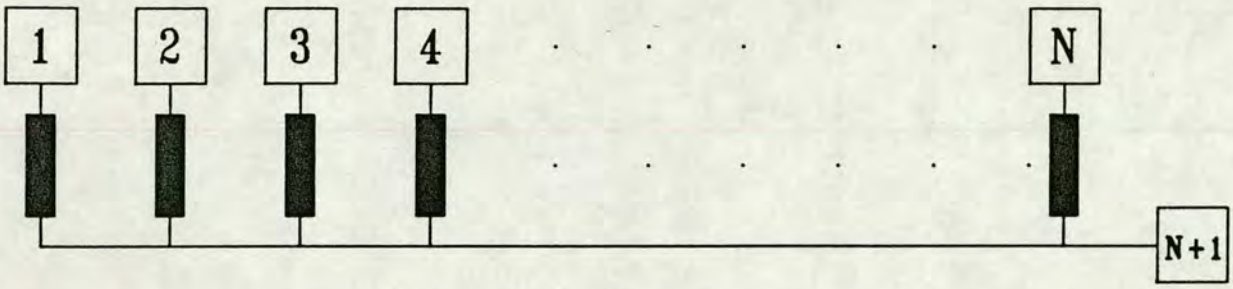


Figure 5.3. N test structure elements accessed by N + 1 pads.

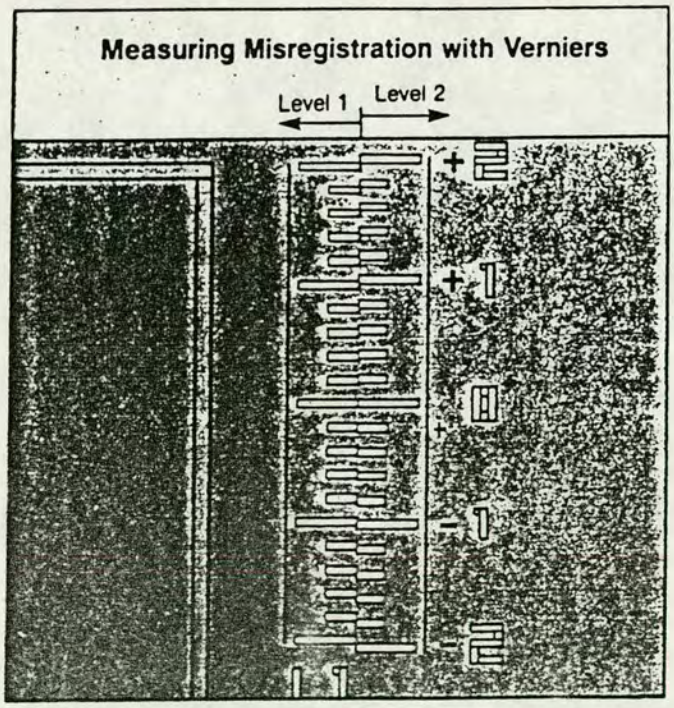


Figure 5.4. An optically measured vernier. After [50, chapter 3].

A derivative of this idea was used to measure polysilicon to diffusion misalignment [6]. Instead of a vernier tooth the digital element was a set of transistors. Figure 5.7 shows how this functioned. These have the polysilicon gate offset within each element of the complete structure. Thus at some point along the row of elements conduction will occur along the diffusion element due to current flowing round the end of the gate region. The net result, illustrated by figure 5.8, of this is an area of elements which are electrically off sandwiched between two regions where the elements are on. Misalignment, in the given direction, is found from the displacement of the 'as-designed' zero misalignment position from that of the measured position. A complete misalignment vector requires separate structures for the X and Y directions, each structure requiring a ten pad 'footprint'.

A tapered comb structure was devised by Yamaguchi *et al.* to digitally measure misalignment [7]. This structure which is formed using a minimum of three layers is shown by figure 5.9. The relative displacement of the central region relative to the two tapered comb structures, either side of it, defines the magnitude of the misalignment. This magnitude is deduced by ascertaining the number of contacts electrically connected to the left of the central structure and subtracting this from the number on the right. As this number contains positional information only and is independent of any relative layer to layer overetch, the misalignment (M) is given by,

$$M = (N_R - N_L) \times \frac{S}{2} \tag{5.3}$$

where N_R and N_L are the number of electrically connected elements to the right and left respectively of the central region and S is the pitch of the digital elements. The output from each stage was loaded to a shift register before serial output.

An electrical vernier was used by Nishimura *et al.* for misalignment measurement in their digitally addressed test chip [8]. 120 sites in X and a similar number in Y were used with a pitch of $0.04\mu m$ to measure contact to polysilicon and contact to diffusion alignment error. Figure 5.10 shows the particular construction of the vernier. Other digital structures were employed to gather data for degree of process maturity and design rule checking. Output was made with use of row and column multiplexers to access each individual element.

A test structure for measuring contact size using digital means has been described by Freeman and Lukaszek [9, 10]. This structure can also measure polysilicon to contact

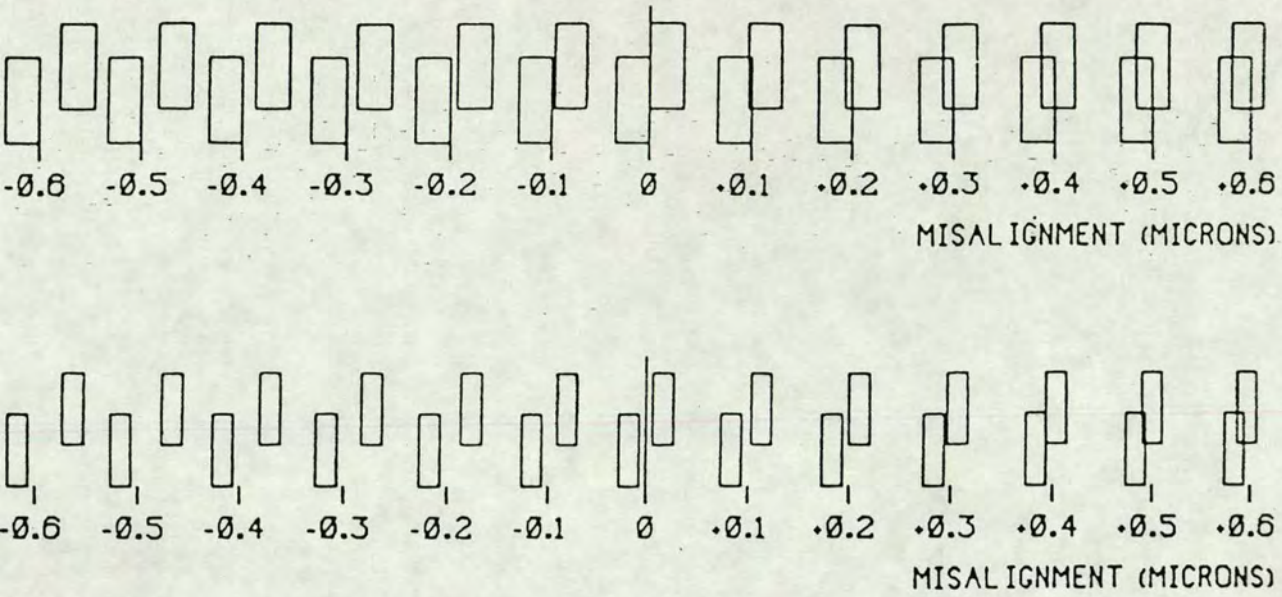


Figure 5.5. A conventional vernier showing no overetch (top) and 0.2μm overetch (bottom) with zero misalignment in both cases. After [11].

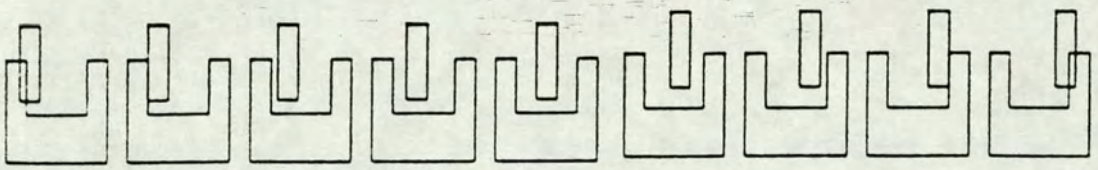


Figure 5.6. Digital vernier using U-shaped tooth which compensates for layer overetch.

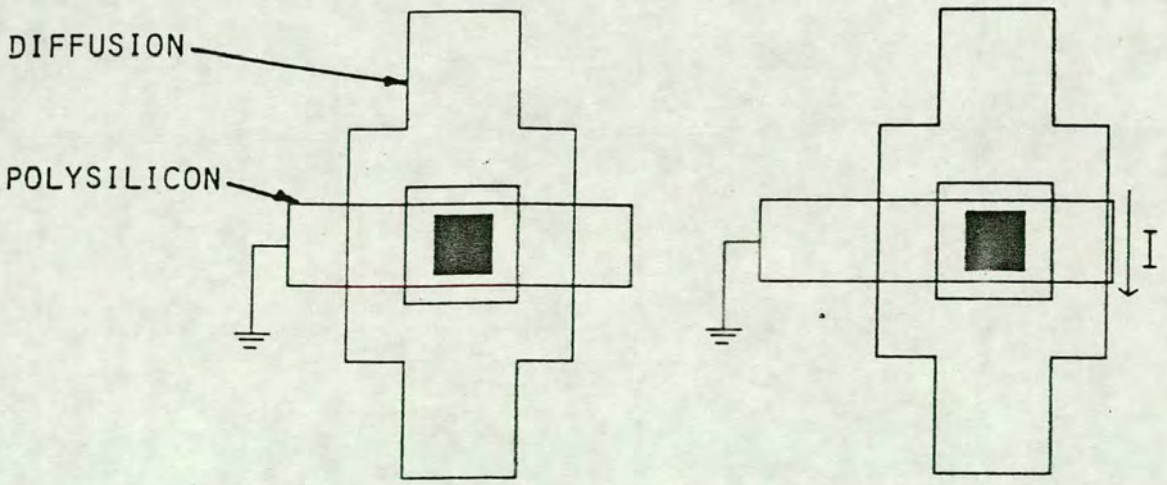


Figure 5.7. Principle of operation of transistors used for polysilicon to diffusion misalignment measurement. Shown are a non-conducting (left) and conducting transistor (right). After [6].

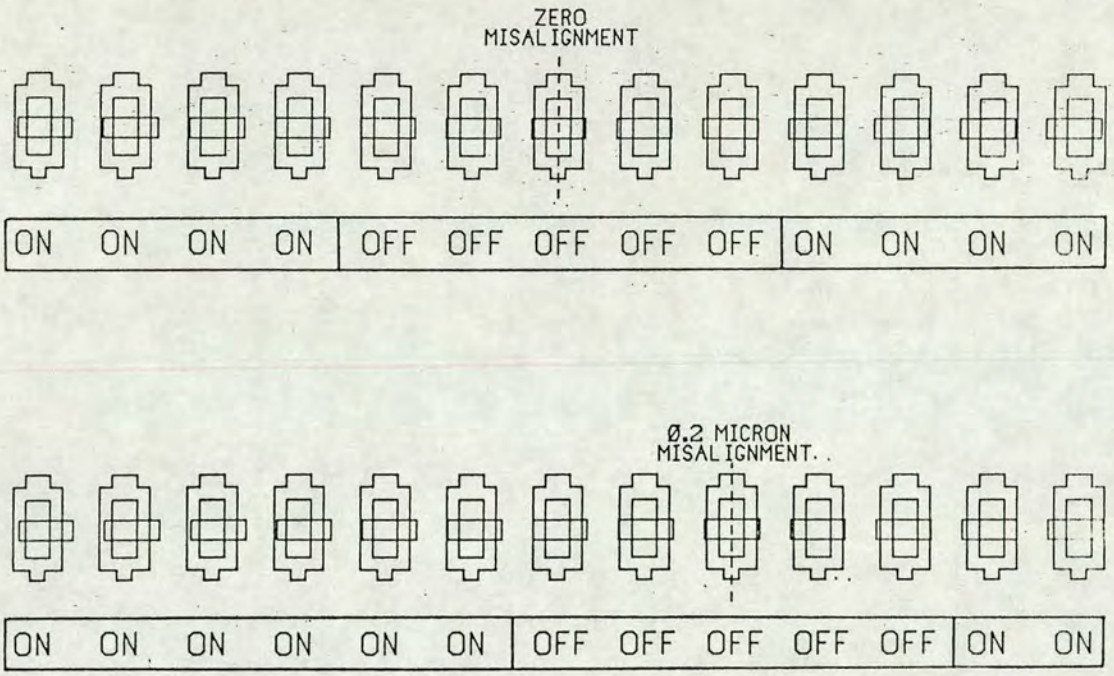


Figure 5.8. Array of transistors used to measure misalignment showing zero (top) and +0.2μm (bottom) misalignment. After [6].

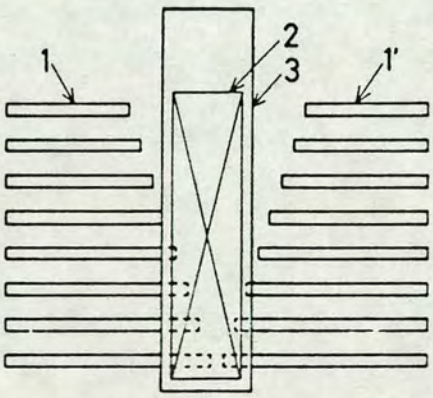


Figure 5.9. Tapered comb structure used for misalignment measurements. Areas 1 and 1′ are the comb elements, area 2 the contact hole and area 3 metallisation. After [7].

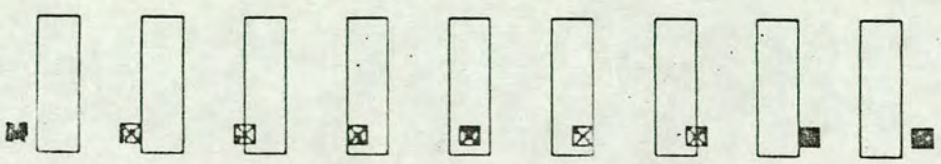


Figure 5.10. Misalignment vernier structure used by Nishimura et al. After [8].

alignment as well as polysilicon linewidth. The structure, shown in figure 5.11, is similar in concept and design to that of Yamaguchi [7]. Contact width (W_C) was determined by locating the two contacts on either side which 'just' touched the central polysilicon region. As the designed distance between these two contact centres (D_C) is known the polysilicon width of the central region (W_P) is thus found and will indicate any under/overetch of the polysilicon. The contact width is then given by,

$$W_C = D_C - W_P \tag{5.4}$$

Misalignment could also be measured with this structure in the same way as Yamaguchi. Output was achieved through a multiplexing scheme which allowed individual elements to be isolated without the need for active on chip circuitry. Figure 5.12 depicts this scheme. This multiplexing idea formed the basis of the [illegible] scheme discussed later in this chapter and explained in more detail there.

5.3. The Digital Vernier

As illustrated in the previous section it is necessary to design digital misalignment structures so that any relative overetch between the measured layers is allowed for. A design to achieve this has been devised which utilises a U-shaped tooth [5, 11]. Figure 5.13 illustrates how this structure works with a vernier which has a $0.1\mu m$ pitch. In figure 5.13a) the case of no overetch and zero misalignment is depicted. With $+0.2\mu m$ misalignment, figure 5.13b), the central 'bar' pattern can be seen to have moved $0.2\mu m$ to the right and the bar which 'just fits' the U-tooth with no overlap is the tooth corresponding to the $+0.2\mu m$ mark. With $0.3\mu m$ relative overetch it can be seen in figure 5.13c) that the elements $-0.1\mu m$ and $+0.5\mu m$ are now the ones 'just touching' and all intermediate elements have no overlap between layers. The misalignment is then found as the central point of this region with no layer overlap. Numerically this can be calculated as,

$$-0.1 + \frac{0.5 - (-0.1)}{2} = +0.2\mu m \tag{5.5}$$

If the overetch were of a different magnitude the same end result for misalignment would occur.

In figure 5.13a) and b) it is clear that this vernier could be read optically but that electrical implementation requires a tooth which is slightly narrower than the gap in the U-

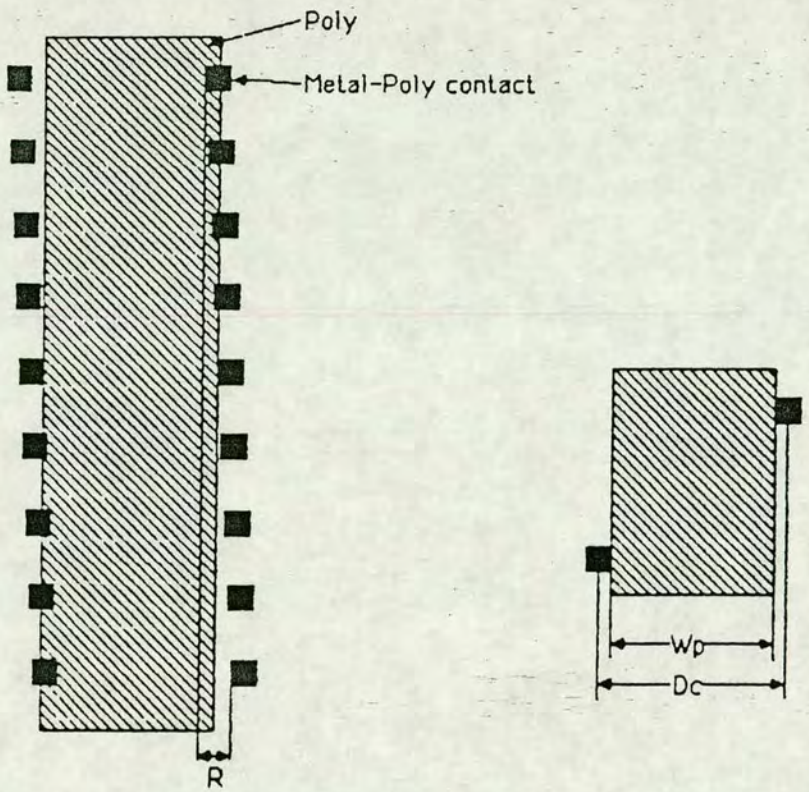


Figure 5.11. Structure used by Freeman and Lukaszek to measure contact hole size and polysilicon to contact misalignment. After [9].

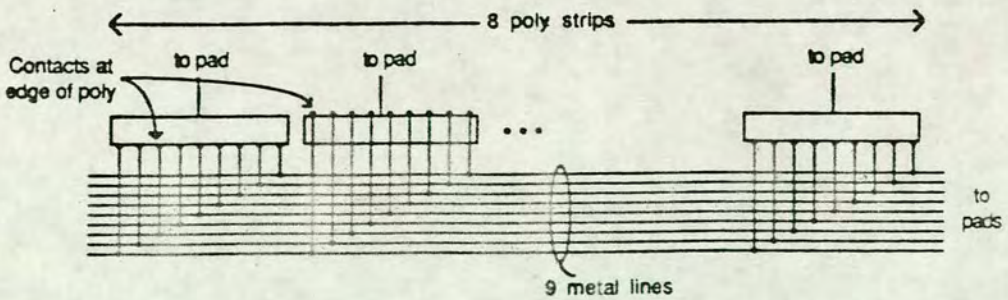


Figure 5.12. Output scheme utilised by Freeman and Lukaszek. After [9].

tooth. This can be brought about purely by relative overetch, as shown in figure 5.13c), or by deliberately designing the tooth smaller. In practice this depends on the relative overetch expected between the two layers implemented in the vernier and the designed gap size. The vernier must be designed with the aim that the area of elements where there is no layer to layer contact does not extend past either of the two end elements of the vernier otherwise all positional information is lost. Thus the vernier must be designed such that the potential combination of misalignment and overetch does not cause this to occur.

Testing this vernier electrically will result in outputs such as shown in figure 5.14 which could be obtained by testing the continuity between each layer for each vernier element. The electrical output shown in figure 5.14a) corresponds to a case where there is zero misalignment and no overetch but as the bar and U-tooth has been designed such that the bar is $0.4\mu m$ smaller than the tooth the given output results. With $0.2\mu m$ misalignment figure 5.14b) shows that this output is merely that depicted in a) but shifted two elements to the left. Introducing $0.3\mu m$ relative overetch, as shown by figure 5.14c), as well as $+0.2\mu m$ misalignment gives the output of figure 5.14c). The overetch has the effect of increasing the number of disconnected vernier elements. As this increased number of elements is symmetrical it can be seen that the centre of the open circuit portion does not move, hence positional information is retained. Thus as this information represents the misalignment the structure is seen to compensate for relative overetch between the verniers constituent layers.

In common with all digital structures both the pitch (the variation in tooth offset along the vernier structure) and the range (the number of elements in each structure) of the vernier are only limited by the process lithography. The vernier concept is also independent of technology and could be applied to any although here, in this work, it was implemented on the EMF $6\mu m$ NMOS process.

5.4. Vernier Design

Vernier element layout for measuring misalignment can be demonstrated as follows. A vernier element to measure misregistration between a conductor and contacts is shown in figure 5.15. The U-tooth is set out in the conductive layer and the central 'bar' delineated by the contact. To make electrical continuity between the layers the contact area is then covered in metal. For this construction figure 5.16 shows cross-sections of the two possible

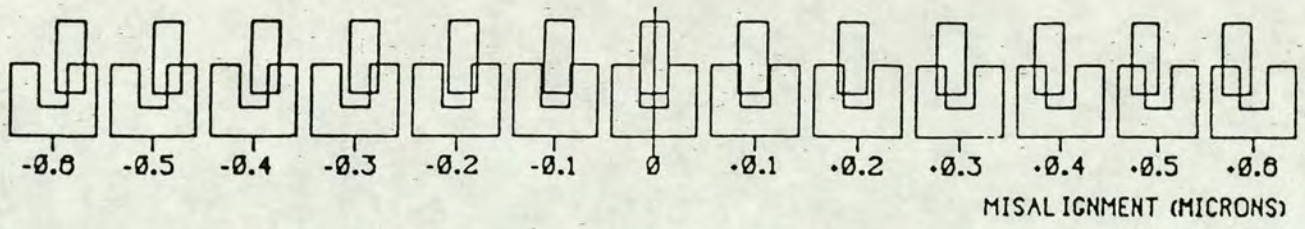


Figure 5.13a) Vernier showing no overetch and zero misalignment. After [11].

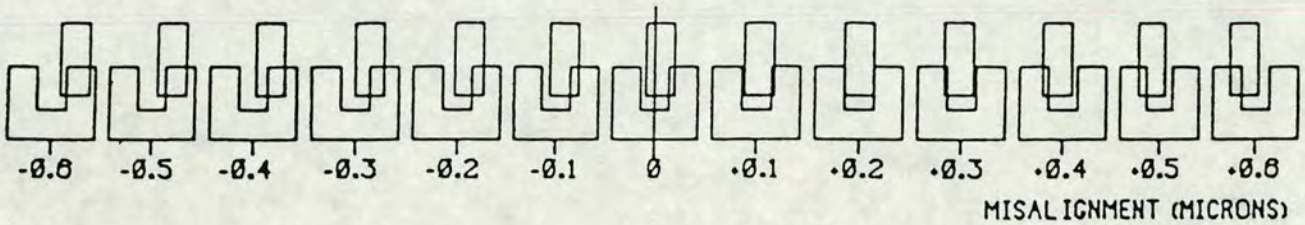


Figure 5.13b) Vernier showing no overetch with +0.2μm misalignment. After [11].

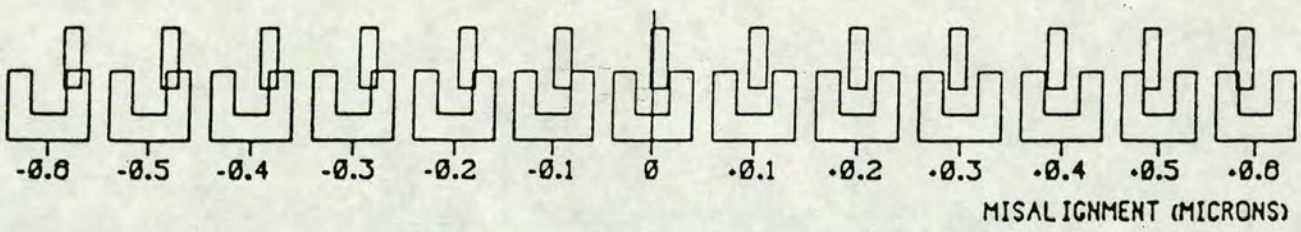


Figure 5.13c) Vernier showing +0.3μm overetch with +0.2μm misalignment. After [11].

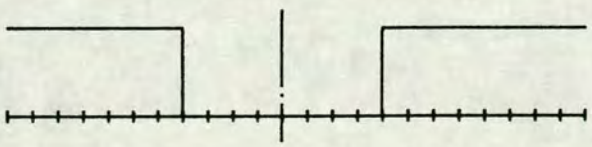


Figure 5.14a) Electrical output of vernier structure with 0.4μm zero offset showing no overetch and zero misalignment.

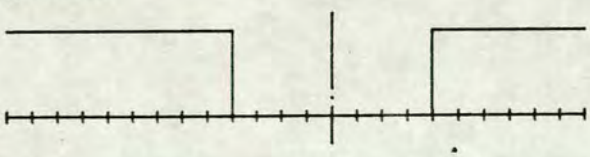


Figure 5.14b) Same vernier as a) showing no overetch with +0.2μm misalignment.

Figure 5.14c) Same vernier as a) showing +0.3μm overetch with +0.2μm misalignment.

cases where there is no contact (switch open) and contact (switch closed). This structure can be used for measurement between the following layers: contact to diffusion, contact to polysilicon, contact to metal and metal 1 to via (for a two layer metal process). Layouts to measure misalignment between two conducting layers require a different layout from the above. A suitable construction for this is shown by figure 5.17, where one of the conducting layers forms the 'bar' while the other forms the U-tooth. So that electrical contact can be made between the two layers the whole area of at the centre of the tooth is delineated as a contact region between the two conductors. The two possible cases of switch open and switch closed are shown in cross-section by figure 5.18. Metal to polysilicon and metal 1 to metal 2 misalignment can be found using this construction. For a self-aligned silicon gate process the vernier structure can be adapted to measure the misalignment between the gate and diffusion (active area). Figure 5.19 shows a structure which is capable of doing this and is similar to the structure proposed by Walton *et al.* [6]. The polysilicon of each element is offset along the line of elements forming the complete structure. With the switch open the polysilicon completely covers the active area and as the polysilicon is earthed no current will flow through the diffusion (i.e. this is essentially a transistor with zero gate voltage and thus off). With the switch closed the polysilicon is offset exposing the active area to the source-drain implant. This results in a conductive path around the polysilicon, allowing current to flow to turn the switch on. Cross-sectional views of the on and off cases are shown by figure 5.20.

A single vernier structure will clearly only give information on misalignment in one particular direction. To generate a complete misalignment vector it is necessary to have two verniers measuring in orthogonal directions. Three methods of achieving this are possible. The simplest is to rotate the whole vernier design through 90°, as shown by figure 5.21, so that the Y vernier elements and interface circuitry run in the Y direction. The second method is to have both the X and Y vernier elements running in the X direction, as illustrated by figure 5.22. Here the Y vernier has the vernier elements rotated through 90° while the interface circuitry continues to run in the X direction. The final method is to interdigitate the X and Y verniers into a combined vernier. This is illustrated in figure 5.23 which shows that as with the previous method measurements for the Y direction are obtained with a vernier element rotated through 90°.

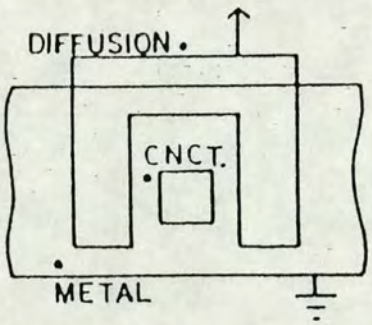


Figure 5.15. Layout for U-shaped vernier element for conductor to contact misalignment measurement. After [11].

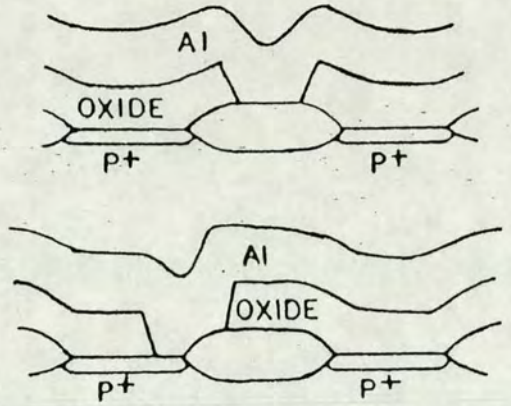


Figure 5.16. Cross sectional views of the switch open (top) and closed (bottom) for the layout of figure 5.15. After [11].

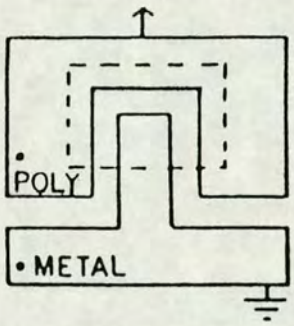


Figure 5.17. Layout for U-shaped vernier element for conductor to conductor misalignment measurement. After [11].

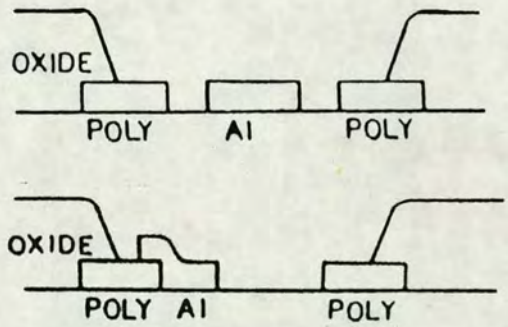


Figure 5.18. Cross sectional views of the switch open (top) and closed (bottom) for the layout of figure 5.17. After [11].

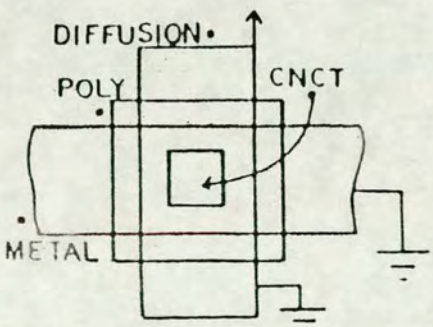


Figure 5.19. Layout for U-shaped vernier element for polysilicon to active area misalignment measurement for a self aligned process. After [11].

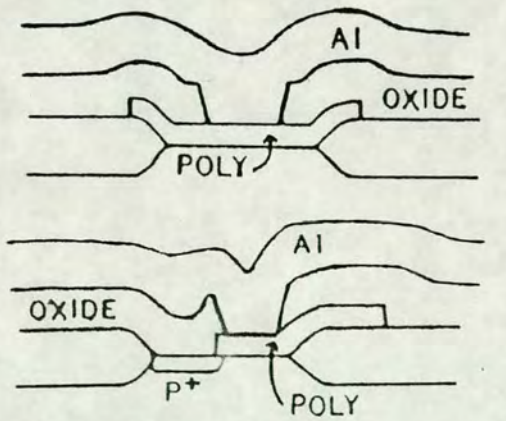
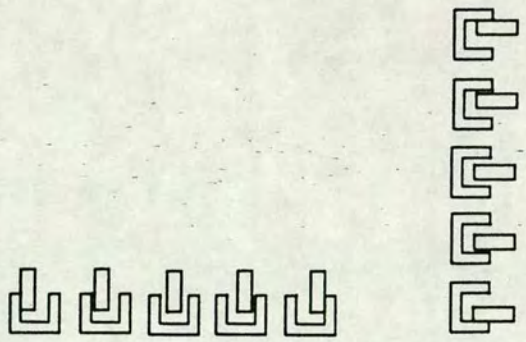
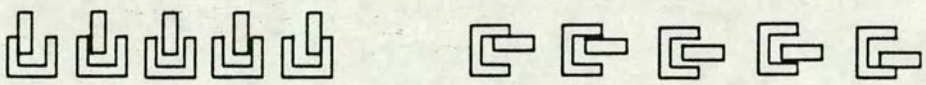


Figure 5.20. Cross sectional views of the switch open (top) and closed (bottom) for the layout of figure 5.19. After [11].



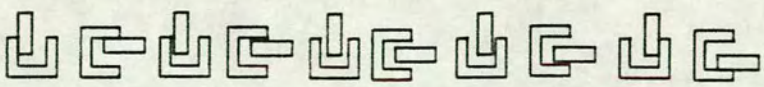
x vernier y vernier

Figure 5.21. Vernier element layout for X and Y measurements. Here the Y elements run in the Y direction.



x vernier y vernier

Figure 5.22. Vernier element layout for X and Y measurements. Here the Y elements run in the X directions.



x and y verniers

Figure 5.23. Vernier element layout for X and Y measurements. X and Y elements are interdigitated.

5.5. Vernier Interface Circuitry

With the large number of vernier elements necessary to make an individual test structure it is clear that some form of circuitry must be employed to reduce the potential number of output pads to a manageable number; certainly to a number comparable with those required for an analogue measurement. This is a problem for any digital test structure and is not unique to the verniers employed here. With a conventional output scheme N vernier teeth would require a minimum of N + 1 pads where each U-tooth was commoned to a single pad and each bar element connected separately. One solution which has been employed to overcome this problem is the use of a shift register. The principle of operation for this is that the output from each vernier element (a digital 1 or 0) is loaded into a shift register stage. The data is then clocked along the line of register stages and the output read at the final stage. This is an example of a parallel load, serial out arrangement for the shift register with one shift register stage for each vernier element. This reduces the pad count considerably as with this scheme only a minimum of six pads need be required. These being V_{dd}, V_{ss}, load enable, data out, Φ_1 and Φ_2: the latter two being the clock signals necessary for correct shift register operation. There are problems associated with using a shift register though. These are that a large area is required for the register, a fully functional process is required to fabricate it and that a suitable shift register must be designed. More importantly testing requires the use of some sort of functional tester capable of clock generation to operate the registers. In this case a hybrid digital parametric tester, which may be as simple as a basic parametric tester with an 'add-on' clock generator, may suffice. The shift register solution, as described in section 5.2, has been adopted as the chosen output method for the digital structures of Henderson *et al.* [5, 11], Walton *et al.* [6] and Yamaguchi *et al.* [7].

Shift register design should not ideally cause a problem as these items are a common element of many functional circuits and may be found in design libraries which enable these to be called up into any new design. Unfortunately in practice test structures are not designed by experienced functional circuit designers but by product, test and process engineers with little or no layout knowledge of functional designs.

5.6. Implementation of Verniers

5.6.1. Aim of Work

The aim of this section of work was to design a test chip based on the vernier concept. Although the vernier concept had originated some time ago no working NMOS vernier circuits had been produced in the EMF. The work here was designed to analyse previous vernier circuits, to evaluate them and then produce a test chip with working vernier circuitry.

5.6.2. Investigation of Previous Work

The initial point for the work for this chapter was to evaluate the design and layout of the digital misalignment circuits which had previously been designed and fabricated on site at the EMF facility. These were the designs by Henderson and Walton [5, 6]. Investigation revealed that both these designs utilised an identical shift register design (from the work of Henderson). Layout was based on a D-type flip-flop design which could be found in a standard text book [12]. This is a semi-static design which is composed of two similar half cells as illustrated by the circuit diagram of figure 5.24. These two half cells are in turn connected by a pass transistor ($M7$) under clock control (Φ_2) while the cell to cell link is via another pass transistor ($M1$) under control of a second clock, (Φ_1). Φ_1 and Φ_2 are two phase non-overlapping clock signals as shown in figure 5.25. The feedback transistors ($M4$ and $M10$) are also under the control of Φ_1 and Φ_2. When Φ_1 comes on the data input from the left is sampled and fed into the first half cell (Φ_2 is off). This input, now double inverted, then appears at the half cell output. Φ_1 is then briefly off before Φ_2 comes on. The feedback transistor for the first half cell is also under Φ_2 control and maintains the input to transistor $M3$ to stop it floating while $M7$ is on and feeding information forward. The output of $M7$ is then double inverted before appearing at the output/next stage. The circuit is essentially static although there is a small period where both Φ_1 and Φ_2 will be off and information must be retained on the input gates. Hence the appellation of semi-static for this circuit.

To allow the data from the vernier to be loaded into the shift register the circuitry shown by figure 5.26 was employed at each vernier element. The vernier tooth itself effectively forms a switch in this circuit which means that if contact was made between the

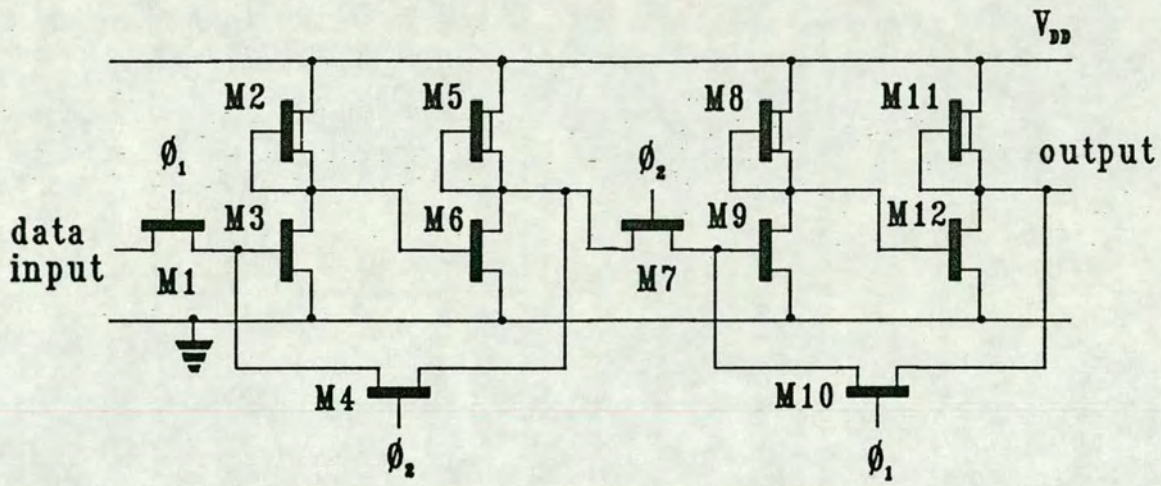


Figure 5.24. D-type flip-flop shift register cell.

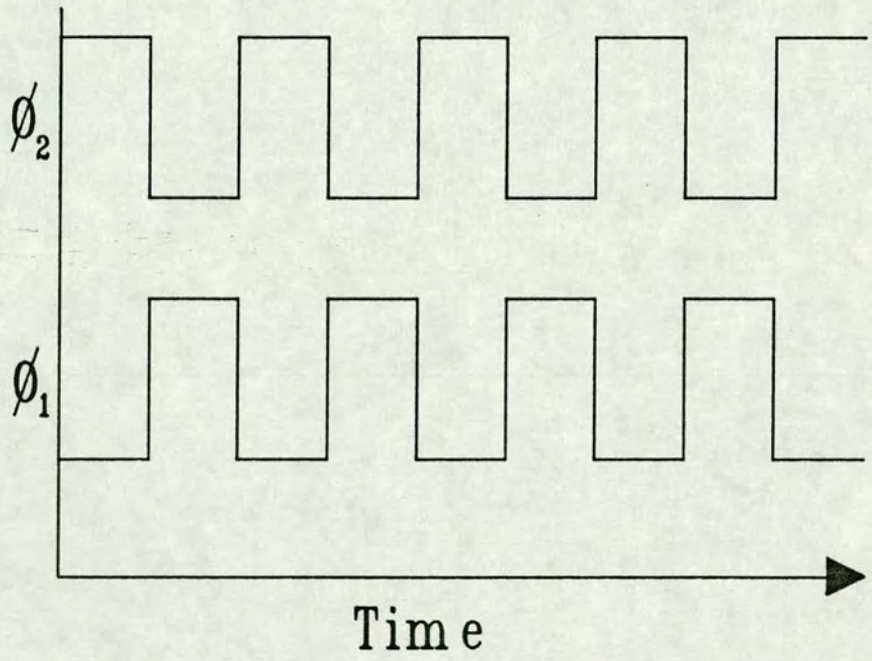


Figure 5.25. Two phase non-overlapping clock.

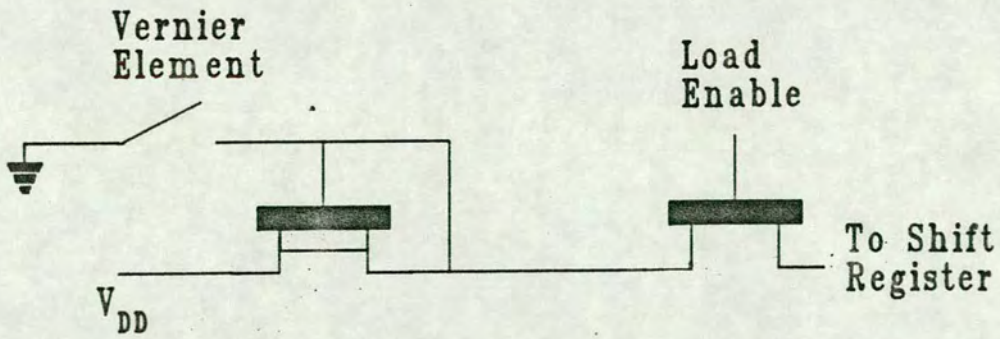


Figure 5.26. Load circuitry to allow vernier element information to be loaded into shift register cell.

tooth and bar a digital zero is loaded into the shift register as the central bar region of the verniers is earthed and pulls the source side of the depletion transistor down to near zero potential. With the bar and tooth not touching the gate of the depletion transistor floats and potential at the source side rises to within a threshold voltage of V_{dd} causing a digital one to be loaded into the shift register. Data is only loaded into the shift register when the load enable line is high, switching on the load enable pass transistors.

As had been stated neither of the previous designs were successfully implemented and no conclusive explanation of this offered [13]. The circuit design used for both these layouts was critically investigated. Investigation of the shift register and its load circuitry revealed two problems, one with the layout of the register and one with the load circuitry.

The layout of the shift register was found to contain an error which involved the feedback transistors ($M4$ and $M10$ of figure 5.24). The result of this error was that instead of the circuit in figure 5.24 being reproduced on silicon, the incorrect circuit of figure 5.27 had been implemented. This has the effect of destroying the feed-forward necessary for the register to work as the inputs to $M4$ and $M10$ will be floating as they have been placed on the output side, rather than the input side, of $M7$ and $M1$ respectively.

The second error was found in the loading of the shift registers from the vernier. One separate bit of information from each vernier element was found to have been loaded into each half-cell (i.e. at the inputs to $M1$ and $M7$), rather than one input to each cell as is required for correct operation (i.e. at the input $M1$). This meant that only half the number of shift register stages that should have been required, were actually present. These two errors were taken to be the cause of the non-operation of these circuits and a redesign of the load circuitry combined with a new layout of the D-type flip-flop cell was undertaken.

5.6.3. Shift Register Layout

The layout employed was the same electrical design as used by Henderson [5,6] (i.e. the static D-type flip-flop) but utilised a completely new layout. Before layout this design was simulated using SPICE on the RAL PRIME computer. As no automatic circuit extraction software was available the data on the circuit interconnect was generated by hand to result in the SPICE file shown in figure 5.28 and several simulations performed.

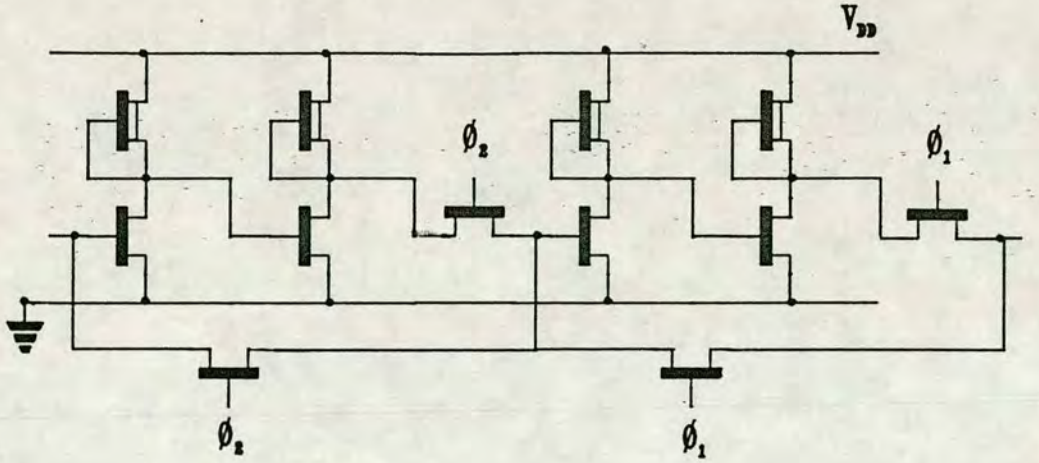


Figure 5.27. Shift register cell implemented in previous non-functioning vernier designs.

```
* CELL1. SIMULATION FOR SINGLE SHIFT REGISTER CELL.
* 1KHZ CLOCKS
VDD 8 0 DC 5V
VBB 10 0 DC -2.5V
VIN 50 0 PULSE 0 5 4.5MS 0MS 0MS
VPH1 11 0 PULSE 0 5 0.5MS 0.1MS 0.1MS 0.3MS 1MS
VPH2 12 0 PULSE 0 5 1MS 0.1MS 0.1MS 0.3MS 1MS
ME0 1 50 0 10 MENH1 L=6U W=12U
ME1 3 2 0 10 MENH1 L=6U W=12U
ME2 4 3 0 10 MENH1 L=6U W=12U
ME3 6 5 0 10 MENH1 L=6U W=12U
ME4 7 6 0 10 MENH1 L=6U W=12U
MD0 8 1 1 10 MDEP1 L=24U W=6U
MD1 8 3 3 10 MDEP1 L=24U W=6U
MD2 8 4 4 10 MDEP1 L=24U W=6U
MD3 8 6 6 10 MDEP1 L=24U W=6U
MD4 8 7 7 10 MDEP1 L=24U W=6U
RLOAD 7 0 100MEG
CLOAD 7 0 0.1PF
R1 1 0 100MEG
C1 10 0.1PF
R3 1 0 100MEG
C3 10 0.1PF
R4 1 0 100MEG
C4 10 0.1PF
R6 1 0 100MEG
C6 10 0.1PF
*******************************************************
.MODEL MENH1 NMOS (LEVEL=1 VTO=1.05 UO=500 GAMMA=0.3 CGSO=4.5E-10
+TOX=8.5E-8 CGDO=4.5E-10 CJ=1.0E-4 CJSW1.0E-9 JS=1.0E-7 LD=1.93E-6
+XQC=0.4 THETA=0.01)
*******************************************************
.MODEL MDEP1 NMOS (LEVEL=1 VTO=-3.8 UO=700 GAMMA=0.7 CGSO=4.5E-10
+TOX=8.5E-8 CGDO=4.5E-10 CJ=1.0E-4 CJSW1.0E-9 JS=1.0E-7 LD=1.93E-6
+XQC=0.4 THETA=0.05)
*******************************************************
.MODEL MENH3 NMOS (LEVEL=3 VTO=1.05 UO=700 GAMMA=0.5 CGSO=4.5E-10
+TOX=8.5E-8 CGDO=4.5E-10 CJ=1.0E-4 CJSW1.0E-9 JS=1.0E-7 LD=1.93E-6
+NFS=2E11 XJ=0.8E-6 VMAX=1.5E5 DELTA=0.1 ETA=0.15 THETA=0.041 KAPPA=0.3
*******************************************************
.MODEL MDEP3 NMOS (LEVEL=3 VTO=-3.8 UO=700 GAMMA=0.7 CGSO=4.5E-10
+TOX=8.5E-8 CGDO=4.5E-10 CJ=1.0E-4 CJSW1.0E-9 JS=1.0E-7 LD=1.93E-6
+NFS=2E11 XJ=0.8E-6 VMAX=1.5E5 DELTA=0.1 ETA=0.15 THETA=0.041 KAPPA=0.3
*******************************************************
.TRAN 0.1MS 10MS
.PRINT TRAN V(1) V(2) V(3) V(4) V(5) V(6) V(7)
.WIDTH OUT=72
.END
```

Figure 5.28. SPICE file for shift register cell analysis.

Firstly simulations on a single cell were performed with the nodes numbered as figure 5.29. Initial simulation were made using 'default' level 1 parameters, but these were followed by simulations made with parameters derived for the EMF process for level 1 and the generally accepted more accurate level 3. Simulations were performed with clocks at $1000Hz$ with up and down ramps of $0.0001s$ to simulate actual drive conditions. Figure 5.30 shows these drive conditions. This frequency was chosen, as most problems were thought would occur when both clocks were off, or partially off, when data would be stored dynamically. A low frequency was thought to be a stiffer test of the circuit in this respect than a higher frequency. Figure 5.31 shows the level 3 simulation for this single cell showing both its input and output. Figure 5.32 shows the output of each of five consecutive stages and indicated that no problems would be present. This latter simulation was performed using level 1 SPICE due to the large consumption of CPU time necessary when the level 3 model is employed with such a large circuit.

The shift register was then laid out using the GAELIC design suite on RAL PRIME-F and the final design of the shift register cell is shown by figure 5.33. The shift register design formed the basis of a test chip using the previously described vernier misalignment structures. This chip enabled misalignment between polysilicon and metal, contact to diffusion and contact to polysilicon to be measured using the appropriate vernier structures. Each vernier structure had 40 elements and the pitch between each one was $0.1\mu m$, giving a range of $\pm 1.9\mu m$ from the central point. To facilitate easier design the vernier elements were grouped in 20 element units which ranged from $0.0\mu m$ to $+1.9\mu m$ misalignment. The full 40 element structure was formed using a mirror image of the 20 element unit to form the complete structure, the mirror image unit giving the $0.0\mu m$ to $-1.9\mu m$ elements of the structure. To allow for process overetch each of the vernier structures was designed with a zero offset which made each element's bar smaller than the U-tooth gap. The polysilicon to metal structure had a $0.6\mu m$ offset while the contact to diffusion and contact to metal structures both had a $1.7\mu m$ offset. Output from each circuit was to a standard 2 × N pad array [14]. Although only six *different* pads were needed (V_{dd}, V_{ss}, Φ_1, Φ_2, load enable and data out) some pads were doubled up to allow easier structure layout. Figure 5.34 shows the pad out allocation for the X vernier structures and figure 5.35 for the Y. The verniers to measure Y misalignment were of the type which had the X vernier and shift register physically rotated 90°, although the pad output was arranged so that a prober scanning in the X direction could probe them (i.e. no wafer rotation was

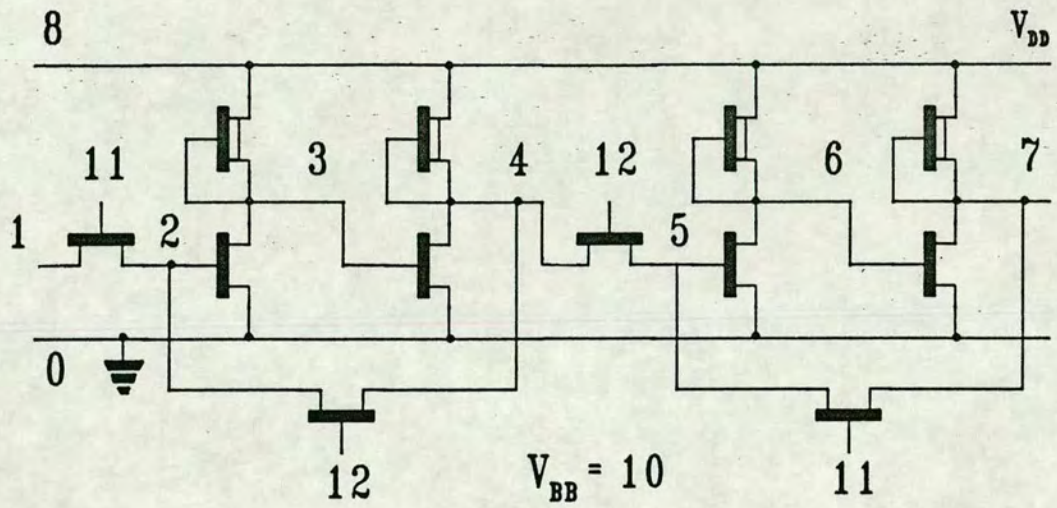


Figure 5.29. Node numbers as used in the SPICE file of figure 5.28.

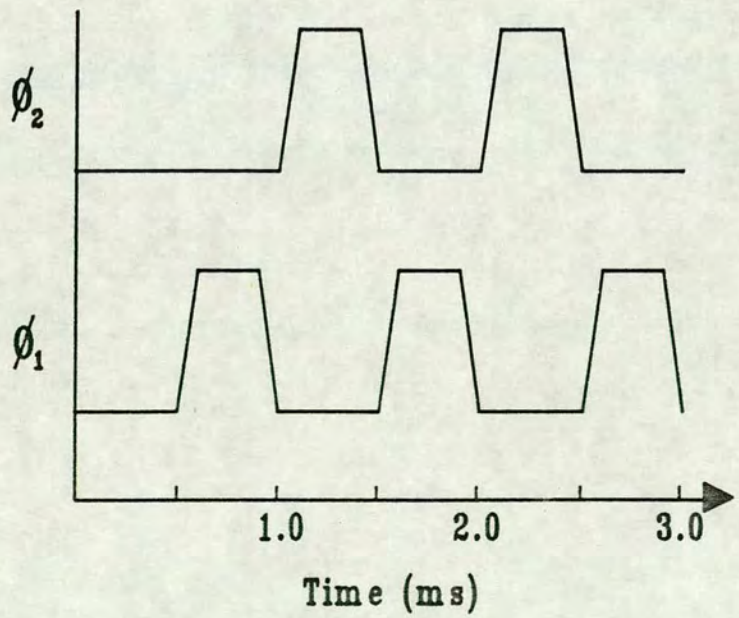


Figure 5.30. Clock drive used for simulation in figure 5.31.

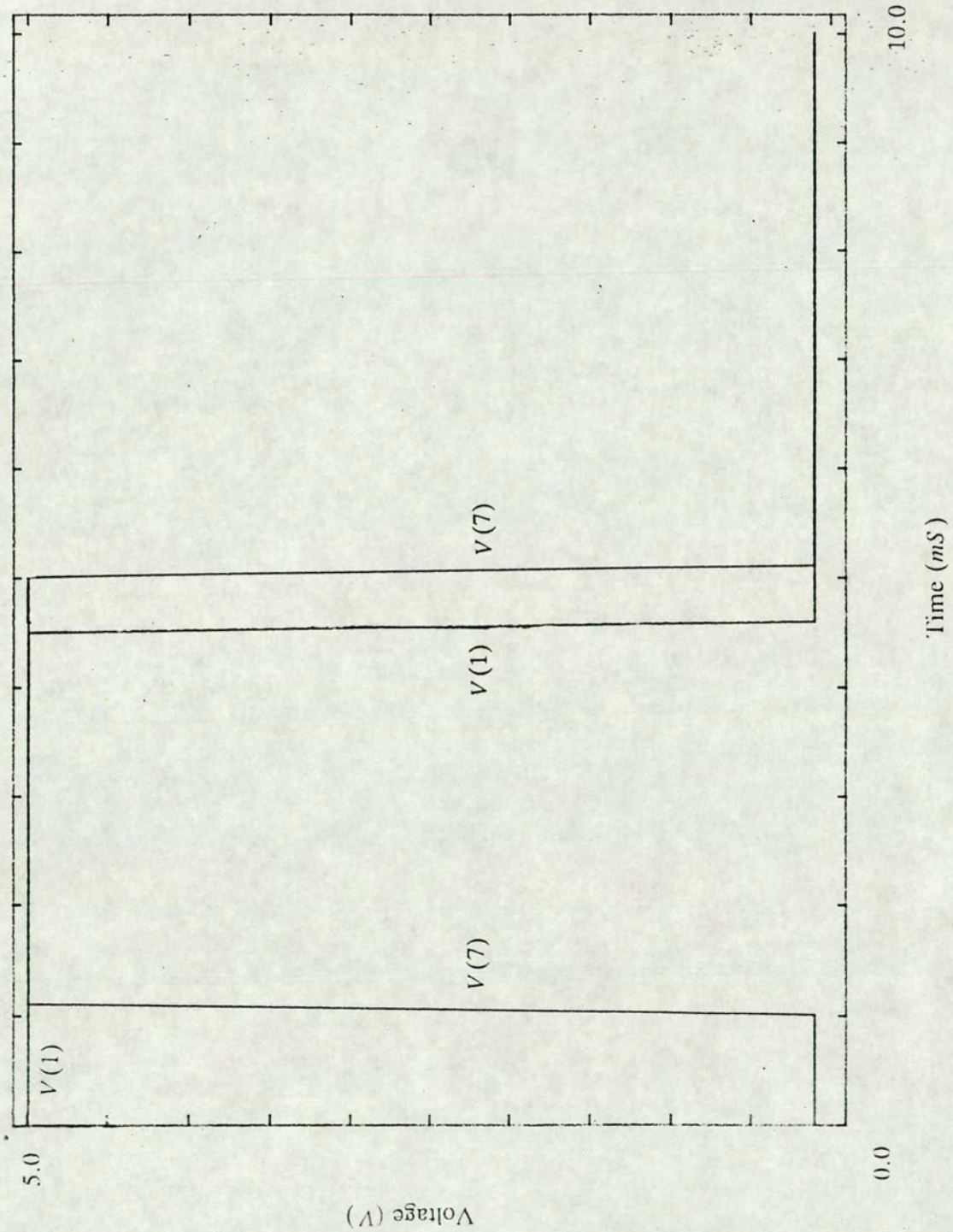


Figure 5.31. Simulation result for shift register cell of figure 5.24. The voltage labels follow the node numbering of figure 5.29.

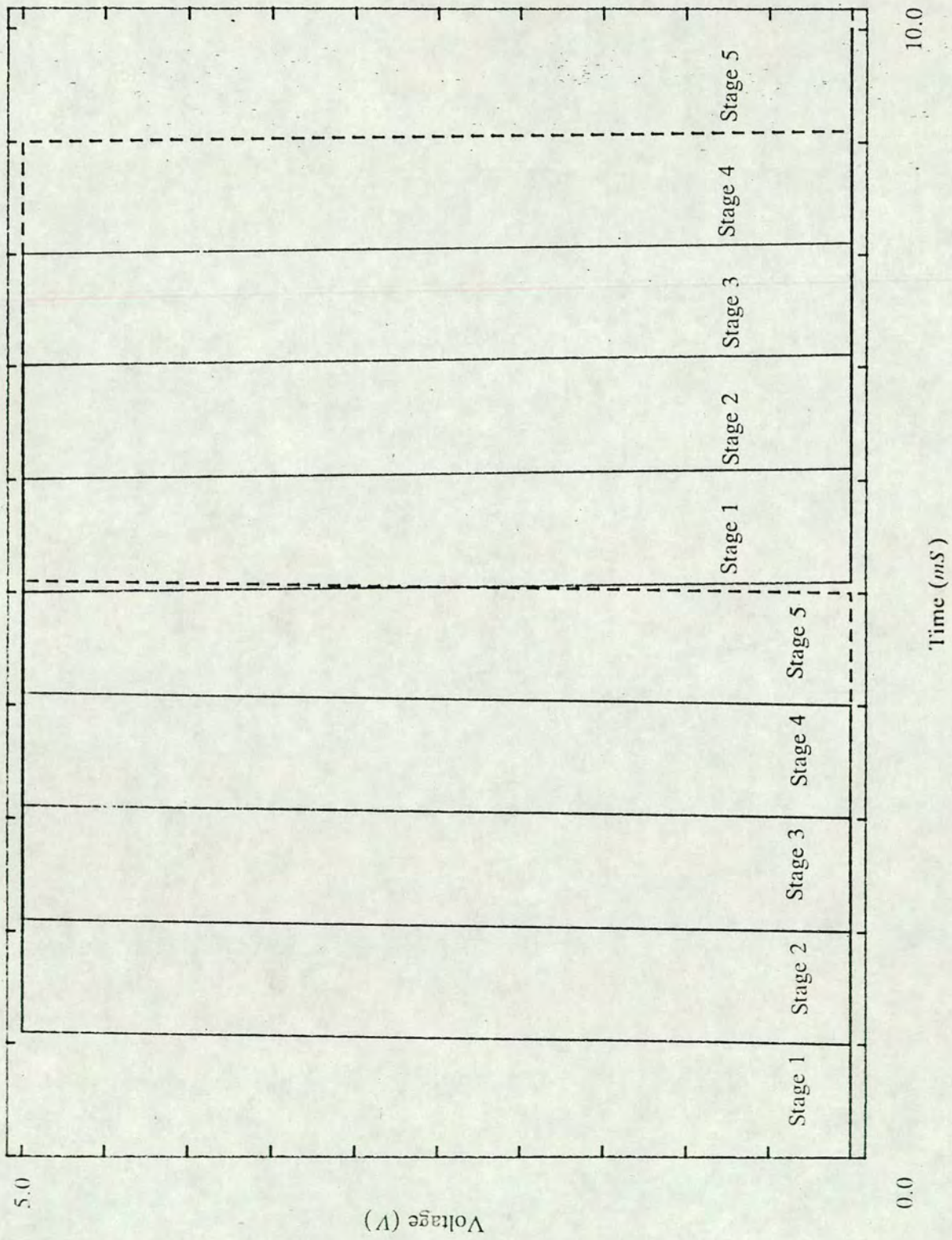


Figure 5.32. Simulation result showing output from five successive shift register cells.

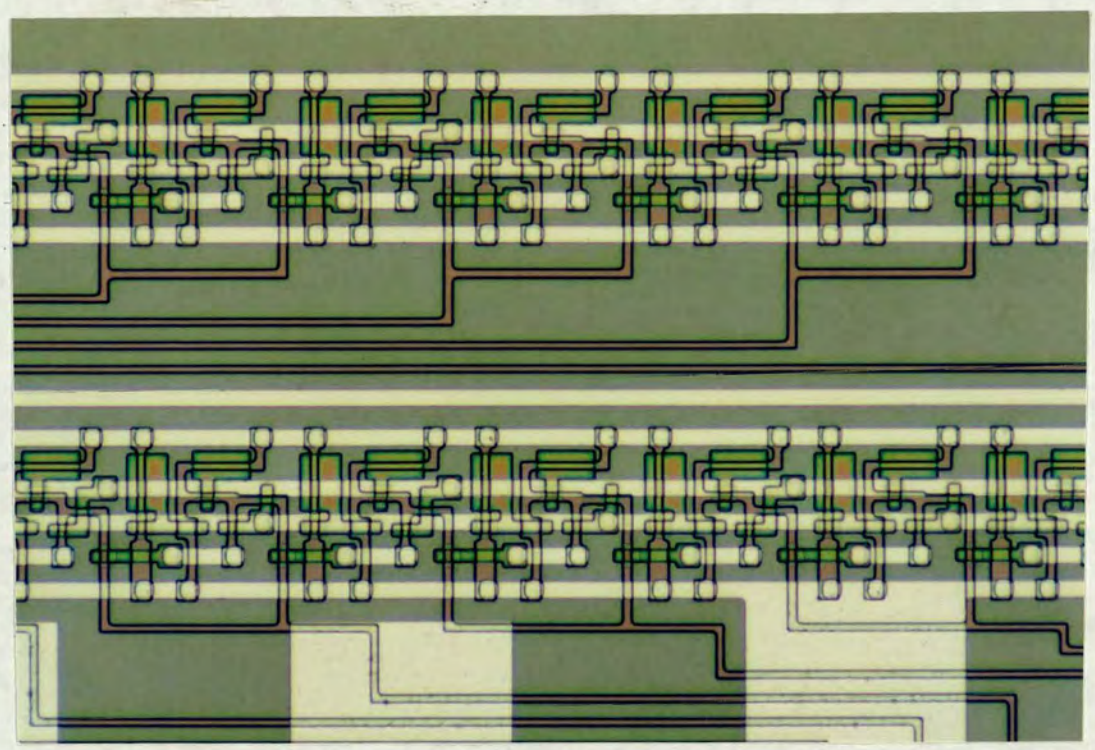


Figure 5.33. Shift register cells of Eμ 651.

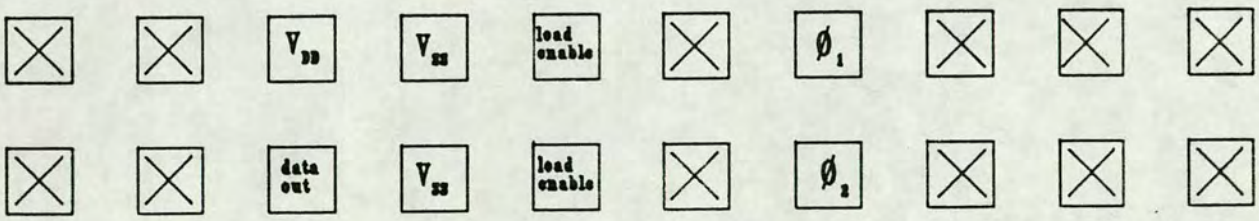


Figure 5.34. Pad out allocation for X verniers of Eμ 651.

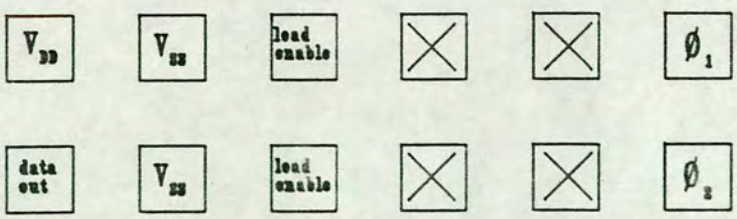


Figure 5.35. Pad out allocation for Y verniers of Eμ 651.

required and thus could be probed in the same pass as the X structures). This required a slightly different pad out allocation for the Y structures which because of chip space restrictions meant that each structure was not in a separate 2×10 array, although could be probed by a 2×10 probe card provided that suitable tester or software provision had been made.

As there were 40 vernier elements in each structure a 40 stage shift register was obviously required to output data from this. As a consequence of the size of the shift register it was necessary to design the register in four 10 stage parts. For a vernier to measure the X misalignment component two of these 10 stage parts were above the vernier containing part of the design and two below. To simplify layout of the data loading to the register, the output from the shift register would not be in a simple sequential order. If the vernier element's output to the top and bottom register cells are labeled as in figure 5.36 then the time order of output will be as shown in figure 5.37. Thus a deconvolution of this data is required after the raw measurements.

Figure 5.38 shows the layout of this chip, ($E\mu$ 651#1), which was fabricated with the standard EMF $6\mu m$ NMOS process.

5.6.4. Problems Encountered with Shift Register Design

Testing the verniers needed the use of test equipment capable of producing a two phase non-overlapping clock. The equipment used to do this was a Tektronix DAS (digital acquisition system). In its basic operation mode this generates a 'window' whose period is variable in which strobe signals can be defined. By defining the delay time and width of the two strobes within this window a two phase non-overlapping clock can be generated. Figure 5.39 illustrates this mode of operation. The DAS repeats this 'window' continuously, thus generating the clock cycles. The delay and width of the pulses and the 'window' duration are variable so that any frequency, within limits, can be chosen. Test circuit output may also be monitored by the DAS, but for initial testing an oscilloscope was sufficient.

When testing the vernier circuits a null output was found. A number of different testing frequencies and clock duty cycles were tried but it was found that the fault was due to an error in the design. Analysis revealed that the load enable circuitry had been designed incorrectly. The load line from each vernier element to each shift register

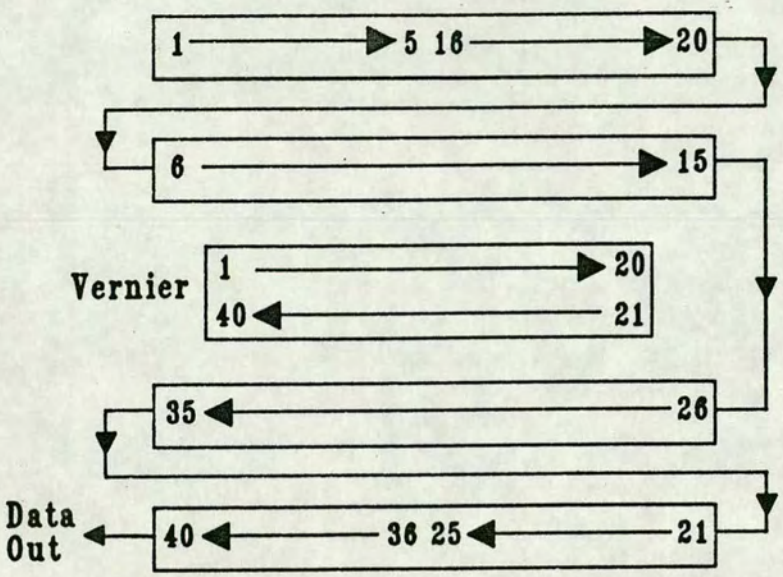


Figure 5.36. Arrangement of vernier element output to shift register cells.

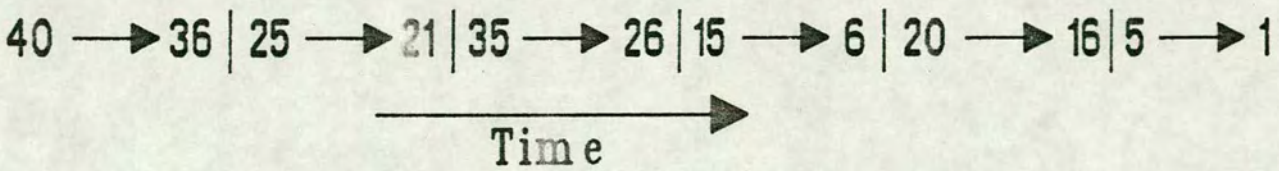


Figure 5.37. Time order output of data from shift register cells.

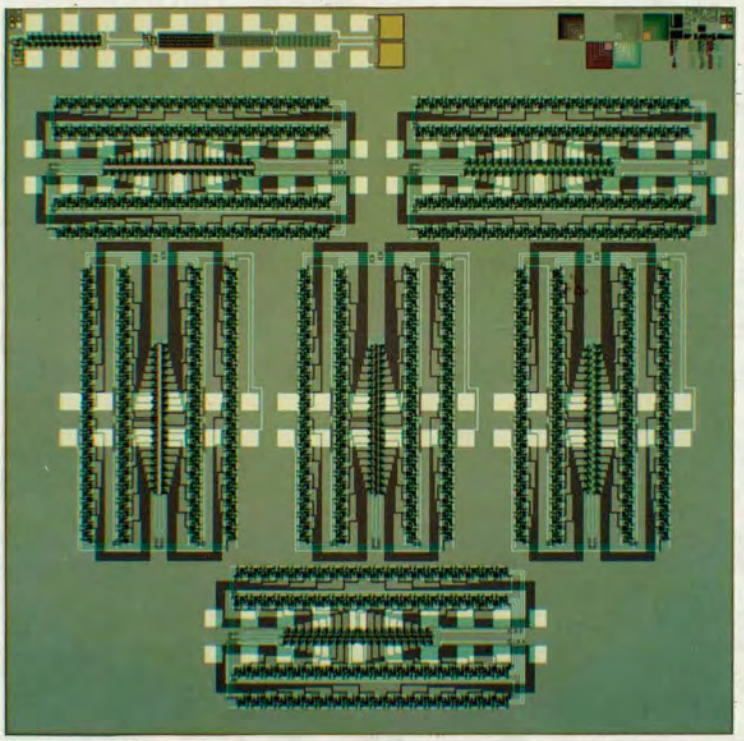


Figure 5.38. Layout of Eμ 651.

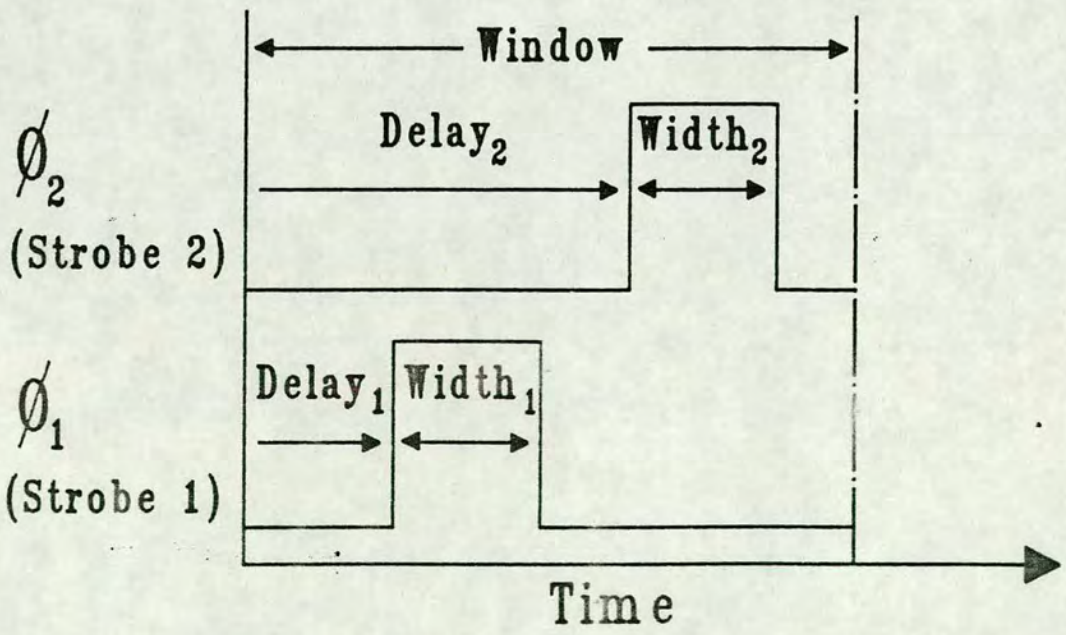


Figure 5.39. Principle of DAS output, used to test verniers.

stage had been designed with the intention that each half-cell would be loaded simultaneously, figure 5.40. Unfortunately it had not been appreciated that although this achieved the correct loading it also meant that once this had been performed the tracks effectively shorted both halves of the shift register cell together, thus rendering the shift register inoperative. This had not been detected at the design stage as the SPICE simulations had not included the load circuitry and cell design together.

5.6.5. Shift Register Re-design

The shift register load circuitry was then redesigned with only a single load line leading to the first half cell, as shown by figure 5.41. To enable both half cells to be loaded with the same piece of information load data is 'clocked' through to the second half cell on a Φ_2 cycle. A timing diagram for the necessary load enable and the clock cycles for this is shown in figure 5.42. This new layout was simply a revised design of $E\,\mu\ 651\#\,1$ with the above fault corrected and was given the number $E\,\mu\ 651\#\,2$.

5.6.6. Failure of Shift Register Re-design

$E\,\mu\ 651\#\,2$ was tested using the same method and apparatus as $\#\,1$ described above. Thorough testing of this design version revealed that this also did not operate correctly and a consistent, low output was obtained. This was irrespective of any manipulation of the clock and load enable cycles with respect to frequency, duty cycle and clock separation. It was clear by optical inspection that at least some of the vernier teeth of the structures tested were making contact and hence should be giving a 'high' output. This indicated a potential problem with the shift register layout. Several methods of analysis were then used to attempt to locate the problem with this circuitry. To evaluate if a static problem was causing this problem a number of devices were packaged to enable voltage contrast work under SEM analysis to be completed. This allowed tracks and inputs to be electrically activated while inside the SEM chamber. As the potential on any electrically activated metal track affects the electrical brightness of that track, as seen by the SEM, the connectivity of any track can be established. This is due to the probing electrons either being attracted or repulsed by circuit tracks leading to dark and light areas respectively which are interpreted as track voltage (high or low) when viewed. Figure 5.43a)-e) illustrates some of the photographs taken. Only DC circuit characteristics were observed but all indicated that no DC problem existed. For more accurate dynamic analysis of the

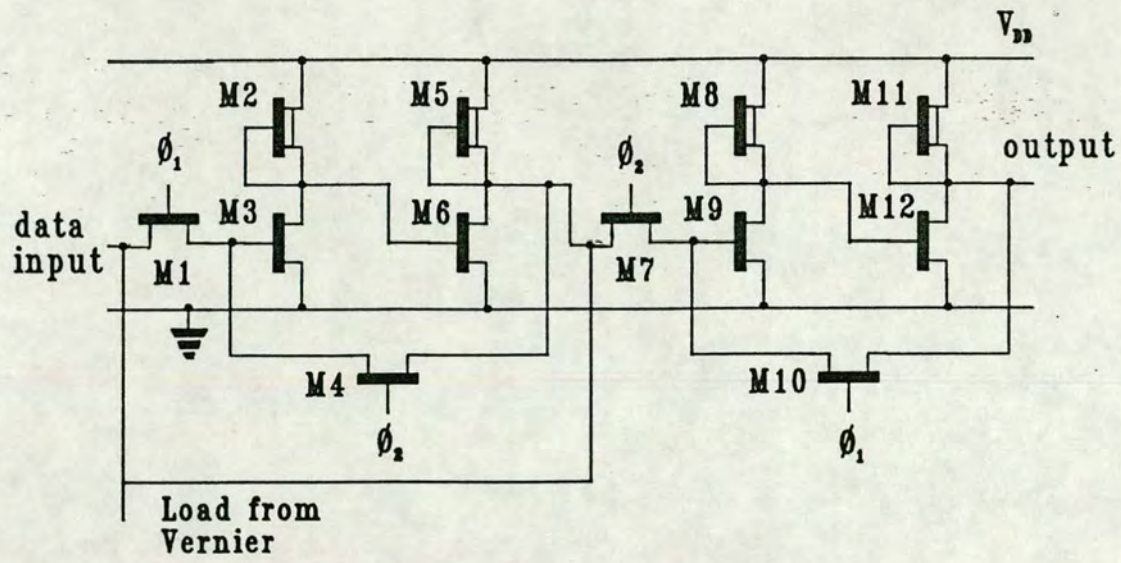


Figure 5.40. Layout of shift register cell showing incorrect load circuitry.

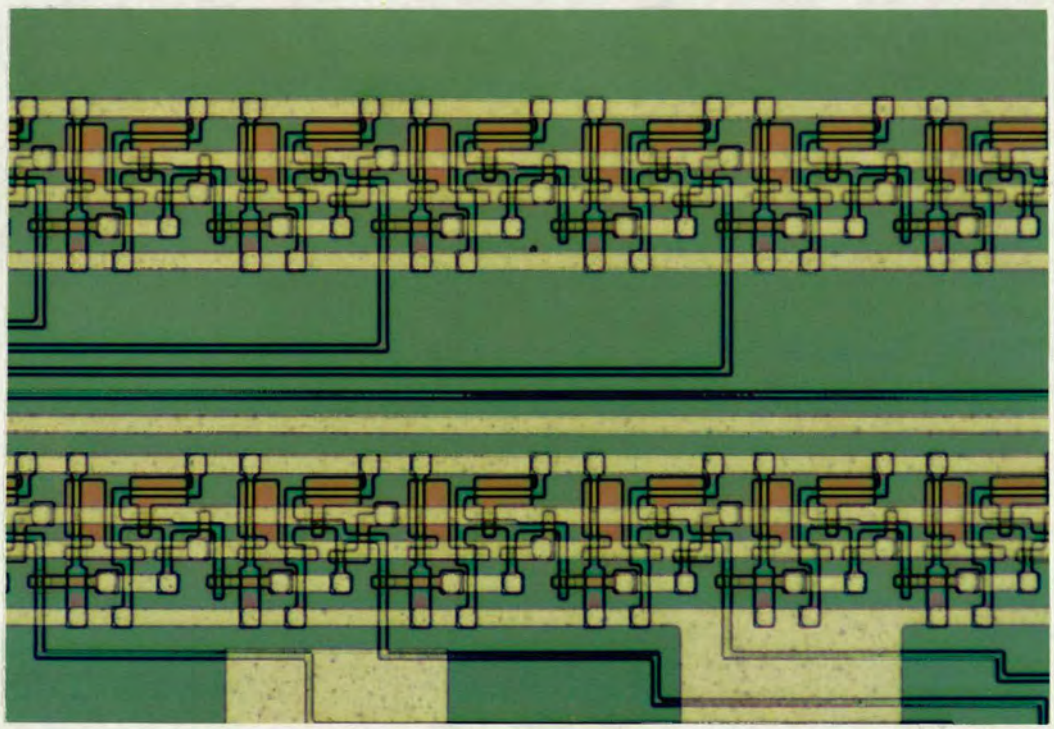


Figure 5.41. Shift register cells, with corrected load circuitry, of Eμ 651#2.

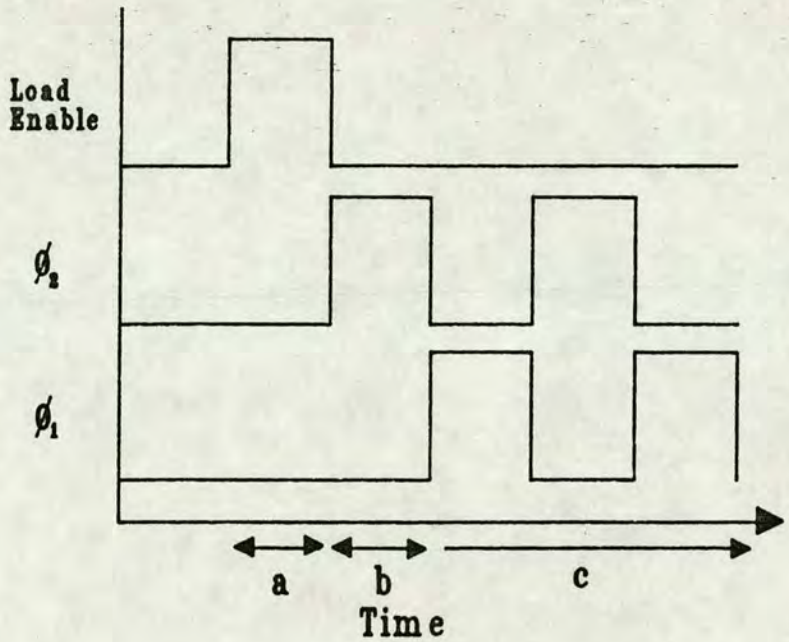


Figure 5.42. Timing diagram for shift register loading. In period 'a' load enable is on and the data is loaded to the first half-cell. In 'b', Φ_2 is on and the data is clocked to the second half of each cell. In period 'c' the data is then clocked from cell to cell.

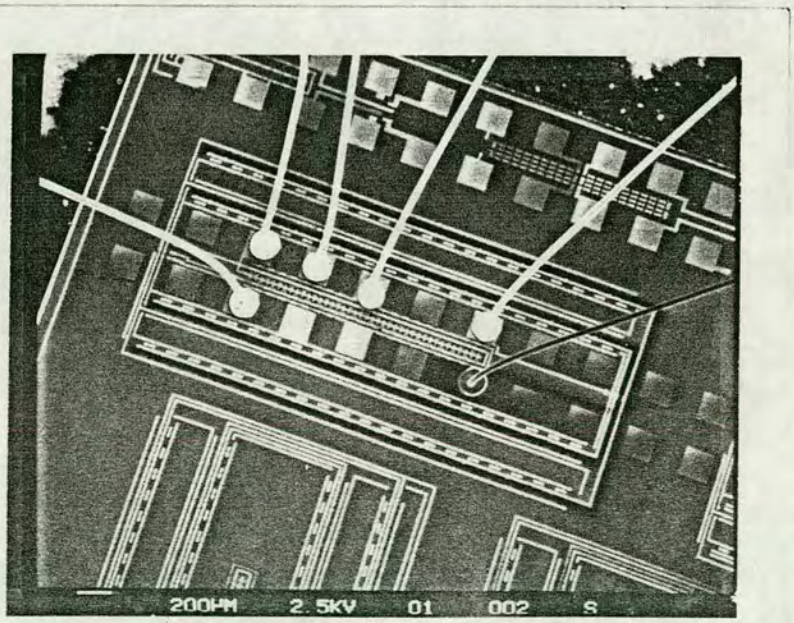


Figure 5.43a) SEM voltage contrast photograph of bonded up Eμ 651#2 device showing Φ_1 as dark areas.

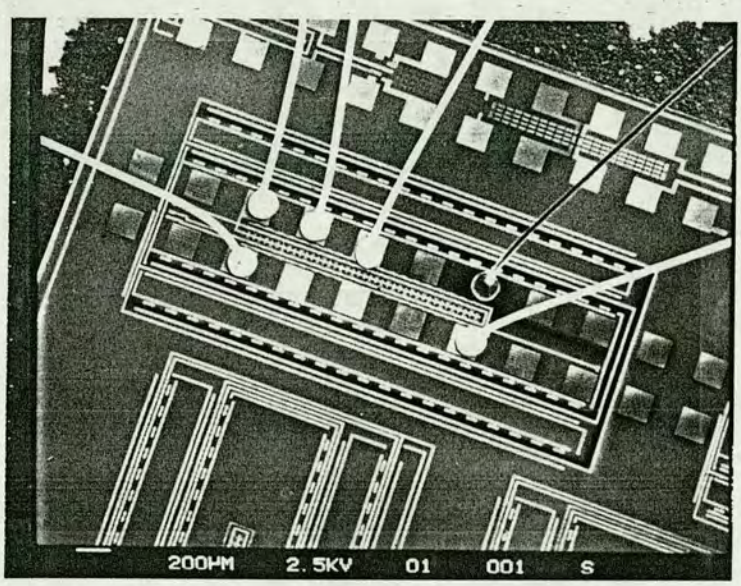


Figure 5.43b) As a) but with Φ_2 shown as dark areas.

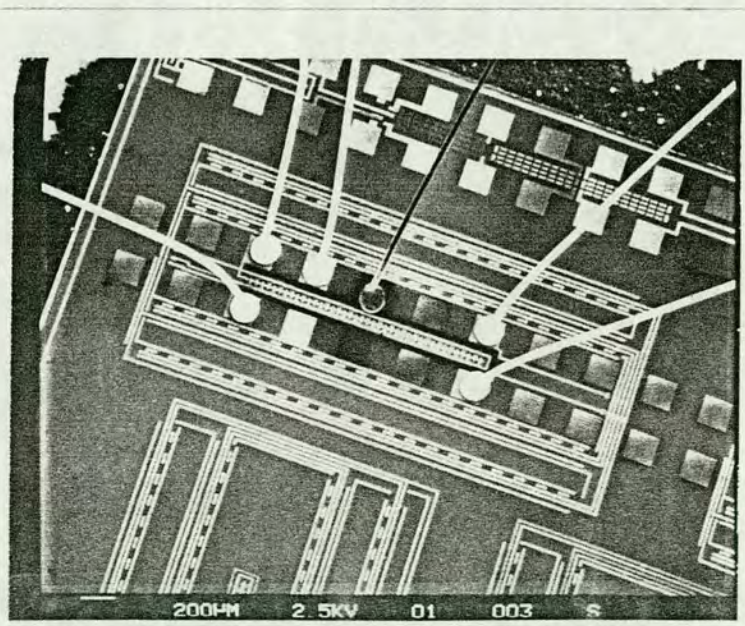


Figure 5.43c) As a) but with load enable shown as dark areas.

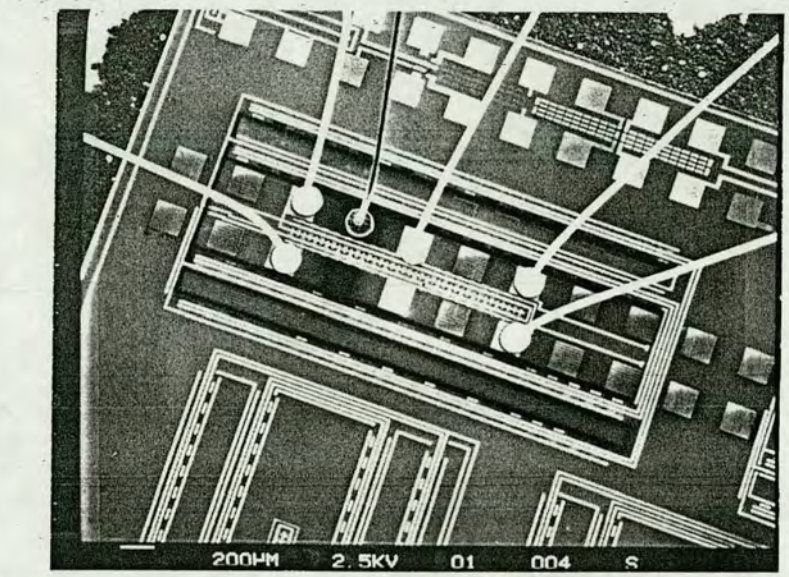


Figure 5.43d) As a) but with V_{ss} shown as dark areas.

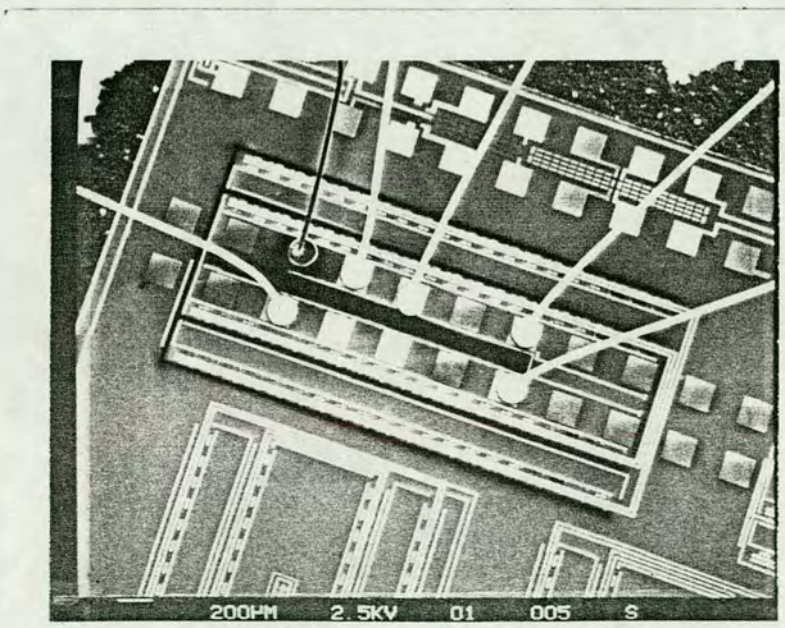


Figure 5.43e) As a) but with V_{dd} shown as dark areas.

shift register circuits it was thought desirable to use a facility which would allow automatic SPICE extraction, including parasitics, from a design. This facility was not available with the GAELIC design suite used so it was necessary to transfer the design to a local VAX which had facilities for this. A program was run to convert the GAELIC design to the CAESAR language used by this VAX. The resultant SPICE files were run with variations in clock frequency ramp and overlap, number of cells and SPICE parameters. None would reproduce the null output that had been found experimentally. Consultations were then made with a functional circuit expert. This led to the proposition that due to the particular layout and capacitances of the circuit, charge sharing was occurring [15]. This is caused by nodes with large capacitances not being fully charged up (to their nominal $5V$) hence information failing to flow along the shift register due to a breakdown of the feed-forward mechanism necessary for operation.

5.6.7. Test Chip Design to Find Working Shift Register

By this stage it was seen that it would be necessary to find a working shift register before utilisation in an application such as vernier output. To this end several shift register designs were evaluated. In particular three shift register layouts which had been developed for the EMF $1.5\mu m$ NMOS process were located. These three shift registers had been shown to work for this process and these consisted of a simple dynamic design, a chain type and a D-type flip-flop [16]. All three designs were taken from a standard text book and indeed the latter being the same circuit design as the failed design used for $E\mu 651\#2$ [12]. Design cells for each of these three designs were converted from CAESAR to GAELIC and were then scaled up to be used for the $6\mu m$ process which was to be used. This involved introducing a scaling factor of four into the language design file of each of the register cells. Parts of the design such as metal 2 layers and test points which were required in their previous application were removed. Metal track widths and spacing were reduced to the minimum design rule levels to enable all the desired structures to be placed in one test chip. This chip design was chosen to have these three scaled designs together with the failed D-type flip-flop, of $E\mu 651\#2$, in a number of configurations which would allow testing of each shift register design in a number of ways. Each shift register was to have three test configurations on the test chip. Simplest was a ten stage register sequence with serial (external) load to the first stage and serial output from the final stage. This would enable testing of the shift registers ability to work without any complicating factors

such as a parallel load interfering. The second circuit for each register was another ten stage design but with each stage capable of being loaded in parallel. The data loading was hardwired (to save pad count) to a repeating 1010... pattern. In addition the register could be serially addressed to its first stage as in the first configuration mentioned. In either case output would be serial from the final stage. This circuit would test each shift registers ability to accept parallel loaded data but without this information coming from a vernier structure. The facility for serial load would allow comparison with the first test circuit configuration. The final structure configuration was a full 40 stage shift register with the input data coming from a 40 element vernier. The vernier design chosen was for polysilicon to contact in the X direction. This vernier had a pitch of $0.1\mu m$, a range of $\pm 1.9\mu m$ and a zero offset of $+1.7\mu m$ (i.e. the central teeth had a $1.7\mu m$ gap between tooth and bar). Summarising, the three test configurations for each vernier were intended to show if each design would,

(1) Work on its own with serial in/out.

(2) Work with parallel in/serial out.

(3) Work with parallel load from vernier/serial out.

The D-type flip-flop of $E\mu$ 651#2 which had been shown to be inoperative with a vernier load was included to see if this design might work in the absence of such a load. These twelve structures (four shift register designs × three test configurations each) were laid out on a test chip, $E\mu$ 812. Figure 5.44 shows the floorplan of this chip and figure 5.45 its layout.

5.6.8. Testing of Shift Register Test Chip

Testing of these circuits was again made using the functional tester used before, the Tectronix DAS. To enable a wider control of the clock frequencies a different test procedure was used which did not make use of the 'window' and 'strobe' features described in a previous section. This involved writing a 'low level' control program which described the length of the load enable, Φ_1 and Φ_2 cycles in terms of multiples of the basic clock frequency. This allowed for easier control of the input waveforms as well as operation at frequencies lower that those possible using the 'window' and 'strobe' facilities. Output was again monitored using a normal oscilloscope. Testing of these circuits revealed that only the dynamic register could be made to work. All the other three designs could not be

Test Strip	
Dynamic Vernier Input	"Old" Vernier Input
Dynamic Serial in/out	Chain Serial in/out
"Old" Serial in/out	D-type flip-flop Serial in/out
Dynamic Parallel in/serial out	Chain Parallel in/serial out
"Old" Parallel in/serial out	D-type flip-flop Parallel in/serial out
Chain Vernier Input	D-type flip-flop Vernier Input

Figure 5.44. Floorplan of shift register test chip Eμ 812. The shift register labelled 'old' is the design used for Eμ 651#2 (figure 5.41).

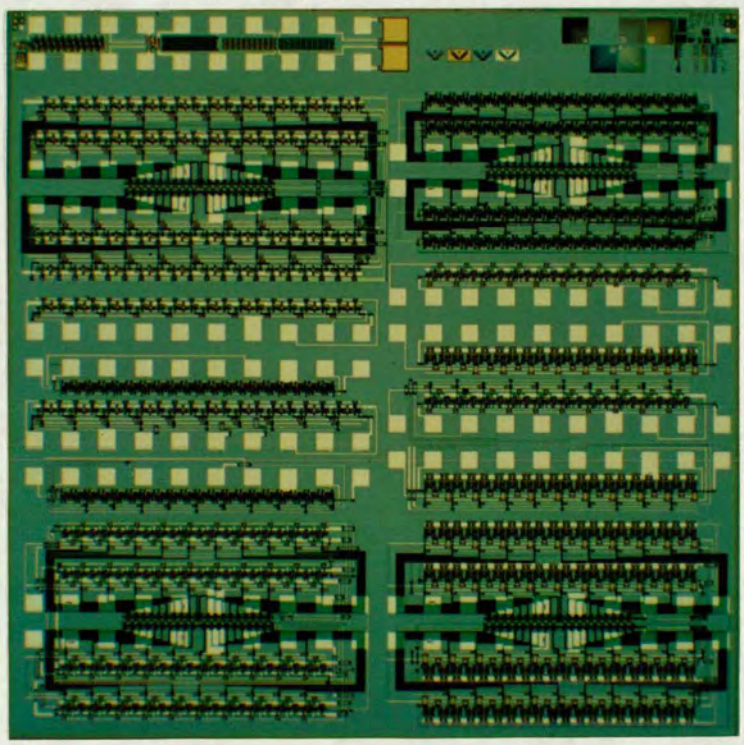


Figure 5.45. Layout of Eμ 812.

made to work even in the simplest serial in/out case. A wide range of operating frequencies, clock underlap and duty cycles were attempted but in no case did any of these three circuits show any 'life'. The dynamic shift register worked up to a maximum clock frequency of around $200kHz$ and for a wide range of clock duty cycles and underlap between phases. It was found to work with both the parallel load and vernier load circuits. This enabled data to be accumulated from the vernier structure present on the test wafer. Using a digital oscilloscope to monitor the register output a whole wafer was analysed for this particular vernier. Readings were taken manually of the extremities of the area of vernier non-contact. As the register is in four, ten stage parts with the loading from each vernier element done in a way to simplify layout considerations, the electrical output from the shift register appears in a convoluted form. Thus the oscilloscope display requires a deconvolution before misalignment data can be interpreted. Figure 5.46 shows a typical oscilloscope output, captured by screen dump, where the data was output in the time order given by figure 5.37 following the vernier element numbering by figure 5.36. Misalignment and relative overetch values for a wafer were obtained and were mapped by hand. Figure 5.47 shows this misalignment map while figure 5.48 the relative overetch information. Yields for the shift register are high and few circuits failed completely, showing that this is a viable technique for use with output of digital parametric test data.

The dynamic shift register design, a cell of which is shown by figure 5.49, was then used to again re-design the original $E\mu 651$ design which was then fabricated as $E\mu 651\#3$.

5.7. An Alternative Multiplexing Scheme: the 'Diode Vernier'

Although the use of shift registers to output data from digital test structures had been demonstrated it requires a fully functional process and the design of a suitable shift register. This is a potentially error-prone process and the shift register itself takes up significant silicon area. This latter aspect is becoming more important due to the increased use of kerf (scribe channel) test vehicles where silicon area is at a premium [17]. Allied to this is the desire to reduce the amount of active circuitry to a minimum, to minimise the number of potential failure sites. To this end a novel multiplexing scheme, applicable for use with vernier or any other digital test structures, was devised. This structure was a development of that proposed by Freeman and Lukaszck [9, 10] but the measurement problems encountered by them were eliminated by using diodes, rather than a measurement

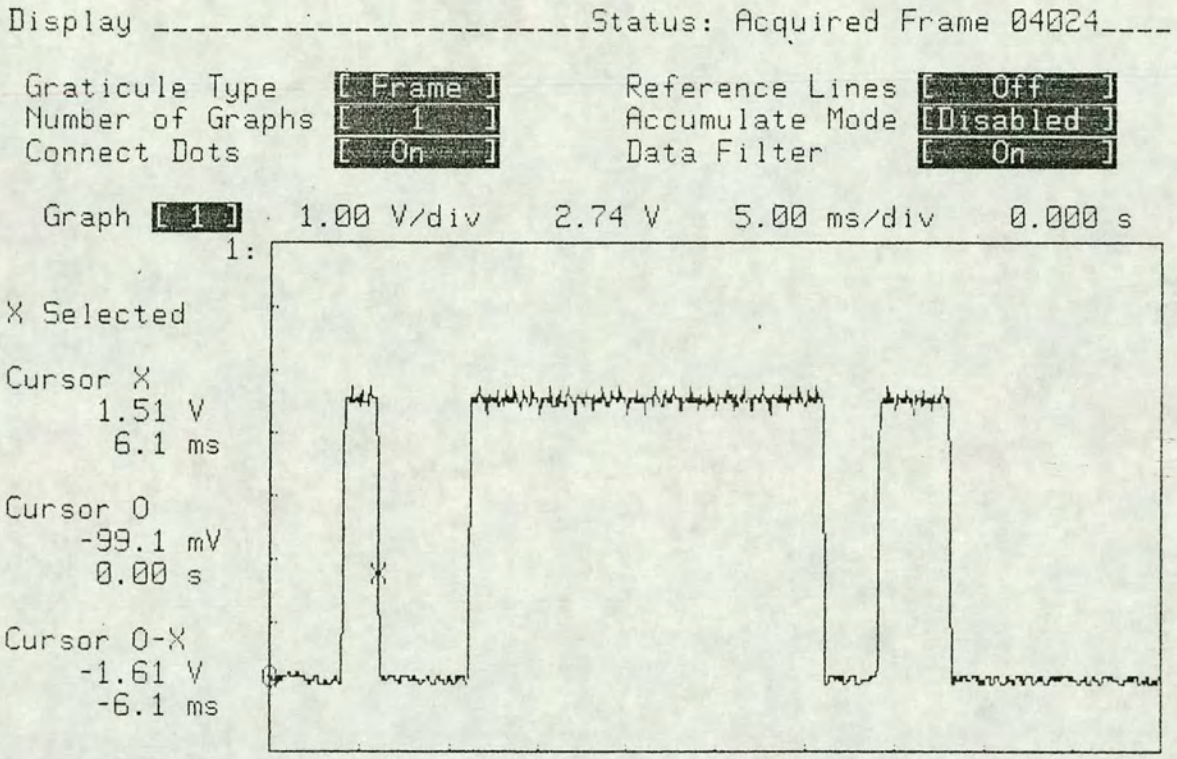


Figure 5.46. Example of digital oscilloscope output used to analyse vernier output.

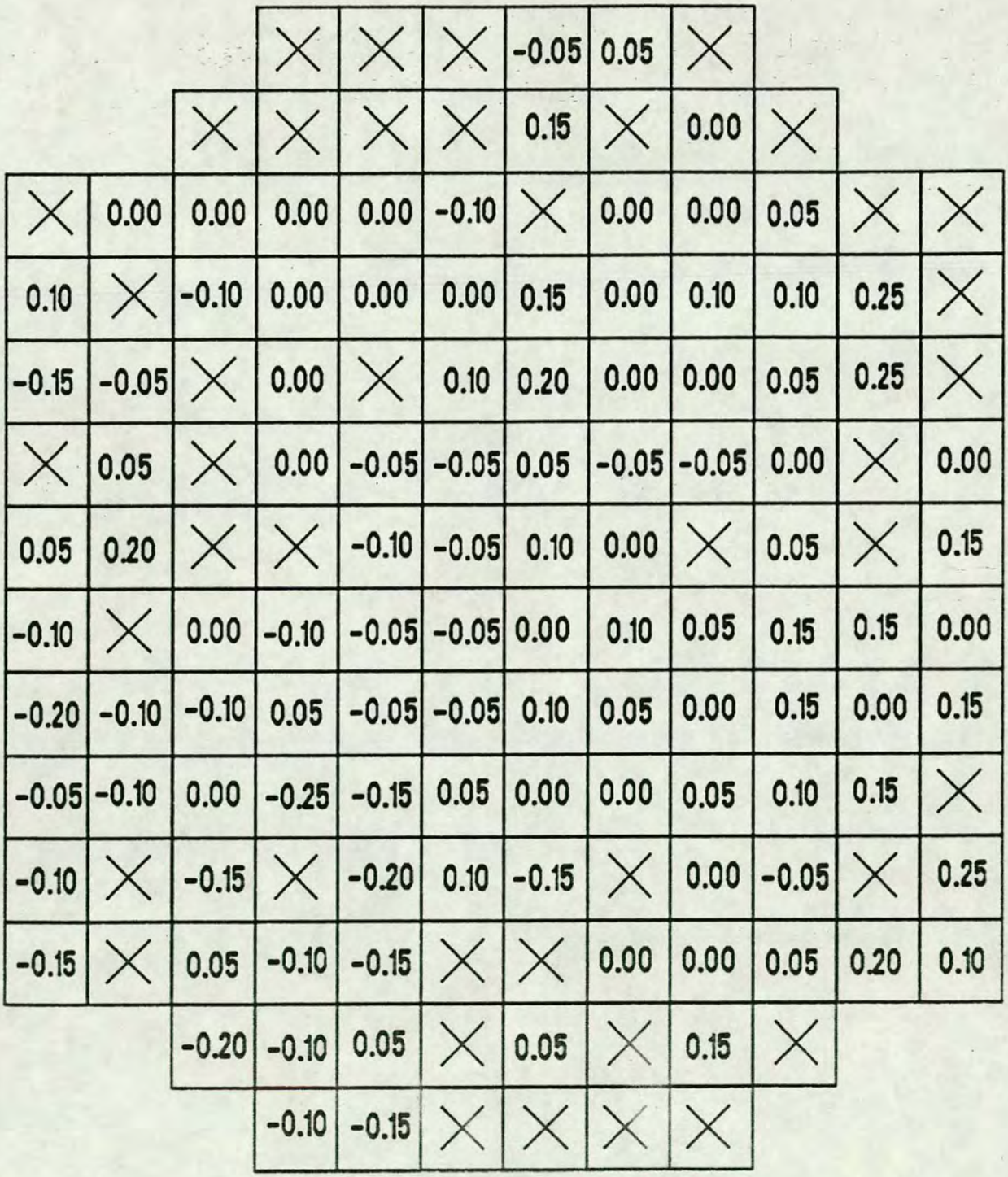


Figure 5.47. Wafer map of misalignment found for X polysilicon-contact misalignment on test chip Eμ 812.

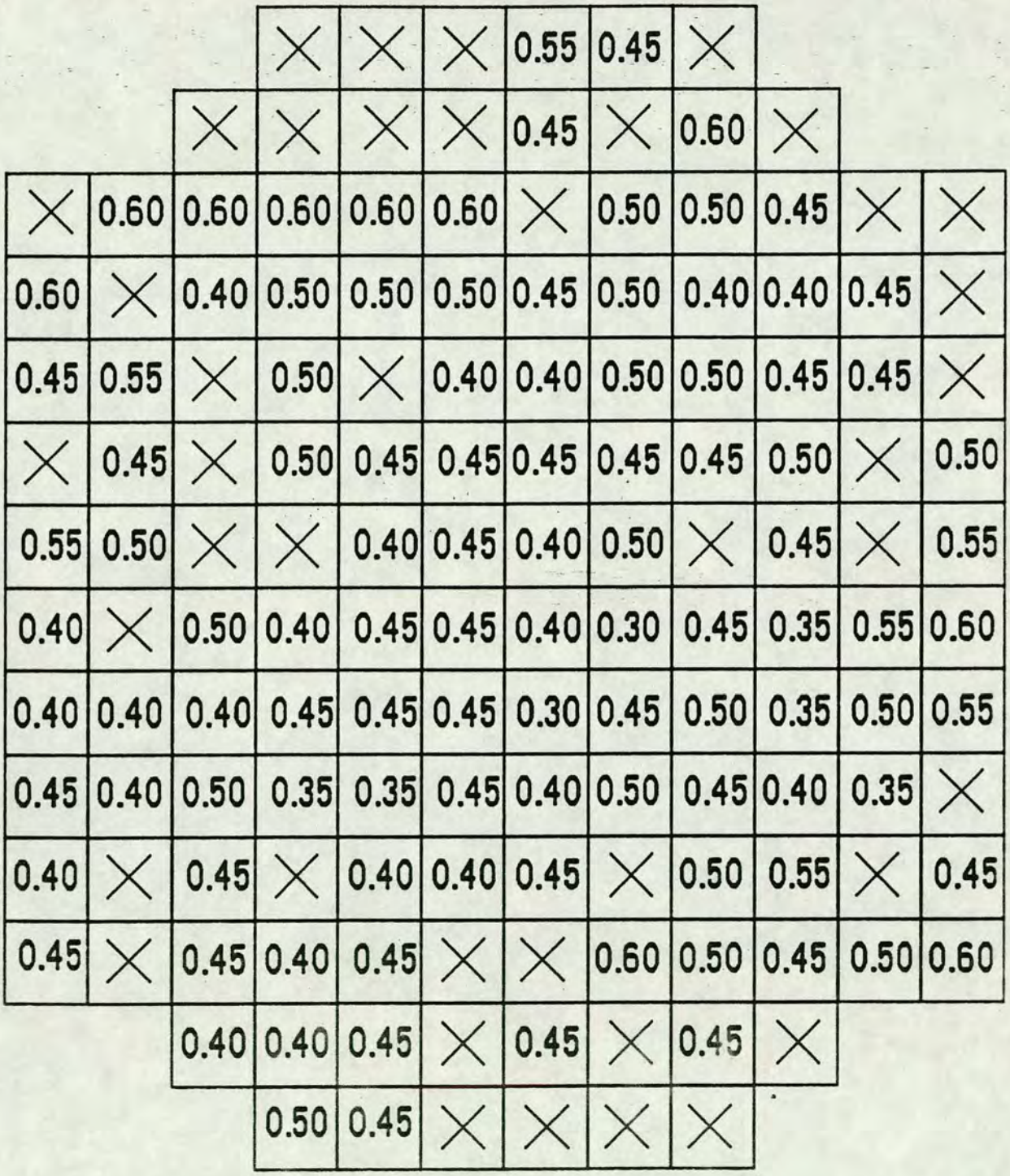


Figure 5.48. Wafer map of relative overetch found for X polysilicon-contact misalignment on test chip Eμ 812.

configuration, to constrain parallel current paths.

To illustrate this scheme a simple electrical layout for a 25 tooth vernier is shown in figure 5.50. Ten pads are required to output the necessary information on whether each element is open or short circuited. Vernier elements are grouped together in fives to make 'group pads', (numbered 6, 7, 8, 9, 10 in figure 5.50) while the first element of each group is accessed by the first access pad, the second and subsequent elements are by the corresponding access pads. To test the first five vernier elements from the left continuity is tested between the first group pad (pad 6) and then the pads 1, 2, 3, 4 and 5 in sequence. To stop alternate current paths affecting the measurement it is necessary to insert a diode in series with each vernier element eliminating all other low resistance return paths. As only diode leakage current provides parasitic paths a very high level of discrimination is possible.

Using this interconnect scheme saves a large amount of silicon area. Although requiring more pads than the previously described shift register structure, the interconnect, operation and layout are simpler while still offering a large saving in required pad numbers over a conventional vernier. The pad requirement for a standard vernier and that of the diode vernier is compared in table 5.1.

No. of Teeth in X and Y Axis Vernier	Number of Pads		Pad-tooth Ratio	
	Standard	Diode	Standard	Diode
36	37	12	1.03	0.333
64	65	16	1.02	0.250
100	101	20	1.01	0.200

Table 5.1. Showing number of pads required and pad-tooth ratio for standard and diode verniers.

It can be seen from the table that as the number of elements in the vernier increases the diode vernier is clearly superior. One considerable advantage of this interconnect scheme for vernier measurement is that a parametric tester is sufficient to make the necessary measurements since no clock generation apparatus or functional test equipment is required. This means the vernier structure is integratable with other test structures and can be tested on the same 'pass' as conventional structures.

This multiplexing scheme (the 'diode vernier') has applications for measurements beyond that of verniers. Indeed any parametric test structure which involves a continuity test can be adapted for use with this circuitry with a resultant large saving in the number of

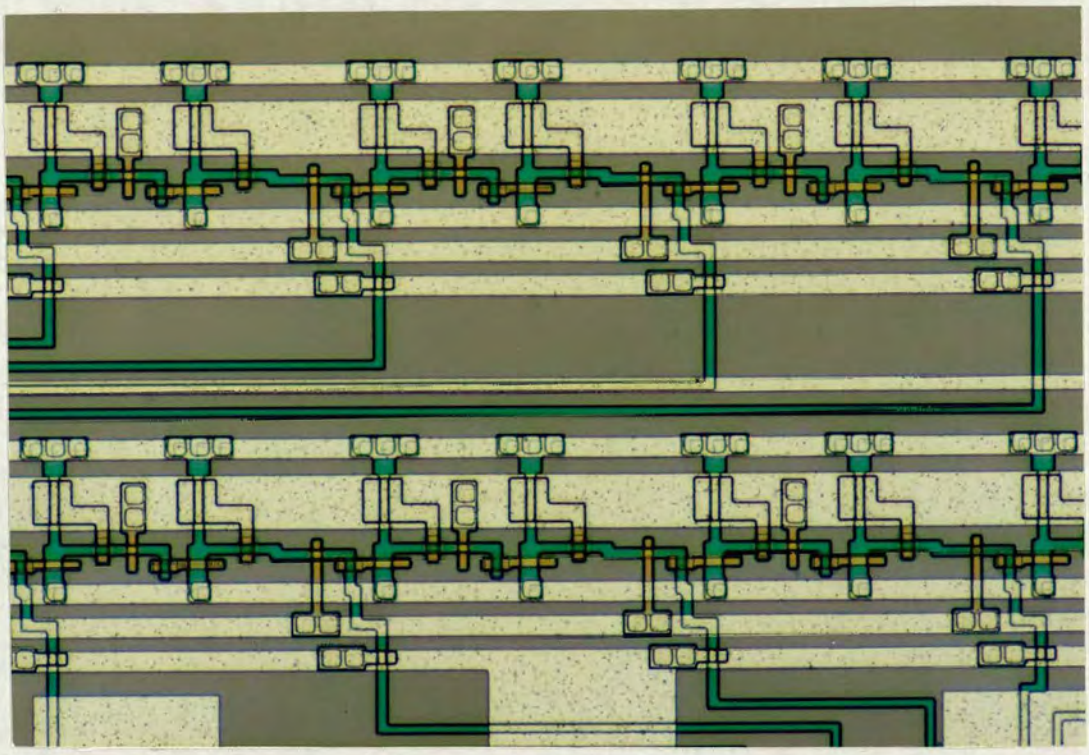


Figure 5.49. Dynamic shift register cells of Eμ 651#3.

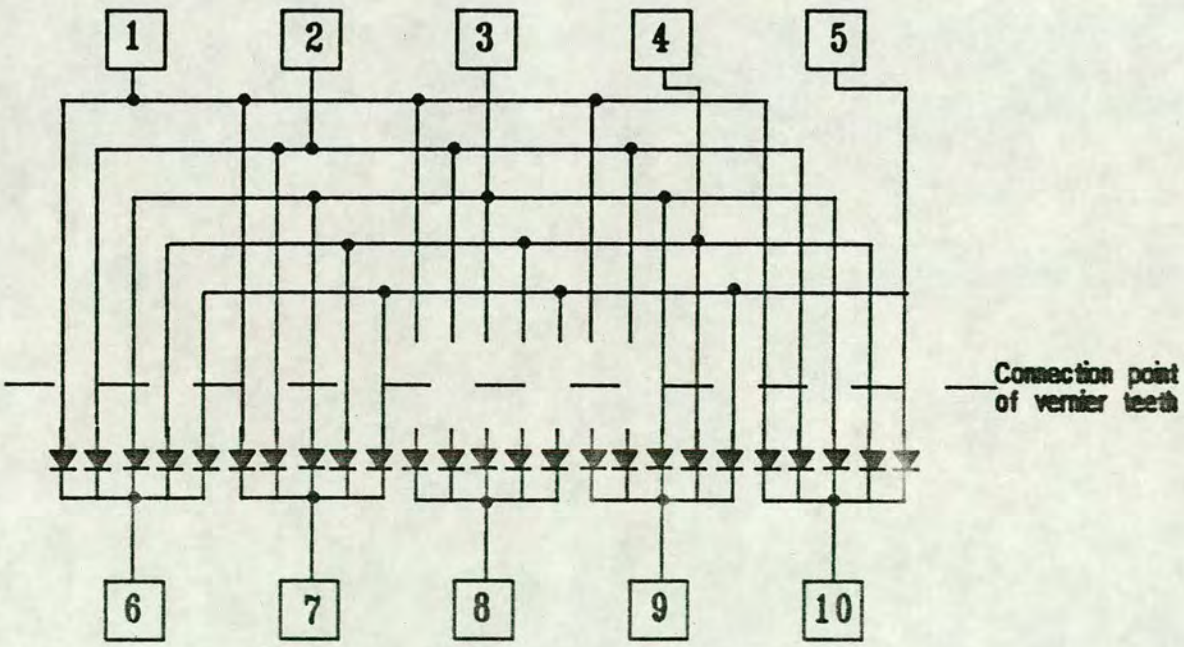


Figure 5.50. Schematic layout of 25 tooth 'diode vernier'.

probe pads needed. An example of such use is contact chains, where taps at various intervals along its length are taken to ascertain number of continuous unbroken contacts [18]. Here each tap to the contact chain would be the analogue of the vernier element. Comb and serpentine resistors which also require checking of continuity are also suited to multiplexed output [19, 20]. Chequerboard structures (by necessity for conducting layers only) which can monitor lithography and etch performance can also be incorporated with this multiplexing scheme [21, 22].

5.8. Conclusions

The results from this chapter have demonstrated the usefulness of the vernier concept for measuring layer to layer misalignment due to its minimum resolution being solely dependent on the process lithography. The U-toothed vernier was used for this purpose and was shown to allow compensation for any relative overetch between the layers structures.

To output data from the digital vernier it is necessary to use some form of output circuitry to reduce the pad count. To this end two possible output schemes for digital structures were used and both shown to be feasible. These methods were the use of a multi-stage dynamic shift register and that of the 'diode vernier' multiplexing configuration. The simple design of the latter scheme is shown to have many advantages over the shift register based design and its application is demonstrated in the next chapter.

References

1. M.G. Buehler, "The Use of Electrical Test Structures Arrays for Integrated Circuit Process Evaluation," *J. Electrochem. Soc.*, vol. 127, no. 10, pp. 2284-2290, October 1980.

2. T.J. Russell, T.F. Leedy, and R.L. Mattis, "A Comparison of Electrical and Visual Alignment Test Structures for Evaluating Photomask Alignment in Integrated Circuit Manufacturing," *IEDM Technical Digest*, pp. 7A-7F.

3. D.S. Perloff, "A Van Der Pauw Resistor Structure for Determining Mask Superposition Errors on Semiconductor Slices," *Solid-State Electronics*, vol. 21, pp. 1013-1018, 1978.

4. D.S. Perloff, "A Four-point Electrical Measurement Technique for Characterizing Mask Superposition Errors on Semiconductor Wafers," *IEEE Journal of Solid-State Circuits*, vol. SC-13, no. 4, pp. 436-444, August 1978.

5. B.M.M. Henderson, A.M. Gundlach, and A.J. Walton, "Integrated-circuit Test Structure Which Uses a Vernier to Electrically Measure Mask Misalignment," *Electronics Letters*, vol. 19, no. 21, pp. 868-869, 13th October 1983.

6. A.J. Walton, W.R. Gammie, R. Holwill, and B.M.M. Henderson, "Digital Measurement of Polysilicon to Diffusion Misalignment for a Silicon Gate MOS Process," *Electronics Letters*, vol. 20, no. 23, pp. 951-952, 8th November 1984.

7. R. Yamaguchi, K. Komatsu, S. Moriya, and K. Harada, "Integrated Electrical Vernier to Measure Registration Accuracy," *IEEE Electron Device Letters*, vol. EDL-7, no. 8, pp. 463-464, August 1986.

8. A. Nishimura, S.S. Mahant Shetti, J. Givens, E. Born, R. Haken, R. Chapman, and P. Chaterjee, "Multiplexed Test Structure ; A Novel VLSI Technology Development Tool," *Proc. of IEEE VLSI Workshop on Test Structures*, pp. 336-355, Long Beach, California, February 17-18, 1986.

9. G. Freeman and W. Lukaszek, "An Electrical Test Structure for Measuring Contact Size," *Proc. of the 1988 International Conference on Microelectronic Test Structures (ICMTS)*, vol. 1, no. 1, pp. 9-14, Long Beach, California, February 1988.

10. G. Freeman, W. Lukaszek, T.W. Ekstedt, and D.W. Peters, "Experimental Verification of a Novel Electrical Test Structure for Measuring Contact Size," *IEEE Trans. on Semiconductor Manufacturing*, vol. 2, no. 1, pp. 9-15, February 1989.

11. B.M.M. Henderson and A.J. Walton, "A Complete Digital Vernier Tool for the Measurement of Mask Misalignment," *Proc. of IEEE VLSI Workshop on Test Structures*, pp. 34-49, Long Beach, California, February 1986.

12. J. Mavor, M.A. Jack, and P.B. Denyer, *Introduction to MOS LSI Design,* Addison-Wesley.

13. W.R. Gammie, Personal Discussions, 1986.

14. M.G. Buehler, "Comprehensive Test Patterns with Modular Test Structures: The 2 by N Probe-pad Array Approach," *Solid State Technology*, pp. 89-94, October 1979.

15. D.R. Renshaw, Personal Discussions, 1988.

16. D. McKnight, Personal Discussions, 1988.

17. C. Alcorn, D. Dworak, N. Haddad, W. Henley, and P. Nixon, "Kerf Test Structure Designs for Process and Device Characterization," *Solid State Technology*, pp. 229-235, May 1985.

18. M.A. Mitchell, "Defect Test Structures for Characterization of VLSI Technologies," *Solid State Technology*, pp. 207-213, May 1985.

19. P. Gill and K. Dillenbeck, "Using Snake Patterns to Monitor Defects and Enhance VLSI Device Yields, Part One," *Microcontamination*, pp. 23-60, February 1989.

20. P. Gill and K. Dillenbeck, "Using Snake Patterns to Monitor Defects and Enhance VLSI Device Yields, Part Two," *Microcontamination*, pp. 33-60, March 1989.

21. R.J. Holwill, J.T.M. Stevenson, A.J. Walton, and J.M. Robertson, "Wafer Scale Etch Assessment Using Single Layer Test Patterns," *Proc. IEEE VLSI Workshop on Test Structures*, pp. 68-76, Long Beach, California, February 1986.

22. I.B. Binnie, R.J. Holwill, J.T.M. Stevenson, J.M. Robertson, and J. Burnie, "Chequerboards: a Novel Technique to Measure Linewidth Uniformity for Process Control," *Proc. 1989 International Conference on VLSI and CAD*, pp. 438-441, Seoul, Korea, October 1989.

Chapter 6

A Complete Digital PCC

6.1. Introduction

The aim of this section of work was to bring together the concept of on-chip switching to access transistors with that of using vernier misalignment structures. These ideas have already been discussed in chapters 4 and 5 respectively of this thesis and this chapter outlines the design of a test chip which utilised both these concepts, to demonstrate that a digital PCC can be used for process evaluation.

6.2. Chip Design

The chip design utilised the standard EMF $6\mu m$ NMOS process and its layout could be considered in two parts. The first contained vernier circuits for misalignment measurement with the second part having both individual and multiplexed access transistors allowing transistor characteristic and SPICE parameter extraction. The design of these parts is now discussed in more detail.

6.2.1. Vernier Design for Eμ 930

The vernier circuits placed on chip $E\mu$ 930 were of the diode vernier type which were described in detail in chapter 5. This format gives a simple and easy way of outputting vernier information using a simple multiplexing scheme. Two sets of diode vernier were placed on this chip, $E\mu$ 930, with each set utilising a different method of access. One set was designed for direct access with each pad connected directly to a group or access line. The second set was designed to be accessed using digitally addressed multiplexers. Each set of verniers consisted of six individual vernier structures which allowed for polysilicon-metal, metal-contact and polysilicon-contact misalignment measurements in both the horizontal and vertical directions. The vertical verniers were of the type with the vernier elements rotated 90° but with the output circuitry still running horizontally. All were designed with 48 elements and a pitch of $0.1\mu m$ between them.

For ease of design two zero misalignment elements were used thus giving a total measurable misalignment window of $4.6\mu m$ for each structure. The verniers for each layer all had a different zero offset to accommodate the anticipated relative overetch and this is summarised by table 6.1.

Vernier Type	Zero Offset (μm)
metal-polysilicon	1.0
metal-contact	0.0
polysilicon-contact	2.1

Table 6.1. The zero offset of verniers in chip design.

For the individual vernier structures fourteen pads were required consisting of seven 'group' and seven 'access' pads. These were placed in a portion of a 2×10 array [1].

The multiplexer accessed verniers were designed in two separate structures, each accessed separately and requiring a 2×10 array to probe. One structure contained three vertical verniers while the second contained the corresponding horizontal verniers. All six of these verniers were designed with an identical pitch, zero offset and number of elements as their individually accessed counterparts.

Each group of three verniers was designed to be accessed by two multiplexers. One multiplexer allowed electrical connection to the group pads of the verniers, the other the access pads. Thus as each individual vernier required seven group and seven access pads each multiplexer had a requirement for 21 switched output lines. The multiplexer takes a digital input which allows one output line to be set 'high'. All other output lines are set 'low' due to at least one pass transistor in each output line being on and thus forming a path to ground (V_{ss}). The single multiplexer line which is on, switches on the pass transistors allowing electrical connection to the relevant test structures for the voltage and current force/measure lines.

The design for this multiplexer falls into three parts; the input circuitry, the decoding matrix and the pass transistor switches. Each of these is now described.

6.2.2. Multiplexer Input Circuitry

The input circuitry was designed so that a single digital input (A) could be taken and produce two outputs, A and its inverse ($\bar{A}$), necessary for multiplexer operation. The circuitry to produce this required two inverters in series and was laid out as depicted in

figure 6.1. $\bar{A}$ is produced from the output of the first inverter and is used to drive the input of the second inverter which produces A. Both inverters had enhancement transistors of 2:1 aspect ratio and depletion transistors of 1:4. A total of six input inverters circuits were used.

6.2.3. Decoder

The decoding matrix was designed with ten functional input lines and an eleventh which acted as a load enable. Figure 6.2 shows this layout. Each input line was designed to run the length of the matrix in a polysilicon line. These polysilicon lines formed the gates of minimum geometry pass transistors which were designed so that the sources of these pass transistors were connected directly to ground while the drains were connected to a matrix output line. Consequently if a polysilicon line was 'high' this pass transistor would be 'on' and the output line pulled low. The pass transistors were positioned in the matrix such that each output line being 'high' corresponded with a unique input. The inputs $00000_2 \rightarrow 10100_2$ were designed to correspond to the setting of lines $1 \rightarrow 21$ high in turn, where the output lines are numbered from the matrix's input end.

6.2.4. Switching Circuitry

To interface the test structures to the decoding matrix, each matrix output line required some switching circuitry. The switches allow electrical testing of the chosen test structure (here a vernier element) via the force/sense lines. The output line from the matrix forms the gates of the two pass transistors which control access to the force/sense lines. One pass transistor was designed with an aspect ratio of 4:1 so that this would be best suited to current forcing/sensing while the second had a 2:1 ratio which was intended for voltage forcing/sensing. The use of separate forcing and sensing lines allowed fully Kelvin measurements to be made, if required, although it was realised that for this application it would not be necessary as only continuity would be required to be measured.

6.2.5. Pad Allocation

Two complete multiplexers were used per structure and this necessitated a full 2×10 pad array for output. The pad allocation for this structure is given by figure 6.3.

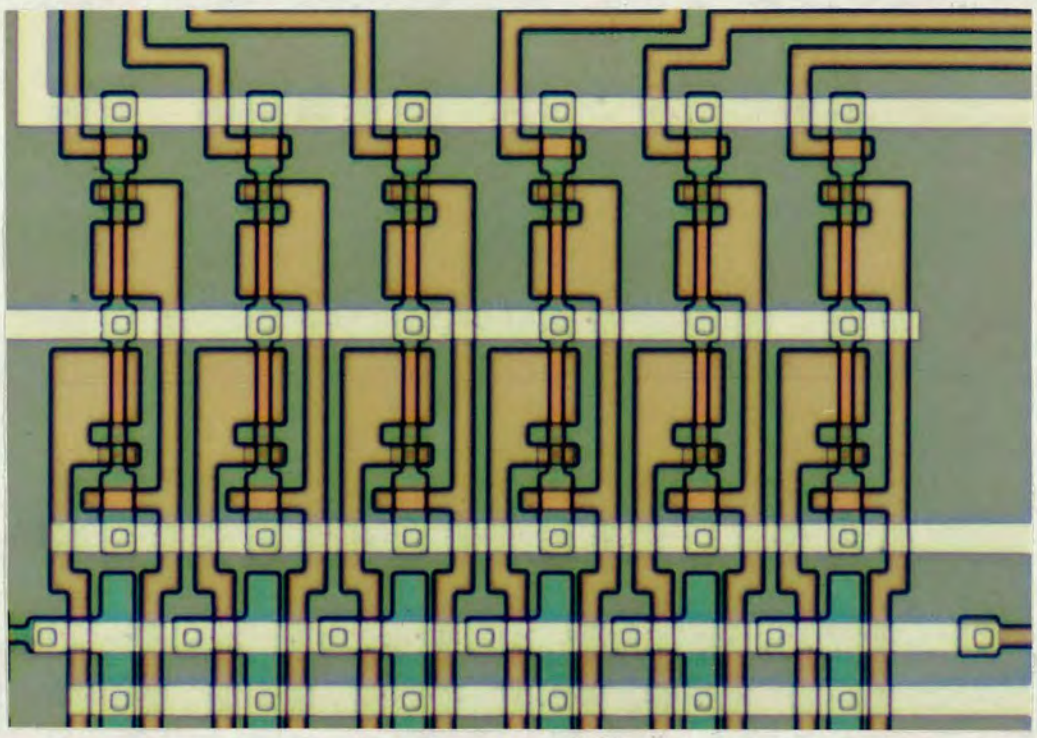


Figure 6.1. Multiplexer input circuitry.

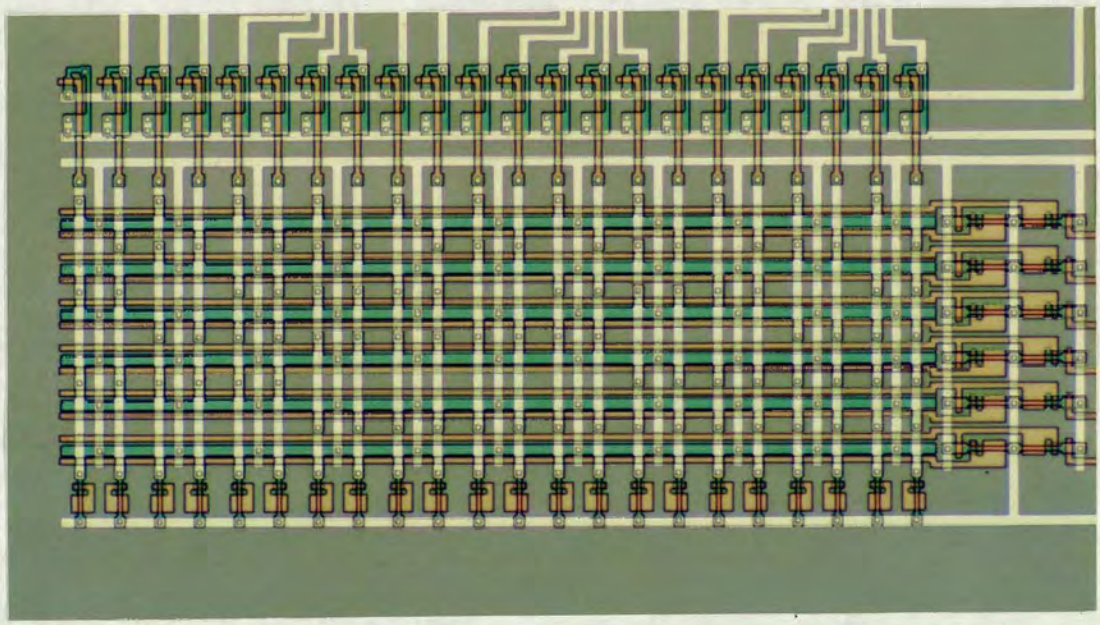


Figure 6.2. Multiplexer decoder layout showing switching circuitry (top) and input circuitry (right).

6.2.6. Transistor Arrays

The array of transistors was made up of an array of eight test transistors with the dimensions given by table 6.2.

Dimensions of Transistors in Matrix (μm)			
6 × 6	12 × 6	48 × 6	96 × 6
24 × 24	60 × 60	6 × 12	6 × 96

Table 6.2. The dimensions of eight transistors in matrix.

These were chosen to give a wide spread of aspect ratios necessary for device characteristic and SPICE parameter extraction. The matrix allowed each of the test transistors sources to be accessed via an output line from the multiplexer unit. The drains of all the test transistors were commoned to a single pad while each row of the transistor array was accessed via a separate gate pad. The multiplexer design for the transistor array was similar in principle to that for the verniers. One important difference though was that separately controllable gates were used for the switch circuitry which allowed different gate voltages to be applied to the current and voltage pass transistors. This consequently meant a doubling of the circuitry required in the decoder matrix, as identical pass transistors were required for the current and voltage output lines of each matrix section. The switches themselves were designed with a 4:1 aspect ratio transistor for the voltage pass transistor and a 14:1 ratio for the current one. A 2 × 10 array was used to output data from the complete structure although not all the pads were required. Figure 6.4 illustrates this pad out configuration with figure 6.5 the whole transistor array. Individual transistors with the same aspect ratios as those in the array were also placed on the test chip. These would allow comparison of transistor characteristics and SPICE parameters between devices accessed individually and those measured via the matrix. The individual transistors had separate gate, source and drain pads and were placed where unused pads of 2 × 10 array blocks occurred in the diode vernier section of the chip.

6.3. Chip Fabrication

The floorplan of the complete chip, $E\mu 930$, is shown by figure 6.6 and its layout by figure 6.7. This design was fabricated using a reticle which was shared with another user's design. Thus only half the chips on the completed wafers were of this design. The

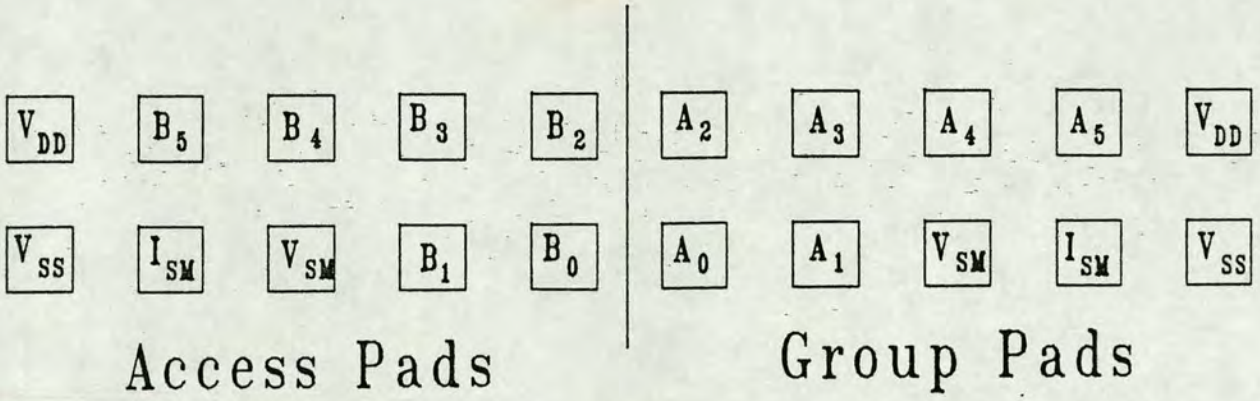


Figure 6.3. Multiplexer pad out allocation. 'A' and 'B' are the digital multiplexer inputs, I_{SM} and V_{SM} are the current and voltage force/sense lines respectively.

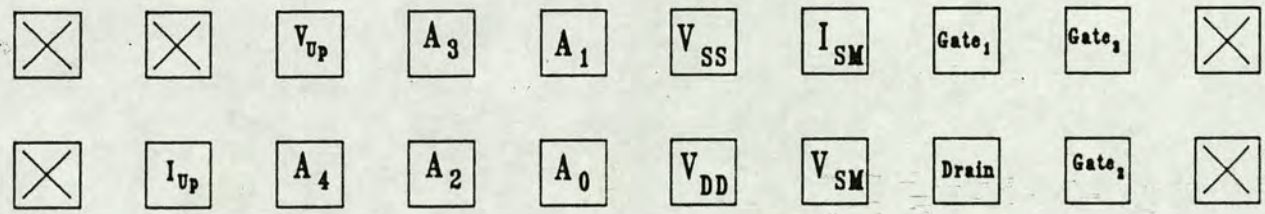


Figure 6.4. Transistor array pad out allocation. 'A' is the digital multiplexer input, V_{up} and I_{up} are the pass transistor control voltages for the voltage and current force/sense lines respectively.

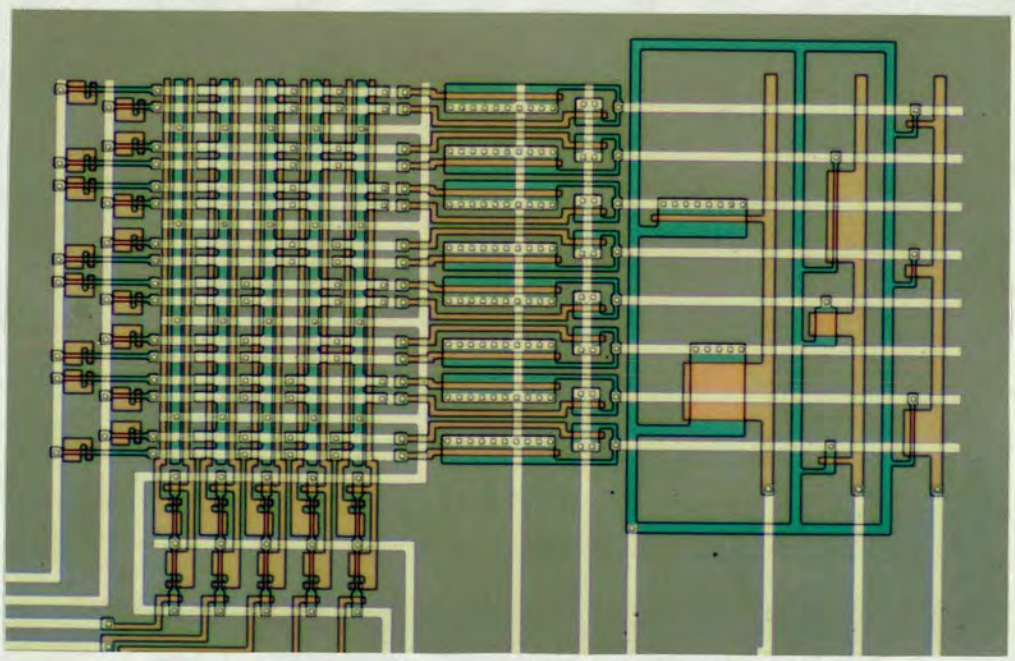


Figure 6.5. Layout of transistor array and multiplexer circuitry.

<table>
<tr><td colspan="4">Test Strip</td></tr>
<tr><td>Metal-Poly.(x)</td><td>X</td><td>Metal-Poly.(y)</td><td>Individual Transistors</td></tr>
<tr><td>Poly.-Contact(x)</td><td>X</td><td>Poly.-Contact(y)</td><td>Individual Transistors</td></tr>
<tr><td>Metal-Contact(x)</td><td>Individual Transistors</td><td>Metal-Contact(y)</td><td>Individual Transistors</td></tr>
<tr><td colspan="2">Multiplexed Verniers(y)</td><td>Multiplexed Verniers(x)</td><td>Transistor Matrix</td></tr>
</table>

Figure 6.6. Floorplan of Eμ 930.

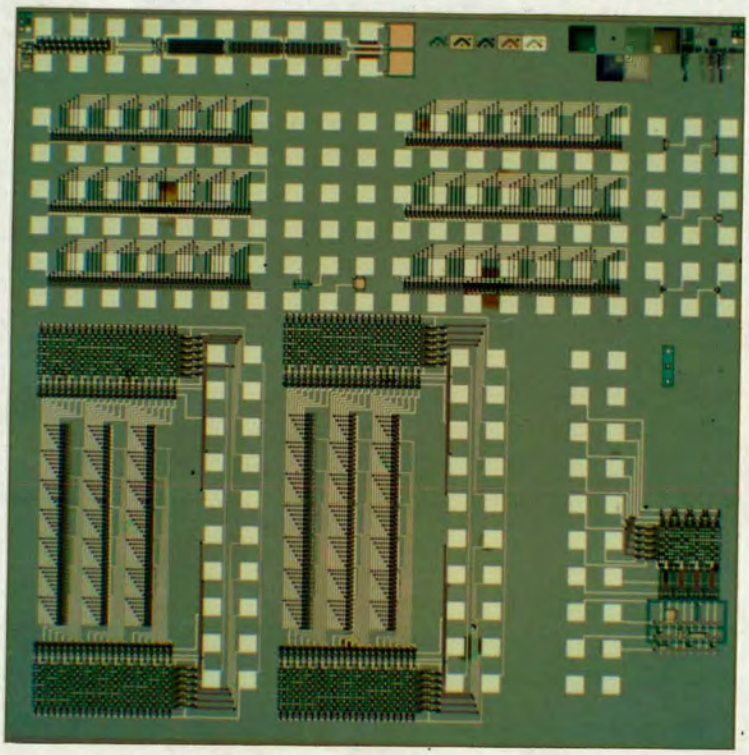


Figure 6.7. Layout of Eμ 930.

particular reticle layout chosen gave the layout shown in figure 6.8 which has alternating columns of this test chip giving a total of 76 die sites.

6.4. Vernier Results

6.4.1. Individual Verniers

The individual vernier circuits were tested using an HP 4062 parametric test system and a TAC prober used in manual mode. A standard 2 × 10 probe card was used. Software was written which allowed the digital state of each element of the vernier structure to be displayed on the computer controller screen. This program was a simple continuity checker which determined the conductivity for each vernier element in turn. The value of the layer to layer misalignment was then calculated before being displayed on screen. Error messages would be returned by the program if either both ends of the vernier were not short circuited (error 'A'), or if there were an incorrect number of 0/1 transitions (error 'B').

From chapter 5 it will be recalled that to obtain a measurement from a vernier there should be an area of open circuits located somewhere within the 'window' of the vernier. Error A mentioned above would be expected to occur if the relative overetch between the layers composing the vernier was too large for the vernier window and the area of short circuits had overlapped one end of the vernier. Error B would occur if a faulty vernier element(s) occurred giving a spurious short/open circuit(s) (and therefore an increased number of transitions) or if the vernier elements were all short/open circuit (i.e. zero transitions due to over/underetch between the vernier layers).

X and *Y* verniers for metal-polysilicon, polysilicon-contact and metal-contact were measured for each of the 76 sites across a typical wafer. Some test sites on dice at the wafer edge were physically incomplete and hence could not tested. Results for each of these layers are given by tables 6.3a) for metal-polysilicon , 6.3b) for polysilicon-contact and 6.3c) for metal-contact with the die numbering follows that given by figure 6.8. Die sites labelled 'A' or 'B' refer to the error codes explained previously. The results of each vernier type are now discussed in turn.

It was clear with the metal-polysilicon vernier that the zero-offset and window had been insufficiently large to allow for the large degree of relative overetch which had

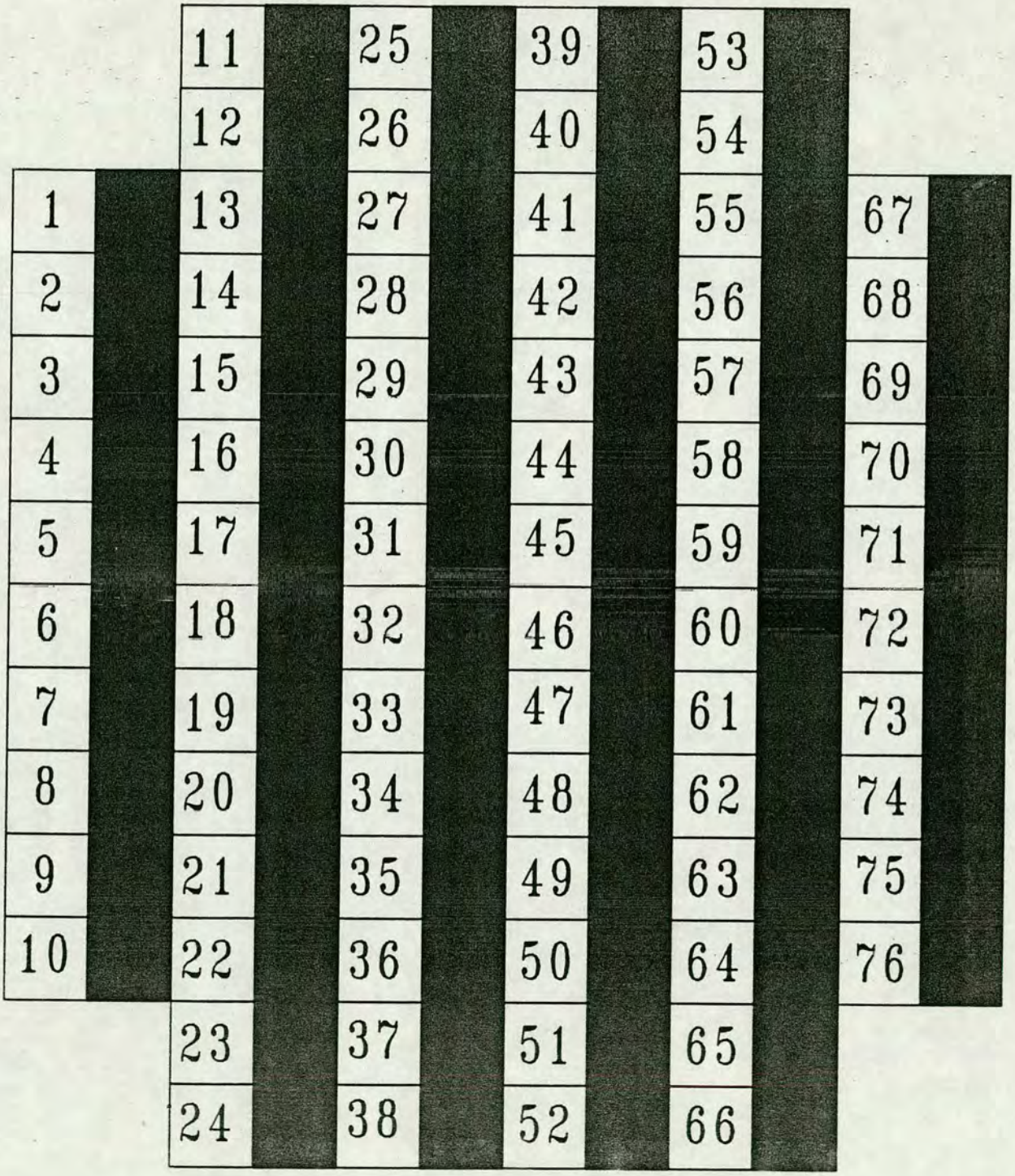


Figure 6.8. Die sites of Eμ 930.

Site Number	X (μm)	Y (μm)	Site Number	X (μm)	Y (μm)	Site Number	X (μm)	Y (μm)
1	A	A	27	A	A	52	A	A
2	A	A	28	A	A	53	*	*
3	A	A	29	A	A	54	A	A
4	A	A	30	A	A	55	A	A
5	A	A	31	A	A	56	A	A
6	A	A	32	A	A	57	A	A
7	A	A	33	A	A	58	A	A
8	A	A	34	A	A	59	A	A
9	A	A	35	A	A	60	A	A
10	A	A	36	A	A	61	A	A
11	A	−0.30	37	A	A	62	A	A
12	A	A	38	A	A	63	A	A
13	A	A	39	A	A	64	A	A
14	A	A	40	A	A	65	A	A
15	A	A	41	A	−0.10	66	A	A
16	A	A	42	A	A	67	A	*
17	A	A	43	A	A	68	A	A
18	A	0.05	44	A	A	69	A	A
19	A	A	45	A	A	70	A	A
20	A	A	46	A	A	71	A	A
21	A	A	47	A	A	72	A	A
22	A	A	48	A	A	73	A	A
23	A	A	49	A	A	74	A	A
24	A	A	50	A	A	75	A	A
25	A	A	51	A	A	76	A	A
26	A	A						

Table 6.3a) The metal-polysilicon misalignment for the individual verniers. * indicates that no physical device was present at that site.

occurred between these layers. The error code returned by the extraction program were mostly of the A type so it was clear that the verniers themselves were functional. Despite the fact that few quantitative measurements were made it was possible to observe the individual element output for each vernier on the controller and from this make some general qualitative assessments. Hence it was noted that the X vernier was consistently misaligned in the $+X$ direction across the whole wafer. Although a small number of quantitative Y misalignment measurements were made most returned error A. Again evaluation of the element output revealed a misalignment in the $-Y$ direction at the top of the wafer shifting to a $+Y$ misalignment at the bottom. The few quantitative measurements possible for these layers were noted to occur at the point where the misalignment was changing from negative to positive where the number of short circuited elements fitted the vernier window.

Site Number	X (μm)	Y (μm)	Site Number	X (μm)	Y (μm)	Site Number	X (μm)	Y (μm)
1	A	0.05	27	A	–0.35	52	B	A
2	A	–0.30	28	A	–0.15	53	*	*
3	A	0.40	29	A	0.10	54	0.65	B
4	A	0.10	30	A	0.20	55	0.60	–0.30
5	A	0.50	31	A	0.75	56	0.85	B
6	A	B	32	A	0.55	57	0.55	0.15
7	A	0.75	33	A	0.80	58	0.70	0.25
8	A	0.75	34	A	0.95	59	0.50	0.70
9	A	0.80	35	A	1.05	60	0.60	0.75
10	A	0.80	36	A	1.05	61	0.50	0.90
11	A	–0.65	37	A	A	62	0.60	0.85
12	A	–0.65	38	A	A	63	0.40	A
13	A	–0.35	39	0.80	–0.45	64	B	0.95
14	A	–0.15	40	1.05	–0.55	65	0.50	A
15	A	0.25	41	A	–0.20	66	0.75	A
16	A	0.10	42	A	–0.25	67	0.30	0.05
17	A	0.55	43	0.75	0.20	68	0.35	–0.30
18	A	0.40	44	A	0.20	69	0.15	0.05
19	A	0.75	45	0.80	0.55	70	0.40	0.25
20	A	0.75	46	0.75	0.80	71	0.20	0.45
21	A	1.00	47	0.75	0.75	72	0.45	B
22	A	0.95	48	0.75	B	73	B	B
23	A	B	49	0.75	1.00	74	B	0.80
24	A	A	50	A	0.95	75	0.10	B
25	A	–0.30	51	0.90	A	76	B	1.05
26	A	–0.55						

Table 6.3b) The polysilicon-contact misalignment for the individual verniers. * indicates that no physical device was present at that site.

The polysilicon-contact X vernier returned an A error reading for the first three columns from the left hand side of the wafer. These were noted to be off-scale in the $+X$ direction of the vernier window. The remaining three columns gave quantitative results and indicated a misalignment varying between $0.10\mu m$ and $0.90\mu m$. The Y vernier for these layers gave results across the whole wafer and a small $-Y$ misalignment at the top of the wafer of around $0.4\mu m$ was found. This varied to a larger $+Y$ misalignment at the bottom of the wafer of approximately $1.0\mu m$. Figures 6.9 and 6.10 give wafer maps of these X and Y misalignments respectively.

The metal-contact verniers gave quantitative results across the whole wafer for both the X and Y verniers. A number of verniers in the first two columns from the left returned error B, which in conjunction with observation of the vernier element output suggested insufficient overetch between the vernier layers. Figures 6.11 and 6.12 give wafer maps of

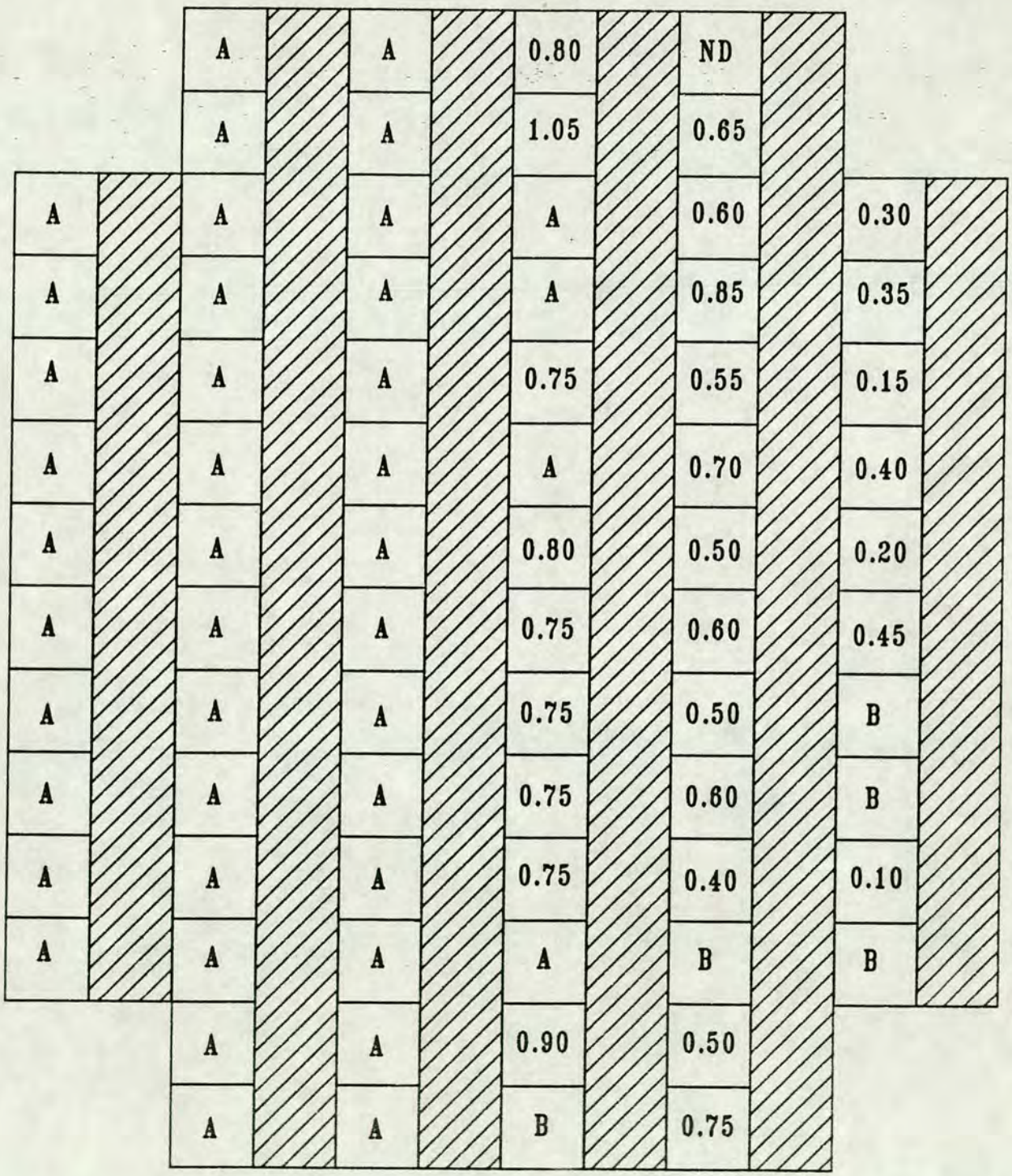


Figure 6.9. Polysilicon-contact X misalignment found for individual diode vernier.

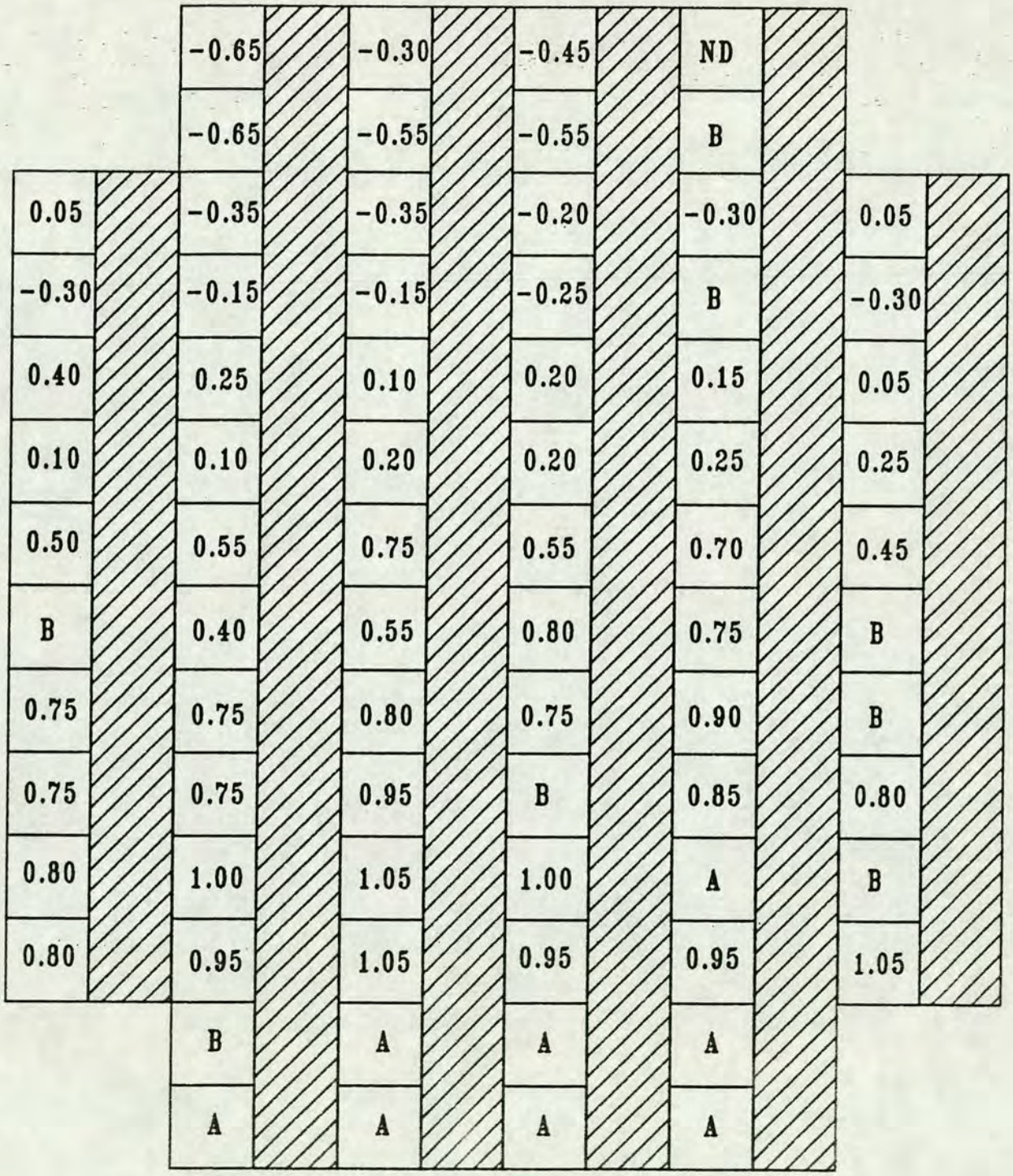


Figure 6.10. Polysilicon-contact Y misalignment found for individual diode vernier.

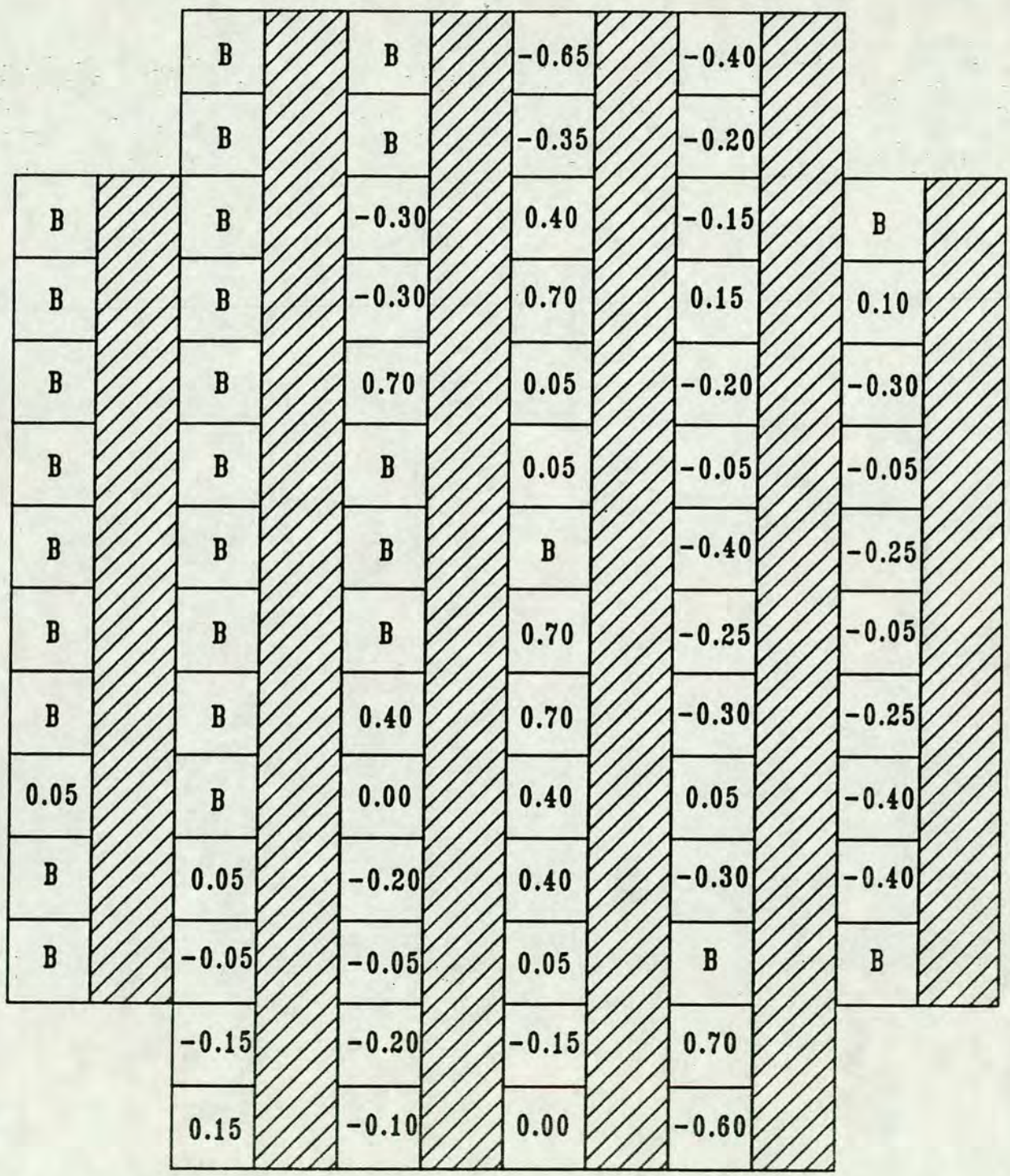


Figure 6.11. Metal-contact X misalignment found for individual diode vernier.

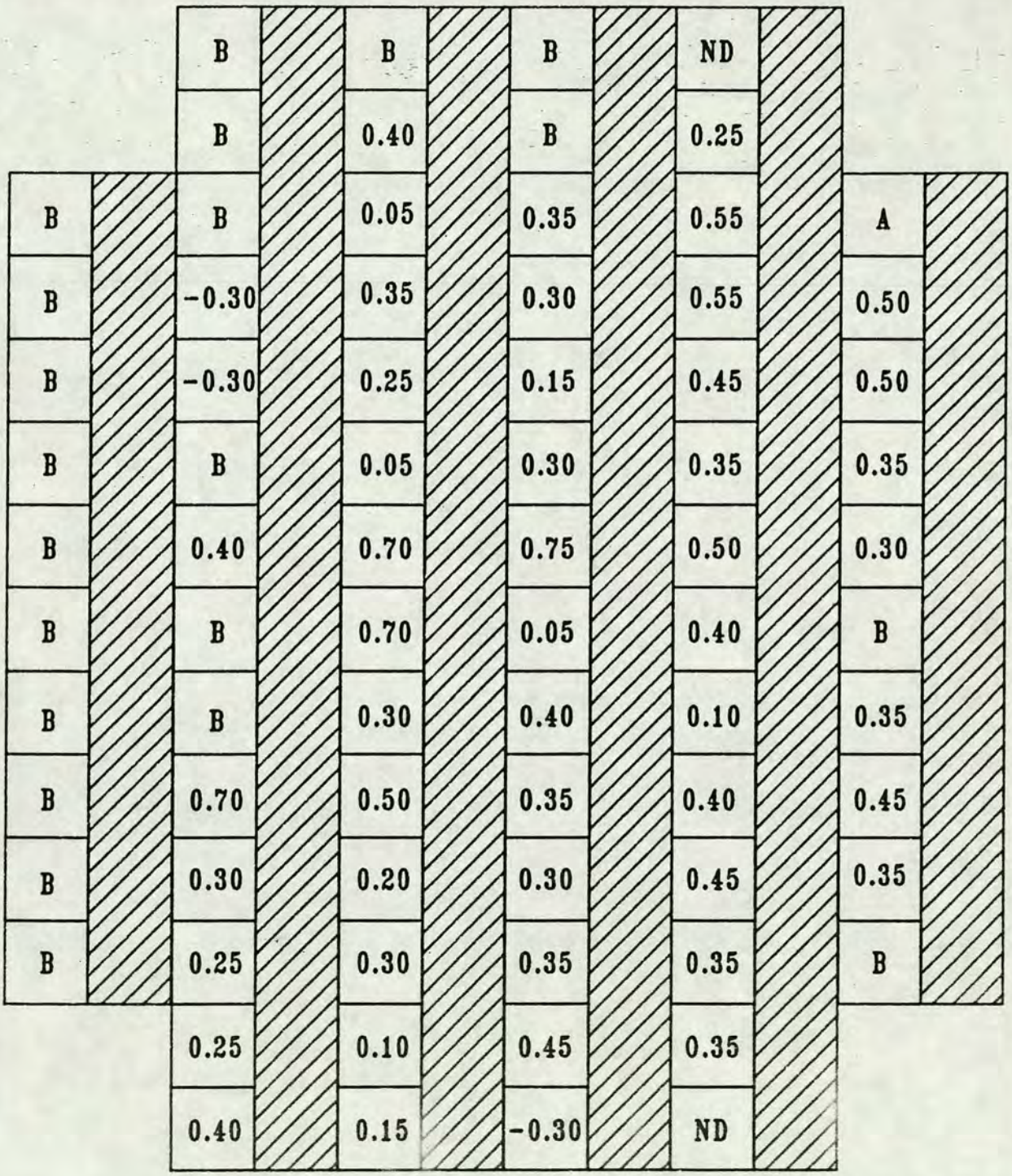


Figure 6.12. Metal-contact Y misalignment found for individual diode vernier.

Site Number	X (μm)	Y (μm)	Site Number	X (μm)	Y (μm)	Site Number	X (μm)	Y (μm)
1	B	B	27	–0.30	0.05	52	0.00	–0.30
2	B	B	28	–0.30	0.35	53	–0.40	*
3	B	B	29	0.70	0.25	54	–0.20	0.25
4	B	B	30	B	0.05	55	–0.15	0.55
5	B	B	31	B	0.70	56	0.15	0.55
6	B	B	32	B	0.70	57	–0.20	0.45
7	B	B	33	0.40	0.30	58	–0.05	0.35
8	0.05	B	34	0.00	0.50	59	–0.40	0.50
9	B	B	35	–0.20	0.20	60	–0.25	0.40
10	B	B	36	–0.05	0.30	61	–0.30	0.10
11	B	B	37	–0.20	0.10	62	0.05	0.40
12	B	B	38	–0.10	0.15	63	–0.30	0.45
13	B	B	39	–0.65	B	64	B	0.35
14	B	–0.30	40	–0.35	B	65	0.70	0.35
15	B	–0.30	41	0.40	0.35	66	–0.60	*
16	B	B	42	0.70	0.30	67	B	A
17	B	0.40	43	0.05	0.15	68	0.10	0.50
18	B	B	44	0.05	0.30	69	–0.30	0.50
19	B	B	45	B	0.75	70	–0.05	0.35
20	B	0.70	46	0.70	0.05	71	–0.25	0.30
21	0.05	0.30	47	0.70	0.40	72	–0.05	B
22	–0.05	0.25	48	0.40	0.35	73	–0.25	0.35
23	–0.15	0.25	49	0.40	0.30	74	–0.40	0.45
24	0.15	0.40	50	0.05	0.35	75	–0.40	0.35
25	B	B	51	–0.15	0.45	76	B	B
26	B	0.40						

Table 6.3c) The metal-contact misalignment for the individual verniers. * indicates that no physical device was present at that site.

these X and Y misalignments respectively.

6.4.2. Multiplex Verniers

The multiplex verniers were tested on the same HP 4062 and TAC prober system as used for the individual verniers. The software used for this was expanded to allow control of the multiplexer. The software was structured such that any selected vernier (out of the three possible per structure) could be tested at one time. The program would then output the same vernier element information and misalignment or error calculation as the individual vernier program.

Problems were encountered in making this program operational. Initial trials with nominal circuit voltages of $V_{dd} = 5V$ and $V_{ss} = 0V$ did not result in working vernier circuits. Experimentation with the supply voltages revealed that increase of V_{dd} or the voltage forced

through the vernier element continuity circuitry (V_{force}) had no effect on output yield. Only by decreasing V_{ss} to at least $-2.0V$ was it found that the multiplexer circuitry would work. This was found to be independent of the choice of both V_{ss} and V_{force} ($V_{bb} = -2.5V$ in all cases). These results are summarised in table 6.4.

$V_{dd}(V)$	$V_{ss}(V)$	$V_{force}(V)$	Output	Description
5	–1.0	6	No	Test V_{ss}
5	–1.5	6	No	at $V_{dd}=5V$
5	–2.0	6	Yes	
12	–1.0	6	No	Test V_{ss}
12	–1.5	6	No	at $V_{dd}=12V$
12	–2.5	6	Yes	
5	–2.5	2	Yes	Test V_{ss} at $V_{dd}=5V$ and $V_{force}=2V$
12	–2.5	6	Yes	Test V_{force}
12	–2.5	4	Yes	at $V_{dd}=12V$
12	–2.5	3	Yes	and $V_{ss}=-2.5V$
12	–2.5	2	Yes	
10	–2.5	6	Yes	Test V_{dd}
8	–2.5	6	Yes	at $V_{force}=12V$
6	–2.5	6	Yes	and $V_{ss}=-2.5V$
5	–2.5	6	Yes	

Table 6.4. Voltages used in experiment on multiplexer operating voltages.

Evaluation of a number of dice at V_{ss} voltages less than $-2.5V$ suggested that this would result in little further improvement of multiplexer yield. It was thought that $V_{ss}=0V$ did not result in a gate voltage sufficient to completely turn off the pass transistors. Thus when testing a vernier element spurious readings would occur due to pass transistors, other than the intended pair, conducting. Increase of V_{dd} would have no effect on this problem as it would only increase the voltage on the gate of the pass transistor, increasing any leakage current. On the other hand decreasing V_{ss} reduces the gate voltage on the pass transistor thereby switching them 'hard' off and eliminating all but the chosen testing path. This suggests that the depletion pull-up transistor aspect ratio had not been optimally chosen and would require re-design if the circuit were to operate at the nominal voltages of $V_{dd}=5V$ and $V_{ss}=0V$.

Experimental measurements were then made on the same wafer that measurements of the individual verniers had previously been taken. It was found that both the X and Y metal-polysilicon vernier gave mostly error A across the whole wafer with a number of B's.

This indicated that the combination of misalignment and relative overetch was too large for the vernier window chosen. The B errors corresponded to faulty vernier or multiplexer operation. The polysilicon-contact and metal-contact *X* vernier gave mostly error A across the whole wafer again indicating too large a misalignment and relative overetch for these verniers. The *Y* verniers for both these layers gave results across most of the wafer. The polysilicon-contact gave results across the whole wafer apart from the first column from the left where error B was returned due to low multiplexer yield. It was noted that these results matched closely those obtained individually. That is a misalignment of around $-0.6\mu m$ near the top of the wafer varying to about $1.0\mu m$ at the bottom. For the metal-contact *Y* vernier error B was returned for the first three columns. This was attributed to underetch between the two layers, which had also been observed in the individual verniers for these columns. Table 6.5 gives the polysilicon-contact and metal-contact *Y* vernier results while figures 6.13 and 6.14 respectively give wafer maps of these.

6.4.3. Comparison of Individual and Multiplex Access Verniers

The individual vernier circuits were found to yield well with only a small number being seen to fail due to faulty vernier circuitry. Those individual verniers not yielding results were mainly due to relative layer overetch resulting in measurements outside the vernier window. A number of the metal-contact verniers also did not yield due to underetch between the vernier layers. A numerical estimate of the yield of the individual vernier circuits was difficult due to the many off-scale measurements. As a rough estimate of this the polysilicon-contact *Y* vernier was used as this had most within scale measurements. Error B was interpreted as a failing vernier but error A, an off-scale measurement was not. Thus 68 out of 75 devices were seen to function giving a yield of 90.7%. Similarly the yield of the multiplex verniers was estimated. Here as with the individual access verniers many off-scale measurements were present but to allow comparisons the polysilicon-contact *Y* vernier was again used. Using the same criteria as before 55 out of 74 devices were seen to function giving a yield of 74.3%. It was thought that this was a lower estimate of the actual multiplexer yield as most of the non-functioning multiplexers were localised to the first two columns of devices. Comparisons of the yields of both vernier types in the area excluding the first two columns gives the results that 46 of 52 individual access verniers functioned giving an 88.5% yield compared to 45 of 53 multiplex access verniers, a yield of 84.9%.

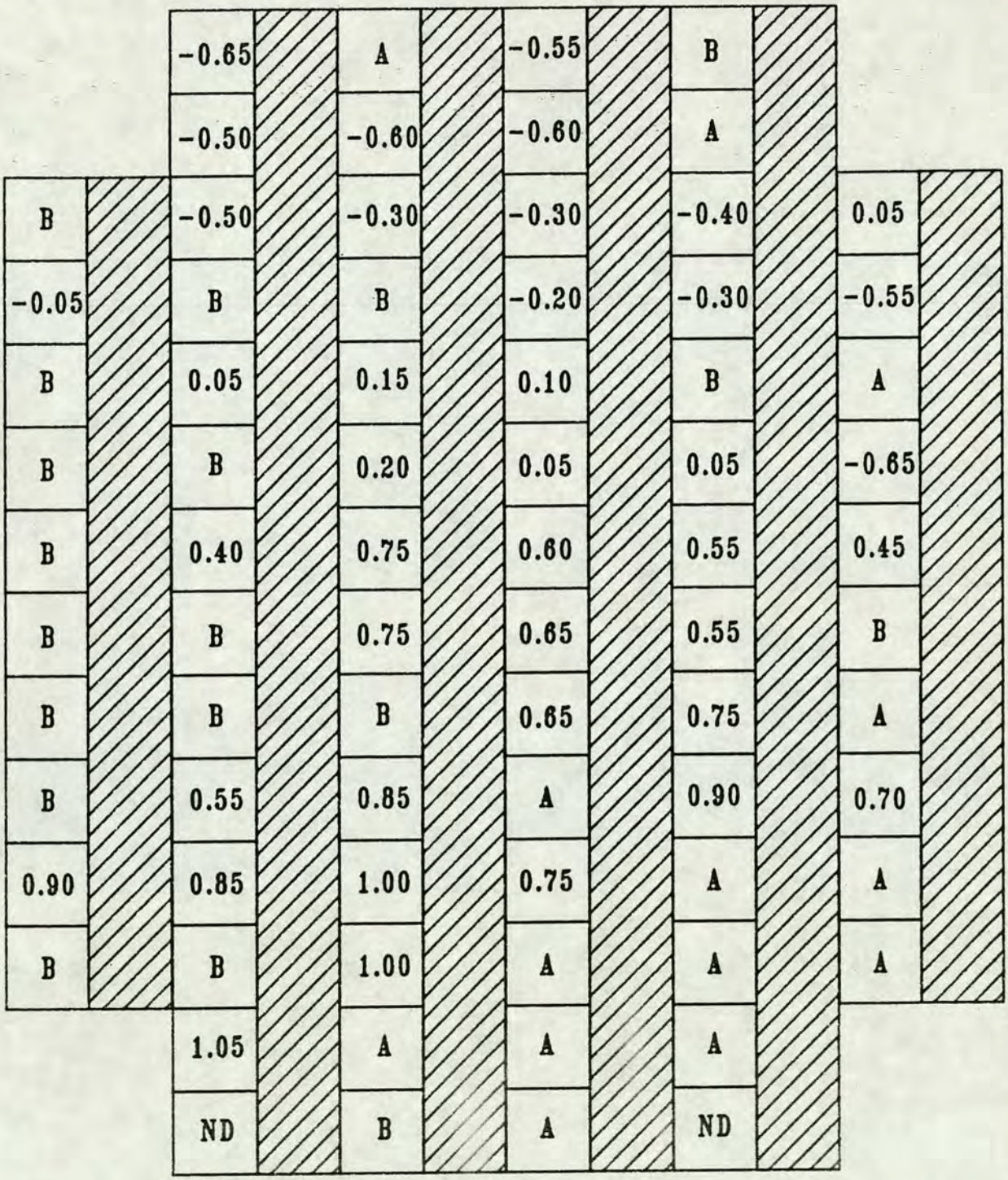


Figure 6.13. Polysilicon-contact Y misalignment found for multiplex access verniers.

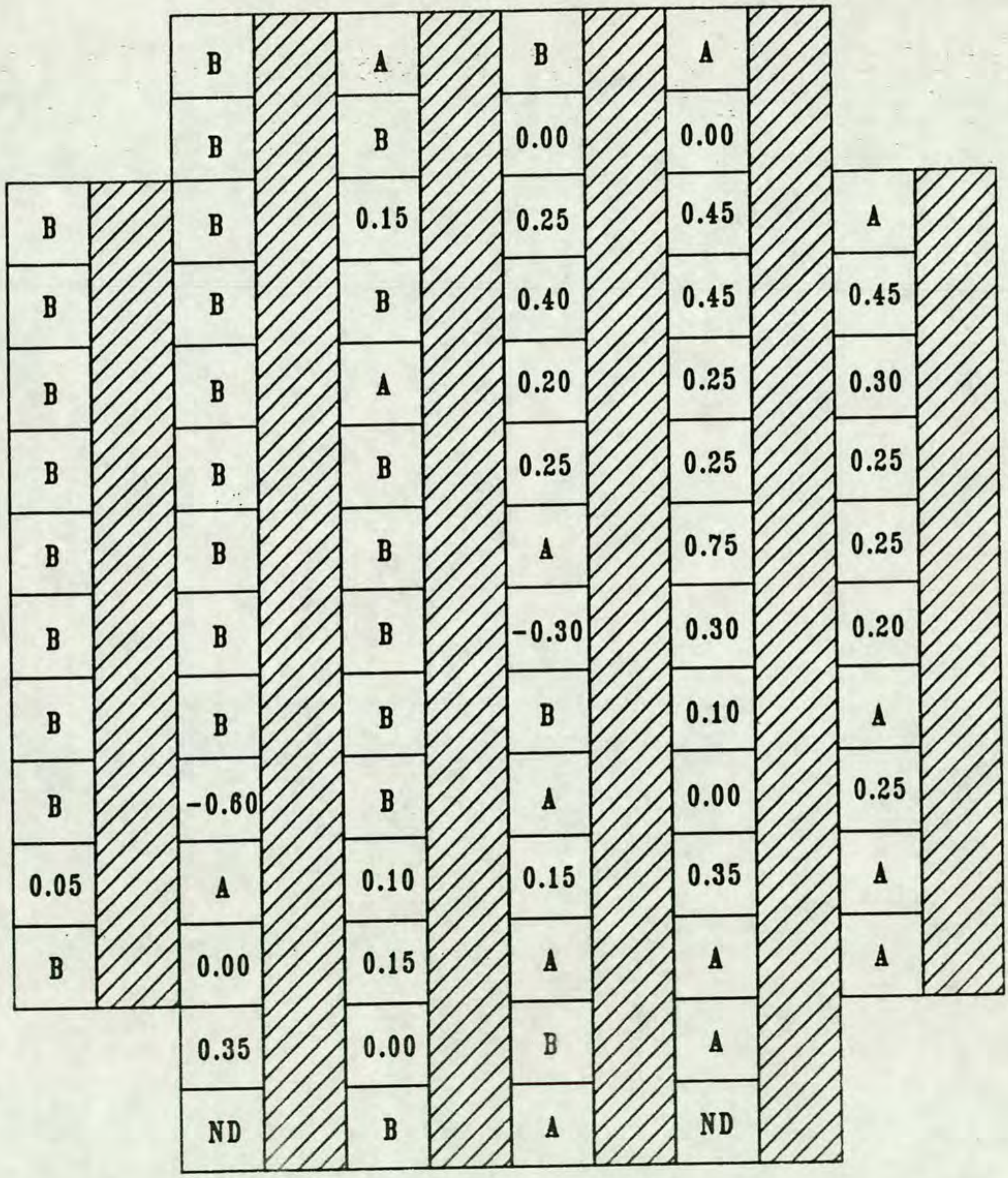


Figure 6.14. Metal-contact Y misalignment found for multiplex access verniers.

Site Number	Polysilicon-contact(μm)	Metal-contact(μm)	Site Number	Polysilicon-contact(μm)	Metal-contact(μm)	Site Number	Polysilicon-contact(μm)	Metal-contact(μm)
1	B	B	27	–0.30	0.15	52	A	A
2	–0.05	B	28	B	B	53	B	A
3	B	B	29	0.15	A	54	A	0.00
4	B	B	30	0.20	B	55	–0.40	0.45
5	B	B	31	0.75	B	56	–0.30	0.45
6	B	B	32	0.75	B	57	B	0.25
7	B	B	33	B	B	58	0.05	0.25
8	B	B	34	0.85	B	59	0.55	0.75
9	0.90	0.05	35	1.00	0.10	60	0.55	0.30
10	B	B	36	1.00	0.15	61	0.75	0.10
11	–0.65	B	37	A	0.00	62	0.90	0.00
12	–0.50	B	38	B	B	63	A	0.35
13	–0.50	B	39	–0.55	B	64	A	A
14	B	B	40	–0.60	0.00	65	A	A
15	0.05	B	41	–0.30	0.25	66	*	*
16	B	B	42	–0.20	0.40	67	0.05	A
17	0.40	B	43	0.10	0.20	68	–0.55	0.45
18	B	B	44	0.05	0.25	69	A	0.30
19	B	B	45	0.60	A	70	–0.65	0.25
20	0.55	–0.60	46	0.65	–0.30	71	0.45	0.25
21	0.85	A	47	0.65	B	72	B	0.20
22	B	0.00	48	A	A	73	A	A
23	1.05	0.35	49	0.75	0.15	74	0.70	0.25
24	*	*	50	A	A	75	A	A
25	A	A	51	A	B	76	A	A
26	–0.60	B						

Table 6.5. The Y polysilicon-contact and metal-contact misalignment or error code returned for verniers accessed via the multiplexer. * indicates that no physical device was present at that site.

Reasonable consistency between the *Y* polysilicon-contact and metal-contact individual and multiplex access verniers were seen. The corresponding *X* components for these two verniers did not give results which could be compared as although the individual access verniers for these verniers yielded data those with multiplex access resulted in off-scale readings. This was thought attributable to a combination of intra-chip variations in etch characteristics or variations in the *X* misalignment component between the individual and multiplex vernier sites due to their physical separation.

6.5. SPICE Extraction from Transistors

Measurements made for SPICE extraction on chip $E\mu$ 930 used the same hardware and software as that utilised for the work described in chapter 4 of this thesis. This consisted of an HP 4145 parametric tester with HP control computer. Software was the PARAMEX SPICE extraction program [2]. Interface of the wafer to the test equipment was achieved by use of a manual prober and 2 × 10 probe card. The probe card edge connector wiring was routed to a 'proto' board. The proto board acted in effect as a manually operated switching matrix on which the force, measurement and multiplexer control lines could be switched so that a chosen test transistor could be accessed and tested. A dual power supply was used as an ancillary voltage source. From this a $5V$ supply was used as both the V_{dd} source and as the digital high for the multiplexer. The second supply was used as a variable voltage source connected to both the current and voltage pull-up transistors which controlled the gate voltages on the switch transistors. Initial experimentation found that the multiplexer switching circuitry worked satisfactorily with $V_{dd}=5V$ and $V_{ss}=0V$ and exhibited none of the problems encountered in operation of the vernier multiplexers. This was demonstrated by extraction of V_t curves for all the test transistors in the matrix for a sample die. SPICE parameters were then extracted for a 6 × $6\mu m$ device. This was done initially with a voltage of $5V$ applied to the switching transistors but repeated at $1V$ steps up to $9V$. L_{del} and ΔW measurements were made with use of 6 × $12\mu m$ and 12 × $6\mu m$ devices respectively. Table 6.6 gives the SPICE parameters thus extracted. The SPICE parameters found showed that no problems were encountered in their extraction and that consistent sets of parameters could be obtained at different pass transistor gate voltages.

6.6. Conclusions

A test chip has been designed which incorporated the ideas originated in chapter 4 and 5 of this thesis. Testing of this test chip demonstrated that the implementation of these ideas provide a new approach for parametric testing. On-chip switching using a multiplexer to access test transistors was demonstrated to be feasible in chapter 4 and has been successfully implemented in this chapter to extract SPICE parameters. The test chip also incorporated digital structures to evaluate layer to layer misalignment. These structures were demonstrated in chapter 5 where a shift register had been used to output data but in this chip design the idea of a novel multiplexing scheme, 'the diode vernier', was included

SPICE Parameters	Pass Transistor Gate Voltage				
	5V	6V	7V	8V	9V
N_{fs} (m^{-2})	2.25×10^{15}	2.32×10^{15}	2.37×10^{15}	2.49×10^{15}	2.74×10^{15}
V_{t0} (V)	0.98	0.98	1.03	0.98	0.94
γ $(\sqrt{V})$	0.74	0.74	0.71	0.74	0.68
L_{del} (m)	1.35×10^{-6}	1.36×10^{-6}	1.36×10^{-6}	1.36×10^{-6}	1.36×10^{-6}
ΔW (m)	4.22×10^{-7}	4.93×10^{-7}	4.53×10^{-7}	4.06×10^{-7}	3.92×10^{-7}
μ_0 $(m^2V^{-1}s^{-1})$	0.074	0.080	0.082	0.078	0.079
θ (V^{-1})	0.076	0.093	0.102	0.091	0.094
V_{max} (ms^{-1})	3.85×10^5	4.36×10^5	3.88×10^5	3.64×10^5	3.49×10^5
η	0.066	0.091	0.115	0.107	0.113
δ	0.701	0.680	0.607	0.730	1.055
κ	0.146	0.265	0.373	0.399	0.368

t_{ox} $(m) = 8.5 \times 10^{-8}$ and X_j $(m) = 1.0 \times 10^{-6}$ (non-measured parameters used)

Table 6.6. SPICE parameters measured via the switching matrix at the noted gate voltages.

to accomplish this. This idea was implemented and tested successfully on this test chip where these individually accessed verniers gave results for layer to layer misalignments in both the X and Y directions. Each of these individual verniers required a fourteen pad 'footprint' for operation. This test chip also incorporated a second idea to reduce pad count and this was the use of multiplexers to access digital structures. This idea was demonstrated using the diode vernier structures. Each structure had a twenty pad 'footprint' but allowed access to three vernier structures via two multiplexers. The operation of this was demonstrated successfully and enabled misalignment measurements to be made for both the X and Y directions.

The ideas presented have given results which demonstrate their feasibility for use in situations where pad count and dense packing of test structures is required.

References

1. M.G. Buehler, "Comprehensive Test Patterns with Modular Test Structures: The 2 by N Probe-pad Array Approach," *Solid State Technology*, pp. 89-94, October 1979.

2. A. Gribben, J.M. Robertson, and A.J. Walton, "Accurate Physical Parameter Extraction for Small Geometry Devices," *Proc. of Semiconductor International Conference (SEMICON)*, pp. 186-202, Birmingham, 1986.

Chapter 7

Conclusions and Future Work

7.1. Summary

The text of this thesis began presenting the background of silicon semiconductor processing and how its control can be implemented by the techniques and methods of parametric test. These aspects were outlined in chapters 2 and 3 to place the work in context with the field of parametric test.

Chapter 4 evaluated the accessing of test transistors, via pass transistors, with the purpose of extracting their SPICE parameters. This consisted of circuit simulation work followed by test chip design and experimental measurement on test circuit configurations. This demonstrated that provided the pass transistors size and gate voltage were carefully chosen SPICE parameters could be extracted which were of comparable accuracy to the parameters derived from direct device measurement [1].

Chapter 5 was concerned with the problem of making misalignment measurements. A digital measurement technique to measure this parameter was investigated using a U-shaped vernier tooth [2, 3]. Design faults in previous vernier output circuitry were identified and a dynamic shift register successfully fabricated. The use of shift registers in this application requires careful layout at the design stage and results in a large amount of functional circuitry that must be tested using functional (i.e. clock generating) test equipment rather than conventional parametric test equipment. These limitations can be overcome by using the 'diode vernier' whose only active circuitry is one diode per vernier element, necessary to prevent parasitic conduction paths. This combined with the multiplexing scheme outlined in chapter 5 considerably simplifies the implementation of digital verniers as design is simple and testing only requires continuity testing using a parametric tester [4].

Chapter 6 described the design and testing of a test chip which incorporated the ideas explored and tested in chapters 4 and 5. The work of chapter 4 was extended by the inclusion in this test chip of an array of test transistors which were accessed via a digitally addressed multiplexer. The multiplexer controlled the operation of pass transistor switches

allowing measurements on the test device. This approach proved successful and SPICE parameters were extracted. The idea of the 'diode vernier' introduced in chapter 5 was also implemented on this test chip. In its simplest form each vernier was accessed individually and misalignment measurements were made for a number of layers across a wafer. A second idea for pad reduction was also introduced in this test chip. This was the use of digitally addressed multiplexers to control access to digital test structures. This results in a large saving in pad count particularly if it is required to access a large number of structures. This technique can be applied to any digital test structure although in this case it was demonstrated using digital misalignment verniers. These structures which were also present individually on the same chip and were used for purposes of comparison. Testing revealed that the multiplexer performed as designed which enabled misalignment measurements to be made across a wafer.

In summary several new ideas for increasing test structure density and/or reducing the number of output pads needed for parametric test structures have been presented in this thesis. The use of a multiplexer has been demonstrated in two different applications. Firstly where analogue type transistor measurements are made and secondly where connectivity tests are required. The use of a digital test structure for layer to layer misalignment has also been demonstrated and its implementation efficiency increased by the use of the diode vernier for data output rather than the previously used shift register method.

7.2. Conclusions and Suggestions for Future Work

As with any subject which is large, parametric testing generates many threads of work which cannot all be exploited fully. The work, undertaken in the course of thesis, suggested further work which is now outlined.

This thesis has demonstrated the feasibility of on-chip switching both for transistor parameter extraction and for digital test structures. In the former case although only one particular transistor switching configuration (the simplest) was considered experimentally, several others which were included in the test chip designs could be investigated to find an optimal pass transistor configuration. In the latter case on-chip switching can be extended to the testing of a wide variety of structures where electrical continuity is to be tested [5]. In all cases the individual diode vernier scheme, itself saving a number of output pads, can

be combined with the use of multiplexer circuitry to still further reduce the required pad count. As well as the vernier structures tested in this thesis, structures such as the following are seen as suitable,

(1) Contact chains. These are normally tapped at intervals along their length making them well suited to use in a multiplexed interconnect scheme.

(2) Chequerboards. Electrically connected chequerboards, with different dimensions, can be used to gauge layer etch parameters and the continuity testing of these can be adapted for multiplexer use.

(3) Area structures. Comb and serpentine as well as electromigration structures which require continuity checking for their operation can also be designed for multiplexer use.

Further improvement in pad count, for vernier structures, could be achieved by use of interdigitated X and Y elements in the same structure, obviating the need for separate X and Y structures. One problem observed while testing digital verniers was that a faulty element, away from the 0/1 transition region, was designated by the software to be part of a faulty structure. In most cases test structure yield could be increased by the use of algorithms to positively identify and hence ignore spurious outliers. A second problem was that vernier structures were unable to provide any information when a greater than anticipated amount of overetch between its constituent layers had occurred. Therefore it is recommended that the number of vernier elements be increased since this takes up little area, and in conjunction with the diode vernier interconnect scheme and a multiplexer has little overhead in terms of pad count.

The multiplexer design needs to be modified in the light of the experience of its use with the diode vernier in chapter 6. This design must be made more robust so that it is capable of functioning within a wide band of process parameters. This is essential if it is to be used to help develop new processes rather than just being used to monitor optimised production processes. Investigation of the transistor aspect ratios forming the multiplexer would be the first modification investigated.

The diode vernier can be improved by increasing the pad to tooth ratio from $N : (N/2)^2$, of the diode vernier implemented in this thesis, to $N : N(N-1)$ of the measuring scheme suggested by Morrow *et al.* [6]. This is achieved by removing the concept of 'group' and 'access' pads and making bi-directional continuity measurements between pads.

This method of making measurements makes it unsuitable for use with a multiplexer, without modification, as it is not possible to have more than one element of a multiplexer on at a given time and the 'Morrow vernier' testing scheme requires that every pad out be accessible from every other. A related use of a multiplexing scheme similar to the diode vernier, the 'passive vernier', has been developed with the advantage that no functional circuitry is required hence tests on structures with as little as three layers may be performed [7]. Testing of the 'passive vernier' requires a measurement configuration which earths all group and access pads other than those involved with the element under test thus eliminating all parasitic current paths. This design could be easily implemented into a multiplexed chip.

Table 7.1 Summarises the use of the multiplexed access schemes and shows the relationship between the number of pads and the maximum number of connectivity tests for each configuration.

Number of Pads	Number of Connectivity Tests			
	Non-multiplex Access			Multiplex Access
	Standard	Diode/Passive	'Morrow'	Standard Diode/Passive
10	9	25	90	64
12	11	36	132	256
14	13	49	182	1024
16	15	64	240	5096
18	17	81	306	16384
20	19	100	380	65536
n	$n-1$	$(n/2)^2$	$n(n-1)$	$2^n - p$

Table 7.1. The number of connectivity tests for digital vernier structures and the indicated connection scheme. p is the number of pads which are are used for the relevant voltage and current rails. Here p=4 was used.

Table 7.2 shows the increase in number of analogue measurements that can be made on transistors in an array when using a multiplexer.

These tables both demonstrate the gains that can be made using the schemes outlined in this thesis. Furthermore the increased number of connectivity tests which can be performed with a significantly reduced pad count give the designer of test structures an opportunity to design structures which would not otherwise have proved practically feasible.

Number of Pads	Number of Transistors	
	Row/Column Access	Multiplex Access
10	25	16
12	36	64
14	49	256
16	64	1024
18	81	4096
20	100	16384
n	$(n/2)^2$	2^{n-p}

Table 7.2. Comparison of number of transistors which can be measured accessible for a given number of pads. p is the number of pads which are are used for the relevant voltage and current rails. Here p=6 was used. This is two more than the required in table 7.1 as Kelvin measurements are required here.

Finally, as outlined in chapters 2 and 3, increasing emphasis is being placed on automation of all aspects of semiconductor technology and parametric test is no exception to this. One future avenue for this is the automatic layout of parametric test structures at the design stage [8,9]. The proposed system would simply require the process engineer to define the test structures required and, where appropriate, their dimensions, e.g. transistor W and L, after which the complete design layout would be generated. This would also include any multiplexing circuitry so that the engineer would have no need to become involved in any functional circuit design. Since both the test structure types and their layout will be known software can also be written to automatically generate the measurement routines thereby significantly reducing the engineering effort required. Work to integrate compiler software such as this would be an obvious extension to the work of this thesis.

References

1. D. Ward, A.J. Walton, and J.M. Robertson, "The Measurement of Transistor Characteristics Using On-chip Switching for the Connection of Instrumentation," *Proc. of the 17th European Solid State Device Research Conference, ESSDERC 1987*, pp. 919-922, Bologna, September 1987.

2. B.M.M. Henderson, A.M. Gundlach, and A.J. Walton, "Integrated-circuit Test Structure Which Uses a Vernier to Electrically Measure Mask Misalignment," *Electronics Letters*, vol. 19, no. 21, pp. 868-869, 13th October 1983.

3. B.M.M. Henderson and A.J. Walton, "A Complete Digital Vernier Tool for the Measurement of Mask Misalignment," *Proc. of IEEE VLSI Workshop on Test Structures*, pp. 34-49, Long Beach, California, February 1986.

4. A.J. Walton, D. Ward, J.R. Robertson, and R.J. Holwill, "A Novel Approach for an Electrical Vernier to Measure Mask Misalignment," *Proc. of 19th European Solid State Device Research Conference, ESSDERC 89*, pp. 950-953, Berlin, September 1989.

5. A.J. Walton, W. Gammie, D. Morrow, J.T.M. Stevenson, and R.J. Holwill, "A Novel Approach for Reducing the Area Occupied by Contact Pads on Process Control Chips," *Proc. of the 1990 International Conference on Microelectronic Test Structures (ICMTS)*, vol. 3, no. 1, pp. 75-80, San Diego, March 1990.

6. D. Morrow, A.J. Walton, W.R. Gammie, M. Fallon, J.T.M. Stevenson, and R.J. Holwill, "A New Improved Electrical Vernier to Measure Mask Misalignment," *Proc. of 20th European Solid State Device Research Conference, ESSDERC 90*, pp. 85-88, Nottingham, September 1990.

7. A.J. Walton, W. Gammie, M. Fallon, D. Ward, and R.J. Holwill, "A Passive Electrical Vernier for Measuring Mask Misalignment," *Electronics Letters*, vol. 26, no. 16, pp. 1173-1175, July 1990.

8. G.A. Jennings and C.A. Pina, "Automated Parametric Test Software," *Proc. IEEE VLSI Workshop on Test Structures*, pp. 415-432, Long Beach, California, February 1986.

9. A.A. Walker, A.J. Walton, R. Holwill, and J.M. Robertson, "The Implementation of a Process Control Chip Compiler," *Proc. IEEE VLSI Workshop on Test Structures*, pp. 433-453, Long Beach, California, February 1986.

Appendix 1

EMF 6μm NMOS Runsheet

The following is a sample EMF runsheet for its standard NMOS process. This particular runsheet is a copy of that employed in production of device *E*μ 930.

EDINBURGH MICROFABRICATION FACILITY

N-CHANNEL SILICON GATE PROCESS 2

BATCH NUMBER: 90009 START DATE: 27/2/90

DEVICE IDENTIFICATION: Eu928,930

MASK SET: SERCB207,1989

MASKING SEQUENCE: 1 2 3 4 6 7
MASK REV.LETTERS: A A A A A A

STARTING MATERIAL: 14-20 ohm.cm.(100) P-type,3in.Dia.

No. OF WAFER STARTS: 12 + 1

INITIAL CLEAN

Start date: Start time: Initials:

10 min. boil in 2:1, Sulphuric acid:Hydrogen peroxide in Teflon jig
D.I water wash
Dip 3 min. in 10% HF in Polypropylene jig
Wash and spin dry

Finish date: Finish time: Initials:

INITIAL OXIDE

Start date: Start time: Initials:

Furnace #1, 950oC, idling on oxygen
Preset gas flows as follows:
Oxygen 20% (1.5 l/min.)
HCl 15% (0.15 l/min.)
Hydrogen 10% (1.7 l/min.)

Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen + HCl
10min.Oxygen + HCl + Hydrogen
5 min.Oxygen

Measure oxide thickness:

Finish date: Finish time: Initials:

SILICON NITRIDE DEPOSITION

Furnace #3, 800oC
Preset flows: Dichlorosilane,30 cc/min. Ammonia,90 cc/min.
Deposition time: 10 min.
Pressure during deposition: mTorr

Measure Si3N4 thickness:

Finish date: Finish time: Initials:

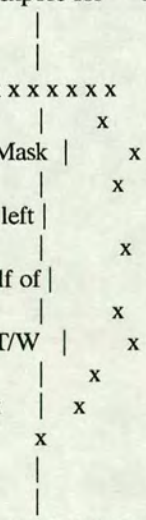
1st PHOTO (POSITIVE RESIST) LAYER# 1

Start date: Start time: Initials:

HMDS vapour box prime for 30 min.

Spin HPR 204 at 6000 rpm for 30 secs
Soft bake at 105oC for 30 min in static oven

Align and expose for secs. (Optimetrix)



Develop in 1 vol LSI 2 Developer, 3 vols DI water at 30oC for 60 secs
Inspect for proper development.

Measure resist image: microns

Hard bake at 130,oC for 30 min. in static oven
Inspect for proper baking

Finish date: Finish time: Initials:

BORON IMPLANT

Start date: Start time: Initials:

B11+ 2 e13 atoms/sq.cm. 130 keV

Finish date: Finish time: Initials:

4:1 ETCH

Start date: Start time: Initials:

Immerse in 4:1, Ammonium Fluoride soln.(40%w/v) : HF
Etch time: 30 secs
Wash and spin dry

Finish date: Finish time: Initials:

SILICON NITRIDE RIE ETCH

Start date: Start time: Initials:

RIE etch 48 cc/min CF4 + 8 cc H2, 30 mTorr, 750 W

Repeat above with wafers face downwards to etch backs.

Finish date: Finish time: Initials:

RESIST STRIP

Start date: Start time: Initials:

Immerse in Fuming Nitric Acid 10 min
Wash and spin dry
Inspect for removal of resist.

Measure etched image: microns

Finish date: Finish time: Initials:

PRE-DIFFUSION CLEAN

Start date: Start time: Initials:

Dip in 10% HF for 15 secs.
Wash and spin dry.

Finish date: Finish time: Initials:

FIELD OXIDE

Start date: Start time: Initials:

Furnace #7, 950oC, idling on oxygen

Preset gas flows as follows:
Oxygen 24.5% (1.22 l/min.)
Hydrogen 20% (2.0 l/min.)
HCl 10% (0.1 l/min.)
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen + HCl
0.5 hours Oxygen + Hydrogen + HCl
15.5 hours Oxygen + Hydrogen
5 min.Oxygen

Measure oxide thickness:

Finish date: Finish time: Initials:

RESIST COAT

Start date: Start time: Initials:

Spin HPR 204 at 6000 rpm for 30 secs.
Hard bake for 30 min. at 130oC in static oven.
Inspect for proper baking

Finish date: Finish time: Initials:

4:1 ETCH

Start date: Start time: Initials:

Immerse in 4:1, Ammonium Fluoride soln.(40%w/v) : HF
Etch time: (Backs dewet ~6 min)
Wash and spin dry

Finish date: Finish time: Initials:

RESIST STRIP

Start date: Start time: Initials:

Immerse in Fuming Nitric Acid 10 min
Wash and spin dry
Inspect for removal of resist.

Finish date: Finish time: Initials:

OXIDE ETCH

Start date: Start time: Initials:

Immerse in 4:1, Ammonium Fluoride soln.(40%w/v) : HF for 15 secs.
Wash and spin dry

Finish date: Finish time: Initials:

SILICON NITRIDE RIE ETCH

Start date: Start time: Initials:

RIE etch 48 cc/min CF4 + 8 cc H2, 30 mTorr, 750 W

Finish date: Finish time: Initials:

OXIDE ETCH

Start date: Start time: Initials:

Immerse in 4:1, Ammonium Fluoride soln.(40%w/v) : HF to dewet scribelines
~45 secs

Wash and spin dry

Measure etched image: microns

Finish date: Finish time: Initials:

2nd PHOTO (POSITIVE RESIST) LAYER# 2

Start date: Start time: Initials:

Pre-spin bake, furnace#1, 950oC, Nitrogen 20% (2 l/min), 5 min.

Spin HPR 204 at 6000 rpm for 30 secs
Soft bake at 105oC for 30 min in static oven
Align and expose for secs. (Optimetrix)
Develop in 1 vol LSI 2 Developer, 3 vols DI water at 30oC for 60 secs
Inspect for proper development.

Measure resist image: microns

Hard bake at 130oC for 30 min. in static oven.
Inspect for proper baking

Finish date: Finish time: Initials:

ARSENIC IMPLANT

Start date: Start time: Initials:

As75++ 1.5e12 atoms/sq.cm. 90 keV

Finish date: Finish time: Initials:

RESIST STRIP

Start date: Start time: Initials:

Immerse in Fuming Nitric Acid 10 min
Wash and spin dry
Inspect for removal of resist.

Finish date: Finish time: Initials:

PRE-DIFFUSION CLEAN

Start date: Start time: Initials:

Dip in 10% HF for 15 secs.
Wash and spin dry.

Finish date: Finish time: Initials:

GATE OXIDE

Start date: Start time: Initials:

Furnace #1, 950oC, idling on oxygen
Preset gas flows as follows:
Oxygen 20% (1.5 l/min.)
HCl 15% (0.15 l/min.)
Hydrogen 10% (1.7 l/min.)
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen + HCl
17min.Oxygen + HCl + Hydrogen
5 min.Oxygen

Measure oxide thickness:

Finish date: Finish time: Initials:

BORON IMPLANT

Start date: Start time: Initials:

B11+ 4.0 e11 atoms/sq.cm. 40 keV

Finish date: Finish time: Initials:

RESIST STRIP

Start date: Start time: Initials:

Immerse in Fuming Nitric Acid 10 min
Wash and spin dry

Finish date: Finish time: Initials:

ANNEAL

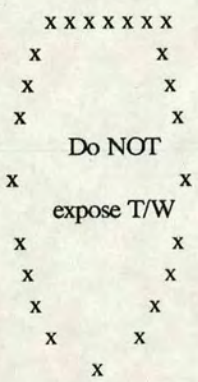
Start date: Start time: Initials:

Furnace #1, 950oC, idling on nitrogen
Preset gas flows as follows:
Nitrogen 20% (2.0 l/min.)
Load wafers into furnace for 30 min.

3rd PHOTO (POSITIVE RESIST) LAYER# 3

Start date: Start time: Initials:

Spin HPR 204 at 6000 rpm for 30 secs
Soft bake at 105oC for 30 min in static oven
Align and expose for secs. (Optimetrix)



Develop in 1 vol LSI 2 Developer, 3 vols DI water at 30oC for 60 secs
Inspect for proper development.

Measure resist image: microns

Hard bake at 130oC for 30 min. in static oven.
Inspect for proper baking

Finish date: Finish time: Initials:

OXIDE ETCH

Start date: Start time: Initials:

Immerse in 4:1, Ammonium Fluoride soln.(40%w/v) : HF to dewet scribelines
~1.5 min

Wash and spin dry

Finish date: Finish time: Initials:

RESIST STRIP

Start date: Start time: Initials:

Immerse in Fuming Nitric Acid 10 min
Wash and spin dry
Inspect for removal of resist.

Measure etched image: microns

Finish date: Finish time: Initials:

PRE-DIFFUSION CLEAN

Start date: Start time: Initials:

Dip in 10% HF for 5 secs.
Wash and spin dry.

Finish date: Finish time: Initials:

POLY-SILICON DEPOSITION

Start date: Start time: Initials:

Furnace #4, 600oC
Preset flows: Silane,60 cc/min.
Deposition time: 45 min.
Pressure during deposition: mTorr

Measure poly-silicon thickness:

Finish date: Finish time: Initials:

POLY OXIDE

Start date: Start time: Initials:

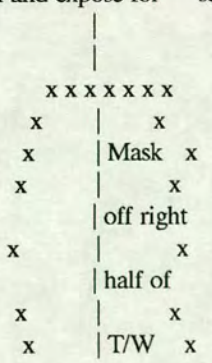
Furnace #1, 950oC, idling on oxygen
Preset gas flows as follows:
Oxygen 20% (1.5 l/min.)
HCl 15% (0.15 l/min.)
Hydrogen 10% (1.7 l/min.)
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen + HCl
18min.Oxygen + HCl + Hydrogen
5 min.Oxygen

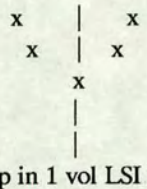
Finish date: Finish time: Initials:

4th PHOTO (POSITIVE RESIST) LAYER# 4

Start date: Start time: Initials:

Spin HPR 204 at 6000 rpm for 30 secs
Soft bake at 105oC for 30 min in static oven
Align and expose for secs. (Optimetrix)





Develop in 1 vol LSI 2 Developer, 3 vols DI water at 30oC for 60 secs
Inspect for proper development.

Measure resist image: microns

Hard bake at 130oC for 30 min. in static oven.
Inspect for proper baking

Finish date: Finish time: Initials:

OXIDE ETCH

Start date: Start time: Initials:

Immerse in 4:1, Ammonium Fluoride soln.(40%w/v) : HF to dewet t/w
~1 min

Wash and spin dry

Finish date: Finish time: Initials:

POLY SILICON RIE ETCH

Start date: Start time: Initials:

RIE etch to clear patterns in CF4/O2

Repeat above with wafers face downwards to etch backs.

Finish date: Finish time: Initials:

RESIST STRIP

Start date: Start time: Initials:

Immerse in Fuming Nitric Acid 10 min
Wash and spin dry
Inspect for removal of resist.

Measure etched image: microns

Finish date: Finish time: Initials:

OXIDE ETCH

Start date: Start time: Initials:

Immerse in 4:1, Ammonium Fluoride soln.(40%w/v) : HF to dewet t/w
~1.5 min

Wash and spin dry

Measure etched image: microns

Finish date: Finish time: Initials:

PRE-DIFFUSION CLEAN

Start date: Start time: Initials:

Dip in 10% HF for 15 secs.
Wash and spin dry.

Finish date: Finish time: Initials:

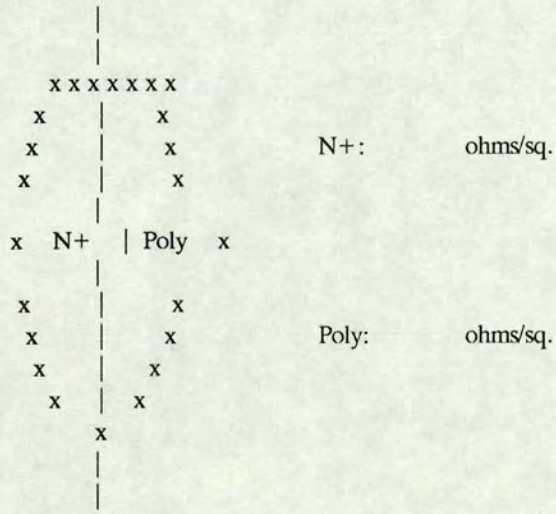
PHOSPHORUS DEPOSITION (SOLID SOURCE)

Start date: Start time: Initials:

Furnace #5, 850oC, idling on Nitrogen
Preset gas flows as follows:
Nitrogen 50 (2.0 l/min.)

Insert wafers at 4 ins./min.
20 min. ramp at 8.1oC/min. to up 1000oC
15 min. soak
20 min. ramp at 8.1oC/min. down to 850oC
Remove wafers at 4ins./min.

Measure sheet resistances



Finish date: Finish time: Initials:

PHOSPHORUS DEGLAZE

Start date: Start time: Initials:

Immerse for 30 secs. in 10% HF (1 vol HF, 9 vols DI)
Wash and spin dry

Finish date: Finish time: Initials:

POLY OXIDE

Start date: Start time: Initials:

Furnace #7, 950oC, idling on oxygen
Preset gas flows as follows:
Oxygen 20% (1.5 l/min.)
HCl 15% (0.15 l/min.)
Hydrogen 10% (1.7 l/min.)
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen + HCl
18min.Oxygen + HCl + Hydrogen
5 min.Oxygen

Finish date: Finish time: Initials:

REFLOW PYRO DEPOSITION

Start date: Start time: Initials:

PWS 2000 Hotplate at 430oC, in right hand rest position.
Preset SPEED: 200
Preset gas flows as follows:
Nitrogen(02),80 (4.0 l/min):Nitrogen(SiH4),60 (2.9 l/min)
5%Silane,110 (1.3l/min): 1%Phosphene,80 (0.96l/min): Oxygen,60 (0.65l/min)
Water flow, 100

Include one fresh 14-20 ohm.cm. P-type test wafer per batch.

Place up to 6 wafers onto hotplate as close as possible to centre.
Press button <-- to deposit
When hotplate stops, remove wafers to steel worktop with Bernoulli tweezer
Reload with fresh wafers and press button -->
Continue with whole batch.

Measured thickness:

NOTE: Proceed immediately to First Reflow

Finish date: Finish time: Initials:

FIRST REFLOW
FURNACE# 2 (O2)
Temperature: 1050oC
Idling ambient: Oxygen

Preset gas flows as follows:
Oxygen 50 (2.0 l/min.)

Start date: Start time: Initials:

20 min. furnace time

Etch reflow pyro off extra T/W in 4:1, NH4F:HF.

Measure sheet resistance at 5 points: ohms/sq.
Discard T/W after use.

Finish date: Finish time: Initials:

DENSIFICATION OF REFLOW PYRO

Start date: Start time: Initials:

Furnace #7, 950oC, idling on oxygen
Preset gas flows as follows:
Oxygen 28% (1.4 l/min.)
Hydrogen 20% (2.0 l/min.)
Load wafers into furnace with Oxygen only flowing.
5 min.Oxygen
15 min.Oxygen + Hydrogen
5 min.Oxygen

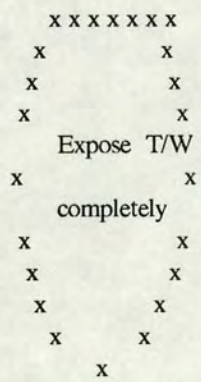
NOTE: Proceed immediately to resist spin for contact photo.

Finish date: Finish time: Initials:

5th PHOTO (POSITIVE RESIST) LAYER# 6

Start date: Start time: Initials:

Spin HPR 204 at 6000 rpm for 30 secs
Soft bake at 105oC for 30 min in static oven
Align and expose for secs. (Optimetrix)



Develop in 1 vol LSI 2 Developer, 3 vols DI water at 30oC for 60 secs
Inspect for proper development.

Measure resist image: microns

Hard bake at 130oC for 30 min. in static oven.
Inspect for proper baking

Finish date: Finish time: Initials:

OXIDE RIE ETCH

Start date: Start time: Initials:

RIE etch in CHF3 + He

Finish date: Finish time: Initials:

RESIST STRIP

Start date: Start time: Initials:

Oxygen plasma ash 30 min.
Immerse in Fuming Nitric Acid 10 min
Wash and spin dry
Inspect for removal of resist.

Measure etched image: microns

Finish date: Finish time: Initials:

SECOND REFLOW

Start date: Start time: Initials:

Furnace #2, 1050oC, idling on Nitrogen
20 min. Nitrogen ,25,(1 l/min.)

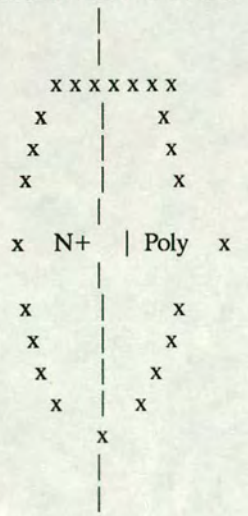
Finish date: Finish time: Initials:

PRE-ALUMINIUM EVAPORATION CLEAN (N-CH.SI GATE)

Start date: Start time: Initials:

Dip 20 secs. in reflow etch: 25 vols Ammonium Fluoride soln.(40%w/v),1 vol HF
Wash and spin dry

Re-measure sheet resistances



N+: ohms/sq.

Poly: ohms/sq.

Discard test wafer

Finish date: Finish time: Initials:

ALUMINIUM EVAPORATION (Si GATE)

Start date: Start time: Initials:

Load wafers on palettes and load into Balzers BAS 450 coater.
Pump system to 5e-6 or better with Meissner trap.
Close shutter
Throttle pump and admit argon at 2e-3.
Set integrator at 11500, Range 3
Run up Aluminium/Silicon target to 6 kW.
Open shutter until integrator times out.
Warm up Meissner and chamber.
Vent system and remove wafers.

Finish date: Finish time: Initials:

6th PHOTO (POSITIVE RESIST) LAYER# 7

Start date: Start time: Initials:

Spin HPR 204 at 4000 rpm for 30 secs
Soft bake at 105oC for 30 min in static oven
Align and expose for secs. (Optimetrix)
Develop in 1 vol LSI 2 Developer, 3 vols DI water at 30oC for 60 secs
Inspect for proper development.

Measure resist image: microns

Hard bake at 130oC for >60 min. in static oven.
Inspect for proper baking

Finish date: Finish time: Initials:

ALUMINIUM ETCH

Start date: Start time: Initials:

R.I.E. etch to clear patterns.

Finish date: Finish time: Initials:

RESIST STRIP

Start date: Start time: Initials:

Immerse in Fuming Nitric Acid 10 min
Wash and spin dry
Inspect for removal of resist.

Measure etched image: microns

Measure AlSi thickness: Microns

Finish date: Finish time: Initials:

SINTER

Start date: Start time: Initials:

Furnace #8, 435oC, idling on Nitrogen
5 min. Nitrogen,25,(1 l/min.)
10 min. 40% Hydrogen/Nitrogen,25,(1 l/min.)
5 min. Nitrogen

Finish date: Finish time: Initials:

ELECTRICAL TEST

Start date: Start time: Initials:

Finish date: Finish time: Initials:

Appendix 2

SPICE Parameters: a Description

This appendix gives a brief outline of the physical meaning of the level 3 SPICE parameters employed by the PARAMEX extraction software [1]. The parameters used in PARAMEX were based on those employed by Vladimirescu and Liu in their description of SPICE 2.G [2] but with "some further theoretical and some empirical factors added to produce greater accuracy" [3]. The level 3 SPICE model is a semi-empirical model where a number of the parameters are dimensionless 'curve-fitting parameters'. The level 3 parameters can be divided into electrical and processing types. Of the parameters employed in PARAMEX, t_{ox} the gate oxide thickness, and X_j the junction depth are of the processing type while the remainder are electrically derived.

V_{t0} is the extrapolated zero-bias threshold voltage. PARAMEX finds this value by evaluating the point of the maximum rate of change of slope of extracted $I_{ds} : V_{gs}$ data.

γ is the bulk threshold parameter and represents the proportionality factor relating the back bias voltage to the threshold voltage.

L_{del} is the lateral diffusion of the source/drain under the gate region. If L_{mask} is the drawn channel length then the effective channel length (L) is given by, $L = L_{mask} - 2L_{del}$.

ΔW is width reduction due to processing caused by the bird's beak effect in the field oxide and the enroachment of the field implant into the channel region. If W_{mask} is the drawn channel width then the effective channel width (W) is given by, $W = W_{mask} - 2\Delta W$.

μ_0 is the surface mobility at low gate voltages. The model assumes that mobility is at its maximum at threshold voltage and that there is a gradual mobility degradation as gate voltage increases. θ models this degradation of mobility as a function of gate voltage.

V_{max} is the maximum carrier velocity and is a measure of the reduced carrier mobility with increasing drain voltage. This affects the drain-source saturation voltage of the MOSFET.

N_{fs} is the effective fast surface state density and is a parameter related to charge concentrations. This parameter is a measure of the slope of the subthreshold gate voltage

against drain current characteristic.

η is the static drain feedback coefficient and models the effect that the drain voltage has on threshold voltage.

δ is the narrow channel width factor and takes account of the effect on threshold voltage that occur in a narrow device at a non-zero substrate bias.

κ is the saturation slope coefficient which characterises the slope of the drain voltage against drain current curve in saturation.

References

1. A. Gribben, J.M. Robertson, and A.J. Walton, "Accurate Physical Parameter Extraction for Small Geometry Devices," *Proc. of Semiconductor International Conference (SEMICON)*, pp. 186-202, Birmingham, 1986.

2. A. Vladimirescu and S. Liu, "The Simulation of MOS Integrated Circuits Using SPICE 2," *Memo. No. UCB/ERL MBO/7*, Electronics Research Laboratory, College of Engineering, University of California, Berkley, February 1980.

3. A. Gribben, SPICE 2 Level 3 MOSFET Model, University of Edinburgh, Dept. of Elec. Eng., Internal Report.

Appendix 3

Published Papers

The following pages give copies of the papers, containing work by the author, which are relevant to the work of this thesis.

"The Measurement of Transistor Characteristics Using On-chip Switching for the Connection of Instrumentation" was presented at the 17th European Solid State Device Research Conference (ESSDERC 1987) held in Bologna, September 1987.

"A Novel Approach for an Electrical Vernier to Measure Mask Misalignment" was presented at ESSDERC 1989 held in Berlin, September 1989.

"A Passive Electrical Vernier for Measuring Mask Misalignment" was published in Electronics Letters, Volume 26, Number 16 in July 1990.

C4.1.2

The Measurement of Transistor Characteristics Using On-chip Switching for the Connection of Instrumentation

D Ward, A J Walton, J M Robertson

Department of Electrical Engineering,
Kings Buildings,
University of Edinburgh,
Edinburgh, EH9 3JL,
Scotland

This paper investigates the feasibility of using on-chip switching for the instrumentation used to measure transistor characteristics. The effect of the switching transistors on the measurements are evaluated by comparing the SPICE parameters extracted from measurements made via the switching transistors with those derived directly. It is shown that accurate SPICE parameters can be extracted from process control chips with on-chip switching.

1. INTRODUCTION

The measurement of transistors is traditionally performed by a parametric tester using a switching matrix to connect the instrumentation to the appropriate pins. Each transistor may use up to four pads and hence much of the area on the test chip is not occupied by the test devices themselves. Not only are a large number of pads required but as a consequence, a large number of expensive relays are necessary and these significantly reduce the speed of measurement. If the switching matrix can be located on the chip then the pad count can be reduced and switching speeds increased. This approach has been used previously to make yield evaluations with contact chains and transistor arrays when only qualitative measurements were required [1]. This paper will address some of the factors that need to be considered when quantitative measurements are to be performed.

2. SIMULATION OF THE SWITCHING TRANSISTOR

Figure 1 shows one configuration for measuring transistor characteristics. Initial simulation of this circuit with pass transistors as switches for both forcing current and sensing voltage were made using SPICE [2]. These indicated that the use of pass

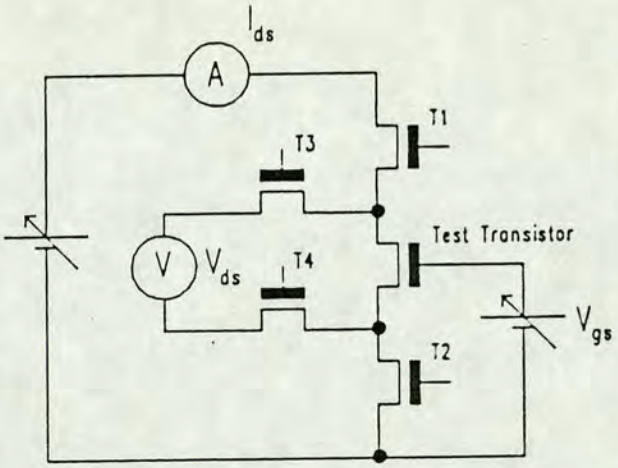


Figure 1. Circuit using pass transistors for on-chip switching to measure transistor characteristics.

transistors in a voltage sensing circuit would cause no appreciable voltage drop across the pass transistor provided the gate voltage on that transistor was at least V_t above the voltage to be sensed. This is illustrated in figure 2. However it was found that in a current forcing situation, the transistor $T1$ in figure 1 limited the current flow in the circuit, saturating at a lower I_{ds} due to its non-zero source voltage. This is shown in the simulation of figure 3 where current limiting can be observed for transistor $T1$. The above

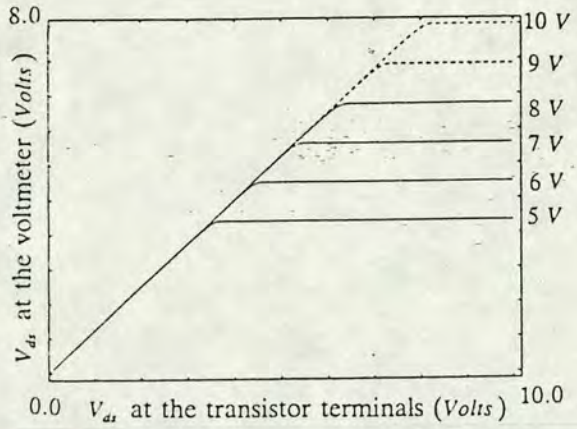


Figure 2. SPICE simulation of V_{ds} sensed by the voltmeter plotted against V_{ds} at the transistor terminals for different values of gate voltage on the pass transistors T3 and T4.

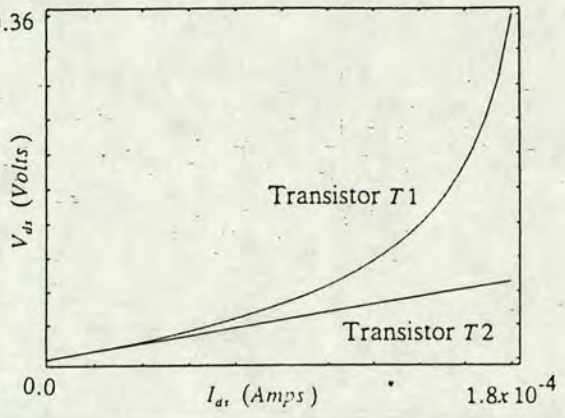


Figure 3. Simulated relationship between V_{ds} and I_{ds} for the transistors T1 and T2 in Figure 1.

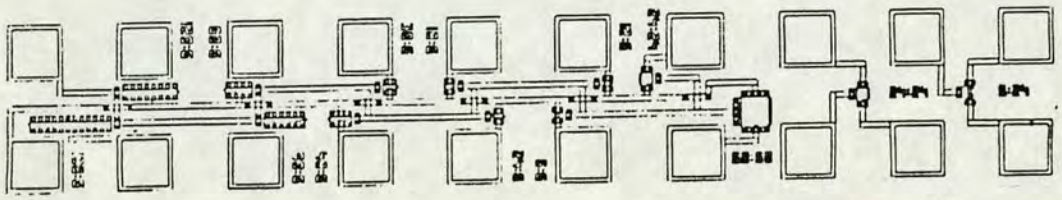


Figure 4. Module used to examine the performance of pass transistors. It contains two test transistors and twelve pass transistors.

simulations were taken into account and two test chips designed to evaluate the performance of the switching transistors. These both contained a number of different measurement configurations, with a range of pass and test transistor geometries. For example, the configuration given in figure 4 allows two test transistors with different geometries to be accessed using one of the twelve pass transistors, all of which have different dimensions. The layout has been designed so that the test transistor characteristics can also be directly measured to allow the switching performance of the pass transistors to be evaluated.

3. MEASUREMENTS

The simplest design that includes both current forcing and voltage sensing pass transistors is shown in figure 5. It will be used in the following measurements to highlight the problems which need to be considered. Figure 6 shows the characteristics of a transistor measured using pass transistors with

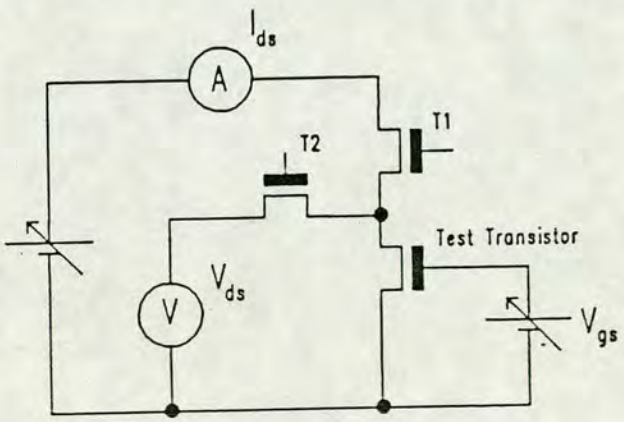


Figure 5. Circuit for measuring transistor characteristics using only two pass transistors.

different dimensions and compares them with those made directly on the test transistor. It can be observed that the transistor characteristics in the linear region are less sensitive to the dimensions of the pass transistors since $T1$ does not limit the current.

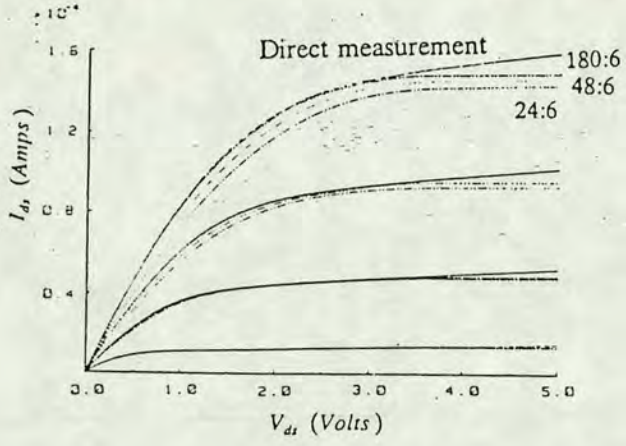


Figure 6. The effect of different sized pass transistors (T1) on the measured I_{ds}: V_{ds} characteristics for the test transistor, compared with the direct measurements.

However, in the saturated region this is not the case and a larger pass transistor helps to obtain a better representation of the device under test. Increasing the size of the pass transistors *ad infinitum* is not a practical solution to the measurement. The current through the test device is limited because V_{g1} of the pass transistor never reaches $5V$ because there will always be a voltage drop across the transistor being measured. Figure 7 shows how the characteristics obtained with higher gate voltages on the pass transistor overcome this problem with the measurements approaching the true characteristics as V_{g1} is increased.

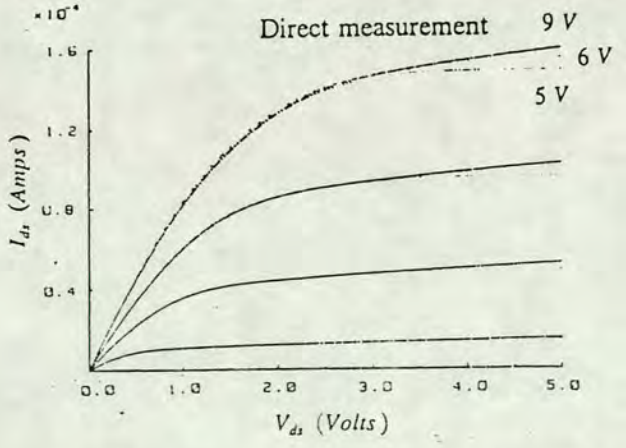


Figure 7. The effect of increasing the gate voltage of the pass transistor(T1) on the measured I_{ds}: V_{ds} characteristics for the test transistor, compared with the direct measurements.

4. SPICE MEASUREMENTS

One very sensitive test of the accuracy of the measurements is to extract SPICE parameters from measurements made through the pass transistors and then compare them with those obtained directly from the transistor terminals. PARAMEX [3] was used for these extractions and derives SPICE 2 level 3 parameters sequentially without recourse to any numerical optimisation. As a result all the extracted parameters have physical significance and can consequently be used for process control.

Table 1 compares the individual SPICE parameters extracted from direct measurements on the test transistor and those made through a pass transistor when its gate voltage was set at $9V$. The errors in the characteristics simulated using SPICE parameters derived from measurements via pass transistors compare very favourably with those obtained when the parameters are extracted from measurements made in the normal manner. This is illustrated in table 2 where the SPICE parameters have been extracted from measurements performed for different values of V_{g1} on transistor $T1$.

SPICE parameters	Measured at the transistor terminals	Measured through the pass transistor (120 x 6 μm V_g = 9V)
t_{ox} (m)	8.5×10^{-8}	8.5×10^{-8}
X_j (m)	1.0×10^{-6}	1.0×10^{-6}
N_{fs} (m^{-2})	1.0×10^{15}	2.9×10^{15}
V_{t0} (V)	1.03	1.06
γ ($\sqrt{V}$)	0.65	0.62
L_{del} (m)	1.35×10^{-6}	1.35×10^{-6}
ΔW (m)	1.46×10^{-6}	1.47×10^{-6}
μ_o ($m^2V^{-1}s^{-1}$)	0.085	0.087
θ (V^{-1})	0.051	0.067
V_{max} (ms^{-1})	4.28×10^5	5.69×10^5
η	0.159	0.134
δ	0.367	0.329
κ	0.402	0.495

Table 1. SPICE parameters extracted from direct measurements on the test transistor compared with those using measurements via the pass transistors.

V_{gs}	Average % rms error with the measured characteristic				
	Terminal measurement	Pass transistor gate voltage			
		5	6	8	9
2.0	11.4	19.7	18.5	16.2	16.3
3.0	6.3	7.2	8.6	7.2	7.2
4.0	2.5	3.0	4.1	3.0	3.0
5.0	0.6	1.3	2.3	1.4	1.3

Table 2. Rms error for simulated characteristics using SPICE parameters extracted from conventional measurements and via the pass transistors for different values of V_{gs}.

Figure 8 shows the variation of κ as a function of gate voltage on the pass transistor. This parameter has been selected since it is the SPICE parameter which characterises the slope of the $V_{ds} : I_{ds}$ curve in the saturation region. From figure 7 it would be expected that κ would increase rapidly between 5V and 6V and, as the gate voltage is further increased would, approach the value extracted from direct measurement on the transistor. This is the case in figure 8 with the small overshoot being explained by variations in other parameters which offset the slightly increased value of κ.

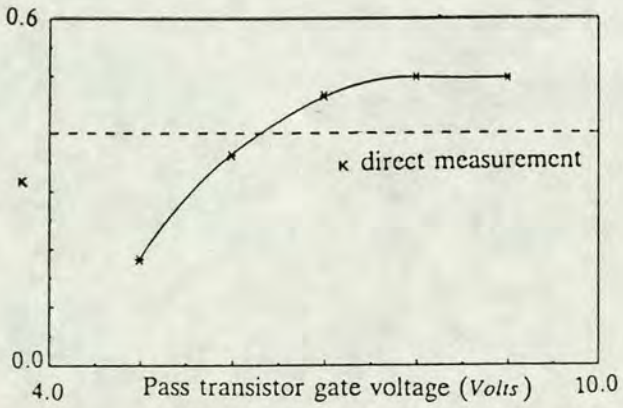


Figure 8. The effect of increasing the gate voltage of the pass transistor(T1) on the measured κ of the test transistor. The dotted line indictes the κ value obtained by direct measurements.

5. CONCLUSIONS

The results which have been presented illustrate that it is feasible to implement a switching matrix on-chip which can be used to measure transistor characteristics. It has been demonstrated that SPICE parameters can be extracted with an accuracy comparable to those derived using conventional techniques. This opens up the possibility of process control chips being measured using equipment with no switching matrix; the individual devices being addressed through pass transistors. With fewer pads required, these test chips can be designed to occupy reduced.

ACKNOWLEDGEMENTS

The authors would like to acknowledge the EMF staff who were involved in the fabrication of the wafers and Dr H Coltman of GEC for useful discussions. D Ward would also like to acknowledge financial support from GEC.

REFERENCES

1. A.J. Walton, J.M. Robertson, R. Holwill, M.B. Moore, Electronics Letters, Vol 21, No 4, pp 127-128, February 1985.
2. A. Vladimirescu, S Liu, "The Simulation of MOS Integrated Circuits Using SPICE2", Memorandum No. UCB/ERL M80/7, University of California, Berkeley, Feb 1980.
3. A. Gribben, J.M. Robertson, A.J. Walton, Semicon, pp 186-202, Birmingham, Sept 86.

A Novel Approach for an Electrical Vernier to Measure Mask Misalignment

A.J. Walton, D. Ward, J.M Robertson, R.J. Holwill

Edinburgh Microfabrication Facility,
Department of Electrical Engineering,
Kings Buildings, University of Edinburgh,
Edinburgh, EH9 3JL, UK.

Summary

A novel interconnect scheme is presented which reduces the number of pads required by electrical verniers to measure mask misalignment. It makes the use of a shift register no longer necessary to keep the pad count to a reasonable number and the process is only required to support the fabrication of diodes. The vernier can be measured using any test equipment which can test for continuity.

Introduction

The misalignment that occurs between layers during the IC fabrication process must be allowed for in the design rules and this ultimately reduces the packing density. As a consequence it is important that the misalignments can be monitored in a routine manner. The use of optical verniers has long been commonplace [1] but their measurement is time consuming, tedious and error prone. Another approach is to use electrical structures that are based on the measurement of voltages between taps [2,3]. These devices all assume a uniform sheet resistivity and with misalignment tolerance being reduced as circuits become smaller so the accuracy of the voltmeter become more of a limiting factor.

The Electrical Vernier

One method of overcoming the above problem is to use an electrical vernier [4-7] which operates on the principle illustrated in figure 1. Connection between the teeth is electrically tested and the degree of misalignment extracted. This has the advantage that its resolution is only limited by the lithography and etch of the process. One other advantage of this structure is that information on the combined over-etch between two layers can also be extracted from the contact pattern. This pattern also provides a check on data integrity since the number of teeth which are not connected should always be an odd number and always adjacent to one another. An even number of open circuits or the presence of outliers indicate that there are potential problems with the integrety of the data. To individually test the connection between each tooth of the vernier obviously requires a large number pads. The number can be reduced by using

a parallel load shift register to clock out the measurements (see figure 2). However, this has the disadvantage that a fully functional process is required and the test structure designer may not have the necessary skills required for the layout. The test structure proposed in this paper overcomes the limitations of all the above designs.

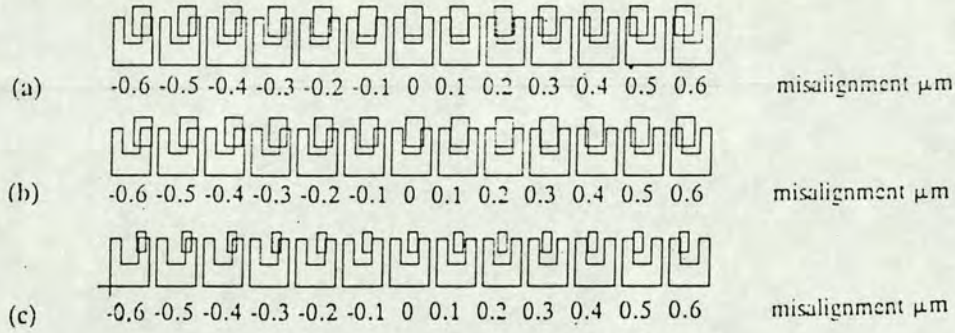


Figure 1. An electrical vernier which compensates for over-etch. (a) No over-etch with zero misalignment. (b) No over-etch with +0.2μm misalignment. (c) 0.3 over-etch with +0.2μm misalignment.

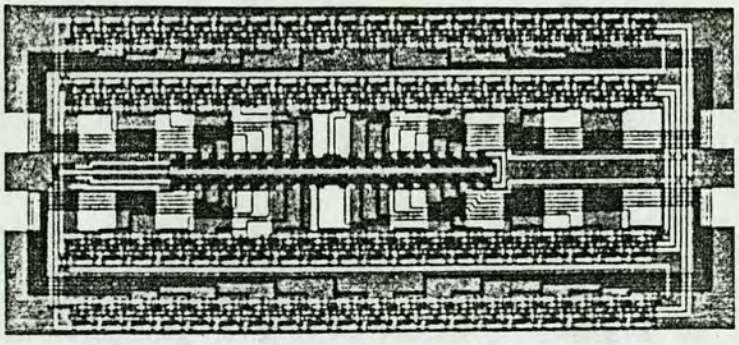


Figure 2. Electrical vernier that uses a shift register for the measurement.

The Diode Vernier

In this new diode vernier design the pads are connected to a number of teeth on the vernier in such a way to ensure that the information can be decoded in a very simple manner. Figure 3 shows a schematic illustrating the interconnect matrix and a typical contact pattern between the vernier teeth. Contact between the teeth is tested by sequentially forcing a voltage between every combination of group and access pads. The diodes which are in series with the bottom set of teeth are required to prevent current flowing via other parallel paths which may exist if the teeth are connected in a certain pattern. Figure 4 shows the layout of a diode vernier for measuring metal to

polysilicon misalignment. This design performs the same function as the shift register vernier shown in figure 2 and the reduced area required can be observed since the pad size in both cases is the same. Table 1 gives the contact matrix between the pads for the vernier of figure 3 and from this it is possible to easily decode the position of the teeth that do not contact each other. Table 2 summarises the capabilities of the test structure and its superiority in terms of pad count to that where every tooth is connected to an individual pad is self evident. It can be observed that the pad to teeth ratio improves as the number of teeth increases. It is consequently advantageous to combine the x and y verniers on one interconnect matrix.

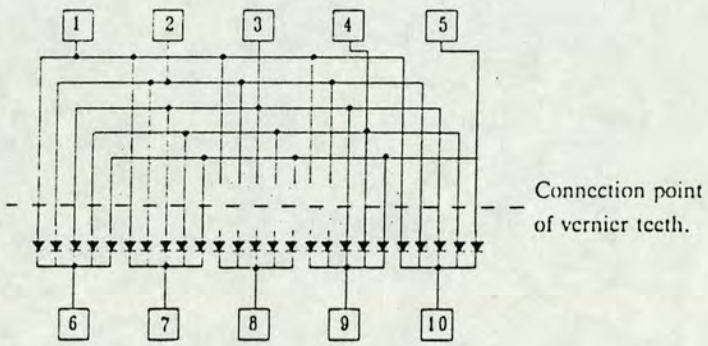


Figure 3. Schematic diagram of the diode vernier showing the pad connection.

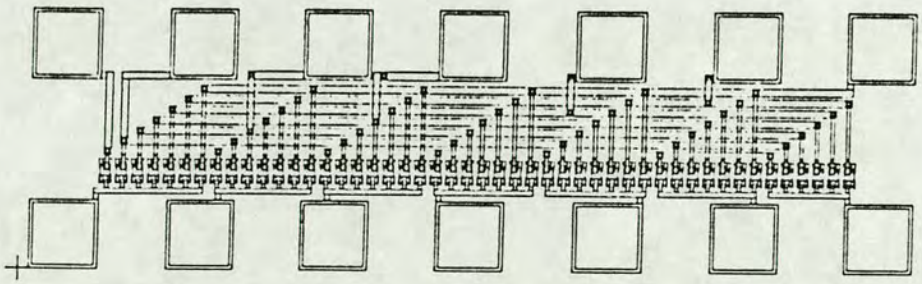


Figure 4. Layout of a diode vernier in nMOS technology.

Access Pads	Group Pads				
	6	7	8	9	10
1	1	1	0	0	1
2	1	1	0	0	1
3	1	1	0	1	1
4	1	1	0	1	1
5	1	1	0	1	1

Table 1. The contact matrix for the vernier schematically represented in figure 3.

No. of teeth per layer		16	25	36	49
No. of pads for diode vernier		8	10	12	14
No. of pads for standard vernier		17	26	37	50
Maximum range of misalignment and overetch	0.1μm resolution	1.6μm	2.5μm	3.6μm	4.9μm
	0.05μm resolution	0.8μm	1.25μm	1.8μm	2.45μm

Table 2. Comparison of the standard and diode vernier specifications.

Conclusions

In conclusion a test structure has been proposed which can measure misalignment with a resolution of that commensurate with that of the lithography and etch capabilities of the process. It has all the advantages of the vernier compared with the analogue structures but since it does not require a shift register its operation and measurement are much simpler. As a result it has more in common with other test structures and can be measured on an unmodified parametric test system. Furthermore, since the measurement is digital in nature, the accuracy will not be compromised if pads are commoned with those of other test structures to reduce the pad count still further.

References

1. W.C. Schneider, "Testing the Mann Type 4800DSW Wafer Stepper", SPIE Developments in Semiconductor Microlithography IV, vol 174, 1979, pp 6-14.
2. D.S. Perloff, "A Four-Point Electrical Measurement Technique for Characterizing Mask Superposition Errors on Semiconductor Wafers", IEEE J Solid-State Circuits, vol sc-13, no 4, Aug 1978, pp 436-444.
3. C.M. Cork, "Off-line Photolithographic Parameter Extraction using Electrical Test structures", Proc ICMTS, Edinburgh, 13-14th March 1989, pp 7-14.
4. B.M.M Henderson, A.M. Gundlach, A.J. Walton, "Integrated Test Structure Which uses a Vernier to Electrically Measure Mask Misalignment", Electronics Letters, vol 19, no 21, 13th Oct 1983, pp 868-869.
5. A.J. Walton, W.R. Gammie, R.J. Holwill, B.M.M. Henderson, "Digital Measurement of Polysilicon to Diffusion Misalignment for a Silicon gate MOS process", Electronics Letters, vol 20, no 23, 8th Nov 1984, pp 951-952.
6. B.M.M Henderson, A.J. Walton, "A Complete Vernier Tool for the Measurement of Mask Misalignment", IEEE VLSI Workshop on Test Structures, Long Beach, USA, 17-18th Feb 1986, pp 34-50.
7. R. Yamaguchi, K. Komatsu, S. Moriya, K. Harada, "Integrated Electrical Vernier to Measure Registration Accuracy", IEEE Electron Device Letters, vol EDL-7, pp 463-464.

pinch-off voltage of 2·5 V. At $V_{gs} = 0$ V and $V_{ds} = 3$ V, the transconductance is 140 mS/mm. The transconductance as a function of the gate voltage at $V_{ds} = 1·8$ V is shown in Fig. 4. The source resistance is approximately 45 Ω which yields an intrinsic transconductance of 190 mS/mm. The DC output conductance is 30 mS/mm. Based on measured *S*-parameters of these initial devices, the value of f_T was determined to be 11 GHz and is expected to improve with further optimisation of the device processing.

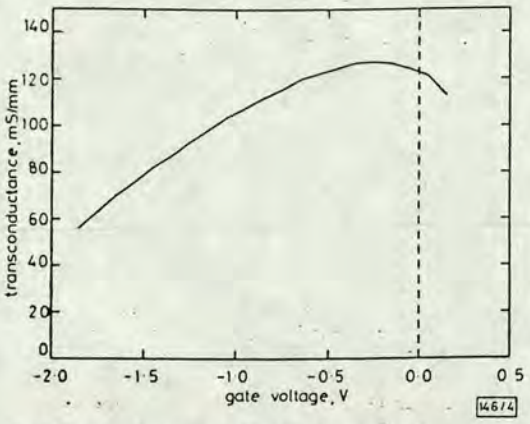


Fig. 4 *Transconductance as a function of gate voltage*
$V_{ds} = 1·8$ V

Acknowledgment: This work was supported by the US Office of Naval Technology. The authors would like to thank A. Fathimulla, D. Shupe, and K. J. Sleger for helpful discussions and J. Mittereder for technical assistance.

J. B. BOOS
S. C. BINARI
Naval Research Laboratory
Washington, DC 20375-5000, USA

W. KRUPPA
SFA, Inc., Landover, MD 20785, USA

H. HIER
Allied-Signal Aerospace Technology Centre
Columbia, MD 21045, USA

9th April 1990

References

1 MISHRA, U. K., JENSEN, J. F., BROWN, A. S., THOMPSON, M. A., JELLOIAN, L. M., and BEAUBIEN, R. S.: 'Ultra-high-speed digital circuit performance in 0·2-μm gate-length AlInAs/GaInAs HEMT technology', *IEEE Electron Device Lett.*, 1988, **EDL-9**, pp. 482–484

2 HO, P., CHAO, P. C., DUH, K. H. G., JABRA, A. A., BALLINGALL, J. M., and SMITH, P. M.: 'Extremely high gain, low noiose InAlAs/InGaAs HEMTs grown by molecular beam epitaxy'. IEEE IEDM Tech. Dig., 1988, pp. 184–186

3 HONG, W. P., CHANG, G.-K., BHAT, R., GIMLETT, J. L., NGUYEN, C. K., SASAKI, G., and KOZA, M.: 'Monolithically integrated $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ MSM-HEMT receiver grown by OMCVD on patterned InP substrates'. IEEE IEDM Tech. Dig., 1989, pp. 733–736

4 BROWN, A. S., CHOU, C. S., DELANEY, M. J., HOOPER, C. E., JENSEN, J. F., LARSON, L. E., MISHRA, U. K., NGUYEN, L. D., and THOMPSON, M. S.: 'Low-temperature buffer AlInAs/GaInAs on InP HEMT technology for ultra-high-speed integrated circuits'. Tech. Dig. GaAs IC Symposium, 1989, pp. 143–146

5 KRUPPA, W., and BOOS, J. B.: 'Microwave performance of ion-implanted InP JFETs', *IEEE Trans.*, 1988, **ED-35**, pp. 2279–2287

6 WANG, K.-W., CHENG, C.-L., LONG, J., and MITCHAM, D.: 'High-performance InGaAs junction field effect transistor with P/Be co-implanted gate', *IEEE Electron Device Lett.*, 1988, **EDL-9**, pp. 205–207

7 SUZUKI, Y., HIDA, H., TOYOSHIMA, H., and OHATA, K.: 'High-speed ring oscillators using planar p^+-gate *n*-AlGaAs/GaAs 2DEG FETs', *Electron. Lett.*, 1986, **22**, pp. 672–673

8 FATHIMULLA, A., ABRAHAMS, J., HIER, H., LOUGHRAN, T., and HEMPFLING, E.: 'High current planar-doped InGaAs/InAlAs HEMTs'. Int. Symp. GaAs and Related Compounds, Inst. Phys. Conf. Ser., 1988, **96**, pp. 455–457

9 BOOS, J. B., WENG, T. H., BINARI, S. C., KELNER, G., and HENRY, R. L.: 'InP JFETs by shallow Zn diffusion'. IEEE IEDM Tech. Dig., 1983, pp. 625–627

10 FATHIMULLA, A., ABRAHAMS, J., LOUGHRAN, T., and HIER, H.: 'High-performance InAlAs/InGaAs HEMT's and MESFET's', *IEEE Electron Device Lett.*, 1988, EDL-9, pp. 328–330

PASSIVE ELECTRICAL VERNIER FOR MEASURING MASK MISALIGNMENT

Indexing term: Measurement

A passive electrical vernier for the measurement of the misalignment between the layers of integrated circuits is presented. This three layer structure has the same simplicity of processing as analogue structures along with the advantages of digital measurement which make it an attractive alternative for measuring the mask misalignment between layers.

Introduction: The misalignment between the different layers of integrated circuits is one of the limiting factors as geometries are reduced. It is consequently important that this parameter can be measured so that the performance of the lithography process can be monitored and optimised.

The electrical vernier measures misalignment by checking for continuity between two sets of teeth which have a slightly different pitch. The difference in the pitch sets the resolution of the structure and for a detailed discussion of the layout and design of the teeth the reader is referred to Reference 1. The major problem when electrically measuring misalignment with a simple passive vernier, is that the continuity between a large number of teeth needs to be monitored. This results in a high number of pads with the area occupied by them being somewhat excessive. One solution which significantly reduces the pad count is the use of a parallel load shift register.[1–4] The problem with this approach is that a fully functional process is required and, if a dynamic design is used, a functional test system must be used for the measurement.

The passive vernier: The structure proposed in this letter is based on the diode vernier.[5] The diode vernier has a significant advantage over the shift register design as the only active components are diodes which are required to prevent current flowing through parallel paths. Its main disadvantage is that it still requires a full process. The passive vernier is shown in Fig. 1*a* with the central portion where the teeth are open circuit being shown in more detail in Fig. 1*b*. This structure only requires a three layer process which makes it comparable with analogue structures[6,7] and because the instrumentation only needs to test for continuity it can be of relatively low cost.

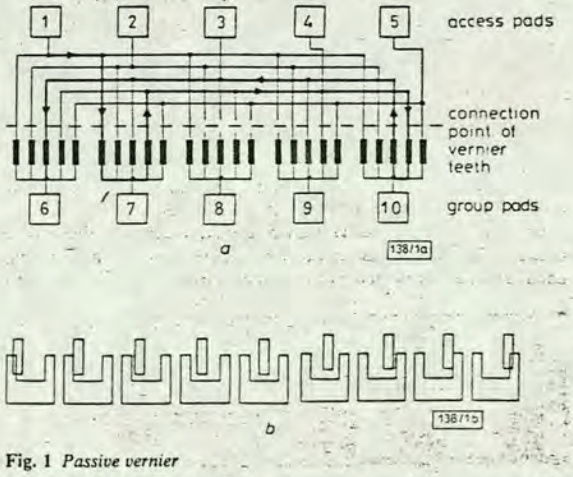


Fig. 1 *Passive vernier*
a Schematic representation
b Layout of teeth

The measurement procedure requires some consideration to ensure that the current flowing through parallel paths does not distort the measurement. The structure has two types of pads. The group pads (6–10 in Fig. 1) connect together groups of teeth, and individual teeth in each group can then be tested for continuity using the access pads (1–5 in Fig. 1). If continuity is tested by forcing a voltage across pads 1 and 6 of Fig. 1, then a current would flow through the tooth set that directly connects pad 1 and 6. If these teeth were not connected current would flow through other routes to give an erroneous indication of contact. One of many such potential paths is shown in Fig. 1. The purpose of the measurement is to detect continuity between pairs of teeth so there is no prior knowledge of the number and route of these parallel current paths. This makes it very difficult to design a robust algorithm to be sure of extracting the correct contact pattern.

The approach suggested is to suppress all the parasitic current paths. This can be achieved by earthing all the group pads as indicated in Fig. 2*a*. Current will then only flow through the connected sets of vernier teeth that are directly attached to the pad into which current is being forced. An example of this is illustrated in Fig. 2*a* where the ammeter is used to detect contact between the specified teeth. Since all the group pads are at the same potential there should be no parasitic current flow between them. In practice a small current does flow because of the finite resistance of the ammeter and the equivalent circuit is shown in Fig. 2*b*. Provided that the resistance of the ammeter R_A is very much less than the resistance of the combination of parallel paths R_P then there is a very high level of discrimination between the open and short circuit sets of teeth. The connection between every set of teeth can be simply checked by forcing a voltage across all combinations of access and group pads while ensuring that all groups pads which are not directly involved in the measurements are earthed.

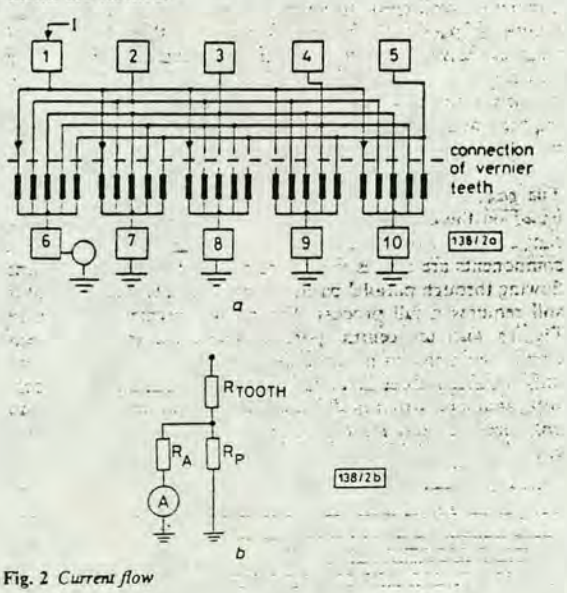


Fig. 2 *Current flow*
a Measurement
b Equivalent circuit

For a set of 100 Ω resistors, representing interconnected resistance between the teeth of the vernier as shown in Fig. 1, a nominal value of 100 Ω was obtained whenever there was contact. The worst case condition, where most parallel paths exist, is when only one path is open circuit. In this case the resistance was measured at 27 kΩ. This provides an excellent degree of discrimination in the test for contact between teeth.

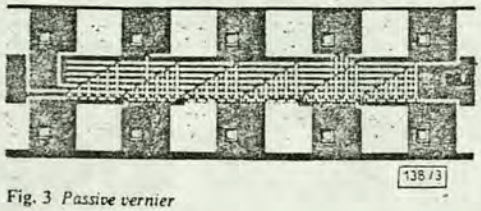


Fig. 3 *Passive vernier*

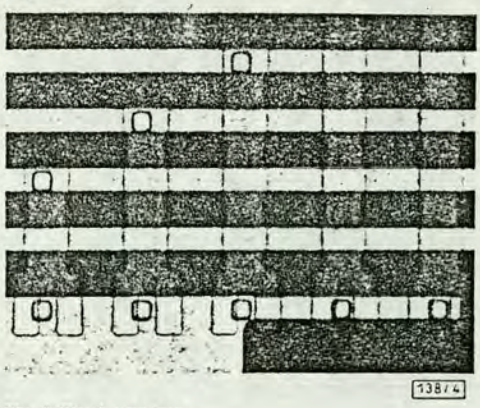


Fig. 4 *Tooth structure*

Fig. 3 shows the layout of a single axis passive vernier with 36 teeth. The layout is considerably less complicated than that of the shift register design. The structure is designed to measure the misalignment between the polysilicon and the contacts and Fig. 4 shows a close up of a number of teeth. The difference in pitch between the teeth is 0·1 μm and it can be observed that a more robust contact is made as the contact and tooth overlap is increased. Fig. 5 shows a histogram of the measured misalignments in the x direction for a wafer that was blind stepped on a 10X machine. The mean misalignment was in agreement with that measured optically.

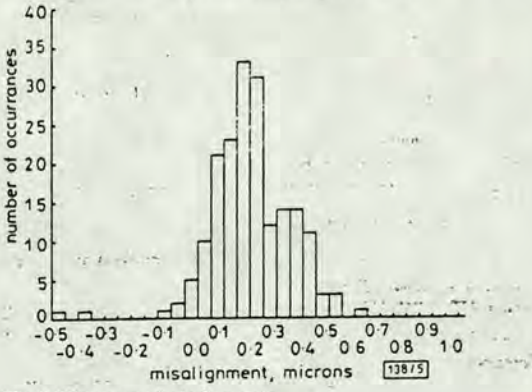


Fig. 5 *Histogram of misalignments*

The advantages of the passive vernier in terms of pad count compared with the more conventional approach to continuity testing are summarised in Tables 1 and 2. It can be seen that not only is the pad count significantly reduced but that, as the number of teeth increases, the pad to tooth ratio reduces.

Conclusions: The passive vernier has been presented in conjunction with a measurement strategy which significantly reduces the number of pads required. Both the design and measurement is very much simplified when compared with the shift register approach because only continuity needs to be tested. This gives it an advantage over the equivalent ana-

Table 1 COMPARISON OF THE NUMBER OF PADS REQUIRED FOR TWO AXES STANDARD AND PASSIVE VERNIERS FOR MEASURING MASK MISALIGNMENT

Number of teeth in x and y axis vernier	Number of pads		Pad-tooth ratio	
	Standard	Passive	Standard	Passive
36	37	12	1·03	0·333
64	65	16	1·02	0·250
100	101	20	1·01	0·200

logue structures which require high accuracy instrumentation. The resolution accuracy of the passive vernier is totally defined by the lithographic process. As a consequence this structure will scale with deep submicron technologies. These factors make the passive vernier an attractive alternative for incorporation on process control chips when mask misalignment is to be monitored.

Table 2 RESOLUTION AND RANGE OF A SINGLE AXIS PASSIVE VERNIER AS A FUNCTION OF THE PAD COUNT

Number of pads*	Number of teeth	Maximum range of misalignment and overetch	
		0·1 μm resolution	0·05 μm resolution
		μm	μm
8	16	1·6	0·80
10	25	2·5	1·25
12	36	3·6	1·80
14	49	4·9	2·45
16	64	6·4	3·20
18	81	8·1	4·05
20	100	10·0	5·00

Acknowledgment: The authors would like to acknowledge the support of SERC under grant number GR/F 30499.

A. J. WALTON
W. GAMMIE
M. FALLON
D. WARD
R. J. HOLWILL

Edinburgh Microfabrication Facility
Department of Electrical Engineering
Kings Buildings, University of Edinburgh
Edinburgh EH9 3JL, United Kingdom

9th April 1990

References

1 HENDERSON, B. M. M., GUNDLACH, A. M., and WALTON, A. J.: 'Integrated test structure which uses a vernier to electrically measure mask misalignment', *Electron. Lett.*, 1983, **19**, pp. 868–869
2 WALTON, A. J., GAMMIE, W. R., and HOLWILL, R. J.: 'Digital measurement of polysilicon to diffusion misalignment for a silicon gate MOS process', *Electron. Lett.*, 1984, **20**, pp. 951–952
3 HENDERSON, B. M. M., and WALTON, A. J.: 'A complete vernier tool for the measurement of mask misalignment'. IEEE VLSI Workshop on Test Structures, Long Beach, USA, Feb. 1986, pp. 34–49
4 YAMAGUCHI, R., KOMATSU, K., MORIYA, S., and HARADA, K.: 'Integrated electrical vernier to measure registration accuracy', *IEEE Electron Device Lett.*, 1986, **EDL-7**, pp. 463–464
5 WALTON, A. J., WARD, D., ROBERTSON, J. M., and HOLWILL, R. J.: 'A novel approach for an electrical vernier to measure mask misalignment'. ESSDERC 89, pp. 950–953
6 PERLOFF, D. S.: 'A four-point electrical measurement technique for characterizing mask superposition errors on semiconductor wafers', *IEEE J. Solid-State Circuits*, 1978, **SC-13**, pp. 436–444
7 CORK, C. M': 'Off-line photolithographic parameter extraction using electrical test structures'. Proc. ICMTS, Edinburgh, 1989, pp. 7–14

SIMPLE METHOD FOR CALCULATING OPTIMUM CUT OF PIEZOELECTRIC MATERIAL WITH SMALL BAW GENERATION BY IDTS

Indexing terms: Ultrasonics, Acoustic waves, Piezoelectric devices and materials

A method is presented for calculating the optimum cut of piezoelectric material with small bulk acoustic wave (BAW) generation by interdigital transducers (IDTs). The theoretical results for Y-rotated cut X-propagation and Y-rotated cut X-90° propagation $LiNbO_3$ are given. A new cut of $LiNbO_3$ has been found which has smaller BAW generation than Y-128°X $LiNbO_3$. The experimental results agree with the theoretical prediction.

It is important that the spurious signals of BAWs generated by IDTs must be small for high quality surface acoustic wave (SAW) devices. Much works have been done in this respect.[1–4] A simple method presented here can be used for predicting the cut of piezoelectric material with minimum BAW generation.

Using the Christoffel wave equations and boundary conditions, the effective surface permittivity, ε_{eff}, can be obtained as the function of s, the component of BAW slowness in the propagation direction of the SAW.[1] $\varepsilon_{eff}(s)$ is defined as

$$\varepsilon_{eff} = \frac{\sigma(k)}{|k|\phi(k)}$$

where σ and ϕ are charge density and electric potential of surface, respectively. $k(=\omega s)$ is the component of wave vector in the direction of the SAW. Let the current density $i(k)$ and the admittance $Y(k)$ be

$$i(k) = \frac{d\sigma(k)}{dt} = j\omega\sigma(k)$$

$$Y(k) = \frac{i(k)}{\phi(k)} = j\omega|k|\varepsilon_{eff}$$

so

$$G(k) = -\omega|k| \text{ Im } \varepsilon_{eff}$$

that is to say, the total strength of the BAWs generated by the IDTs is related to the imaginary part of effective surface permittivity as the slowness is smaller than the surface wave. The optimum cut of the piezoelectric material with small BAW generation can be found by searching for the minimum Im $\varepsilon_{eff}(s)$. This is very simple because the $\varepsilon_{eff}(s)$ may be obtained while searching for the velocity of SAW.

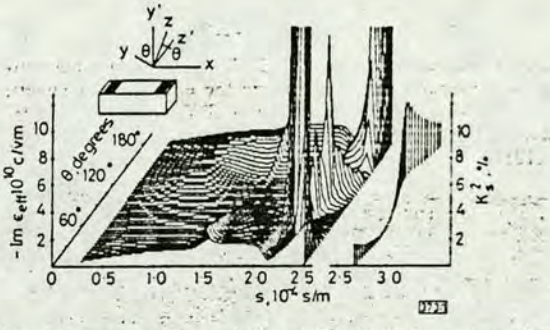


Fig. 1 *Im ε_{eff} against s and K_s^2 and K_s^2 of $LiNbO_3$ substrate of Y-rotated cut X-propagation*

As an example, we have calculated Im $\varepsilon_{eff}(s)$ of a Y-rotated cut X-propagation $LiNbO_3$ as shown in Fig. 1 and the Im $\varepsilon_{eff}(s)$ of a Y-rotated cut X-90° propagation $LiNbO_3$ as shown in Fig. 2. θ is the rotated cut angle. The electromechanical coupling coefficient K_s^2 of the SAW is also calculated and shown in the right side of Figs. 1 and 2. The crystal constants used in evaluation are obtained from the work of

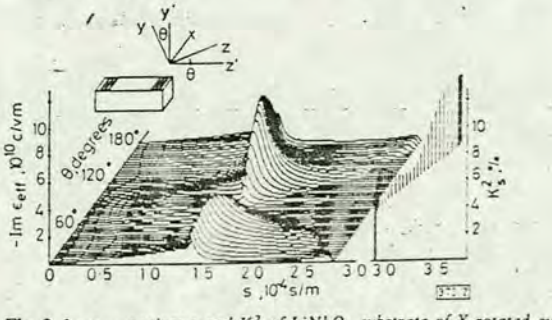


Fig. 2 *Im ε_{eff} against s and K_s^2 of $LiNbO_3$ substrate of Y-rotated cut X-90° propagation*