Techniques to Improve the Optical Quality of Liquid Crystal over Silicon Spatial Light Modulators

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To Mum, Dad and Mary

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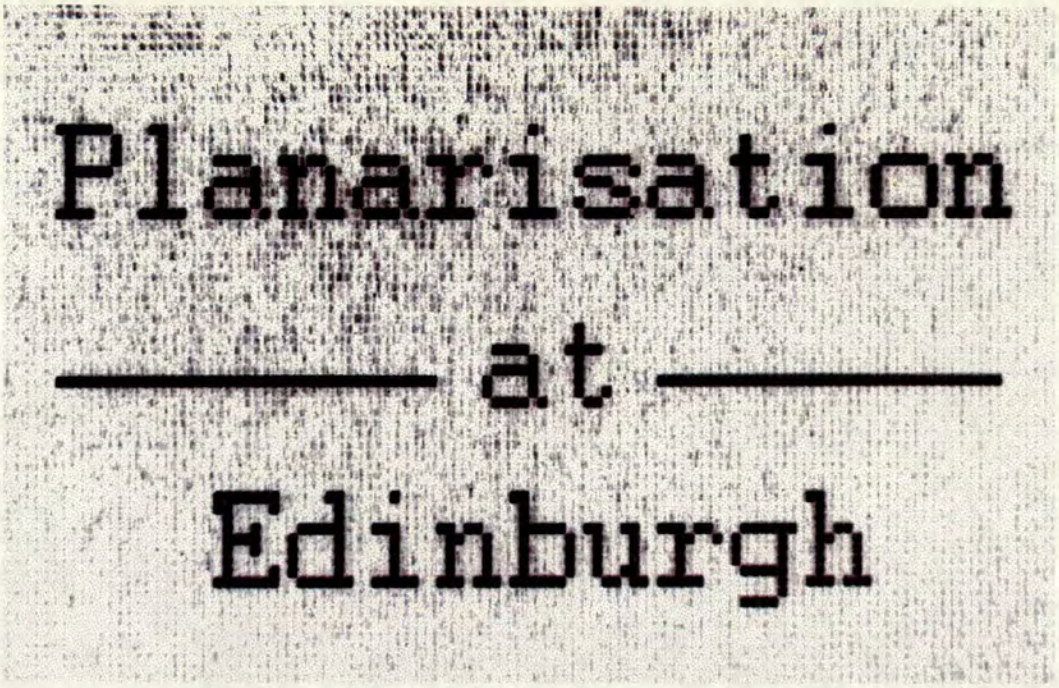

Images displayed on FLCoS SLM's
Courtesy of A. O'Hara and I. Rankin, respectively.

Abstract

Systems using Ferroelectric (F) Liquid Crystal over Silicon (LCoS) Spatial Light Modulators (SLMs) have been limited, in the past, by the poor optical performance of the devices. The high degree of backplane flatness and hence LC layer thickness uniformity required have been very difficult to achieve due to stresses induced in the silicon wafer as a consequence of CMOS processing. Mirror quality and LC alignment are also major factors in determining the (F)LCoS SLM optical efficiency and contrast ratio.

A process of forming "thin" high-quality mirrors was developed, using an intermediate metal chemical mechanical polishing process (CMP). An associated process was also developed in which the thin mirrors were fabricated flush with the surrounding oxide, using a novel interpixel gap fill process (flat to 2.5nm) which allowed a major improvement to be made in the liquid crystal flow front, during cell filling.

We have successfully demonstrated a technique for reducing the backplane warpage from 3.0λ down to λ/8, over a die, thus improving the LC layer thickness uniformity.

The robust silicon dioxide spacers used in the die flattening experiments, above, were fully characterized and the deposition and patterning process optimized to consistently provide spacer layer thickness uniformities of <1% over a 75mm wafer.

Issues relating to the transparent ITO layer were addressed. We have shown that the surface roughness of the granular "in-house" deposited ITO can be reduced by ~40% (on a sub-micrometer scale) using a slight variant of the oxide CMP process. The optical performance of LC devices was also found to be improved by optimizing the ITO and SiO layer thickness. Reflections from the ITO coated glass have been reduced by approximately 10% by optimizing the ITO layer thickness for a particular wavelength.

In this study, I have sucessfully demonstrated processes which will allow the fabrication and construction of higher quality LCoS SLM's than have previously been produced.

Contents

Abbreviations

AFM	Atomic Force Microscope
AM	Active Matrix
AO	Applied Optics
APCVD	Atmospheric Chemical Vapor Deposition
AR	Anti Reflectance
ASTM	American Society for Testing and Materials
BCB	Benzocyclobutene
BOE	Buffer Oxide Etch
BPSG	Borophophosilicate Glass
CMOS	Complementary Metal Oxide Semiconductor
CMP	Chemical Mechanical Polishing/Planarization
CR	Contrast Ratio
CVD	Chemical Vapor Deposition
dc	Direct Current
DI	De-ionized
DRAM	Dynamic Random Access Memory
EASLM	Electrically Addressed Spatial Light Modulator
ECR	Electron Cyclotron Resonance
EMF	Edinburgh Microfabrication Facility
FLC	Ferroelectric Liquid Crystal
FPD	Flat Panel Display
HMDS	Hexamethyldisilazane
HPSLM	High Performance Spatial Light Modulator
ITO	Indium Tin Oxide
JTC	Joint Transform Correlator
LC	Liquid Crystal
LCoS	Liquid Crystal over Silicon
LPCVD	Low Pressure Chemical Vapor Deposition
MAD	Medium Angle Deposition
MINDIS	Miniature INformation DIsplay Systems
M/S	Mark to Space ratio
NLC	Nematic Liquid Crystal
nMOS	n-channel Metal Oxide Semiconductor
OASLM	Optically Addressed Spatial Light Modulator
PACMAN	PACkaging and MANufacturability of microdisplays
PECVD	Plasma Enhanced Chemical Vapor Deposition
PGA	Pin Grid Array
PR	Photoresist
PSG	Phosphosilicate Glass
PVA	Poly(vinyl alcohol)
PVD	Physical Vapor Deposition
rf	Radio Frequency
RIE	Reactive Ion Etch
rms	root mean square
SAD	Small Angle Deposition
SBWP	Space Bandwidth Product
sccm	standard cubic centimetres per minute
SCIOS	Scottish Collaborative Initiative in Optoelectronic Sciences
SEED	Self-Electro-optic Effect Device
SEM	Scanning Electron Microscope
SHD	Step Height Distribution

SIFT	Self-aligned Insulator Filled Trench
SLIMDIS	Silicon LIquid crystal Miniature DIsplay System
SLM	Spatial Light Modulator
SmA	Smectic A
SmC*	Chiral Smectic C
SRAM	Static Random Access Memory
SSFLC	Surface Stabilaized Ferroelectric Liquid Crystal
STM	Scanning Tunneling Microscope
STN	Super Twisted Nematic
TN	Twisted Nematic
UV	Ultraviolet
VLSI	Very Large Scale Integration
XOR	Exclusive OR

Chapter 1.

Introduction to Liquid Crystals & Spatial Light Modulators.

1.1 Liquid crystals

It is well known that matter usually exists in one of three phases; solid, liquid or gas. Liquid crystals (LC), as their name suggests, are a less common phase in which the material is neither a solid or a liquid. They posess physical properties that are intermediate between conventional fluids and solids. The LC phase is also known as a mesophase. The molecules in all LC phases move about much like the molecules of a liquid, but as they do so they maintain some degree of orientational and, sometimes, positional order. As a result, there is anisotropy in the macroscopic mechanical, electrical, magnetic, and optical properties of the LC [Blinov, 1983]. A measure of the orientational order of a nematic LC (1.1.1) is given by the function $(3\cos^2\theta - 1)/2$ which is called the order parameter (S), where θ is the angle between the long molecular axis and the nematic director. An order parameter of 1 implies perfect orientational order, whereas the order parameter of an isotropic liquid is 0. There are essentially three variables which determine the phase which a liquid crystal material exhibits. LC materials in which the temperature (or pressure) determine the phase are classified as thermotropic LC. Where the concentration determines the phase of the material, the LC is classified as lyotropic. The remaining discussions will be on the former. The most common type of molecule that forms LC phases is a rod-shaped (calamitic) molecule. (*i.e.*, one molecular axis is much longer than the other two). In fact it is the interactions between the anisotropic molecules which promote the orientational (and positional) order in an otherwise fluid phase.

An electric or magnetic field causes the molecular director, of a LC, to change orientation The direction depends on whether the LC has a *positive* or *negative*

dielectic anisotropy (*i.e.,* whether the molecules try to line parallel or perpendicular to the electric field). Deformation of the liquid crystal structure with applied electric field strength is not gradual. At some threshold value of the field, the deformation begins and then gets greater as the field strength is increased. This transition from an undeformed to a deformed texture at a certain value of field is called the *Freedericksz transition* [Blinov, 1983].

1.1.1 Liquid crystal phases

At the present time thermotropic LCs are divided into three groups-nematic, chiral nematic (or cholesteric) and smectic, figure 1.1. Nematic LCs are characterized by long range orientational order, whereas smectic phases posses both long range orientational and positional ordering. There is still disorder within each layer. Many variants of the smectic phase exist; in some the molecules are tilted relative to the layers, figure 1.1(d), and in others there is additional ordering within the layers. The name Nematic comes from the Greek word for "thread". Chiral simply means "twisted" and Smectic, "soap like".

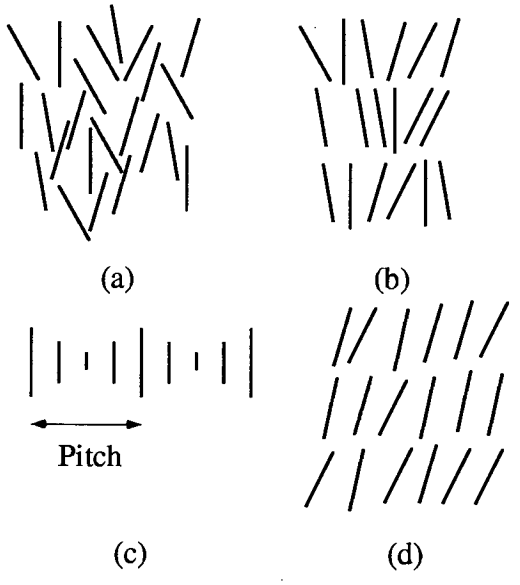

Figure 1.1 (a) Nematic, (b) smectic A, (c) chiral, and (d) tilted smectic phase.

The addition of a chiral component to the smectic C phase produces the chiral smectic C phase (SmC*), figure 1.2(a). This special phase differs from the previously mentioned phases in that it is ferroelectric[1], *i.e.*, it now exhibits a permanent polarization in the absence of an electric field. The director of the SmC* rotates in a cone in going from one smectic layer to the next. If the cell is thin enough, the interaction of the LC with the surfaces produces a texture in which there is no rotation of the director within the cell [Clark, 1983], known as surface-stabilized, shown in figure 1.2(b).

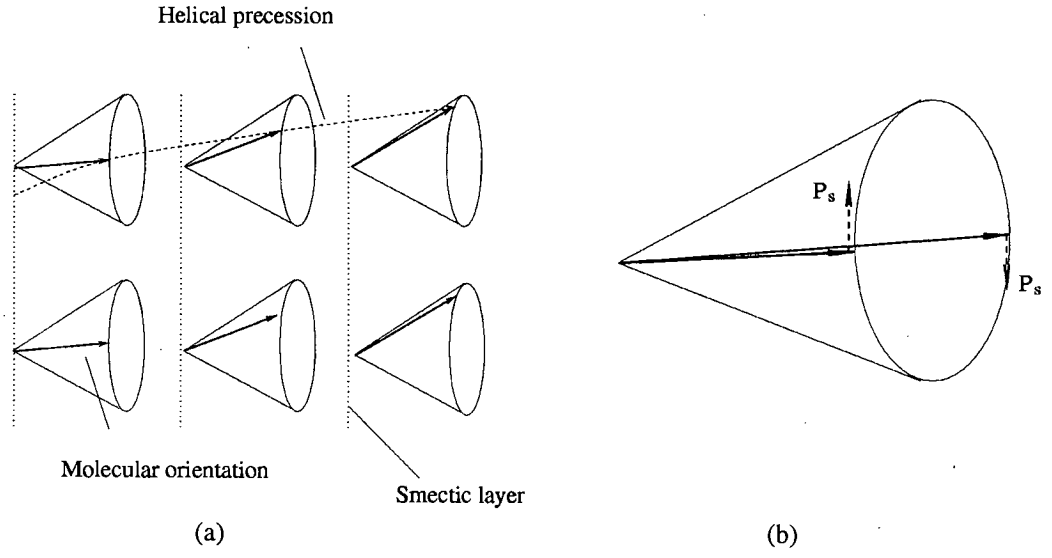

Figure 1.2 (a) Chiral SmC phase, (b) surface stabilized (SS) FLC director has two stable states.

Ferroelectric Liquid Crystals (FLCs) are allegedly susceptible to mechanical stress and thermal shock, poor contrast, ghost images and difficulty of alignment [Efron, 1995]. The director distortions in NLCs decay exponentially with distance from the boundary, but the smectic layer structure propagates defects more extensively. Consequently, the smectic layered structure is, in general, more difficult to align than NLC. Although FLCs suffer from the problems described above, they have the desirable properties of fast switching (10-100s of microseconds) and bistability.

[1] A new phase, only discovered in 1989, is the anti-ferroelectric phase [Ouchi, 1991]. This tri-stable phase differs from the ferroelectric phase in that its constituent molecules tilt in alternate directions from layer to layer, which produces a zero spontaneous polarization. This phase shows great potential in display devices as it offers better defined electric field thresholds and is less fragile than normal FLCs.

Direct alignment of the smectic phase on cooling from the isotropic phase is possible. However, the most uniform alignment is achieved through the alignment of the precursor long-pitched N*LC, which undergoes a SmA phase transition and finally SmC* transition with decreasing temperature.

1.1.2 Liquid crystal alignment

The liquid crystal orientation at the boundaries are very important as they determine the orientation of the liquid crystal molecules in the bulk. Depending on the combination of the surface preparation of the two bounding substrates, various orientations are possible. There are a wide range of LC molecular orientations; seven of the most common types being homeotropic, homogenous, tilt, hybrid, twist, planar, and focal conic. The mechanisms involved in liquid crystal alignment are discussed later.

LC aligning layers can be formed by various methods, summarized in table 1.1, the simplest of which is commonly known as Chatelain's method. This method involves mechnically rubbing the glass/electrode surface with a cotton cloth or paper [Chatelain, 1943]. The rubbing creates a microrelief in the surface in the form of ridges and troughs which promotes the orientation of the molecules along these formations. Alternatively, the surface preparation can be preceded by coating the substrate(s) with a suitable film before the unidirectional rubbing.

LC aligning method	Comments
Direct processing	The substrate is coated with a solution of an aligning agent, the solvent removed leaving a thin film of the aligning agent on the substrate surface [Zhu, 1994].
Substrate surface transformation	Rubbing, oblique evaporation, stamping [Lee, 1993], etched gratings in SiO, photoresist, metal *etc.*, [Newsome, 1998], [Smela, 1993].
Polymer matrix	Photopolymerization [Jain, 1984a&b]
Other methods	Include flow, shear alignment and the adsorption, onto the substrate, of an aligning agent dissolved in the LC [Krekhov, 1993], [Leslie, 1994], [Calmers, 1996], [Chevallard, 1997], [Derfel, 1997].

Table 1.1 Some of the main methods of aligning LC's.

The main methods of aligning LC, which are commonly used by microdisplay manufacturers, at the time of writing, are the oblique evaporation and rubbing techniques.

Oblique evaporation

Oblique evaporation of metals or oxides onto the surface, sometimes referred to as the Janning method, after its discoverer [Janning, 1972], offers a big advantage over rubbing techniques, for Spatial Light Modulators (SLMs) or displays based on active silicon backplanes, as electrostatic damage in Complementary Metal Oxide Semiconductor (CMOS) backplanes is minimized. The angle and rate of deposition are both important in determining the tilt angle of the columns [Geszti, 1987],[Goodman, 1976]. Grazing angle (phi1) depositions ~5-20° are referred to as Small Angle Deposition (SAD), and produce an inclined or tilted orientation of the

LC directors. Larger angles (phi2) of deposition (20-45°) are called Medium Angle Deposition (MAD), which yield a parallel alignment of the LC. Figure 1.3.

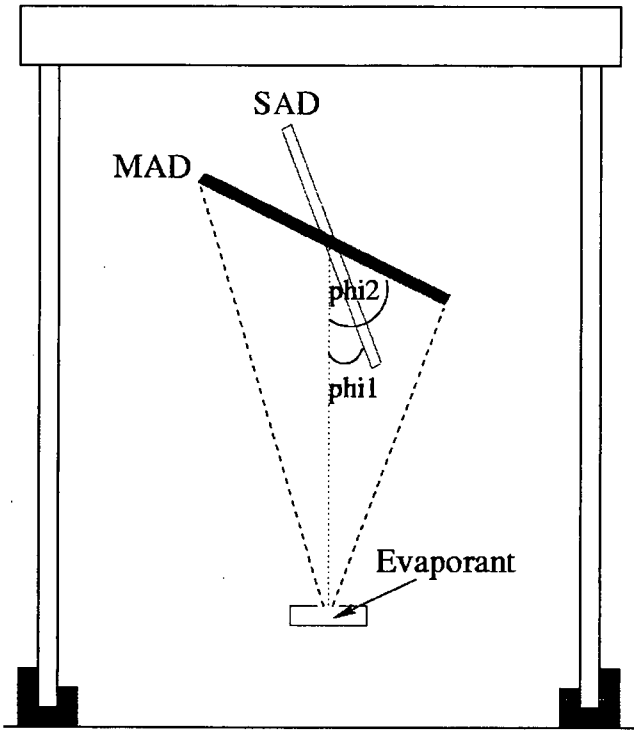

Figure 1.3 Schematic illustration of SAD and MAD oblique evaporation.

Many materials, which can be obliquely deposited, have provided liquid crystal alignment with differing results. For example Cr, Pt, Au, and SiO provide homogeneous alignment, whilst Cu gives homeotropic alignment. The oblique deposit causes a film growth in a preferred direction, which results in a "sympathetic alignment" of the nematic liquid crystals when applied [Janning, 1972].

Mechanism of liquid crystal alignment at a boundary

A uniform surface alignment is essential for many device applications. The bulk orientation of a LC is controlled by the alignment of the surface region. Mechanisms responsible for the orientation of LC on solid surfaces can be divided into two basic kinds, physical and chemical [Guyon, 1976]. In their analysis of the alignment of LCs on solid films deposited at grazing incidence, Guyon *et al.*, explained the

experimental results by a physical mechanism - the orientation dependence of the elastic energy. They assumed that the director was locally parallel to the surface everywhere, *i.e.*, chemical bonding. Although there are many publications, [Faetti, 1991], [Xiao, 1997], [Yokoyama, 1984], on the subject of liquid crystal alignment at boundaries, it is still poorly understood. One well known model which attempts to explain the planar or perpendicular alignment of nematic liquid crystals on a grooved surface is given by Berreman [1972]. As an explanation of the planar orientation along the direction of the rubbing it is suggested that the ends of the molecules all have the same affinity for the surface and the molecules tend to arrange themselves parallel to the surface. Comparing figures 1.4(a) and (b), it can be seen that orientation of the director perpendicular to the surface relief (a) requires elastic energy deformation of the medium, whereas positioning the director along the troughs in surface (b) is not accompanied by such a deformation. A similar argument is used for homeotropic or tilted orientation on columnar topologies. Several other theories have been proposed to explain surface alignment of LC's including; the surface tension model [Nakano, 1995], *van der Waals* force model [Seo, 1997], excluded volume effect model [Okano, 1983] and frictional rubbing [Mada, 1993], [Sugimura, 1993].

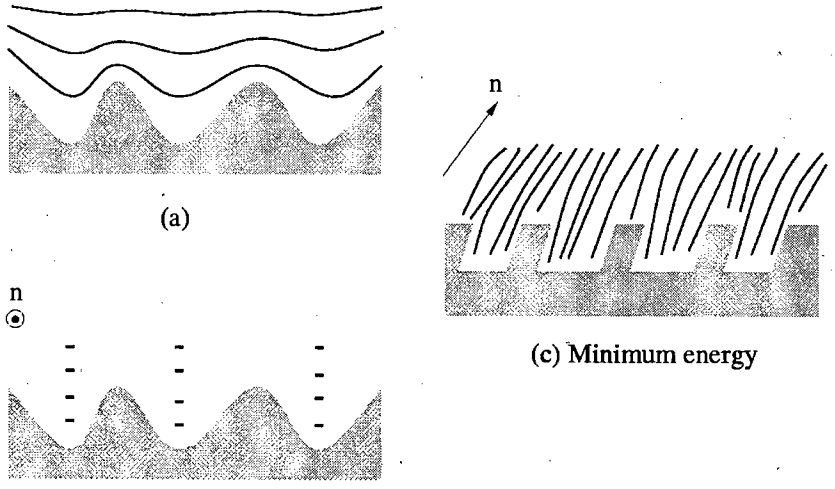

Figure 1.4 The directors (n) tend to align along the direction which minimize the elastic energy.(a) This orientation is energetically less favorable than (b) or (c). (b) Medium angle deposition leads to planar and (c) small (grazing) angle deposition to perpendicular/tilted LC alignment.

angle deposition to perpendicular/tilted LC alignment.

1.2 Modulation of light

There are essentially four variables in an optical wavefront which can be modulated as a function of spatial coordinates and time (i) intensity (amplitude), (ii) phase, (iii) polarization and (iv) spatial frequency (texture). It should be noted, however, that intensity (amplitude) and phase are the most commonly used representations in an optical computing system. The latter two are often used as intermediate representations that are converted into intensity or phase modulation before the information is used in the next stage of the optical computing system [Neff, 1990].

Surface stabilized FLCs (1.1.1) can operate in any of the first three modes described above, *i.e.,* amplitude, phase or polarization modulation.

(1) Amplitude modulation

A transmission mode SSFLC cell is placed between two crossed polarizers, figure 1.5, such that the FLC n_o axis is parallel to the input polarizer. In the "off" state, the path length experienced by the light, is $(2\pi/\lambda)n_o t$, where n_o is the refractive index experienced by plane polarized light traveling along the ordinary axis of the material and t is the material thickness, and the two orthogonal components of plane polarized light experience no phase retardation, and the exiting plane polarized light is blocked by the crossed analyzer. If the state of the director is then switched, the FLC director rotates through an angle, θ. The plane polarized light entering the FLC now experiences a phase retardance as the two orthogonal components propagate along n_e and n_o respectively. If the thickness of the FLC layer is correctly set, a π phase retardance can be achieved and the emerging waveform is plane polarized, but rotated by $\pi/2$. The light is then transmitted through the crossed analyzer.

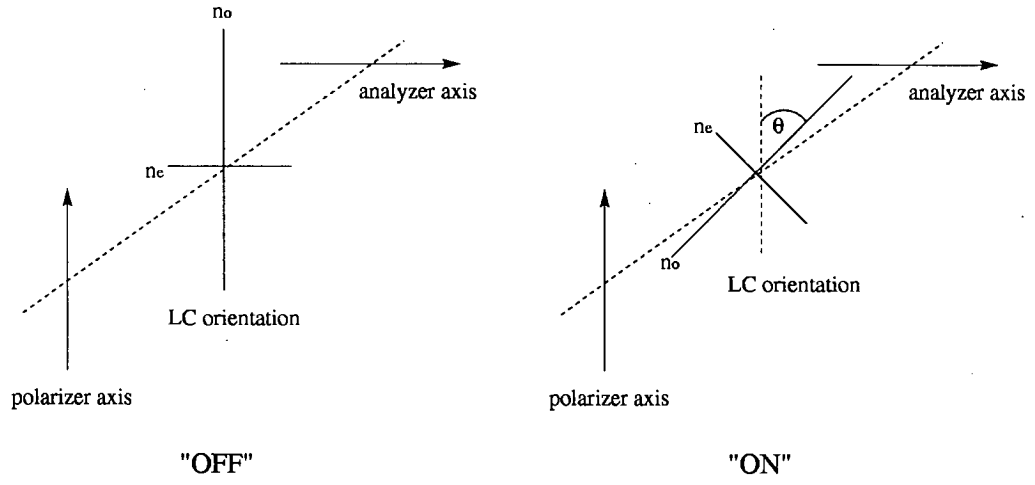

Figure 1.5 Amplitude modulation in transmission mode. Where the optimum cone angle of the SSFLC is 22.5^0. n_o and n_e are the refractive indices along the ordinary and extraordinary axes respectively.

(2) Phase modulation

To achieve phase modulation (which is the relative shift in phase between the two orthogonal components of the plane polarized light), cell is oriented such that the incident plane polarized light bisects the angle between the two director orientations, figure 1.6. If the correct FLC thickness (see chapter 4) is correctly set, the polarization can be rotated either clockwise or anti-clockwise upon switching.

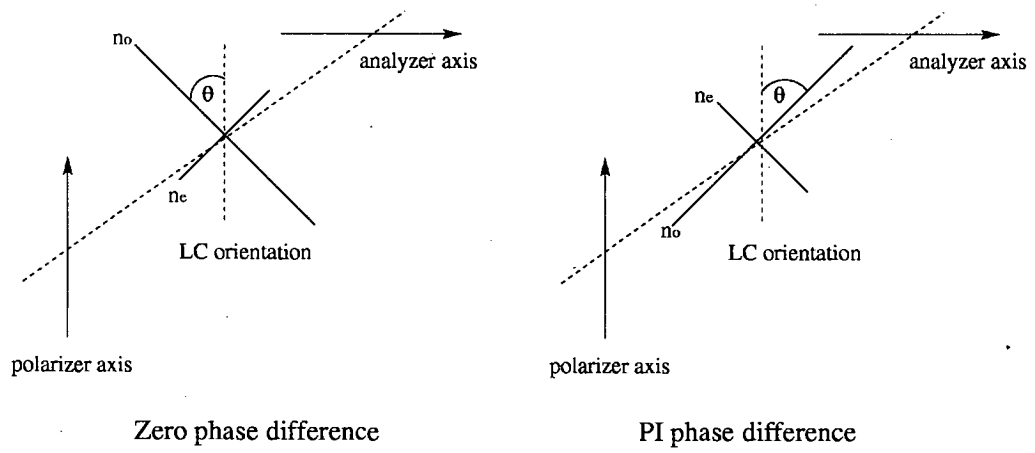

Figure 1.6 Where the cone angle should be 45^0

The same ideas can be applied to reflective mode devices. Figure 1.7 illustrates the operation of amplitude modulation in reflective mode.

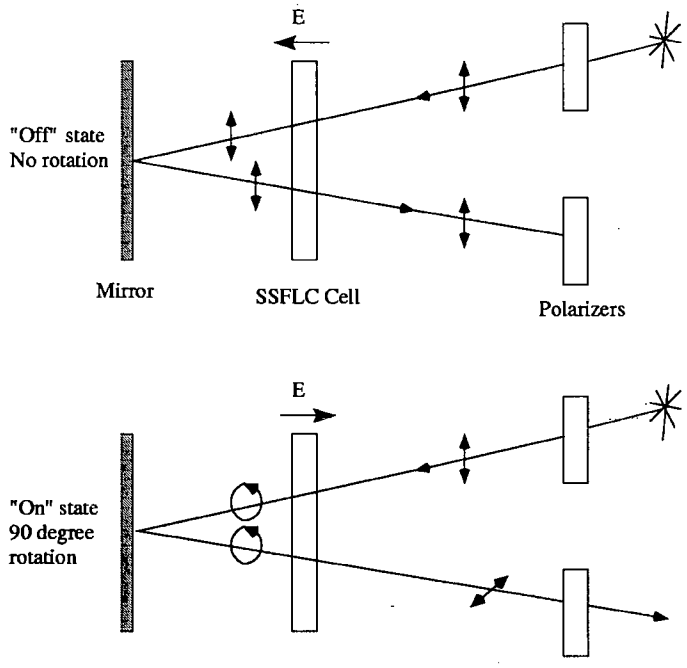

Figure 1.7 Illustrates reflective amplitude mode of operation which requires only half the LC thickness of transmissive mode due to the double pass of the transmitted light. The configuration for phase modulation is the same except that the orientation of the LC cell is as shown in the previous figure.

1.3 Spatial Light Modulators

Any device that spatially controls the light that passes through it is called a Spatial Light Modulator (SLM). This ability of SLMs to modulate spatially, as well as temporally, a 2-D optical wavefront gives optics a degree of parallelism not found in electronics.

1.3.1 SLM technologies

SLMs exist in many forms [Fisher, 1985]. Light modulation may be carried out by many mechanisms including electro-optic, acousto-optic and mechanical effects [Underwood, 1997] a selection of which are given in table 1.2.

Mechanism	Technology
Electro-optic	Self-electro-optic effect (SEED)[Liveai, 1988], [Millar, 1993] Liquid crystal (LC) [Underwood, 1986],[McKnight, 1989],[Cotter, 1990] Ceramic based (PLZT)[Land, 1974],[Smith, 1972]
Magneto-optic	Bismuth-substituted iron garnet film[Davis, 1988].
Mechanical	Elastomer[Hess, 1987],[True, 1987] Membrane [Vdovin, 1995] Cantilever mirrors [Younce, 1993] Acousto-optic Bragg cell [Pape, 1992]

Table 1.2 A selection of light modulation mechanisms.

The most important characteristic of LCs, compared with other modulator technologies, are their low power consumption, low voltage operation and large number of pixels. LC SLMs can be broadly divided into transmissive and reflective mode devices. The major advantages and disadvantages of the reflective mode are listed below, for both electrically and optically addressed pixels, section 1.3.2.

Advantages of the reflective mode

- Doubled depth of modulation of the electro-optic modulator (electrically addressed EA and optically addressed OASLM's), for a given thickness (by double passing).
- Isolation of the input write beam from the output, readout beam (OASLM's). To avoid having it write over the image, the read light must differ from the write light in wavelength, intensity or timing.
- Independence of the particular substrate used for growth of the modulator array (OASLM's) *i.e.,* the substrate need not be transmissive at the particular read out wavelength used [Efron, 1995].

- Reflective EA also permits the use of large fill-factor mirrors over the active pixel electronics.

Disadvantage of the reflective mode

- Added complexity in optical readout system. If polarization rotation is employed, a polarizing beam splitter can be used to achieve an efficient readout operation (EA and OASLM's).

The reflective-mode device is considered, by some investigators to be the preferred configuration [Efron, 1995]. For our application (LC over silicon), figure 1.8, we are constrained to operate in the reflective mode, in the visible.

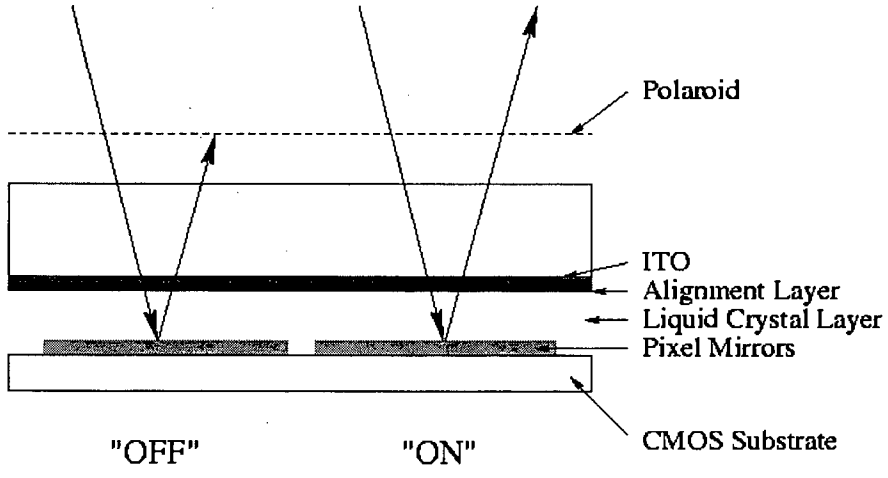

Figure 1.8 Cross-sectional illustration of a LCoS SLM.

1.3.2 Liquid Crystal SLM addressing.

LC SLM addressing falls into one of two categories; (i) electrical and (ii) optical addressing.

Electrical addressing

There are three main types of electrically addressed SLMs, figure 1.9: direct addressed, matrix addressed and active backplane addressed SLMs [Efron, 1995].

1) The area taken by the interconnects in direct addressed SLMs increases rapidly with the number of pixels, limiting arrays to having approximately 16 x 16 pixels [Collings, 1989].

2) A passive matrix of transparent electrodes is formed to address lines deposited on one substrate, and a perpendicular set deposited on the other substrate. A "strobe" voltage pulse is applied to each row, selecting it for a particular period. Strobe voltage, "data" voltage pulses are then applied to all the columns simultaneously.

3) In active matrix (backplane) SLMs each pixel has its own active circuit elements which drive it. Unlike the matrix addressed devices, it is not necessary to wait for the SSFLC to have switched before moving along to the next row. Active matrix addressing is used to overcome inherent difficulties due to slow response times of the modulating medium. It is the preferred approach especially when panels with large numbers of rows and columns are involved [Sherr, 1993]. There are several potential functions of the circuitry at each pixel, including charge storing.

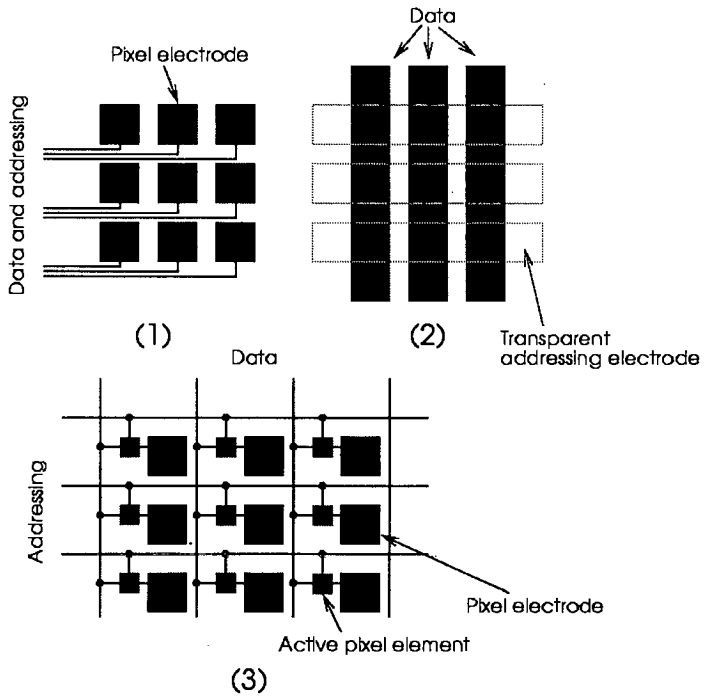

Figure 1.9 Graphical 3x3 matrix illustration of the addressing methods.
(1) Direct, (2) passive and (3) active addressing.

Because the frame rate of passive matrix (2) addressing is low compared to active backplane devices (3), their chief applications are flat panel displays, whereas active backplanes are better suited to optical processing and high resolution projection displays.

Optical addressing

In this study we are only interested in electrically addressed SLMs but this section will provide a brief introduction to optical addressing for completeness.

Several types of photodetector have been developed by various groups, including ZnS, ZnO, CdS, Se, CdSe, c-Si and a-Si:H [Efron, 1995]. The Huges liquid crystal light valve [Beard, 1973] incorporated a CdS photosensor and TNLC. Most recently developed Huges OASLM's incorporated an a-Si:H photoconductor [Sterling, 1990]. Hydrogenated amorphous silicon was used as an OASLM photosensor with nematic LC [Samuelson, 1979], and has become the most commonly used photosensor in LC OASLMs [Moddel, 1991].

The pin diode is formed from a-Si:H layer, figure 1.10, where the p-region is doped with boron. When the pin diode is under a reverse bias, an incident photon creates an electron-hole (e-h) pair in intrinsic layer. The photocurrent varies linearly with light intensity over a wide range of intensities because one e-h pair is collected for each absorbed photon.

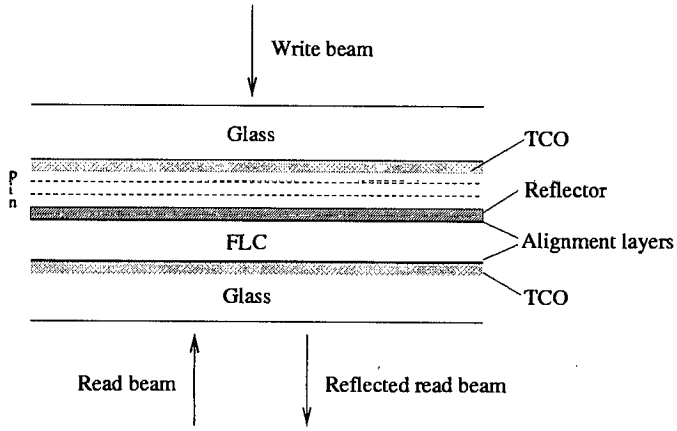

Figure 1.10 a-Si:H/FLC OASLM.

It should be noted that although OASLM's process information at higher rates and exhibit a higher optical resolution than EASLM's (addressing information arrives in parallel), the EA (LCoS) LC over silicon can posess smart pixels which enables the SLM to perform logic functions. LCoS also combines two mature technologies; namely liquid crystals and Very Large Scale Integrated (VLSI) circuits.

1.3.3 DRAM vs. SRAM Pixels

Active backplane EASLM's are based upon two types of memory used VLSI circuits: Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM). Where dynamic logic differs from static logic that the logic values are represented by the presence or absence of a charge stored isolated on capacitors, whereas static logic values are pulled firmly to Vss or Vdd via MOSFET's.

The DRAM pixel

The 1T-DRAM is the simplest memory element, figure 1.11. DRAM pixels require that there is sufficient charge stored in the pixel capacitor during the addressing part of the cycle to allow for charge redistribution, equation 1, induced by the dipole rotation [Johnson, 1993].

$$Q = 2 P_s A \qquad (1)$$

Where P_s is the spontaneous polarization of the FLC, A is the pixel area and Q is the charge. So enough charge must be stored in the pixel capacitor to ensure complete switching of the FLC.

From nMOS theory, the maximum drive voltage, from an nMOS DRAM pixel, is

$$Vo = Vdd - Vt$$

Where Vt is the threshold voltage and Vdd is the drain voltage. Therefore in an nMOS device, the output voltage (high) is degraded [Underwood, 1986]. This results in a lower FLC drive voltage and hence a reduction in switching speed.

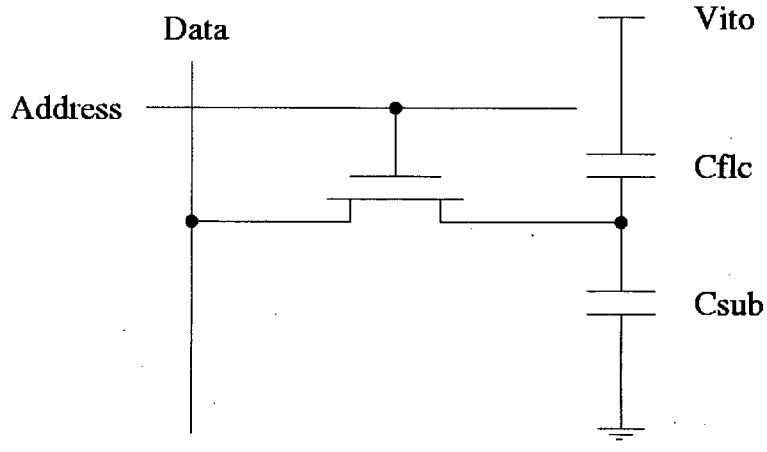

Figure 1.11 A single transistor DRAM pixel, where V_{ITO} is the voltage applied to the common ITO electrode, C_{FLC} is the LC capacitance and C_{SUB} is the substrate capacitance.

The SRAM pixel

With the SRAM memory element once the pixel has switched, electrical power remains connected to the LC for the entire frame time. Therefore limitations imposed by dipole switching are irrelevant [Collings,1989]. The XOR-SRAM pixel is used at present, figure 1.12.

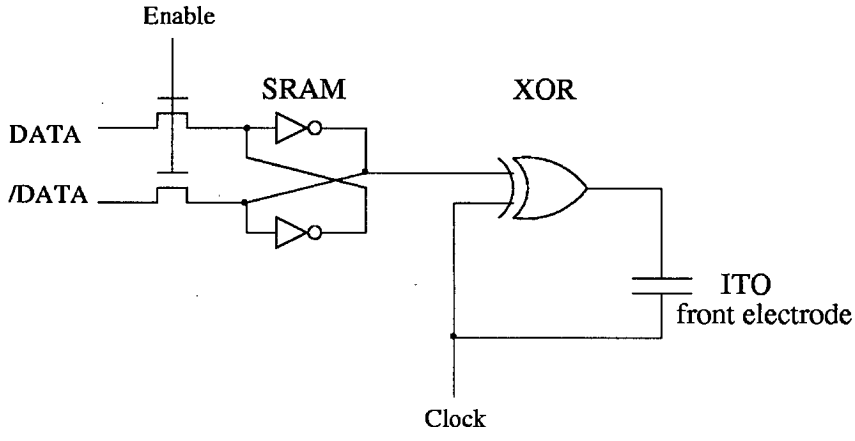

Figure 1.12 XOR-SRAM pixel [Burns, 1995].

Data is loaded into the SRAM latch when enable is at logic high. Charge balancing is achieved through the XOR part of the circuit, table 1.3. When DATA is at logic "1", the output of the XOR gate toggles between logic "1" and logic "0". When DATA is at logic "0", the output of the XOR gate is the same clock.

in	clock	out
0	0	0
0	1	1
1	0	1
1	1	0

Table 1.3 XOR truth table.

The table below provides a summary of the DRAM and SRAM pixels used in LCoS devices.

DRAM	SRAM
Small area	Large area
Easy connectivity	Complex connectivity
	High power consumption switching transients
Poor driving voltage	Full rail voltages to drive FLC
Needs refresh	no refresh
Charge leakage, charge balancing required (inverse frame) therefore pulsed light source	Charge balancing in circuitry (XOR), Constant illumination
nMOS pixel transistors	CMOS-latchup

Table 1.4 Characteristics of DRAM and SRAM backplanes.

Charge balancing

Liquid crystals always contain ionic impurities, which drift under the influence of an applied electric field, to the insulating LC alignment layer. These charges then accumulate at the LC bounding plates introducing an electic field, which must be overcome during switching. One way around this problem is to ensure that the time averaged voltage across the LC layer is zero.

DC balancing, in FLC devices, is generally achieved at the pixel level as follows. A frame of data is written onto the array and optically interrogated to produce a bit plane image. This is immediately followed by a complementary frame, *i.e.,* an inverse of the image. This complementary image is not usually optically interrogated [Underwood, 1997].

SRAM pixel devices achieve charge balancing using XOR circuitry, figure 1.10, as described earlier.

Charge balancing in nematic LC displays is achieved by applying a sinusoidal voltage, as the LC responds to the root mean square (rms) of the driving voltage.

Charge leakage

The voltage across the LC layer in DRAM pixel/backplane devices, decays as described above, require refreshing periodically. This is due to the charge in the pixel capacitor, which maintains the voltage across the liquid crystal layer, decaying, figure 1.11. It is also important to avoid the reduction of the decay time due to photoconductivity in the silicon backplane [Johnson, 1993].

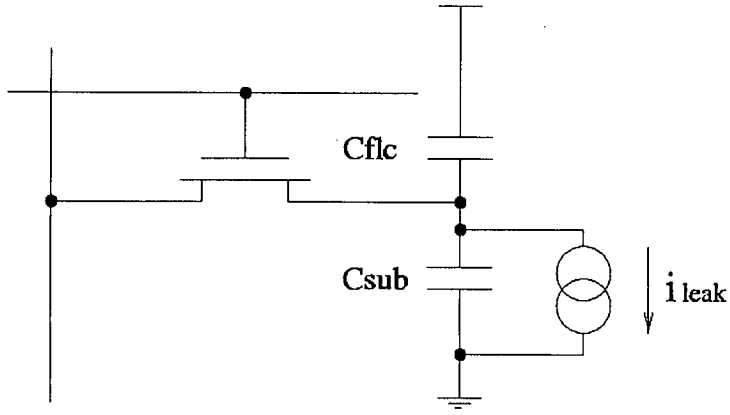

Figure 1.13 Equivalent circuit, where C_{FLC} is the capacitance of the FLC layer and C_{SUB} is the substrate capacitance.

1.4 Applications of LCoS SLM's

A complete review of the applications is beyond the scope of this thesis. Instead, a brief introduction of some of the main applications of LCoS SLM's will be given. Efron [1995] provides a more detailed review.

1.4.1 Optical information processing

Many specialized optical information processing systems have been reported, which make use of the physics of light propagation through various optical components to perform transformations on input datasets. Examples include optical corellation [Turner, 1993], and Fourier plane image processing [Lin, 1996].

In optical correlation an object at the first focal plane of a thin lens is illuminated with coherent light, the Fourier Transform ($\mathcal{F}$) of the object is obtained at the second focal plane. Filtering operations on the transform can allow a variety of image processing operations to be performed such as frequency filtering, matched filtering, pattern recognition, image recognition, image compression and feature extraction. The inverse Fourier Transform $\mathcal{F}^{-1}$ can be performed by a second lens, *i.e.*, $\mathcal{F}\{F(fx,fy)\}=f(-x,-y)$.

Optical correlation between two images f(x, y) and s(x, y), is written as

$$c(x, y)=f(x, y)\otimes s(x, y),$$

Where $\otimes$ represents the correlation operation. This equation can be re-written as

$$c(x,y) = \mathcal{F}\{F(f_x,f_y)S^*(f_x,f_y)\},$$

Where $F(f_x,f_y)$ is the Fourier Transform ($\mathcal{F}$) of f(x,y) and $S^*(f_x,f_y)$ is the complex conjugate of the $\mathcal{F}$ of s(x, y).

Two well known optical architectures for finding c(x,y) are;

(1) the Joint Transform Correlator (JTC)

(2) and the VanderLugt correlator.

Joint Transform Correlator

The JTC consists of two spatially separated images f(x, y) and s(x, y), which are simultaneously displayed on an input EASLM. A lens takes the analog $\mathcal{F}$ of the two images which is then recorded on an OASLM. A second lens performs the inverse $\mathcal{F}$ ($\mathcal{F}^{-1}$) of the intensity pattern and spatial filtering to yield the correlation function.

VanderLugt Correlator

In the VanderLugt correlator the images f(x, y) and $S^*(f_x,f_y)$ are encoded onto two separate EASLMs.

Performance limiting factors

The main factor which influences the performance of an LCoS based correlator is the backplane flatness and LC layer uniformity, 4.0.

The relative phase and absolute phase introduced by LCoS modulator depends on the LC layer thickness. Also a backplane flatness of $\lambda/16$ to $\lambda/20$ is required [Gourlay, 1995 and Lee, 1995].

Other requirements often include a high contrast ratio and very high switching speeds (in the microsecond range or better).

1.4.2 Optical computing and switching

The key concept for optical computing and switching is that light beams are used to encode and relay information, in place of flows of electric charge. In the case of optical computing, light can be used to route data around a system consisting of many separate electronic processors [Hart, 1998] in a flexible and changeable way. Fibers are used to carry information. To route this information from one fiber to another, the

optical signal is often converted to an electronic signal, routed electronically and then converted back to an optical signal. It would be much faster and more efficient to route signals optically, *i.e.,* without converting to electronic signals and back again.

Crossbar switches

Optical switching refers to the process of routing light beams carrying streams of information, to a number of destinations, in a dynamic, user defined way [Ichikawa, 1992].An optical crossbar is a means of achieving routing where the information remains in an optical form. N input channels require a 2-D array of N^2 pixels to fully connect to N output channels.

Performance limiting factors

The optical information is fanned out by diffractive or refractive optics. The main criteria for the modulator is a high contrast ratio, as a low contrast limits the number of channels routable due to cross-talk [Lee, 1995], and efficiency.

1.4.3 Displays

LCoS miniature displays are emerging as an important new class of displays. They are the engines that power electronic view finders, projection products and head mounted devices and are potentially the largest market for LCoS SLMs is displays [Chinnock, 1996].

Performance limiting factors

In displays, spatial frequency is one key factor of image quality. Other desirable properties include high light throughput efficiencies and a moderately high switching speed, to avoid visible flicker and ghosting. The typical requirements for reflective LCoS include a large pixel count, high pad reflectivity, good contrast ratio (100:1 or

better), the ability to produce grey scale and modulate incident light of multiple wavelengths (color displays), see table 1.5.

1.4.4 Requirements for some of the main applications of LCoS SLMs

	Contrast ratio	**Switching speed**	**Optical throughput (efficiency)**	**Flatness and uniformity**	**Space-bandwidth product**[1]
Optical information processing	High C.R desired	Video rates for real time optical processing [Lee, 1995]	Low insersion loss required. Especially as multiple SLM's are cascaded together, further exacerbating the problem.	Flatness of λ/16 to λ/20 required	High (parallel data processing)
Digital optical computing/ swithing and routing	Needs to be high as there is an intrinsic fan-out/fan-in (1/N) loss	High (video rates)	Low insersion loss required.	Similar as requirements for display	Low (few 100s of pixel elements)
Displays	Require C.R's of ≥100:1	High (frame rate in kHz for color displays)	Broadband antireflectance coating typically offers ~1% reflectance from top surface of coverglass	LC thickness uniformity over device <100nm	The human eye is most sensitive for spatial frequencies near 2-4 cycles per degree [lee, 1995]

Table 1.5 Summary of the more important LCoS specification requirements for optical systems.

All of the above, except the SBWP, can potentially be improved using the custom post-processing techniques described in this thesis.

[1] Number of pixel elements

1.5 Chronicle of LCoS Spatial Light Modulators development

The development of Liquid Crystal over Silicon (LCoS) SLM's was pioneered by the A.O. Group at the University of Edinburgh from 1983 with a 16x16 pixel guest-host LC [Underwood, 1986], and then a 50x50 NLC in 1988 [McKnight, 1989]. Later a collaboration between Displaytech and the Georgia Institute of Technology resulted in the design, fabrication and analysis of a 64x64 SRAM [Cotter, 1990] and a 256x256 DRAM SSFLCoS SLM. In 1993 Jared *et al.* and McKnight *et al.* from the University of Colorado developed 64x64 and 256x256 devices, respectively [Jared, 1993], [Mcknight, 1993]. In a collaboration between the University of Edinburgh, BNR Europe and GEC Marconi a 176x176 device was built [Underwood, 1991]. Table 1.6 summarizes the SLM's produced by the A.O. Group (or as part of a collaboration). The main current state of the art LCoS SLM's, including the 1280x1024 DRAM AFLCoS SLM being designed at the University of Edinburgh, are listed in table 1.7.

Device	Pixel/ pitch	Year	Fill factor[1] before/after planar-ization	Frame rate	Comments/ref (design house)
16x16	SRAM 200μm	1986	30/96	5Hz	nMOS [Underwood, 1986] (EU)
50x50	SRAM 72μm	1988	31/not applicable.	60Hz	Nematic [McKnight, 1989] (EU)
176x176	DRAM 30μm	1990	26/75	1KHz	Planarized [Underwood, 1991] (HPSLM)
64x64	DRAM 80μm	1992 1998	30/88 [Seunarine, 1999]	3KHz	High voltage (fault(s) found) Faults corrected (EU)
256x256	SRAM 40μm	1995	23/81	4KHz	Planarized (EU)
512x512	DRAM 20μm	1995	16/75	250Hz	Light protected [Rankin, 1997] (EU)
1024x768	DRAM 12μm	1997		5kHz	Light tight [Worboys, 1998] (SLIMDIS)

Table 1.6 Summary of the backplanes produced by the UoE (or as part of a colaboration described below).
EU→Edinburgh University
HPSLM→Edinburgh University, GEC Marconi and STC Technology
SLIMDIS→Edinburgh University, GEC Marconi, Admit Design Systems, Davin Optical Holdings and Swindon Silicon Systems.

[1] Does not include deduction for contact/via holes.

Manufacturer	Model	Resolution	Pixel pitch (μm)	Pixel fill factor(%)	Contrast ratio	Frame rate (Hz)	Comments
Microdisplay	MD640G2 MD800G6 MD1024G5	640x480 800x600 1024x768(XGA)	15.7 10 12.5	>85 91 >89	>50:1 >50:1 >50:1	30-90 180 30-180	NLC, each pixel is a triad of RGB diffraction gratings. Available 1999
SpatiaLight	M4-704x512	704x512	20				Available 1995
Three-Five Systems Inc.		640x480 (SVGA) 800x600 (SXGA)			>200:1		
MicroPix		1024x768	12	>75	100:1	180	DRAM, FLC
IBM		2048x2048	17			74	10V CMOS, DRAM, NLC, Light absorbing layer, planarized. Available 1998
Siliscope		800x600					Available 1998
Colorado Microdisplay (CMD)		800x600	12	80		75-90	NLC
Darpa		320x240 1280x1024 2560x2048				180 60 60	Available 1997
Motorola	MCVVQ410	320x240			80:1	72	CMOS SOI TFT
Displaytech	Lightcaster™	2560x1024	13.2			60	FLC
Varitronix Ltd. (HK)	VL704 VL1024	704x576 1024x768	9.6 13.3	88 91	70:1 70:1		NLC NLC
JVC	DLA-G10	1365x1024	13.5	>93	>250:1	50-78	
S-Vision	MicroLCD™	1024x768					Available 1999
Boulder Non-linear Systems Inc. (BNS)		256x256 512x512	21.6 15	60	70:1		
MOSAREL (ESPRIT IV project)	TFCG Micro-display	2560x2048	15				Light shielding layer, PDLC
University of Edinburgh	MINDIS	1280x1024	~10μm				Analog, anti-ferroelectric liquid crystal (under development)

Table 1.7 A selection of the current[1] state of the art LCoS microdisplays (a full description of the acronyms is given on page ii).

[1] Compiled from manufacturers web pages listed at http://www.microdisplayweb.com/developer/index.html

1.6 Aims of the project

Very Large Scale Integrated (VLSI) circuits and Liquid Crystal Displays (LCD's) are, independently, two very mature technologies. Unfortunately, difficulties arise when these two technologies are bought together in the form of a reflective Liquid Crystal over Silicon SLM. LCoS SLM's have generally been constructed using techniques "borrowed" from the LC display fraternity, since the first prototype was developed by Underwood [1986].

At the start of this research, the state of the art Liquid Crystal over Silicon SLMs were characterized, primarily, by a significant backplane warpage, poor LC layer thickness uniformity, poor optical quality mirrors and difficulty in maintaining the smectic layer structure in the FLC. These problems have hindered the construction of devices which offer an acceptable performance for applications such as those described in 1.4. Although vast improvements have been made to the quality of the mirror layer by previous workers in the field, they were still intolerably thick and the texture granular and there remained much room for further improvement.

The goal of my work was therefore to develop processes based on custom microfabrication processes which would significantly improve the LCoS SLM backplane flatness, uniformity (LC thickness and alignment texture), device contrast ratio, modulation efficiency and pad reflectivity.

An outline of this thesis.

In chapter 1 of this thesis I have introduced the main classifications of LCs and SLMs. In chapter 2, relevant LCoS microfabrication techniques will be discussed. Chapter 3 discusses the post-processing procedures which are under development or that have been developed by others. I also describe the work that I have carried out, with a colleague, to develop a process of patterning high reflectivity/pixel fill factor mirror electrodes and a novel inter-pixel trench filling process. In chapter 4, I present a novel die flattening technique, and cell assembly process, which has been used,

along with custom microfabricated spacer layers, fully characterized in chapter 5, to reduce significantly the backplane warpage and improve the LC layer thickness uniformity of assembled LCoS SLM's.

Chapter 6 describes some work that I have performed related to the transparent conductive ITO coated cover glass, in which I have suggested improvements which can be made to the inner surface coatings of the cover plate, which would lead to higher modulation efficiencies.

In the concluding chapter, the implications of such custom microfabrication processes on future LC based SLM's are discussed.

Chapter 2.

A Review of Relevant Microfabrication Techniques.

2.1 SLM Post-processing

LCoS Spatial Light Modulators backplanes are fabricated in silicon foundaries using conventional silicon semiconductor processing techniques. These techniques produce devices which have a poor optical quality and are significantly warped so are therefore not ideally suited for use as LCoS SLM's. Further backplane and coverglass processing is usually required, to enhance the devices optical quality for use in many of the applications, discussed in chapter 1.

Post-processing usually involves the deposition and patterning of thin films. In this chapter I will describe some of the most commonly used processes in detail before going on to discuss the specific post-processing procedures used by the Applied Optics Group/Silicon Technology Research Group, University of Edinburgh and others.

In the first part of this chapter I will define wafer bow/warp and describe some of the main thin film properties which we are interested in. I will then introduce the main thin film deposition methods which are used during the post-processing procedure for silicon backplane SLM's. An introduction to photolithography will be given followed by a discussion of planarization techniques, with an emphasis on chemical mechanical polishing (CMP), which is the only method to date of achieving global planarization (defined in 2.9). Various methods of patterning will then be introduced, including lift-off and the damascene process.

2.2 Wafer bow and warping

Since one of the aims of this work is to reduce the silicon backplane warpage and bow in assembled SLMs it will be appropriate to define these detrimental effects.

Wafer bow is defined as the concavity due to sawing, or the deformation from thermal processing of the wafer centerline. It is measured according to ASTM[1] std. F-534-84. Warpage, on the other hand, is defined as the deviation (difference between the maximum and minimum distance) exhibited by the centerline of a wafer from a planar condition, where such a deviation includes both concave and convex regions. Warpage is measured according to ASTM std. F-657-80 [Biddle, 1985].

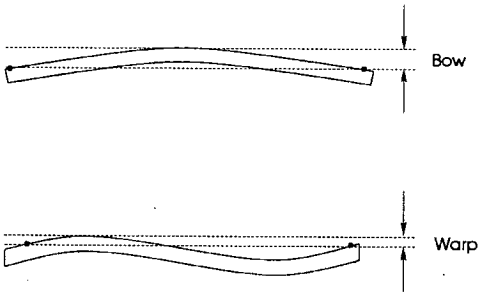

Figure 2.1 Wafer bow and warp.

The stresses that lead to warpage, in silicon wafers, originate from the temperature transients, which occur during insersion of the wafers into and the extraction of wafers from furnace tubes in high temperature processing. Following high temperature processing the periphery of the wafers cool at higher rates than the center, which leads to a temperature gradient and hence stresses in the wafers. When the stress in the wafers exceeds the yield point of silicon, dislocations form and plastic deformation occurs to partially relieve the stress. When the wafers have been cooled to room temperature, a reversed stress distribution, which cannot be relieved by plastic deformation, will be present. This stress causes the wafers to buckle. It should be noted that these stresses are also cummulative, which means that the warpage gets progressively worse through more processing. The parameters that influence warpage the most are [Einspruch, 1981]:

[1] American Society for Testing and Materials.

- Growth method of the starting material.
- Diameter / thickness ratio of the wafer.
- The nature of the cummulative thermal processing *i.e.* temperature, temperature gradients, heating and cooling rates *etc.*
- Amount and form of precipitates (oxygen) and the direction and magnitude of the initial bow.
- Nature of the films grown or deposited on the wafer surface.

2.3 Thin film properties

When deciding on a thin film deposition technique to deposit the various materials required for post-processing the LCoS SLM's it is important to consider properties of the film such as thickness uniformity, step coverage over features, adhesion to underlying films, film purity, film grain size and density. Obviously, a good thickness uniformity is required for most applications to ensure that the film thickness is maintained over the entire wafer. The step coverage, which is a measure of the film thickness uniformity over steep features, may or may not be a desirable property, depending on the application. The film adhesion to any underlying films and substrates should be high to avoid the film peeling away during subsequent processing. Other properties such as the purity, stoichemistry, grain size and density, again, may or may not be important, depending on the application.

2.4 The glow discharge

A plasma is a partially ionized gas in which the following processes may occur [Chapman, 1980]; dissociation, atomic ionization, molecular ionization, atomic exitation and molecular exitation.

The term "glow discharge" refers to the light given off by plasma sources due to the atomic/molecular exitations. Plasmas can be used in place of thermal techniques to

drive some chemical process [Chapman, 1980]. The radiation flux impinging on the deposition surface from the discharge consists of photons, electrons, and ions.

If the glow discharge is driven by an rf electric field, the electrons and ions move about the plasma, ionizing and exciting the gas, but few strike either electrode. Glow discharge plasmas are usually created at pressures in the 0.01 to 0.1 Torr range by the action of an electric field on the contained gas molecules. This causes the breakdown of the gas molecule into a variety of reactive species. The electric glow discharge which is usually generated by an rf source can also be created by ac, dc, or microwave sources [Levy, 1989]. Although the reactive molecules are near ambient temperature, the effective electron temperature can be 1-2 orders of magnitude higher.

2.5 Physical Vapor Deposition

Most layer deposition processes are carried out in the vapor phase. If the material to be deposited does not react chemically during deposition, then the process is referred to as physical vapor deposition (PVD). There are two types of physical vapor deposition (PVD); evaporation and sputtering. All PVD processes proceed according to the following sequence of steps:

- Converting the condensed phase into a gaseous or vapor phase.
- Transporting the gaseous phase from the source to the substrate.
- Condensing the gaseous source on the substrate, followed by the nucleation and growth of the film.

2.5.1 Evaporation

Evaporation is the simplest method of PVD. In this method the deposition material is vaporized in a ultra high vacuum (typically 10^{-5} to 10^{-6} Torr) [McGuire, 1988] from its liquid (or solid) phase, and the vapor is then transported and deposited onto the

substrate. There are several methods of heating the evaporants, including resistive, inductive, e-beam and laser methods, some of which are shown in figure 2.1.

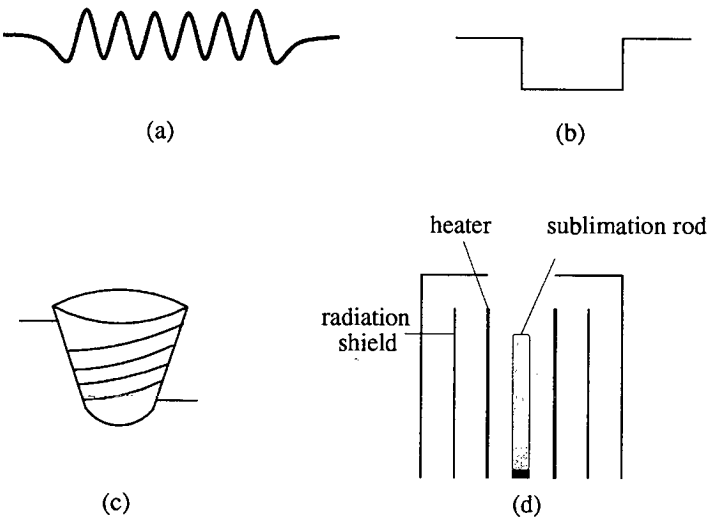

Figure 2.1 Methods of resistive heating (a) Wire, (b) metal foil, (c) crucible and (d) sublimation.

Wetting of the wire or foil surface by the evaporant is desired in order to achieve a good thermal contact. The most commonly used support materials are tungsten, molybdenum and tantalum. Crucible sources, figure 2.2, are required to support molten metal in quantities of a few grams or more. Sublimation sources remove the problem of contact between the evaporant and foreign support materials, thereby reducing contamination of the deposited film.

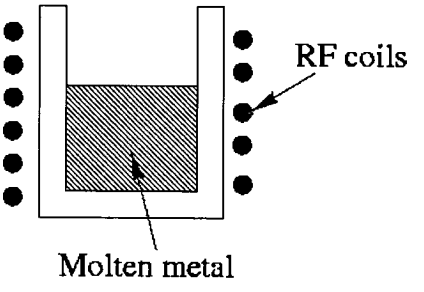

Figure 2.2 Inductive or rf heating.

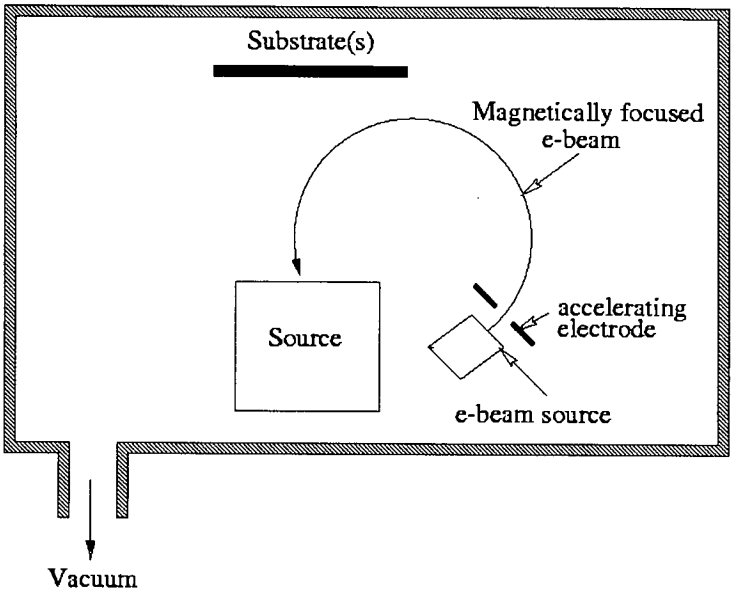

Figure 2.3 E-beam evaporation high evaporation rates and high purity deposits.

An electron beam (e-beam) can be used to heat the source, figure 2.3. Since the beam is concentrated on the evaporating surface, while other portions of the evaporant are maintained at lower temperatures, the evaporant can form its own crucible. Hence, interactions between the evaporant and support materials are greatly reduced.

2.5.2 Sputtering

Sputtering is the primary alternative to evaporation for metal film deposition in microelectronics. A target material is bombarded by inert, energetic ions, such as argon ions, to release some atoms from the target (into the vapor phase). Sputter deposition is very well controlled and provides a better step coverage[2] than evaporation [Wolf, 1986]. The two main disadvantages of this type of film deposition are that (a) the substrate is exposed to ion bombardment, which causes substrate damage and (b) the film trap small quantities of the sputtering gas.

[2] Uniform film thickness across the substrate and on steep sidewalls.

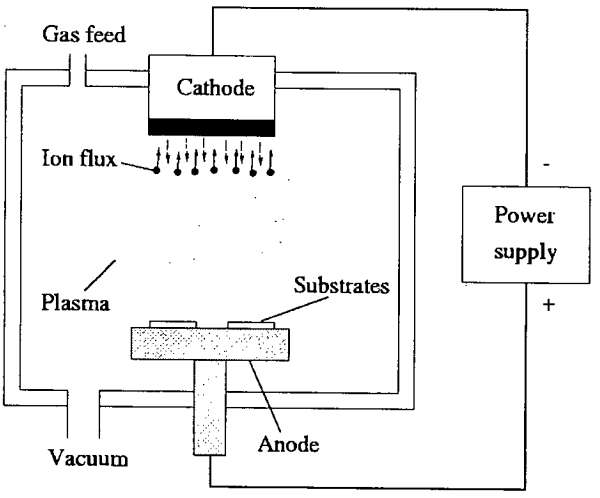

Figure 2.4 The simplest sputtering configuration is the planar diode type sputtering system, where the target is on the cathode [McGuire, 1988].

There are various methods of sputtering.

- Direct current (DC) sputtering, generally used for elemental metals, figure 2.4.
- Radio frequency (RF) sputtering, for insulating materials.
- Magnetron sputtering.

In both dc and rf sputtering, most of the secondary electrons emitted from the target do not cause ionization events with the Ar atoms. Magnetron sputtering can be used to increase the percentage of electrons that cause ionizing collisions, by utilizing a magnetic field to help confine the electrons near the target surface. The magnetic field applied to the plasma causes electrons in the plasma to spiral around the direction of the magnetic field lines. This orbital motion of the electrons increases the probability that they will collide with neutral species and create ions. The increased ion density decreases the Crooke's dark space [McGuire, 1988] and increases the rate of ion bombardment of the target.

2.6 Chemical Vapor Deposition

Chemical Vapor Deposition (CVD) is a method of depositing thin films, used extensively in the microelectronics industry. In our applications it is used for depositing dielectrics only as metal CVD films suffer from an extremely high surface roughness. CVD is a process where one or more gaseous species react on a solid surface and one of the reaction products is a solid phase material [Sherman, 1987]. The temperature of the surface must be high enough to cause a decomposition (pyrolysis) of the gas molecules. Most CVD processes are heterogeneous, that is, they take place at the substrate rather than in the gas phase.

The steps that must occur in every CVD reaction are:

- Transport of reacting gaseous species to the surface.
- Absorption, or chemisorption, of the species on the surface.
- Heterogenous surface reaction catalyzed by the surface.
- Desorption of the gaseous reaction products.
- Transport of the reaction products away from the surface.

Typical reactions which occur in the formation of SiO_2 and SiN (materials used extensively during post-processing) are shown below, by equations 2 and 3, respectively.

$$SiH_4 + 4N_2O \rightarrow SiO_2 + 4N_2 + 2H_2O \quad (2)$$

$$SiH_4 + N_2 \rightarrow 2SiNH + 3H_2 \quad (3)$$

To prevent homogenous gas phase nucleation, which causes particulate contamination on the wafer, the silane is diluted in an inert gas, typically He or N_2.

2.6.1 CVD techniques

The main methods of heating wafers during CVD are irradiation, direct resistive heating and inductive heating. Optical heating has one advantage over the other two methods of heating; the wafers can be heated from both sides enabling the wafer to be uniformly heated [Sherman, 1987]. CVD reactors come in a variety of forms, the nature of which depends on the tradeoffs made between performance criteria for a particular application. These criteria can include total wafer loading (*i.e.*, throughput), uniformity, sensitivity to particulates, sensitivity to contaminants, ultimate vacuum requirements, and so on. The form of the reactor also depends on the sensitivity of the process to temperature and flow conditions [Einspruch, 1987].

Atmospheric Pressure CVD

Chemical Vapor Deposition was originally developed as an atmospheric pressure process- APCVD. It is the simplest type of CVD process, as no vacuum pumps are required. The reactant gases are introduced into the reactor at close to atmospheric pressure and the temperature and gas flow rates determine the rate of film deposition.

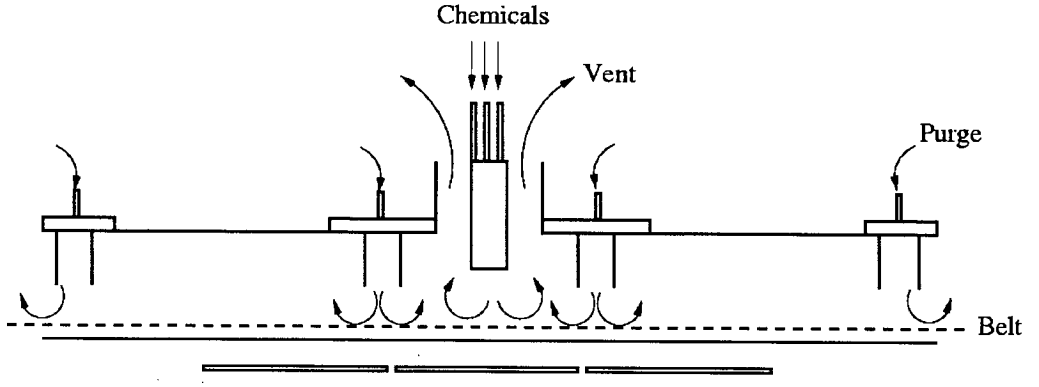

Figure 2.5 Simple continuous feed APCVD reactor [Wolf, 1986].

Low Pressure CVD

A major drawback of APCVD is particle formation. While particle formation in the gas phase can be controlled by adding a sufficient amount of N_2 or other inert gas, heterogeneous depositions can also occur at the gas injectors. Instead of a dilutent gas, the use of low pressures (0.1 to 1.0 torr) reduces gas phase nucleation. This process is commonly called LPCVD.

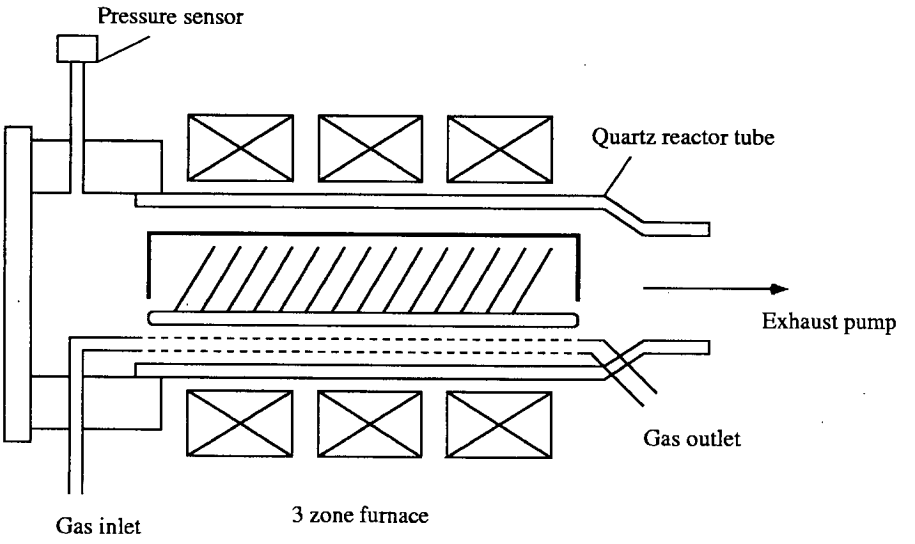

Figure 2.6 One of the common LPCVD reactor geometries [Wolf, 1986].

Plasma Enhanced-CVD

In many applications, it is necessary to deposit films at very low substrate temperatures. To accomodate these lower temperatures, an alternate energy source must be applied to the gaseous and/or adsorbed molecules. Plasma Enhanced CVD (PECVD) is a combination of a discharge process and low pressure chemical vapor deposition (LPCVD) in which highly reactive chemical species are generated from gaseous reactants by a glow discharge, 2.4, and interact to form a thin solid film product on the substrate [Levy, 1989].

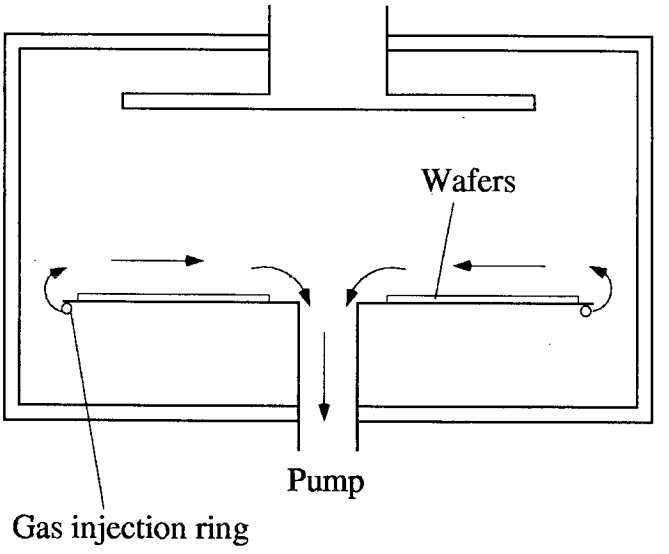

Figure 2.7 Parallel plate radial flow reactor [Wolf, 1986].

While photo-enhanced deposition has been experimentally demonstrated, the primary non-thermal energy source used to drive CVD reactors is the rf plasma [Campbell, 1996].

A summary of the main CVD techniques is given below in table 2.1.

	Advantages	**Disadvantages**
APCVD	Fast deposition, low temperature.	Poor step coverage, particulate contamination.
LPCVD	Excellent purity and uniformity, conformal.	High temperature, low deposition rate.
PECVD	Low temperature, fast deposition rate and good step coverage.	Chemical and particulate contamination

Table 2.1 Summary of CVD techniques.

Deposition method	Typical deposition rates	Comments
Sputtering	≥1.67nm/s for Al.	Ion damage to substrate, better step coverage than evaporated film, entrapment of small quantity of sputtering gas (poor optical quality films), good adherence of film to substrate.
Evaporation	0.1nm/s to 0.75nm/s for SiO_x and 7nm/s to 23nm/s for Al.	Extremely directional vapor flux, pure films (high vacuum 10^{-5} to 10^{-6} torr), poor thickness uniformity at high evaporation rates.
ECR-PECVD	0.167nm/s to 0.58nm/s for SiO_x	Excellent thickness uniformities and step coverage, film stoichemistry easily controlled.

Table 2.2 Summary of our "in-house" film deposition methods.

2.6.2 Electron Cyclotron Resonance

A subset of the PECVD type reactor is Electron Cyclotron Resonance-PECVD, figure 2.9. This type of reactor permits the deposition of thin films at much lower temperatures than with the standard PECVD reactor. The density of ionized species in the plasma can be greatly increased by application of a magnetic field. The ECR-PECVD reactor forms a plasma using a perpendicular static magnetic field along with an alternating electric field, $E_o\cos\omega t$. The electric field increases the magnitude of the electrons velocity, and the magnetic field changes the direction of the velocity vector. As the electron moves to the left, figure 2.8, the magnetic field deflects the electron toward the top of the page. If the frequency of oscillation is set to the electron cyclotron resonance frequency, equation 4, the deflection caused by the magnetic field is just enough to turn the electron by 180 degrees as the electric field changes sign. This resonance enables the electrons to gain much more energy than if no magnetic field were applied. Although ECR enables the plasma to be generated at very low temperatures, the actual ECR electron temperature is about 20,000K.

$$\omega = \omega_o = \frac{qB}{m} \qquad (4)\ \text{[Campbell, 1996]}$$

Where ω is the angular frequency of the electron, q is the electronic charge, m is the electron mass and B is the magnetic flux density.

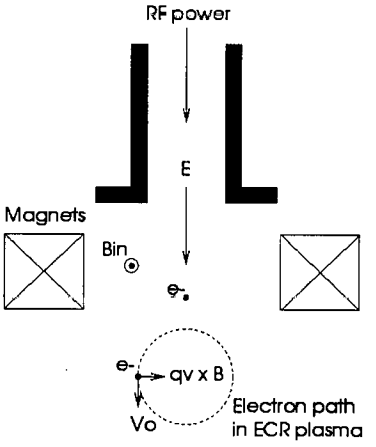

Figure 2.8 Electron cyclotron resonance. Where q is the electronic charge, v is the velocity vector of the electron in a magnetic field of flux density B and m is the mass of an electron.

2.6.3 ECR-PECVD

The ECR-PECVD reactor, figure 2.9, consists of two chambers. The first chamber is where the ECR plasma is formed, section 2.4. The second chamber, which contains the wafer(s), is where the reaction takes place. A shower ring directly above the table introduces the SiH_4/He mixture. The intense degree of ionization which occurs in the plasma chamber, is located away from the wafers. The ionized gasses are then, fluid dynamically, transported to the plenum chamber where the silane is introduced and the reaction takes place on the wafer surface [Sherman, 1987]. Magnet coils, placed underneath the wafer can also shape the extracted plasma into either a cusp shape, for good uniformity, or mirror shape, for filling high aspect ratios. A planar or compacted deposit can be obtained by introducing argon into the reaction chamber and providing rf power (typically 180 to 200W) to accelerate the argon ions into the depositing film causing compaction or even sputtering (if the RF power is high enough).

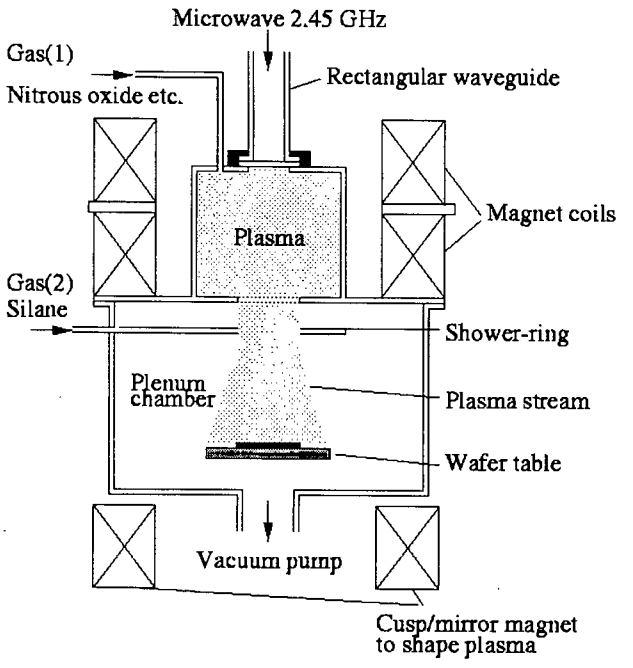

Figure 2.9 Schematic of an ECR-PECVD reactor.

2.7 Photolithography

The films deposited, as described in the previous sections, usually require patterning. All patterning processes are preceded by a photolithographic stage which involves the printing of an image onto a photoresist layer and removal, by some means, of the unwanted areas of the thin film. Photoresists for microelectronics are typically spun, sprayed, roller coated, or vapor deposited onto the substrate.

2.7.1 Photoresists

The primary requirement of the photoresist is that it should be capable of resolving the minimum feature size required. The resist should also have a high sensitivity, since this reduces the required exposure and good adhesion to the underlying film [Einspruch, 1981], [Ghandi, 1983].

Photoresists can be broadly divided into two classes - *positive* and *negative* resists. Positive photoresists are usually made up from a photosensitive dissolution inhibitor,

novolac resin and a solvent. The dissolution inhibitor prevents the novolac resin from dissolving in the alkaline developer. Following exposure to light the dissolution inhibitor concentration is reduced in the selected areas, which makes these areas more soluble in the developer. Negative resist, on the other hand, become less soluble in the areas exposed to light due to cross-linking in the base polymer. Negative resists are not in widespread use today due to their limiting characteristics. The main reason is that the resist suffers from swelling during the develop cycle. Removal of positive resists is relatively easy by means of a chemical solvent such as acetone. Unfortunately, negative resists are much harder to remove. One method of removal is to boil the wafers in concentrated sulfuric acid for about 20 minutes, followed by mechanical agitation [Ghandi, 1983]. Prior to coating the silicon substrate with the organic photoresist an adhesion promoter, Hexa-Methyl-Di-Silazane (HMDS) is applied. The HMDS molecules have two ends, one organic and the other inorganic. Upon spin coating (or vapor priming) the inorganic end of the molecule bonds to the silicon wafer, while the organic end is exposed, forming a monolayer with which the photoresist can easily bond.

2.7.2 Printing

The printing process consists of imaging a patterned mask[3] onto the photoresist coated substrate. The photoresist layers are usually exposed by means of a collimated UV light source shadowed by a photomask. The most common methods of printing, described below all have their own strengths and weaknesses in terms of performance. The four main parameters which affect the performance of a printer are resolution, level to level alignment accuracy, throughput and depth of focus.

Contact and proximity printing

In contact and proximity printing, the mask is pressed against or brought close to the wafer. When the distance between the mask and the wafer is less than the wavelength of the exposing light diffraction effects may be ignored. Contact printing, therefore,

[3] A typical photomask may consist of a quartz plate, which is transparent to the exposing light, with a patterned opaque layer such as chromium.

offers a greater resolution (providing there is uniform contact between the wafer and mask) than proximity printing, which has a wafer mask separation of 20 to 50μm. Unfortunately, contact between the mask and the wafer usually produces defects which limit the useful lifetime of the mask.

Projection printing or step-and-repeat

In projection printing, the image of the mask is projected onto the wafer through a high resolution optical lens, whose de-magnification can vary between 1 and 20 times. The resolution of projection printing technique is comparable to that of proximity printing, but it also offers greater flexibility of wafer handling. Because the wafer is printed in a step and repeat process, the throughput of the wafers can be very low.

Other types (e-beam and X-ray)

One limitation of the printers described above is the lack of resolution due to diffraction of the exposing light. One way around this is to use shorter wavelength sources, indeed this has been done with deep UV systems. The diffraction effects can be further reduced by use of non-optical printing methods such as electron beam and X-ray techniques.

2.8 Layer registration

Each level of an integrated circuit must be accurately positioned on the surface of the substrate/wafer. For this to occur, each level must be aligned to the previous, underlying, level.

2.8.1 Global & local alignment

Wafer alignment, in a stepper, can be performed both globally and locally. Global alignment performs rotational and translational alignment of the entire wafer [Wolf,

1986]. Following this "global alignment" the wafer is stepped and exposed (or blind stepped). Local alignment provides alignment to a target within the particular die which is in position for immediate exposure [Wolf, 1986]. Note: Local alignment is always preceded by global alignment.

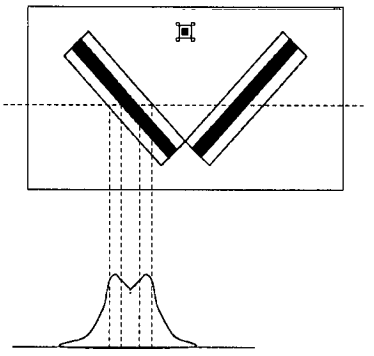

Figure 2.10 Target for automatic alignment.

In one type of automatic alignment procedure, figure 2.10, two rectangular patterns are set at 45^0, to the directions of the stage motions on the wafer. Two corresponding rectangular patterns are located on the reticle and illuminated by a He-Ne laser. The diffraction pattern produced by the edge of these marks is then detected by photosensors in the stepper, and the mask movement automatically adjusted until the response, from the photosensors, is equal, indicating a good geometrical alignment. Of course a good geometrical alignment does not necessarily mean that the layers will be perfectly aligned (registered) one on top of the other.

There are two main causes of mis-registration during printing. They are as follows;

1) variations in line sizes across a mask (not significant when used in a reduction stepper). The resist image on wafers may vary due to non-uniformities in resist thickness, variations in develop cycle *etc.*

2) uncertainty in aligning the image, summarized in figure 2.11.

The five types of image mis-alignment are [Wolf, 1986]; translation, rotation, magnification, trapezoidal and distortion.

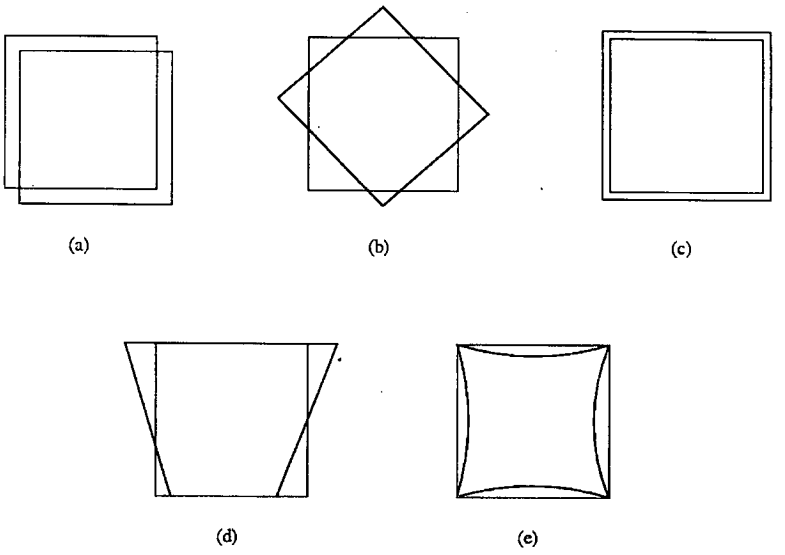

Figure 2.11 Illustration of the five types of image mis-alignment. (a) Translation, (b) rotation, (c) magnification, (d) trapezoidal and (e) distortion.

2.8.2 Registration accuracy of the optimetrix 8600 series 5X stepper

We are ultimately aiming to produce spacer features which would be positioned between the pixel mirrors of the SLM. The main reasons for deciding to print the spacers on top of the mirrors, were that;

(a) the sputtered aluminum, which is patterned to form the mirror/electrodes (chapter 3), has to fill the vias and for this reason the mirrors are 1-2μm in height and

(b) the lateral spacing between the mirrors is around 1.6 to 3μm, depending on the mirror layer reticle used and the etch process.

Obviously these high aspect ratio inter-pixel gaps place severe restrictions on any subsequent post-processing. Even without the problem of the 1-2μm high mirrors, there are limitations on the aspect ratio of the patterned photoresist layer, 4.3. One way around this is to produce mirrors whose top surface is flush with the surrounding oxide. This maybe achieved with the damascene process or via polishing/thin mirrors, 3.2. From section 5.2, we can see that thin film growth rates vary with substrate material. If the cell spacing is set from the spacer on the surrounding oxide layer, it

must not be permitted to overlap onto the Al mirrors, even if the mirrors are "flush" with the oxide. To allow for any misregistration of the projected image, during printing, the registration uncertainty must be known and accounted for in the spacer layer design.

Image registration uncertainty

This registration uncertainty places even more restrictions of the geometry on the spacer layer. The best alignment which can be achieved using the Optimetrix 8600 series 5X stepper is about +/-0.5μm, but to account for the other factors such as magnification, rotation *etc.* (2.6.1) this value should be doubled to +/-1μm [Stevenson, 1998].

2.9 Planarization

As the number of metalization levels in integrated circuits increases the topography of the top surface become more uneven. The depth of focus limitations of steppers, requires that the layers are made planar[1]. Obviously, the larger the planarization distance, the better the planarity of the layer. Typically, local planarization (<10μm) is a result of smoothing and filling, figure 2.12, whereas planarization beyond 10μm is regarded as global planarization [Cook, 1995]. The conventional planarization techniques, described in the following sections, only provide planarization in the micron range. Chemical Mechanical Polishing (CMP), on the other hand, can provide planarization in the millimeter range [Cook, 1995], section 2.9.2.

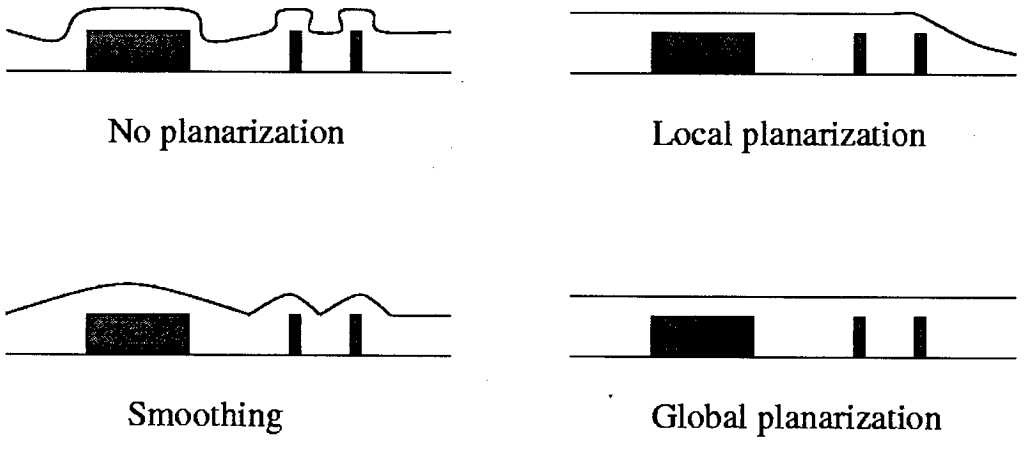

Figure 2.12 Planarization capability.

2.9.1 Local planarization techniques

Some of the more common local planarization techniques are discussed below.

[1] LCoS SLM's require post-processing planarization for different reasons, see section 3.1.

Spin-on techniques

A liquid material is spun onto a wafer in a spin coater and cured by heating, typically on a hot plate. Materials used include polymers, such as polyimides and photoresists and spin-on glass (SOG). Before curing the material is allowed to level out to provide some degree of planarization. SOG materials are well known for their ability to fill small gaps.

Thermal flow

Phosphosilicate glass (PSG) is reflowed at high temperatures (900-1100°C) to achieve planarization. The softening point of the glass may be reduced if it is suitably doped with boron, to produce borophosphosilicate glass (BPSG), which softens at up to 300°C lower than that of PSG.

Bias-sputtered dielectrics

The SiO_2 dielectric layer deposition can be modified such that an rf bias causes simultaneous resputtering during deposition, see section 2.4.4. The substrate is biased so that back-sputtering is facilitated on the surface. This sputter deposition and back-sputter etching occur simultaneously across the sample. Backsputtering is asymmetric and is favored at sharp corners and edges in such a manner that, when optimized, it gives excellent step coverage of the deposit, ending up as a flat surface. Bias sputter deposition rates are, however, low. Also ion damage may occur during these depositions.

Etch back

A very thick layer dielectric layer (~ 3 times the original step height) is deposited by CVD and as the thickness of this layer increases the surface becomes more planar. The surface is then coated with a thick layer of photoresist, which covers all the steps leaving a planar surface. The photoresist and dielectric layers are then etched back to

the desired thickness in a planarizing anisotropic etch, such as RIE or plasma etching, in a suitable chemistry. The dielectric and phototresist layer should have similar etch rates to ensure a planar surface.

Oxide spacer approach

Phosphosilicate glass (PSG) is deposited over metal and then anisotropically etched. This leaves portions of unetched PSG by the vertical sides of the conductor, called oxide spacers. These spacers are also formed at the bottom of steep steps. After this a second layer of PSG is conformally deposited, which provides a semiplanarized topology.

Self-aligned silica spacer particle method

A layer of silica spacer particles with a diameter equal to that of the height of the patterned metal layer, is deposited onto the patterned substrate. The particles fill the gaps between the metal lines, leveling the substrate for a subsequent P-TEOS SiO_2 deposition and SOG coat [Ohkura, 1995].

2.9.2 Global planarization - Chemical Mechanical Polishing

Chemical Mechanical Polishing/Planarization (CMP), figure 2.13, is an extremely complicated process involving removal of the sacrificial dielectric layer material, to obtain a high degree of planarity, by both mechanical and chemical means. The abrasive slurry, used in the polishing process, is dispersed in an alkaline solution. The polishing process is essentially the result of a combination of material removal by direct (abrasive) contact of the slurry particles and by chemical reactions mediated by the local conditions of contact, that is, elevated pressure and temperature. The material removal rate depends on various parameters, such as polishing pressure, speed, slurry chemistry and temperature, pad type and condition, film material and topology and materials under layer being polished [Islamraja, 1995], [Ohtani, 1995], [Wang, 1995]. CMP is the only method, to date, of achieving global planrization.

Planarity is measured over distances ranging from micrometers to millimeters and is a gauge of die flatness. Uniformity is measured over milimeters or centimeters and is a gauge of film thickness variation across the wafer. Thus a wafer can be planar but not uniform and vice versa. The recipe for good planarity requires opposing tool settings and pad characteristics than are needed for good uniformity. For example, planarity requires a hard pad and low pressure to prevent the pad from conforming to the device features and thus polish low spots as well as high. Conversely, uniformity requires a soft pad and high pressure to conform to variations of the wafer surface. Most device manufacturers now compromise by using a stacked pad consisting of a hard pad with an underlying soft pad [DeJule, 1996].

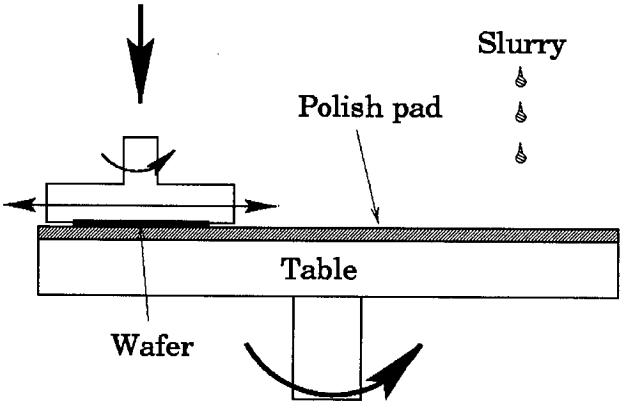

Figure 2.13 Key tooling elements of CMP equipment, where the table rotates as indicated.

The CMP process

Abrasives in the slurry play the very important role of transferring mechanical energy to the surface being polished. The slurry provides both the chemical action through the solution chemistry and the mechanical action through the abrasives. The most commonly used abrasives include silicon dioxide, alumina and cerium oxide. The most frequently referenced expression for polish rate is the Preston equation [Preston, 1927], equation 5.

$$\frac{\Delta H}{\Delta t} = K_p\left(\frac{L}{A}\right)\left(\frac{\Delta s}{\Delta t}\right) \qquad (5)$$

Where $\Delta H/\Delta t$ is the removal rate of the material, L/A is the pressure between the pad and polished surface and $\Delta s/\Delta t$ is the relative velocity of the polish pad with respect to the surface and K_p is the Preston coefficient.

The concepts discussed next are broadly applicable to all types of CMP.

Models of abrasion

The main difference between grinding and polishing is the abrasive size, table 2.3. Polishing (as opposed to microgrinding) may occur by either Hertzian indentation or by fluid-based wear [Steigerwald, 1997]. During Hertzian indentation, the abrasives are dragged across the surface and act as cutting tools. During fluid based wear, however, abrasive particles are not dragged across the surface but rather impinge on the surface at some velocity and angle. As particles collide with the surface they impart energy to the surface resulting in strain, weakened bonds, and eventually material removal. There is still some debate whether the polishing occurs as a result of Hertzian indentation or fluid-based wear. The polishing mode and role of the fluid layer is poorly understood at this point in time.

Abrasion mode	Mass removal via	Scale of mass removal
Grinding	Crack propagation fracture	Macroscopic particles (μm)
Ductile grinding[2]	Crack initiation plastic flow, densification	Colloidal particles (nm)
Polishing	Bond breakage chemical reaction	Atomic clusters (Angstoms)

Table 2.3 Summary of abrasion modes from [Cook, 1995].

[2] Ductile grinding refers to the plastic deformation of the material during polishing.

Role of chemistry in CMP

Chemistry plays a significant role in the CMP process. Each material has a different chemistry as far as chemical interactions with the slurry are concerned. Slurry chemicals affect primarily the chemical components, *e.g.*, etch rate. However, chemical reactions modify the mechanical properties of the film, pad, and abrasive surface, which in turn affects the mechanical component.

Some of the variables, which affect the polishing process, are;

- the chemical composition of the surface being polished,
- formation of the passivating layer at the solid surface caused by the oxidizer,
- dissolution of the solid surface or the mechanically abraded solid fragments or atoms/molecules of the original passivating layer,
- the isoelectric point related to abrasive and solid surface charge layers,
- effective removal or re-deposition of the polished material *etc.* are all determined by chemical interactions induced by the chemicals in the slurry and the solid surface.

In general, metal CMP slurries are more chemically active than oxide CMP slurries [Steigerwald, 1997].

Slurry contamination

KOH based coloidal silica slurry is a major source of silica particles, and agglomeration of the silica particles during CMP is known to be a source of particles. Particles generated during CMP can either adhere to or become embedded into the wafer surface. The adhesion forces become increasingly significant for fine particles. The principle interactions that are encountered in the particle adhesion include molecular adhesion, electrostatic interactions, liquid bridges, double layer repulsion and chemical bonds such as polar and metallic bonds. Chemical bonding of the silica

particles to the oxide surface occurs when it dehydrates. Once this occurs, the bonding is so strong that conventional chemical and mechanical cleaning of the surface is ineffective [Roy, 1995].

A low concentration hydrofluoric acid (HF) can be sprayed onto the wafer, during scrubbing, to remove a thin oxide layer. This not only removes the adhered and mechanically embedded particles but also the metallic and ionic contaminants.

2.10 Layer patterning

Fabrication of circuits and/or structures on silicon substrates requires layers to be patterned into the desired geometries. There are essentially four methods of patterning layers, which will be described in this section.

2.10.1 Chemical etching

Chemical etching involves the dissolution of a material in a solvent as well as the conversion of the material into a soluble compound which can be disolved by the etching medium. Chemical etching can be divided into wet and dry etching techniques. Wet etching is isotropic whereas dry etching techniques such as Reactive Ion Etching (RIE), which combines the effects of energetic species and ion bombardment, are anisotropic. The main advantage of chemical etching, over techniques such as lift-off, is the resulting square profiles of the patterned features [Wolf, 1986].

Simplified equations for chemical etching of Al (6) and silicon dioxide (7) are given by

$$Al + 3Cl \rightarrow AlCl_3 \quad (6)$$

$$SiO_2 + 4F \rightarrow SiF_4 + O_2 \quad (7)$$

2.10.2 Lift-off

Lift-off was first developed in the late 1960's with the advent of e-beam lithography. The most important part of lift-off is the overhang in the photoresist which is essential for maintaining the discontinuity in the patterned film figure 2.14. E-beam lithography utilizes the fact that electron scattering in the resist and backscattering from the substrate produces a pear shaped energy absorption profile in the resist [Collins, 1982] in which an undercut profile results after developing.

The absorption profile of conventional optical (UV) lithography differs from that of e-beam lithography in that most of the energy is absorbed at the top surface of the photoresist layer. Obviously this type of exposure will not provide the overhang, in the photoresist layer, required for the lift-off process. A way of achieving this overhang, with UV exposure, is to use multi-layers of photoresist, described later.

The diagram below, in figure 2.14, shows how chemical etching differs from liftoff. In chemical etching the material to be patterned, in our case oxide, is deposited, followed by the photoresist. The photoresist layer is then patterned and developed prior to either isotropic wet etching or anisotropic dry etching of the material. Patterning by liftoff differs in that the photoresist layer is put down first. Again the resist is patterned and developed, but prior to developing some form of surface modification is carried out to achieve the liftoff profile. The material (oxide or metal) is then blanket deposited over the patterned photoresist layer, followed by removal of the photoresist layer and unwanted material.

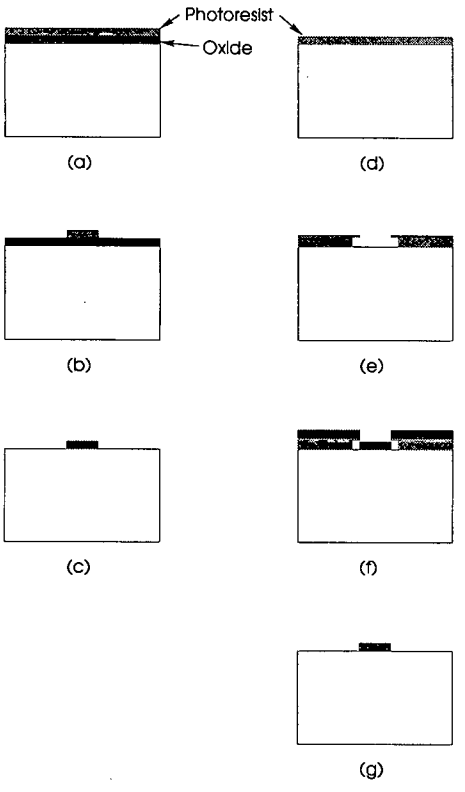

Figure 2.14 (a)-(c) Chemical etching and (d)-(g) liftoff.

Multi-layer resists for lift-off

The main advantage of multilayer resist schemes is the higher resolution which is possible. Planarization is necessary in photolithography for printing at diffraction limited dimensions in thick resist films. Organic and inorganic processing layers beneath a thin imaging layer was invented to surmount step coverage problems. Two or more layers of photoresist with different solubility's in the developer have been used to provide the lift-off profile. Unfortunately it is difficult to spin coat two layers without excessive mixing of the PRs at the interface. This mixing occurs when the first layer is re-dissolved by the solvent in the second layer [Hatzakis, 1980].

Surface modification for lift-off

Chlorobenzene, or similar compounds, have been used in industry, for many years, to provide a lift-off profile in the PR and to also increase the resolution. The softbaked photoresist is either soaked in chlorobenzene before or after printing. The depth of the modified layer depends on the soak time and temperature and the resist pre-bake cycle [Collins, 1982]. Chlorobenzene works by removing the residual solvent and low molecular weight resin, thereby reducing the solubility of the modified layer in the developer solution [Hatzakis, 1980], [Halverson, 1982].

2.10.3 Damascene

The Damascene process derives its name from the practice used by the ancient artisans of Damascus for patterning metal inlays [Singer, 1997]. This process involves patterning a layer such that it is flush with the surrounding dielectric. This method is useful for patterning materials which are difficult to etch chemically, such as copper. In this method, the dielectric layer is etched, instead of the material to be patterned. The material is then blanket deposited and polished back to the dielectic layer. This is explained in more detail in section 3.14.

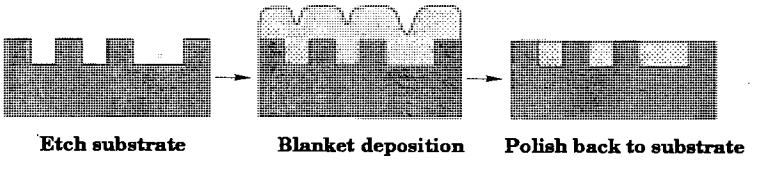

Figure 2.15 The interlayer dielectric is etched with the pattern of the metal, followed by a blanket deposition of metal and polishing back to the substrate.

Problems exist with this technique which will be described in detail in chapter 3.

2.10.4 Plating or selective deposition

This method differs from the conventional subtractive etch methods, described above, in that it is totally additive. A common deposition method is selective CVD [Amazawa, 1998] other methods include the use of an electron beam to alter the nature of a polymer film so that nucleation of a subsequent evaporated metal layer occurs only in the desired regions.

Chapter 3.

SLM Backplane Post-processing.

3.1 Introduction

Probably the most important issues which we have found to affect the optical performance of LCoS devices are the liquid crystal thickness uniformity, backplane warpage and LC alignment. In this section I will discuss the custom fabrication techniques, developed in the past. These improvements can be broadly divided into two areas; (1) increasing the pixel fill factor for increased optical efficiency and improved LC alignment, and (2) introducing a light blocking layer to improve the stability of the FLC, by reducing light induced charge leakage in the silicon. I will then go on to discuss the problems which still exist with the current mirror forming processes. An alternative method of fabricating mirror electrodes will be presented and a novel inter-mirror trench filling technique discussed. Most of the work discussed on thin mirror processing was carried out, approximately equally, by the author and D.W. Calton.

3.2 Planarized SLM

The early FLC/VLSI SLM's were characterized by low pixel fill factors[1] and very poor optical quality mirrors [O'Hara, 1993, 1994 and 1995]. The only way of drastically increasing the fill factor of the pixel mirrors is to fabricate the pixel mirror over the circuitry using a multi-level metalization technique. By depositing an intermediate layer of dielectric material, conducting mirror-electrodes can be

[1] Defined as the pixel area divided by the pixel pitch squared.

deposited over the circuitry, figure 3.1. Various dielectric materials have been used, but we have found that polished silicon dioxide layer produces the best results [O'Hara, 1996]. This polished silicon dioxide has the advantage of being optically flat. A problem which affected the mirror optical quality was hillock formation. This well known phenomenon [O' Hara, 1993], [Pico, 1993] occurs during the heating and cooling cycle of the sintering[2] process.

Irregular surface depressions, on the LC bounding substrates, locally alter the alignment of the LC on the bounding surfaces, required for a good SSFLC device. They disturb the formation of parallel smectic planes, vary the surface molecular tilt angle and randomly induce defects from the device ideal. Ideally, the surface energy of the LC should be uniform across the bounding plates of the FLC device. If large enough, any perturbation from this uniformity will unduly affect the molecular alignment in the bulk FLC material. Therefore, mirror quality will directly determine structure and may undermine any post-filling FLC cell treatment techniques [Gourlay, 1994].

The relatively low melting point of the aluminum (660°C) therefore limits the interlayer dielectric material to one which can be deposited at low temperatures(<100°C). It has been reported that hillocks begin to form in the aluminum at temperatures of ~200-300°C [Ross, 1999]. Fortunately ECR-PECVD silicon dioxide, section 2.4.4, offered the characteristics which made it the ideal interlayer dielectric material for this application. A compacted form of the silicon dioxide was deposited and polished by Chemical Mechanical Polishing (CMP)[3] to provide a high quality planar surface for the subsequent pixel mirrors. Although a local surface variation of less than 10nm rms had been quoted [O'Hara, 1995] the author remains sceptical as to the validity of this figure due to the measurement technique used[4].

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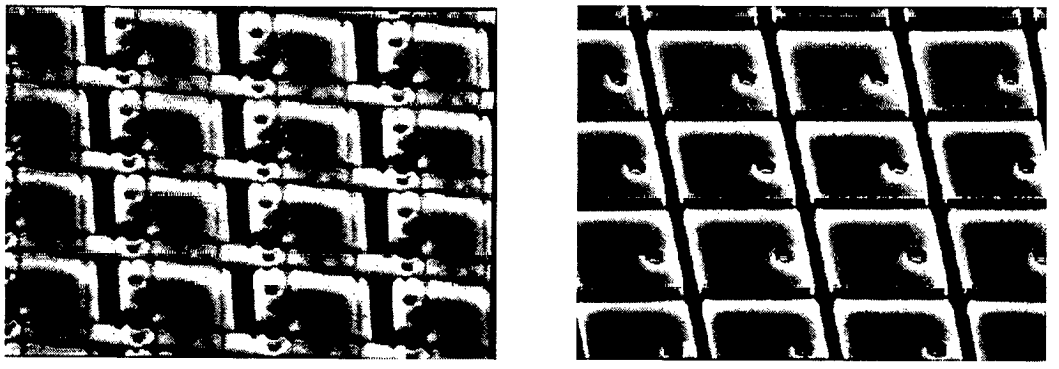
[2] Sintering is carried out to provide a good adhesion of the metal to the dielectric layer.

[3] Early CMP was performed using the Logitech PS2000 polisher rather than the Presi 460 now used.

[4] Dektak 8000.



(a) (b)

Figure 3.1 (a) Non-planar 512x512 pixel and (b) planarized 512x512. Courtesy of A. O'Hara.

3.3 Light blocking layer

The light blocking layer has been developed [O'Hara, 1995], [Huang, 1996] to act as a light shield to prevent light reaching the silicon substrate. The gap between the pixel mirrors of the 256x256 pixel SLM [Burns, 1995] and 512x512 pixel SLM are currently 3μm and 1.6μm, depending on the mask set used to pattern the mirrors. Obviously, with the underlying dielectric being silicon dioxide, which is optically transparent, there is a danger that incident photons will reach the underlying pixel circuitry of the device. This can then lead to charge leakage in DRAM devices (1.1), and the potentially destructive situation of latchup[5]. To overcome this problem additional processing steps require specially designed masks, figure 3.2. These are incorporated into the post-processing procedure in which a metal or black matrix layer is used to block the gap between the pixels.

[5] The formation of lateral and vertical bipolar, parasitic transistors is intrinsic to the bulk CMOS process. These transistors contribute to the effect known as "latchup", which is undoubtedly the most destructive event that can take place in CMOS circuitry (during device operation).

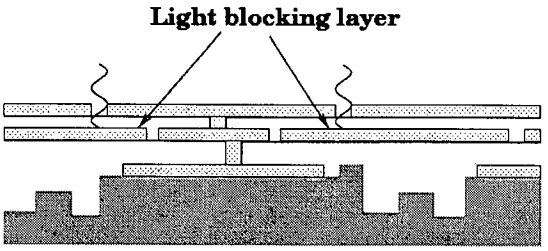


Figure 3.2 An additional metallization level is used to shield the underlying CMOS circuitry from the incident light through the gap between the pixel mirrors.

An attempt to characterize these layers was made by M. Sussiek, of the Department of Electrical Engineering, University of Edinburgh. Test structures consisting of two metal layers representing the light blocking and mirror layers were deposited and patterned onto glass wafers. The metal layers were separated by a layer of ECR oxide, which had been planarized by CMP. It is expected that light propagation in the "light guiding" structure should not be supported when the thickness is less than half the wavelength of the incident light. The results of this experiment indicated that the Huygens-Fresnel diffraction dominated, but his expermental results could not dismiss the mode propagation between the metal layers in the planarized oxide [Sussiek, 1998].

3.4 Damascene process

The next logical progression from planarization of the silicon backplane was to introduce processes which would enable us to produce mirrors which were flush with the surrounding oxide. This would provide a substrate which is more conducive to LC and in particular SSFLC alignment, as described earlier. In the conventional multi-layer metallization process used to fabricate mirrors on the planarized device, the via and final metal layer are deposited simultaneously in aluminum. To ensure that there is an electrical contact between the vias and mirrors layer, a 1-2μm thick layer of aluminum is sputter deposited. This meant that the mirror layer formed was excessively high. This unfortunate situation meant that the liquid crystal flow front encountered very large obstacles (gaps between pixel mirrors) during cell filling, which lead to capillary pinning [Bodammer, 1998] and may have contributed to the

flow defects, evident from the work carried out by W. Zheng [1998]. Of course, these large, high aspect ratio steps, also have huge implications for the spacer layers discussed in chapter 4.0. It was therefore desirable to develop a method of forming a mirror layer which was flush with the interlayer dielectric, *i.e.,* with no large steps. A method of patterning the aluminum pixel mirrors is currently being investigated by D.W. Calton using the damascene process, section 2.6.3, for this purpose.

Technique	Description	Comments
Planarization	Optically flat mirrors produced by SiO_2 CMP.	Excellent results achieved, under SCIOS[6] project.
Light shielding	Intermediate layer of metallization.	DRAM pixels.Under SLMDIS project.
Damascene	Aluminum CMP to produce mirrors which are flush with the substrate.	A long way from implementation.

Table 3.1 Summary of recent performance enhancing processes.

3.4.1 Issues hindering the implementation of the Damascene process

Despite the report of successful fabrication of DRAM memory devices using aluminum damascene structures, widespread adoption of aluminum damascene processes is not expected due to the immaturity of aluminum CMP processes and the rapid transition to copper damascene structures [Peters, 1998]. The major problems with aluminum CMP, figure 3.3, are;

(1) the severe dishing which tends to be worse on the large area, aluminum pixel mirrors,
(2) erosion of the oxide in the array and
(3) poor surface finish of the polished aluminum.

The poor finish of the polished aluminum comes about from scratching of the mirror surface, figure 3.4, which reduces the reflectivity of the mirrors. The culprit of some of the larger scratches was thought to be large grains of silicon dioxide which had

[6] Scottish Collaborative Initiative in Optoelectronic Sciences

been dislodged from the polish pad. In fact, although pure aluminum sputter targets were available, the aluminum targets which had been used in the past by the EMF, had contained about 1 atomic percent silicon dioxide, and this may have been a significant source of the grains [Calton, 1998].

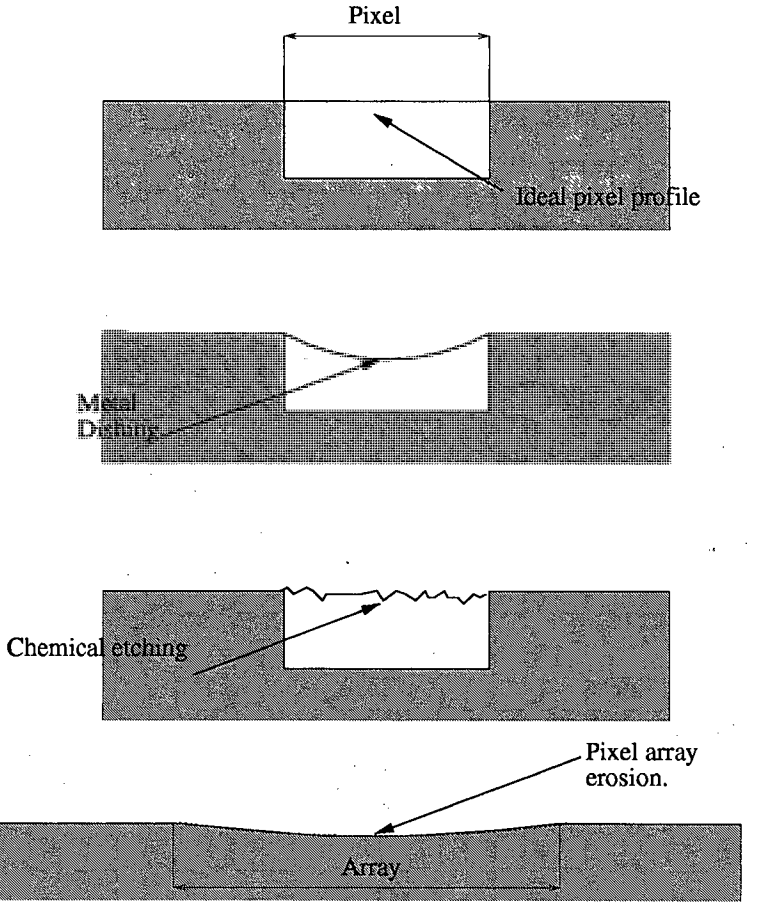
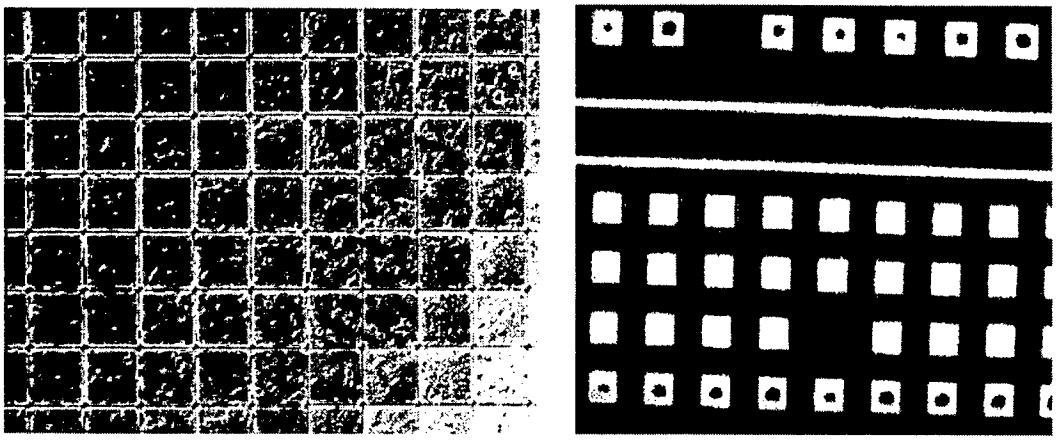


Figure 3.3 Schematic illustration of dishing, pitting and erosion.

Damascened 176x176 pixel test cells filled with FLC by Zheng *et al.* although suffering from the effects mentioned above, exhibited a surprisingly uniform alignment texture. As a more achievable alternative we have investigated the use of via polishing and thin mirrors, which will be discussed next. The initial polishing was performed on a Logitech 2000 polisher by the author and D.W. Calton, and later it was performed by D.W. Calton on the Presi 460 system. All of the investigations into the evaporated aluminum mirrors were performed by the author.



(a) (b)

Figure 3.4 Polished 176x176 mirror and bond pads. Polishing aluminum by CMP introduces (a) scratching and pitting of the mirror surface and (b) dishing (dark patches in the center of the bond pads) of the individual mirrors as well as erosion (not shown) of the array. Courtesy of D. W. Calton.

Dishing, figure 3.3, during CMP is the tendency to remove metal in preference to the surrounding harder dielectric. The polisher removes the soft metal and combined with pad deformation, the metal in the middle of a feature is preferentially removed. Dishing is defined as the difference in height between the surface of the metal at the center of the feature, which is the lowest point of the dish, and the point where the interlayer dielectric levels off, at the edge of the feature. Erosion, on the other hand, comes from the tendency of the polisher to remove the dielectric during metal polishing, i.e., the interlayer dielectric has a non-zero polish rate. This effect is more pronounced in regions with densely packed narrow regions of dielectric, such as between the pixel mirrors in a damascened SLM. It is defined as the difference in the interlayer dielectric thickness before and after polishing. Other types of polishing defects are sumarized below in table 3.2.

Oxide CMP defect types	Metal CMP defect types
Residual slurry following post-CMP cleans	Puddles
Surface voids from dislodged particles or weak points in the oxide	Surface voids
Microscratches from particles or debris	Residual slurry
Surface particles	Surface particles
	Metal-filled microscratches and
	Cored metal plugs [SCI, 1997].

Table 3.2 Other types of oxide and metal CMP defects.

3.5 The thin mirror process

As most metals in standard fabrication processes are alloyed with silicon and copper to help prevent electromigration[7] and spiking[8], the texture of the aluminum layers is somewhat grainy and not as reflective as a more pure metal electrode would be. The need exists for metallization of a higher optical quality than that available through normal wafer fabrication processing. A reduced grain size, freedom from hillocks and high reflectivity are all required. There are techniques available to achieve these, but not necessarily pursued in the industry at large as optical quality is not of prime importance. From the standard process flow described next, it quickly becomes clear why the method of depositing mirrors used is not desirable. The processed wafers received from the foundry are usually coated in a passivation layer, which may have a non-uniform thickness over the wafer. For this reason the via contacts are generally over etched to ensure that they have all cut through the passivation layer. There are generally two methods of forming the metal via plugs; selected CVD or blanket deposition and etching. As we do not have the capability of depositing metal by CVD at Edinburgh we use the latter method.

[7] Electromigration describes the movement of atoms in a metallic conductor induced by the passage of a direct current.

[8] Spiking, or pitting, is a process of mass transport across an interface that takes place in the absence of an applied bias, and results in metal penetration deep into the junction.

The vias, which now vary in aspect ratio from die to die, are filled by blanket deposition of a sputtered aluminum layer, which also serves as the top mirror electrode layer when patterned. Electrodes formed in this way have the major disadvantage of a very large step height, which leads to capillary pinning during LC cell filling [Bodammer, 1998] and possibly flow defects. To reduce these effects it was proposed that following the blanket deposition of the final metal layer, instead of patterning the mirrors, the metal is polished back to the substrate, by CMP, table 3.5, such that the only metal remaining is in the vias, and it is flush with the substrate (*i.e.*, damascened via contacts), figure 3.5. This then enables us to deposit a much thinner layer of aluminum, which has not been damaged by the polishing process.

The polished vias, like the polished mirrors still suffered from dishing, but with the vias being only 2-3μm in diameter, as opposed to tens of microns in the case of the mirrors, the dishing was much less severe. Since this work was carried out the author has discovered that a group at IBM have published a paper describing their use of polished tungsten via plugs followed by thin mirror deposition on their NLCoS SLM's [Colgan, 1998]. However due to the higher resistivity of W compared to Al (ρ_W=7-8μΩcm and ρ_{Al}=3-4μΩcm respectively) and problems that arise from the W/Al interfaces, there is now an emphasis on replacing tungsten plugs with aluminum alloys.

The final mirror layer deposition method need not be limited to sputtering, as it has been in the past. Indeed deposition by evaporation, 2.1.1, produces purer and hence higher optical quality films than sputtering [Levinstien, 1949]. The surface roughness of aluminum films varies with sputter conditions and film thickness [Lee, 1996], [Nagata, 1995]. The aluminum grain size, which affects the reflectivity of the layer, may be reduced by limiting the film thickness [Colgan, 1998]. Also as a general rule an evaporated metal film will be more pure and less granular the more rapid its formation [Holland, 1961]. The reflectivity of an aluminum film can be related to its surface roughness by equation 8.

$$R \propto e^{-\left(\frac{4\pi\sigma}{\lambda}\right)^2} \qquad (8)\ [\text{Campbell, 1996}]$$

if $\lambda >> \sigma$.

Where R is the reflectivity of the surface, σ is the rms roughness and λ is the wavelength of the incident light.

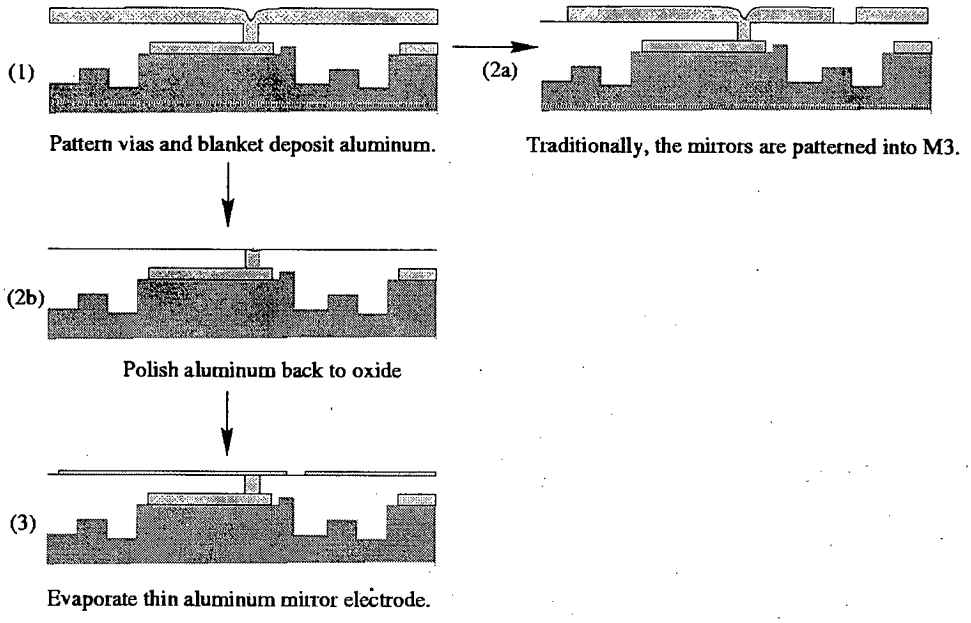


Figure 3.5 Via plug polishing. Note no additional masking steps are required as in the case of the damascened mirrors.

Some advantages and disadvantages of sputtered and evaporated aluminum films deposited "in-house" are summarized in table 2.2.

Wafers for thin-mirror process development

Product SLM wafers were very expensive, so the development of this post-processing technique necessitated the use of dummy wafers processed in such a way that they mimic the surface of the actual SLM wafers. This was achieved as follows:

- Four inch silicon wafers are coated with 0.5μm of compacted oxide, using the Oxford Plasma Technology ECR-PECVD reactor, table 3.3.
- Wafers coated with photoresist and patterned.
- Vias were then etched, in the usual manner, with the Plasmatherm PK2440 RIE (5.6.4).
- Resist de-scum in asher.
- 1μm of aluminum was sputter deposited, with the Balzers BAS 450 sputterer, onto the wafers filling the vias. A cross section of a via on the finished wafer is shown in figure 3.6.

SiH_4/He flow rate	100sccm
N_2O flow rate	35sccm
Ar flow rate	30sccm
RF power	180W
Microwave power	350W
Magnets 1& 2 current	120A, 65A

Table 3.3 Compacted oxide deposition recipe for Oxford plasma technology ECR-PECVD reactor.

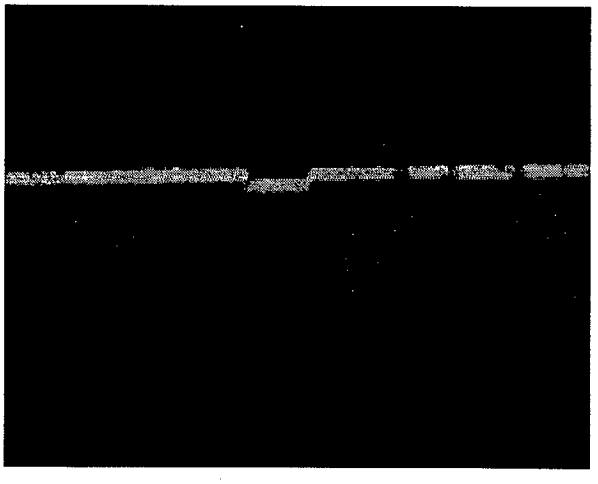


Figure 3.6 Cross section of a 5μm wide aluminum filled via hole (~1μm deep), etched into an oxide layer.

3.5.1 Preliminary experiments into polished vias

The early experiments, which we had carried out, into polished vias were performed using a Logitech PS2000 polishing system with reasonable results, figure 3.7 and 3.8. The recipe used in these early experiments is described in table 3.4.

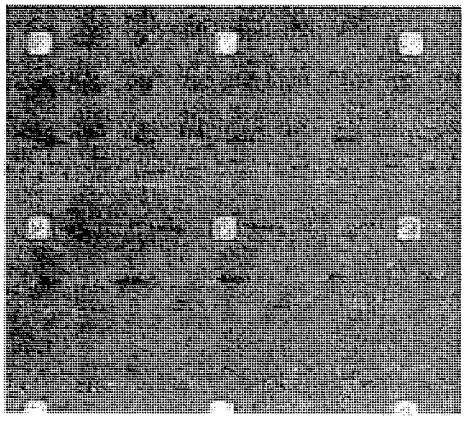


Figure 3.7

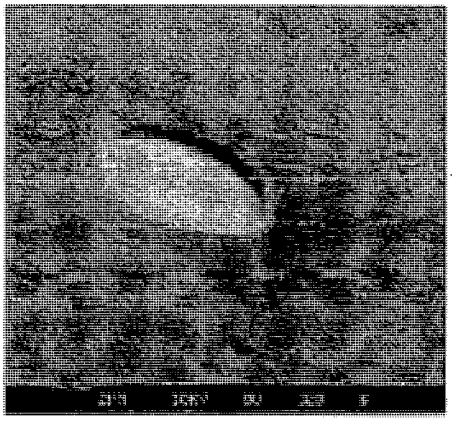


Figure 3.8

Figure 3.7 Optical micrograph of a small section of polished 256x256 SRAM vias. The pitch between the via plugs is 40μm.

Figure 3.8 SEM of an individual polished (Logitech system) aluminum 5μm wide via. Note the dishing.

The in-house CMP experiments, using a Logitech PS2000 polisher, for both metal and oxide polishing were plagued by scratching, poor uniformity, planarity, and repeatability. The scratching issue was dealt with by ensuring that all consumables were thoroughly cleaned prior to use. The slurry autofeed components were cleaned and rinsed ensuring that no loose dried slurry agglomerates were present, which could find their way onto the polish pad. The polish pad, which clogs up during material removal, was conditioned before use. In our first attempt at polishing aluminum a new pad was used, see table 3.5. Little could be done regarding the uniformity and planarity of polishing with this system. Following polishing the wafer was given a post-polish buff by replacing the slurry feed with de-ionized (DI) water and allowing the platten to continue to rotate for ~1 minute. The wafer was then removed and the wafer holder replaced by a stainless steel ring to clean the pad. The machine was allowed to run for about 1 hour, with a constant supply of DI water, to ensure that the

pad was thoroughly cleaned and that all potentially damaging particles were removed. The machine was then switched off and all surrounding surfaces wiped down with clean tissues to prevent the drying slurry from flaking off and contaminating the pad.

Logitech PS2000	
Slurry	~95g ammonium persulphate (oxidizer) & 100ml of ultra fine (0.05μm) Al_2O_3 powder in 500ml DI water.
Pad	Rodel Politex Supreme
Platten speed	~70 rpm
Wafer/pad pressure	~ 0.5 PSI

Table 3.4 Aluminum polishing parameters. The polish duration is typically 0.5-1hr. depending on the initial film thickness. The wafer is inspected periodically, with increasing frequency as the oxide layer starts to "break" through the aluminum. Note: the slurry is continuously rotated in the auto-feed to prevent the particles from settling.

Aluminum CMP on the Presi 460 polisher, preliminary results.

Since these initial experiments the new Presi 460 polisher was aquired, at the end of this study, by the department, and the new machine provided much more controllable and reproducable results. Evaluation damascene mirror samples polished by Presi exhibited very little dishing, only 600 Å over an 80μm bond pad, but the oxide in the high feature density regions of the arrays had eroded by about 0.12μm [Calton, 1998]. The vias should not have this problem as the feature density is very low. Also Kallingal *et al.* [1998], have recently aquired data which shows that the dishing of aluminum patterns increases in a non-linear manner with feature width. The polishing pad used, by Presi, was a rigid IC1400[9] stack from Rodel, rotated at low speed (~20rpm) and with light down force on the wafer (~0.5bar over a 4" wafer) [Calton, 1998].

[9] IC1400 is a stacked pad composed of an IC1000 (rigid microporous polyurethane material) and foam base.

3.5.2 Pre-deposition substrate cleaning

The main disadvantages of evaporated aluminum films in this process was its poor adherence to the silicon dioxide substrate. To obtain the most durable and adherent coatings on SiO_2 the surface had to be free from contaminant films such as grease, absorbed water, *etc.* Various methods exist for removing gross surface contaminants, but they are not capable of freeing the substrate from mono-molecular films of water, and hydrocarbons [Holland, 1961]. On exposure to the atmosphere, even for a short period, the surfaces rapidly become dirty. Such surface contaminants condensing from the atmosphere, or remaining after chemical cleaning can be removed from substrates prior to deposition by raising the temperature of the substrate under vacuum, or by exposing the surface to bombardment of high velocity ions. The final mirror metallization should be capable of withstanding the spacer layer fabrication, described in chapter 5. As the final stage in the fabrication of the spacers involved ultrasonic scrubbing in solvents and DI water/Neutracon (@60°C), it was decided to use this as a qualitative measure of the films adherence to the substrates. It was found that with no pre-deposition plasma clean, the aluminum film peeled away quite drastically, figure 3.9, whereas films deposited onto substrates held in the air plasma for > 20 minutes, prior to film deposition, exhibited much less damage.

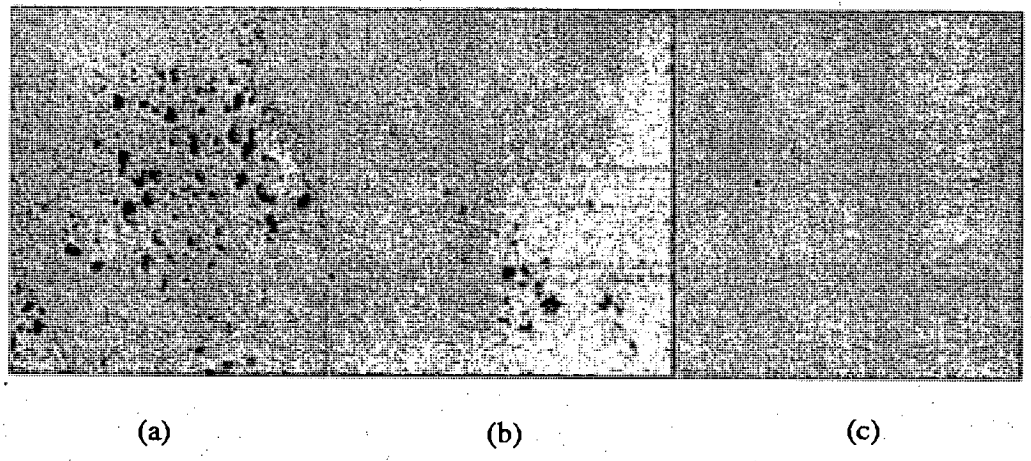


Figure 3.9 500 Å aluminum evaporated onto a silicon wafer and scrubbed for 10 minutes (a) with no pre-deposition clean, (b) with 10 minutes pre-deposition clean, and (c) with 20 minutes pre-deposition clean. In future an argon plasma may be used to obtain cleaner surfaces.

3.5.3 Thin mirror deposition and patterning

As discussed at the start of the section, evaporated aluminum films produce extremely high optical quality mirrors and in fact evaporated aluminum films are frequently used for front surface mirror coatings [Kingslake, 1965]. Following the via plug formation and substrate cleaning the aluminum mirror layer was deposited. With the current polishing characteristics the vias and importantly, the local aligning marks were quite visible through the thin aluminum layer. It was important that these aligning marks remained visible even after the polishing optimization to reduce the dishing, erosion, scratching *etc.* Fortunately these defects, which had dissuaded the semiconductor industry from using polished aluminum, were likely to remain to an extent, in the larger features such as the aligning marks, figure 3.10. This produced an aligning target which had a contrast high enough for the stepper to detect. Following the blanket deposition of the aluminum, the wafer was coated with photoresist and patterned in the usual manner, described later.

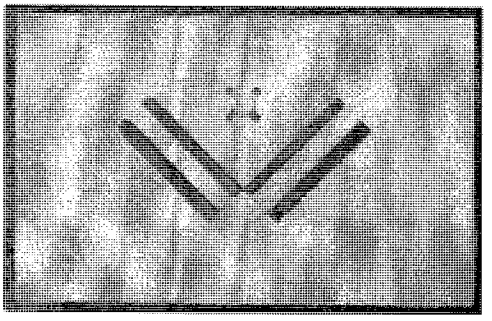


Figure 3.10 Damascened aluminum aligning mark with overlying evaporated mirror layer aligning mark.

3.5.4 Characteristics of thin mirrors deposited by evaporation

For the purpose of cell filling (LC alignment) and spacer layer fabrication (4.0) the more flush the the mirror layer is with the substrate the better. Unfortunately, if the aluminum mirrors are too thin they will no longer be completely opaque to the indident light. This results in a loss in the reflectivity of the mirror as well as an

increase in the transmittance of the incident light into the underlying circuitry, 3.2. To determine the minimum acceptable thickness, in terms of light transmission/ reflection, various thicknesses of aluminum were evaporated onto glass slides. The relative film transmittances were measured with a 10mW HeNe laser and photodetector (type OSI5K Centronic), as illustrated in figure 3.11. We found that the minimum thickness of the evaporated aluminum mirrors, before the transmittance started to increase rapidly, figure 3.12, was ~25-30nm, but ideally the mirrors should be around 60-70nm thick to be completely opaque at 632nm. This value was significantly less than the thickness suggested by Colgan *et al.*, who stated a lower limit (dictated by agglomeration of the film during annealing) of 150nm [Colgan, 1998].

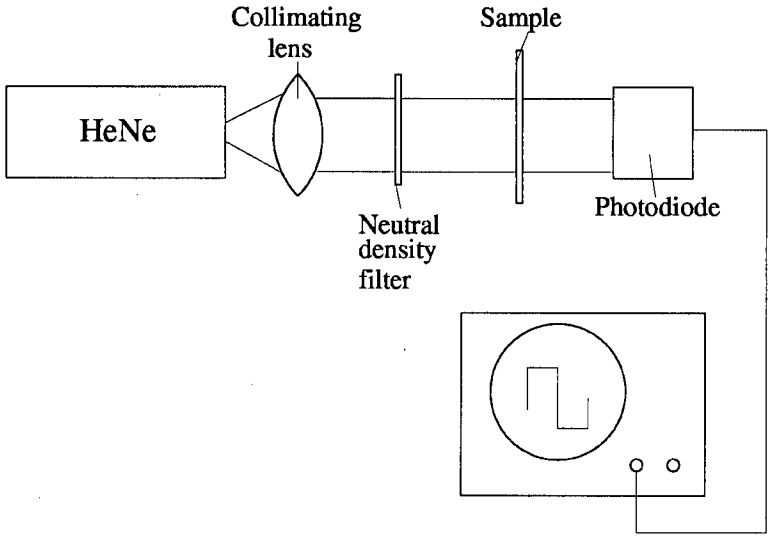


Figure 3.11 The intensity of the incident HeNe on the sample is set to a level which prevents the photodiode from saturating.

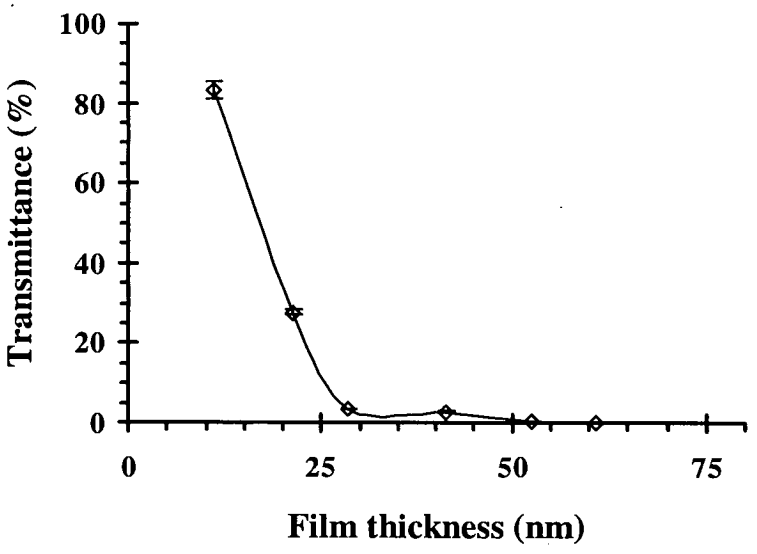


Figure 3.12 Evaporated aluminum film transmittance vs. thickness (λ=632nm),which is in close agreement with Walkenhorst [1941].

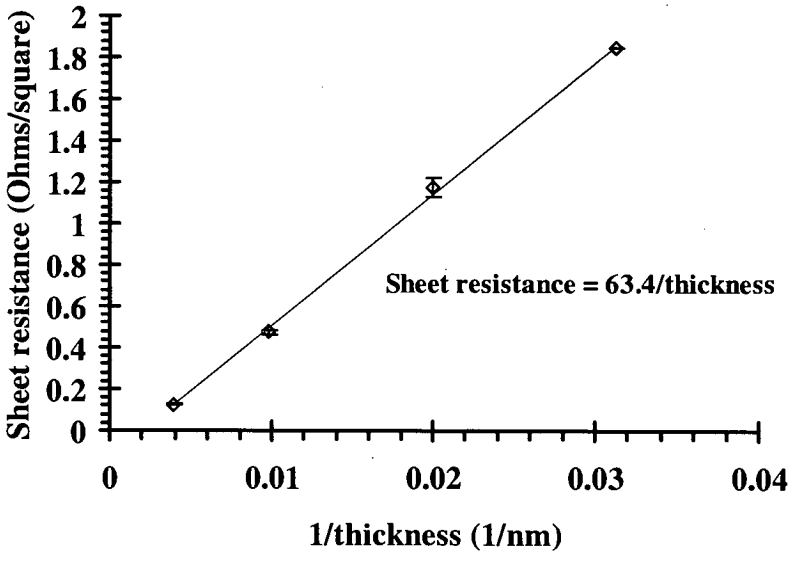


Figure 3.13 Sheet resistance of an evaporated aluminum film as measured by Veeco Inst. Inc. FPD5000 four point probe.

Obviously the thinner the Al film, the greater the light transmission and the higher the film sheet resistance. From figure 3.13 we see that an evaporated Al electrode thickness of 50nm has a corresponding sheet resistance of 1.1Ω /square[1], which is about 60 times higher than that of the 1-2μm sputtered aluminum used for conventional mirrors. One should, therefore, be mindful of all the effects mentioned above when deciding on the pixel mirror electrode thickness, as a gain of a better liquid crystal alignment may be offset by poor switching characteristics.

Another concern regarding evaporated aluminum films is that of thickness uniformity. When the film is deposited at high rates, the vapor pressure in the region immediately above the source can be high enough to place the region in a viscous flow regime. Operation in this regime affects the deposition uniformity by creating a virtual source at some distance above the filament.

The reasons for being concerned with the thickness uniformity of the aluminum over the wafers were as follows;

1) Thickness non-uniformities in the mirror layer may alter the FLC layer thickness, assuming that the cell gap thickness of the cell is set from the planarized oxide layer.
2) We need to be sure that the mirrors are optically opaque over the entire wafer.
3) The sheet resistance of the mirrors may vary across the wafer.
4) The optical quality of the mirrors is dependent on the evaporation rate of the aluminum, which in turn affects the uniformity of the deposit.

To obtain the best uniformity[2], the evaporator must be run at low rates and these low rates require an extremely high vacuum to avoid contamination of the film. The E306 aluminum evaporator was characterized to determine the uniformity of deposition at various deposition rates. This particular evaporator was very difficult to control, as it had no feedback control, and as such the results obtained must only serve as a guide. Three 4-inch diameter wafers were coated with aluminum to approximately equal thicknesses, as shown below, at the power settings indicated. The deposition times

[1] Typical sheet resistance of commercially available ITO film (45nm thick) is 60Ω/sq, see appendix B.

[2] Both the angular dependence of the emission law (~cosφ) and the orientation of the film-gathering surface contribute to uniformity problems.

were recorded and the thicknesses of the films were calculated from the sheet resistance values obtained at the three locations, the center the edge and midway between the center and edge, of the wafer, using a four-point probe, figure 3.14.

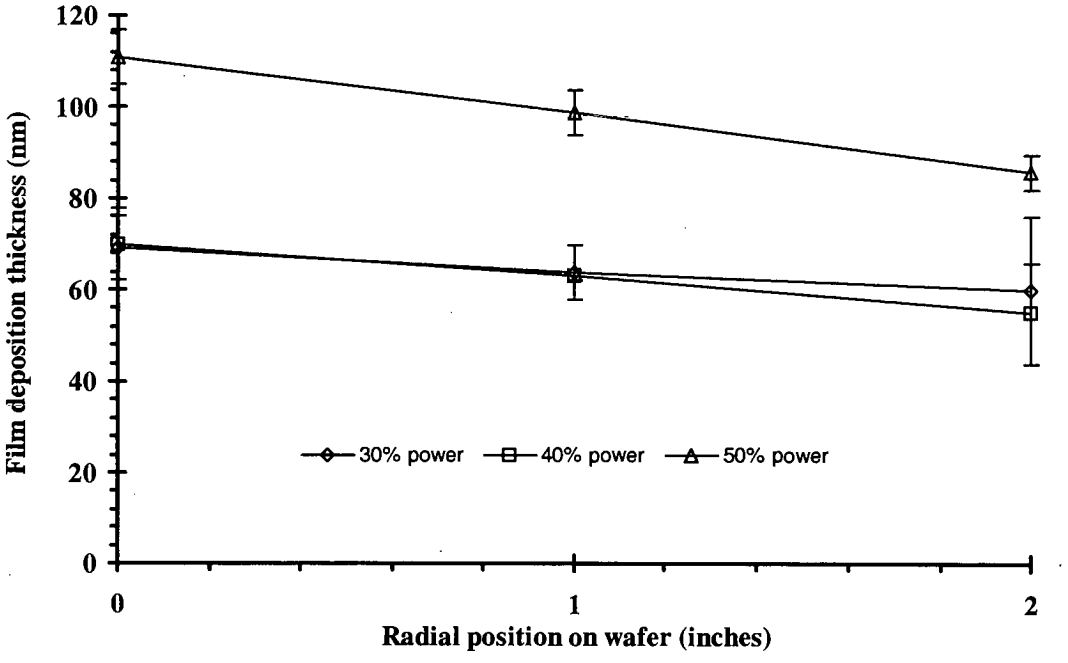


Figure 3.14. Evaporated aluminum thickness uniformity across a four inch wafer.

Low tension power supply (%)	30	40	50
Average deposition rate (nm/s)	1.6 ±0.13	3.7 ±1.1	23.7 ±3.6
Average %age uniformity	7.2	11.8	12.4

Table 3.5 Evaporated aluminum film thickness uniformity versus film evaporation rate. Note that in increasing the aluminum evaporation rate from 3.7nm/s to 23.7nm/s there was only an very small decrease in the deposition uniformity.

From the results above in figure 3.14 and table 3.5 we see that evaporation at very low rates yields the best thickness uniformity, but at higher rates (which would provide the best optical quality films) the film uniformity was much poorer, but remains fairly constant.

It can be seen that the deposition non-uniformity (over a 4"diameter wafer), with the Edwards system, would not adversely affect the transmission of the aluminum. For example, using the results shown in figure 3.12, we saw that an aluminum thickness

of >35nm was required for the mirrors to be optically opaque. If the aluminum was evaporated, to this thickness, at a high rate, to produce the best optical quality mirrors, we could expect the thickness at the edge of the wafer to be ~27nm. This would give a variation in the aluminum thickness of only 7.7nm over the entire 4" wafer. LC thickness variations of 7.7nm are negligible. It was therefore possible to evaporate the aluminum at high rates (~20nm/s) without being concerned by the thickness non-uniformity. Of course with future batches possibly being fabricated on the larger 6" diameter wafers it will not be physically possible to coat the wafers by evaporation using the present Edwards system, and the disscussion above will not apply. To coat these larger diameter wafers it will be necessary to aquire a larger evaporator system with a rotating substrate holder.

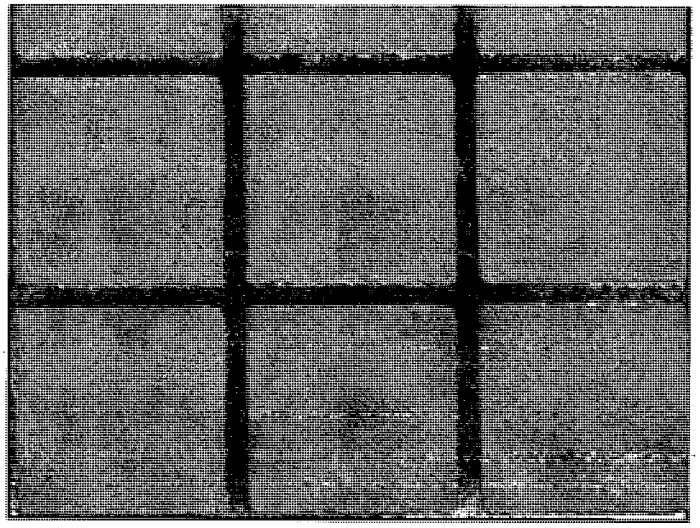


Figure 3.15 Optical micrograph of the new thin (50nm) evaporated aluminum mirrors over polished vias.

Following metal patterning the mirrors were examined, figure 3.15, with a phase contrast microscope. Bearing in mind that this sample was a first attempt at polishing aluminum via plugs on the new Presi polisher a visual inspection of the vias showed that they were barely visible, compared with the planarized 512x512, figure 3.1(b). Also the evaporated aluminum mirrors in this particular case were wet etched, real LCoS mirrors will be etched in an anisotropic dry etch where there will be very little if any under cutting of the photoresist. As the metal was polished back to the oxide, it should be possible to sinter the aluminum (which had proved problematic in the past)

before CMP, to improve the electrical contact of the vias to metal 2. No additional ECR oxide capping layers, discussed in 3.2, would be required during this sintering process.

3.5.5 Inter-pixel mirror gap filling

As with conventional 1-2μm thick mirrors the problem of capillary pinning, figure 3.16, and the subsequent destruction of the linear LC flow front could still be seen on the thin mirrors, albeit, to a lesser extent, figure 3.24. This linear flow front is important as the alignment of NLC's, under certain conditions, has been reported to be along its flow direction during cell filling [Mi, 1998]. The anchoring of nematics on a solid substrate, in most cases, is determined during the wetting of the substrate by the nematic liquid crystal [Jerome, 1988]. As reported by Bodammer [1998], capillary pinning, figure 3.25, could be avoided by eliminating the trenches between the pixel mirrors.

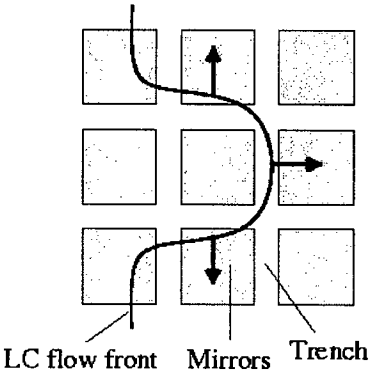


Figure 3.16 The LC filling the cell fills along one column of pixels mirrors before proceding to the next column of pixels.

Prior to the thin mirror development, researchers in the Applied Optics Group, including the author, had contemplated the problem of the deep inter-pixel trenches present on conventional mirrrors. Any method involving lift-off to fill the 1-2μm deep trenches was considered by the author to be impractical due to the photoresist step coverage (defined in 2.5.2) problems, and was therefore dismissed.

Since the thin mirror technology became a likely candidate to replace conventional mirror processing techniques (planarized), I proposed a novel technique of filling the trenches, see figure 3.17, using the existing, unaltered, photoresist layer used in patterning the aluminum. In the following investigations, the backplane preparation was performed by the author and D.W. Calton and the cell construction and filling was performed by the author.

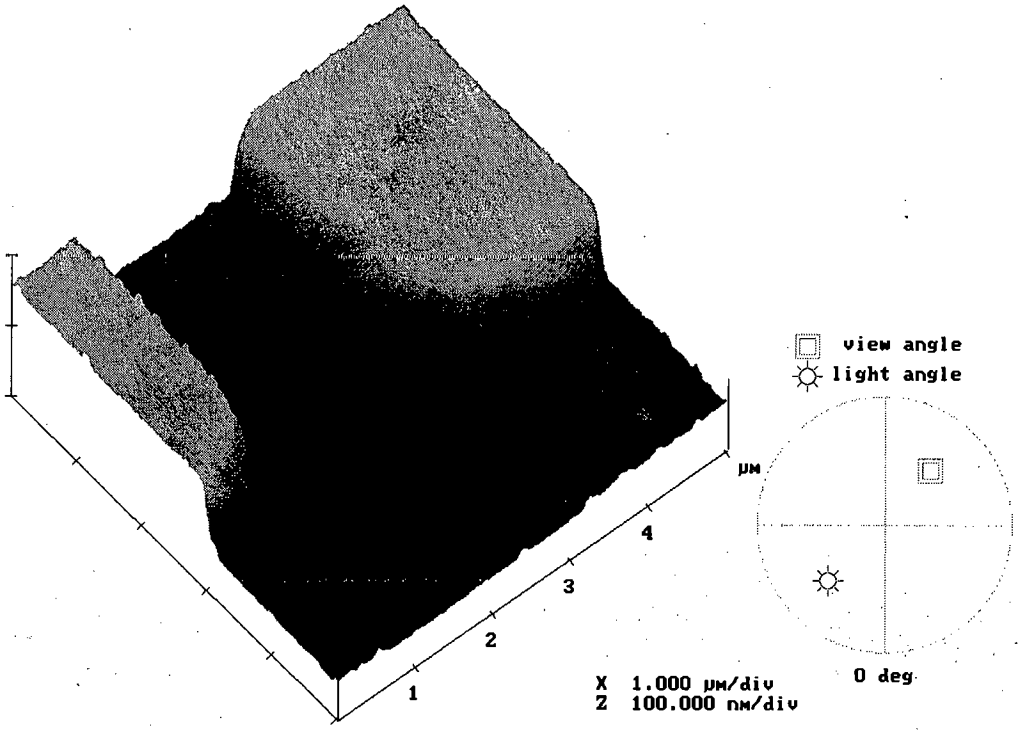


Figure 3.17 AFM image of the trench between the "thin" mirrors. Note the z scale is 100nm/div. Courtesy of D.W. Calton.

The idea behind this technique was to deposit oxide/dielectric material over the patterned wafer in a lift-off process (which is still coated with the photoresist from the mirror patterning), figure 3.18, to a thickness equal to that of the thin mirrors. As the mirror layer and hence the required oxide layer deposition were very thin (~1/10th the thickness of the photoresist) there would be very little step coverage of the 1.2μm thick PR layer from the oxide, which would enable removal of the photoresist. This technique will be referred to as the Self-aligned Insulator Filled Trench (SIFT) process, from this point forward.

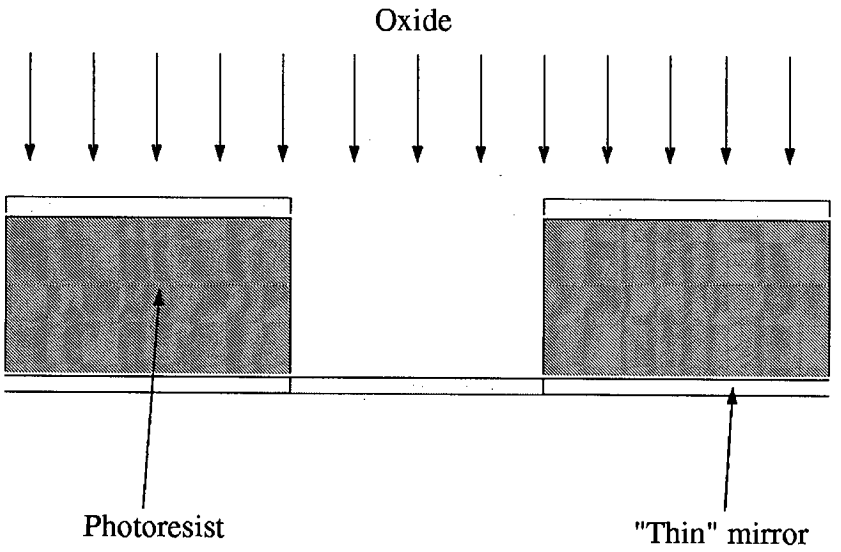


Figure 3.18 Crossectional illustration of mirror gap fill process. Drawn approximately to scale.

Experimental

As a proof of principle, a dummy 4" wafer was coated with 80nm of evaporated aluminum and the layer patterned with the 512x512 mirror mask. Evaporated SiO was chosen by the author in the first instance due to its poor step coverage, which lends itself to the "lift-off" process. Later experiments by D.W. Calton justified the authors descision for using evaporated SiO rather than ECR-PECVD SiO_2. Following wet etching of the aluminum the wafer was diced to provide samples for experimentation.

The silicon oxide was deposited by evaporation, using the Edwards Auto306 system. The samples were held ~110mm above the source, and the SiO_x evaporated at a rate of 0.75nm/second.

The sacrificial photoresist, which was also used in patterning the mirrors, was then removed by one of two methods;

(1) oxygen plasma ashing

(2) ultrasonic scrubbing in acetone.

The samples were then examined optically and using a surface profileometer, Sloan Dektak 200-Si. From the first run it was found that the photoresist on the samples stripped in the asher had been removed, but the overlying oxide remained. The second set of samples, on the other hand, which had been scrubbed in acetone were completely free of the unwanted oxide, figure 3.19. Following examination with the Dektak it was discovered that the oxide deposited in the first run was too thick (~2000 angstroms), subsequently the duration of the evaporation on the second run was reduced by 2.5 times in an effort to hit the target thickness of 800 angstroms. Upon examining the samples from the second run it was found that the oxide filled trench was much closer to the mirror layer, figure 3.20(a).

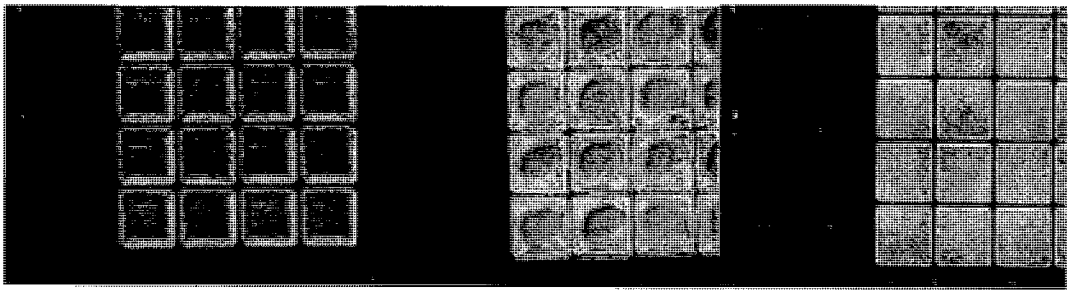
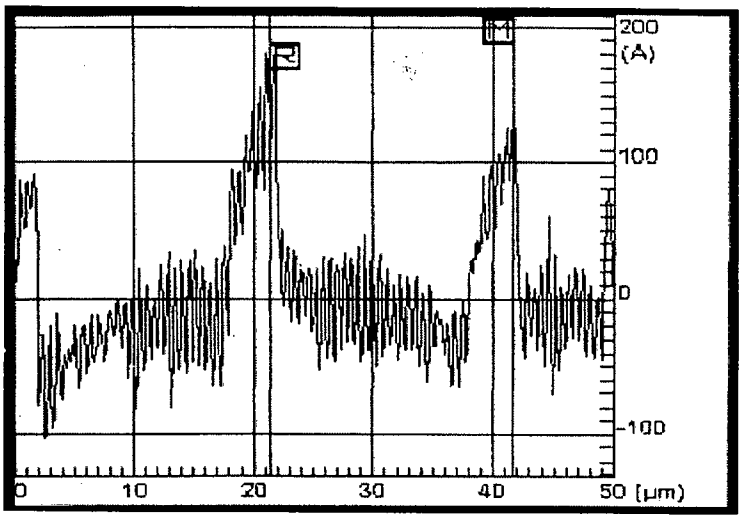
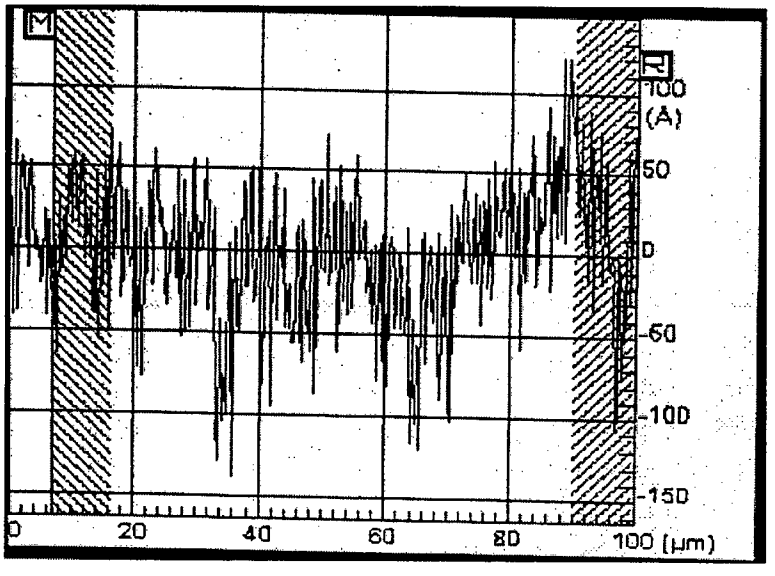


Figure 3.19 Optical micrographs of a corner of the mirror array showing the various stages of overburden removal. The picture on the left of the figure shows the mirrors before scrubbing in acetone. The picture in the middle shows photoresist begining to clear from under the silicon oxide. The final picture, on the right, shows the mirrors when they have been fully cleaned.

It was found that the deposition thickness of the evaporated silicon oxide was independent of the feature size, unlike the ECR-PECVD silicon dioxide, in which the deposition thickness did vary with feature size (see chapter 5). In the case of the evaporated silicon oxide layer the thickness of the deposit was the same in the array (between the pixel mirrors) and outside the array on the relatively bare parts of the die.

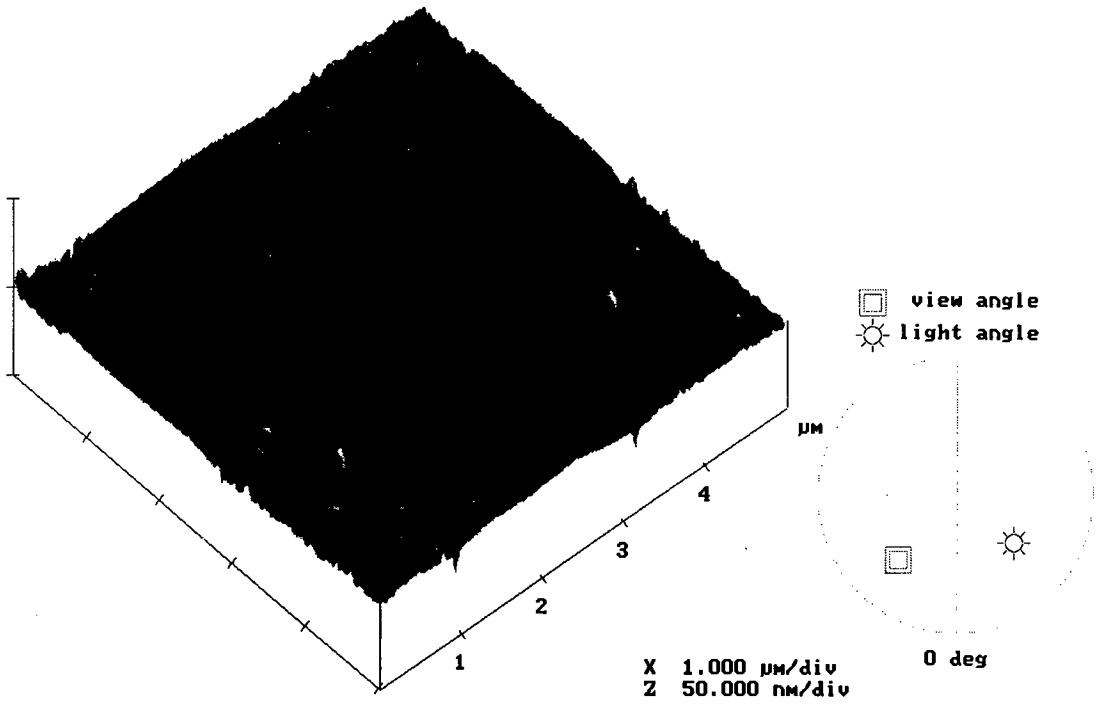


(a)



(b)

Figure 3.20 (caption below)



(c)

Figure 3.20 (a) Surfaceprofileometer trace of mirrors from the second run in which the oxide deposition is only ~10nm above the mirror array, (b) from the third run in which the "trench" is indistinguishable from the mirror layer, (c) AFM image of (b). Note the z scale is 50nm/div.

A third run was the performed in which the deposition time was further reduced, figure 3.20(b&c). Upon examination, again with the Dektak, all that could be seen was noise, *i.e.*, the "trenches" and mirrors could not be identified.

3.5.6 Improvement in the evaporated film thickness uniformity

In the experiments described so far, the SIFT processed was performed on a die scale. This enabled us to obtain the desired silicon oxide thickness and thickness uniformity over the device, but risked particulate contamination between the mirrors. In order for the SIFT process to be performed on a wafer scale the deposition uniformity had to be improved.

We had seen that evaporated silicon oxide produced a much more planar surface profile in filling the inter-pixel gaps than ECR-PECVD silicon dioxide. The deposition rate in the evaporator depends on the location and orientation of the wafer in the chamber. So in an effort to improve the evaporated oxide deposition thickness uniformity an extension to the Auto306 chamber was used, figure 3.21.

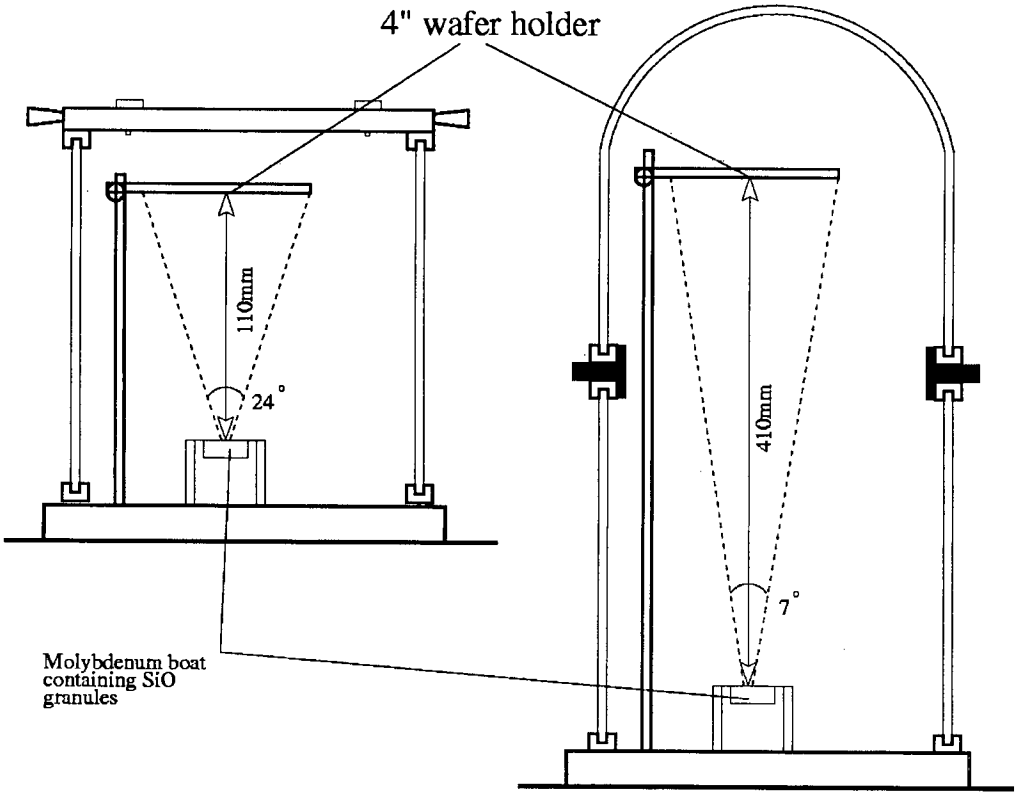


Figure 3.21 Extension of the distance between the wafer and the source.

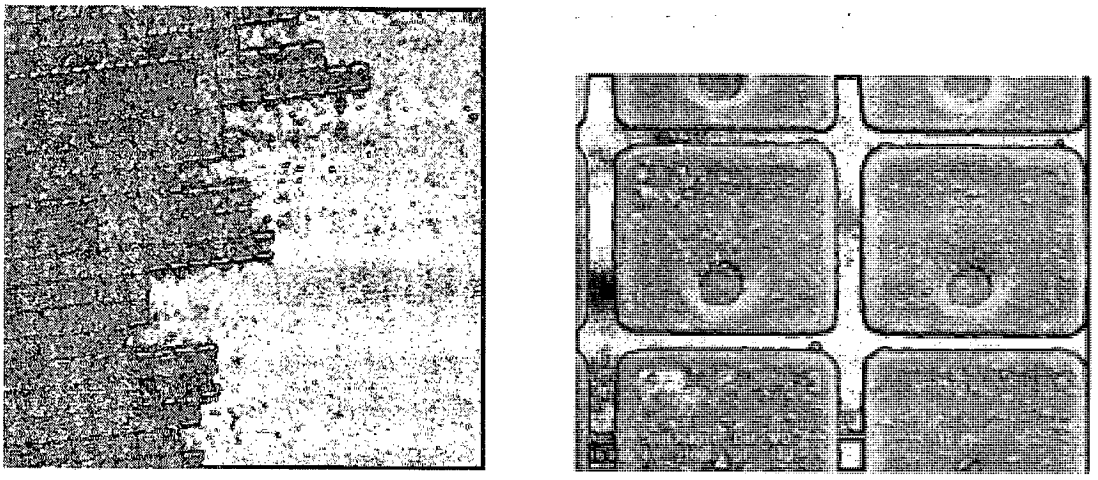
By extending the distance between the wafer and source from 110mm to 410mm, it was found that the silicon oxide deposition thickness non-uniformity was reduced from >12% to 2.7%, respectively, over a 4-inch wafer.

3.6 Cell construction and filling with Nematic liquid crystal

A selection of backplanes, including the new SIFT processed backplanes, were used in the construction of test cells to observe the effect of the surface topology on the LC flow front. The cells were constructed with 3.1μm spacer rods in Norland adhesive type NOA88. The empty cells were placed under a polarizing microscope, type Olympus BH2-UMA with a JVC TK-1070E RGB video camera, with the polarizers crossed and a small quantity of NLC (Merck E7) placed at the cell opening, at room temperature. The LC cell filling was then observed, with the 20X microscope objective. The images were "grabbed" using the Computer eyes/RT software.

Conventionally processed backplanes

Initial observations of the LC flow front over the conventional mirrors, figure 3.22, were slightly different to that which we had expected. The LC flow front was observed to propagate preferentially along the rows of pixel mirrors rather than along the columns as described earlier. It had been suggested that the surface roughness of the 2μm thick mirrors may have been the cause for this unexpected filling phenomenon. To test this speculation an oxidized silicon wafer was coated with 2μm of aluminum and given a superficial polish on the Presi 460 before patterning. The cells constructed and filled using these backplanes then exhibited the predicted LC flow front shape, figure 3.23.



(a) (b)

Figure 3.22 (a) Conventional "thick" mirror 512x512 SLM being filled, left to right. (b) SEM of the pixels mirrors. Note that poor quality mirrors such as this were a common occurrence (cell filling from left to right).

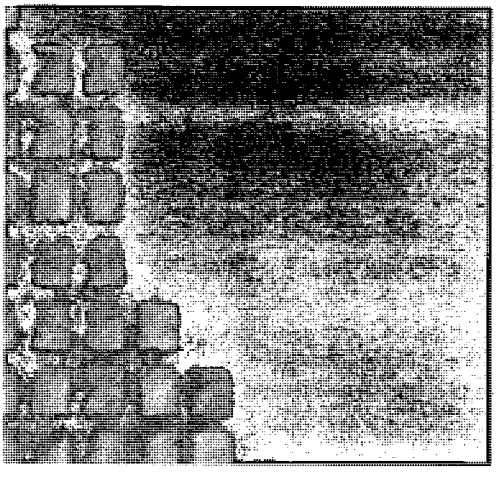


Figure 3.23 LC flow front over polished "thick" mirrors. The LC fills the columns (bottom to top) before progressing to the next column (cell filling from left to right).

Thin mirror backplanes

The LC flow front over the thin mirrors, figure 3.24, with 80-100nm deep inter-pixel trenches was much less severe than that of the conventional mirrors, above.

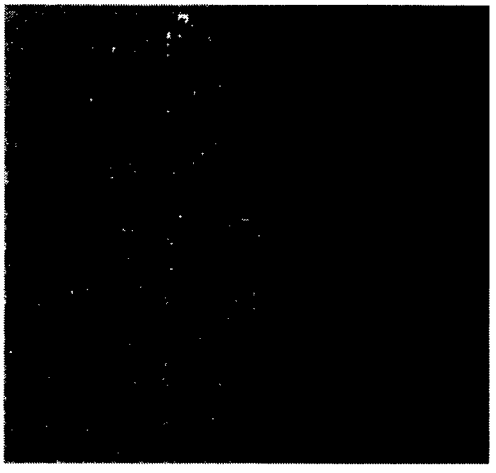


Figure 3.24 A device with thin 512x512 mirrors (no SIFT processing) being filled with NLC. Although the wave front is not disturbed nearly as much as the LC over the conventional mirrors, a disruption can still be observed (cell filling from left to right).

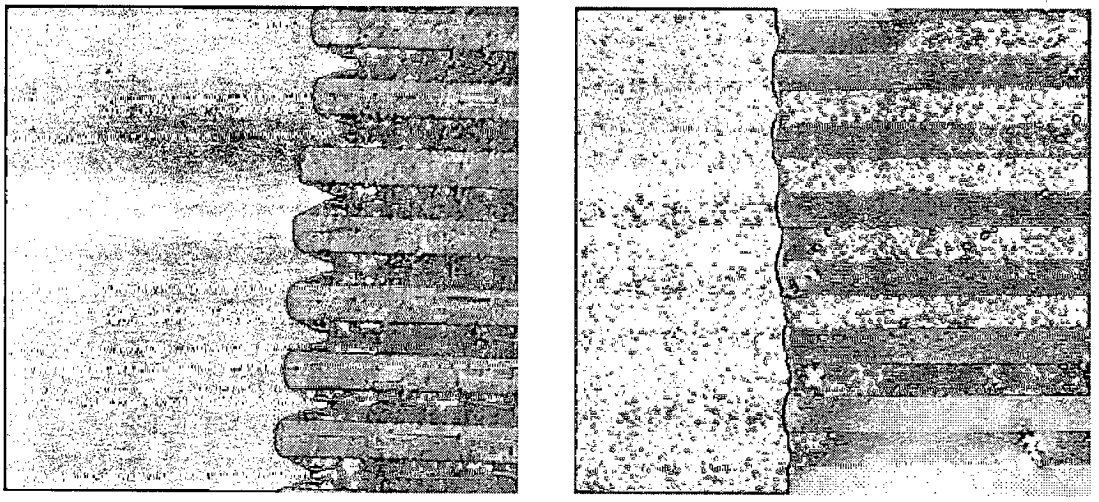
SIFT processed thin mirror backplanes

Finally, the cells constructed using the SIFT processed backplanes were examined. The LC flow front propagating over the mirrors was seen to progress both parallel and later diagonally to the mirror sides, figure 3.25, in the desired manner *i.e.,* with no sign of the capillary pinning reported earlier.

Figure 3.25 SIFT processed thin 512x512 mirrors NLC filling the cell from left to right and filling from bottom left to top right. Note that the flow fronts appear to be unaffected by the pixellated backplane.

3.7 Aluminum vs. silicon dioxide wetting by LC

As the surface topology variations had been almost completely removed, we wanted to know what effect the differing substrate material properties would have on the LC flow front. The oxide layer between the mirrors of the SIFT processed backplanes were very narrow, typically 2-3μm wide and it was therefore impossible to satisfactorily observe the LC flow front over the oxide with the equipment available. To enable us to observe the effect of the differing substrate materials on the LC flow front velocity a silicon wafer coated with SiO_2 was patterned with 30nm thick aluminum gratings (with a pitch of 100μm). Test substrates were cleaned using the standard process and cells constructed with rubbed Poly(vinyl alcohol) (PVA) coated cover glass and 3.1μm spacers. It was repeatedly observed that the LC flowed preferentially along the aluminum rather than the SiO_2 strips. It appeared that the LC propagating along the aluminum strips caused a flow front to spread out across the oxide leaving a visible LC contact line at the center of the SiO_2 strip.



(a) (b)

Figure 3.26 E7 filling 3.1μm cell gap with 200μm wide (30nm thick) aluminum grating backplane (a) with an alignment layer on coverglass only and (b) with an alignment layer on both the coverglass and silicon backplane (filling from right to left).

It was clearly evident that the NLC (E7) preferentially "wet[3]" the aluminum surface.

[3] Contact angle between the liquid and the substrate is <90°.

The average speed (appendix D) of the LC flow front, filling the cell, is highly dependent on the substrate material and, for a specified substrate material, is given by

$$\bar{v} = \frac{(\gamma_{sv} - \gamma_{sl})}{6\eta l} d \qquad (9) \qquad \text{[Mi, 1998]}$$

Where γ_{sv} is the surface tension at the substrate-air interface, γ_{sl} is the surface tension at the substrate-LC interface, η is the translational viscosity coefficient of the LC, l is the length of the LC cell and d is the LC layer (cell gap) thickness. On examination on cells filling which had a rubbed PVA alignment layer on both the coverglass and silicon backplane the wetting differential was much less pronounced. In fact, the non-linearity of the flow front may have been caused by the slight undulations in the silicon substrate topology, due the the very thin aluminum strips. Unfortunately we were unable to measure the LC flow front speed due to the limitations of the video equipment. From these observations we see that it may be benificial to apply the LC aligning layer to the silicon substrate rather than the coverglass. Furtherwork is required to evaluate any potential gains in LC aligning quality before any conclusion can be drawn.

3.8 Preliminary investigations into cell filling with FLC

Although NLC's are relatively easily aligned, the alignment of FLC's is a much more formidable undertaking. Cells, such as those described earlier, were filled with FLC (CS-1031) in its isotropic phase. The cells were filled and the flow fronts observed by placing a "blob" of FLC material at the opening of the cell and heating the device on a hotplate (to allow the FLC to reach its isotropic phase). When the cell was approximately half filled, the device was carefully lifted from the hotplate and allowed to cool.

The FLC flow front over the conventionally processed backplanes was, as in the case of the NLC, severely disrupted. The FLC flow front over both the "thin" mirrors and

SIFT processed "thin" mirrors were, however, very difficult to differentiate, *i.e.*, the flow fronts were similar to that of NLC over the "thin" mirrors. This suggested that the wetting properties, viscosity and, in particular, the phase of the LC materials used may be very important in determining the quality of the flow front in the cells.

Another relevant observation was noted on conventional mirror electode cells filled with FLC, which has previously been reported [Blinov, 1983], [Bodammer, 1998]. The wavefronts shown in the figures below were preceded, by a much thinner (~20nm) [Bodammer, 1999] wetting layer, figure 3.27.

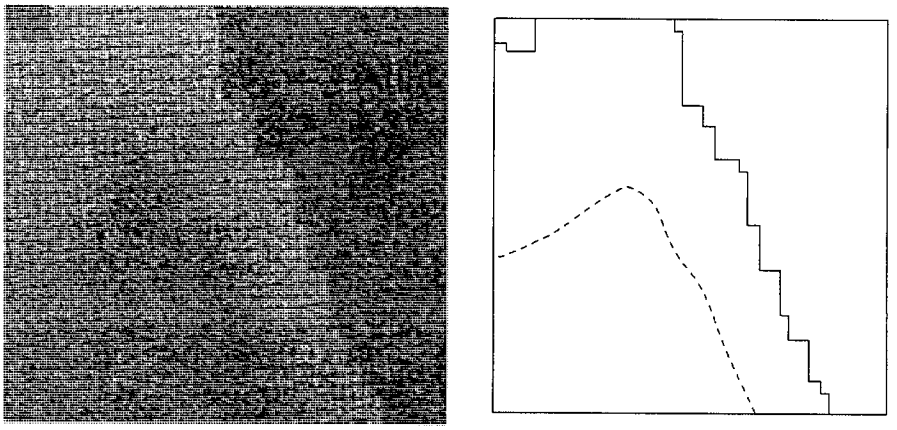


Figure 3.27 Although in its isotropic phase, the FLC can clearly be seen filling the cell gap from right to left (solid line). Not so clear is the "precursor" film (dashed line) which extends 5-10 pixel mirrors ahead of the main wave front, which may influence the orientation of the bulk FLC during filling.

3.9 SIFT experiment summary

The important findings from the SIFT process investigations were that;

1) The photoresist used in patterning the "thin" mirrors could be used as a sacrificial mask for patterning the subsequent silicon oxide layer, filling the inter-pixel trenches.

2) The photoresist was easily removed following silicon oxide deposition (evaporation) by ultrasonic scrubbing in acetone.

3) The evaporated silicon oxide films suffered from adherence problems (so a pre-deposition plasma clean is required) but an AFM investigation of the filled trench revealed an extremely planar surface (rounding of only 2.5nm from the center to edge of the filled trench).

4) ECR-PECVD silicon dioxide was found to be sufficiently adherent to the substrate, but the silicon dioxide deposited in the gap was severely domed and burrs were present (21.8nm rounding).

5) The technique had been demonstrated to completely fill the inter-pixel gap.

6) The shape of the NLC flow front, which is extremely important for good LC alignment, was undisturbed by the mirror array, when the SIFT process was used in conjunction with thin mirrors.

7) An LC aligning layer, deposited on the silicon backplane, can further reduce the LC flow front disruption.

8) FLC filled cells produced very different results from NLC in that the effects of the thin mirrors and SIFT processed thin mirrors, on the FLC flow front, were very subtle.

Work which is being continued includes;

a) Implementing an argon ion pre-deposition clean process to improve the adherence of the SiO to the substrate (this will allow an extended pre-alignment layer deposition substrate scrub)

b) Filling SIFT processed cells with FLC and examining the flow fronts in more detail.

3.10 Post processing summary

A revised post-processing procedure based on the polished via/SIFT process is given below. This takes the "as-received" wafer through the custom fabrication processes to a stage where they can be used to construct full SLM's.
The table, at the end of this section, provides a comparison between the three mirror/electrode forming processes discussed in this thesis.

1) ECR-PECVD silicon dioxide is deposited to a thickness of 1.5-2.0 times the height of the tallest feature of the die/wafer.

2) The silicon dioxide is planarized by Chemical Mechanical Polishing (CMP). The quality of the polished wafers are device dependent. The planarization process has been well characterized for the 512x512 SLM, but future generations of devices should contain dummy mirrors around the pixel array to avoid the effects of errosion [Seunarine, 1999].

3) The CMP slurry residue is removed using a post-CMP wafer scrub. Early post-CMP wafer scrubbing was inadequate, but with the PVA wafer scrubber being brought on-line shortly, the slurry residue problem will be reduced.

4) **Light shielding layer deposition and patterning. This is an optional procedure and requires an additional via layer.**

5) ECR-PECVD silicon dioxide deposition.
6) CMP oxide/scrub.
7) The via holes are etched by RIE ensuring that passivation layer is completely etched.

8) The wafer is blanket coated with sputtered aluminum to fill vias to a thickness sufficient to completely fill the vias (1-2 micometers).

9) The metal is polished back by CMP (possibly using an etch back technique, appendix B) to polish aluminum back to vias. The CMP process still to be optimized on the Presi polisher.

10) A post CMP wafer scrub is performed to remove slurry particles and degrease the substrate surface.

11) Thin mirror deposition by evaporation. A laboratory evaporator was used, but production equipment is required for >4" product wafers.

12) The mirrors are patterned into the evaporated aluminum by a masked RIE.

13) Before stripping the photoresist the wafer is coated (by evaporation) with a pre-calculated thickness of silicon oxide, which fills the trenches between the mirrors leaving a planar array surface profile.

14) The unwanted resist/oxide is then removed by ultrasonic scrubbing in acetone.

15) Oxide spacer layer deposition, patterned by lift-off. The "best" geometry is yet to be decided. The usual thickness required for CS-1031 filled cells is 2.4μm or 0.8μm. The latter is desired as it will allow the optimum electro-optic response of the FLC, and the spacers will be much easier to fabricate to small geometries.

16) Spin coat wafer with protective photoresist layer.

17) The wafer is diced using a scribe and break method.

Technology	Advantages	Disadvantages
Conventional mirrors	Simple, no slurry contamination.	Thick aluminum layer (granular) and therefore deep trenches between mirrors, difficult (impossible) to pattern spacers by lift-off in interpixel gap.
Dual damascened mirrors	Mirrors "flush" with oxide, no wet/dry aluminum etch required, small impact on LC flow front (mirrors dished in center).	Mirrors are etched into the oxide, with no etch stop and then vias are etched down to metal 2, scratching, dishing and erosion problem, slurry residue, via "dimples" present on real devices, considerable development required.
Thin (via polished) mirrors	High optical quality evaporated mirrors possible, trenches are easily filled using novel technique, liquid crystal flow front is unaffected by resultant substrate, technology exists and ready to implement, increased fill factor due to negligible dishing of vias.	Evaporated aluminum adhesion problem, slurry residue, post CMP clean required before final metal, excessively thin mirrors transmit %age of incident light, two metal depositions required (one to form via plugs and the other to form the mirror layer), in-house evaporation uniformity issues.

Table 3. 7 Although the "thin" mirror technique has some disadvantages, they are all relatively easily overcome, and the potential gains on offer are unequalled by the other two methods at present.

3.11 Discussion

At the beginning of these studies the highest quality LCoS devices were achieved through planarization of the foundry wafers. Although the pixel fill factor of these early devices was greatly increased it was still far from ideal. One of the main problems which remained included via "dimpling". This via dimpling would have been a major problem for future LCoS devices, such as the MINDIS[4] 1280 x 1024, which is to consist of extremely small mirrors (<10x10μm after post-processing).

[4] Miniature Information Display Systems. Funded by the European Commission (project Esprit 26300).

Simple calculations show that a 10μm x 10μm pixel will have a maximum fill factor of 70.56% (assuming a 1.6μm gap between mirrors stipulated by the EMF). A 2μm x 2μm via, which is in reality much larger following etching (~3-5μm) will then degrade mirror efficiency further. Another major problem with the early planarized devices was that of the deep trenches present between the pixel mirrors.

Via polishing has been shown to almost completely remove the via "dimple. The thin evaporated aluminum, which is patterned over the polished vias, provides an extremely high optical quality mirror layer which is relatively easy to etch. We have also demonstrated a novel technique of filling the thin mirror inter-pixel trenches (flat to 2.5nm) by using the existing photoresist layer, used to pattern the mirrors. Upon deposition of a thin layer of oxide (~80-100nm) we have sucessfully demonstrated the entire removal of the unwanted PR and oxide layers leaving a planar pixel array surface which obviates the need for fully polished (damascened) aluminum mirrors.

Subsequent filling, with LC, of test cells constructed from these thin mirror, SIFT processed die shows that the surface of the pixel array has no detrimental effect on the LC flow front, in which the highly desired linearity is maintained.

Chapter 4.

Techniques for Backplane Flattening and Cell Gap Spacing.

4.1 Need for a flat backplane and accurate cell gap spacing

The main limitation in LCoS device, figure 1.8, performance arises from the lack of uniformity in the FLC alignment, FLC layer thickness and backplane (die) flatness [Underwood, 1997]. The transmission of light, of intensity, I, at a point in a reflective mode FLC cell, equation 10, is dependent on the layer thickness, d.

$$I(\lambda) = I_0(\lambda)\sin^2(4\theta)\sin^2\left(\frac{2d\pi\Delta n(\lambda)}{\lambda}\right) \qquad (10)$$

Where,

θ is the cone angle of the FLC (defined in section1.3.1),

$\Delta n(\lambda)$ is the birefringence of the FLC,

and λ is the wavelength of the incident light I_o.

Any non-uniformity in the FLC cell gap may result in one or more of the following:

1. Incomplete cell filling.

   The result of incomplete filling of the LC cell is disastrous, in that the device, or part of the device, cannot be used.

2. Poor alignment, *i.e.*, spatial variations in LC alignment.

   Non uniformities in the cell gap thickness usually mean that the liquid crystal flow, during cell filling, will not be as desired. As the flow of LC affects its

alignment, the direction of filling must be uniform, *i.e.*, the flow front must proceed in a linear manner. Any deviation from this scenario may result in domains of the liquid crystal cell which have different LC director orientations (parallel to the substrate).

3. Spatial variations in the optical path length of the LC layer.

   From equation 10, it can be seen that any variation in the liquid crystal layer thickness will affect the light transmission throught the display, resulting in colour fringing or even contrast inversion.

4. Spatial variations in the switching characteristics of the LC.

   In a non-uniform cell the local electric field may vary considerably which will in turn affect the local liquid crystal switching characteristics.

While a thicker cell gap makes cell assembly easier, it sacrifices display performance by requiring a higher backplane voltage (increased power dissipation) and hence a lower pixel density [Kazlas, 1996]. Ideally we would like $d = 0.8\mu m$, but in practice SLMs of this nominal FLC thickness can be difficult to produce with acceptable small thickness variations both within and between devices [Underwood, 1997]. Typically the maximum acceptable variation in the cell gap spacing is 100nm over a 10mmx10mm device area [Kazlas, 1996]. The alternative is to aim for an FLC thickness of 2.4μm. SLM's which are used as optical elements in processors, correlators *etc.*, have an additional constraint of requiring an extremely flat backplane to prevent spurious phase modulation effects.

4.2 Backplane flattening

We have very little or no control of the CMOS processes used in the fabrication of our wafers, so SLM backplane flattening must be carried out as part of the post-processing or cell assembly procedure. Methods reported (at the time of writing) of flattening optical device wafers and backplanes, are the electrostatic bonding technique, transfer bonding technique and the self-aligned solder technique.

Electrostatic bonding

The electrostatic bonding technique involves bonding a 250-300μm thick high resistivity silicon wafer to a low thermal expansion glass (4.5.1) substrate. A high dc electric voltage (1kV) is applied across the structure at a temperature close to the strain temperature of the glass (600°C). The resulting bond between the silicon wafer and glass substrate is chemical and therefore permanent. Following bonding the wafer can be polished to the desired thickness and flatness by standard lapping techniques [Sayyah, 1989].

Sayyah *et al.* have reported flatnesses of λ/4 or better over a 5cm diameter area, using the electrostatic bonding technique. The main disadvantage with this technique is that the wafers are not processed before bonding, *i.e.,* the technique cannot be used as a post processing procedure.

Transfer bonding

The transfer bonding technique is based on the adhesion of two very clean and flat surfaces, in contact with each other. The adhesion between the two surfaces is only physical and not chemical, so they can be easily seperated at a later stage in the process. The processed 125μm thick product wafer is contact bonded, on the top side, to a λ/10 optical flat. Any non-uniformity in the thickness of the wafer is transposed onto the nonbonded backside, which is then bonded to a supporting optical flat with epoxy adhesive. After the epoxy has cured the wafer can be removed from the contact bonded flat for further processing [Sayyah, 1989].

Unlike the electrostatic bonding method, this technique can be applied after the high temperature CMOS processing, but not after final metallization. The glass supporting substrate in this method will prove problematic in that, depending on the glass substrate thickness, wafer handling will be affected and final wafer dicing will be severely complicated by the composite silicon-epoxy-glass structure.

Self-aligned solder technique

A very different method is the self-aligned solder technique. This technique relies on the strong pulling forces of the molten solder joints between the cover glass, which overlaps the silicon die, onto the device package. The technique has been developed to achieve the following objectives (1) uniform cell gap and (2) align the cover glass, silicon and package (substrate) to a high accuracy (within 10μm). The best cell gap uniformity reported, with this technique, was ~3/2λ over the device. The spacer layer used was reported to be on the glass cover plate. This technique may possibly benefit from microfabricated features in the pixel array, such as our robust ECR-PECVD SiO_2 spacer layers described later. The same group is also looking into using die attachment materials, sandwiched between the backface of the die and the device package, which when cured at various temperatures, control the VLSI chip warp. Initial results reported indicate that reasonable die flatnesses (λ/2) can be achieved with this technique [Lin, 1993].

4.3 Cell gap spacing

There are many cell gap spacing methods reported. Some of these will be described in this section. The most common method used, and the only method used by the A.O. Group at this time, is spacer rods/balls blown across the substrate, or mixed with adhesive. The problems with such particles are:

(1) They are, in the case of blown spacers, randomly distributed across the device, figure 4.1, which may cause light scattering and wipe out a large portion of individual mirrors.

(2) They are very fragile, *i.e.*, easily crushed during cell assembly, see figure 5.14.

(3) Any lateral motion of the coverglass during cell assembly may cause the particles to tear the soft aluminum mirrors [Begbie, 1997].

(4) They are only readily available in specific sizes [Bangs, 1998].

All of the above may potentially affect the cell gap and hence the LC layer thickness. It is apparent that a robust microfabricated spacer layer is required, which will enable us to deposit spacers on a wafer as opposed to a die scale.

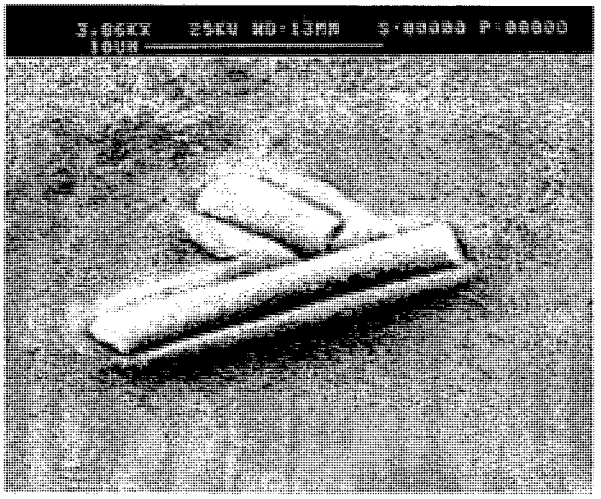


Figure 4.1 Pressure exerted on the coverglass has been found to cause silica spacers to become embedded into the 1μm of sputtered aluminum. Courtesy of M. Begbie.

The most recent developments in cell gap spacing has been described by two independent groups, Kazlas at the University of Colorado and Lee at Samsung Display Devices, Korea [Kazlas, 1996], [Lee, 1997]. Both groups used a photodefinable Benzocyclobutene[1] (BCB) from Dow Chemicals. The BCB material is spin coated and patterned in a similar manner to negative photoresists. One interesting aspect of this material is that it can, under suitable conditions, act as an adhesive, to bond the cover glass to the silicon by thermocompression bonding.

[1] BCB has previously been used to planarize liquid crystal over silicon devices and flat panel displays [Perettie, 1992].

Work carried out by A.W.S. Ross, of the A.O. Group, University of Edinburgh, into BCB has shown that this material is extremely difficult to use, in that the spin coater requires a suitable atmosphere to prevent "skinning over[2]" of the material during coating. The minimum thicknesses possible with BCB were reported to be around 2.4μm [Ross, 1999]. There are also significant reductions in the BCB thickness following the soft bake, exposure and developing, which makes calculating the final spacer height difficult. It also has the disadvantage of not being patternable (with the developer) to the dimensions required for spacers in the active area of the device. To achieve smaller feature sizes the cured BCB material has to be dry etched. To use BCB as an adhesive, the curing conditions are also found to be crucial.

Other methods of cell gap spacing reported include posistive photoresist spacer dots, CVD diamond patterned dummy structures, screen printing and adhesive coated spacers [Yaniv, 1996], [Nakanowatari], [Sato], [Sletmoe, 1985], [Gourlay, 1994].
Low melting temperature glass has also been used in much larger flat panel displays (FPD) in an effort to compensate for the diameter distribution of conventional silica spacers across the display [Kasahara, 1994]. Early investigations into spacer layers which were performed by the A.O. Group included evaporated SiO_x which was patterned by an aluminum mask or standard lithographic techniques, into pillars. The thickness of the spacer layer, measured by quartz crystal monitor during deposition, was found to be difficult to control, and the pillars also became very fragile at thicknesses exceeding 1μm [Gourlay, 1994]. Also to obtain the best uniformity, the evaporator must run at low rates [Aceves, 1992], but low evaporation rates mean extremely long processing times.

An ideal spacer material for our work will be extremely robust, chemically inert to LC and patternable on a wafer scale by lift-off, to protect the high optical quality aluminum pixel mirrors. Fortunately silicon dioxide deposited by ECR-PECVD satisfies these requirements. Another important quality of PECVD SiO_2 is its low compressive stress and good adhesion to aluminum, which permits very thick films to be deposited, without the film blistering or cracking [McGuire, 1988].

[2] Where a thin skin is formed on the liquid layer.

Spacing method	Advantage(s)	Disadvantage(s)
Polyester sheet [Underwood, 1987]	Readily available.	Crude, layers greater than ~50μm, rough edges.
Silica particles	Readily available, choice of method of application.	Limited choice (size), fragile, random distribution.
Photoresist (PR)	Well characterized standard microfabrication process.	Chemical impurities, attacked during standard cleaning process.
BCB	Patternable as *negative* photoresist. Also acts as an adhesive under certain conditions.	Large features, difficult to coat (min thickness of ~2.4μm), height reduction on cure *etc.* High cure temperature 200-300°C (degrades optical quality), sensitive to solvents.
Evaporated SiOx	Simple, inert.	Fragile.
CVD diamond	Robust	High deposition temperature (>500°C)
Dummy structures	Uses existing circuitry.	Can't planarize.
ECR oxide/lift-off	Well characterized, excellent uniformity, robust, inert to LC, low deposition temp., small features, no chemical etch.	Height pattern dependent, *i.e.*,depletion of reactant gasses in deep, high aspect ratio, trenches.

Table 4.1 Summary of the main cell spacing methods.

4.4 SLM construction

In this section I give a brief description of the cell assembly procedure currently used by the group. Potential assembly problems are discussed and solutions proposed. Details of the alignment layer deposition and filling of the cell gap with FLC are described in detail in appendix D.

4.4.1 Substrate cleaning

Clean substrates are crucial in the fabrication and assembly of LC devices. A rigorous cleaning regime must be adhered to as the LC alignment is affected by contamination section 1.1. Larger particulate contamination on the substrate during spacer layer patterning causes "comet tails" in PR during spin coating and may also become trapped in the oxide spacer layer during deposition. Even with ultrasonic scrubbing these trapped particulates are impossible to remove, see the example in figure 4.2.

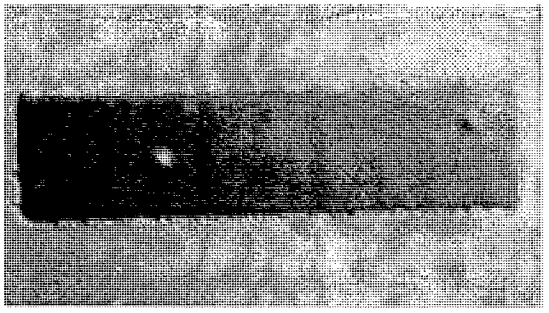


Figure 4.2 Particulates trapped in the spacer layer during fabrication.

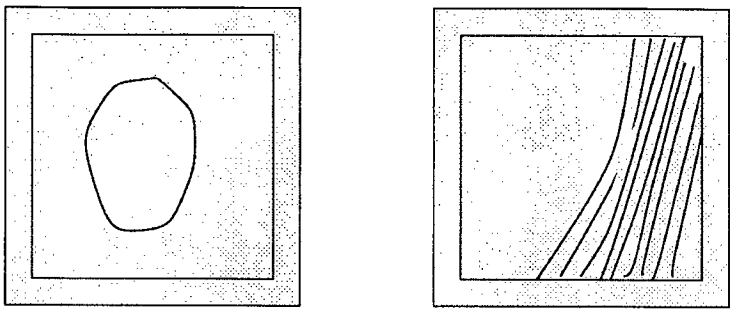
4.4.2 Device assembly

All liquid crystal test cells and SLMs were assembled in the A.O. Group LC cleanroom, on a bench in front of a laminar-flow HEPA filter unit. Prior to assembly all the equipment, jigs and work surfaces were cleaned to minimize contamination. The ITO coated side of the coverglass was identified visually or by resistance measurement using a multimeter before mounting in a jig. Aluminum evaporation, for the common electrode electrical contact was performed using an Edwards E306 system at a pressure of $<4x10^{-4}$ Torr, as described in appendix D. The substrates were then removed from the jig and any loose particulates blown away in a filtered ionized nitrogen stream. The substrates, usually just the coverglass, were then mounted in a second jig for evaporation of a SiO_x LC alignment layer. The evaporation was carried out in an Edwards Auto-306 evaporator with the SiO_x beam incident to the substrate

at 60°. In order to minimize the amount of particulates being ejected into the evaporation chamber a baffled Mo boat was used for heating the SiO_x, and any SiO_x which had flaked off the chamber walls *etc.*, was removed using a vacuum cleaner nozzle located in the LC cleanroom. The film thickness was monitored by a quartz crystal oscillator monitor. The film deposition was then ended when the film thickness monitor measured a pre-set value, typically 30-60nm.

In the early days of LC SLM construction the A.O. Group performed cell assembly after PGA packaging and ultrasonic gold ball wire bonding. From the group's experience with the 16^2 [Underwood, 1986] device, it was believed that when the chip was glued into the chip package, serious bowing of the backplane resulted. This may have been due to the fact that the package was not optically flat. Later it was decided to construct the FLC cell and fill the cell before gluing the chip to the chip package and wire bonding. To allow access of the bonding equipment to the chip bonding pads, a thin 12mm x 12mm x 1.1mm piece of ITO coated glass, supplied by Merck, see appendix D, was used as the coverglass [Gourlay, 1994].

The appropriate size spacer rods/balls (2.4μm for display applications) could be applied to the substrate in three ways, (1) spin coat particles which were contained in DI water, (2) blown spacers on with nitrogen, and (3) mixed spacers with the UV curing adhesive. Obviously, the 3rd method only had spacing at edges of cell, but no random distribution of spacers in array. The exact cell construction details, in the group, varied from operator to operator, but they were all very similar. Ultraviolet (UV) curing adhesive was placed, usually at the corners of the ITO side of the coverglass. The coverglass was then placed, ITO side down, onto the chip and pressure applied to the coverglass, at various positions, until the white light fringes were circular and minimized. The orientation of the coverglass should be such that the direction of the evaporated SiO is perpendicular to the LC filling edge [Bodammer, 1996].



(a) (b)

Figure 4.3 Illustration of the white light fringes present following cell assembly (a) a maximum of one circular fringe was acceptable, and (b) a wedge caused by dirt meant that the cell was rejected.

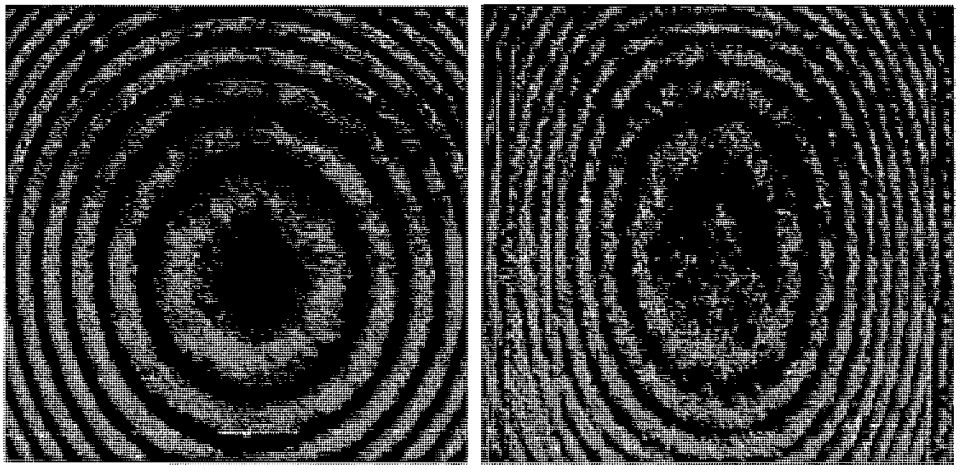
The pressurized die flattening assembly technique used 12mm x 12mm x 3mm λ/10 Pyrex 7740 cover glass, which could be ITO coated in-house. The actual device flattening/cell assembly was performed as described in earlier sections.

4.5 Backplanes for test cells.

Product wafers were generally warped due to the thermal processing, described in detail in 2.2. 256x256 SRAM dice were examined with the interferometer and surface profileometer to determine the magnitude and direction of bowing. To emulate this severe bowing stresses were introduced into dummy silicon wafers. 3000Å of thermal silicon nitride, which has a high tensile stress, was grown on 75mm wafers, in a furnace. The silicon nitride was dry etched from the surface of the wafer to have the convex bow, in our case the front surface. The bow produced was on the order of 50-60μm, which was comparable to that of the bow in a 100mm product wafer. The wafers were blanket deposited with 1μm of sputtered aluminum prior to the spacer layer patterning and deposition. The spacer layer pattern used in these experiments[3] consisted of an array of 70μm x 200μm rectangles set in a diamond pattern on a 1mm pitch, deposited by ECR-PECVD as detailed in chapter 5, using a recipe optimized to produce high deposition uniformities. From the interferograms in figure 4.4 and the

[3] Designed by M.Begbie, Dept. of Physics and Astronomy, University of Edinburgh.

surfaceprofileometer traces we see that the direction and magnitude of bowing of the test die are similar to that of the actual 256x256 SRAM die.



(a) (b)

Figure 4.4 Interferograms of (a) 14mm x 14mm die from a 75mm silicon wafer (3000 Angstroms of thermal nitride on backface) and (b) 256x256 SRAM die.

4.6 Backplane flattening and cell spacing investigations

Three methods of backplane flattening were investigated in this study, which all utilized the robust silicon dioxide spacer layers described in chapter 5. These methods will each be described in the following sections, but first I will describe the method of inspection of the flattened devices. Initial experiments into cell assembly and die flattening were based on our usual SLM assembly procedure. It was quickly discovered that the silicon die was forced to conform to the coverglass, which was supplied by Merck (appendix D). This type of glass was found to be very flexible and of a poor flatness ($\lambda/2$). It was apparent that a more suitable cover glass was needed before any progress could be made. Subsequently a supplier was found who could provide 12mm x 12mm x 3mm corning 7740 $\lambda/10$ optical flats[1]. The pressure required to flatten a 380μm thick 14mm x 14mm silicon die was on the order of 1-2 bar. Note: The slightly thicker product die, 525μm, may be thinned by backface grinding if needed.

4.6.1 Flattened backplane inspection

A Fizeau Interfire 633 interferometer was used to investigate the backplane flatness of assembled cells. In order for the interference fringes from the backplane to be examined, the fringe intensity must be high enough to prevent them being swamped by the fringes from the other interfaces. This was achieved by increasing the reflectivity of the backplane (aluminizing), and minimizing reflections from the first air-glass interface. A simple way of reducing the reflections from this first air-glass interface was by depositing a $\lambda/4$ MgF_2 coating on the front surface of the cover glass. The assembled cell was then mounted on a stage in which movement in the x,y plane and rotation about the x axis was possible by micrometer screw. The position of the cell was adjusted until the correct set of fringes were found. This was determined by

[1] If the coverglass is too thick, and/or the bond pads too close to the pixel array, the wire bonding process will be hindered, or made impossible.

comparing the fringes from the cell with those from the part of the backplane not obscured by the cover glass.

4.6.2 Backplane flattening (Method 1)

This method was based on bonding the bowed silicon backplane to a rigid supporting substrate. A quantity of adhesive was applied to the top surface of the supporting substrate, a 1.1mm thick coverglass. The adhesive was then left for 10 minutes, to allow gravity to force the adhesive "blob" to spread over the substrate, and to permit the adhesive to partially cure. The remaining two components making up the backplane flattening assembly were then cleaned and inspected as follows. The cleaned backplane with an optical flat resting on the top surface was placed on a cleanroom tissue. By pressing down on the optical flat with a pair of plastic tweezers the white light interference fringes were observed. Clean components were evident when the fringes were minimized. Components which were not satisfactorily clean were put through the cleaning cycle again. These two components, were then carefully lifted and placed facing upwards, on top of the adhesive coated substrate, figure 4.5.

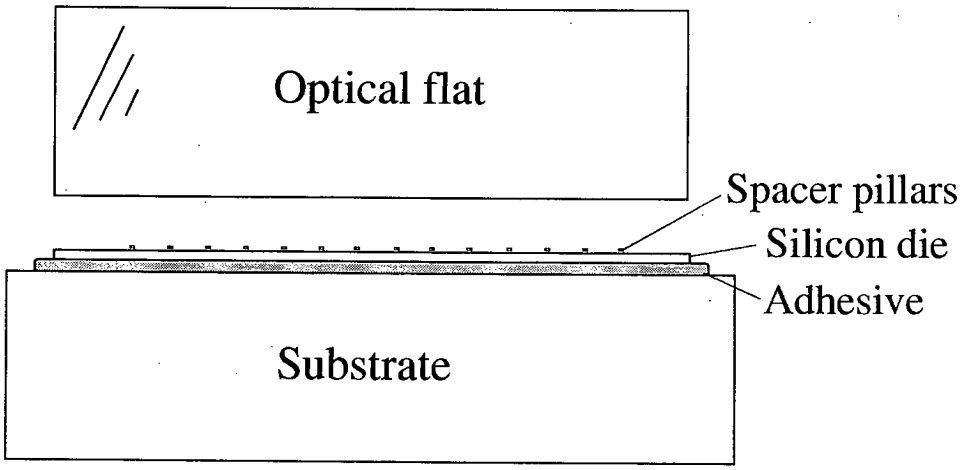


Figure 4.5 Backplane flattening schematic.

Pressure was then applied to the whole structure using the vacuum packer, shown in figure 4.6, and left over night to allow the epoxy adhesive to fully cure.

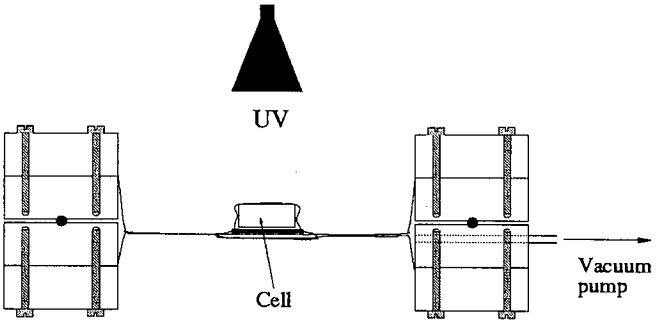


Figure 4.6 Cell held under pressure by vacuum packer.

Upon examination of the top surface of the silicon die surface, with the interferometer, we found that the backplane was flattened from about 3λ down to about 3/2λ, figure 4.7, over the pixel array.

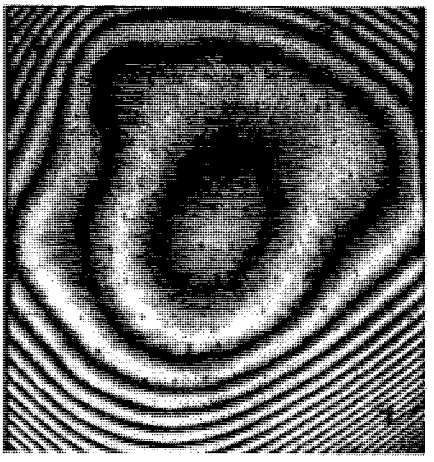


Figure 4.7 Backplane flattened using method 1.

These investigations have shown that this method (1) is a feasible method of flattening device backplanes, but major problems remained in the form of

(1) Particulate contamination.

The components of the die flattening assembly need to be kept free from all particulates.

(2) Adhesive thickness uniformity.

The adhesive should be spead uniformly over the substrate.

(3) Adhesive viscosity/curing.

The adhesive should have a high viscosity to minimize the material seepage from the sides of the structure. It should also be UV curable for convenience.

(4) Spacer layer geometry.

We have found that the existing spacer layer geometry is inadequate for the purpose of die flattening and requires modifications as described in 4.6.6.

It was also found that the UV curing adhesive did not adhere to the silicon nitride on the backsurface of the silicon die. So a layer of epoxy adhesive was used in the construction of the test device, above.

4.6.3 Backplane flattening (Method 2)

The idea behind this technique was to use the stresses in the cell assembly, indicated by the arrows in figure 4.8, to clamp the silicon backplane to the coverglass (optical flat).

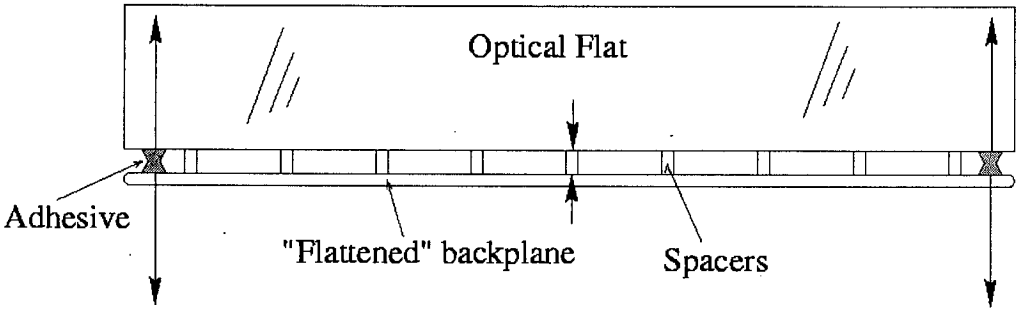


Figure 4.8 Internal stresses in conventionally assembled glass on silicon cells.

The test cells were constructed in the usual manner, by applying small quantities of UV curing adhesive to the coverglass and placing the coverglass, adhesive side down, onto the silicon backplane. A uniform pressure was then applied to the cell assembly using the vacuum packer, shown in figure 4.6, whilst the adhesive was curing. Examination of the flattened backplane revealled much better results than was seen in method 1. The flatness achieved was estimated to be around $\lambda/3$, figure 4.9.

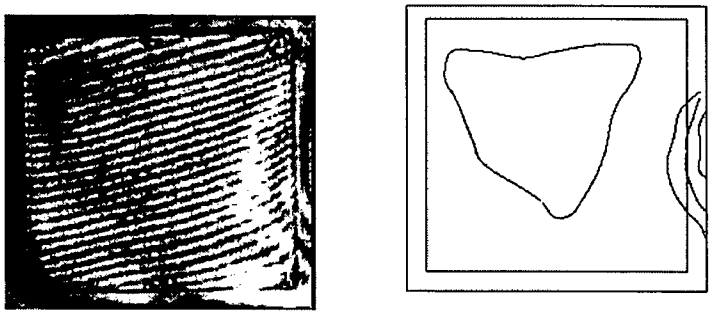


Figure 4.9 Flattened backplane (unfilled), where the horizontal fringes are from the top surface of the cover glass. The diagram to the right shows the location of the fringe of interest.

Upon filling the cells, however, It was discovered that the surface tension forces at the LC/glass interface caused the flexible silicon backplane to bend.

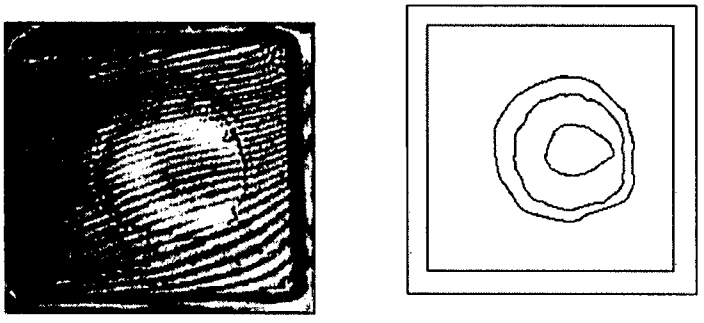


Figure 4.10 The surface tension forces cause an elastic deformation of the silicon die, which results in incomplete filling of the cell gap (air gap is in center of cell) .

4.6.4 Surface tension forces in cell during filling

On filling these assembled cells with nematic liquid crystal, the surface tension forces, which enable the cell to fill, also "pulled" the substrates together. The pressure differential, ΔP, at the LC-glass/air interface, equation 11, is dependent upon the surface tension of the LC-glass/air interface, α, the contact angle, θ, and the seperation between the plates, x. Since $\theta < 90$ degrees, the plates will be pulled together, equation 12.

$$\Delta P = P_{Atm} - P_{Surf} \qquad (11)$$

$$F = \left(\frac{2\alpha S}{x}\right)\cos\theta \qquad \text{[Landau, 1967]}$$

$$\therefore \Delta P = \left(\frac{2\alpha}{x}\right)\cos\theta \qquad (12)$$

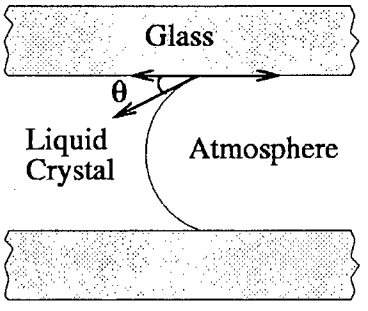


Figure 4.11 Liquid crystal filling the cell by capillary action.

It was observed that most of the fringing, in the unfilled cells, was around the perimeter of the pixel array, and this associated thickness variation may have been a contributing factor to the poor uniformity of the cells during filling, figure 4.10.

4.6.5 Backplane flattening (Method 3)

The final method developed independently by both the author and Begbie [1997], was a combination of the first two techniques, in that the coverglass and supporting substrate were simultaneously bonded to the silicon backplane. The early experimental devices constructed used an epoxy adhesive between the substrate and silicon die. At the same time, unknown to the author, Sanford *et al.* [1998] reported a similar assembly technique in which they used a UV curing adhesive with a bottom support substrate. Begbie, used a Rodel wafer insert[2], cut to the required dimensions, sandwiched between the device and the supporting substrate, figure 4.12, to produce a

[2] Rodel Corporation, Scottsdale, Arizona.
Part number A12610

restoring force on the backplane. Although flatnesses of $\lambda/8$ have been reported using this technique [Begbie, 1997], the author has only achieved flatnesses of $\geq \lambda/3$ in cells constructed using either an adhesive or the Rodel insert in these investigations. The main cause for this poor flatness is, again, due to particulate contamination on the components. We also found that the pressure applied to the cell assembly was important. When the pressure was too low, the backplane was not flattened completely, and when the pressure was too high the silicon began to flex between the supporting spacers. A major disadvantage of this technique, using a Rodel insert, which must be addressed before it can be used on working devices, is the stability of the Rodel insert. There was some concern whether the Rodel insert would retain its desired mechanical properties over the operational life time of the device. Alternative materials, which do not deteriorate with aging and exposure to heat, should be sought.

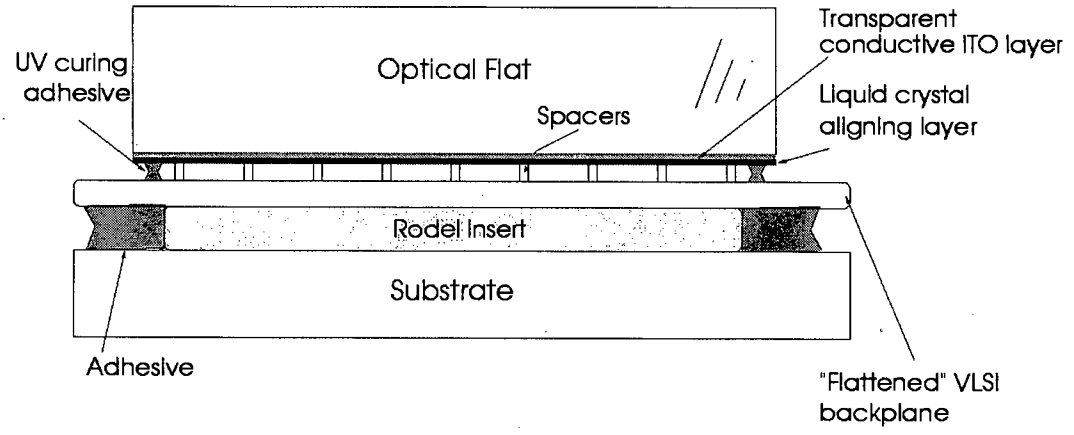


Figure 4.12 LCoS cell assembly cross section.

4.6.6 Future metal and spacer layer geometry modifications

To enable the backplane flatness to be improved the spacer layer geometry was re-designed, to extend the area covered by the spacers, figure 4.13. This extended geometry spacer layer, should provide support for the cell over the entire cell area and, when used instead of the earlier geometry layers, designed by Begbie, may reduce the fringing at the edges of the cells. Up until this time, SLM backplanes,

made within the A.O. Group, were designed without giving consideration to the ramifications of planarization (especially CMP) of the device. So dummy structures should be included into metal 3 (mirror electrode layer), of current SLM's, to ensure that the spacer layer can maintain the correct spacing across the entire display (as the first generation of spacers were to be fabricated on top of the pixel mirrors). Also, the level of planarization must be such that there is no step from the pixel array (before final metalization) to the surrounding substrate. Fortunately, this extremely high degree of oxide flatness may be achieved by use of a masking and etching step before polishing [Seunarine, 1999]. This mask and etch process was only regarded as a short term solution by the author as it entailed an additional photolithography step. Modification of the first two (foundry) metal layers, in future devices, where high spatial density dummy features are placed around the array in the relatively bare parts of the backplane (adhering to the specified CMOS design rules) will prevent the need for this device dependent mask and etch process.

4.6.7 Thermal coefficient of expansion mismatch

The procedure for filling the cell with FLC, appendix C, requires that the device and FLC are heated to above the Chiral Nematic-Isotropic transition temperature of the FLC, (~97^{0}C for the CS-1031 material supplied by Chiso, appendix D). The phase transitions of CS-1031 are as follows:

$$\text{SmC}^* \xrightarrow{60^0\text{C}} \text{SmA} \xrightarrow{85^0\text{C}} \text{N}^* \xrightarrow{97^0\text{C}} \text{Isotropic}$$

This immediately places a limitation on the materials used to construct the cells. Although, at the time of writing, low thermal expansion glasses were freely available, B.2, a suitable low thermal expansion adhesive was not. Clearly, an adhesive which expands at a different rate than the glass/silicon is undesirable. It would be desirable, therefore, to reduce the number of glass/silicon-adhesive interfaces to a minimum. We kept the adhesive bonding the cover glass to the backplane[3], whilst investigating

[3] NOA81 is selected as it is rated to 125^{0}C, compared to the previously used NOA68/88 adhesives, which are rated to only 90^{0}C.

alternatives to bonding structures to the back of the device. Since this investigation was carried out the author has discovered that Micropix [1998] have used a matched thermal expansion glass on their devices.

Technique	Advantages	Disadvantages
Electrostatic bonding [Sayah, 1989]	Excellent flatness over a wafer. $\lambda/4$	No good for post-processing.
Transfer bonding [Sayah, 1989]		Wafer handling and dicing problems, thermal mismatch.
Self-pulling [Lin, 1993]	Self aligning. Within 10μm.	Complicated, 0.3μm variation in cell gap across active area, wire bonding and cell filling obstructed.
Die attachment [Lin, 1993]	Relatively simple, no spacers in array.	Flatnesses reported to date are poor for reflective SSFLC SLMs ($\lambda/2$), requires backface polishing, thermal mismatch.
Method 1	Flatness of about $3/2\lambda$[4] achieved.	Thermal mismatch.
Method 2	Flatness of $\lambda/3$[4] achieved.	Little thermal mismatch and therefore the most compatible of the latter three methods for use with FLC.
Method 3	Flatnesses down to $\lambda/8$, with 80nm variation in LC thickness across device.	Thermal mismatch. The author has only acheived a flatness of $> \lambda/3$[4].

Table 4.2 Comparison between various backplane/wafer flattening techniques. Note that Methods 1, 2 and 3 use robust oxide spacers which protect mirrors during cell assembly. The glass used in flattening the backplane acts as one plate of an interferometer, thereby allowing the operator to view the relative flatness of the die.

Other methods of flattening the wafers/die such as depositing stress compensating layers (sintered aluminum) on the backface of the wafer were considered to be unfeasible as the stress distribution across the wafer/die varied from sample to sample. In order to flatten a sample in this way a complicated finite element analysis would need to be performed, to determine the geometry of the patterned stress compensating layer, and this would vary from die to die and possibly wafer to wafer.

[4] Potential for improvement.

4.6.8 Adhesive encroachment

At present bonding of the cover glass to the silicon backplane with a UV curing optical adhesive was the only method used by the A.O. Group. Unfortunately, the capillary forces in the very small cell gap, caused the adhesive to spread considerably, before it was finally cured. Quite often this spreading reached the active area of the display, reducing the yield of useful devices. It was apparent that this problem would only worsen with the decreasing cell gap thicknesses. Although the quality of cells assembled depended on the operator skill, adhesive spreading could be reduced by controlling the above mentioned capillary forces.

Perimeter trench

In addition to using a continuous spacer layer to restrict the spreading of adhesive in the small cell gaps, a trench etched into the planar oxide, was shown to minimize the adhesive encroachment into the cell gap, as shown in figure 4.14.

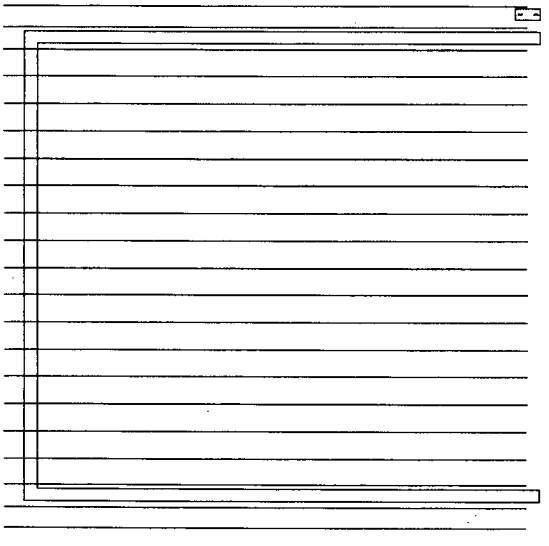


Figure 4.13 Modified spacer layer geometry and trench etch masks. The area enclosed by the spacer layer is also representative of the area covered by the cover glass.

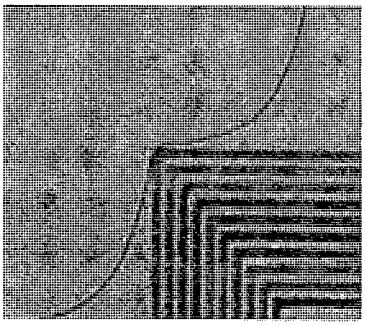


Figure 4.14 Adhesive (left) spreading in the small cell gap, which would be exacerbated by the move from 2.4μm to 0.8μm cell gaps, was controlled by a trench etched into the substrate.

4.6.9 Spacer aligning mark issues

The registration marks, used to align the reticles to the underlying layers on the wafer, were in close proximity to the pixel array, figure 4.13. As we will see in the next chapter, the height of any feature patterned by lift-off, depends on its lateral dimensions. The spacer aligning marks (local) are 20μm wide, figure 4.15, whereas the spacer pillars are 8μm wide. This has serious implications if we are to place a cover glass over the array to form an accurate cell gap. If we are to move from an unrepeatable manual to a highly repeatable automated SLM manufacturing process in which the cover glass is positioned very accuratelly in some assembly jig, these alignment issues must be addressed.

Local spacer aligning mark removal

The perimeter trench, 4.6.8, and spacer layer local aligning mark removal were combined on a single mask, figure 4.13 and 4.15. Following spacer deposition and patterning, the wafer will be patterned with the mask which is aligned globally. As no automatic alignment will take place, the pattern is blind stepped, 2.8.1. The accuracy of registration of the perimeter trench and local aligning mark etch is not critical, so the relatively large registration uncertainty, of global alignment will be acceptable.

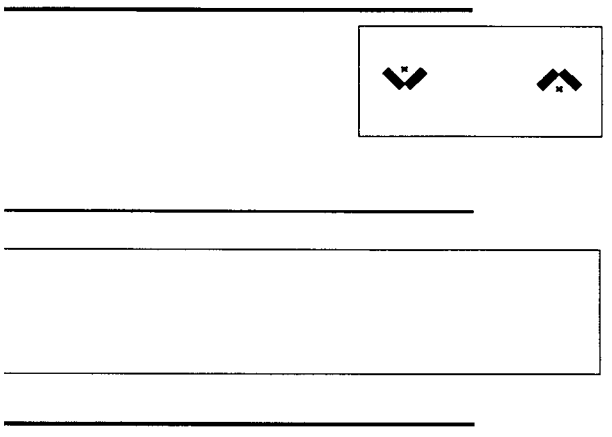


Figure 4.15 256x256 SLM spacer layer local aligning marks in close proximity to pixel array. The cover glass may extend past one or both of the local aligning marks shown. This problem is even worse for the 512x512 SLM as both sets of alignment marks are only 500μm from the array.

4.7 Cell inspection

The uniformity of the unfilled cells was measured by the white/monochromatic sodium light interference fringes observed between the two substrates. A visual inspection of the liquid crystal filled cells was carried out by placing the cell between two crossed polarizers, on a light box, if the cell was transmissive. If the cell was a reflective mode device, it could be inspected under an analyzer with a suitable ambient light. Further evaluations of the device quality could be made by measuring the LC switching speed and contrast ratio. Where the CR can be measured on two scales namely the "small area" and the "large area", where "small area" refers to pixel sized areas and "large area" to groups of pixels that may cover half the display. The "large area" CR is important as it includes the deleterious effects of the edges of the pixels.

4.7.1 Cell gap thickness

Various methods have been reported of measuring the gap thickness. The simplest of which is to observe the fringes under white light. As the light is polychromatic, colored fringes can be observed (from blue to red). This allows the identification of which direction the variation is progressing due to the color variation (*i.e.*, blue is thinner than red).

A white light scanning interferometric method, developed by M. Hart [1997], had a nanometer resolution, but was only effective in transmission mode. Another method involved illuminating the cell at an oblique angle, using a monochromatic source. The reflected light, which was projected onto a suitable screen was in the form of interference patterns. The separation between the fringes at a known distance from the cell, could be equated to the cell gap, *d*. Unfortunately, this method was not accurate enough (+/-0.5μm) for our needs. Other methods such as capacitive measurements and measuring the state of polarization of light reflected through the unknown thickness of LC maybe possible. Kazlas [1996] used a 4mm diameter tungsten probe beam on transmissive glass-on-glass cells to measure the cell gap thickness, by plotting the optical transmission as a function of wavelength.

A good indication that the LC thickness was equal to the spacer height, which we would expect to set the cell gap, was to examine the cells under a polarizing microscope. It was found in the early experiments, that on cells constructed from smaller backplanes which had not been pre-bowed, the liquid crystal had flowed over the spacer layer. Examining the larger cells, with the pre-warped backplanes, we saw that there was much less LC between the spacer layer and cover glass. In fact there was no observable LC on the spacers toward the edges of the cell and the cells assembled by Begbie [1998] showed no LC over any of the spacer pillars.

4.7.2 Spacer layer geometry

Unlike conventional spacer particles and other spacer materials such as BCB (4.3), our SiO_x spacers patterned by lift-off, could be patterned into almost any geometry down to sub-10μm, without etching with the harmful chemicals which attack the aluminum mirrors. Although pillars were sucessfully used in our method of flattening the device backplane and setting the cell gap thickness, they tended to cause defects in the liquid crystal during cell filling. Possibly, a better geometry of spacer layer would consist of a series of fences running the length of the display. These fences would section off the display into smaller cells, which fill simultaneously. As mentioned in section 4.4.3 the spacer layer geometry was extended to cover at least the same area as the coverglass. In the future, issues such as the spacer distribution density needs to be investigated to determine the effect of the spacer pillars on the texture of the LC (*i.e.,* the number LC defects). Colgan *et al.* [1998] has used finite-element modelling to determine the optimum spacer distribution density required to produce the flatest possible backplanes. The spacers in our investigations were to be patterned on top of the mirrors for a number of reasons, the first due to the ability to fabricate pillars(features) between the mirrors. It was considered impossible to fabricate mirrors using lift-off into a high aspect ratio gap [Stevenson, 1998]. Other considerations such as ECR-PECVD deposited silicon dioxide growth rate and loss of pattern resolution during photoresist exposure due to light scattering futher made patterning a spacer layer between the pixels less feasable. Having said that, the thin mirror process, which has been developed, should eliminate most of these problems. Various authors have presented strong experimental evidence that the LC orientation is influenced by surface adsorption and hydrodynamic flow [Bodammer, 1998]. Therefore, in an effort to maintain the desired straight flow front during cell filling, we designed a spacer layer mask consisting of fences running the length of the display. These and other spacer geometries will be fabricated and tested by others in the A.O. Group.

4.8 Discussion

I have reviewed the main LC cell spacing and backplane flattening techniques reported at the time of writing. At the start of these studies there were no working LCoS devices within the A.O. Group. One of the main issues hindering the group in the manufacture of devices with an acceptable optical quality was that of the liquid crystal thickness uniformity and backplane flatness. We have demonstrated three techniques of flattening bowed silicon backplanes. All three techniques rely on robust microfabricated silicon dioxide spacers on the silicon backplane which serve to protect the delicate pixel mirrors as well as setting the required cell gap. Although the flatnesses achieved and hence the cell gap uniformities were good, the backplanes produced were still not flat enough for use in coherent light applications. Particulate contamination and the spacer layer geometry were found to be the limiting factors in obtaining the flatnesses required. My studies have, however, demonstrated techniques which enable the construction of devices which can be used in non-coherent light applications (*i.e.*, displays). This work has also served to highlight and address some of the problems present when assembling such cells. These problems included those of the potential for poor cell gap uniformities due to the thick ECR-PECVD deposited spacer layer aligning marks in the cell gap and adhesive encroachment into the device array during cell construction. There are still issues remaining which need to be addressed before it is possible to use these techniques for the manufacture of FLCoS devices, but these techniques will enable the A.O. Group to manufacture NLCoS devices with a level of LC thickness uniformity not possible before these studies.

Chapter 5.

Microfabricated Layer Characterization.

5.1 Introduction

A precise control of both the absolute value and uniformity of the LC cell thickness is required for high contrast and good uniformity. It is therefore very important that we can accurately set the liquid crystal cell gap thickness, chapter 4. In order to do this we must characterize the spacer layer patterning and deposition processes. This section will start by describing the spacer layer fabrication process in some detail. The results of the patterning characterization followed by the deposition optimization are then discussed.

5.2 Spacer layer fabrication by lift-off

A lift-off procedure was used to pattern the silicon dioxide spacer layer because the presence of the underlying aluminum mirrors was not compatible with chemical etchants. Control of the step, edge and sidewall coverage was critical for providing a "weak link" to permit the seperation of the deposited silicon dioxide film. The silicon dioxide was deposited over a patterned sacrificial layer, which can be removed by mechanical, chemical or chemo-mechanical means, so "lifting" the unwanted material from the surface. Several methods of "lifting" the undesired material were available, but they all relied on a solvent or etchant to dissolve the sacrificial layer. Typical photoresists are quite soluble in acetone or other organic solvents. Subsequently, the unwanted material and the sacrificial layer are floated or scrubbed off the surface of the wafer with agitation, a high pressure spray or other mechanical means.

The wafers were thoroughly cleaned prior to the treatment with an adhesion promoting Hexa-Methy-Di-Silazane (HMDS) vapor prime and coating with photoresist, figure 5.1. The photoresist, Shipley SPR2, was spin coated @ 5.4Krpm to a thickness (typically 1.2μm of phototresist for <1μm spacers) exceeding that of the desired ECR-PECVD deposited silicon dioxide spacer layer height. Following the soft bake cycle of 110°C for 60 seconds, the photoresist layer was exposed to UV via the spacer layer mask. The chlorobenzene soak, described in 2.10.2, effectively hardened the top surface of the photoresist leaving the characteristic lift-off profile after developing. To prevent particulates, 4.4.1, becoming trapped in the spacer layer, the wafers were subjected to a thorough rinse in de-ionized water and then dried in a N_2 stream. The spacer material was deposited at a low temperature, by ECR-PECVD, 2.6.3. The last stage was lift-off - this was achieved by ultrasonic scrubbing in acetone. The wafers were then rinsed in isopropanol and dryed in a N_2 stream.

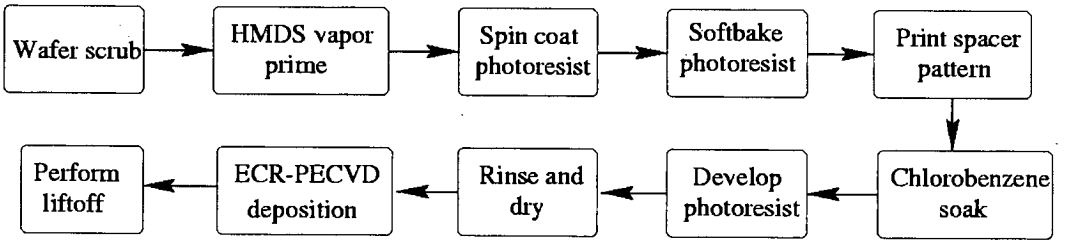


Figure 5.1 Spacer layer fabrication procedure.

5.3 Patterning optimization and characterization

In order to provide the best in-house resolution, with the Optimetrix g-line 5X 8600 series printer, the photolithography process was optimized. Three (bare) 3" diameter silicon wafers spin-coated, see figure 5.2, with 1.6, 2.4 and 3.6μm soft baked (110°C) photoresist (HPR206) were patterned with a test mask on an exposure matrix, in which the exposure durations varied from 2000*ms* to 7500*ms*. The wafers were then soaked in chlorobenzene and developed in Microposit 351 at room temperature (19°C) in 30 second intervals. The main reason for choosing to develop the photoresist manually was that the 4" product wafers could not be handled by the two

SVG track systems, available in the EMF, see appendix D. As a guide to the exposure duration required, for a specified photoresist layer, the smallest feature developed on each wafer was determined. It was found that the thicker resist layers were, as expected, more difficult to pattern with the smallest feature sizes and over exposure of the thinner resist layers lead to all the features being lost. The optimum exposure time for the HPR206 photoresist was found to be around 4000*ms*, see figure 5.3. Thinner layers of photoresist were obtained from SPR2 photoresist, which could be coated automatically on the SVG track using the standard program to a thickness of 1.2μm. The standard exposure time for this photoresist, over silicon, was 1400*ms*.

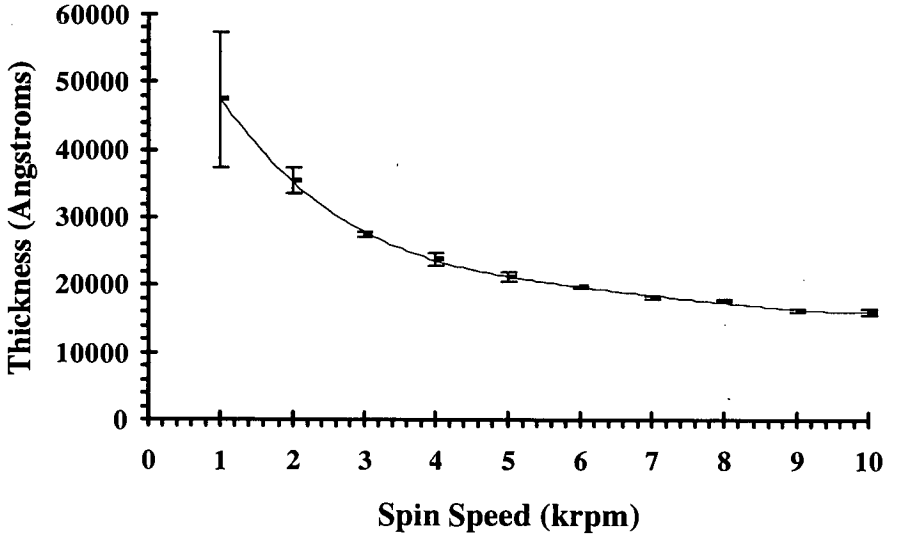


Figure 5.2 Spin speed curve (HPR206 photoresist).1.2μm was obtained by spin coating SPR2 photoresist at 5.4krpm[1], where the standard deviation of the resist thickness across a 75mm diameter wafer is shown by the error bars.

[1] HPR206 photoresist was used to obtain thicker layers of photoresist. Although it can be spin coated to thicknesses as low as 1.6μm, this is not recommended as the high speeds required cause unnecessary wear of the coater bearings. Instead SPR2 is used in the fabrication of our 0.8μm spacer layers.

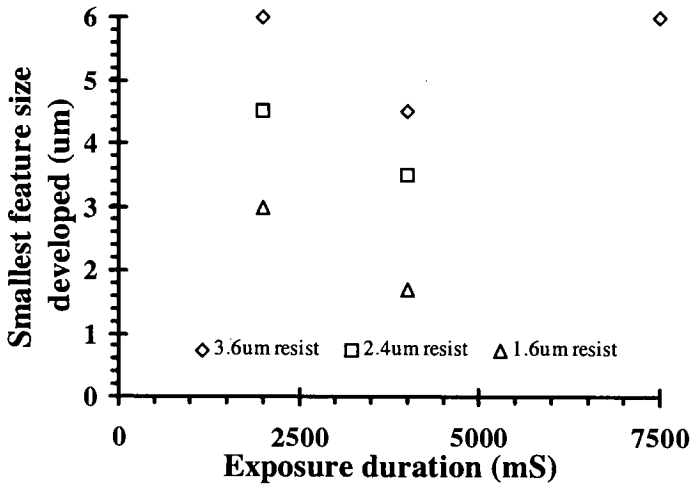


Figure 5.3 The smallest feature sizes developed in HPR206 on the exposure matrix. All of the features in the thinner resists were over developed with excessive exposure.

5.4 Patterned feature characterization

In this section we will describe the characterization of the spacer layer patterning process.

5.4.1 Deposition rate versus geometry

The deposition rate of the ECR-PECVD silicon dioxide was found to be dependent on the aspect ratio of the patterned photoresist layer due to a depletion of the reactant gasses in the deep trenches. It was important that the factors which may affect the deposition rate of the ECR-PECVD silicon dioxide were known. A mask was designed, figure 5.4, which took into account the following factors:

(1) Spacer width (constant length 200μm and spacing 50μm).

(2) Spacer length (constant width, from 1μm to 20μm and spacing 50μm).

(3) Spacer seperation (constant length 200μm and width, from 1μm to 25μm).

(4) Spacer orientation (right angles)

(5) Corner effects (constant spacing 50μm and widths varying from 1μm to 25μm).

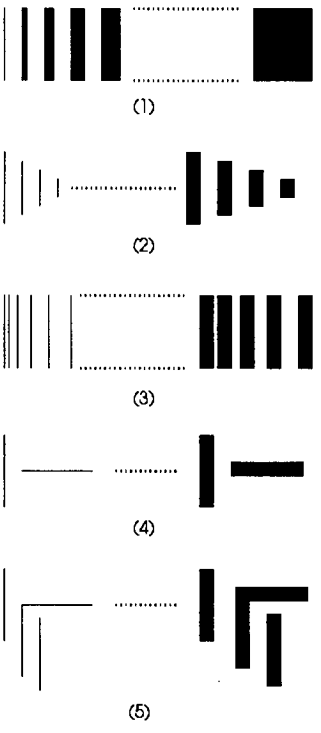


Figure 5.4 Spacer layer patterning characterization test patterns. (1) width, (2) length, (3) separation, (4) orientation and (5) corner effects are examined.

In this experiment three wafers were coated with photoresist to thicknesses of 1.2μm, 1.9μm and 2.6μm, respectively. The wafers were then patterned with the test mask design, see appendix E, as described in section 5.2. The spacer/feature height and geometries were measured with a surface profileometer (Sloan Dektak 8000)[2], with a 2.5μ*m* radius diamond tip, figure 5.5. It was found that the main factor which affected the feature height was the width, see figure 5.6. The length of the spacer only effected its height when it was of a similar magnitude to the width <10 μm.

[2] It should be mentioned at this point that consideration must be given to the possibility of errors in measurement due to the stylus tip profile. Tall features tend to follow the profile of the stylus much more than the smaller features. As the spacer features, under investigation, were ≤ 0.75μm in height we were able to measure the feature widths with a high degree of certainty that the traces we saw were accurate representations of the spacer cross sections (evident from the near vertical walls in the traces). The surface profiler was calibrated against a standard which is traceable to the National Institute of Standards and Technology.

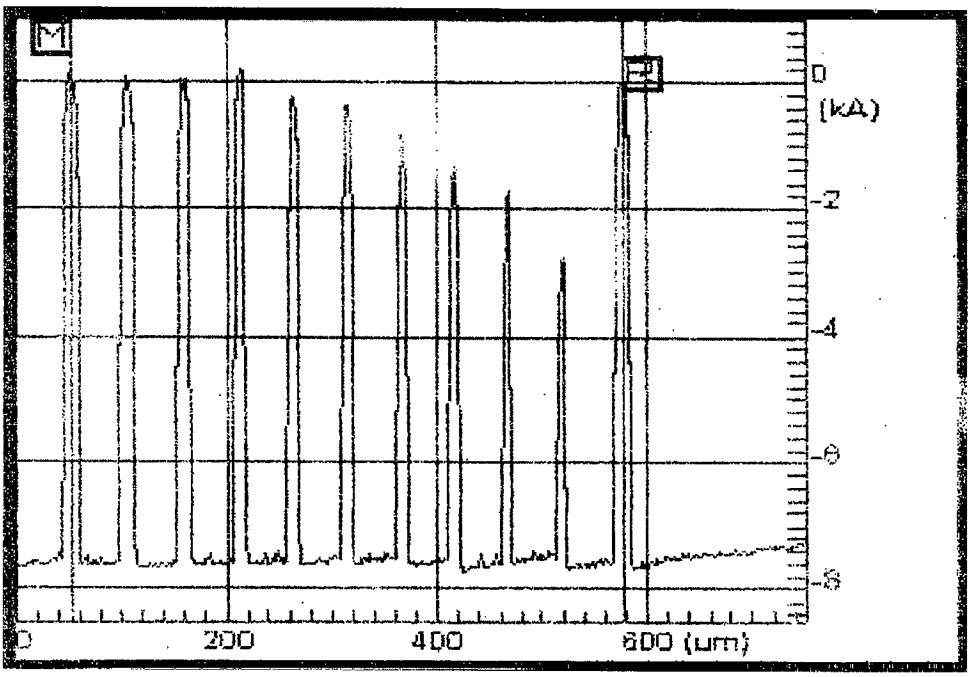


Figure 5.5 Dektak trace of a section of the test pattern showing how the spacer height (kÅ) varies with its width (μm). The outer features are for reference and leveling of the trace.

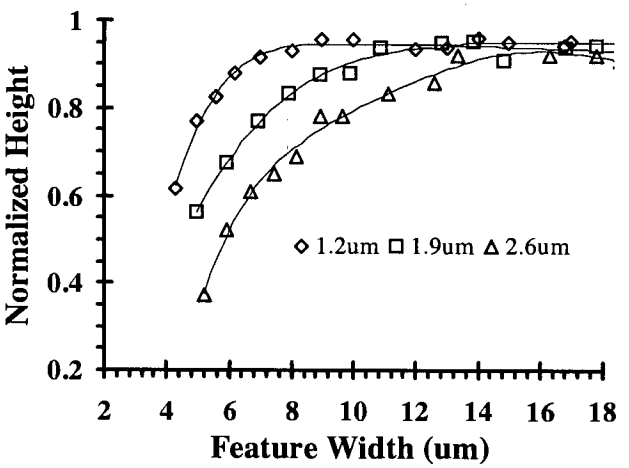


Figure 5.6 Spacer height vs. width with various photoresist thicknesses. Note: The widths of the features were measured from approximately 2/3 of the height from the base.

5.4.2 Deposition rate versus time

From the spacer layer characterization experiments, section 5.4, it could be seen that the deposition rate of the patterned spacers depended on the aspect ratio of the patterned photoresist stencil. We then needed to know whether the deposition rate was time dependent. As the deposition progresses we could see, from figure 5.7, that the material being deposited *may* alter the "aspect ratio" of the hole, in the photoresist, in which the spacer layer material was being deposited. In order to determine whether this effect would introduce any non-linearities into the spacer deposition/patterning process three identical silicon wafers (1,2 and 3) were coated with 1.2μm of Shipley SPR2. The spacer characterization pattern, appendix E, was printed on the wafers and the photoresist developed in Microposit 351 as described in 5.2. ECR-PECVD silicon oxynitride (table 5.3, recipe 16) was then deposited onto wafers 1, 2 and 3 for 20, 40 and 60 minutes, respectively.

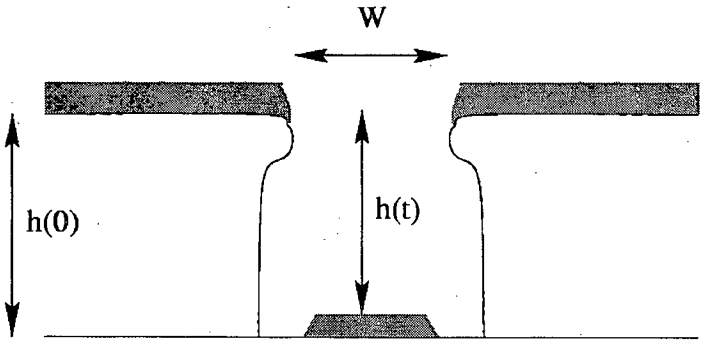


Figure 5.7 Lift-off profile. Aspect ratio is given by h/w.

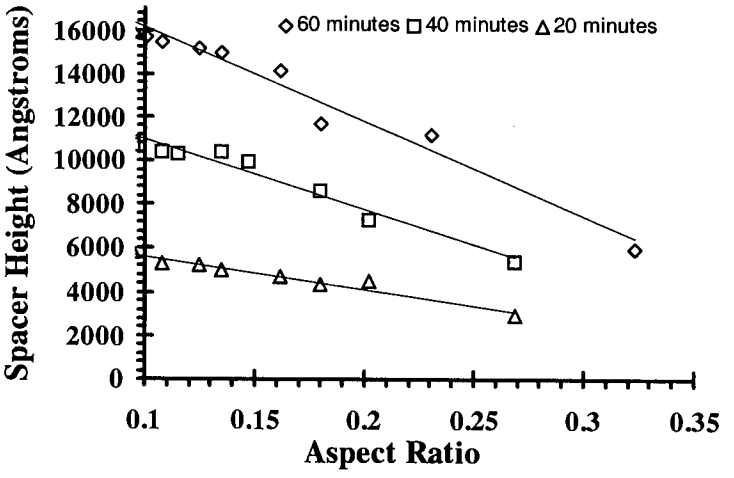


Figure 5.8 Deposition thickness after 20, 40 and 60 minutes.

The height and width of the features were measured with the surfaceprofileometer, as in 5.4. It was found that, under the conditions stated, the feature deposition rate could be assumed to be constant, over the range shown, see figure 5.8.

5.5 Spacer layer deposition uniformity

In addition to having a high thickness uniformity and thickness tolerance the spacer material used must be robust, inert to the LC and have a strong adherence to the substrate on to which it is deposited. The deposition method must also be capable of depositing the spacer material at close to room temperature for it to be compatible with the lift-off process described in 2.10.2 and 5.2. The only method known to date of achieving these results was ECR-PECVD, see 2.6.3. SiN was considered as a harder and more robust alternative to SiO_x, but unfortunately it was found that the uniformity of the standard recipe was much poorer than that of the standard SiO_x recipe. The reason for the poor uniformity of our in-house SiN may have been due to the absence of NH_3 in the process [Sherman, 1987]. Compacted ECR-PECVD silicon oxynitride, which again was harder and more robust than the standard SiO_x was also discovered to be incompatible with the lift-off process. It was found that the residual solvents in the soft baked photoresist outgassed, during the film deposition, causing the oxide/resist to blister. The subsequent removal of the unwanted material then became much more difficult than when the uncompacted SiO_x was used. Even with a prolonged lift-off and cleaning cycle, material was still found at the edges of the spacer layer, figures 5.9, 5.10 and 5.11.

5.6 ECR uniformity optimization experiment

The aim of this experiment was to find a recipe which allows us to obtain the best possible deposition uniformity with the the Oxford Plasma Technology ECR-PECVD reactor. A good thickness uniformity was very important, both within a die area and on a wafer scale to enable us to set an accurate FLC cell gap. The characteristics of the ECR-PECVD system could be changed significantly by altering the process parameters. For example by altering the gas flow rates it was possible to change the glow discharge behaviour even if the power and pressure remained unchanged. This could have a huge effect on the thickness uniformity of the deposit as well as its stoichemistry. Since no theoretical description of such a complex system existed at

the time of writing, the reactor had to be characterized to obtain the best deposition thickness uniformity [Sherman, 1987]. As there were many factors which may have affected the deposition uniformity a designed experiment was performed to gain the maximum amount of information with the least number of experimental runs.

The film refractive indices and thicknesses were measured with an Applied Materials Ellipsometer II and Nanospec AFT, respectively, see appendix E. A sample of the AFT measurements was also checked with the Dektak, which was found to be in close agreement.

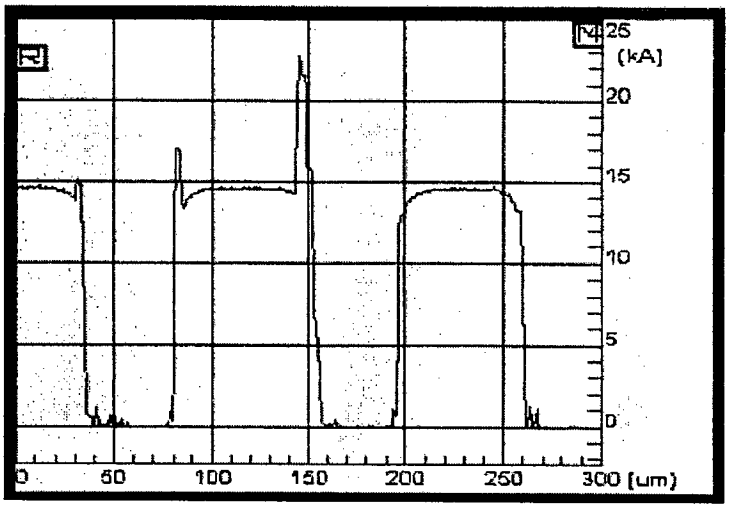


Figure 5.9 Surface profileometer trace of feature, center, in which lift-off is incomplete. The spikes show the presence of unwanted material.

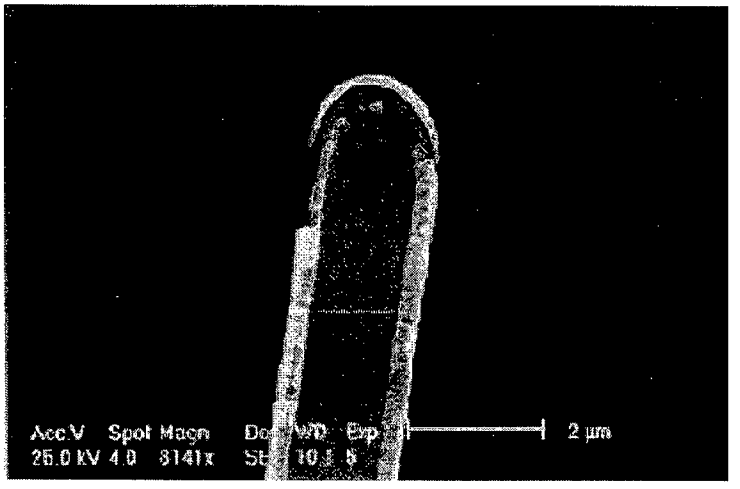


Figure 5.10 SEM micrograph of an uncompacted SiO_x spacer in which lift-off is incomplete. The unwanted material can be seen around the perimeter of the feature. This is illustrated further in the figure below.

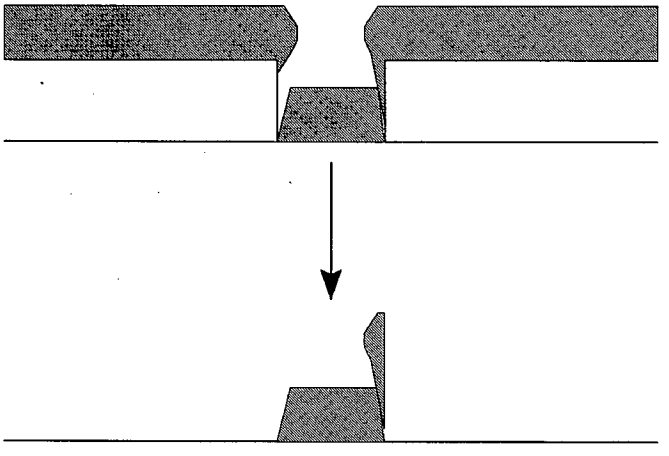


Figure 5.11 Burr formed after removal of photoresist and oxide layers.

If the photoresist layer was too thin and/or too much oxide was deposited or there was an improper trench edge definition (over hang in the photoresist) burrs could be formed at the edges of the patterned features as shown above. To overcome this problem the wafers were coated with a thicker layer of photoresist, see figure 5.1 (spin speed curve), to prevent burrs forming. Ultrasonic scrubbing also helped by removing any existing burrs.

5.6.1 Screening

In a conventional PECVD process, there are three main variables to control: plasma, pressure and gas composition, compared to an ECR-PECVD process, in which there are five major variables: the magnetic field, microwave source, as well as the magnetron plasma, pressure and gas [Kearney, 1989]. Obviously even if we did perform the designed experiment with just the major variables, there would have been far too many runs to perform. It was therefore necessary to run a screening experiment to reduce the number of variables with which we would perform the experiment allowing only the most significant and/or controllable factors to be investigated. Of the possible variables, table 5.1, we needed to select the three which had the greatest effect on the film uniformity, see chapter 2. Unfortunately, the limitations of the Oxford Plasma Technology ECR system dictated the factors which were to be used in the optimization experiments. Major variables affecting the film deposition range and uniformity were rf power density and distribution, gas phase composition and distribution, and total pressure in the reaction zone. Of greatest importance was the distribution of power density, because the lifetimes of the reactive species are generally very short lived and must be continually generated and regenerated across the deposition zone [Levy, 1989].

#	**Factor**
1	Silane (SiH_4) flow rate
2	Nitrous Oxide (N_2O) flow rate
3	Table Height
4	Table/Wafer temperature
5	Chamber pressure
6	Microwave (MW) Power
7	Argon (Ar) flow rate
8	RF power
9	Magnet currents

Table 5.1 List of possible variables.

We were able to eliminate five of the variables, from our experience of the ECR deposition process. The table height was set to 100mm to give the maximum vertical distance between the silane shower ring and the wafer, as the plasma profile in this part of the chamber was cone shaped. The table was liquid cooled and was only heated by the ion bombardment *etc.*, during film deposition, so there was little control of the wafer temperature. The chamber pressure was also difficult to control accurately. The magnets were used to shape the plasma, see section 2.6.3, and were set up for resonance [Ruthven, 1997].

RF power	0W
Wafer temperature	38-40^{0}C
Chamber pressure	~5 x 10^{-8} torr
Argon flow rate	0sccm
Magnets 1&2	130 and 55A

Table 5.2 Setting which we had little or no control over with the OPT reactor.

This left factor numbers 1,2,6,7 and 8 in table 5.1. The Argon flow rate, 7, and RF power, 8, were known to be incompatible with the lift-off process and was also eliminated from the list.

5.6.2 Input parameter level settings

The factor space to be investigated was determined from known level settings. The level settings not only affected the film composition, uniformity *etc.;* certain combinations may have also prevented the plasma from striking. The three remaining factor levels were determined, from existing deposition recipes, to be SiH_4 (100 sccm to 125 sccm)[1], N_2O (20 sccm to 35 sccm) and the microwave power (300W to 500W). The mid-points were then set as 113 sccm, 28 sccm and 400W, respectively, to estimate any curvature in the reponse that might exist in the factor space being investigated.

[1] Nominally 4.09% SiH_4 in He

5.6.3 Orthogonal table for deposition optimization.

The matrix experiment was designed by drawing up a table of the factors to be investigated, see table 5.3.

A matrix can be called orthogonal if and only if the following requirements are met:

1) The number of occurences of each level setting must be equal within each column.

2) All rows having identical level settings in a given column must have an equal number of occurances of all other level settings in the other columns.

3) The matrix for a given number of columns must be the one with the minimal number of rows that satisfy the above conditions.

The matrix in table 5.3 satisfies all of these requirements. A more detailed description of orthogonal matrix design is given in [Yin, 1987] and [Wolf, 1986].
Response, %U, is given by

$$\%U = \frac{(\max - \min)}{(\max + \min)} x100\% \qquad (14)$$

The responses selected were the deposition uniformity, %U, defined by equation 14, the deposition rates and refractive indices of the film, table 5.3. Although the latter two responses were not used in the optimization experiment, they were referred to in later sections.
The main effects for each individual factor are defined to be the difference between two averaged responses.

The sequence of experiments were randomized to allow any parameters, such as temperature variations, to have an equal opportunity to effect all the experimental runs.

Run #	*SiH_4 (sccm)*	*N_2O (sccm)*	*MW (W)*	*%U*		*Avge dep. rate (Å /min)*	*Refractive Index (n)*
1	113	28	300	U1	2.60	106	1.43
2	113	28	400	U2	2.68	220	1.42
3	100	20	300	U3	1.45	167	1.38
4	113	35	400	U4	1.87	222	1.45
5	125	28	400	U5	2.26	287	1.40
6	113	28	400	U6	2.60	297	1.42
7	113	28	400	U7	1.86	258	1.42
8	113	28	500	U8	4.28	314	1.40
9	113	28	400	U9	2.84	279	1.42
10	100	35	300	U10	0.75	166	1.40
11	100	35	500	U11	3.41	279	1.41
12	113	28	400	U12	2.90	283	1.42
13	100	28	400	U13	2.71	258	1.40
14	125	20	500	U14	5.95	348	1.36
15	100	20	500	U15	3.93	266	1.40
16	125	35	300	U16	0.40	206	1.42
17	113	20	400	U17	3.21	281	1.42
18	125	20	300	U18	1.24	207	1.42
19	125	35	500	U19	2.00	290	1.40
20	113	28	400	U20	1.44	254	1.42

Table 5.3 Experiment run sheet. Highlighted are the runs which gave the best and worst deposition uniformites. The latter happened to be the recipe used as standard in all non-planar depositions carried out by the EMF.

$U_{silane1}$	2.450	$U_{nitrous1}$	3.156	U_{mw1}	1.288
$U_{silane2}$	2.928	$U_{nitrous2}$	2.906	U_{mw2}	2.546
$U_{silane3}$	2.370	$U_{nitrous3}$	1.686	U_{mw3}	3.914
ΔU	**0.558**		**1.470**		**2.626**

An initial visual inspection of the wafers indicated that films on wafers 10 and 16 were extremely uniform, whereas the other wafers exhibited varying degrees of non-uniformity ("bulls eye" effect). A first order data analysis, which is sufficient in the vast majority of process optimization and characterization experiments, was performed as follows [Yin, 1987]:

The arithmetic mean for each level setting for each input parameter is determined, table 5.4. The average of the repetitions was 2.39 with a standard deviation of **0.596**.

$U_{silane1}$= 1/5 (U3+U10+U11+U13+U15)	$U_{nitrous1}$= 1/5 (U3+U14+U15+U17+U18)	U_{mw1}= 1/5 (U1+U3+U10+U16+U18)
$U_{silane2}$= 1/5 (U1+U2+U4+U8+U17)	$U_{nitrous2}$= 1/5 (U1+U2+U5+U8+U13)	U_{mw2}= 1/5 (U2+U4+U5+U13+U17)
$U_{silane3}$= 1/5 (U5+U14+U16+U18+U19)	$U_{nitrous3}$= 1/5 (U4+U10+U11+U16+U19)	U_{mw3}= 1/5 (U8+U11+U14+U15+U19)
	$\Delta U = U_{(max)} - U_{(min)}$	

Table 5.4 Formulae for calculating the output function averages and differences.

Comparing the standard deviation of the repetitions value (0.596) with the output function differences, ΔU, we can see that the effect of the silane flow rate on the deposition uniformity is of a similar value, and is therefore not significant over the range studied. This was not really surprising as the silane was introduced, into the plenum chamber, away from the area where the plasma was generated 2.6.3. ΔU for the nitrous oxide and microwave power were, however, much larger than the standard deviation of the repetitions, which meant that they were significant, see figure 5.12.

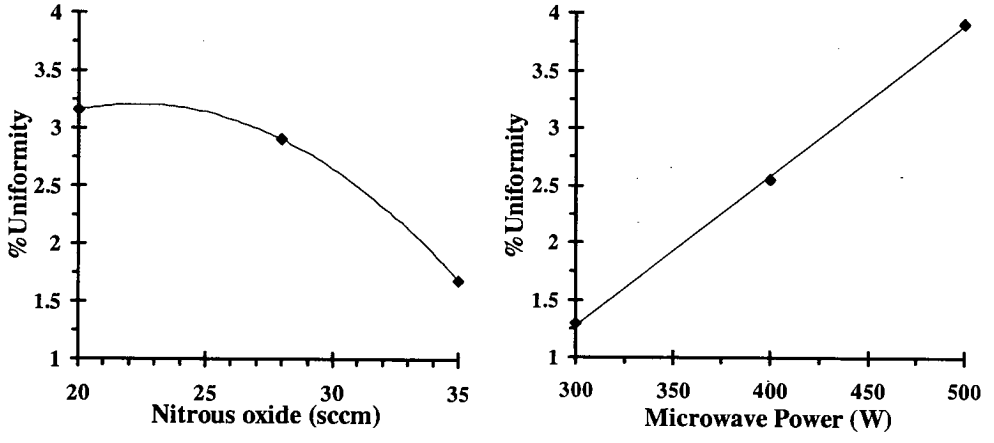


Figure 5.12 First order effects. MW power had the greatest effect, followed by the nitrous oxide flow rate, on the deposition thickness uniformity.

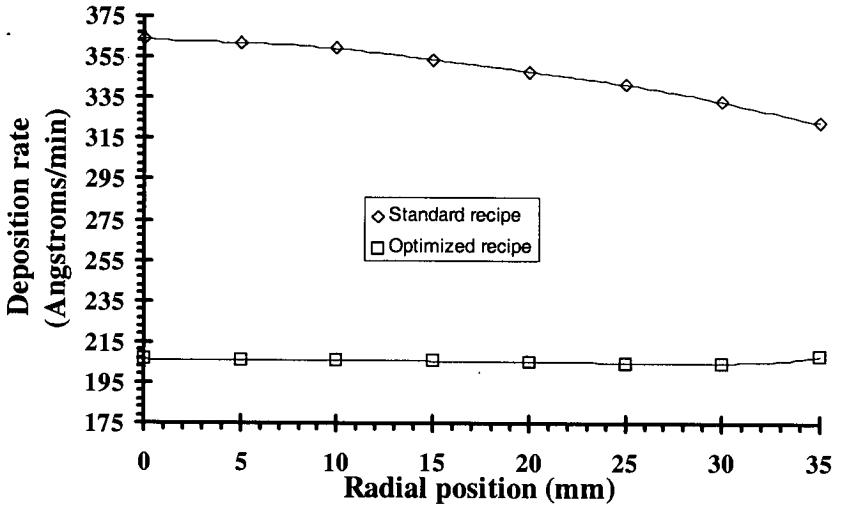


Figure 5.13 Deposition rate across the two test 75mm wafers from the center, 0mm, to the edge, 35mm.

Run 14, table 5.3, was the standard recipe, deposited by the EMF. It could be seen that this was the worst recipe in terms of deposition uniformity (5.95%) for the spacer layer deposition. The uniformity of the optimized recipe, run 16, was found to be as low as 0.4%, see figure 5.13.

5.6.4 Properties of the spacer material

A measure of the film composition/quality, which is commonly used in industry, can be obtained from the refractive index and buffered oxide etch (BOE) rate data. It was found that the film BOE rates, of these ECR-PECVD films, were too high to be measured, which indicated that the films were porous. A dry etch approach was therefore used to determine the film etch rate of the films. A Plasmatherm radial flow reactor (PK 2440 RIE), with a fluorine based chemistry, was used to determine the film dry etch rate, with the reactor parameters listed in table 5.5.

CHF_3 Flow Rate	75sccm
He Flow Rate	15sccm
RF Power	750W
Base Pressure	1mT
Temperature	44°C

Table 5.5 Silicon oxide RIE parameters.

The refractive indices of the films, table 5.3, were low compared to that of thermally grown SiO_2, (1.46 @ 633nm), which also indicated that the films were indeed porous. The plasma etch rate of the optimized spacer layer recipe (run 16, table 5.3) was measured to be 400Å/min compared to that of the standard recipe (run 14) of 270Å/min. Although the un-compacted ECR-PECVD SiO_x films were very porous, their strength was not a real concern as the ECR-PECVD silicon oxide pillars would be patterned into fairly rigid structures, compared to the conventional (spherical / cylindrical) silica spacer particles, figure 5.14. The first generation of devices were to have spacers patterned on top of the mirrors which would be 8μm wide and between 0.8 and 2.4μm high.

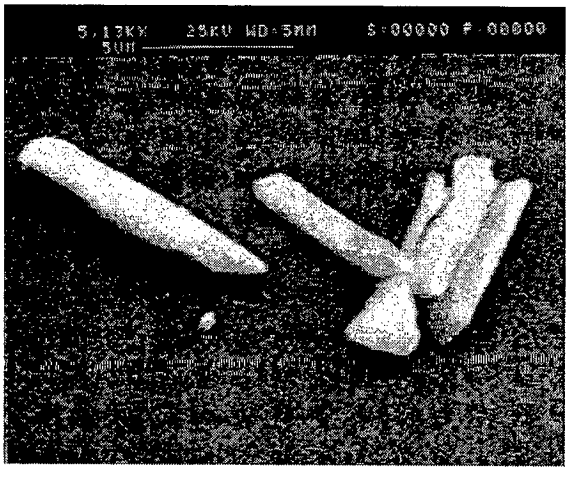


Figure 5.14 SEM of a silica spacer rod fractured along its long axis. Courtesy of M. Begbie.

5.7 Spacer layer growth rate

As the first generation of spacer layers were to be deposited on the aluminum pixel mirrors, we needed to know how its deposition rate differed from that on silicon/silicon dioxide. Increasing the deposition temperature increases the film deposition rate [Sherman, 1987]. Because the emissivity of SiO_2 is much higher than that of aluminum the surface of the SiO_2 will radiate heat more efficiently and reach a lower steady state temperature than the aluminum [Sherman, 1997]. To measure the deposition rates on the two substrates a patterned aluminized silicon wafer was

blanket deposited with ECR-PECVD SiO_x and the SiO_x film thickness measured, with a Nanospec AFT, both on the silicon and aluminum. The ECR-PECVD SiO_x deposition rate below, was found to be ~14% higher on aluminum than on silicon.

Substrate material	Deposition rate
Aluminum	241Å /min (σ=4.5)
Silicon	212Å /min (σ=0.9)

Table 5.6 ECR-PECVD deposition rates on aluminum and silicon.

5.7.1 Repeatability of deposition and patterning process

To set accurately the LC spacing, the spacer layer thickness must be known to within a high tolerance. Unlike other types of plasma deposition/etch reactors, the geometry of the Oxford Plasma Technology ECR reaction chamber did not facilitate the use of an optical thin film thickness monitor, which would have been needed to be positioned above the wafer. Therefore, the film deposition rate on specific substrates under specified conditions, must be known and highly repeatable. From the repetitions, performed in the optimization experiment, 5.6.3, table 5.3, we saw that the standard deviation of the deposition rates, σ, was 27Å/min. Clearly, this inconsistency in the deposition rate was unacceptable, for our application, and needed to be improved upon.

An explanation for this poor repeatability was that the table/wafer heating during reactor operation was the cause of the change in deposition rates [Ruthven, 1997]. To test this hypothesis an investigation was carried out in which five depositions were performed, one directly after the other, with a minimal time delay between them, see table 5.7.

Wafer #	1	2	3	4	5
Average film thickness (Å)	8099	8071	8028	8153	8039

Table 5.7 Process time 30 minutes (target thickness 8000Å). The mean thickness, measured by the Nanospec AFT, is 8087Å with a standard deviation of σ = 50Å.

The standard deviation of the deposition rates in this case was found to be much lower, only 1.68Å/min. From these results we concluded that the best deposition rate consistency, within a batch of wafers, occured when the batch of wafers were coated with the shortest possible time delay between depositions. Prior to each "batch" of runs the deposition rate should be re-calculated. Of equal importance, to the above, was the repeatability of the photoresist patterning process. At the feature sizes we were interested in, any variation in the feature width would ultimately affect the spacer height, 5.3.

Three wafers coated with photoresist were printed and developed, as described in 5.2, over a period of days. Upon measuring the width of the patterned photoresist features, we found that there were no significant variations between them, and the measured height of the patterned ECR spacers on each wafer was very close to our predicted value.

5.8 Summary

The spacer layer patterning process has been characterized to enable us to pattern spacers to a known thickness. At the start of these investigations the ECR-PECVD SiO_2 film deposition process was not set up for depositing LCoS spacer layers. In fact the standard recipe used by the EMF was of a very poor deposition thickness uniformity. The deposition thickness uniformity has been optimized and the deposition thickness repeatability has been drastically improved, see table 5.8. These fully characterized and optimized spacer layers now present the opportunity to fabricate <1μm thick FLC cells to fully utilize the potential of FLC.

Before investigations	After investigations
Masks designed which did not account for effects of spacer layer geometry.	Spacer layer patterning was characterized.
ECR-PECVD deposition uniformities of 5-6% over a 75mm diameter wafer was available.	Optimized uniformity of <1%
	ECR-PECVD SiO_2 growth rate on silicon and aluminum determined (14% difference in deposition rates)
Repeatability of the ECR-PECVD SiO_2 deposition process was unacceptably low (standard deviation of 27Å/min)	Process was optimized to produce deposition rate with a standard deviation of 1.68Å/min between wafers.

Table 5.8 Improvements to the spacer deposition and patterning process following these investigations.

Chapter 6

Transparent Conductive (ITO) Layer Enhancements.

6.1 Introduction

The transparent conductive Indium Tin Oxide (ITO) layer on the inner-surface(s) of LC devices is important as it allows voltages to be applied across the LC cell thus switching the LC layer as well as allowing the device to be optically interogated. ITO is a transparent (in the visible), highly degenerate wide bandgap semiconductor used extensively in the liquid crystal display industry in which the conduction carriers in the ITO come from the tin dopants and oxygen vacancies. It can be deposited by various methods including sputter deposition and evaporation [Song, 1998], [Uthanna, 1998]. Typically thin films of sputter deposited ITO consist of domains of grains having the same orientation. This grain-subgrain structure is characteristic of sputter deposited polycrystalline ITO. The conductivity of the layer is limited by these domain boundaries, which cause electron scattering [Higuchi, 1993]. The origin of the granular structure has been described by crystalline plane dependent re-sputtering during sputter deposition. The re-sputtering rate is considered to be dependent on the orientation of the crystalline plane of the ITO [Kamei, 1995].

We have identified two problem areas in which this layer can be further processed to improve the optical performance of current LC devices.

(1) The ITO layer can have an extremely rough topology, depending on its deposition conditions, which may adversely affect the alignment of the adjacent LC layer.

(2) The ITO layer, in a typical LC cell, has a refractive index which is significantly higher than that of any of the adjacent layers and therefore it introduces unwanted reflections of the incident light.

In this chapter we will describe the use of a standard polishing process to reduce the surface roughness of the ITO and the optimization of the layer thickness to improve the light throughput efficiency of the device.

6.2 Chemically Mechanically Polished ITO

The alignment of the liquid crystal molecules at a surface is determined by the angle of evaporation of the SiO_x (see section 1). Small or grazing angles of incidence of the evaporant flux generally leads to columnar growth whereas medium angle evaporation gives a corrugated or "ploughed field" morphology. It has been reported that the morphology of the boundary substrates may have an effect on the subsequent SiO_x aligning layer and hence the LC orientation [Gazdag, 1979], [Clark, 1984], [Bodammer, 1996]. ITO coated substrates have two scales of roughness. Long range, from the undulations in the glass, and short range from the rough ITO layer, figure 6.1. The purpose of this investigation was to reduce the roughness of the surface on a small or microscopic scale, which should be conducive to good LC alignment.

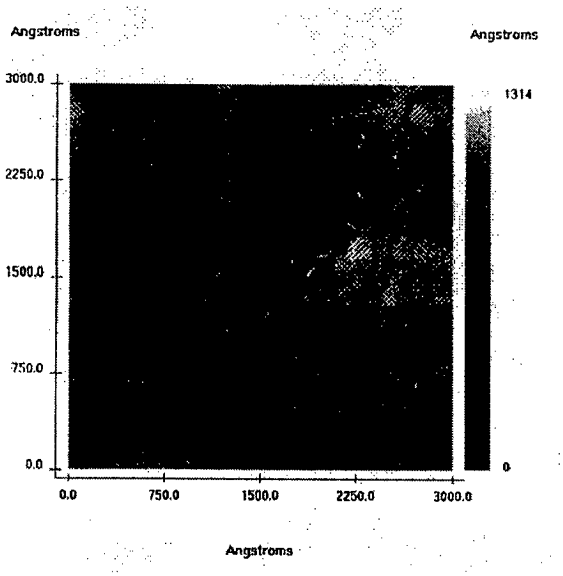


Figure 6.1 Scanning tunneling micrograph of ITO on glass (supplied by Merck). The grain-subgrain structure can clearly be seen[1].

Other methods of "smoothing" ITO have been reported in the past [Fujita, 1997], [Pulham, 1996]. AFM investigations by Fujita *et al.* on ITO surfaces treated by mechanical rubbing, HCl/H_2O dipping and O_2 plasma irradiation have all shown a decrease in the surface roughness. The most marked reduction in surface roughness, however, was reported to have resulted from mechanical rubbing [Fujita, 1997]. Another group which is currently working on this problem is based in the Department of Chemistry, University of Edinburgh. They are developing an electro-chemical polishing process [Pulham, 1996], which removes the ITO material on the "high" points of the film and then re-deposits it on the low points.

6.2.1 Slurry chemistry selection

As ITO CMP was a novel process, no custom polishing slurry chemistry was available. It was decided, following a consultation with the Department of Chemistry [O'Hara, 1996], that we should use the standard SiO_2 slurry, as a starting point.

[1] Liquid crystal molecules are typically 15-20Å in length [Efron, 1995].

6.2.2 ITO polishing and cleaning process

ITO was sputtered in-house as described in section 6.3.1, onto 3" diameter borosilicate glass wafers. The ITO coated wafers were then annealed at 430°C (in air) for approximately 20 minutes.

The samples were polished with a Logitech PS2000 polisher, with the parameters set as given in table 6.1. Prior to polishing, the polish pad on the Logitech system, was conditioned, by replacing the slurry feed with DI water and allowing the system to run with a stainless steel conditioning ring (instead of the wafer), to increase the pads porosity and surface roughness.

The slurry residue was not permitted to dry out at any stage as the zeta[2] potentials present would have caused the slurry particles to bond irreversibly to the substrate, see figure 6.2. As no wafer scrubber was available in the department at the time these experiments were performed, we removed any residual silica slurry contamination by briefly immersing the polished samples in HF/DI[3] water (1:9) for approximately 1-2 seconds followed immediately by a DI water rinse. As the effect of the HF on the ITO was unknown, samples of ITO coated glass, which had not been polished, were examined by STM following this treatment and no obvious change in the film morphology was found.

Logitech PS2000	
Slurry	Colloidal silica slurry type SF1
Pad	Rodel SUBA IV
Platten speed	~35rpm
Wafer/pad pressure	~0.5PSI

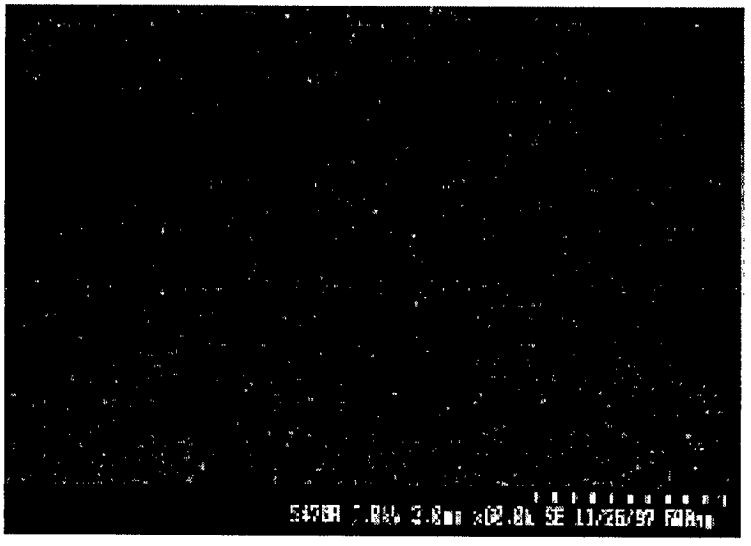
Table 6.1 ITO polishing parameters. Note that the other variables, such as slurry feed rate, platten temperature *etc.*, could not be easily measured using this polisher.

[2] Particles suspended and surfaces immersed in the slurry are usually charged by the adsorption of ions from the solution.

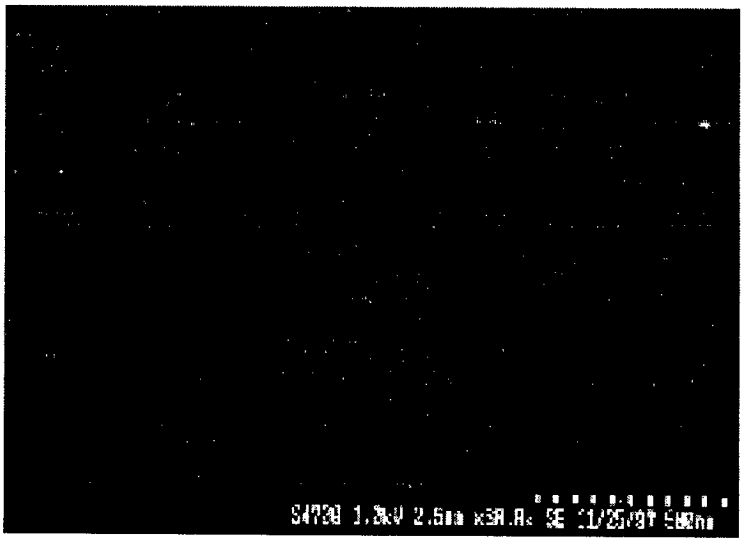
[3] A diluted HF buff has been proposed by Hymes *et al.* [Hymes] to remove post oxide and W CMP by etching of the surface during PVA brush scrubbing.

6.2.3 Polished ITO examination

The polished ITO films were examined primarily by scanning electron microscopy and scanning tunneling microscopy. The surface roughness and step height distribution curves were obtained from scans over an area of 0.76x0.76μm using a Burleigh Instructional STM.

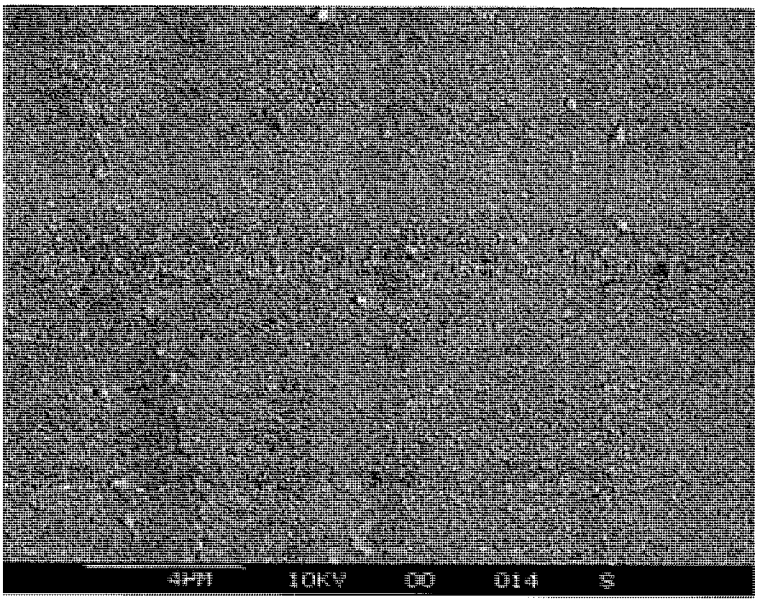


(a) 500nm size bar



(b) 500nm size bar

Figure 6.2 (caption below)



(c) 4μm size bar

Figure 6.2 SEM micrographs of a sputtered ITO (700Å) layer. (a) unpolished (b) polished and (c) polished ITO but with slurry residue. Note the scale on each micrograph.

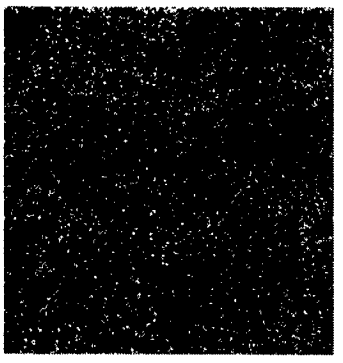
Images from both forms of microscopy revealed that the ITO surfaces were highly textured and exhibited the characteristic polycrystalline grain-subgrain structure of sputter deposited films. Further to this the step height data from the STM scans were used to calculate the surface roughness of the samples.

The roughness (rms) values were calculated by,

$$\zeta = \sqrt{\frac{1}{N}\sum_{i}^{N}\left(h_i - \bar{h}\right)^2} \qquad (14)$$

Here h_i is the individual "pixel" height of the N samples and $\bar{h}$ is the mean height. All images were obtained in the constant current mode using a cut Pt/Ir (80/20) 0.25mm wire tip, with a 2mV bias and tunneling current of 8nA. The scan delay[4] was 1 millisecond. All images were corrected for global tilt, but not further enhanced.

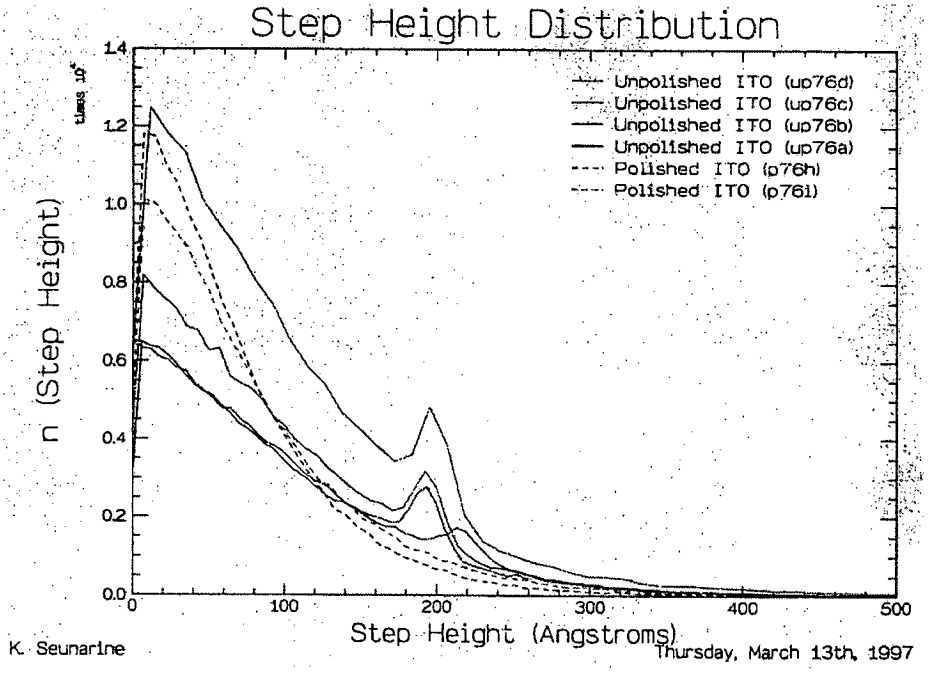
[4] Time the probe takes to aquire the data at each individual measurement point.



Unpolished ITO typical roughness of 134Å rms,

polished ITO typical roughness of 79Å rms.

(a)



(b)

Figure 6.3 (a) Images obtained from Burleigh STM of unpolished(left) and polished (right) "in-house" deposited ITO (b) Step height distribution. Note the secondary peaks in the unpolished ITO (solid) curves, which correspond to the large ITO grains.

In addition to measuring the global surface roughness of the STM images a step height distribution (SHD) analysis was carried out. The SHD is useful because it takes only local correlations into account (the surface roughness over the scan width reflects the global picture, equation 14). It facilitates estimations of the height of

plateaux through peaks in the distribution, which decays exponentially with increasing δh, evident from the curves in figure 6.3. [Bodammer, 1998].

The SHD, n(δh), where n is the number of height differences, was calculated from a 256 x 256 portable grey map (pgm) image obtained from the STM data file. Each pixel in the 256 x 256 image is stored as an 8-bit value which corresponds to a height value in the image. The SHD was then obtained by calculating the height difference, δh, between each pixel and its three nearest neighbors $|h_{ij} - (h_{i+1,j})|$, $|h_{i,j} - (h_{i,j+1})|$, $|h_{i,j} - (h_{i+1,j+1})|$, where $h_{i,j}$ is the height of a pixel at a position in an array of pixels i,j.

The sheet resistances of the in-house sputtered ITO following dc sputtering, after annealing at 430°C and polishing are shown in figure 6.4. As the deposition from the Edwards sputterer had a poor uniformity over large (3" diameter wafers) substrates ("Bulls eye" effect) measurements were taken at regular intervals, from the center to the edge of the wafer.

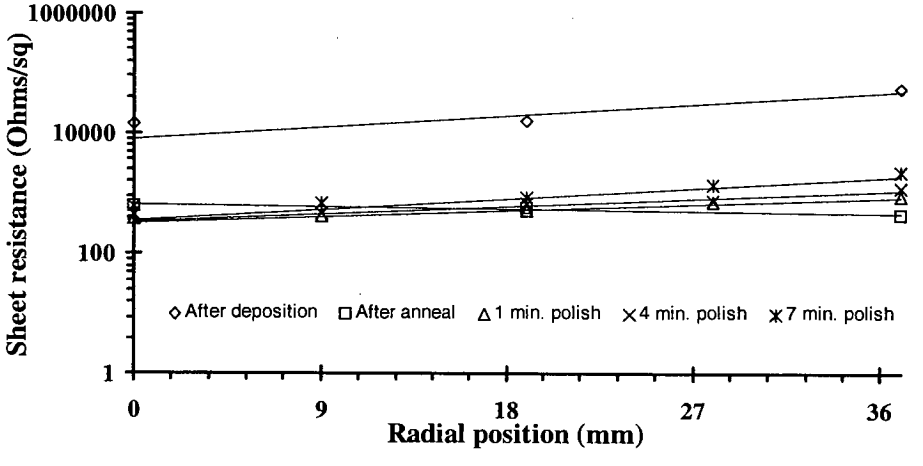


Figure 6.4 (Caption below)

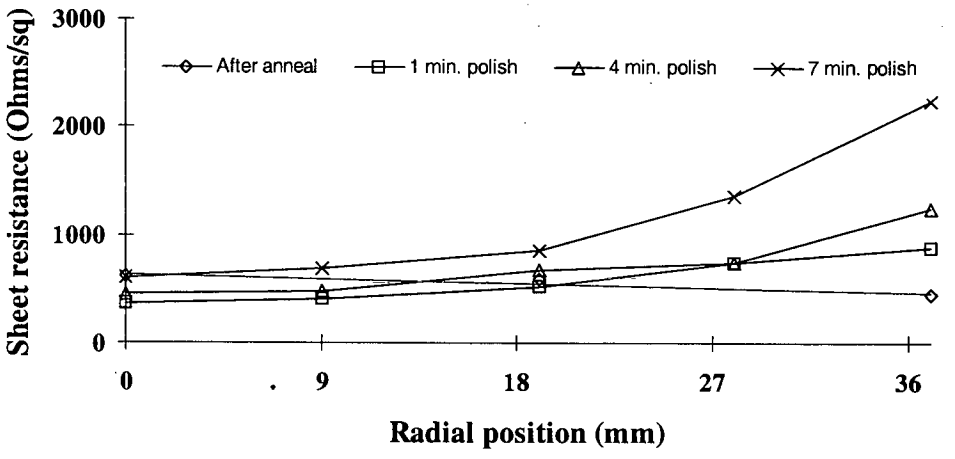


Figure 6.4 Sheet resistance measurements, across the wafer, of the sputtered ITO film. Note that the sheet resistance of our in-house deposited ITO is generally higher than that of the commercially available ITO.

From the curves in figure 6.4, it can be seen that annealing the ITO in air at 430°C drastically reduces its sheet resistance. Polishing of the ITO has only a small effect on its sheet resistance at the wafer center. We only measured an increase in optical transmittance of around 1% (at 633nm) after polishing. Due to over polishing (poor uniformity of polishing) at the edge of the wafer the resistivity increased more significantly in this region[5]. There is virtually no change in the transmission of the samples (at the center of the wafer). Following polishing the samples were all examined with the STM and no improvement of the film morphology found with subsequent polishing, *i.e.,* the ITO was a porous material, which after removal of the larger grains, could not be polished any smoother using this technique.

6.2.4 Oblique SiO LC alignment layer evaporation

The formation of structures during oblique evaporation is attributed to the self-shadowing mechanism. Previously deposited nuclei or molecules at random positions on the substrate prevent particles in the vapor stream from reaching the substrate in the geometric shadow of each nucleus. Consequently, as the evaporation proceeds and the growth of the deposits increase in size, vacant regions are left in the film, and

[5] The Presi polisher will allow us to produce a much more uniform removal rate over the wafer.

individual islands of material eventually coalesce into a two dimensional array of rows whose long axis is approximately perpendicular to the plane of incidence [Goodman, 1976].

6.2.5 Factors affecting LC surface alignment

Relatively few studies of LC alignment have been carried out on ITO coated substrates. As was mentioned in chapter 1, a widely accepted explanation for the surface alignment of LC on an obliquely evaporated film is that the arrangement of the LC molecules minimizes the deformation energy [Faetti, 1991]. Berreman has shown that the elastic energy can be sufficiently large for the topographic mechanism to dominant for NLCs. The basic assumption underlying the theory is that the physiochemical interaction between the LC molecules and the substrate acts only to restrict the director parallel to the local plane of the substrate, while allowing the director to rotate freely in it [Yokoyama, 1984]. Xiao [1997] has shown that the alignment of FLC molecules on ultra thin SiO_x layers evaporated at 80 degrees to the substrate normal are almost planar. His explanation for this is based on Goodmans studies. Although no anisotropic structures were observed by SEM analysis of his SiO_x samples he concluded that the ultra thin SiO_x film at 80 degrees consists of channels which have an average direction perpendicular to the plane of the incident flux, and that the columnar structure, which exists in thicker films deposited at 80 degrees, had not appeared because the film is too thin. Consequently, the channel structure is thought to be the dominant factor in the alignment of the LC and the molecular arrangement is similar to that of the LC on the SiO_x film deposited at 60 degrees. We know that the angle of the incident SiO_x flux leads to two completely different modes of alignment, namely planar (homogenous) and perpendicular (homeotropic)/tilted. If therefore, the substrate presents both a grazing angle and medium angle of incidence to the incoming SiO_x flux, how will the growing film morphology be affected? It can be seen from figure 6.5(a) that a 60nm SiO_x film deposited obliquely at an angle of 60° to the substrate, forms no obvious striations or columnar structures. It is difficult to see how Berreman's model can be applied to

such a surface which appears to be equally rough in all directions. Barberi [1994] has recently carried out a fractal examination of AFM images from obliquely evaporated SiO_x on glass plates. Such a sophisticated analysis of the substrates showed that the usual elastic models for LC planar anchoring could also be applied to this kind of complex surface. Yokoyama [1984], on the other hand, reported that a layer of liquid crystal molecules adsorbed on the SiO_x film plays an important role in aligning the bulk LC. There is evidence that the LC molecules form, by themselves, an anisotropically adsorbed layer in which molecules can no longer rotate freely. Nematic phase hydrodynamic motion is also known to couple strongly with the director exerting a torque which tends to align the director approximately along the flow direction. Although many authors support the Berreman model, there are others who have argued that other effects maybe more dominant in the surface orientation of LC's.

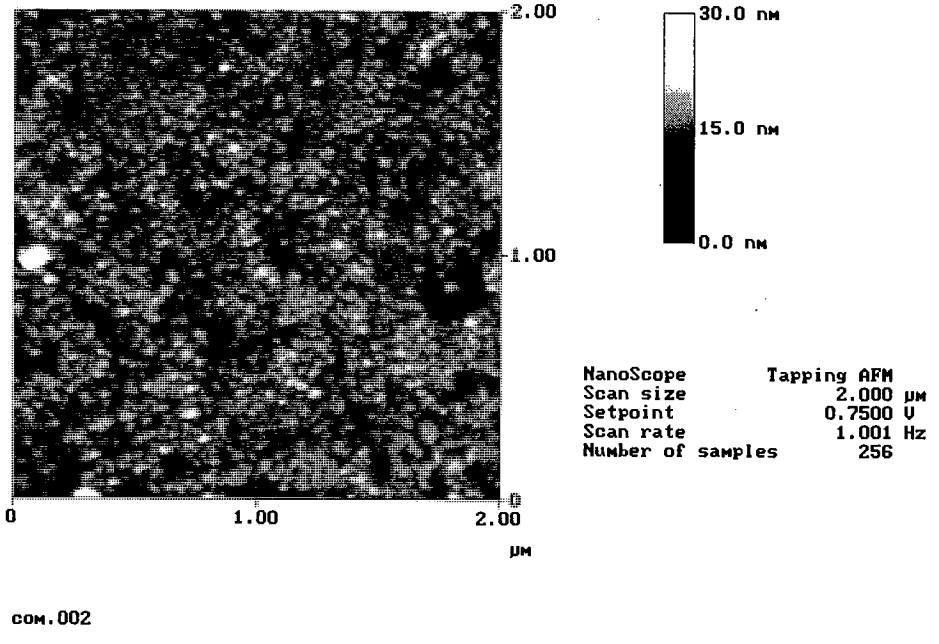
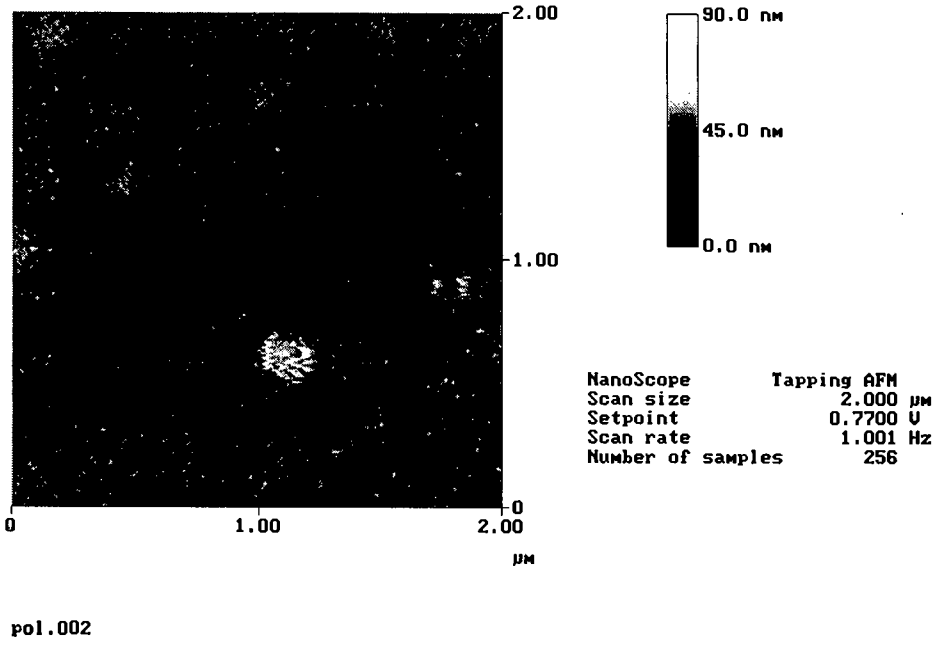


Figure 6.5 Nanoscope IIIa (Digital Instruments) Atomic Force Micrograph[6] of (a) Balzers ITO coated glass, coated with 60nm obliquely evaporated SiO_x.

[6] AFM of samples performed by the Dept. APEME, University of Dundee, Scotland.



(b) Polished in-house sputtered ITO with 60nm obliquely evaporated SiO. The surface structure of these micrographs are very different indeed. Although there appears to be a periodic anisotropy on the sub-micrometer scale, they are probaly artifacts caused by ringing of the AFM tip [Bodammer, 1999].

The polished ITO sample, on the other hand, which had undergone the same treatment exhibits a very different surface morphology, compare the micrographs in figure 6.5. Further more detailed examination of these surfaces is required to acertain the topological anisotropy of the SiO_x layer.

6.2.6 Contrast ratio measurements and discussion

The in-house ITO coated borosilicate glass wafers were diced into 10mm x 10mm samples and the SiO alignment layer deposited (section 4.5.2). Transmissive test cells were then constructed from these samples and filled with CS-1031 as in appendix C. The polished and unpolished ITO cells were assembled in a random order to eliminate any bias in the results due to increasing operator experience.

The main measure of the quality of LC alignment is the contrast ratio (CR) of a LC cell. The CR is defined as the ratio of the cells "on" state to the transmission in its

"off" state. Obviously light leaking through the LC device in its off state degrades the CR.

$$CR = \frac{T_{ON}}{T_{OFF}} \qquad (15)$$

To measure the device CR a 100Hz +/-10V squarewave was used to drive the LC test cell, between two crossed dichroic sheet polarizers (with an extinction ratio of 10^{-4} in white light). A collimated ~5mm diameter 10mW HeNe laser beam illuminated the cell in transmission mode. The cells were rotated to find their best "off" state prior to measurement. A photodetector, with a built in amplifier (type OSI5K, Centronic) 5kHz, 1.3nW to 4.1μW dynamic range, was used to detect the transmitted light and voltage measurements taken from a HP digitizing oscilloscope.

Contrast ratio measurements of ~20-30 units each of polished and unpolished ITO samples were made, but although the best polished ITO cells generally had slightly higher CR's than the best unpolished ITO samples the spread in values, of all the samples, was far too large to enable us to draw any helpful conclusions. The causes of this large spread in CR values was thought to be due to inconsistencies in the cell manufacturing and filling process. If there were any differences in the performance characteristics, *i.e.,* CR, of the cells, they were very subtle and were masked by the variables of the cell manufacture /filling processes.

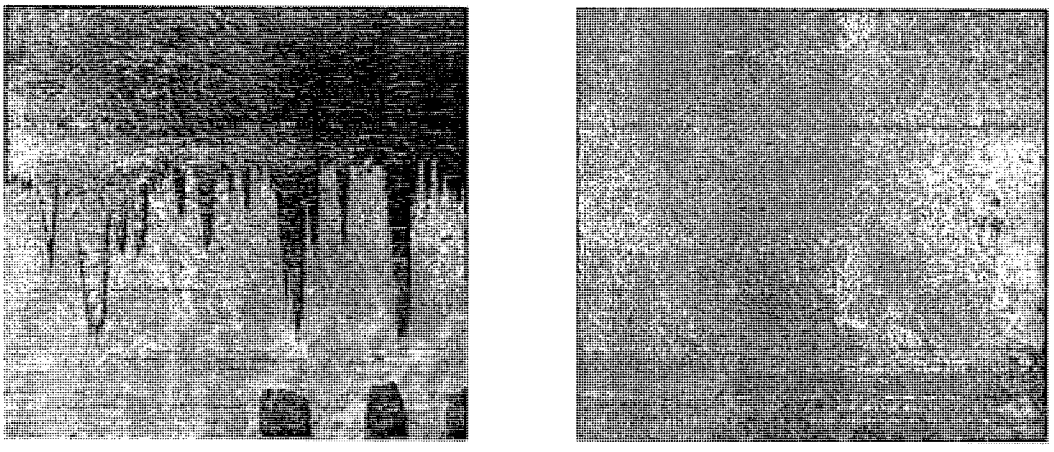
There were many factors which could have lead to the irreproducibility of the results. These included;

- SiO alignment layer deposition (*i.e.,* rate, angle, depth *etc.*). In our case reasonably repeatable.
- Cell construction (*i.e.,* non-flat cells). Operator dependent, but generally improves with experience.
- Cell filling (*i.e.,* temperature uniformity, cooling rate, vacuum pressure and filling rate). Variations in these parameters are the most likely cause of the large spread in results.

Observations of cells fabricated

As just stated, there was a huge variation in the CR of the FLC cells, from <10:1 upto 180:1, for both the polished and unpolished ITO cells[7]. Common characteristics of both types of cell were;

- The thickness uniformity of the cell gap was good and appeared to remain uniform when filled with FLC (one white light interference fringe).
- The same type of FLC alignment defect (chevron[8]) was present, to a greater or lesser extent, in both polished and unpolished ITO cells.



(a) *(b)*

Figure 6.6 The most common observation, in both cells types, were (a) domains and (b) zig-zags, which result from chevron defects.

6.2.7 CMP ITO summary

To summarize, we have demonstrated the possibility of using a standard planarization process (CMP) to reduce the small or microscopic scale surface roughness of ITO coated glass plates by about 40%, by removing the larger 20nm ITO grains. It is apparent that ITO is fairly porous, so it is not likely that we can improve any further

[7] Further experience of assembling and filling cells resulted in cells with CR's of ~300:1.

[8] Chevron defects are the most common defects found in SSFLC devices. They are caused by a shrinking of the smectic layers on cooling from the SmA to the SmC* phase [MacLennan, 1990].

can improve any further on the surface topology with this technique. As with other types of material, ITO CMP using SiO_2 slurry, not surprisingly, still suffers from slurry contamination.

It remains to be seen whether the "improved" surface topology of the polished ITO samples will promote a more homogenous FLC texture. The limited AFM investigations performed, on the Medium Angle Deposited (MAD) evaporated SiO_x layers, on polished and unpolished ITO show very different surface topologies onto which the LC must align.

Future investigations should include a more detailed examination of the surfaces with the AFM, which is to come into commission shortly, to determine roughness on various scales. When a more controllable and repeatable LC cell filling process becomes available it will be informative to repeat the CR measuring experiments on a larger number of both polished and unpolished ITO LC cells to obtain more useful statistical results.

As I mentioned earlier, there are authors who argue that the role of the topology of the SiO_x aligning layer may not be as great as previously thought [Bodammer, 1997] and that the role of the past history of the bounding surfaces is far more significant. It is the authors opinion that any effect that the "smooth" pre-SiO_x alignment layer deposition substrate may have on the FLC alignment is very subtle, and that other factors have a much greater effect. LC alignment and in particular FLC alignment remains an intriging problem which still is not completely understood at the molecular level.

6.3 ITO/SiO_x antireflectance coatings

Anti-reflectance (AR) coatings are deposited on the outer surface of the coverglass to improve the light throughput efficiency[1] of the SLM's. At present, a $\lambda/4$ thickness of MgF_2 is deposited on the top surface of the coverglass to reduce the reflected light intensity, from 4±0.25% to ~1±0.25% (at a wavelength, λ). Another reason for using these AR coatings is to reduce the interference of long-coherence-length light[2] reflected from the SLM coverglass and the bottom surface of the polarizing beamsplitter [Sanford, 1998] in a reflective mode device. Dielectric quarter-wave stacks on the front surface have also been used to reduce the reflectance to close to 0% over a broad-band of wavelengths, but they are difficult to fabricate and require lengthy in-house evaporation cycles.

Unfortunately, none of the AR coatings mentioned above addressed the problem of reflections from the bottom surface of the coverglass [Vass, 1998]. We know, empirically, that the refractive index of ITO section 6.3.1 (~2.00) is very different to that of glass (1.50) and this difference will produce a significant (~2%) reflection of the incident light intensity at that interface, equation 16. It was therefore desirable to determine the ITO, and possibly subsequent film, thicknesses which would minimize these reflections. The coverglass, currently used by the A. O. Group and supplied by Merck Display Technologies, was only available with certain specific ITO thicknesses, see appendix B.

The reflectivity, R, at an interface is given by,

[1] In the absence of absorption or scattering, the physical principle of conservation of energy indicates that all "lost" reflected intensity will appear as enhanced intensity in the transmitted beam [Melles, 1995].

[2] An ideal single wavelength laser source has the property that its light is temporally coherent, which means that there is a definite phase relationship between the fields at any one point after a time delay. In practice, however, real lasers maintain this phase relationship for only a finite time, called the coherence time, or when multiplied by the speed of light for a finite distance called the coherence length of the laser [Corle, 1996].

$$R = \rho^2 = \left[\frac{n_o - n_1}{n_o + n_1}\right]^2 \qquad (16)$$

Where ρ is the reflectance, n_o is the refractive index of the first medium and n_1 is the refractive index of the second medium in the interface. The optical path through the second medium must be as below for destructive interference, equation 17.

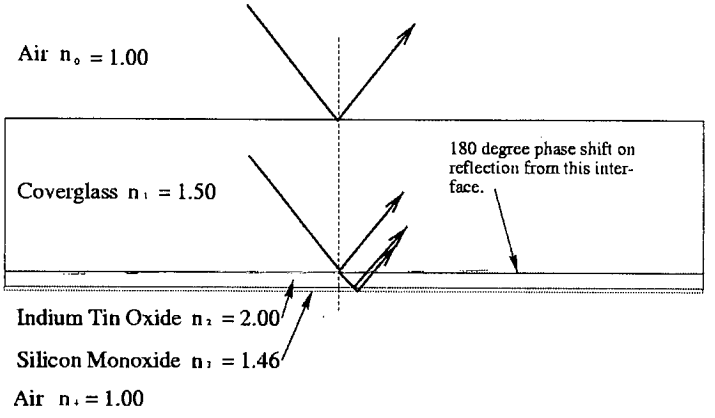


Figure 6.7 Reflections from the interfaces may combine to produce constructive or destructive interference.

$$nd = \frac{\lambda}{4} \qquad \text{if} \qquad n_o > n_1 \qquad (17)$$

or

$$nd = \frac{\lambda}{2} \qquad \text{if} \qquad n_o < n_1$$

6.3.1 ITO deposition characterization

The first stage of our investigations was to determine the ITO deposition rate. The ITO was deposited by DC sputter deposition in an Edwards sputterer as detailed in table 6.2. To allow a range of measurements to be taken on the ITO films, the depositions were carried out on cleaned glass microscope slides. A small section of the slides was masked prior to deposition to facilitate measurement of the film thickness with a SLOAN Dektak 8000 surfaceprofileometer, figure 6.8(a). The resulting deposition rate, under the stated conditions, was calculated to be approximately 71.6 Å/min. The ITO was then annealed to improve its transmittance and reduce its resistivity, figures 6.2(b) & 6.8. The refractive indices of the ITO and

SiO_x layers to be used were measured with an Applied Materials Ellipsometer II. Where the refractive indices of the in-house deposited ITO and SiO_x, n_{ITO} and n_{SiO} were measured to be 2.00±0.05 and 1.46±0.05, respectively. The SiO_x was deposited as described in appendix B.

Edwards sputterer	
Target material	In_2O_3:Sn (ITO)
Target-substrate separation	105mm
DC bias	380Vdc
Plamsa current	100mA
Ar partial pressure	10^{-3} torr

Table 6.2 Edwards sputterer setttings.

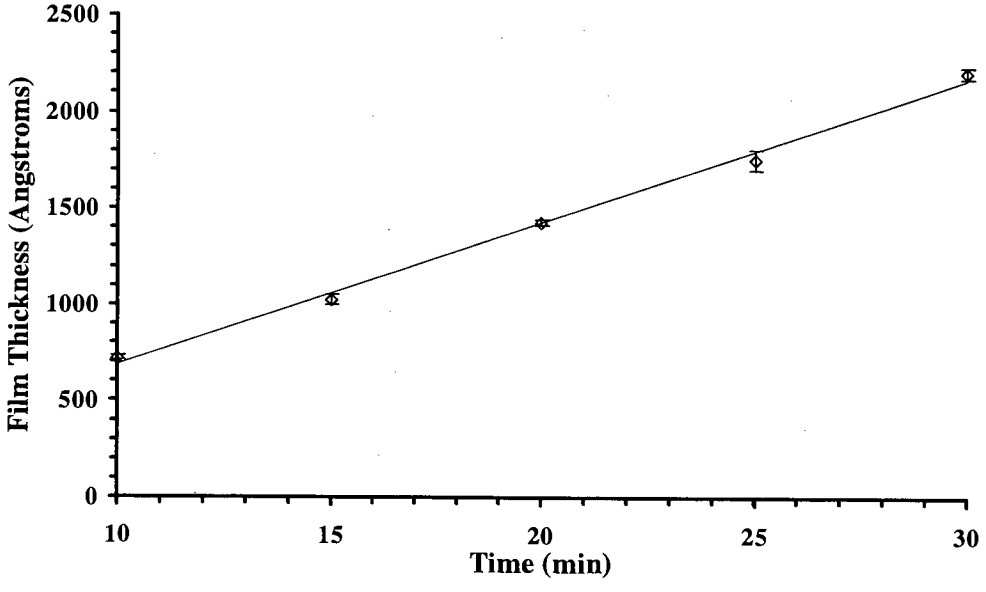
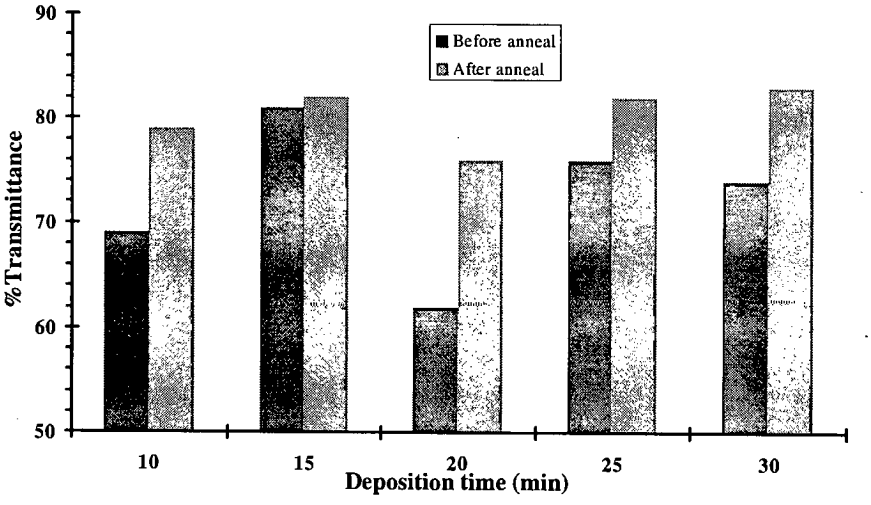


Figure 6.8 (a) Deposition rate of the dc sputtered ITO @105mm was ~ 7.16nm/min.



(b) The in-house sputtered ITO layer transmittance is improved by annealing at 250°C (in air) for 20 minutes.

Although the deposition rate of the in-house sputtered ITO was found to be very consistent, given the same operating conditions, there appeared to be a large and random variation in the films optical absorption from run to run. Following annealing, however, the absorption of each sample was reduced to a level which was essentially independent of film thickness, over the range examined.

6.3.2 Reflectance measurements

Using equations 16 and 17 and the refractive indices measured, we calculated the optimum ITO thickness which produced a minimum reflection at a wavelength λ. The SiO_x thickness was kept constant at a value commonly used in the fabrication of LC cells. The glass slides, one with no coatings, one with 70nm of ITO and 30nm of SiO_x and the third with the ITO thickness set for minimum reflection at λ=633nm and 30nm of SiO_x, were all examined for transmission and reflection with a Lambda 9 spectrophotometer, figures 6.8(b) and 6.9(a)-(c).

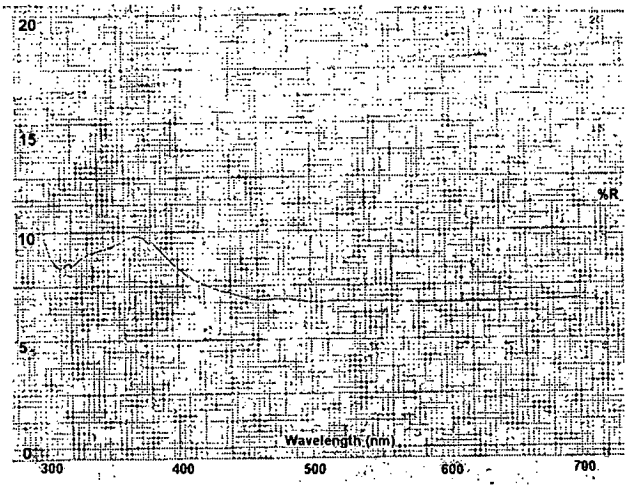
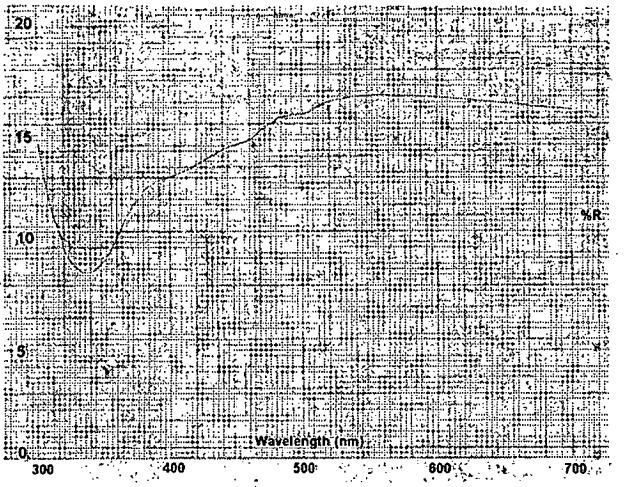
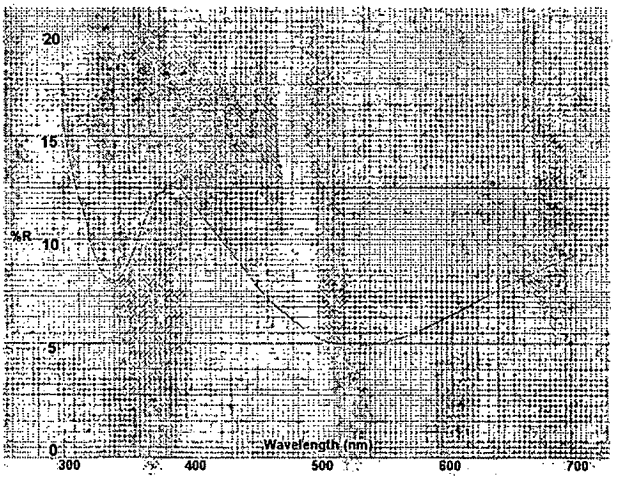


Figure 6.9 (a) Reflectance of a glass substrate with no additional coatings.



(b) Previously used ITO and SiO_x thicknesses of 700Å 300Å respectively had a broad, high reflectivity region in the green and red.



(c) "Optimized" 1580Å ITO and 300Å SiO_x exhibited a minimum in the green.

From these traces we saw that by ensuring that the ITO thickness was approximately equal to a quarter of the incident light wavelength, the reflection from the inner surface could be reduced from 17±0.25%, of the previous coverglass, to <5%, figures 6.9 and 6.10.

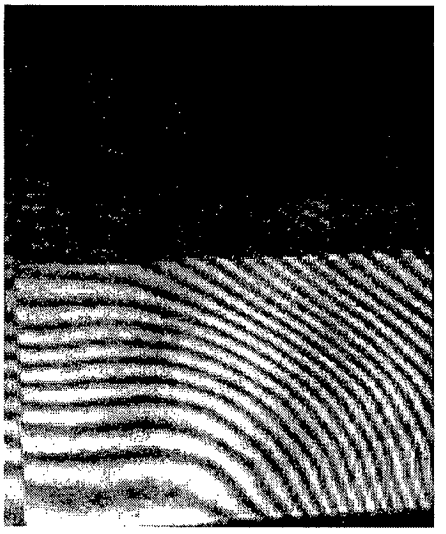


Figure 6.10 150nm (top) and 75nm (bottom) of ITO sandwiched between a glass microscope slide and 30nm SiO_x.

Two sets of test cell were then constructed. The first set consisted of two glass coverplates, one of which was coated with 75nm of ITO. The second set of test cells was the same as the first except that the ITO film thickness was 150nm. The test cells were then visually inspected. The reflected light from the first set of cells (unfilled and filled with NLC, E7) appeared white, while the second set of cells exhibited a yellow-orange tint. These colours were in agreement with the earlier spectrophotometer measurements.

The next stage in our investigations was to examine the SiO_x/LC interface to observe the effect of the SiO_x layer thickness on the reflectivity of the surfaces. Further calculations and experiments revealed that a reduction in reflectance could be made through careful selection of the SiO_x film thickness, figure 6.11.
Using the values of refractive index for two common NLC mixtures, E7 and 5CB, A1, we were able to calculate the SiO_x-LC interface reflectance, table 6.3. Assuming

that the plane of polarization of the incident light was parallel to the extraordinary and ordinary axes of the LC respectively.

	E7	5CB
$n_{LC\,e}$	1.6339	1.62
$n_{LC\,o}$	1.4093	1.44
R_e	0.32%	0.27%
R_o	0.03%	0.005%

Table 6.3 Calculated reflectivity at the SiO_x-LC interface, using the refractive index values given in A.3.

As a proof of principle, a cell was constructed with a coverglass coated with two different thicknesses of SiO_x, figure 6.11.

Figure 6.11 Although this 6μm E7 filled cell was not optimized for λ=632nm (the wavelength of the illuminating light), the interferogram clearly shows that the reflectivity of the top half is lower than that of the bottom half.

The components making up the cell were prepared by masking one half of the glass and coating them 15nm of SiO_x. The mask was then removed and the deposition repeated, leaving a film which was 15nm thick on one half and the standard 30nm thickness on the other half of the substrate. The cells were then filled with NLC and

were inspected using a Fizeau interferometer (λ=633nm), to observe the effect of the LC on the device reflectivity. It could be seen, from the Fizeau interferogram, figure 6.11, that the overall reflectivity of the sample could be altered quite noticeably by doubling the SiO_x layer thickness.

6.3.3 ITO AR coating summary

We have demonstrated the possibility of increasing the light throughput efficiency of a LC device by reducing the reflected light intensity through the selection of suitable ITO/SiO_x thicknesses. Calculating the reflectance of the light incident onto each interface we see that the reflectivity at the SiO_x/LC interface, although noticeable, is relatively small compared to that of the glass-ITO interface (due to the refractive indices of the SiO_x and LC being similar). In these studies we have only investigated the reflected light intensities fom the various interfaces. A more detailed examination, which was beyond the scope of this study, should be performed to take into account the relative phases of the reflected light. This may possibly be performed using a Computer Aided Design (CAD) package. ITO coated glass, which is available commercially is currently only available to specific ITO layer thicknesses. It is apparent, from the experimental results, and from the poor quality observed of the in-house sputtered ITO, that a company who can coat individual optical flats/coverglass must be found to enable us to obtain the best possible optical performance from our LCoS SLM's. Since performing these investigations, described above, IBM have reported their use of 1/2λ thick ITO films to reduce the unwanted reflections from the inner-surface of the coverglass [Stanford, 1998].

Chapter 7.

Conclusions and Future Work.

We have investigated various methods of improving the optical performance of LCoS SLM's, each of which are discussed individualy below. At the end of each section, I will discuss the implications of my work on future research and make recommendations for future work.

7.1 Mirror improvements

Mirror quality and FLC alignment are major factors in determining the overall efficiency of FLC modulators. The idea of forming inlaid aluminum mirrors by CMP had been around for some time. Early in-house metal polishing attempts were performed with a Logitech PS2000 system but with poor results, such as dishing of the mirrors ~100nm and errosion (0.12μm) of the silicon dioxide between the mirrors in the array. In my studies the initial motivation for developing a thin mirror process was due to the limitations of patterning spacers between the mirrors in the high aspect ratio (1:1) gaps. Since our first experiments we have discovered that via polishing and thin mirrors produced by evaporation of aluminum may have more far reaching benefits than just facilitating the fabrication of oxide spacer pillars by the lift-off technique. Toward the end of my studies a Presi 460 system was purchased by the EMF and was used to produce our first thin mirror over polished via plug samples. These samples looked very encouraging with the via dishing of around 10nm (unoptimized). Conventional mirrors had large via "dimples" of ~16-25μm^2. Upon examination of the mirrors on the polished via samples with a phase contrast microscope we found that the via "dimples" were almost undetectable. By eliminating the effects of the via on the top mirror we can effectively increase the pixel fill factor

of a 512x512 pixel SLM by 4-6%. The fill factor becomes even more significant for devices with smaller pixel mirrors such as the future 1280x1024 DRAM device which consists of mirrors of 10μmx10μm. Removing the detrimental effects of the vias in this case would increase the pixel fill factor by 16-25%.

In order to reduce further the dishing of the polished via plugs, we have proposed the use of an aluminum etch back to remove the "field" aluminum leaving the recessed via plugs and a small amount of undersired aluminum around the via area. The small area of aluminum can be polished for a shorter period of time, thus giving reduced via dishing. These ideas are discussed in detail in appendix A.

Evaporated aluminum offers superior optical quality over sputtered or CVD aluminum. Adhesion was an issue which was addressed by ion bombardment of substrate for about 20 minutes before coating. A set of via chain masks with >8000 vias have been designed in order to perform electrical evaluations on the polished aluminum via plug/evaporated mirror structures. Unfortunately, these experiments were obstructed by the lack of an in-house mask making facility during these studies.

To maintain the linear LC flow front over the pixellated backplane I proposed a novel method of filling the inter-pixel gaps of the thin mirrors, to produce the most planar pixellated substrates to date. Examination of the backplanes with a surface profiler showed only noise from the measuring system. The filled trenches were flat to 2.5nm. This was a vast improvement over the conventionally patterned (1-2μm deep trenches) and even experimentally damascened (dishing of ~100nm and errosion of 0.12μm) mirrors. Upon filling devices constructed from the backplanes processed in this novel way, with NLC, I have shown that the LC flow front was undisturbed by the pixel array and the shape of the flow front was only affected by the uniformity of the cell gap. From these results we expect a more uniform LC alignment and a more uniform optical response across the modulator.

Since these via polishing experiments were started, via polishing has become a major research project which shows great promise. Work which is currently underway includes characterizing the metal polishing process on different size features selecting

slurries, many of which are not sold commercially and are only available to the University on signature of a non-disclosure agreement, and pads. An optical characterization of the polished samples is to be performed to assess any possible gains in this technique.

7.2 Backplane flattening and device assembly

Three methods of backplane flattening were investigated, which utilzed robust microfabricated oxide spacers. The first method improved the backplane flatness from about 3λ down to about $3/2\lambda$. I found that the second method, which used no backface support, yielded the flattest backplanes, of $\lambda/3$, in my experiments. The third method, which was a combination of the first two methods, produced backplanes with a flatness of $>\lambda/3$, but the best flatnesses reported was $\lambda/8$ and was achieved by M. Begbie [1997] using this method. The reasons for the poor results of the first and third methods in my experiments was found to be due to particulate contamination.

The first and third methods relied on an adhesive layer to bond the silicon die to a supporting substrate. The adhesive was found to "squeeze" out from the sides of the sandwich structure when pressure was applied. It is clear that much work needs to be carried out to test various adhesives and find the best combinations of adhesive and curing cycles to reduce this problem and to provide a bond which is stable over a wide range of temperatures and operating conditions.

Microfabricated spacer layer aligning marks were found to destroy the uniformity of the cell gap of the assembled devices. This issue was resolved by aligning an etch mask pattern globally to facilitate the removal of the spacer layer aligning marks following patterning. It also became apparent that the geometry of the microfabricated spacer layer was important and metal modifications were required to optimize the cell gap uniformity of the device. In future the optimum spacer distribution density must be determined to achieve these aims.

During my experiments the problem of adhesive spreading in the cell gap whilst bonding the coverglass to the silicon die, was addressed and a possible solution found, which appears very promising.
Pyrex 7740 optical flats, which have a coefficient of thermal expansion ($3.24x10^{-6}$ $\mu m/^{o}K$) similar to that of silicon($2.60x10^{-6}\mu m/^{o}K$) , were obtained as a replacement for the relatively high thermal expansion borosilicate ($4.60x10^{-6}\mu m/^{o}K$) coverglass. This should enable the cell to be heated to the isotropic phase of the FLC with much less stress at the adhesive layer.

Although good flatnesses were acheived with the third technique, it is the authors opinion that this method of placing an elastic material, such as epoxy adhesive or a Rodel wafer insert, between the silicon die and a supporting substrate will never be suitable for use with FLC's, in which the FLC requires heating to become isotropic during cell filling. Due to the large coefficient of thermal expansion of adhesives which are typically one-two orders of magnitude greater than silicon.

Early experiments into using robust spacers to protect the delicate pixels mirrors and provide an excellent cell gap spacing did not use any kind of backface support. It was found that, although the warpage of the die was greatly reduced (1-2 white light fringes) a slight pressure on the back of the structure with a finger was enough to further reduce the white light fringing. Upon filling conventional LCoS cells, that is, cells with no backface support, a deformation of the relatively thin silicon backplane was observed. I then proposed that experiments be performed to determine the viability of using the surface tension forces present at the LC-air-bounding plate interfaces in some way as to apply a light pressure to keep the die flat. Subsequently, problems with the existing spacer geometry, designed by M. Begbie, were found and needed to be resolved before any serious investigations could take place. These problems included,

- Spacer layer covered an area of only 10mmx10mm (pixel array) whereas the coverglass was 12mmx12mm in size.

- The spacer pillar distribution density may have been too low.

A research project (PACMAN[1]) which has received a £350K EPSRC grant, has begun to look at the packaging and manufacturing of microdisplays in collaboration with Micropix Ltd., CRL and Admit Design Systems. These investigations came about, in part, due to the work that has been described in this thesis.

C. Miremont [1998] is developing a novel technique to flatten die using surface tension forces of re-flowed BCB between die and supporting substrate. This technique is loosely based on the technique reported by Lee at the University of Colorado, who used re-flowed solder. G. Bodammer [1998] is testing and evaluating a die flattening jig, which is based on the techniques described in chapter 4, and was designed by A.W.S. Ross. Initial results have proved disappointing again due to the problems associated with particulate contamination.

My recommendations for future work are primarily that a cleaner "clean-room" is found for SLM assembly work and that it is, preferably, adjoining the EMF clean rooms. Ideally LCoS fabrication/assembly would be performed with as little human interaction as possible. Experience gained of assembling LCoS cells, with LC layer gaps of <1μm, had emphasised the importance of particulate contamination control in the LC cell fabrication area. The use of clean, air tight containers for transporting wafers and die/cover-glass around/between clean areas should be implemented. Device fabrication, inspection, assembly and LC cell filling should be performed in the clean area. More stringent cleanroom procedures must be enforced to ensure the successful move to <1μm SSFLC cell gaps.

The Centre for Display Research, Hong Kong UST, have a current research program looking at the chip on glass technology. They are testing bonding materials for bonding glass to silicon chips[2]. It may also be advantageous to the Group to make full use of the solder bump technology now on offer by Heriot Watt University.

[1] Packaging and Manufacturability of Miniature Liquid Crystal Displays.
[2] Obtained from web site http://www.microdisplayweb.com/developer/index.html

7.3 ECR oxide spacer characterization

Oxide spacers can now be deposited to a known thickness with excellent thickness uniformity (down from 5-6% to <1% over a 3" diameter wafer) and repeatability (down from σ=27Å/min to 1.68Å/min), using data obtained in my experiments. My results showed, empirically, that the nitrous oxide flow rate followed by the microwave power of the ECR-PECVD reactor during film deposition both had significant effects of the film thickness uniformity. The optimum settings were as follows,

Nitrous oxide flow rate = 35sccm
Microwave power = 300W

No such dependence was found with the silane flow rate. I had also found that, contrary to earlier belief, the most consistent run to run deposition rates occured when wafers were processed with minimal time delay between them. It is important to remember that at least one test run should be performed before each batch of wafers are processed. A suggestion for future work might be to find a way of accurately measuring the deposited film thickness *in situ*. We expect that this technique will be the technique of choice both within the A.O Group and beyond.

7.4 Polished ITO

The surface roughness of ITO has been reduced by about 40% over a sub-micron scale using a conventional oxide CMP. The post-CMP slurry residue, which remained on the ITO surface, was found to be removed effectively, with no obvious degradation of the ITO film, by a short immersion (1-2 seconds) in dillute HF (HF/DI water 1:9).

Preliminary results indicated that the subsequent oblique SiO_x LC aligning layer deposition morphology was very different on the polished ITO surface.

Unfortunately, due to the irreproducibility of the FLC cell filling process I was unable to observe any possible effects of the polished ITO on the FLC alignment.

One of the biggest problems in FLC cell filling is that of maintaining a uniform temperature, not only across the bounding plates of the cell, but through the FLC layer itself. In addition to this the FLC cell filling rate must be optimized and a constant (0.1 degree Centigrade per minute [Zheng, 1998]) cooling rate over the plates is required after filling. It is important, therefore that a suitable method of cell/FLC heating is found. Also a more detailed AFM examination of the SiO_x on ITO is required.

7.5 Anti-reflectance coatings

The effect of the ITO/SiO_x film on the reflectivity of the glass-ITO-SiO_x-LC interfaces has been investigated. It was found that the commercial ITO coated glass used by the A.O. Group gave rise to a relatively large percentage of reflected, ~17%. This figure was reduced to about 6% by optimizing the ITO thickness (150nm). The effect of the SiO_x layer, on the interface reflectivity, was found to be much less significant, but still noticeable. In order to minimize the reflections from the inner interfaces, the ITO layer must be set to a value of ~1500-1600 Angstroms (green). This thickness of ITO was not available from our current supplier, so a supplier must be found who can coat individual 3mm thick polished glass flats with an acceptable quality ITO to the specified thickness. The important ITO film parameters to be considered are light absorption, sheet resistance and film surface roughness. The optimum thickness of the SiO_x layer, for a particular wavelength, can then be found experimentally.

7.6 Final summary

At the start of my studies, FLCoS SLM's were being fabricated and constructed using standard microfabrication and LCD/FPD techniques. As such, these early SLM's were characterized by a poor optical performance.

It was clear that custom microfabrication and construction processes had to be developed in order that LCoS devices maintained their standing in the SLM and microdisplay community and that these devices make the transition from a laboratory environment to the consumer market.

This study has sucessfully demonstrated such techniques which significantly enhanced the optical performance and quality of our LCoS devices. These processes will now enable the fabrication and manufacture of high quality SLM's for the much needed coherent and incoherent light systems based research within the A.O. Group.

Feature	Principal parameter	Effect	Importance
Via polishing	Fill factor	Reduced dimple depth from 1-2μm down to ~10nm	Very important in reducing LC defects and increasing the pixel fill factor
Thin mirror and SIFT	LC flow front shape and direction	Drastic improvement in LC flow front shape	Very important in ensuring a homogenous LC alignment texture
Backplane flatness	Bow and cell gap uniformity	Best flatnesses achieved is λ/8	Very important esp. for coherent applications
Spacer layer	Deposition rate and thickness uniformity	Fully characterized. Uniformities of <1% over 3" wafer and repeatability improved to an acceptable level	Extremely important to obtain the correct cell gap thickness, esp. for SSFLC cells
CMP ITO	rms roughness and step height distribution SSFLC cell contrast ratio	reduced by upto 40% removed large 20nm ITO grains Effect on CR swamped by other effects	Smooth substrate should improve the LC alignment. Also removal of large grains may reduce light scattering
AR coating	Intensity	Reduction in reflected light intensity from inner-surface of LC cell by about 11%	Very important for most applications

Table 7.1 Final summary of the improvements achieved through this study.

A.1 CMP optimization

CMP optimization is currently being carried out and electrical tests performed to ensure a continuity of the contacts between the vias and their respective pixel mirror electrodes will be investigated shortly using a set of via chain masks, which I have designed, see A.6. AFM scans of polished vias, have revealed that the dishing is actually on the order of 40nm. Various authors have suggested the use of "dishing support structures" to minimize the dishing of bond pads [Tseng, 1997], [SCI, 1997]. D.W. Calton proposes to investigate further the use of "support structures" which have been included into the via mask design in A.6. The effect of dishing and erosion of the bond pads will be examined, and from the results a dedicated mask will be designed which will consider various structure geometries, and allow the technique to be characterized.

A.2 Post aluminum CMP scrubbing

Following CMP on the Presi 460 system wafers were rinsed in DI water and stored in a petri dish filled with DI water to prevent the wafer from drying. Ultrasonic scrubbing of wafers, held vertically or near to vertical, in heated DI water (60°C) and Neutracon[1] for about 30-60 minutes removed much of the slurry contamination. This can then be followed by scrubbing in a high pressure (3000PSI) mask scubber. A PVA brush wafer scrubber, is to come into commission shortly will also improve the cleaning process.

A.3 Future work on metal polishing and via formation.

From our aluminum CMP experiments we had discovered that it is important that the excess field aluminum is removed prior to polishing. The reason for this is due to the

[1] Neutracon is a derivative of Decon, but unlike Decon it has a near neutral pH and is therefore safe to use with aluminum.

fact that the soft and bi-layer stack polish pads tend to deform to match the contours of the wafer, during polishing, which leads to dishing of the soft aluminum features. The maximum potential fill factor of the 20μm 512x512 SRAM mirrors, assuming a 1.6μm gap (as specified in the "Design rules for post-processing at the EMF") between them, is calculated to be about 85%. As can be seen in figure 3.1, there is still a large dead area of the mirror as a result of the via "dimple". This results in a significant reduction in the mirror fill factor to ~78%. Although polishing significantly reduces the depths of the via dimple, they still remain visible. To reduce this via and bond pad dishing further we (DW. Calton and the author) have jointly proposed the use of an etch back technique to remove the excess field aluminum thereby reducing the polishing (CMP) time required.

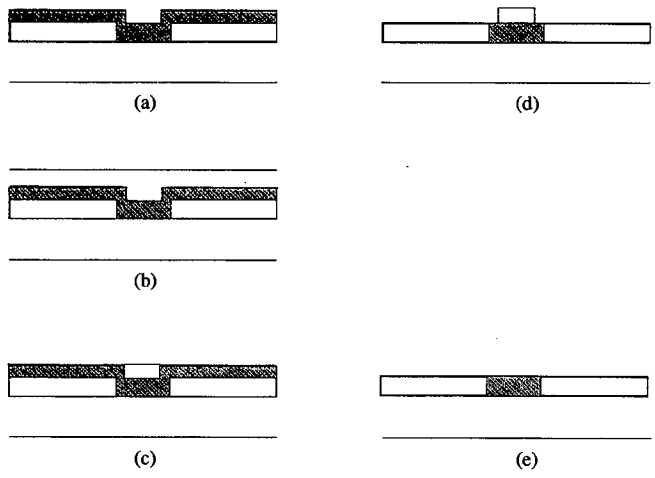


Figure A.1 (a) Aluminum is blanket deposited over pattered oxide as usual. (b) A layer of photoresist is spun onto the wafer surface and allowed to level for about 10 minutes, before soft and hard baking. (c) A oxygen RIE is used to anisotropically etch the photoresist back to the aluminum. (d) A Cl based RIE is then used to anisotropically etch the aluminum back to the oxide substrate, leaving (e) a recessed contact.

A blanket deposition of ECR-PECVD silicon dioxide will be carried out as described in section 3.5, on to dummy four inch wafers. The silicon dioxide layer will then be patterned with the mask used in chapter 5 for the spacer layer characterization experiments, in a plasma etch. These wafers will then be used to determine the conditions which yield the highest level of planarity of the photoresist coating. Stillwagon reported that PR applied using a short spin time (~5 seconds) and

subsequently baked on a hot plate at 100 degrees Centigrade, planarizes the topography better than normally applied HPR206 films [Stillwagon, 1989]. He reports that a leveling period is required to obtain the best results. The next stage will be to determine the PR etch rate in the oxygen plasma asher using the laser end point detector. Following etch back (PR and aluminum), the recessed aluminum vias will be inspected by AFM and SEM, and possibly followed by a short CMP cycle to remove any remaining protruding features.

Another process which is currently being considered, by researchers in the EMF, is the force fill technique [Mizobuchi, 1995], [Stevenson, 1998], which has been demonstrated to fill submicron high aspect ratio vias. Aluminum is sputter deposited at a high rate to seal the via holes, leaving a void. A dedicated high pressure chamber then applies ~60Mpa pressure to the wafers at temperatures ~400 degrees Centigrade to fill the sealed holes. This technique may be applied to our silicon backplanes. Rather than etching extremely large low aspect ratio mirror via contacts, which drastically reduce the pixel fill factor, much smaller vias, which up until now have been difficult, if not impossible, to fill, may be etched and filled using force-filled aluminum. The wafers may then be polished as described earlier and thin mirrors patterned, which again increase the pixel fill factor because they will exhibit minimal undercutting during etching. In addition to the increase in the fill factor from the processes mentioned above, reduced via dishing will be possible, which will in effect add to the pixel fill factor.

A.4 Via plug/thin mirror inspection and testing

A measure of the effectiveness of the thin mirror process is the electrical yield of the polished vias. A good yield, in which all the vias are electrically connected to their respective mirror electrodes, is essential.

A set of via chain masks had been designed[2], A.6, which were to be used to pattern the three levels required, figure A.2, to investigate the via-mirror contact yield and optimize the post-CMP cleaning process. The pads on the test structures were arranged in a geometry to permit probing and resistance data to be automatically aquired. The mask set consisted of two light field masks (M1 and M2) and one dark field mask (via). The probe pads were 120μmx120μm in size and seperated by 120μm in the x and y directions and the total number of vias in each chain is 8192, where taps were taken from vias 2, 4, 8, 16, 32, 64, 128, 256, 512, 1024, 2048, 4096 and 8192. Two of the pads were directly connected in order that the contact resistance of the probes can be measured. This value of probe contact resistance would then be subtracted from the via resistance measurements obtained.
Again AFM investigations would take place to observe the effect of the cleaning cycles on the via plug topography.

A.5 Post Al-CMP cleaning processes to be investigated

Amozawa [1998] had recently reported that slurry residue remained on the aluminum following via CMP, which reduced the yield and increased the resistance of the contact between the vias and the subsequent level of metalization. A post-polish clean using Cl_2/Ar RIE had been used to remove this residue, thus increasing the yield.
Various cleaning regimes had been proposed, below. A thorough investigation of these cleaning procedures (and combinations of procedures), is to be performed to find the optimum results.

- Standard PVA brush wafer scrub in deionized water (set up for 6" wafers).
- RIE (Cl_2 based)
- Wet etch (ISOFORM aluminum etch containing phosphoric acid)
- Photoresist developer (Microposit 351 *etc.* which contains NaOH)
- Ultrasonic scrubbing
- High pressure DI water jet mask scrubber (3000PSI)

[2] This work was delayed due to the necessary pattern generating equipment being unavailable.

Appendix A. Future work on via polishing.

- Argon ion bombardment prior to aluminum evaporation, *in situ.*

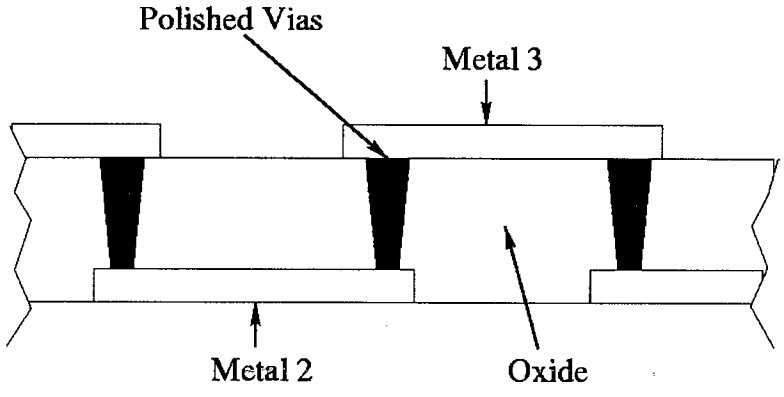
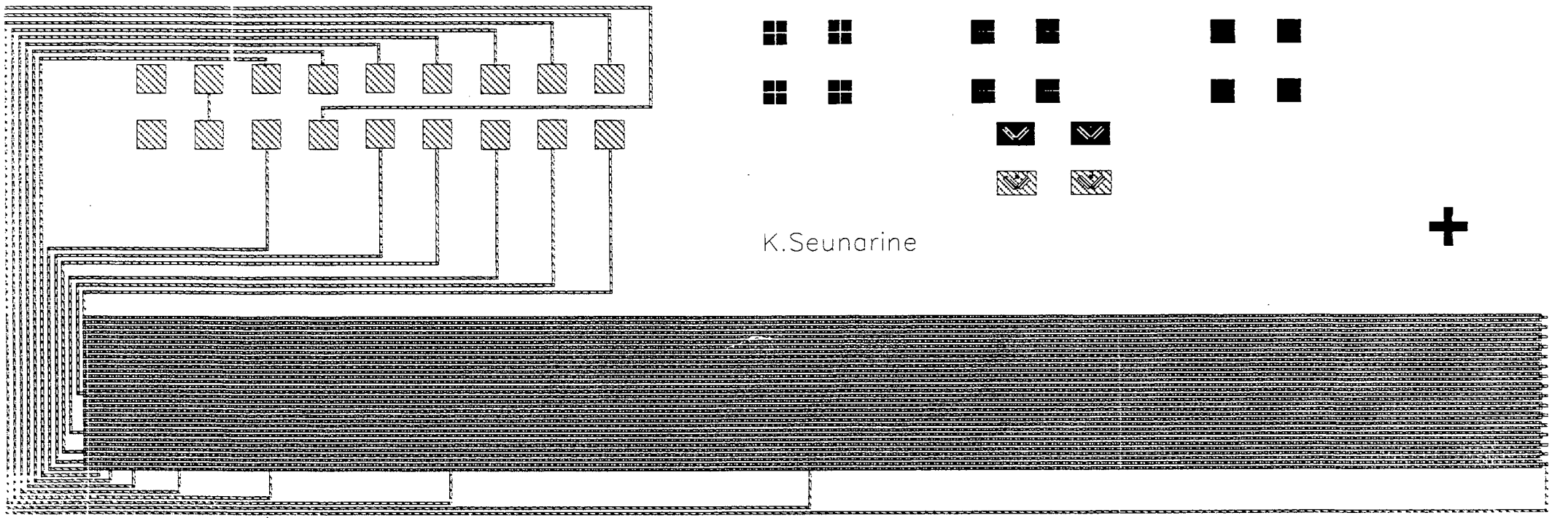


Figure A.2 Via chain to determine electrical yield.

A secondary ion mass spectrometry (SIMS) examination of the recessed plugs will be necessary before cleaning to provide useful information on the type and relative thickness of the post-CMP contamination layer on top of the vias.


K.Seunarine

Appendix B. LC cell materials and construction details.

B.1 Glass properties.

The high quality, commercially available ITO coated glass, which is currently used by the AO Group is supplied by

Merck Display Technology (MDT)
Frankfurter Str.250
64271 Darmstadt, Germany.

The glass types, thicknesses and ITO thicknesses supplied by MDT are listed below.

ITO thickness (nm)	**Ω /sq.**
20	≤ 120
30	80
45	60
80	30
100	20
200	12
240	8

Table B.1 ITO coated glass options

Glass material available is either borosilicate sheet or soda lime float at thicknesses of 0.55, 0.7 or 1.1mm. The type we use is 100nm ITO on 1.1mm thick soda lime glass, order number *255 645 X0*.

For the die flattening experiments I have been using pre-cut 3mm thick Pyrex 7740 glass, polished flat to λ/10. Supplied by

Spanoptic Ltd.
Telford Rd. Eastfield Ind. Est.,
Glenrothes, Fife. KY7 4NX.

Appendix B. LC cell materials and construction details.

The coefficients of thermal expansion of various materials used in the manufacture of SLMs/test cells is shown in table B.2, below.

Material	LCTE, $\Delta L/L\Delta T$ ($^0C^{-1}$)
Silicon	$2.60x10^{-6}$
Soda Lime glass (Merck)	$7.75x10^{-6}$
Borosilicate glass (Merck)	$4.60x10^{-6}$
Corning 7740 borosilicate	$3.25x10^{-6}$
Pilkington CMZ	$3.90x10^{-6}$
Loctite Adhesive 3608	$100x10^{-6}$
Loctite Adhesive 3542 (Low thermal expansion)	$29.0x10^{-6}$

Table B.2 Linear Coefficients of Thermal Expansion, LCTE, @ 300K.

B.2 Adhesives.

Norland Optical Adhesives

Product	**NOA61**	**NOA68**	**NOA81**	**NOA88**
Viscosity (cps)	300	5000	300	200
Modulus (psi)	150,000	20,000	200,000	131,000
Tensile strength (psi)	3000	2500	4000	200
Elongation at failure (%)	38	80	25	41
Shore D hardness	85	65	90	90
Refractive index	1.56	1.54	1.56	1.56
Cure (nm)	354-378	350-380	320-380	315-400
Temperature range (°C)	-80 to 90	-80 to 90	-150 to 125	-

Table B.3 Optical adhesives used for bonding coverplates of LC cells

B.3 Liquid crystal material properties.

Ferroelectric Liquid Crystal

Chisso-1031	
Birefringence, Δn[1,2]	**0.17**
Spontaneous polarization, P_s[1]	**-28.1nC/cm^2**
Tilt angle,θ[1]	**19^0**
Helical pitch[1]	**3μm**
Rotational viscosity[1]	**265mPa.s**
Response time, τ[1,3]	**26μS**

Nematic Liquid Crystal

E7	
Nematic → Isotropic	**61^{0}C**
Crystaline (K) → Nematic	**-10^{0}C**
Birefringence, Δn[4,5]	**0.2246**
$\Delta\varepsilon$[4,6]	**+13.8**
$\varepsilon_{\parallel}$[4]	**19.0**
Viscosity[4]	**39cSt**

Table B.4 Two of the most commonly used liquid crystal mixtures during my studies.

[1] @25^{0}C
[2] @546nm
[3] @10V/μm
[4] @20^{0}C
[5] @589nm
[6] @1kHz

B.4 Substrate cleaning procedure.

The process we use at present, which has been developed by is described below. Cleaning of the backplanes and coverglass are performed in a cleanroom environment. Following each stage in the cleaning cycle the substrates are kept "wet", *i.e.* stored in a solvent or DI water, until they are required. Any substrate left in atmosphere, even in the cleanroom, must be assumed to be contaminated and put through the cleaning process once again.

1. All containers/beakers tweezers *etc.* must be cleaned before use.
2. Cleaning process.
3. The samples are degreased in neutracon(2-5%) /DI water at 60°, for about half an hour.
4. The substrates are then rinsed in DI water before being transferred to a beaker of electronic grade acetone.
5. All subsequent cleaning, where solvents and dangerous chemicals are used, is performed in a fume cabinet.
6. The substrates are then ultrasonically scrubbed for 5 minutes. For obvious reasons, the substrates, and especially the aluminized silicon backplanes, must not be allowed to overlap during the scrubbing process.
7. Following scrubbing in acetone the substrates are individually rinsed in IPA before being placed in another beaker of IPA. The IPA dissolves any acetone residue and also makes drying the samples much easier.
8. The substrates are again scrubbed for 5 minutes before finally being rinsed in IPA and transferred to a container containing IPA for wet storage.
9. Upon use of the substrates they are dried with a filtered ionized nitrogen stream. Care should be taken to prevent the solvent splashing back on to the surface or evaporating.

10. Following cleaning, and drying, the substrates are individually inspected under an ambient light, for any large particles or films of dirt. If such contamination is present the substrates are put back through the cleaning cycle.

B.5 Film evaporation details

Edwards 306 Al evaporation

The aluminum mirrors were deposited in an Edwards E306 evaporation system as detailed below.

1) 1-2cm of aluminum wire is cut and placed inside the W filament.
2) Samples placed, face down, directly above the source (110mm) , ensuring that the Xtal monitor is not obscured.
3) Chamber evacuated to $2x10^{-1}$ torr, by the roughing pump.
4) HT power supply is switched on and the power set to a level to allow the plasma to form.
5) To prevent the residual gas pressure becoming too low and extinguishing the plasma, the gas admittance needle valve is opened to a position of about 6[7].
6) The plasma is maintained for >20mins (see later).
7) Power turned down to 0% and HT switched off.
8) Close needle valve.
9) Allow roughing to evacuate chamber to a pressure lower than 10^{-1} torr.
10) Carefully open the high vacuum valve to allow the diffusion pump to evacuate chamber to at least 10^{-4} torr.
11) Leave samples for 10-20 minutes (not yet determined experimentally) to allow water *etc.* to desorb from wafer surface.
12) Zero the FM3 film thickness monitor (FTM).
13) Switch on LT power supply.

---

7 Note we have used air in our experiments, but argon will be considered in future experiments.

14) Gradually increase power to ~20%, or until aluminum begins to wet the W filament.
15) Increase the power to ~35-40% watching the FTM.
16) Turn power back to 0% and switch off the LT when FTM displays desired thickness.
17) Close valves.
18) Admit air.
19) Remove samples.

Edwards Auto-306 SiO evaporation

The samples were placed into the evaporator using the correct jig for the size of glass and angle of SiO_x flux incidence required (30°). A typical distance between the center of the jig and the top of the source being 190mm. The controller was programmed to automatically pump the chamber down to a high vacuum, by a closed loop refrigerated helium cryopump, when the start button was pressed. When the desired pressure was reached, usually $<10^{-5}$ mbar, run was pressed, ensuring the shutter control was depressed ensuring the automatic mode was selected.

WT	5 seconds
PR	20% : 1 minute
WT	30 seconds
PR	30% : 1 minute
WT	30 seconds
SH	open
WT	5 seconds
TZ	zero
CE	0.15nm/S
TL	30nm
SH	close
PR	0% : 30 seconds

Table B.5 Auto306 SiO deposition sequence.

Key:
WT-wait
PR-Power ramp
SH-Shutter
TZ-Thickness zero
CE-Constant evaporation
TL-Thickness look

B.6 Cell filling.

Nematic LCs have very low viscosities at room temperature, and as such fill cells without heating. However, it is desirable to outgas the LC in the vaccum chamber to eliminate bubbles in cell.

As was mentioned in the text, smectic phases such as FLC have to be heated to above their clearing temperature, before cell filling. The method of cell filling currently employed by the Applied Optics group is as follows [Bodammer, 1996]:

1) FLC is evenly applied along an open edge of the cell (where the opening is perpendicular to the direction of evaporation).
2) The cells are then placed on the hot-plate inside the Edwards vacuum chamber.
3) The chamber is then pumped down to a high vacuum, via a rotary pump and diffusion pump, to a pressure of $<10^{-4}$ mbar.
4) The devices/FLC are left to outgass for approximately 5-6 hours. The chamber is then switched back to the rotary pump (as the liquid nitrogen in the cold trap will completely evaporate over night).
5) The following morning, the chamber is pumped down again to a high vacuum and the hot-plate power supply switched on.
6) When the temperature of the hot plate, measured by a resistive sensor, has reached 120°C, the power supply to the hot plate is switched off and air is admitted into the chamber, at a controlled rate, to allow the cell to fill with LC.

7) After the cells have cooled to room temperature (~3 hours), they are heated again, under high vacuum, to 100 °C.

8) They are again bought back upto atmospheric pressure and allowed to cool.

The disadvantage of this simple technique is that there is little or no thermal contact to the top half of the FLC cell, which means that there is non-uniform heating of the LC.

A slightly different method of filling LC cells, widely used by others [Calton, 1998], is described as follows:

1) The devices are suspended above a bath of the LC material, with the open edge of the cell facing down, in a vacuum chamber.
2) The chamber is pumped down to high vacuum to allow the devices/LC to outgass.
3) The *LC in the bath is heated*[8] and the cells lowered into it.
4) The chamber is now opened up to atmosphere, forcing the FLC to fill the cell.

Disadvantage-requires large volumes of liquid crystal to fill the bath.

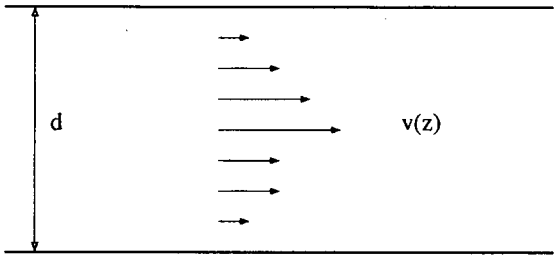
Various temperature cycling magnetic/electric field procedures may be carried out during or after cell filling to improve the FLC alignment [Zheng, 1998].

[8] In the case of smectic phases such as FLC.

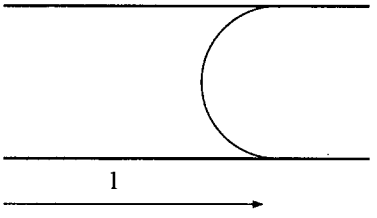
Appendix C. Capillary filling of a cell with LC.

C.1 Liquid crystal flow front velocity

The velocity of the LC in the y-direction depends on z, which is perpendicular to the plates.



(a)



(b)

Figure C.1 (a) LC flow velocity is a function of z, (b) l is the length of LC inside the cell.

Navier-Stokes equation

$$\frac{\partial^2 v}{\partial z^2} = \frac{1}{\eta}\nabla P \qquad (18)$$

Where ∇P is the pressure gradient and η is the translational viscosity coefficient, which is dependent on the orientation of the LC. If the pressure gradient is a constant, the solution to (18) is found to be parabolic

$$v = \frac{-\nabla P}{2\eta}\left(\frac{d^2}{4} - z^2\right)$$

The flow speed at the middle layer (z=0), figure C.1, is

$$V = \frac{-\nabla P d^2}{8\eta}$$

and the average speed is

Appendix C. Capillary filling of a cell with LC.

$$\bar{v} = \frac{\int_{\frac{-d}{2}}^{\frac{d}{2}} v dz}{d} = \frac{-\nabla P d^2}{12\eta} = \frac{2}{3} V$$

$$\nabla P = \frac{-2(\gamma_{sv} - \gamma_{sl})}{ld}$$

Where d is the cell gap thickness, l is the length of LC inside the cell, γ_{sv} and γ_{sl} are the surface tension of the substrate-air and substrate LC interfaces, respectively.

$$\therefore \bar{v} = \left(\frac{\gamma_{sv} - \gamma_{sl}}{6\eta l} \right) d \qquad \text{[Mi, 1998]}$$

Appendix D. Equipment Inventory.

The equipment listed in this section is taken from the EMF web site, and from literature regarding services from other departments within the University.

Equipment in the EMF.

- Linott Series III ion implanter with dose capability of 1e10 to 1e16 atoms/sq cm in energy range 25 to 200 KeV using boron, phosphorus and arsenic impurities. The machine has a run capacity of 54 x 3" wafers or 27 x 4" wafers.

- Balzers BAS450 DC magnetron sputter coater with two 5"x10" targets presently used for coating up to 24 x 3" wafers with Al/1%Si or Al. Ion beam pre-cleaning is posible using an Ion Tec Inc Kaufmann source.

- Three quad stack Tempress Omega L furnaces, with supervisor computer control. System is tooled for 3" wafers to support:

- Dry oxidation (with HCl gettering)
- Wet oxidation (burnt hydrogen with HCl gettering)
- Nitrogen anneals
- Phosphorus deposition (solid source or POC13)
- LPCVD polysilicon
- LPCVD silicon nitride

- Addax Rapid Thermal Processor with dry oxidation capability, handling single 3" wafers.
- Jipelec FAV4 limited reaction processor with oxidation and polysilicon deposition potential.

- Pacific Western PWS 2000 hotplate reactor for PSG deposition at 430 degrees Centrigrade.
- Oxford Plasma Technology ECR deposition of SiO_2 and nitride.

- STS PF 508 barrel reactor for plasma ashing of photoresist from up to 150 wafers/run.
- STS load locked aluminum RIE using $SiCl_2$ and Cl_2 chemistry.

- Plasmatherm PK2440 RIE system using Fluorine chemistry to anisotropically etch silicon dioxide and nitride from 20 x 3" wafers.
- Plasmatherm PK2440 RIE system using Chlorine chemistry to anisotropically etch polysilicon and aluminum/alloys from 20 x 3" wafers.

- 38ft of fume extracted class 100 laminar flow chemical wet stations.

- Photoresist coating, developing and baking are acheived on 3" and 6" wafers on two SVG 8600 track systems, each comprising of:
- Dehydration bake/ vapor prime, coat , hotplate softbake
- Post-exposure bake, spray/puddle develop, hotplate hardbake.

- Mask aligning and exposure are carried out using contact printing or reduction projection printing.
- Contact printer: Cobilt 2020 soft contact (3")
- Projection printer: Optimetrix 8010, g-line, 0.32 NA (3")
- 10X reduction stepper with 1μm resolution over 1cm square field and die by die alignment to +/-0.3μm.

- Projection printer: Optimetrix 8605, g-line, 0.32 NA, (3, 4 and 6")
- 5X reduction stepper with 1μm resolution over 1.4cm square field and die by die alignment of +/-0.3μm.

- Wafers are subject to visual inspection using a variety of metallurgical microscopes.

- Profiling of wafer topology is available using a Sloan Dektak 8000 surface profiler.

- Refractive index and thickness of visually transparent dielectrics such as SiO_2 and Si_4N_3 are measured using an Applied Materials Ellipsometer model AME500. Thick dielectric and polysilicon layers are more readily measured using the Nanoscope Model 010-180 reflectometer.

- Sheet resistance of large processed layers is measured using a Veeco 1000 4-point probe.

- Dicing saw-Kulicke & Soffa Model 602M with ^" wafer chuck.
- Dicing saw-Tempress Model 602M with 4" wafer chuck.
- Eutectic die attach- Dage-Precima Model EDB65 with mechanical scrub wetting
- Wire bond-Kulicke & Soffa Model 472 goold wire ultrasonic ball bonder.

- Parametric testing can be carried out with two HP4062B test systems with 48n switchable pins connected to a TAC automatic wafer prober.

- Logitech PS2000 polisher

- Presi 460 polisher

- Mask scrubber (4")

- PVA brush wafer scrubber (6")

Appendix D. Equipment Inventory.

The SEM Facility operates a Philips XL30CP with Oxford Instruments Isis 300 X-ray analysis system (installed in 1998).

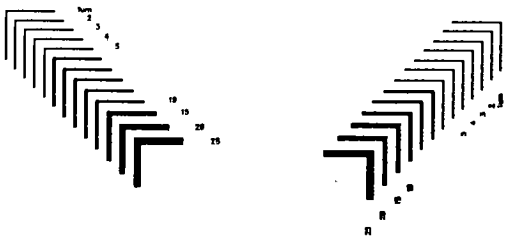
The equipment available at the Science Faculty Electron Microscope Facility includes;

- Cambridge S250 SEM
- Jeol 100s TEM and carbon coating facility

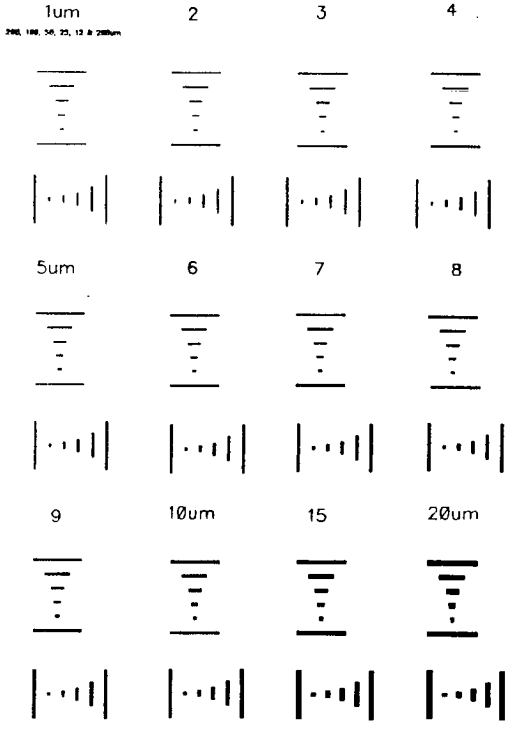
Some of the equipment available from the A.O. Group in the Department of Physics LC Cleanroom.

- Edwards Auto306 silicon monoxide/MgF_2 evaporator with He Cryopump.
- Edwards E306 aluminum evaporator (diffusion pump).
- Ultrasonic baths
- Laminar flow cabinet
- Glue writer
- Polarizing microscope and frame grabber (for inspecting cells)
- Vacuum chamber (diff pump) with hot plate for FLC cell filling
- Edwards sputterer (ITO, Al *etc.*)
- Tallystep surface profiler
- Burleigh Instructional STM.
- AFM with optional STM head (Not yet working in AFM mode).

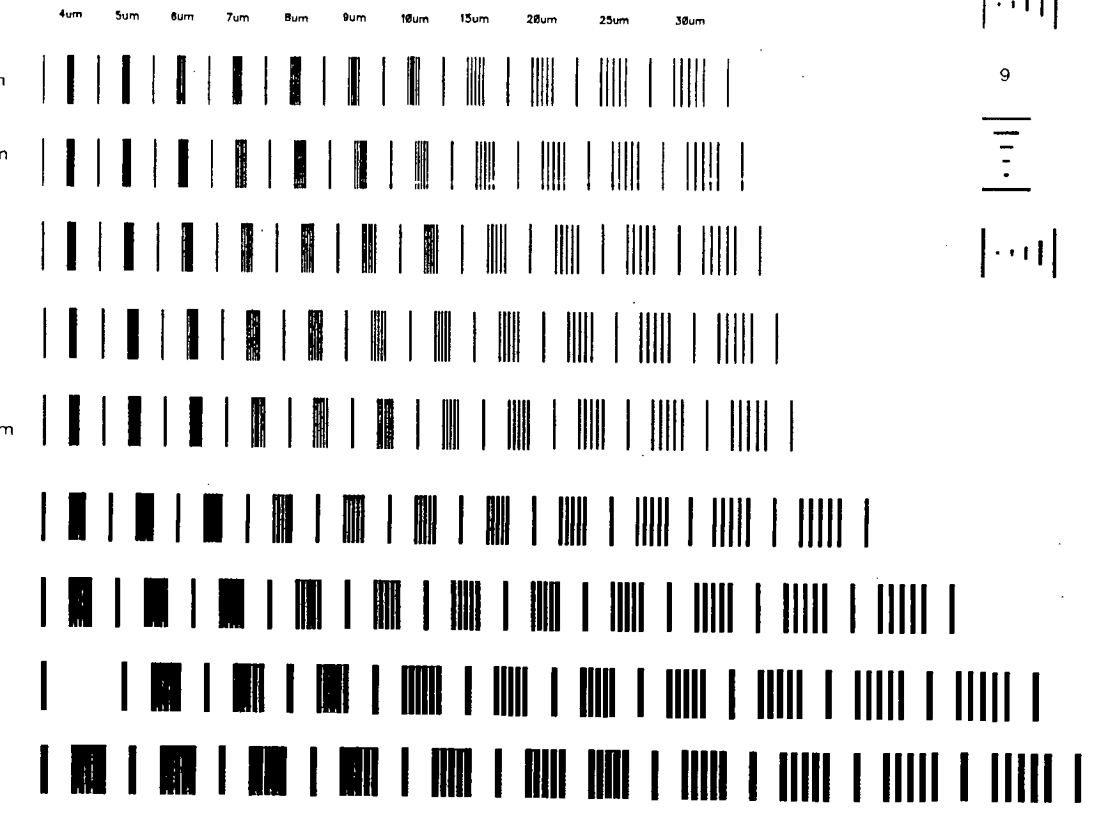
Right Angles & Width

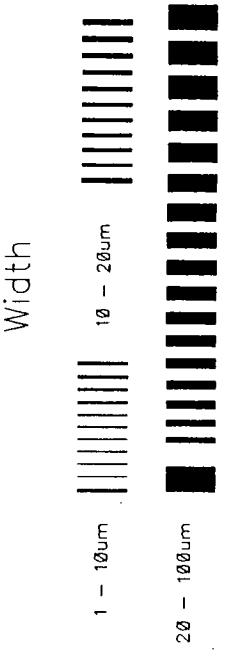


Length, Width & Orientation



Separation & Width





Appendix F. Publications.

Some of the work described in this thesis has been presented at the OSA Spring Topical Meeting, SLMs in Lake Tahoe, Nevada, 1997 and the IEEE/LEOS Summer Topical Meeting in Monterey, California, 1998, and published as

- A. O'Hara, G. Bodammer, M. Begbie, D.G. Vass, I. Rankin, K. Seunarine, D.C. Burns, I. Underwood and J.T.M. Stevenson "*Investigation of Novel Structures on Silicon Backplane SLM's*" In Technical Digest, Optical Society of America, Washington DC (1997), pp.154-6.

- K. Seunarine, I. Underwood "*Technique to Improve Flatness of MEM Backplanes*", Digest of the IEEE/LEOS Summer Topical Meeting Optical MEMS, 1998, pp.79-80.,

respectively.

This and further work was included in

- K. Seunarine, D.W. Calton, I. Underwood, J.T.M. Stevenson, A.M. Gundlach "*Techniques to Improve the Flatness of Reflective Micro-Optical Arrays*" Sensors and Actuators, Physical A. Accepted for publication (1999).

A patent was filed and a post-deadline paper presented at the OSA meeting, SLM's in Snowmass, Colorado on some of the results, described in chapter 3 as

- K. Seunarine, D. W. Calton "*Planarization Technique for Systems over Semiconductors*" Patent application number 9908064.0, filed April 9th, 1999, UK Patent Office.

- K. Seunarine, D.W. Calton, I. Underwood, *"A Novel Thin-Mirror Trench-Fill Technique for the Manufacture of High Optical Quality LCoS Spatial Light Modulators"*, in Spatial Light Modulators and Integrated Optoelectronic Arrays, OSA Technical Digest (Optical Society of America, Washington DC, 1999), pp. PD3-1-PD3-3.

- A.J. Walton, D.G. Vass, I. Underwood, G. Bodammer, D.W. Calton, K. Seunarine, J.T.M. Stevenson, A. M. Gundlach, *"A Review of the History and Technology of Micromachined Miniature Displays Using Foundry Produced Silicon Backplanes"*, Invited paper, SPIE meeting in Queensland, Australia (1999).

- I. Underwood, D. G. Vass, D. W. Calton, K. Seunarine, G. Bodammer, C. Miremont, J. T. M. Stevenson, A. M. Gundlach, *"Recent advances in silicon backplane micromachining for liquid crystal microdisplays"*, Accepted for IEE Colloquium on Microengineering in Optics and Optoelectronics, London, UK, Nov. 1999.

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SPATIAL LIGHT MODULATORS AND INTEGRATED OPTOELECTRONIC ARRAYS

Program Changes

STuA1 Cancelled Presentation – The STuA session will begin at 9:00 AM

Postdeadline Papers

Tuesday, April 13, 1999
5:15 PM – 6:00 PM
Carroll/Sinclair Room

PDP1 **Trigger receivers for optoelectronic-VLSI,** A.V. Krishnamoorthy, P. Chandramani+, T.K. Woodward, K.W. Goossen, B.J. Tseng*, J.A. Walker, W.Y. Jan, J.E. Cunningham, *Bell Labs, Lucent Technologies, Holmdel, NJ *Murray Hill, NJ, +UNC Charlotte, NC.* We describe a "triggered" transimpedance receiver-usable and noisy environments typical of defense OEVLSI chips that combine analog optoelectronic I/O devices with high-density digital logic. Measured data from such a receiver show enhanced immunity to supply variations compared to a conventional transimpedance receiver.

PDP2 **Optically written conical lenses for resonant structures and detector arrays,** Cornelius Diamond[1], Ilkan Cokgor[3], Aaron Birkbeck[2], Sadik Esener[2], *Physics Department, University of California, San Diego[1], Department of Electrical Engineering, University of California, San Diego[2], Call/Recall Inc., Systems Division, San Diego[3].* We demonstate a novel method of making conical lens arrays in photopolymers which offers one-time alignment advantages. The technique may become useful for coupling into detector/modulator arrays as well as fiber couplers.

PDP3 **A novel thin-mirror trench-fill technique for the manufacture of high optical quality LCoS spatial light modulators,** K. Seunarine*, D.W. Calton, I. Underwood, *University of Edinburgh, *Department of Physics and Astronomy, Department of Electronics and Electrical Engineering, UK.* A planarization technique is developed, which enables the total elimination of the capillary pinning of the liquid crystal flow front during LCoS SLM cell filling.

A Novel Thin-Mirror Trench-Fill Technique for the Manufacture of High Optical Quality LCoS Spatial Light Modulators.

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Introduction

The manufacture of high quality liquid crystal over silicon (LCoS) SLM's, has recently begun to show commercial viability. The devices available at the present are relatively expensive and produced in low volumes. Improving the device quality to a sufficient extent that they may be used in coherent applications, (*e.g.*, optical correlation and holographic routing) and to allow mass production of high quality micro-displays is proving a difficult task. Several issues need to be resolved, the main problems being, backplane flatness, cell gap (liquid crystal layer thickness) uniformity and liquid crystal (LC) alignment. We have previously reported on techniques to flatten the backplanes of such devices using Chemical Mechanical Polishing and a novel die flattening technique [1]. The LC alignment issue, which is highly dependent on the LC cell filling conditions [2] will be discussed in this paper.

Existing manufacturing techniques leave the mirrors proud of the surface by as much as 1.5μm, figure 1. This mirror step height causes the LC to flow with a non-linear flow front during cell filling, which leads to a poor LC alignment. A method is needed of producing a planar surface with no inter-mirror trenches. Damascene polishing [3] of the aluminum mirrors has been reported, but problems remained including scratching and dishing of the mirrors, by as much as 30nm over a 20μm square mirror. In addition to the dishing, array thinning, on the order of 400nm over the 10mm array, was introduced. This was caused by erosion of the inter-mirror dielectric "walls" due to the different pattern densities between the array and the surrounding field region.

While mirrors formed using the damascene process greatly reduced the LC flow front disturbance [4], dishing and array thinning were seen to cause a lensing effect and a variation in LC layer thickness (optical path length), respectively. This resulted in a loss of contrast and spurious phase effects which degraded the optical performance of the SLM.

In order to overcome these detrimental effects a novel technique was developed in which the trenches between the thin mirror[1] [5] electrodes were filled with silicon oxide, yielding by far the most planar pixellated backplanes produced to date.

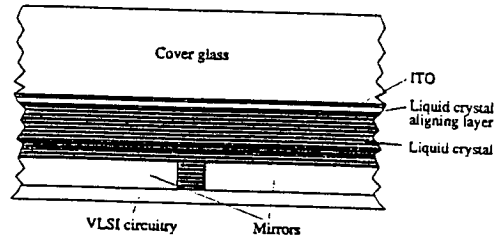


Figure 1. Cross sectional illustration of a conventionally processed (planarized) LCoS backplane. Note the trench between the mirrors.

[1] We have sucessfully fabricated thin mirrors using an intermediate metal CMP process. The results of which will be presented at a later date.

Experimental

The photoresist used to pattern the thin evaporated aluminum mirrors is used as a sacrificial mask for a modified lift-off process. A thin layer of evaporated silicon oxide is then used to fill the inter-mirror trenches. Following the oxide deposition, the photoresist and unwanted silicon oxide overburden is removed by ultrasonic scrubbing.

Results

Atomic force microscopy examinations of the processed backplanes revealed that the filled trenches were flat to 2.5nm, from center to edge.

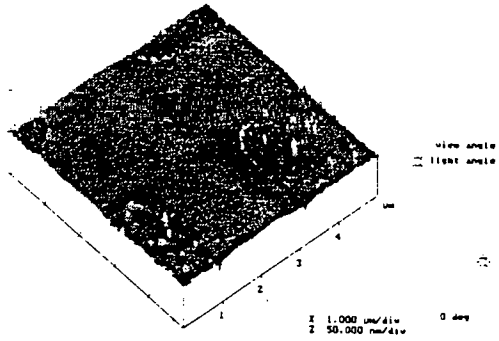


Figure 2. Atomic Force Micrograph of an intersection of four mirrors. The inter-mirror trenches have been filled with SiO_x.

Numerous test cells were constructed from backplanes, with

(1) Conventionally fabricated (1-2μm) mirrors,
(2) Thin (80-100nm) mirrors,
(3) Thin mirrors with filled trenches,

and filled with a nematic liquid crystal (Merck E7) by capillary action.

The LC flow front shape [6], which is extremely important in determining its alignment quality, was observed with a polarizing microscope, between crossed polarizers, figure 3.

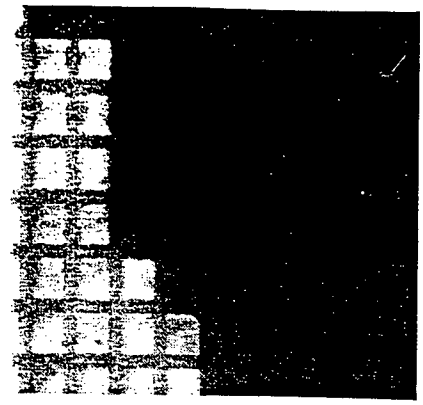
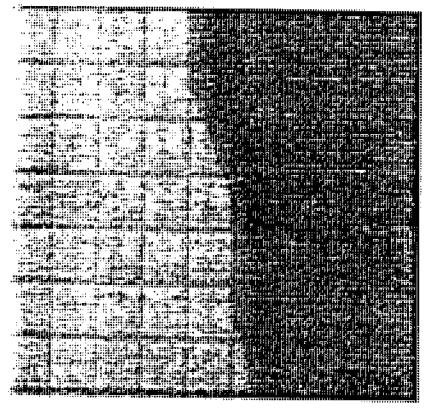
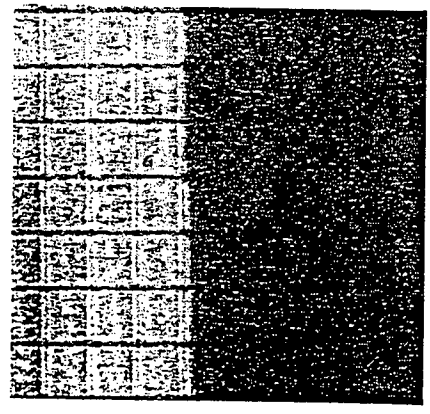


Figure 3. Liquid crystal filling direction from left to right on (a) Conventional "thick" mirrors.



(b) Thin (100nm) mirrors, in which the disruption to the LC flow front is less severe.



(c) Thin mirrors with SiO filled trenches. A total elimination of the LC flow front disruption is achieved.

Capillary pinning is a phenomenon in which the LC, filling the cell, flows along a column of pixel mirrors in a direction perpendicular to the

filling direction, before moving to the next column of pixels.

It was seen that the flow front of the liquid crystal filling the cells was severely perturbed by the capillary pinning [7] effects associated with the rough silicon surface. The effect was greatly reduced on the samples constructed using "thin" 80-100nm thick mirrors and was completely absent, on both a pixel and macroscopic scale, on the samples with SiO_x filled trenches.

Conclusions

The inter-mirror trenches of LCoS SLMs are filled, producing an extremely planar surface on which the liquid crystal flows during cell filling. The process is self-aligned, and no additional masking steps are required.

The liquid crystal flow front, over conventionally fabricated mirrors, during cell filling, was severely disrupted due to capillary pinning at the pixel mirror edges. A thin mirror processes also exhibited this capillary pinning but to a lesser extent. Thin mirrors which were processed using our novel inter-mirror trench filling technique, however, were shown to have no adverse effects of the LC flow front. The straight flow front, which is extremely important in ensuring a uniform LC alignment over large (≥ 10 x 10μm) pixel arrays is maintained.

Acknowledgements

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SENSORS AND ACTUATORS A PHYSICAL

Techniques to improve the flatness of reflective micro-optical arrays

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Abstract

Liquid crystal over silicon is an established technology for reflective spatial light modulators and microdisplays. In this paper, we describe progress in improving two key performance criteria. The first is backplane flatness; we describe recent developments in the use of chemical mechanical polishing to produce optically flat pixel mirrors on top of existing circuit topography; we further describe the use of an assembly technique that reduces chip bow caused by the microfabrication induced stresses in the silicon backplane. The second is liquid crystal layer thickness; we describe the use of a lithographically patterned spacer layer microfabricated on the surface of the silicon backplane to minimize layer thickness variations. Each of the techniques produces improvements in the performance of the final device.

Keywords: LCoS; CMP; ECR; Spacer; SLM assembly

1. Introduction

1.1. Background

A Spatial Light Modulator (SLM) is a device which is used to apply a spatially controlled modulation to an incident wavefront. Over the years many SLM technologies have been reported and many types of modulation applied [1]. Pixellated spatial light modulators based upon the hybrid technology of Liquid Crystal on Silicon (LCoS) have been around for some time (Fig. 1). In recent years the specific combination of fast switching Ferroelectric Liquid Crystal (FLC) over densely packed CMOS silicon circuitry has heralded a substantially increased performance, particularly in terms of space bandwidth product, W, given by

$$W = mnf$$

where m is the number of rows, n is the number of columns, and f is the frame rate of the SLM.

For example, the recently available SLIMDIS device has $n = 1024$, $m = 768$ and $f = 10$ kHz giving a space bandwidth product of 10 Gbit/s. The primary application of LCoS and FLCoS SLMs today is as miniature displays [2]. This is by far the largest potential market, many other markets exist which, while smaller and more specialized, are likely to be of greater added value and thus worth pursuing. These include optical crossbar switches, reconfigurable holograms and optical correlators [3].

1.2. Current situation

Some of the major performance indicators for spatial light modulators (depending upon application) are pixel count, frame rate, space-bandwidth product, throughput efficiency, contrast ratio, modulation depth, phase flatness, uniformity across a SLM and from SLM to SLM, size, weight and cost. For a reflective SLM technology used in non imaging applications, backplane flatness is a key factor at all scales from macro to microscopic. It is generally the case that, if no special care is taken, a silicon backplane will show a degree of non-flatness at all scales due to the following causes:

- **Sub-micron**. Metal granularity causes scattering of incident light. We have previously reported the successful use of unsintered aluminum to minimize this effect [4].

- **Pixel**. Circuit topography also scatters light and causes variations in the director alignment of the liquid crystal layer which show up as sharp variations in contrast in a finished SLM.

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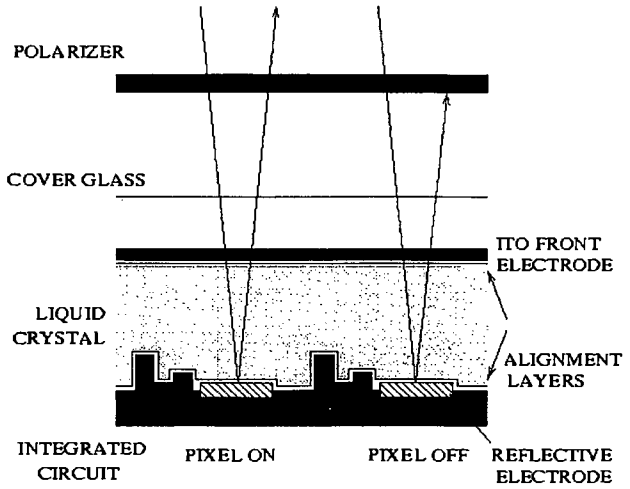


Fig. 1. Illustration of reflective SLM operation.

- **Backplane**. Chip bow causes distortion of a reflected wavefront and large scale variations in FLC thickness and alignment, again resulting in noticeable contrast variations (manifesting as color fringes in a microdisplay) [5].

1.2.1. The issues

Major issues facing the FLCoS SLMs of today, particularly with regard to their use in non-imaging applications, such as those listed in Section 1.1, are those of improving

- the flatness of the silicon backplane at the pixel and array levels

- the thickness uniformity of the FLC layer across a device.

Thickness uniformity is an issue because the FLC acts as a switchable halfwave plate in reflection whose optical response is as shown in Eq. (1).

$$I(\lambda) = I_o(\lambda)\sin^2(4\theta)\sin^2\left(\frac{\pi\Delta n(\lambda)2d}{\lambda}\right) \quad (1)$$

where θ is the cone angle and Δn is the birefringence of the liquid crystal. λ is the wavelength of the incident light I_o.

Clearly for the optimum modulation we require a thickness of $\Delta nd = (2m + 1)\lambda/4$, where m is a positive integer.

1.2.2. The solutions

The solutions we have identified, and on which we report our progress here, involve

- the use of Chemical Mechanical Polishing (CMP) techniques to reduce or remove underlying topography (Section 2)

- the use of microfabrication techniques to implement spacer pillars to set the size of the FLC cell gap (Sections 3.1, 3.2 and 3.3), and

- an assembly technique which sets a uniform cell gap (Section 3.4).

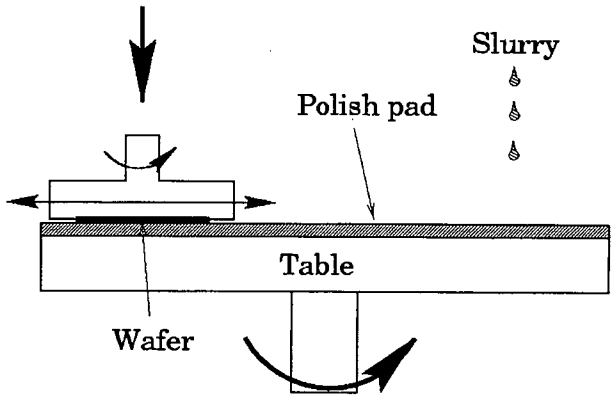


Fig. 2. Simplified CMP tool layout.

2. Backplane planarization

2.1. Chemical mechanical polishing

The requirement of producing optically flat micro-mirrors necessitates the use of some form of planarization to remove the surface topography caused by the underlying circuitry. There are several methods in current use, including; etch back, bias sputtered dielectric, spin on glass or other material and chemical mechanical polishing of dielectric (CMP). Of these methods only [6] CMP offers planarization at both local and global levels [4,7].

In CMP the wafer is placed face down, under pressure, on a polishing pad, both the wafer and pad rotate, slurry is then fed at a controlled rate onto the pad surface. Material removal is by a combination of mechanical and chemical action of the slurry [8] (see Fig. 2). The rate of material removal is related to contact pressure and wafer/pad velocity [9]. The greater the velocity the higher the removal rate, also, the higher the applied pressure the higher

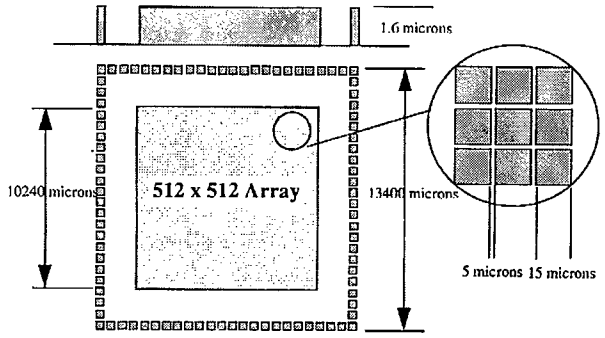


Fig. 3. Schematic of CMP test pattern.

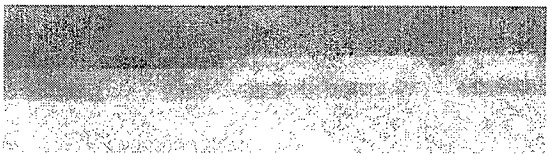
the removal rate. This causes the higher points, which have a greater contact pressure to polish first [10]. Eventually all the high spots are removed, leaving a smooth planar surface.

CMP is a complex process and the quality of the result is dependent on many factors, each of which needs to be optimized. The process variables include pad/wafer velocity, head/back pressure, pad/slurry temperature, slurry flow and pad conditioning. All these parameters have to be optimized with a particular set of consumables, pad, slurry, wafer holders and machine used. As all of the variables are interrelated a 'recipe' which works for one consumable set may not be repeatable for another.

2.2. Issues for CMP of optical arrays

We are investigating the use of CMP to planarize SLMs, which have large arrays of micro-mirrors. The surface topography of a processed wafer is not flat as there are many irregularities caused by the different layers used to build up the underlying circuitry. This has to be removed if high quality, optically flat mirrors, are to be fabricated over the underlying circuitry.

The degree of planarization can be classified into three distinct types: local or feature scale planarization < 20 μm (FSP), die scale planarization < 12 mm (DSP) and global or wafer scale planarization (WSP). In the production of micro-mirrors both FSP and DSP are crucial. FSP is necessary to produce individually flat mirrors while DSP is necessary to give flat die and therefore a uniform cell gap which promotes a high quality LC fill. WSP is the most difficult to achieve, it requires that all die within the wafer have the same oxide thickness, which is necessary for process considerations, such as etching of the vias, and overall yield issues. The process tolerance required for polishing SLMs, is far tighter than for normal, non-optical, electronic device fabrication, where the required planarity set by the depth of focus (DOF) of the photolithography printing system. This can be in the order of 240 nm for $\lambda = 365$ nm systems. In standard CMP the maximum planarization length is in the order of a few 100 μm while SLMs demand that the entire array, which can be larger that 10 mm, needs to be planarized. If the finished device is to be used in a display system it has to be flat, at both pixel and array scale, typically to $\lambda/5$ (120 nm at $\lambda = 633$



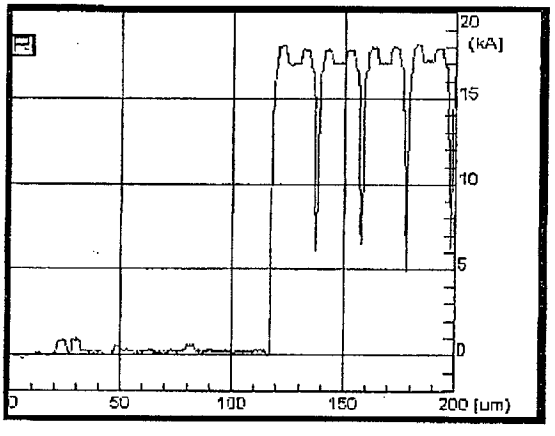


Fig. 4. Oxide on 512×512 array and surface profile.

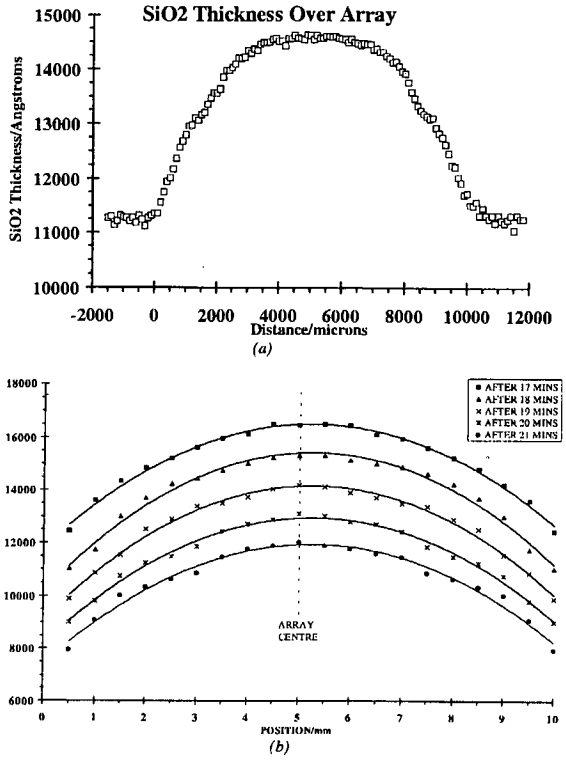


Fig. 5. Polished array with 1.7 μm step height.

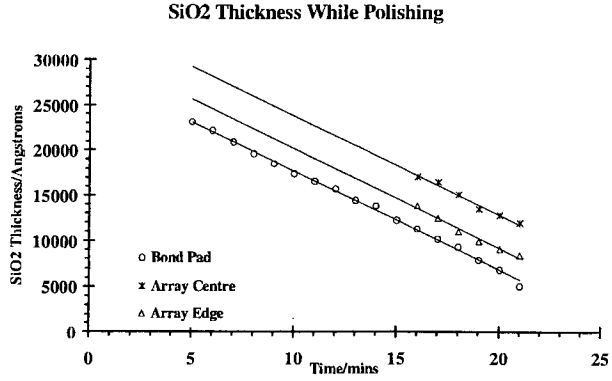


Fig. 6. Variation of SiO_2 thickness with polish time at various locations on die etch/CMP process.

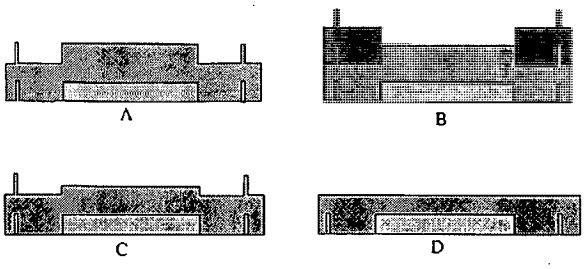


Fig. 7. (a) SiO_2 deposit, (b) mask and etch, (c) after etch showing reduced step height, and (d) after CMP showing no step.

nm). If used for optical computing the requirements are even tighter with $\lambda/10$ (63 nm at $\lambda = 633$ nm) being the minimum flatness required [11].

Other areas of concern are the final surface finish of the oxide and post CMP cleaning. The surface finish must be of sufficient quality, low roughness average (R_a), to allow highly specular aluminum to be deposited. Post CMP cleaning must ensure that no abrasive particles are left behind as they will cause reliability concerns and also degrade the quality of the sputtered aluminum, causing a deterioration in the optical quality of the mirrors.

2.3. Experimental details and results of CMP

The test pattern, see Fig. 3, was patterned onto 1.6 μm of aluminum, sputter coated onto 100 mm wafers. They were then polished using a Presi Model E460 single spindle machine using a Rodel IC1400 stacked pad, and Klebosol 30H50 slurry. The consumable set was the same for all the tests. Two micrometers of Electron Cyclotron Resonance (ECR)-PECVD oxide was then deposited using an Oxford Plasma Technology reactor. ECR oxide is used

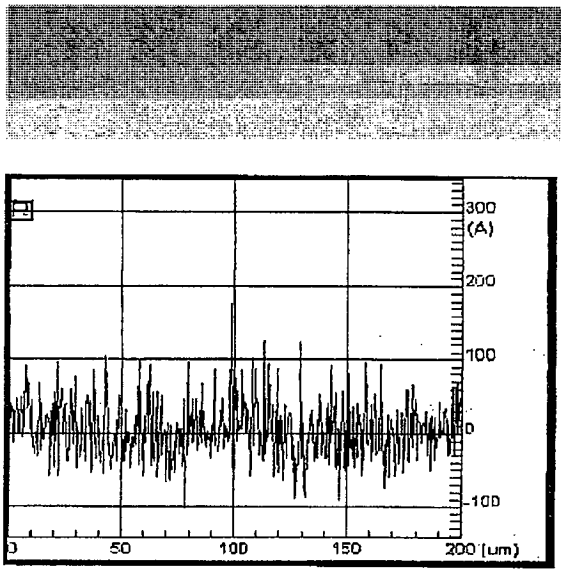


Fig. 9. Image of planarized array and surface profile.

because of it ability to completely fill small gaps between features this is essential because the oxide must contain no voids otherwise they will be exposed, during polishing, leading to defects in the polished surface.

The oxide thickness over the array was measured using a Nanometrics micro-area gauge, the surface profiling was carried out on a Sloan Dektak model 8000. The profile of the first oxide deposition is shown in Fig. 4. It can be seen that this layer follows the underlying circuitry producing a non-planar surface.

Several difficulties arise when polishing large arrays of small features. Firstly, CMP is very sensitive to variations in feature density in that it polishes single, isolated fea-

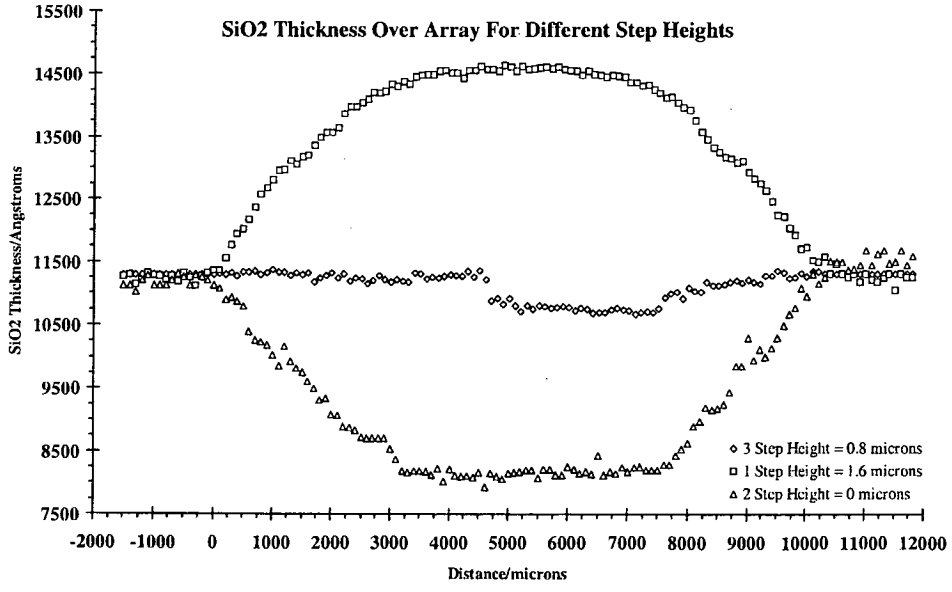


Fig. 8. SiO_2 thickness over the array, following CMP.

Table 1

Machine	Presi Model E460
Head Pressure	0.6 bar
Head Speed	60 rpm
Platen Speed	60 rpm
Back Pressure	0.2 bar
Slurry Flow	75 ml/min
Temperature	10°C
Slurry	Klebasol 30H50
Pad	Rodel IC14000

tures, at a higher rate than groups of features of the same size. Consequently when polishing the mirror array the oxide polishes into a square domed shape, which is thicker in the middle than at the edge. The oxide thickness over the array, which has been polished at 1-min intervals, is shown in Fig. 5a. It can also be seen that once a profile has been established further polishing will only reduce this profile in height, and not alter its shape (Fig. 5b). If the polish rate at the edge of the array is compared with the middle, it can be seen that they are identical (Fig. 6) as is the polish rate for the bond pads. It was seen that the smaller features within the array were removed, to within 80% of their initial height, within the first 4 min of polishing. After 6 min, no structure could be seen on the array surface, but it still exhibited the rounded profile which did not alter even after over 20 min of polishing. This can be attributed to the deformation of the polishing pad [12]. A harder, stiffer pad may help to overcome this problem but would lead to a poor WSP. The pad temperature was controlled at 10°C to increase the stiffness and reduce the amount of pad deflection around the array [13].

One way to overcome the problem of array rounding is to use a pre-CMP etch [14]. This is used to reduce the oxide step height of the array compared to the surrounding field region. It essentially removes the low frequency (large) features, which are the most difficult to remove by CMP, while leaving the smaller features intact. The device

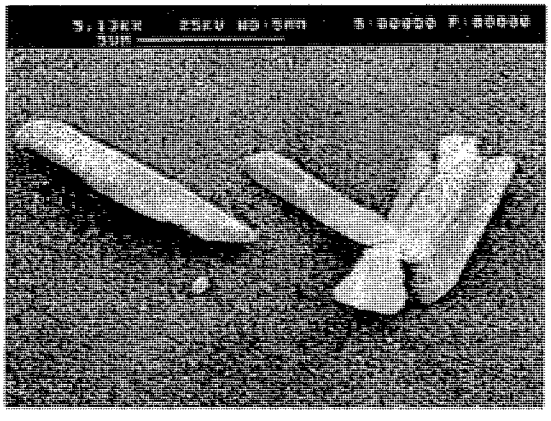


Fig. 10. Conventional silica spacer rods are crushed during cell assembly/die flattening.

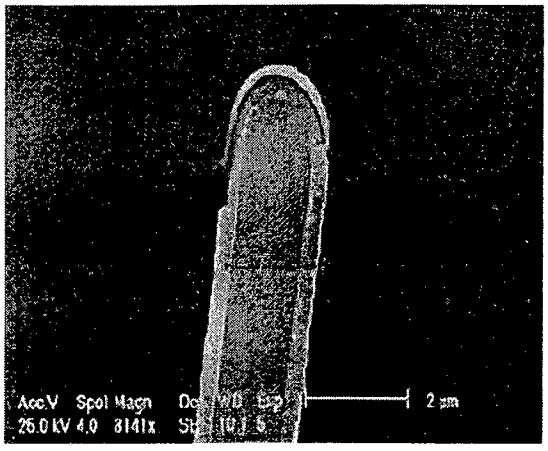


Fig. 11. SEM of an oxide spacer in which lift-off is incomplete.

is first covered with photoresist and then patterned to leave the array exposed. The oxide over the array is then etched using Reactive Ion Etching (RIE) to reduce the step height. The resist is stripped and the wafer then polished (Fig. 7). If the oxide over the array is etched level with the field area, prior to CMP, dishing results. This stems from the fact that the mirror array has a different feature density (~ 56%) compared to the field oxide density (100%) which causes the array to polish faster, creating dishing of the array [15], see trace 2 in Fig. 8.

If the array is etched, pre-CMP, to such a height that the differential polish rate, caused by the different feature density, counteracts the doming effect, caused by pad deformation a flat array profile will result following CMP. On this test pattern, a step height of ~ 0.8 µm is found to produce the best planarity of oxide over the array. The result of polishing an array with this height can be seen in Fig. 8 trace 3. It can be seen that the amount of dishing is minimal. The array oxide has been polished to a uniformity of ~ 75 nm over the 12 mm die, see trace 3 (Fig. 8). The final surface topography can be seen in Fig. 9. The initial step height of 1.7 µm has been reduced to zero with no features present within the array and a surface rough-

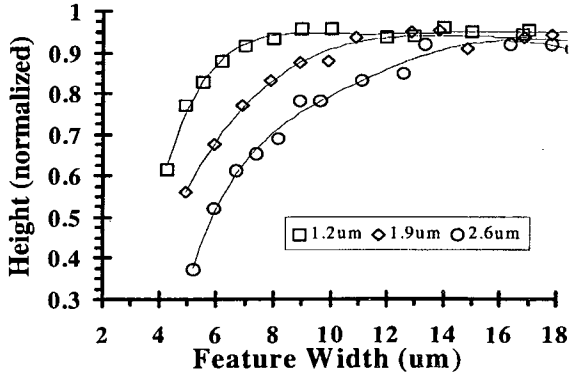


Fig. 12. The spacer height varies quite considerably with photoresist stencil aspect ratios of ≥ 0.15.

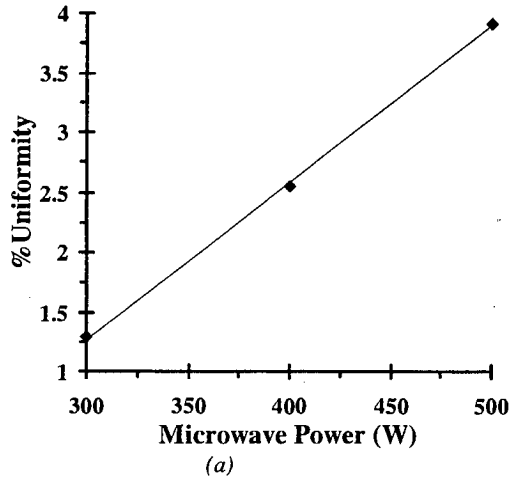
ness of $R_a = 22$ Å. The process variables and consumable set used for the final test can be seen in Table 1.

Table 2

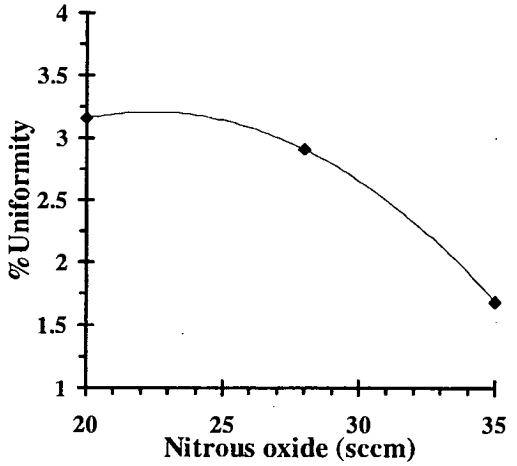
Silane flow rate	125 sccm
Nitrous oxide flow rate	35 sccm
Table height	100 mm
Table wafer temperature	~ 40°C
Chamber pressure	~ 5×10^{-5} Torr
Microwave power	300 W
Magnet currents	130 A and 55 A

3. Backplane flattening and cell spacing

SLMs are currently assembled using traditional silica spacer particles 'borrowed' from the flat panel display fraternity. The problem with these particles, when used in the manufacture of such devices, is that they are (i) randomly distributed across the device, and (ii) easily fractured during pressurized assembly (Fig. 10). To date there have been many other cell gap spacing methods reported including CVD-diamond, dummy structures, positive photoresist and Benzocyclobutene (BCB) [16–21]. The requirements of the spacer material used to set the cell gap, are that it must be robust, inert to liquid crystal, have a strong adherence to the substrate and be compatible with the post-processing procedure.



(a)



(b)

Fig. 13. (a) Effect of microwave power and (b) nitrous oxide flow rate on ECR-PECVD deposition uniformity.

We have developed a process of fabricating robust custom spacer layers on a wafer-scale using conventional microfabrication techniques, which go hand in hand with, and actually benefit from planarization by CMP. The pressurized assembly technique, which relies on these robust spacers, may facilitate the automated assembly of LC/VLSI SLMs, which up to now has been carried out by experienced manual operators [22].

3.1. Spacer layer fabrication

To prevent degradation (hillock formation) of the optical quality of the aluminum pixel mirrors a low deposition temperature ECR oxide is used. A lift-off technique is also required to maintain metal quality which would be attacked (pitted) during an etch process [23].

The wafers are thoroughly cleaned by ultrasonic agitation in de-ionized water/Neutracon @ 60°C and then dried. The adhesion promoting HMDS vapor prime, spin coating and soft bake are all performed on an SVG track system. The photoresist (HPR206 or SPR2) is then soft baked at 110°C for 60 s, and the spacer pattern printed by an Optimetrix 8600 series 5X g-line stepper. The resist overhang profile required for lift-off is accomplished by soaking the resist coated wafer in chlorobenzene for 60 min, at room temperature. Following this the wafer is rinsed in DI water and developed in Microposit 351, again, at room temperature. The wafers are given a final rinse and dry prior to ECR oxide deposition. Due to solvent outgassing in the resist layer the more robust planar/compacted oxide used in CMP of the array, achieved by RF accelerated Argon ion bombardment, is found to be incompatible with the lift-off technique. The RF power and Argon flow rate are therefore both set to zero during deposition. Finally, lift-off is performed by ultrasonic scrubbing in acetone to remove the photoresist and unwanted oxide leaving the patterned spacer layer (Fig. 11).

3.2. Patterning and deposition characterization

To obtain the high tolerances required in the liquid crystal layer thickness and uniformity the spacer layer deposition rate must be known and repeatable. The possible factors which may affect the height of the spacers were

investigated. Test features accounting for width, length, separation, orientation and corner effects of the spacers were designed. Wafers were coated with 1.2 μm, 1.9 μm and 2.6 μm of photoresist. They were then patterned with the test features used to investigate the effect of the variables stated above.

Following oxide deposition and lift-off of the unwanted material, the spacer feature heights and geometries were measured with the Dektak. From these measurements, it is found that only one variable has a significant effect on the spacer feature height; namely the width, and thus the aspect ratio of the patterned photoresist stencil (Fig. 12). The length of a feature only has an effect on its height when it is of a similar magnitude to the width < 10 μm.

3.3. Deposition optimization

In addition to characterizing the patterning process, the ECR-PECVD deposition process is optimized, using a designed experiment method [24], to provide the best possible deposition uniformity over the wafer. It is found that the microwave power and N_2O flow rate have the most significant effects on the deposition uniformity (in that order) (Fig. 13). Deposition uniformities of $\leq 1\%$ over a 75 mm wafer have been achieved with the optimized ECR deposition uniformity parameters (Table 2) compared to commercially available silica spacer particles which may have variations of $\sim 10\%$ [25].

3.4. Device assembly

Various methods have been reported of flattening the severely bowed wafers and die of optical devices [26,27] which all have their merits. Our robust ECR-PECVD spacers have opened up new possibilities for flattening device backplanes, which offers a means of flattening backplanes on a die scale. The cell assembly/die flattening are performed after wafer dicing—so the wafer handling/dicing problems of other techniques are avoided. Also, unlike other methods, no high temperatures or voltages are required during flattening, and the delicate pixel mirrors are protected by the spacer pillars, which also provide an extremely accurate cell gap spacing. The fully fabricated and diced backplanes are assembled under pres-

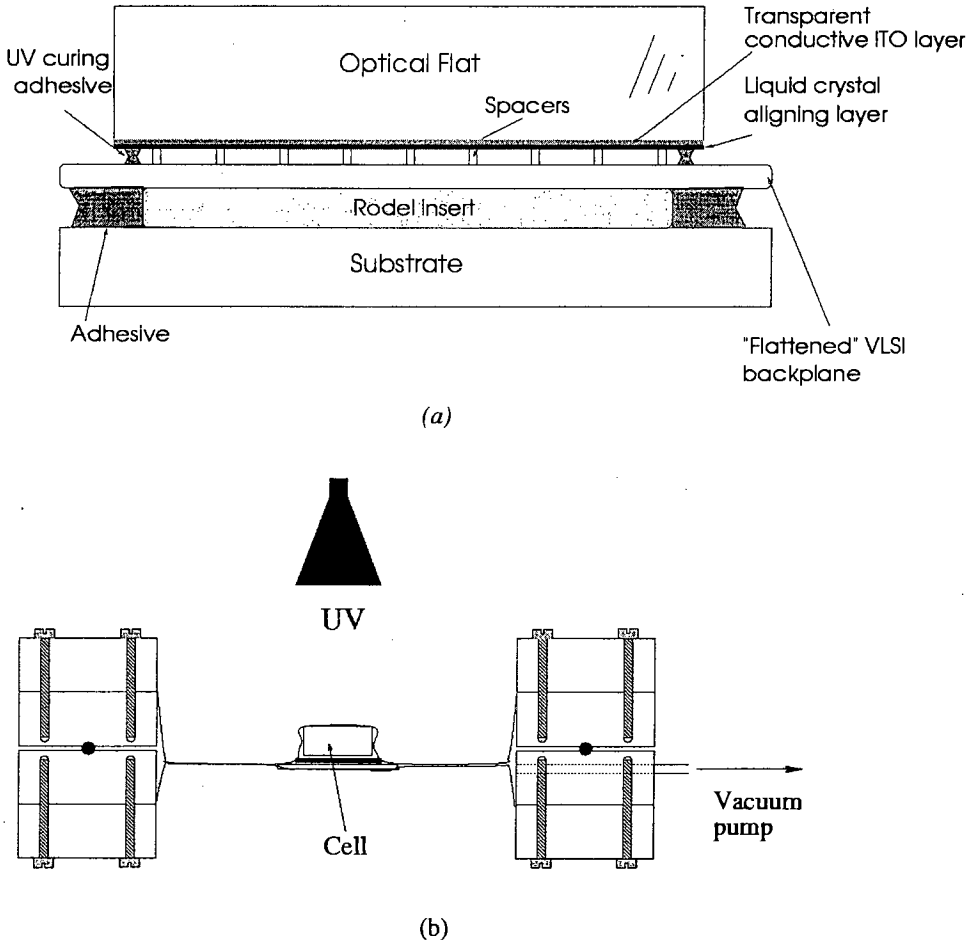
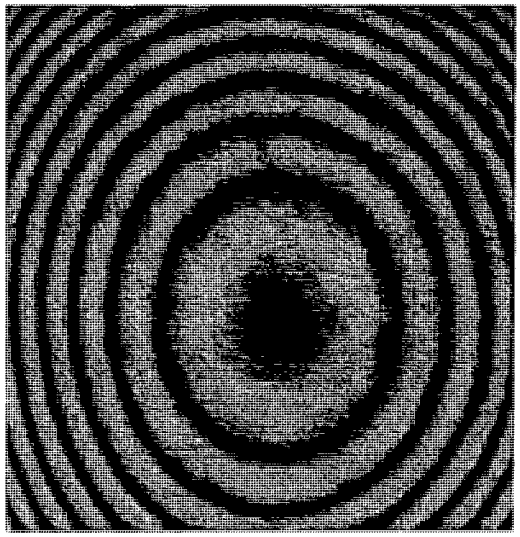
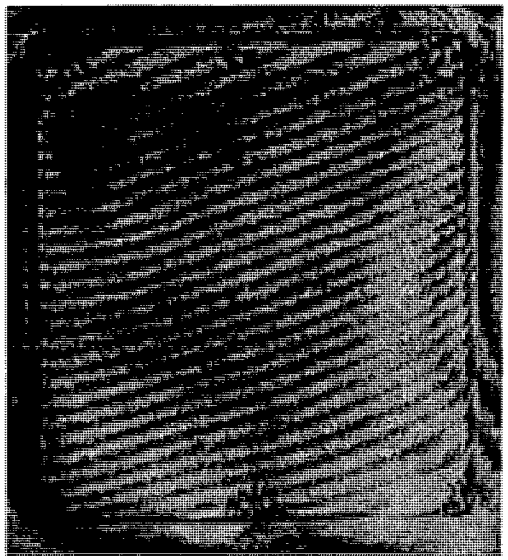


Fig. 14. (a) Cell assembly technique, using a Rodel wafer insert to provide a restoring force on the backface of the die (b) the cell is held under pressure by a vacuum packer whilst the adhesive is curing.



(a)



(b)

Fig. 15. Interferograms of (a) severely bowed silicon backplane before flattening, and (b) after cell assembly (with no backface support).

sure, to force the top surface of the die (spacer pillars) to conform to a 3 mm thick $\lambda/10$ cover-glass (Fig. 14a and b). The assembly technique [1] relies on the stress in the warped backplane and the restoring force of a compressed elastic material to firmly clamp the pillars against the rigid optical flat. A backplane flatness of $\lambda/5$ to $\lambda/8$ over a 14 mm $\times$ 14 mm device have been achieved with this technique [28] (Fig. 15). The cells, which are then filled with nematic liquid crystal are inspected between crossed polarizers. A good contact between the spacer pillars and cover-glass is observed, which is evident from the lack of liquid crystal material in these areas.

3.5. Spacer layer and cell assembly issues

There are many important considerations in assembling reflective LCoS devices and, unfortunately, spacers patterned by lift-off, for use in such devices, introduce a new issue which must be addressed. Because the final height of any feature patterned by lift-off is aspect ratio dependent we are now faced with an additional problem in that the larger geometry stepper registration marks are higher than the spacer pillars in the array. The limited silicon real estate results in these local registration marks (used by the stepper to automatically align the spacer image over each die on the wafer) being in close proximity to the active pixel area. The consequences of this are that the cell gap and backplane flatness, which is set from the optically flat cover-glass (which needs to extend past the pixel array for bonding purposes) may be destroyed by the taller registration marks.

Another problem we have in assembling LCoS devices is adhesive encroachment. Until a suitable method is found to bond the cover-glass to the silicon backplane, conventional optical adhesives will remain the most common method. Adhesive encroachment into the pixel array is a serious problem which may be minimized by a suitable geometry spacer layer. The spacer layer may also be supplemented by a trench etched around the array, into the planar oxide, which is found to be quite effective in controlling the spread of the adhesive into the cell.

3.6. Possible solutions

We have combined the trench etching step on a mask which is used to remove the troublesome spacer layer local alignment marks, Fig. 16. Of course, we still need to align the mask to each die on the wafer. Fortunately this can be done by aligning the wafer globally with a level of registration accuracy sufficient for this purpose.

3.7. Spacer geometry

The spacer layer geometry and distribution density may play an important role in the quality of the liquid crystal alignment achieved during cell filling. It has also been observed that the spacer layer must extend well beyond the pixel array to minimize any adverse effects of fringing in this area.

4. Conclusions

4.1. Planarization

The discipline of planarization of micro-mirror arrays to optical tolerances is still in its infancy. CMP appears to be

[1] Developed by M. Begbie, formerly of the Department of Physics and Astronomy, University of Edinburgh.

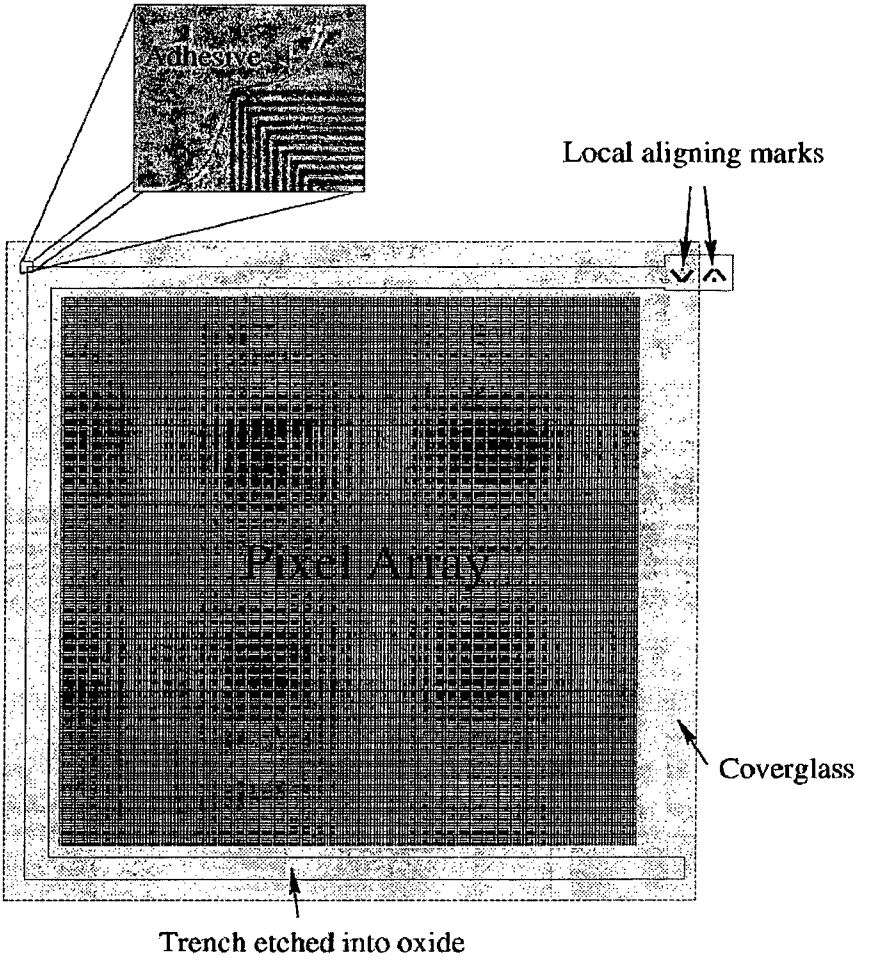


Fig. 16. Spacer layer registration mark and adhesive encroachment issues.

the most promising approach and has, for some time, been capable of reducing in-pixel topography to suitable levels [29]. The problem of using CMP to planarize a backplane with an array of pixels densely packed with circuitry in the center surrounded by a sparsely packed periphery has been highlighted. The problem has been overcome by the use of a novel process which involves the reduction of the array step height by the use of RIE etch-back. This is then followed by CMP to remove the step and surface topography completely.

4.2. Flattening

The use of conventional spacer rods and spacer balls for cell gap specification has been shown to be unsuitable for silicon backplane SLMs because the spacers can sink into the soft aluminum mirrors and can be crushed by the stresses to which they are subjected. ECR-PECVD provides a means of depositing spacers of known and highly uniform thickness which can be patterned using lithography and lift-off. All of the steps are compatible with conventional silicon wafer fabrication. The microfabricated spacers have been used in conjunction with a novel assembly technique to produce cells in which the final backplane flatness far exceeds the flatness prior to assembly.

4.3. Summary

The techniques we have described here and the results achieved using them show the potential to significantly improve the optical quality and uniformity of future SLMs and microdisplays.

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