THE UNIVERSITY *of* EDINBURGH

Reconfigurable Analogue and RF Applications of Memristive Devices

Fan Yang

Doctor of Philosophy

THE UNIVERSITY OF EDINBURGH

2024

Abstract

The Memristor is a two-terminal non-volatile electronic element, whose resistance is decided by the history of voltage or current on it. Because of these characteristics, the memristor is promising in many research directions, like artificial neural networks, memory cells, digital calculation, machine learning and so on. Compared with these directions, research on using memristors in analogue and high-frequency applications typically attracts less attention. However, the memristor also has great potential in designing reconfigurable analogue and RF circuits. By considering memristors as voltage- or current-controlled tuneable resistors, we can combine them with existing circuits and adjust/trim some of their core performance parameters. This project researches the application of memristors in analogue and RF circuit structures, rendering them reconfigurable. This thesis introduces the theories of memristors, reviews the literature on using memristors in analogue and RF applications, analyses the limitations of memristors, and researches the different methods of using memristors in reconfigurable devices. Three reconfigurable circuit structures based on memristors are discussed in this thesis: a tuneable instrumentation amplifier, a tuneable delay circuit, and a tuneable N-path filter.

The instrumentation amplifier is built on breadboards and measured with a memristor package in the laboratory, which can work under 450kHz with 9.5 to 16dB adjustable gain controlled by a memristor. The tuneable delay was simulated in Cadence with two working frequency ranges of [0.2, 10]MHz and [0.05, 1.6]GHz, which has output delay values [13, 55]ns and [269, 632]ps for each frequency range controlled by memristor-based DC voltage sources. The tuneable delay circuit is sent to tape out, and the test bench PCB for taped out tuneable delay chip is also designed. The N-path filter was built on a stripboard and measured with a memristor package in the laboratory at 1MHz center frequency with [1.5, 2]kHz variable bandwidth, controlled by the memristor. A multiple-memristor-based N-path filter structure which works at 1GHz center frequency with [0.99, 1.38]MHz variable bandwidth is also simulated. The memristor packages that have been used in the measurement are $10\times10\mu m^2$ $Pt/TiO_x/Al_2O_3/Pt$ devices. The technology that has been used in Cadence circuit design is 180nm CMOS technology.

Lay Summary

Communications technology, such as what powers mobile telephony and the internet, relies on microchips that can operate reliably and process extremely fast-changing signals (which we call "high-frequency signalling" or HF-signalling). The development of ever-better HF circuitry is the subject of active research. As one of the research approaches, researchers are trying to design devices which have the capability of performance adjustment, allowing a single device to be utilized in a wider range of working environments. To achieve it, a novel type of component called the "memristor" can be introduced into HF circuits. This is a relatively new technology, not many research groups have access to physical memristors yet and its insertion into HF circuits has to be done with extreme care to not upset the delicate balance that HF circuits normally require. For that reason, most studies attempting to understand how memristors should be used to improve HF circuits have thus far remained in the simulation domain.

In this thesis, I attempt to apply memristors in HF circuits, to adjust the performance of these devices. To achieve this goal, I designed three circuits whose partial performance can be adjusted by memristors and that work at 3 different frequency levels, which are low frequency, medium frequency and ultra-high frequency. I combined two circuits with manufactured memristor packages in the laboratory for measurement, and integrated memristor elements with the last circuit in a microchip, sending this chip to a factory for production.

My research shows the difficulties faced when operating memristors directly in HF signal environments, provides realistic measurement data for other researchers attempting to combine memristors with HF signal devices, and offers reliable approaches for combining memristors with HF circuits for other researchers. My research results will benefit researchers in designing electronic products with better performance and a wider range of applications in the future.

Acknowledgements

First of all, I would like to thank my first supervisor Professor Themis Prodromakis, for providing me with the opportunity of PhD study and funding, allowing me to develop deeper into the field of electronic circuit designing and become a better researcher.

I would also like to thank my second supervisor Doctor Alex Serb. You helped me manage the progress of the project in our weekly meetings and provided me with a lot of technical guidance when I encountered difficulties. Without your assistance, I would not be able to finish my projects and complete my PhD study successfully.

I wish to thank Doctor Shiwei Wang and Doctor Christos Papavassiliou, for giving me suggestions about my circuit designs and spending time reviewing my papers. Your advice helped my research avoid many flaws that I didn't notice. I wish to thank Mr. Grahame Reynold. The suggestions about circuit tape-out you gave to me will be valuable experiences in my career as an engineer.

I would like to express my gratitude to my parents. Because of your support, I was able to study abroad to broaden my horizons and ultimately persevere in completing my studies. Thank you for always wishing me to have a better life, and thank you for being my parents. I want to express my thanks to my girlfriend. Whenever I face difficulties, you are always there to support me. Thank you for being a part of my life, and I wish to spend the rest of my life with you.

Declaration

I declare that this thesis was composed by myself, that the work contained herein is my own except where explicitly stated otherwise in the text, and that this work has not been submitted for any other degree or professional qualification except as specified.

Fan Yang

Contents

Figures and Tables

Figures

Tables

Nomenclature

AC	Alternating Current
$CMOS$	Complementary Metal-Oxide-Semiconductor
$CMRR$	Common Mode Rejection Ratio
CPW	Coplanar Waveguide
DC	Direct Current
$ffCorner$	Transistor Fast-Fast Corner
$FPGA$	Field Programmable Gate Array
gm	Transconductance
$I-VCurve$	Current-Voltage Curve
LNA	Low Noise Amplifier
$MMIC$	Monolithic Microwave Integrated Circuit
$NMOS$	N-type Metal–Oxide–Semiconductor
$OpAmp$	Operational Amplifier
OTA	Operational Transconductor Amplifier
PCB	Printed Circuit Board
$PMOS$	P-type Metal–Oxide–Semiconductor
$QFactor$	Quality Factor
RF	Radio Frequency
$RFIC$	Radio Frequency Integrated Circuit
$RRAM$	Resistive Random-Access Memory
SNR	Signal to Noise Radio
$SPDT$	Single Pole Double Through
$ssCorner$	Transistor Slow-Slow Corner
$THD+N$	Total Harmonic Distortion + Noise
TTD	True Time Delay
UWB	Ultra Wide Band
VCO	Voltage-Control Oscillator
Vds	Drain-Source Voltage of Transistor
Vgs	Gate-Source Voltage of Transistor

Chapter 1

Introduction

1.1 Motivation and Challenge

Memristive devices, or memristors, are two-terminal non-volatile passive elements. The resistance of a memristive device is affected by the charge from different directions flowing through it. Besides, the memristive element will maintain its resistance level when no charge flows through it [19]. Because of these characteristics, a memristive device is able to record the history of current or voltage on it, which means it can be used as a memory element. On the other hand, as the history of charge can change the resistance level of the memristive device flow through it, people can also use voltage or current to adjust the resistance of the memristive device easily, hence memristive device can also work as a tuneable resistor controlled by voltage or current. If only changing the resistance between the lowest level and highest level, considering these two levels ON and OFF states, the memristive device then becomes a two-terminal switch. As the memristive device can maintain its resistance level without power supply, its power consumption is much less than other electronic elements which are volatile or active.

Since the concept of memristor was established in 1971, the memristor in the natural world has not been found. However, with the requirement of novel electronic devices, many electronic elements which have the same behavior as memristors had been designed. In 2008, HP laboratories first related their two-terminal thin-film device with the definition of memristor [2]. After that, many different kinds of memristive devices with varying materials and structures have been designed [20] [21] [22] [23] [24] [25]. They are suitable to work in different applications.

Memristors have been used in many research fields. Because the behavior of memristor is similar to the synapse in the neuron network of a human being, it is considered to have good potential in simulating synapses [26] [27] and building artificial neural networks, like spiking neural network [28] [29] [30]. Many types of research have also been done using memristor as memory cell [31] [32] [33] [34] [35], digital computation element [36] [37] [38], and analogue / radio frequency (RF) programmable circuit element [39] [40] [41] [42] [43] [44]. This report mainly focuses on the research of memristor applications in analogue and RF circuit design.

A reconfigurable high-frequency communication device can change some of its characteristics like bandwidth, signal gain, and so on, to deal with different working requirements. There are many methods to reach reconfigurable wireless communication device designing, like using micro-electromechanical (MEM) switches [45], Complementary metal–oxide–semiconductor (CMOS) circuits, monolithic microwave integrated circuit (MMIC), or radio frequency integrated circuit (RFIC) [46]. Compared with them, the advantages of memristor are low power consumption [47], fast switching speed [48] [49], small area usage [50], and good compatibility with CMOS technologies [51] [52] [53].

When considering the “high-frequency behavior” of memristive devices a distinction must be made between two very different aspects: a) the behavior of resistive switching under very fast timescales and b) more classical frequency domain/response characterization dealing with how signals pass through the memristive device. In this work, we mainly preoccupy ourselves with memristors as trimming/tuning elements for high-frequency circuits and hence are more concerned with aspect (b). This includes the study of transmission, reflection, and distortion ratios when high-frequency small signals pass through our devices.

One of the main problems that limited the high-frequency applications of memristors is the parasitic capacitance in the memristor device. As the structure of a metal-oxide-metal memristor is similar to a metal-insulator-metal(MIM) capacitor, the memristor also has an unwanted capacitance in between its two metal layers. The parasitic capacitance value depends on the size, material, and technology of the memristor. For RF reconfigurable circuits design, the type of memristor being used is normally memristor RF switch [54], which can work in very high frequency, but only program between two states. Although the memristors being used in analogue circuit design normally have the ability of analogue resistance programming that can offer multiple resistance levels, most of these analogue memristors have a high signal distortion ratio at high frequency. Because of that, memristors with multiple stages are hard to apply in high-frequency circuits.

1.2 Objectives

This thesis researches on expanding the applications of the memristor in high-frequency reconfigurable devices. To reach this objective, research is done on combining analogue memristors with reconfigurable devices that work in different frequency levels for signal trimming. The research in this thesis includes the applications of memristive devices in three different frequency levels, as shown in Figure 1.1. First, a memristor is combined with an instrumentation amplifier which works at low frequency, to adjust the gain of the amplifier. The circuit is built on a breadboard and measured with a memristor package in the laboratory. This project verifies the feasibility of combining memristors with existing analogue circuit structures and makes them reconfigurable in practice. Second, the memristor is used in the

design of a tuneable delay circuit that can work in low GHz(ultra high frequency). To avoid the condition that the GHz delay circuit doesn't work and nothing can be measured from the circuit, and also as a comparison partner of the GHz delay circuit, a delay circuit which has the same structure as the GHz delay circuit but works at 10MHz(high frequency) is also designed. The whole tuneable delay is sent for tape-out progress. At the same time, a PCB is designed as the testbench of the tuneable delay circuit. Finally, based on the experience of the two subjects before, memristors are considered to be used in N-path filter structures. A tuneable 4-path filter is built on a stripboard and measured with a memristor package in the laboratory. This memristor-controlled 4-path filter can work at 1MHz(medium frequency) in measurement. A memristor-based N-path filter structure that works at 1GHz(ultra high frequency) is also simulated. These three subjects prove the feasibility of applying multi-stage memristors in high-frequency reconfigurable devices in practice and show the potential of multi-stage memristive devices in the direction of designing high-frequency reconfigurable circuits. The memristor package used in the laboratory measurement of this research has $10\times10\mu m^2$ TiO_x/Al_2O_3 memristors, and the technology used in the Cadence simulation is 180nm CMOS technology.

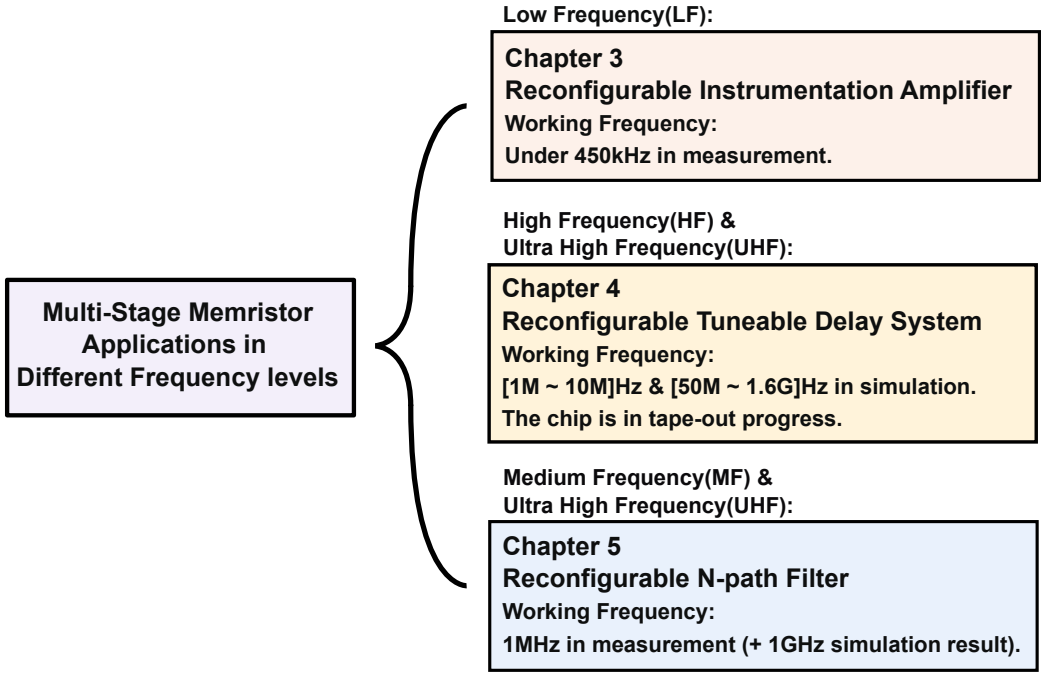


Figure 1.1: The memristor applications that have been researched in this thesis. Based on radio frequency spectrum bands, in this thesis memristors are applied in reconfigurable devices that work in different frequency levels, including low frequency(LF), medium frequency(MF), high frequency(HF), and ultra high frequency(UHF).

1.3 Thesis Overview

Chapter 2 discusses the background knowledge about the memristor and the related analogue/RF reconfigurable designs. First, the concept and behavior of memristor are introduced. Then the frequency domain characterizations of analogue memristors are analyzed, literature on using memristors in analogue and RF reconfigurable devices are reviewed, and methods of using memristor which has relatively poor frequency domain characters at high frequency are considered.

In Chapter 3, a reconfigurable instrumentation amplifier controlled by a memristor is designed, built on a breadboard, connected with a memristor array package and finally measured in the laboratory. In measurement, this reconfigurable instrumentation amplifier can work at frequencies under 450kHz, with tuneable gain in a range of [9.5, 16]dB controlled by a memristor.

In Chapter 4, a memristor-based tuneable delay circuit is discussed. The delay elements are originally controlled by switched capacitors in the literature. In this research, memristor-based DC voltage sources are used to control the delay elements and adjust the output delay time of the circuit. A delay circuit works at 10MHz and a delay circuit works at 1.6GHz are designed. The two delay circuits, the memristor-based DC sources, the memristor programming controller, and the output buffers of the delay circuits are designed as a chip, which is in the tape-out process now. In Cadence simulation, the memristor-based DC voltage sources offer DC voltage in a range of [584, 711]mV, the MHz delay circuit can off a tuneable delay range of [13, 55]ns in the frequency range from 200kHz to 10MHz, and the GHz delay circuit has a tuneable delay range of [269, 632]ps in a frequency range of [0.05, 1.6]GHz. A PCB board is designed to measure the chip. The operations in the chip measurement process are also recorded in this chapter.

Chapter 5 discusses the possibility of combining memristors with N-path filters. Different structures of memristor-based reconfigurable N-path filters are designed, simulated and compared. One of the tuneable 4-path filter structures is measured with a memristor array package in the laboratory. Measurement results show this 4-path filter can work at 1MHz, with a tuneable bandwidth [1.5, 2]kHz controlled by a memristor. The drawbacks of the memristor-based N-path filter are discussed, and a tuneable N-path filter that uses multiple memristors is designed and simulated. In the simulation, the tuneable N-path filter with multiple memristors can work at 1GHz, which has a tuneable bandwidth of [0.99, 1.38]MHz.

Finally, Chapter 6 concludes the research in this thesis, discusses some of the problems of applying multi-stage memristors in reconfigurable RF circuits, and introduces the future work of the subjects in this thesis.

Chapter 2

Review of Memristive Technologies and Memristor-based Applications

2.1 Introduction of Memristor

The memristor concept was first defined by Chua in 1971 [19]. He inferred that based on the existence of three basic circuit elements, resistor, capacitor and inductor, which link to the relationship between voltage, current, flux and charge, there should be a lost fourth electronic element that can link to the charge and flux in mathematics, as shown in Figure 2.1.

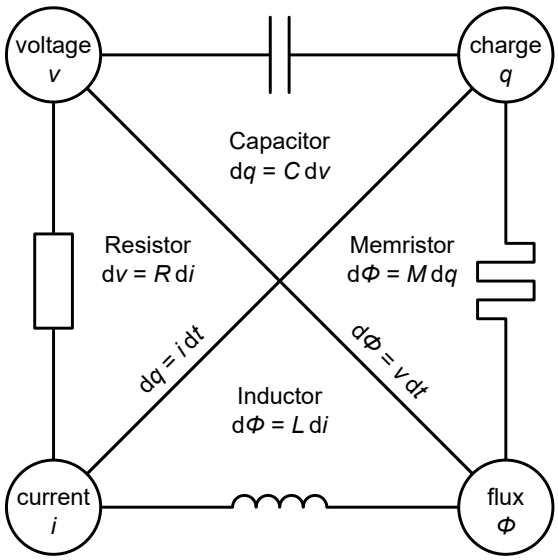


Figure 2.1: The relationship between four basic electronic elements [1]. Memristor is the element that links the relation between charge and flux in mathematics.

The relationship between memristor value, charge and magnetic flux linkage is shown as Equation 2.1, in which M is the memristor value. The equation Equation 2.1 also shows that the memristor works as a charge-dependent resistor. The value of a memristor can be changed by the charge applied to it, and when the memristor value is constant, its function is just like that of a resistor.

$$M(q(t)) = \frac{\frac{d\phi}{dt}}{\frac{dq}{dt}} = \frac{V(t)}{I(t)} \tag{2.1}$$

With the development of nano-electronic technologies, many thin-film nanoscale devices which have similar behaviour as memristor have been designed [20], but nobody connects them with the concept of memristor. In 2008, Strukov et al manufactured a two-terminal non-volatile $P_t/TiO_2/P_t$ device, and first linked this device with the concept of memristor, as they have a similar key function. Since then, this type of artificial metal-insulator-metal electronic elements were also seen as memristors. Until now, many different memristive devices with Metal/Insulator/Metal structures have been designed.

Figure 2.2 (a) shows the basic principle of the memristor element generated by HP laboratory [2]. The memristor has a semiconductor film with a length of D in between two metal layers. The right part of the semiconductor is stoichiometric TiO_2, in which the oxygen to titanium is perfect 2:1. The left part of the semiconductor is also titanium dioxide but misses some of its oxygen, which is written as TiO_{2-x}. Because the oxygen vacancies in the TiO_{2-x} region are positively charged, the TiO_{2-x} part can be considered as "doped" region with length of w whose dopant is positive ions, and the normal TiO_2 part is "undoped" region. As oxygen vacancies work as charge carrier, TiO_{2-x} is conductive low resistance material, while TiO_2 is high resistance semiconductor. The electrode close to the doped region(TiO_{2-x}) is the positive pole of the memristor, and the electrode close to the undoped region(TiO_2) is the negative pole. When voltage applied to the memristor from the positive pole, the positive charged oxygen vacancies are pushed to the TiO_2 part and transform TiO_2 to TiO_{2-x}, increase the length of the TiO_{2-x} part. As the low resistance region expands, the resistance of the whole memristor reduces. Oppositely, when voltage applied to the negative pole, the oxygen vacancies are pushed to the positive pole, makes the TiO_2 region expand and increases the resistance of the memristor. Because of that, a memristor can work like a tuneable resistor whose resistance varies with the voltage on it, as the circuit in the right part of Figure 2.2 (a). The ratio w/D shows the resistance level of the memristor. When w/D closes to 1, nearly the whole semiconductor layer in the memristor is transformed to low resistance TiO_{2-x} material, the memristor resistance trends to minimum value; When w/D closes to 0, nearly the whole semiconductor layer is transformed to the high resistance TiO_2 semiconductor, thus the memristor resistance trends to its maximum value.

Memristor has both "static" and "dynamic" resistance variation characteristics. The static resistance variation happens when different voltages with values lower than a threshold voltage applied to a memristor. The electric field is insufficient to generate significant structural changes in the memristor, but causes limited change in the local charge distribution of the TiO_2/TiO_{2-x} materials, and make the memristor shows different resistance values under different voltages. The dynamic resistance variation happens when a voltage higher than the threshold applied

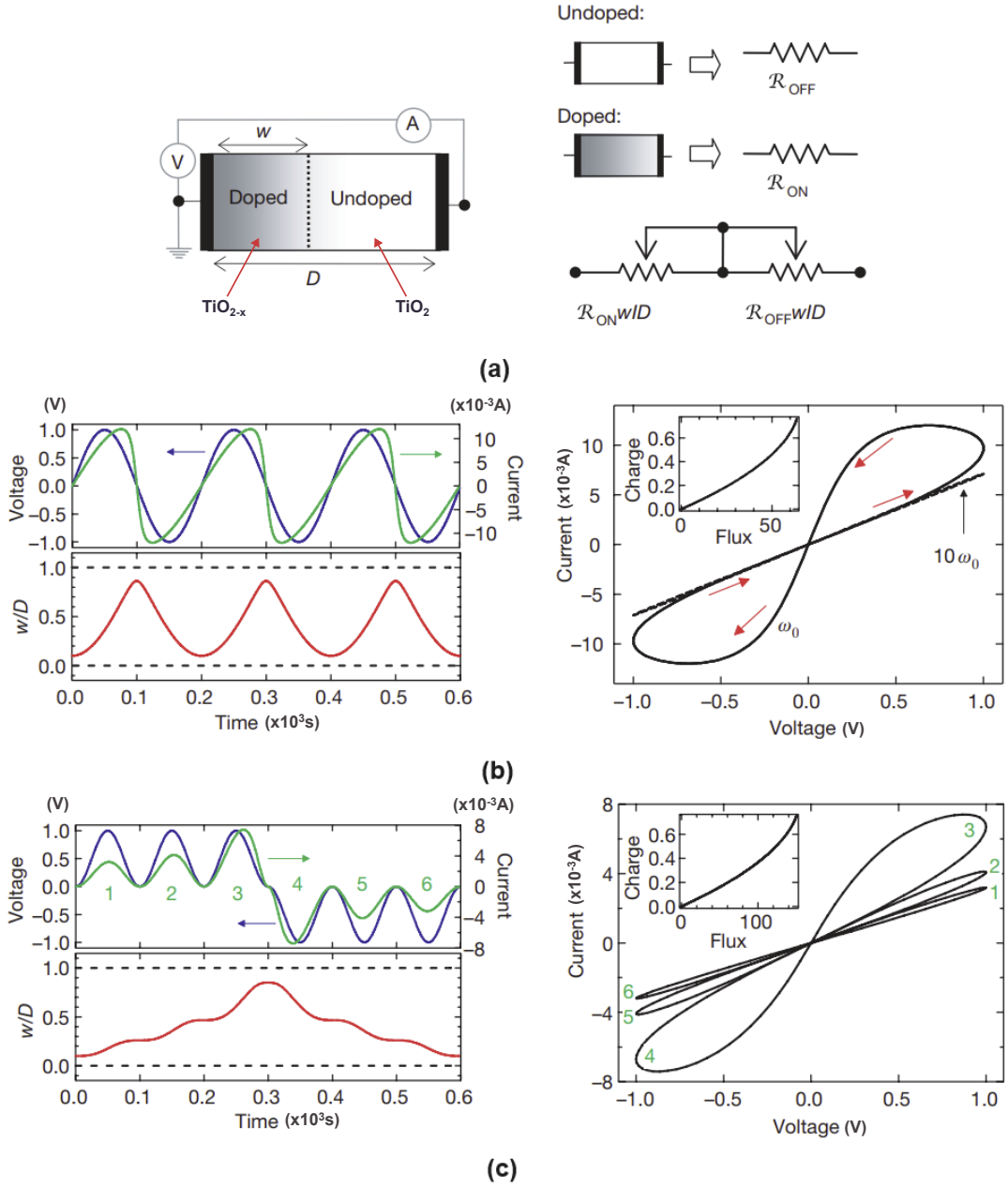


Figure 2.2: (a) Simplified equivalent circuit of a memristor. (b) Output current wave, w/D radio and I-V curves of a memristor when the input voltage sine wave continuously changes direction. (c) Output current wave, w/D radio and I-V curves of a memristor when the input voltage sine wave maintains in one direction for several periods. [2]

on the memristor, large electric field changes the internal structure of the memristor significantly by shifting the boundary between TiO_2/TiO_{2-x} material or forming/breaking the filament in a filament-based memristor, and causes non-volatile resistance changes. The threshold voltage is the minimum voltage required to generate a sufficiently strong electric field to mobilize the ions in the TiO_{2-x} material of Figure 2.2 (a). It is also the minimum voltage to

form or break filaments in filament-based memristor structures, which will be discussed in the following paragraphs. Figure 2.2 (b) shows both the static and dynamic resistance variation characteristics. In the left-hand side waves, a sin wave AC voltage signal is applied to the memristor device, the blue curve is the input voltage wave, and the green curve is the current wave that flows through the memristor. The input voltage fluctuates between 1V and -1V, which shows the voltage applied on the memristor changes direction every period. The right-hand side figure in Figure 2.2 (b) is the I-V curve of this memristor, which shows the variation of current on the memristor with the change of the input voltage value. The red arrows show the time flowing in one period of voltage signal. The voltage starts from 0V, rises to 1V, then reduces to -1V, and finally back to 0V. When the voltage is low, the I-V curve is nearly linear, which means the resistance is close to a constant value. When the voltage is close to 1V, the I-V curve of the memristor becomes non-linear, which shows the memristor static resistance variation. After the voltage reaches the maximum value and reduces to smaller than 0.5V, the I-V curve has a different constant gradient, showing the resistance has been changed to a different constant value, which is the dynamic resistance variation direction. In this example, the threshold voltage of the memristor is about 0.8V. When voltage reduces to minus value, the voltage applies to the memristor from the opposite direction, and will also change the memristor value in the opposite direction. After one period of input voltage wave, the resistance of the memristor is changed back to the original value, as the input voltages to the memristor from the two directions are the same. The charge-flux plot shows the charge is a single-valued function of the flux value [2]. The dynamic resistance variation of a memristive device needs a large amount of charge and a voltage that is higher than the threshold voltage of the memristor. The electrical characteristics of the memristor, including the threshold voltage value and the time needed for memristor resistance level changes between the max/min stages, are closely related to the formation, thickness and structure of materials in the insulating layer of the memristor [55].

Figure 2.2 (c) mainly shows the dynamic resistance variation characteristic. Different from the condition of Figure 2.2 (b), Figure 2.2 (c) first applies 3 periods of input voltage to the memristor from one direction, then applies 3 periods of voltage to the memristor from the opposite direction with the same amplitude. The 6 periods of voltages are labelled as numbers 1 to 6. The I-V curves on the right-hand side show the variation of memristor resistance in each period. In period 1, the slope of the I-V curve is small, showing that the memristor has a large resistance value. In periods 2 and 3, the slopes of the I-V curves increase, which means the resistance is reduced by the input voltage from the same direction step by step. By applying multiple high voltage(1V in this case) pulses to the memristor from the same direction, the resistance of the memristor can be shifted to a different value. After that, periods 4, 5 and 6 show the voltage applied to the memristor from the opposite direction with the same amplitude and increase the memristor resistance back to the original value.

The memristor structure and I-V curve are not limited by the representation of Figure 2.2. Instead of doped and undoped regions in the semiconductor, some memristor structures have low-resistance filaments in the insulator layers [56] [57]. As many transition metal oxides which conduct both electron and ions can be used to generate memristive devices [58], some of the memristors use other materials instead of TiO_2 [56] [59], and some others combine multiple material layers in the memristor [22] [24]. An example of a memristor with filament structure and $LiNbO_x$ material is shown in Figure 2.3 [3]. The basic structure of this filament-based memristor includes two metal electrodes and a dielectric layer($LiNbO_x$/$LiNbO_3$). Similar to the TiO_{2-x} layer in Figure 2.2 (a), the $LiNbO_x$ material also includes large amount of positively charged oxygen deficiencies. When applying a voltage that higher than threshold to the bottom electrode, the ions in the $LiNbO_x$ are pushed toward the top electrode, and form a conductive filament. In Figure 2.3 (b) and (c), it can be observed that with more voltage pulses applied on the bottom electrode, the filament becomes longer and thicker, which reduces the resistance of this memristor. When applying voltage on the top electrode, the filament is dissolved back to ions. Except of generating filament by oxygen deficiencies in semiconductor materials, the filament can also be formed by metal cations. Reference [60] introduces a memristor structure which has an electrochemically active electrode made by Ag, an electrochemically inert electrode made by Pt, and a solid electrolyte layer in between them. When a voltage higher than threshold applied on the active electrode, anodic dissolution reaction happens on the Ag metal and generates Ag^+ cations. Due to the electric field, the Ag^+ cations migrate to the inert electrode, then reduce to Ag metal on the surface of the inert electrode and form an Ag filament according to the cathodic deposition reaction. When applying a high voltage to the inert electrode, the metal filament is dissolved to cations again [56]. With different designs, fabrication technologies and materials, the I-V curves and resistance ranges of different memristors also vary. However, an analogue memristor will always have the static and dynamic resistance variation characteristics, to make it work as a tuneable resistor.

In this research, the operation of memristors can be classified into two modes, which are the normal work mode and the programming mode. In normal work mode, memristors are supposed to behave like a normal constant resistor; In the programming mode, the resistance of memristor will be changed by external devices. The usage of memristors also follows the static and dynamic characteristics of the memristor. As a large DC voltage applied on the memristor continuously will change the memristor resistance or even destroy the memristor elements, to make sure the memristor can behave as a constant resistive element in normal work mode, it is the best to control the DC voltage on the memristive device smaller than or equals to 0.5 V, especially for long sequences of reading operation. Besides, as the memristor resistance value varies with the voltage applied to it, the voltage on the memristor should be maintained nearly constant. Prolonged exposure to even normally sub-threshold voltage may still cause resistive state drift, and hence large margins are used. 0.5V is chosen in the normal work mode as this value is low enough that will not cause dynamic resistance variation of the

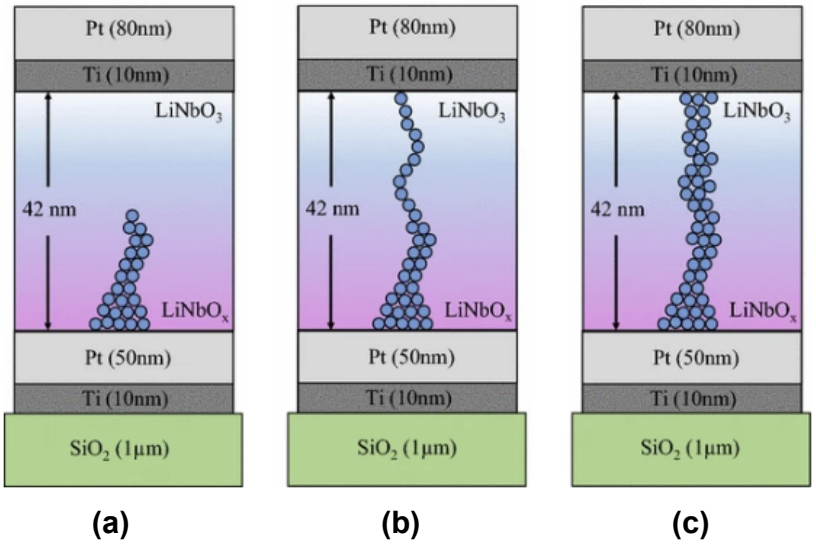


Figure 2.3: A memristor with Ti/Pt/$LiNbO_x$/$LiNbO_3$/Ti/Pt structure. When voltage pulses applied on the bottom electrode of the memristor, (a) The filament starts growing, the resistance of the memristor is reduced. (b) Pulses continuously applied on the bottom electrode, formation of the filament finish, the resistance of the memristor reaches a low value. (c) With more voltage pulses, the filament becomes thicker, and the memristor resistance reaches the minimum value. [3]

memristor with TiO_2/Al_2O_3 structure which is used in this research, but is high enough to offer a good signal to noise ratio when reading the memristor resistance [61]. Opposite to the small constant voltage applied to the memristor in normal work mode, in the programming mode, voltage pulses with large amplitude are applied to the memristor, to make sure the resistance of the memristor can be adjusted to the wanted value [4].

To explain the memristor programming process clearly, a simulation of memristor model programming is made in this research as an example, as shown in Figure 2.4. The simulation is done in Cadence Virtouso environment. The memristor is programmed from 12kΩ to 15.5kΩ, by voltage pulses with amplitude 1.5V and pulse width of 5μs. 5μs is a value that much higher than the minimum memristor programming period. As the aim of this simulation is just showing an example of memristor programming, there is no need to program the memristor quickly, hence this value is chosen to make sure the programming process can be done smoothly. It can be observed that when reading the memristor value under 0.5V voltage, the memristor shows 12kΩ to 15.5kΩ resistance, and when reading the memristor value with 1.5V voltage, it shows 1.7kΩ to 2.2kΩ resistance. When programming memristive devices to a specific resistance value, first the original memristor value will be read, and then positive or negative voltage pulses will be applied to the device, depending on whether the initial resistance needs to be reduced or increased. After several pulses have been applied to the

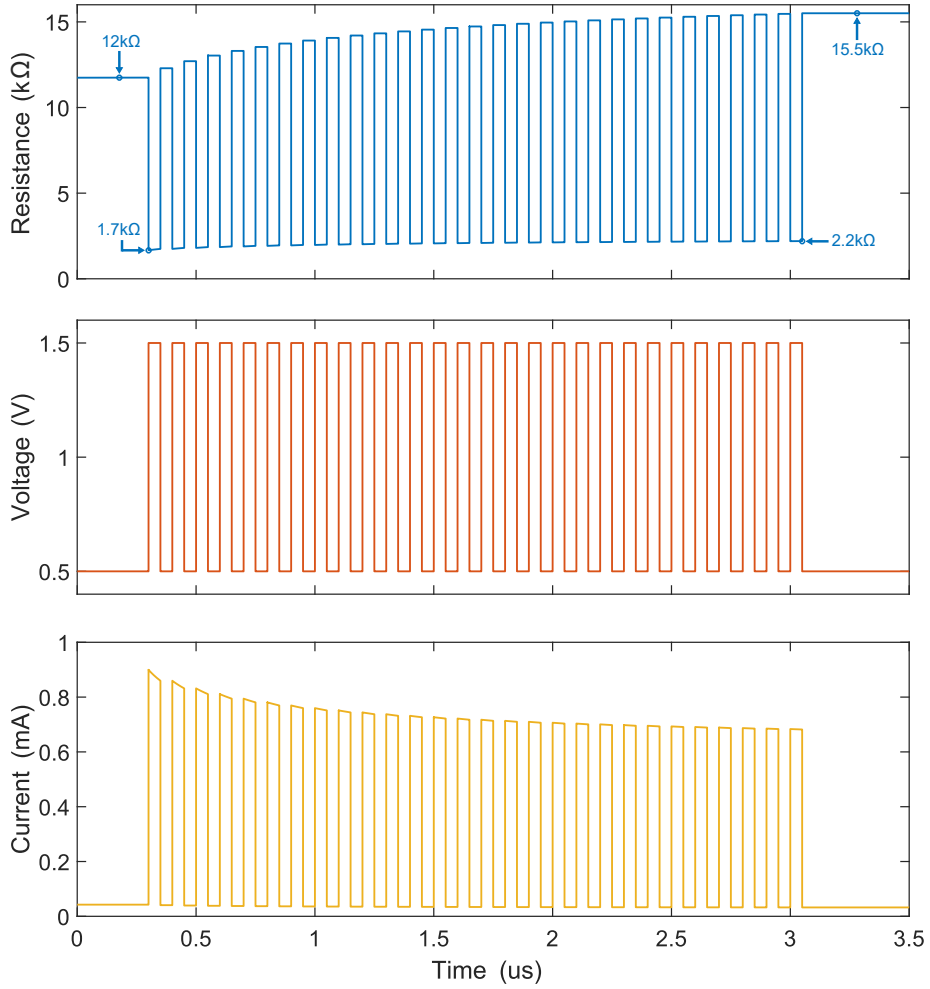


Figure 2.4: An example of programming a memristor model in Cadence. The diagrams from up to down show the resistance of the memristor, the input voltage applied to the memristor, and the current flows through the memristor.

device, the resistance value will be read again. If the resistance has not reached the specific value, the instrument will continue applying pulses to the memristor, and if the resistance has changed too much compared with the target value (resistance “undershoot” or “overshoot”), the instrument will apply pulses in the opposite direction to adjust the resistance.

In this project, measurement instruments “Arc One” and “Arc Two” are used to program the memristor in the laboratory. ArC One and Two are measurement instruments that can work well with crossbars of emerging non-volatile memory technologies, including memristor, resistive memory, phase-change memory, and others [61]. ArC One can be used in read/write of memory components, I-V curve measurement and current cut-off forming. Based on the functions of ArC One, ArC Two has fully parallel characteristic, which allows it to achieve concurrent and independent control of its 128 channels. As an example, when Arc One is used for programming the memristor, it will first transmit some pulses in the default direction. If the

trend of memristor resistance changing is opposite to the wanted result, Arc One will reverse the pulse direction and do the work again. During programming, Arc One will read the value of the memristor in real-time, and when the memristor resistance is close to the target value within an acceptable tolerance, the instrument will stop the program. Pulse amplitude starts from a low value to protect the memristor, and will progressively increase during programming. For the memristors used in this project, the device can maintain a stable resistance level for biasing below approximately 1.2V, loosely defined as the switching threshold of the device, hence the pulse voltages chosen to program the memristor are in the [0.6, 2]V range. The pulse starts from a guaranteed non-invasive level and ramps up progressively in order to give a chance to the device to change its state using gentle pulsing. By starting the programming from a small pulse amplitude, the possibility of accidentally destroying the memristor can be reduced, and the device ageing can also be slowed down [61]. More information about the algorithm used to program the device can be found in reference [61]. In this project, for the memristor package in the laboratory, the programming voltage is limited to 2V to make sure the memristive device is not destroyed. The amplitude of programming voltage depends on the technology of the memristor. In some cases, the programming voltage needs to be higher than 5V. For example, the novel $1\mu m^2$ TiO_2/Al_2O_3 memristor model used in the circuit design of Chapter 5 of this research needs a programming voltage of 5.5V.

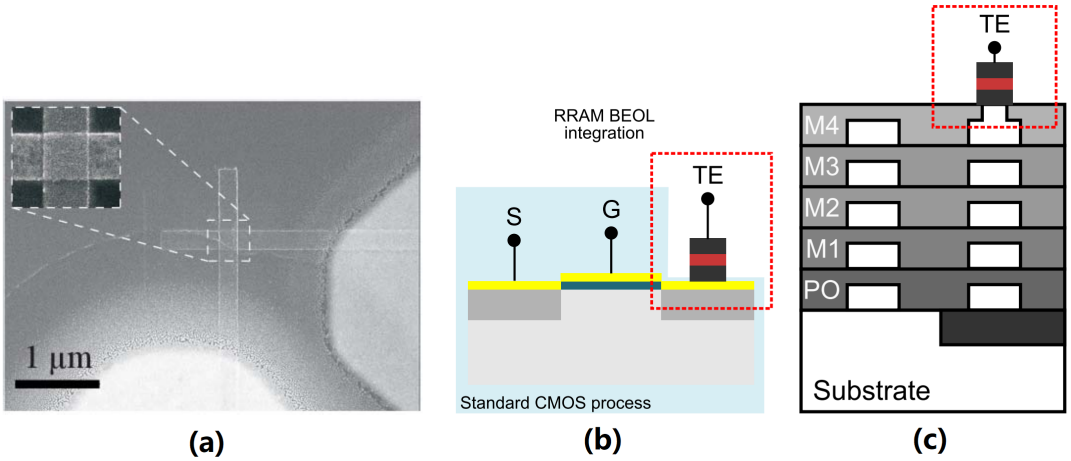


Figure 2.5: (a) Photo of a memristor at the crosspoint sub-$1\mu m^2$ active area. (b) Back-end-of-line integration of a memristor on a standard CMOS process. "TE" is the top electrode of the memristor. (c) Straightforward post-CMOS integration of memristor on a multi-layer material structure. [4]

Figure 2.5 (a) shows a photo of a memristor at the crosspoint of two electrodes [4]. As the typical structure of a memristor is metal-oxide-metal stack layers, a memristor can be formed between two metal electrodes with a dielectric layer in between them. The multi-layer stack structure of memristors allows it to integrate with CMOS technologies, which also have multi-layer structure. Figure 2.5 (b) shows the back-end-of-line(BEOL) integration of a

memristor on the drain of a transistor, and Figure 2.5 (c) shows the physical structure of a memristor integrated on the top of CMOS material layers. The form and connections of different electronic elements in a CMOS circuit are based on different material layers, which are one poly layer and several metal layers. By using the top metal layer(M4 in Figure 2.5 (c)) as one of the electrode metal layers of the memristor, the memristor structure is hence integrated on the top of the CMOS circuit.

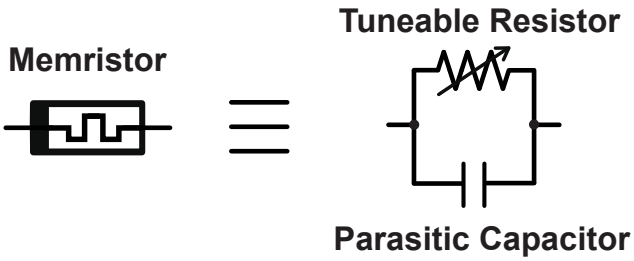


Figure 2.6: A lumped element model of memristor. A memristor can be considered as one tuneable resistive element in parallel with one fixed parasitic capacitive element.

As the two metal layers in the memristor structure can be seen as a capacitor, the lumped element model of the memristor can simply be seen as a tuneable resistor in parallel with a small capacitor, as shown in Figure 2.6. This simplified memristor model only been used in frequency response analysis, and considers the memristor function as a tuneable resistor, excludes the threshold voltage and static/dynamic characteristics of memristors. When using the memristor model in Cadence Virtuoso environment, the tuneable resistor part is replaced by a memristor function model written in Verilog-A language, to simulate the threshold voltage and non-linear I-V characteristics of the memristor. In reality, there are also some small inductances in series with the parallel resistor-capacitor element caused by the connection ports between the memristor and circuit [62] [63]. However, as this inductance only form as an additional impedance in series with the resistive memristor at high frequency, and for RF-used memristors the parasitic inductance is only around 1nH per electrode [64], it is normally ignored when designing lumped element memristor modules. As the distance between two metal layers maintains a constant value, ideally the parasitic capacitance of the memristor is also constant. The value of the capacitance depends on the size and material of the memristor. Because of the existence of parasitic capacitor and inductor, the frequency will affect the impedance of the whole memristor, hence limiting the working frequency range of the memristor.

Figure 2.7 shows the impedance frequency response of a $Pt/TiO_x/Al_2O_3/Pt$ memristor with size $10\times10\mu m^2$ [5]. It can be observed from Figure 2.7 that for this memristor, all the resistance levels start to reduce after about 3MHz, and the higher the resistance level, the earlier the impedance starts to reduce with the increase of frequency. For the highest resistance level shown in Figure 2.7 which is 88kΩ, its impedance starts to reduce from

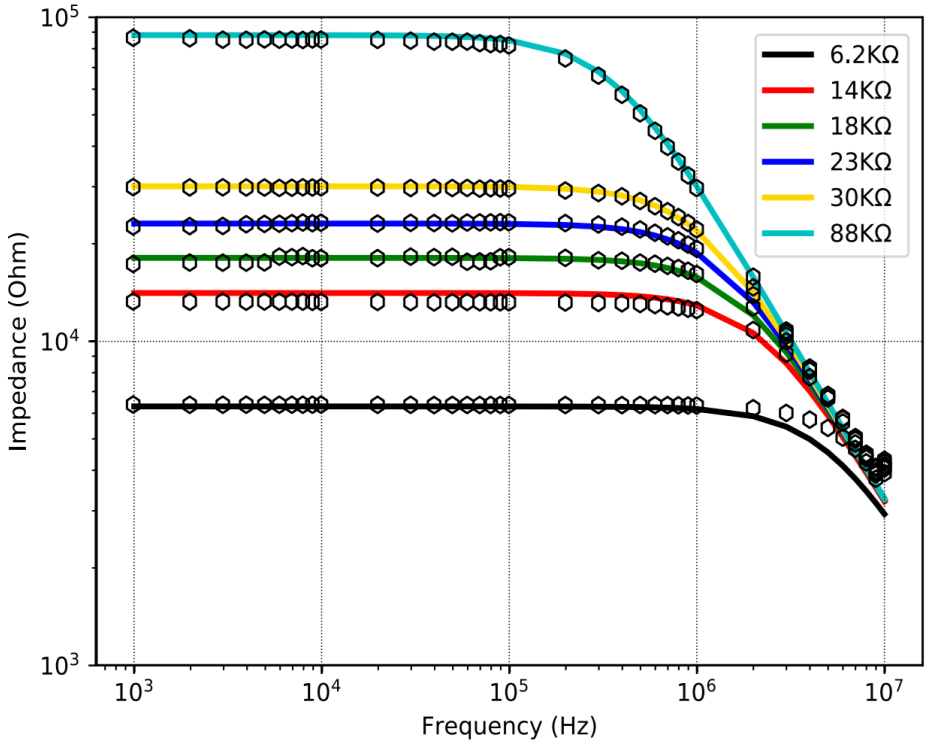


Figure 2.7: Impedance-frequency response of a TiO_x/Al_2O_3 memristor. Related to the resistance level of the memristor, the cut-off frequency of this memristor varies in a range of around [0.3, 3]MHz. [5]

about 100kHz. When a signal with 1MHz frequency flows through this memristor which has a [6.2, 88]kΩ tuneable resistance range, it can only work as a resistor with a [6, 32]kΩ resistance range. When a 10MHz signal flows through it, the memristor can only show about 2kΩ to 3.5kΩ resistance. The problem is mainly caused by the high parasitic capacitance between the metal layers. The metal-oxide-metal layer structure of a memristor is similar to a metal-insulator-metal capacitor, the two metal layers also form a parasitic capacitor. The parasitic capacitance of this memristor is approximately 10pF. The parasitic capacitance mainly depends on the size, thickness and dielectric constant of the semiconductor layer in the memristor. Larger size causes larger parasitic capacitance, as the 10pF large parasitic capacitance of this $10\times10\mu m^2$ size memristor. This characteristic limits the high-frequency applications of multiple-stage memristors.

To expand the application of memristors in radio frequency, many memristive devices which being used as RF switches have been designed [65] [66] [10]. One of the structures of the memristor RF switch is shown in Figure 2.8 [6]. It can be found from Figure 2.8 (a) (b) that the memristor is fabricated on a coplanar waveguide (CPW) transmission line, and the technology and material are all different from the multi-stage memristor discussed before. This memristor RF switch is fabricated on an intrinsic silicon wafer with a 380nm thermally

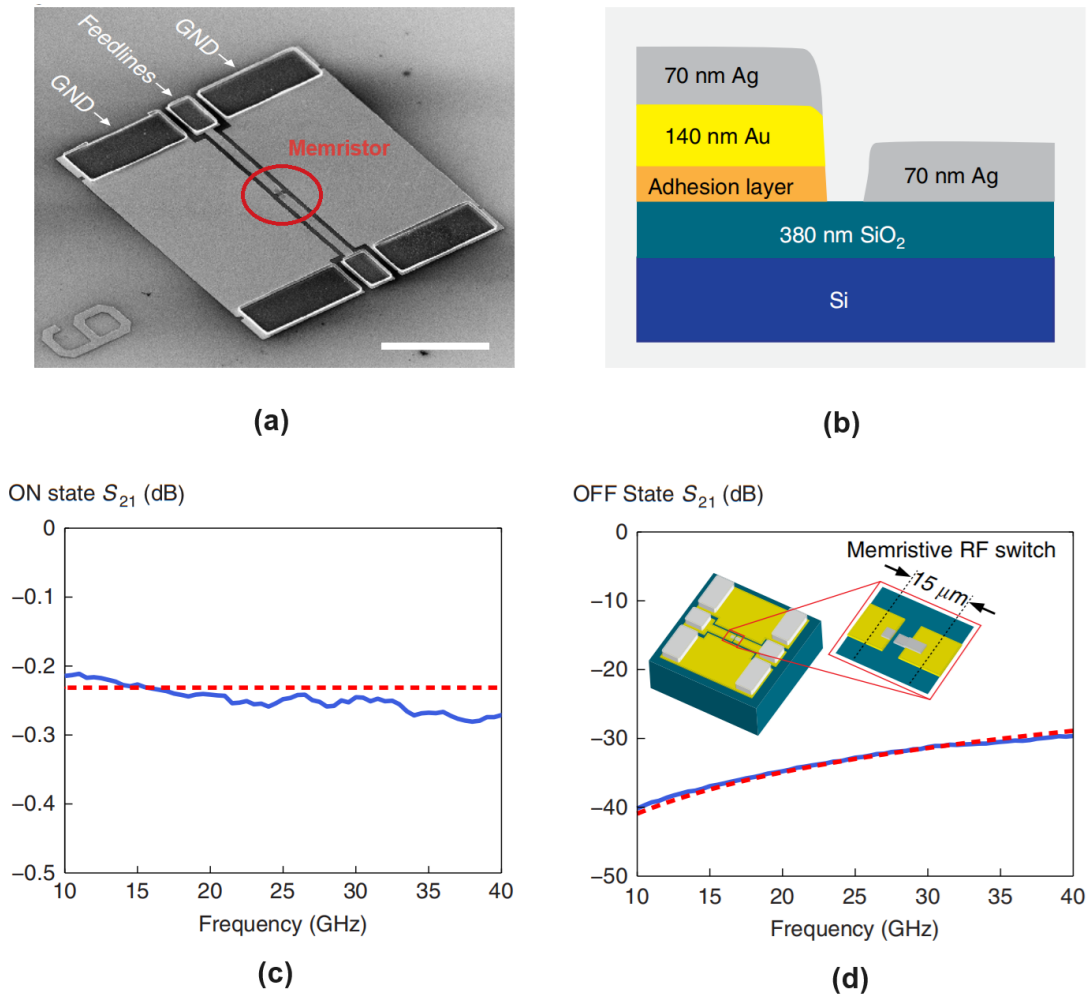


Figure 2.8: (a) Image of a memristor RF switch. (b) Schematic illustration of geometry for this memristor RF switch. (c) Signal transmission loss of the RF switch ON state. (d) Signal transmission loss of the RF switch OFF state. [6].

grown silicon dioxide layer. One terminal of the memristor is composed by a gold(Au) layer with a thickness of 140nm and a very thin titanium(Ti) adhesion layer, another terminal of the memristor is generated by silver(Ag) with a thickness of 70nm. Instead of a dielectric layer, there is a 35nm air gap in between the two terminals. When applying voltage to the Au/Ti terminal, a 100nm-wide continuous Au filament is formed in the 35nm air gap, and the memristor switch is turned on. The thickness of thermally grown silicon layer, gold layer and titanium adhesion layer, as necessary conditions for forming the memristor structure, does not affect the performance metrics of the RF memristive switch. The low bulk resistivity of sliver, combined with the short air gap length (35nm) and the relatively large cross-sectional area ($70\times100nm^2$) of the sliver metal layer, results in a very small ON-state insertion loss (-0.3dB

at 40GHz) and a low programming voltage (0.4V) of the memristor RF switch. On the other hand, the low effective dielectric constant and the high resistivity of the air gap results in a very small parasitic capacitance (average 1.4fF) in between the thermals and a very large OFF-stage isolation rate (-30dB at 40GHz) of the RF switch.

Figure 2.8 (c) (d) show the memristor RF switch has low insertion loss for the ON state and high isolation at the OFF state. The ON resistance of the switch is around 3.6Ω, the OFF resistance is 10^{12} times the ON resistance. The parasitic capacitance is smaller than 2fF, which makes the memristor RF switch work at high GHz. The parasitic capacitance value of the memristor RF switch is much smaller than the analogue memristor in the previous paragraphs. This is because the air gap in the memristor RF switch has a very small dielectric constant, and the cross-sectional area of the terminals in the memristor RF switch is much smaller than the electrode area of the analogue memristor. However, this memristor RF switch only has ON and OFF two states, and can only work with very high frequency.

In addition to the multi-stage memristor and the memristor RF switches, there are still other memristor structures with distinct characteristics, such as the digital memristor that exhibits extremely fast switching speeds [67]. The operation period of this type of memristor can be reduced to smaller than 100ps [68]. However, as this research focuses on applying memristors in analog signal processing, the other memristor structures are not been further discussed in this thesis. When considering the use of memristors in circuit design, it is necessary to differentiate between various types of memristors, identify functional differences among different structural configurations of memristors, and choose the appropriate type of memristor based on the specific design requirements.

2.2 Literature of Analogue / RF Application of Memristor

In this section, some of the analogue and RF reconfigurable circuits based on the application of memristors which have been published by other researchers are shown and compared. As different applications use different types of memristors, all the applications are classified by the types of memristors they use, which are analogue memristors or memristor RF switches. The main applications of memristors in analogue and radio frequency fields shown in this report are designing amplifiers, filters, modulators, resonators, active inductors, attenuators, and delay cells. It is important to note that due to the varying functionalities and design purposes of each designed circuit, and considering that this research aims to explore the application of memristors in larger frequency ranges, this section only documents the working frequency of each product, without recording other performance values.

2.2.1 Analogue and Low-Frequency Application of Memristor

In lower-frequency applications, memristors can be used as tuneable resistors, to help design reconfigurable analogue devices. The simplest method of using a memristor in analogue circuits is replacing some of the resistors in the original circuits with memristors, to make the characteristics affected by these resistors becomes controllable.

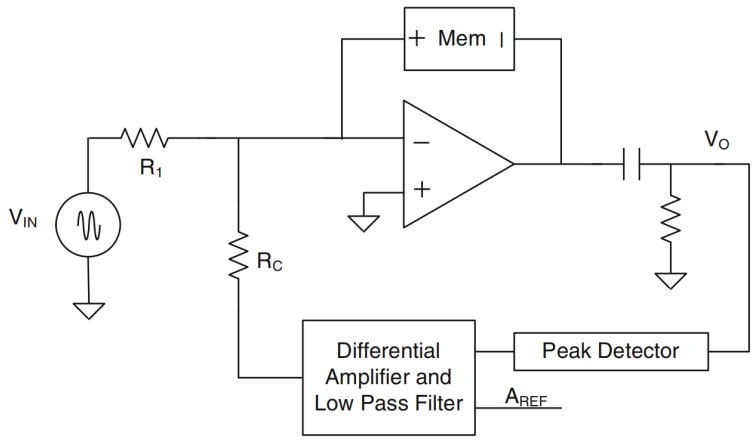


Figure 2.9: A memristor-controlled AGC architecture [7]. A memristor is applied to control the gain of the amplifier.

Figure 2.9 shows an automatic gain control(AGC) circuit based on a memristor-controlled variable gain amplifier(VGA). The memristor takes the place of a resistor in Figure 2.9 to make the gain of the circuit controllable [69]. After that, a peak detector, differential amplifier with a low pass filter, and a feedback resistor form a feedback circuit, to maintain the memristor

resistance at a specific value [7]. The working frequency range of this AGC circuit is only single-digit kHz. This is because the circuit is designed for working in baseband, hence there is no need to consider the condition when it works with high-frequency signal, and the memristor is only been considered as a resistor instead of the combination of resistor and capacitor.

When designing circuits for high-frequency applications, it is necessary to consider the effect of the parasitic capacitance in the memristor. The memristor should be seen as a resistor-capacitor parallel element as Figure 2.6 rather than only a tuneable resistor.

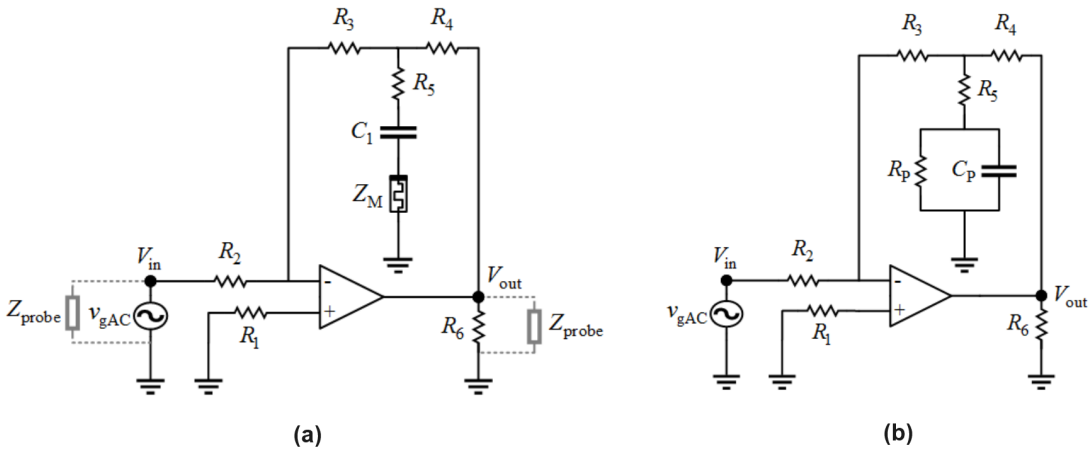


Figure 2.10: (a) An inverting amplifier based on a memristor. (b) The same inverting amplifier which is based on resistor R_p and capacitor C_p [8].

Figure 2.10 (a) shows a gain variable inverting amplifier based on a memristor, and Figure 2.10 (b) replacing the memristor and capacitor C1 with RC element, which has the same lumped element structure as the memristor [8]. The capacitor C1 in Figure 2.10 (a) is used to minimize the effect of input biasing current to the memristor, which has a capacitance value that does not affect the desired working frequency range. Because of that, ideally, as capacitor C1 does not affect the output function in the desired frequency range, the resistors R1 to R6 in Figure 2.10 (a) and (b) have the same values, and resistor R_p combines with capacitor C_p form a simplified memristor model, the two schematics in Figure 2.10 have the same function. Frequency simulation results show that the frequency responses of the two circuits are similar, and both of them can work up to 200kHz. This frequency range result expands compared with the analogue circuit in Figure 2.9. The frequency range in Figure 2.10 is limited by the circuit schematic and analogue op-amp. The op-amp used in the original article has a bandwidth of 10MHz. To expand the frequency range further, a special op-amp and circuit schematic designed for high-frequency applications are necessary.

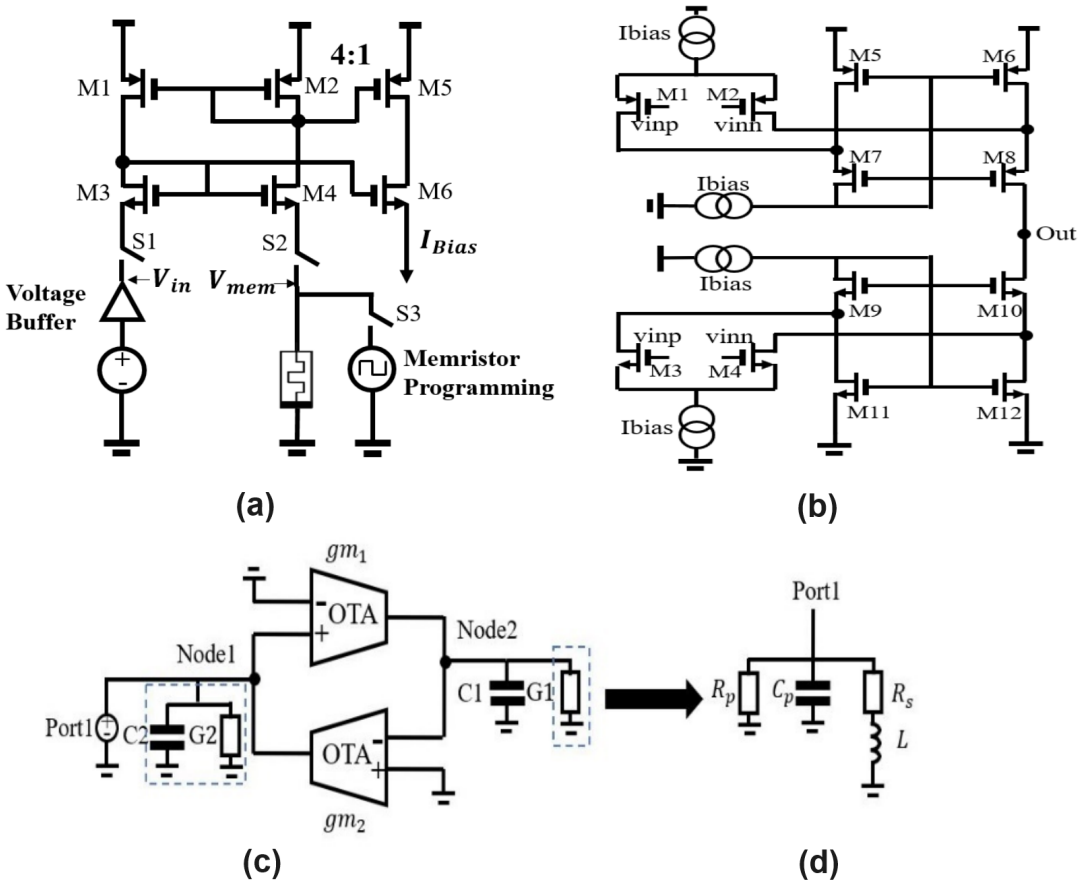


Figure 2.11: (a) A memristor-based tuneable current generator. (b) A current-controlled OTA. (c) The tuneable gyrator-C active inductor. (d) The equivalent circuit of (c) see from port 1. [9]

When using an analogue memristor in high-frequency applications, the frequency range will always be limited by the memristor, as shown in Figure 2.6. To avoid this problem, one of the solutions is setting the memristor at a position where a high-frequency signal does not flow through. Figure 2.11 shows a tuneable gyrator-C active inductor circuit controlled by a memristor [9]. In Figure 2.11 (a), M1 to M4 form a current mirror structure, which makes the M1/M3 branch and M2/M4 branch have the same current and makes the voltage of the memristor V_{mem} follow the value of V_{in} given by the voltage buffer. The current in M2/M4 branch then equals to $[V_{in}/R_{memristor}]$. In this case, the output current can be tuned by changing the memristor resistance value. Figure 2.11 (b) is a rail-to-rail folded cascode operational transconductor(OTA),in which all the biasing currents Ibias are offered by the memristor-controlled current generator. The transistors M1 to M4 in Figure 2.11 (b) form the differential signal input stage, and M5 to M12 form the cascode summing circuit and subsequent stage. Ideally, the currents flow through M7 to M10 equal to Ibias, and currents flow through all the other transistors equal to half of Ibias. By making transistors M1 to M4 in the input stage work in weak-inversion region, the total output transconductance of the OTA is proportional to

the biasing current. Figure 2.11 (c) shows an active inductor in which the transconductance of OTAs can be controlled by memristor (related to Figure 2.11 (a)(b)), and Figure Figure 2.11 (d) is the equivalent circuit of (c) see from Port 1. In Figure 2.11 (c), two OTAs form a gyrator, G_2 and G_1 are two additional conductors placed at Node 1 and 2 in parallel with two capacitors C_2 and C_1. Assume the input voltage and current at Port 1 are V_{in} and I_{in}, the output voltage and current of OTA1 at Node 2 are V_{out} and I_{out}, the equations of I_{in} and I_{out} can be written as [I_{in} = sC_2V_{in} + G_2V_{in} - gm_2V_{out}] and [I_{out} = gm_1V_{in} = sC_1V_{out} + G_1V_{out}]. Based on these two equations, the impedance see from Port 1 can be written as Y=sC_2+G_2+1/(sC_1/gm_1gm_2+G_1/gm_1gm_2), and be considered as a parallel RLC network as Figure 2.11 (d), where R_p equals to [$1/G_2$], C_p equals to C_2, R_s equals to [$G_1/(gm_1gm_2)$], and L equals to [$C_1/(gm_1gm_2)$]. By using a memristor to control the current, and indirectly control the inductance of the simulated active inductor, the frequency range of the active inductor is from 30kHz to 14MHz. The benefit of this structure is, not only the gyrator-C active inductor, the memristor-based current generator can be employed in all the circuits where the biasing currents determine some of the performance values, thus the application scope of memristor is greatly expanded.

2.2.2 Radio Frequency Application using Memristor RF Switch

In high-frequency applications, the memristive RF switch has been used in many devices. Based on the measurement results from [54], the ON state resistance of the memristor RF switch has usually been chosen as about 3Ω, and the OFF state capacitance is 1.4fF. The OFF state resistance of the memristor RF switch is very large, which is about 1TΩ, hence in the OFF state only the OFF capacitance is considered, and the resistance path is seen as cut off.

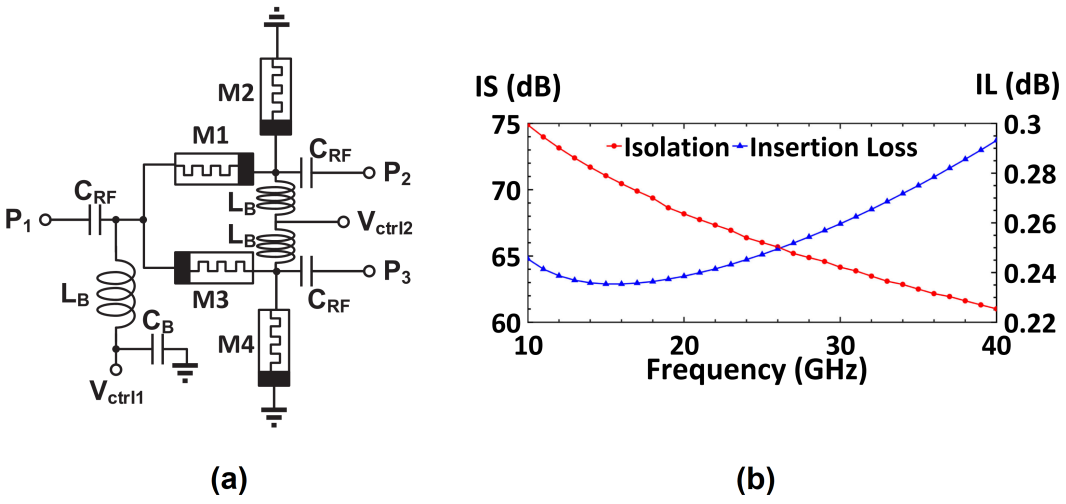


Figure 2.12: (a) The schematic of a memristor-based SPDT switch. (b) Isolation rate (IS) and insertion loss (IL) of the SPDT switch. [10]

Single-pole double-throw (SPDT) switch is one of the examples, as shown in Figure 2.12 (a) [10]. P1 is the input port, P2 and P3 are the optional output ports. V_{ctrl1} and V_{ctrl2} are the control voltages that can program the memristors. In the programming of memristor RF switches, when V_{ctrl1} = ±3V, V_{ctrl2} connects to ground, memristor M1 and M3 will be turned ON or OFF, which depend on the positive or negative voltage in the V_{ctrl1} port; When V_{ctrl1} = V_{ctrl2} = ±3V, M1 and M3 maintain their state, M2 and M4 will be turned ON or OFF. Based on the memristor directions shown in Figure 2.12 (a), the ON/OFF states of M1 and M3 are always opposite, and the ON/OFF states of M2 and M4 are also opposite. In the work of the SPDT switch, when memristor M1 and M4 turn on, M2 and M3 turn off, signal input from P1 and output from P2. Here M4 turns on to make P3 have good isolation performance. When switches M2 and M3 turn on, M1 and M4 turn off, the signal output from P3. Figure 2.12 (b) shows the signal attenuation with frequency at the output port and the isolation port. It can be seen that the SPDT switch isolates the signal in one port and has low signal attenuation in another pass port, in a very large range of frequency (10GHz to 40GHz).

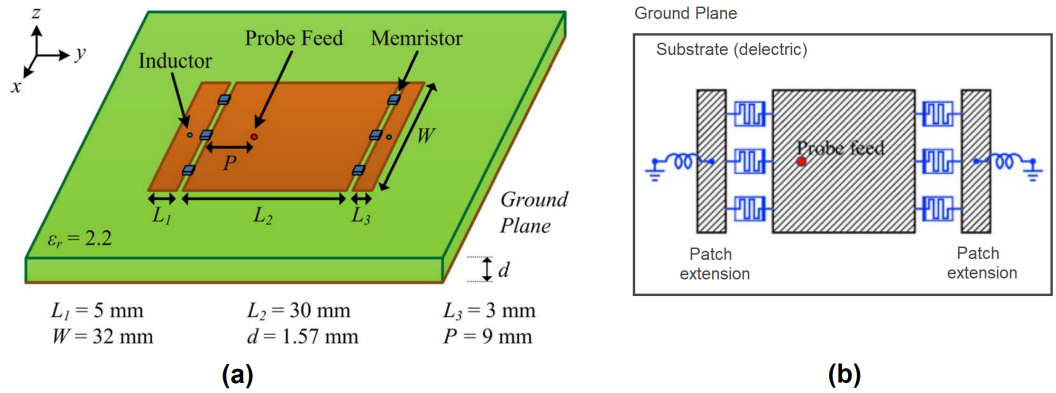


Figure 2.13: (a) A 3D model of memristor-based band-switching reconfigurable antenna [11]. (b) A circuit element schematic of this memristor-based band-switching antenna [12].

An important memristive switch application is to turn on/off a part of the circuit, hence controlling the characters of the circuit and making an RF device reconfigurable. Figure 2.13 shows a band-switching patch antenna structure [11] [12]. The operation frequency of this patch filter can switch between 2.308GHz and 3.143GHz. The band-switching filter has one main patch and two separate patches connect with the main patch by 6 memristors. When the memristors are turned off, this patch antenna can only use the main metal patch for signal receiving. When the memristors turn on, two additional patches connect to the main patch and the resonant frequency of the antenna becomes lower.

Many other reconfigurable RF devices are designed based on this idea. Figure 2.14 (a) shows the 3D model of a tuneable inductor controlled by a memristor RF switch, and Figure 2.14 (b) is a dual-band low noise amplifier(LNA) whose bandwidth controlled by the tuneable inductor [13]. Different from the tuneable active inductor in Figure 2.11, this tuneable inductor applies

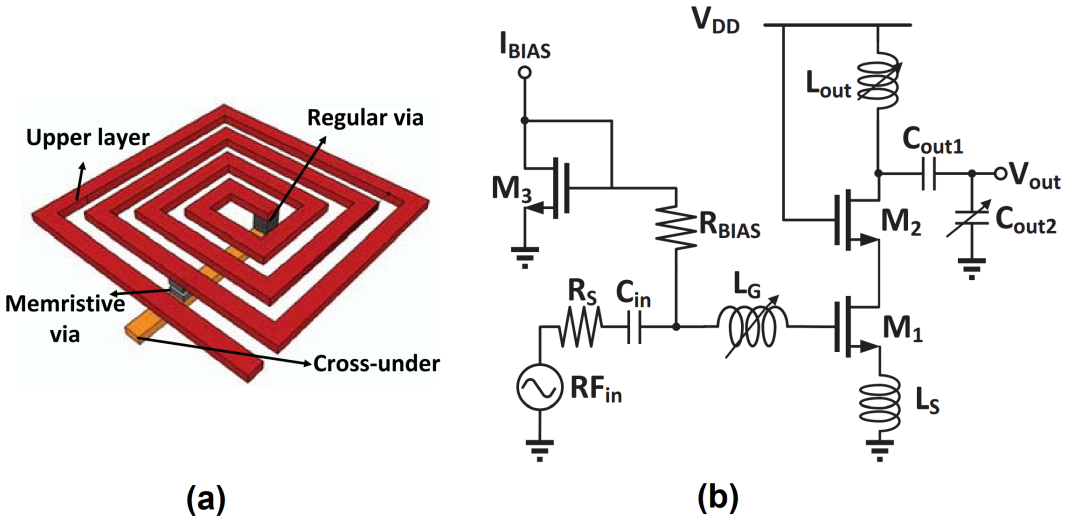


Figure 2.14: (a) 3D model of a tuneable inductor controlled by a memristor RF switch. (b) A dual-band LNA with a tuneable bandwidth controlled by the memristor-based tuneable inductors. [13].

a memristor RF switch in the spiral inductor and adjusts the inductance value by changing the length of the spiral. When the memristor switch turns off, the signal from the upper layer flows to the lower layer from the regular via; When the memristor turns on, the upper layer signal can flow to the lower layer through the memritor with less number of spiral routes, and hence the inductance in this case is smaller than the original inductor. In the cascode common source LNA circuit of Figure 2.14 (b), transistor M1, inductor L_s and inductor L_g form the main LNA structure and decide the LNA input impedance, transistor M2 is in cascode with M1 to reduce the Miller effect of drain-source capacitance in M1 and improve the stability of the LNA, transistor M3 and resistor R_bias offer the DC voltage bias to the LNA. Memristor-controlled inductor structures are used in both L_G and L_{out}. Inductor L_G resonates with the gate-source capacitance of M1; Similarly, inductor L_{out} resonates with the output capacitor group [C_{out1}+C_{out2}] and drain-source capacitance of M2, affects the LNA output impedance. When the values of L_G and L_{out} vary at the same time, the resonating frequency of this circuit changes, hence the LNA can work at different frequencies. As a result, by switching the value of memristor-controlled inductors L_G and L_{out}, this LNA can switch the operation frequency between 2.4GHz and 5GHz.

Figure 2.15 (a) shows a dual-band reconfigurable bandpass filter [14]. When the memristor is off, both the low-frequency bandpass filter (operation frequency 2.44GHz) and high-frequency bandpass filter (operation frequency 5.3GHz) work, hence the system is a filter with two pass bands. When the memristor turns on, the high-frequency bandpass filter is turned off and the device becomes a low-band bandpass filter. Figure 2.15 (b) shows the layout of this dual-band filter. The basic filter structure is a fifth-order Chebyshev interdigital bandpass filter,

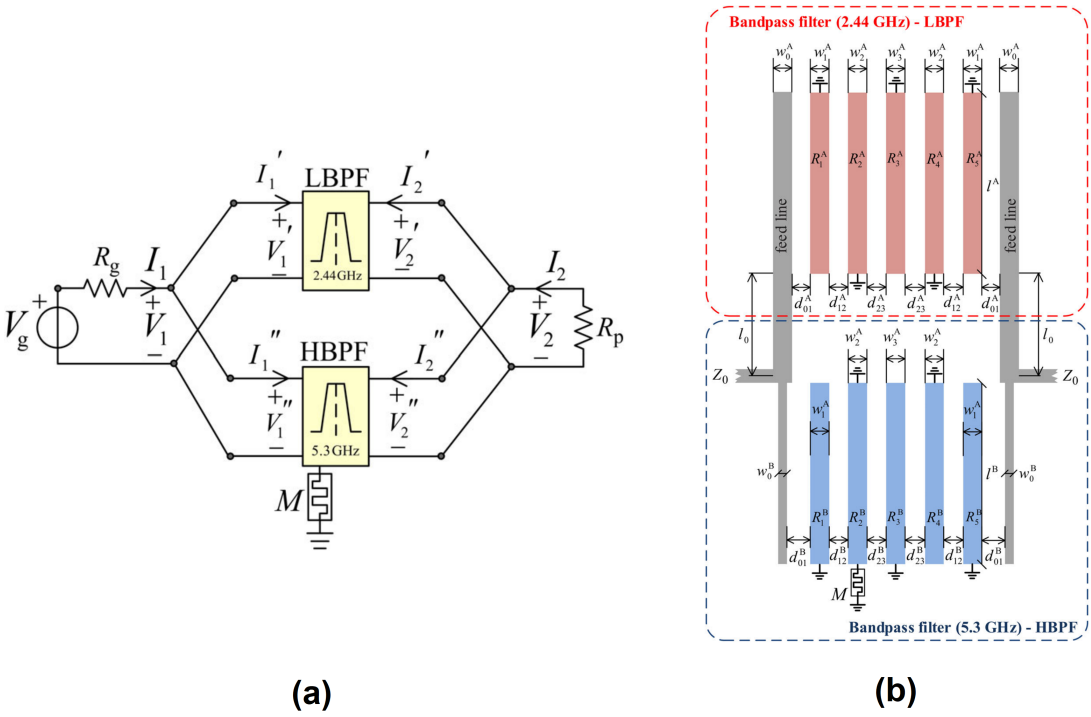


Figure 2.15: (a) The concept of memristor-based dual-band bandpass filter. (b) The layout of the dual-band bandpass filter. [14]

which includes 5 resonators (R1 to R5) in between the input and output ports (Z0 ports). The memristor connects to the open end of the R2 resonator in the high-frequency bandpass filter. When the memristor turns off, the R2 resonator is a quarter-wavelength resonator as all the other resonators, and the function of the filter is not change; When the memristor turns on, the R2 resonator becomes an eighth-wavelength resonator, which suppresses the signal flows through the high-frequency filter, and the dual-band filter becomes a single-band filter.

Figure 2.16 (a) shows the 3D model of a reconfigurable phase shifter controlled by memristor RF switches, and (b) shows the circuit schematic of that phase shifter [15]. Phase shifters are widely used in RF communication systems, especially in designing phase array antennas. This phase shifter is modified from the basic main-line mounted type phase shifter structure, which includes a main transmission line, two stub susceptance loads, and two PIN diodes in between the main line and stub loads. The memristor RF switches are used to take place of PIN diodes in the original circuit. By switching the ON / OFF stages of memristors, the electrical length of the stub loads is going to be changed, hence the phase shift of the circuit can be controlled. In the simulation, the memristor-based reconfigurable phase shifter can work in a frequency range from 5GHz to 5.6GHz and reduces the power consumption compared with the original phase shifter which uses PIN diodes as switches.

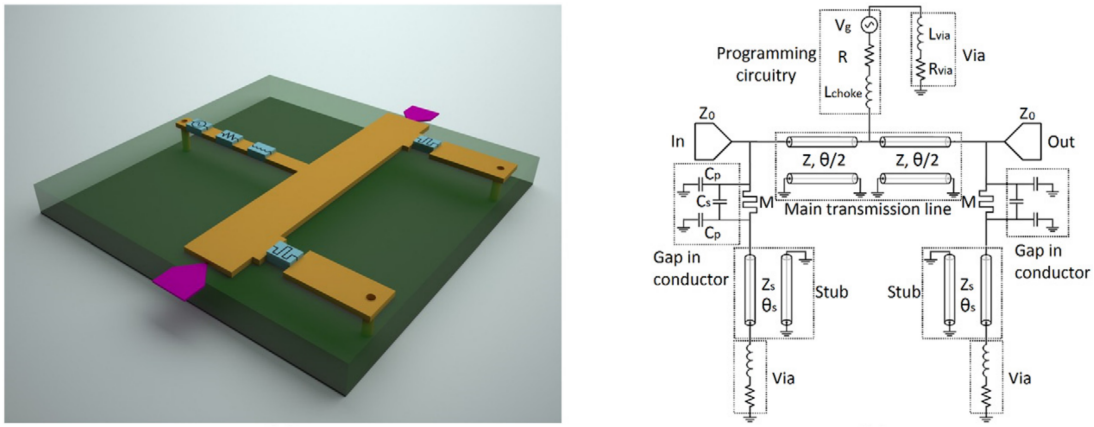


Figure 2.16: (a) 3D model of a memritor-based phase shifter. (b) Equivalent electrical schematic of this phase shifter. [15]

2.2.3 Radio Frequency Application using Analogue Memristor

In the articles about RF applications of memristors, many of them also use analogue memristors which can change resistance level continuously instead of using memristor RF switches. However, in many of these articles, the function of the memristor is only been considered as a tuneable resistor.

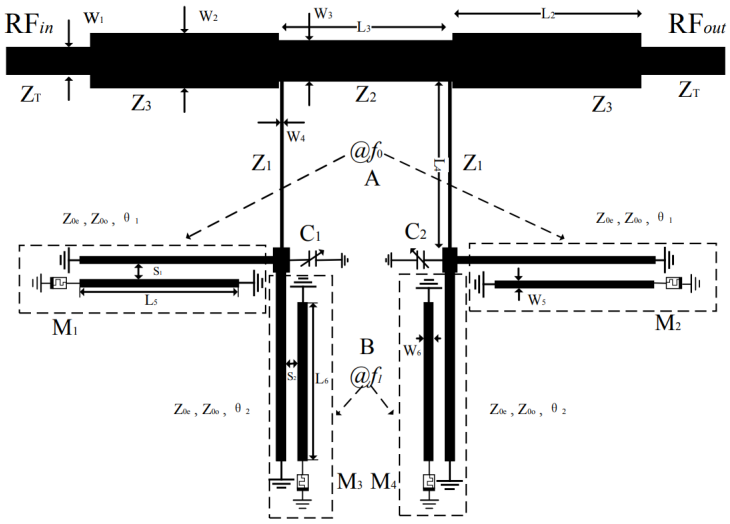


Figure 2.17: A memristor-based tuneable negative group delay filter [16]. Memristors are added to the isolation ports of the short-circuited resonators of the filter, to change the negative group delay value.

Figure 2.17 shows a tuneable negative group delay filter (NGDF) based on memristors [16]. The main structure of this filter includes branch lines and short-circuited coupling lines. Four memristors are connected to the isolation ports of the short-circuited resonators. By changing the memristor resistance, the input admittance of the short-circuit couple lines can be changed, hence the negative group delay time can also be adjusted. In the simulation results of the article, this NGDF has a stop band at 1.92GHz which offers different negative group delay. However, as the memristors are only seen as resistive elements in this article, the parasitic capacitance of the memristor is not included in the analysis, which may make the performance in practice completely different to what is expected from the theory work.

Figure 2.18 is a pulse generator that uses memristors to adjust the output delay time. The pulse generator works in an On-Off Keying(OOK) ultra-wideband (UWB) transmitter [17]. This pulse generator includes a pulsed oscillator, memristors, a programming circuit of memristors, and a pulse-shaping filter. In pulse generator working mode, MN1 to MN3 turn on and MN5 to MN7 turn off. On the other hand, when the pulse generator is in memristor programming mode, MN1 to MN3 turn off and MN5 to MN7 turn on. In the pulsed oscillator, MP1 to MP3 open and close alternately to generate the negative and positive cycle of the pulse. Assume at the start point MP1 starts to turn off, the voltage at Note A (gate of MP2) is going to reduce,

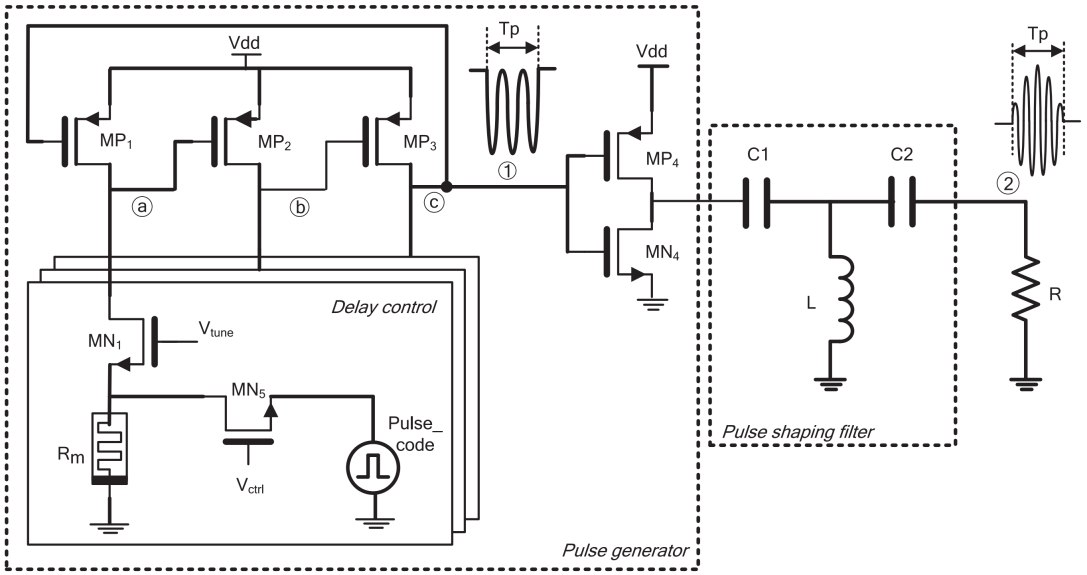


Figure 2.18: A memristor-based tuneable pulse generator [17]. Memristors are applied to change the output delay time of the pulse generator.

the input capacitance of the second stage(mainly the gate-source capacitance of MP2) will discharge through MN1 and R_m. The time that second-stage input capacitor C_2 needed to reduce its voltage to half of Vdd equals to 0.69*RC, which is τ_1=0.69*(RN_{on1}+Rm_1)*C_2, where RN_{on1} and Rm_1 are the resistance of the first stage ON-state NMOS and memristor. Once the voltage on the gate of MP2 reduces to smaller than half of Vdd, MP2 starts to open, and charge the third stage input capacitor(gate-source capacitance of MP3). The time that needed to charge the third stage input capacitor C_3 up to half of Vdd is τ_2=0.69*RP_{on2}*C_3, where RP_{on2} is the ON resistance of MP2. Finally, similar to the first stage, when the voltage on the gate of MP3 increases higher than half of Vdd, MP3 starts to turns off and make the input capacitor of the first stage C_1 discharge, with discharging time τ_3=0.69*(RN_{on3}+Rm_3)*C_1, where RN_{on3} and Rm_3 are the resistance of the third stage ON-state NMOS and memristor. When the voltage at Node 3 reduces to half of Vdd, one negative cycle of the pulse outputs to the pulse shaping filter, which means negative cycle delay τ_N=τ_1+τ_2+τ_3. For positive cycle, the operations are similar. As the positive/negative cycle of the pulse decided by the charging/discharging time of each stage, the frequency of the pulse is thus controlled by the resistance of memristors. The memristor model been used in this circuit has a tuneable resistance range of [60, 214]Ω. The simulation results show the final transmitter can work in a frequency range from 3GHz to 5GHz. In this article, the model been used to simulate memristor is Voltage ThrEshold Adaptive Memristor (VTEAM) model [70]. VTEAM is a general, simple, flexible and accurate model for describing the function of voltage-controlled memristors. It simulates the current-voltage characteristics of memristors based on a threshold voltage, where the resistance of memristors do not change for voltage under this threshold. As the I-V curve offered by

VTEAM model can match most of the voltage-threshold memristors, this model is widely used in the simulation of analogue memristors. As the parasitic capacitance of a memristor can be included in the input capacitance of this stage, this pulse generator, to some extent, takes into account the parasitic capacitance of the memristor and leverages it in the overall design. However, as VTEAM model simulates memristors as purely resistive elements, the parasitic capacitance of memritors are not calculated in the input capacitance of each stage, hence the frequency of the output pulse with practical memristive devices will different from the simulation results. Because of that, it cannot be guaranteed that this pulse generator will also function in practical applications.

The technologies of memristor designing and fabrication are still in development, and different types of memristor can offer varied performance. The RF circuits designed with analogue memristors may also find suitable types of memristors, hence these designs are valuable for reconfigurable RF circuit designing.

2.3 Conclusion

Memristors have the potential to be applied in reconfigurable analogue and RF circuit designs. However, because of the difficulty of using analogue memristors in high-frequency circuit designs, the analogue memristor applications and RF memristor applications are nearly separate. The main problem in the high-frequency applications of memristors is the limited high resistance range and low cut-off frequency of the multiple resistance levels memristor. However, it is still feasible to design analogue circuits which have a frequency range close to the cut-off frequency of the memristor to get possible high-frequency reconfigurable devices, or use some methods to avoid the limitation of the memristor frequency range.

In this thesis, the applications of multi-stage analogue memristors in different frequency levels are attempted. In Chapter 3, a reconfigurable memristor-based instrumentation amplifier whose gain value can be adjusted by the memristor is discussed. This reconfigurable amplifier was measured with a memristor package in the laboratory and can work at frequencies lower than 450KHz. In Chapter 4, a memristor-based reconfigurable delay circuit is designed. Memristors are used in tuneable DC voltage sources, to control the output delay time of delay elements indirectly. The whole delay circuit is designed as a chip, includes a 10MHz delay part, a 1.6GHz delay part, a memristor programming controller, input signal generators, and output buffers. To measure the chip, a PCB board is designed, and the operations of the chip measurement progress with the PCB are also discussed in Chapter 4. Chapter 5 discussed the possibility of combining memristors with N-path filter structures. Different memristor-based N-path filter structures are compared. One memristor-based reconfigurable 4-path filter was measured with a memristor package in the laboratory and can work at 1MHz. The memristor-based N-path filter which can work at 1GHz is also simulated. Finally, Chapter 6 concludes the research in this thesis, and also includes the further plan of my study.

Chapter 3

Memristor-based Reconfigurable Instrumentation Amplifier

3.1 Introduction

Memristors are two-terminal non-volatile passive circuit elements, whose resistance depends on the history of current or voltage applied on them [19]. Their low power operation, small size, ability to store multi-bit information [71] and other characteristics such as their simple, two terminal structure [2] make them good tools for implementing reconfigurability on-chip. However, the characteristics of memristors need to be carefully considered when designing circuits and systems. Typical areas that require attention include avoiding potentially catastrophic overvoltages and the memristors' typically non-linear current-voltage curves that cause static resistance to vary resistance with bias voltage [64]. Comparing with circuits that apply varying voltage on memristors, circuits which apply fixed biasing voltage on memristors can maintain the resistance of memristors stable, and reduce the influence of non-linear I-V characteristics of memristors. Moreover, fundamentally metal-oxide-metal stack memristors act as metal-insulator-metal (MIM) capacitors, potentially adding substantial parasitic capacitance and affecting high-frequency operation. A more complete model of the memristor is thus a resistor in parallel with a capacitor [54], as shown in Figure 3.1 (a), where the value of the parasitic capacitance is mainly decided by the material, structure, and size of the memristor [5].

In this chapter, TiO_x/Al_2O_3 memristor devices are introduced within an instrumentation amplifier to add reconfigurability and test the actual behavior of memristors. The memristive devices replace some of the gain setting resistors (see Equation 3.1) to render gain a tuneable parameter. Previous attempts included using CMOS structures to replace the gain resistor Rg from Figure 3.1 (b), rendering gain tuneable via a tuning signal [72], [73], or controlling the gain with currents as per the current-mode instrumentation amplifier structure [74]. The circuit was implemented on a breadboard, memristor array was set in a package and programmed by a measurement instrument Arc Two. The gain and frequency response of the amplifier with varying memristor resistance levels was measured, to test the performance of the memristor as a tuneable resistor and the effect of parasitic capacitor. The CMRR and THD+N of the circuit with gain resistor and memristor at the same value were also measured, to research

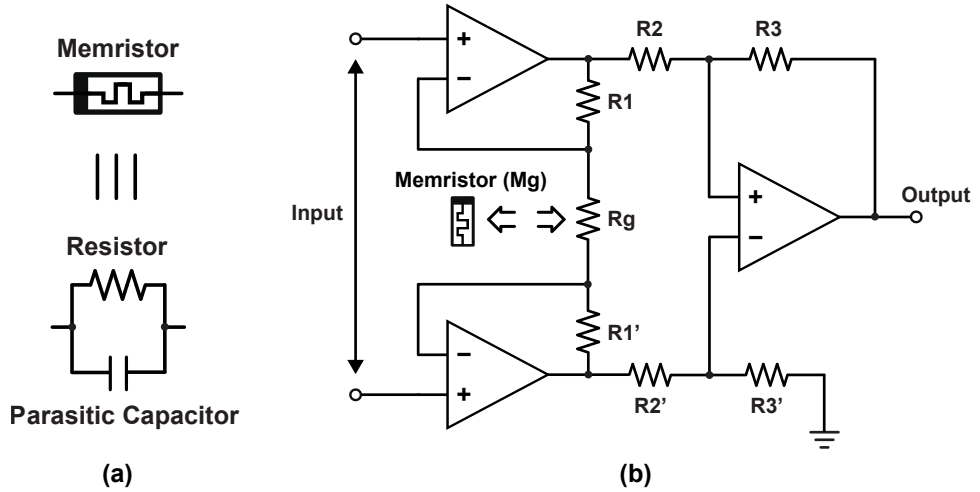


Figure 3.1: (a) Lumped element model of memristor. (b) Memristor-based instrumentation amplifier. Ratio between R_1 and R_g decides the gain of the circuit. A memristor is used to replace the gain resistor, to control the gain of the amplifier. [18]

the effect that memristor gives to the signal. We discovered that the parasitic capacitance of the memristor affects the gain bandwidth of the instrumentation amplifier, but does not have much influence in CMRR characters. The non-linear current-voltage (I-V) function of the memristor strongly increases the THD+N value, but measurement also shows that applying multiple memristors in the amplifier can relieve the increase of signal harmonic distortion.

3.2 Design and Methodology

3.2.1 Design of Reconfigurable Instrumentation Amplifier

An instrumentation amplifier is a type of differential amplifier which have relatively large signal gain with high input impedance, low output impedance and good common mode rejection ratio [75] [76]. The typical structure of an instrumentation amplifier contains 3 Op-Amps, 2 for the input stage and 1 for the output stage, as shown in Figure 3.1 (b). The input stage of the instrumentation includes 2 resistors R_1&R_1', gain resistor R_g and the two input Op-Amps as buffers. At the right-hand side, resistors R_2&R_2', R_3&R_3' and an output Op-Amp form a regular differential amplifier that works as the output stage [77]. Ideally, the input stage focuses on amplifying the input signal, and the function of the output stage is to remove the common mode with a gain of 1 [76]. In the circuit structure, R_x and R_x' have the same resistance, where x is the number 1 to 3. In the input stage, the negative feedback of two Op-amps cause the upper and below point of the gain resistor equals to the voltages at the input ports of Op-

amps, and generate a current with value [V_{in}/R_g] flows through R_1, R_g and R_1'. As R_1=R_1', the voltage difference between the input of R_2 and R_2' becomes [V_{in}(1+2R_1/R_g)]. By multiplying this voltage with the gain of the output stage differential amplifier [R_3/R_2], the instrumentation amplifier output voltage gain can be shown as:

$$A_v = \frac{V_{out}}{V_{in}} = (1 + \frac{2R_1}{R_g}) \times \frac{R_3}{R_2} = 1 + \frac{2R}{R_g} (when R_1 = R_2 = R_3 = R) \tag{3.1}$$

Where the input signal Vin is the voltage difference between input voltage ports of the input stage Op-Amps. When setting all the resistors R_1 to R_3 equal to a resistance R, the gain of this instrumentation amplifier can be defined by R and R_g, which is shown in Equation 3.1.

Equation 3.1 shows that the gain of the instrumentation amplifier can be adjusted by changing the ratio between resistance value R and gain resistor R_g. This means that the instrumentation amplifier can be reformed and become a tuneable gain amplifier by making the gain resistor controllable. Large amounts of modified tuneable circuits have been designed based on instrumentation amplifiers. For example, switching from different gain resistors with varying resistance values to make the gain adjustable, using CMOS structures to replace the gain resistor and change its resistance by another voltage or current signal [72] [73], or controlling the gain with currents based on current-mode instrumentation amplifier structure [74]. With an adjustable resistance level controlled by the history of voltage on the device, the memristor is one of the possible electronic elements which can be used in the designs of tuneable amplifiers. Research has been done in using memristors with instrumentation amplifiers. One of the directions is to use a memristor in the Op-Amps of the instrumentation amplifier to improve some of the performance, like expanding the operational gain range, reducing the on-chip area and power consumption [75]. Another direction is replacing the gain resistor with a memristor, using voltage signals to control the resistance of the memristor and hence control the gain of the amplifier [78]. In this chapter, the second direction, which replacing the gain resistor with a memristor, was tested in the lab. An instrumentation amplifier was built on the breadboard, and a memristor package was connected to the circuit as a gain resistor, with an external instrument for the adjustment of the memristor value. The basic instrumentation amplifier structure which has 3 Op-amps and 7 resistors were chosen for designing the memristor-based amplifier circuit in this chapter, because the gain of the basic instrumentation amplifier is set by R_g, make it straightforward to control the gain by adjusting the resistance of memristors. Besides, the basic instrumentation amplifier structure is inherently simple and robust, makes it easy to integrate with memristor packages in the laboratory. Due to the limited measurement results of memristor-controlled reconfigurable devices, starting with a structure with less complexity to test the memristor-controlled circuit is a more prudent approach.

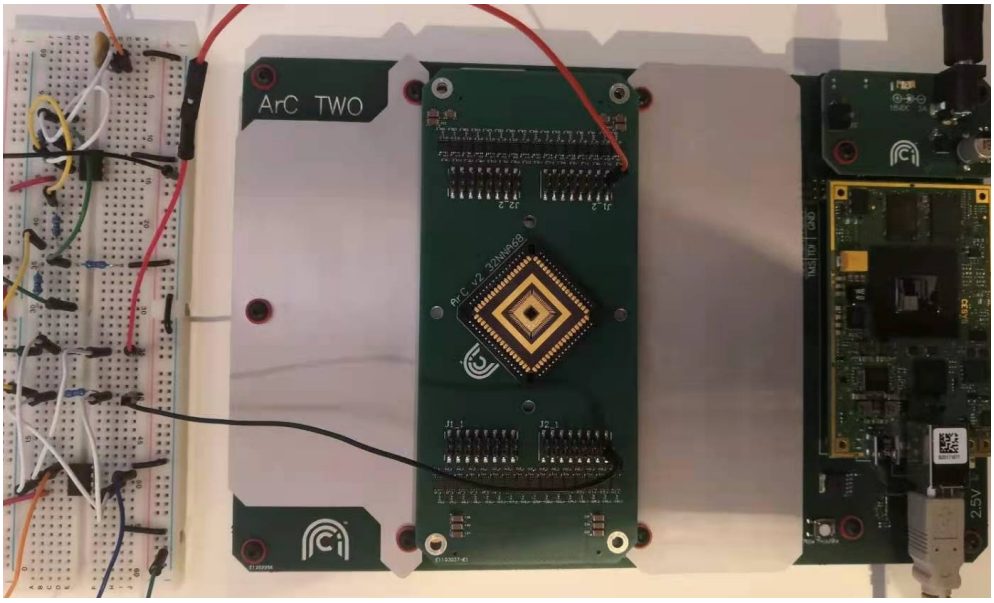


Figure 3.2: The instrumentation amplifier on breadboard(left), and memristor package on ArCTwo(right). In practical operations, the memristor package is placed on a break-board when connecting with the instrumentation amplifier for normal work, and integrated on the ArC Two only in the programming of the memristor.

3.2.2 Construction of the Experimental Circuit

Figure 3.2 shows the hardware of the circuit and memristor control instrument in the laboratory, in which the circuit on the left-hand side breadboard is the instrumentation amplifier, and the instrument on the right-hand side is the memristor control instrument, with memristor board on it.

The memristors used here are TiO_x/Al_2O_3 bi-layer devices [24], with electrode area $10\times10\mu m^2$ and active layer (the material between the electrodes) thickness of 4nm. Multiple memristors are used in the measurement, whose resistances are in the total range of [10, 100]kΩ, and each of them can change their resistances in the range of about ±10kΩ. Based on [5], the cut-off frequency for TiO_x/Al_2O_3 memristor with resistance range from 10kΩ to 100kΩ is in the range of 0.1-1MHz. To ensure that the main gain roll-off effect does not arise from the OpAmps' characteristics we used TLV2372 OpAmps with a gain bandwidth product of 3MHz (typ. open-loop voltage gain 110dB). According to equation 3.1, when chosing R_g value between [0.5, 1] times of R_1, the close loop gain of the circuit is 3 to 5, thus in this case the bandwidth of the circuit is around f=GBW/A_v=[600k, 1M]Hz.The entire circuit was prototyped on a breadboard under a power supply of 5V. The constant DC biasing voltage is generated by a DC voltage source, and the signal is sent by a signal generator. To calculate the power dissipation, the current from the DC voltage source is measured by a current meter.

3.2.3 Operation of the Memristor Package

External instruments “ArC One” and “ArC Two” (ArC instruments, UK) are used to program the memristor [79]. These fundamentally act as source-meter units co-integrated with a routing network with ArC One operating in pseudo-parallel and ArC Two in true-parallel mode [80]. Importantly, ArC Two is used as follows: Initially, the memristive package is connected to the internal electronics of ArC Two, which allows us to adjust the test memristors to a specific resistance level, and measure their I-V curves. Once at an appropriate and known level, the instrument passes control of the device to the breadboard-based instrumentation amplifier. On-board RC filters ensure that charge injection effects that have been previously found to alter the state of memristive devices during such switchovers are sufficiently mitigated. Then the main experiments are carried out and finally, the devices are switched back to internal ArC Two control to check that the “before” and “after experiment” I-V curves do not show significant alteration. Memristive devices were converged to the desired states using automated algorithms similar in spirit to [61] that seek to change resistance states gently, protecting the memristor devices and slowing down ageing. As the programming of the memristor is set to have a tolerance, the memristor resistance values can have 1kΩ to 3kΩ error compared with the desired values. Finally, for the memristors used in this project it was confirmed that the device can maintain a stable resistance level (no resistive switching present) for biasing voltages below ±1.2V (checked by applying multiple pulses of length 100ms at said voltage), we can loosely define as the switching threshold of the device. Hence the pulse voltages chosen to program the memristors are in the [0.6, 2]V range. The 2V upper limit is set to prevent overvoltage-induced memristor failure. As OpAmps are in follower configuration, the voltage across the position Rg is a smoothed version of the input voltage. Hence the memristor is biased invasively, there is no obvious mechanism by which accidental programming can occur.

3.3 Measurement Results

3.3.1 Frequency Responses of Memristors in the Measurement

The impedance curves of the memristors at different frequencies with varying original resistance levels are plotted in Figure 3.3. The data is collected by sending small voltage signals with different frequencies to memristor elements, then measuring current signals flow through memristors, and finally calculating the resistance based on the voltage and current values. The trend of the memristor impedance curves in Figure 3.3 is similar to the memristor impedance-frequency response in Figure 2.7 of Chapter 2. Reference to Figure 3.1 (a), as the memristor has a parasitic capacitance, the impedance-frequency curve of the memristor looks like a "low pass" curve. As the time constant of a memristor is decided by its resistance and parasitic capacitance, the higher the original resistance at low frequency, the lower the

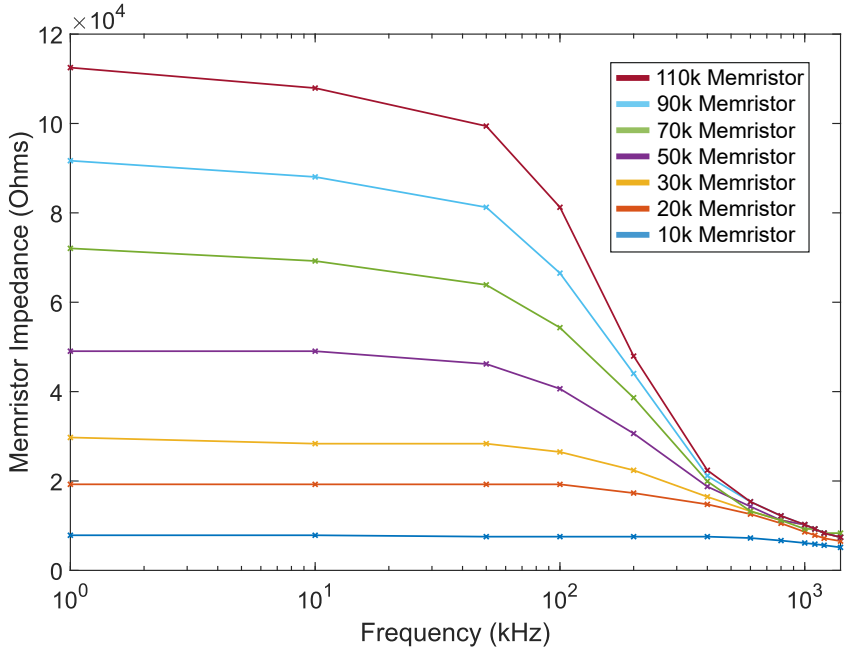


Figure 3.3: The impedance-frequency curves of memristor with different original resistances [18]. For memristor values higher than 20kΩ, the memristor impedance values start to reduce when the signal frequency closes to 100kHz.

"cut-off frequency" of the impedance. It is found from Figure 3.3 that at 100kHz frequency, the memristor resistance variation range [10k, 110k]Ω has reduced to [10k, 85k]Ω. Compared with the memristor impedance curves in Figure 2.7 of Chapter 2, it can be observed that the impedance curves in Figure 3.3 start to reduce at lower frequencies, which shows the memristors being used in this research project have larger parasitic capacitance than the memristors used in the measurement of Figure 2.7.

The memristor impedance curves are measured from several memristors with different resistance ranges. The memristor package used in this research has memristors with a minimum resistance level lower than 10kΩ and a maximum resistance level higher than several hundred kΩ. The memristors in this package have tuneable resistance ranges higher than 10kΩ but smaller than 50kΩ. In the measurement of the instrumentation amplifier with resistors, the instrumentation amplifier can work with a maximum gain resistance range of [10, 100]kΩ, and has the best performance with gain resistor range [30, 70]kΩ. However, there is no suitable memristor that is set at this resistance level and has this tuneable resistance range. Because of that, two memristors that have resistance ranges [30, 50]kΩ and [45, 70]kΩ are chosen to combine with the instrumentation amplifier in this research. Using multiple memristors in the measurement expands the tuneable resistance range, and hence the project can get more measurement data.

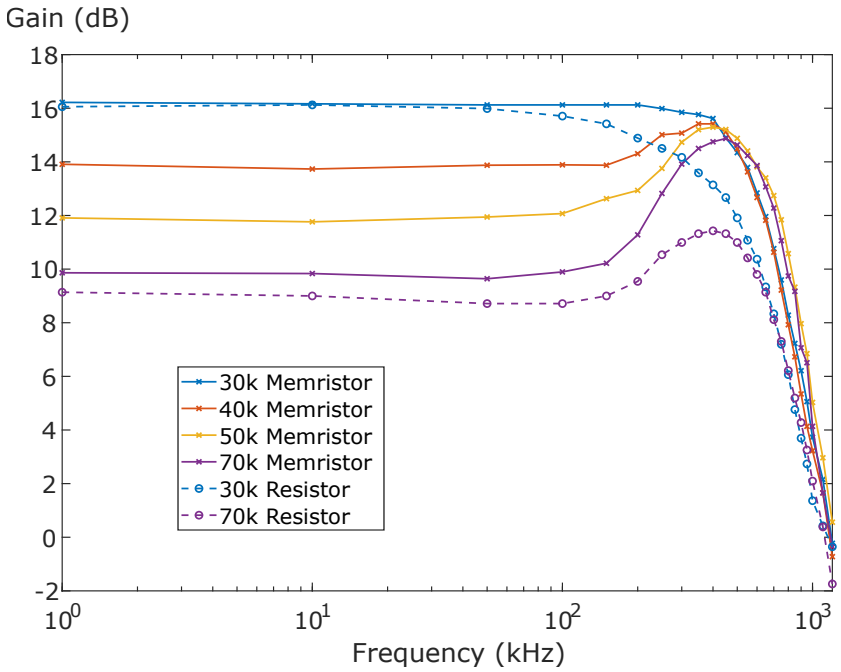


Figure 3.4: Gain-frequency response of the instrumentation amplifier with different memristor values. The results of the circuit with 30kΩ and 70kΩ resistors are also included for comparison. [18]

3.3.2 Memristor-based Instrumentation Amplifier Measurement Results

Based on Equation 3.1, when all the resistors R1 to R3 are set with resistance 75kΩ, and the memristor-defined Rg ranges in [30, 70]kΩ, the gain of the instrumentation amplifier varies in [9.95, 15.56]dB. The gain response of the instrumentation amplifier for different values of Rg is shown in Figure 3.4. Measurement with Rg implemented by a discrete resistor at 30kΩ and 70kΩ are also given for comparison.

It can be observed that the curves for Rg 30kΩ resistor and memristor match very well at low frequencies. The gain values of 30k & 70kΩ resistor at 1kHz is slightly smaller than the calculation results, which is because of the normal gain reduction with the increase of frequency in the circuit. It is found that the -3dB cut-off frequency of the memristor curve is slightly higher than the resistor curve, providing a slight extension to the bandwidth and a slightly cleaner transition into the roll-off region. For Rg > 40kΩ, gain increase peaking is observed at around 450kHz, and the peaking is larger than the 70kΩ resistor curve. Both these phenomena can be explained by considering that the impedance magnitude of the memristive device starts to tail off around 100kHz, affected by its parasitic capacitance as seen in Figure 3.3. The bandwidth of Op-amps TLV2372 are 3MHz, and when using 3 Op-amps together, the bandwidth of the whole circuit further reduces. As a result, observing from the curve with 30kΩ resistor in Figure 3.3, the -3dB bandwidth of the circuit is around 400kHz. On the other hand, the parasitic capacitance of the memristor make the impedance

of memristor reduces at high frequency, and hence increase the gain. The inherent reduction trend of the gain combines with the rising trend caused by the memristor parasitic capacitance, generate a gain peak at around 450kHz. Subsequently, as the upward trend in gain weakens, the gain curve continues to decline. The gain increase peaking in the 70kΩ resistor curve can also be explained by the parasitic capacitance in the through-hole resistor element used in the measurement. The difference in the 70kΩ resistor curve and memristor curve shows the parasitic capacitance in the memristor is larger than the parasitic capacitance in that resistor. This causes Rg to drop and gain to increase before the TLV Op-Amps' natural roll-off takes over. At high frequencies, when the parasitic capacitor dominates the memristor impedance, all memristors show the same low impedance value. This is a direct result of their common parallel plate geometry (same plate size and same dielectric thickness). By $\sim$1MHz, all memristors feature practically the same impedance value (within 8$\%$). This result illustrates the importance of being aware of parasitic capacitance and the role that device geometry plays in setting device characteristics. It suggests device area as an independent engineering parameter in AC applications for devices where it has been shown that device area generally does not directly affect resistive switching characteristics because the conduction mechanism is localized in a filament-like region. This is especially true of metal-oxide devices of the "electrochemical metallization" (ECM) variety [81], because in the ON-state of ECM devices the currents are carried by narrow filaments in the oxide layers and hence have very weak dependence on the device area, while the OFF-state resistance values are very large and hence will not strongly affect the switching performance. However, overall layout geometry may still indirectly affect device performance: for instance, the width of the electrodes used to access the device may introduce series resistance and dull the impact of programming pulses onto the device properly.

The common-mode rejection ratio simulation and measurement results with 30k&70kΩ resistor and memristor are plotted in Figure 3.5. Comparing the measured 30kΩ resistor and memristor results, the CMRR curves are similar, with a CMRR value of around 95dB at 1kHz. Comparing the 30kΩ and 70kΩ memristor measured CMRR curves, it is found with a larger Rg value, the CMRR value is larger at low frequency, but also reduces faster at higher frequency. The measurement CMRR curves show degradation over the simulation results with the same resistance. Simulation was done in TINA-TI, with manufacturer-provided micromodels of the TLV2372 OpAmps, ideal resistor and ideal elements based memristor lumped element model. The degradation is caused by the mismatch of the real resistor elements and three OpAmps. This result is expected since the voltage applied across the memristor remains largely unchanged regardless of common mode, hence mostly eliminating it as a source of additional error.

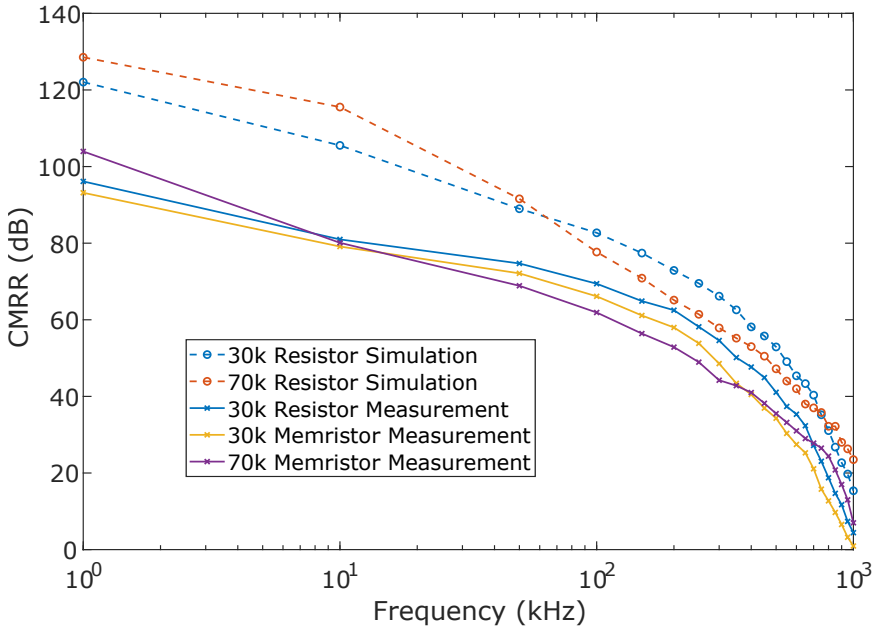


Figure 3.5: CMRR simulation and measurement results with different values of resistor and memristor. The measured CMRR values are lower than the simulation results.

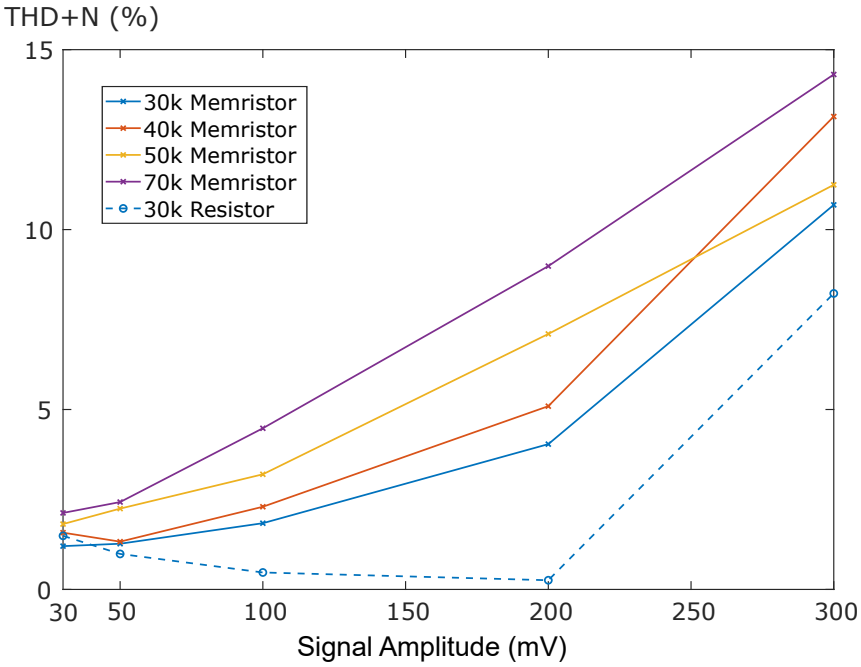


Figure 3.6: THD+N curves for different input signal amplitude and vary memristor value [18]. The results measured with memristors show larger signal distortions compared with the results measured with a resistor.

Figure 3.6 shows the total harmonic distortion plus noise (THD+N) curves of the instrumentation amplifier with different values of memristor and with Rg implemented by 30kΩ resistor at 1kHz. The THD+N values roughly increase with the increase of memristor values. However, it can be observed that the curves of memristor values 30k&40kΩ show one increasing

trend, and the curves of memristor values 50k&70kΩ have another increasing trend. This is because multiple memristors are being used in the measurement, and different memristors have different I-V curves. Different memristors can have the same resistance at a specific voltage, but their resistance will vary at other voltages if they have different I-V curves [82]. The THD+N values of the instrumentation amplifier with gain resistor and memristor at input AC amplitude 30mV are 1.1% and [1.8, 2.1]% range. These values are large compared to simulation results using the manufacturer's OpAmp model and may be caused by the electronic noise in the laboratory environment, possibly affecting probes and oscilloscope. This hypothesis seems to be corroborated by the THD+N curve of the resistor first reduces with the increasing input signal magnitude, allowing it to overpower noise-induced distortive effects, and then increases after input signal amplitude higher than 200mV. We note that at 200mV input signal, THD+N is very close to baseline (0.1%). By 300mV input signal, the amplifier starts to saturate and observed THD+N increases. By comparison, the memristor design's THD+N increases faster and nearly does not benefit from a THD+N reduction during the amplitude sweep. The higher distortion is expected given the non-linearity in the I-V function of the memristive device. What was less obvious a priori was that at a very small input signal the overall levels of THD+N are nearly high enough to hide the non-linearity in the IV of at least the particular flavour of memristive devices used in this work. We can expect that to be both a result of higher noise levels reducing the competitiveness of the resistor-based approach and perhaps more importantly the increasing "linearization" of the memristive device as we enter a truly small-signal regime. It is therefore reasonable to expect that for <10mV signal amplitudes (as may be the case for electrophysiological or other extremely fine signals) the distortion induced by memristor-based amplification may not be a limiting factor, even in systems employing hefty noise mitigation.

To test the signal distortion in the circuit with multiple memristor devices, resistors R1 and R1' are replaced by memristors, and the 3 memristors at positions Rg, R1 and R1' are set to have approximately the same value, as shown in Figure 3.7. As comparisons, results for the amplifier with one memristor are also measured, with resistors R1 and R1' having the same value as the gain memristor. Measurement results show the triple memristors amplifier has the similar Gain and CMRR as the instrumentation amplifier which has three resistors with the same value. Figure 3.8 shows the THD+N results in this condition. To research on the influence of memristor resistance to the signal distortion, in this experiment the memristors are chosen to have extreme values, which are 10kΩ and 100kΩ. The memristors used in (3 × memristors with value 10kΩ) test have accurate values [8, 10, 9]kΩ, and memristors for (3 × memristors with value 100kΩ) test have accurate values [97, 101, 95]kΩ. It can be observed that THD+N values of using 3 × memristors are smaller than using 1 memristor. As the resistance of the memristor floats with voltage changes, when there is only one memristor, the ratio between the R1 resistor and the Rg memristor changes with time, hence the signal distortion is large. However, when using memristors to take the place of R1 resistors, resistances of the

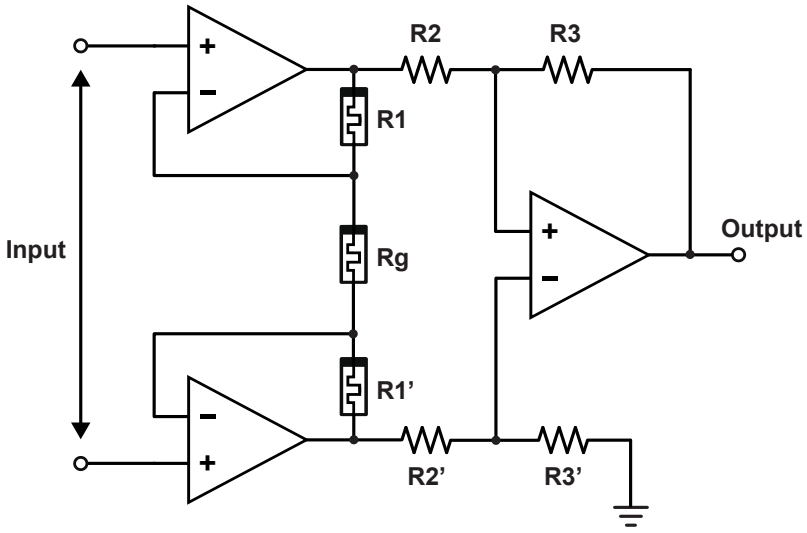


Figure 3.7: Tuneable instrumentation amplifier with 3 memristors. In theory, the three memristors will compensate the non-linear I-V characters of each other, to get a better signal distortion performance.

3 $\times$ memristors vary at the same time, the ratio between R1 and Rg changes smaller, which makes the THD+N value better. The THD+N of using 3 $\times$ 100kΩ memristors is smaller than using 3 $\times$ 10kΩ memristors. This is because in these tests R1 memristors' values have small differences, and the (difference/ required resistance) ratio is larger when the memristor value is smaller.

3.4 Discussion

Table 3.1 lists the performance characteristics of the memristor-based instrumentation amplifier and other tuneable instrumentation amplifiers in the literature. Compared with other tuneable instrumentation amplifiers, the memristor-based amplifier designed in this work has comparable base characteristics such as bandwidth, CMRR and power dissipation. Although the implementation of the circuit in this research is only integrated on a breadboard and using off-the-shelf Op-amps, it still demonstrated a critically good tuneable gain range. Besides, this circuit uses memristive devices with relatively modest ON/OFF ratio compared to other circuits that has been reported in the literature: An $\sim$ 2.63 ON/OFF ratio leads to an $\sim$ 7.5dB voltage gain ratio in the circuit of this work, whereas the literature reports memristive devices with 103 [83] or even 106 ON/OFF ratios. As for different memristive devices, the performance characteristics, including the I-V characteristics, ON-OFF ratio, parasitic capacitance, and so on, are all different. Therefore, we cannot directly compare circuits designed with different memristive devices.

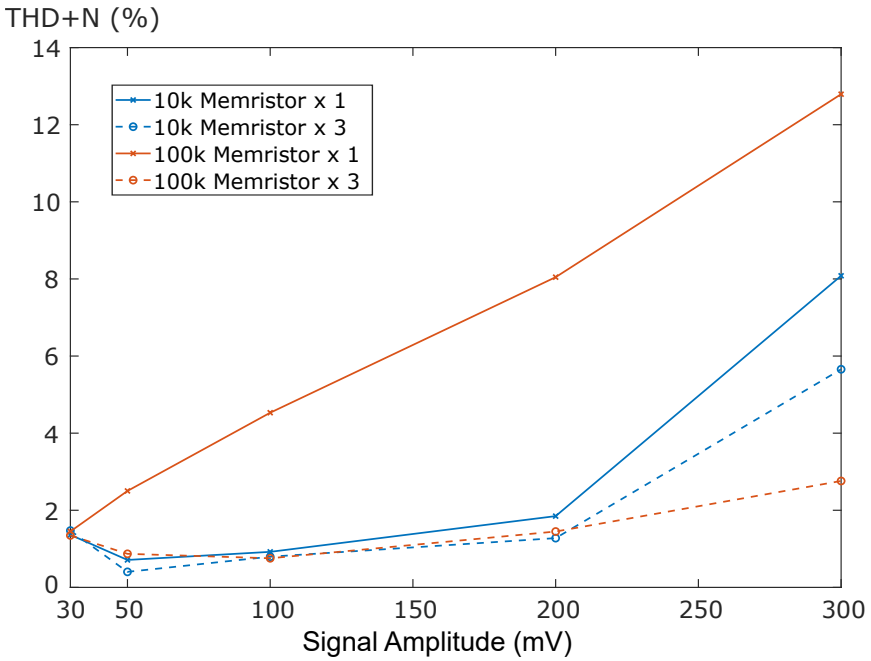


Figure 3.8: THD+N curves for instrumentation amplifier use 3 memristors compare with the results of using 1 memristor [18]. The results of using 3 memristors have lower signal distortion than the results of using 1 memristor in the instrumentation amplifier.

The current implementation of this design was on a breadboard, which means that it carries too much stray capacitance to be competitive as it stands, but with integration on chip it should be able to become competitive in the niche of "non-volatile gain control". In the Table 3.1, reference [74], [84], [85] are all volatile gain control, which need continue voltage / current apply to maintain their stages, in which case the non-volatile control is the benefit of our work.

Table 3.1: Comparison of this work and other tuneable instrumentation amplifier designs.

Ref.	This Work	[74]	[84]	[85]
Gain (dB)	9.5 $\sim$ 16	20 $\sim$ 40	13 $\sim$ 17	4.7 $\sim$ 18
Bandwidth (Hz)	450k	10k	83.75M	3 $\sim$ 14.8M
CMRR (dB)	80	44.4 - 49	96	51.2
Max to Min Gain Ratio (dB)	7.5	20	4	13.3
Power Dissipation (W)	7.33m	72 $\sim$ 385m	4.43m	864u

3.5 Conclusion

In this chapter, memristors with different resistance levels were used to take the place of the gain resistor in the instrumentation amplifier, and made the circuit become a tuneable gain instrumentation amplifier. The tuneable instrumentation amplifier was built on a breadboard and measured in the laboratory. The memristor-based reconfigurable instrumentation amplifier has tuneable gain in a range of [9.5, 16]dB, and can work at frequencies lower than 450kHz. The gain, -3dB bandwidth, CMRR and power consumption were measured and compared with other tuneable instrumentation amplifier designs.

This work sought to understand the effects of using real memristive devices in the usually high-gain and good precision instrumentation amplifier configuration. It was concluded that i) The parasitic capacitance of the memristor needs to be considered carefully either as a nuisance or as a “free capacitor” that can shape amplifier behaviour with a bit more design freedom. ii) Harmonic distortion quickly becomes a problem as signal magnitudes increase if only Rg is replaced by a memristor, but there may be a class of problems involving very fine input signals where the memristors act in a sufficiently linear region to obviate this problem. Also, applying multiple memristors can improve signal distortion, as memristors compensate the nonlinear I-V characters of each other. iii) When balanced finely, the RC characteristics of the memristor can provide a slight but possibly important advantage by extending the -3dB cut-off region and sharpening the transition between pass-band and roll-off as shown in Figure 3.4 30kΩ memristor and resistor. In conclusion, the relatively low-cost reconfigurability bequeathed by memristive trimming unto instrumentation amplifiers seems to come with acceptable losses in other areas such as THD for at least certain application areas, thus removing a roadblock towards the viability of memristive-tuned analogue AC electronics.

Chapter 4

Memristor-based Tuneable Delay Circuit

4.1 Introduction

With the fast development of information transmission around the world, communication systems with less power, higher bandwidth and smaller signal distortion are needed. The phased array antenna system is a widely used communication technology capable of fast steering multiple beams in different directions with a high signal to noise (SNR) ratio [86] [87]. It also has high reliability as the failure of some array components will not strongly reduce the performance of the whole array system [88]. In phased array systems, true time delay (TTD) elements are the key components [89]. True time delay can be used in the sub-array level of the array system to alter the beam of radio wave direction, and reduce the "beam squint" phenomenon [90] [91].

The true time delay needs to be reconfigurable to steer the phase array system. There are many ways to achieve it, including using switched transmission lines [91] [92] [93], inductor or capacitor network [94] [95], microelectromechanical (MEMS) devices [96], and complementary metal-oxide semiconductor (CMOS) technology combined with other controlling signals [97] [98] [99] [100] [101] [102]. In these methods, CMOS technology is the most suitable one for on-chip integration and combines with other techniques. A technique called memristor can be considered when combined with CMOS technology. The memristor, also called resistive random-access memory (RRAM), is a two-terminal non-volatile electronic device [19]. The resistance of a memristor device depends on the history of voltage or current on it, thus the resistance value of the memristor can be controlled by voltage or current signal [2]. Broadly, there are two kinds of memristor devices, one can change its resistance between two digital stages high and low [103], and another one can change its resistance continuously in an analogue way [24] [104]. In the case of an analogue memristor, the memristor device can be seen as a finely tuneable resistor. Memristors have shown good potential in different research areas, especially in artificial neural networks [105] and as memory devices [31]. However, the analogue memristor can also be used in reconfigurable analogue circuit design. By controlling the memristor's resistance value, the characteristics of the circuit output can also be adjusted.

The biggest problem that limits the application of multi-stage analogue memristors in high-frequency circuits is the parasitic capacitance in the memristor device. As the structure of a metal-oxide-metal memristor is similar to a metal-insulator-metal(MIM) capacitor, the memristor also has an unwanted capacitance in between its two metal layers. The parasitic capacitance value depends on the size, material and technology of the memristor. For a $10\times10\mu m^2$ metal-oxide memristor, the parasitic capacitance can be around 10pF [5], which is a very large value for RF applications. This research aims to apply multi-stage memristors in radio frequency reconfigurable designs. To deal with the influence of the parasitic capacitance in the memristor, this research applies memristors in low-frequency voltage generators, and then uses the tuneable voltage generators to control a radio frequency device. By doing that, the memristor can control a high-frequency device without affecting the high-frequency signals.

In this research, a tuneable true-delay circuit that uses memristor-CMOS hybrid circuitry for fine delay tuning is proposed. The output voltage value of the DC source is decided by the memristor resistance level, and the delay time of the delay element is adjusted by its input DC voltage. In this case, the memristors control the delay time of the circuit indirectly. In section 4.2, the schematic of the memristor-based DC voltage source and delay element are reviewed. A 3-stage tuneable delay circuit works in GHz is designed based on the tuneable voltage source and delay element to increase the range of achievable delays to [155, 364]deg at 1.6 GHz. A memristor programming controller is designed to change the memristor resistance level based on digital commands, and a low-frequency delay circuit working in the MHz region is also designed to compare with the GHz circuit. The section 4.3 records the simulation data of the memristor-based DC source, the GHz tuneable delay circuit and the MHz delay circuit. The comparison of the delay with other works is recorded in the section 4.4. The section 4.6 concludes this research and discusses further prospects.

4.2 Design and Methodology

4.2.1 Basic Delay Element Overview

An ideal delay element can be seen as an all-pass filter with gain G=1 [106] [107] [108]. A CMOS all-pass filter was discussed in literature [109]. It uses a reconfigurable capacitor group to control the output delay time ($C1$ in Figure 4.1 (a)). By connecting and combining different capacitors in the reconfigurable capacitor group, the output delay time can be adjusted. However, limited by the quantity of capacitors, the minimum step of delay time is large, and the necessary space for the integration of capacitors is also large. In this research, the basic delay element schematic remains the same, but the output delay is adjusted via the input gate voltage of the NMOS transistors $M1$ and $M2$, as shown in Figure 4.1 (a). The red region is a memristor-based tuneable DC source, and the blue region is the delay element. In the following sections 4.2.2 and 4.2.3, the principles and functions of the memristor-controlled

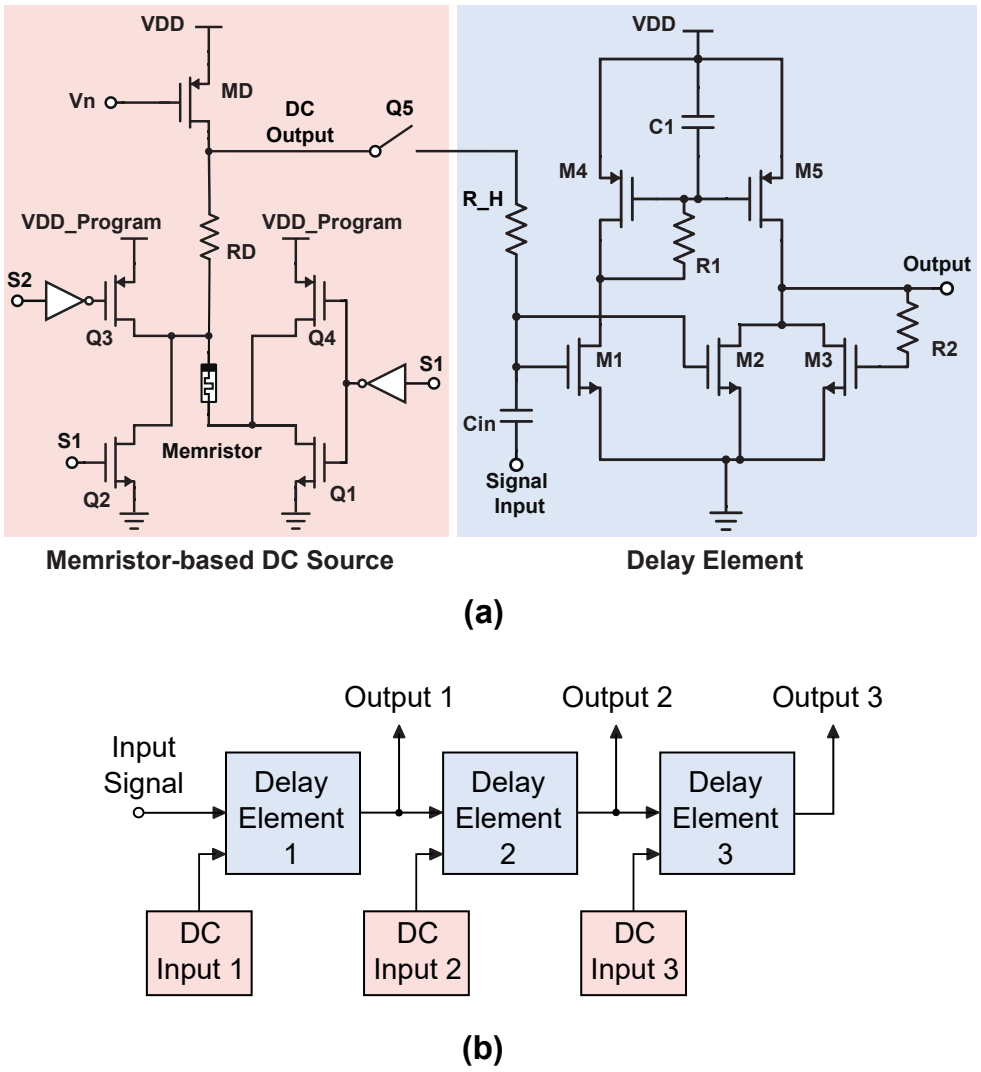


Figure 4.1: (a) The memristor-controlled DC voltage source (red region) and the voltage-controlled delay element (blue region). In the DC voltage source, MD, RD and the memristor form the normal DC voltage source part, and transistors $Q1$ to $Q4$ control the memristor programming. By changing the memristor value, the output voltage of the DC source changed, and hence the output delay of the delay element can be controlled. (b) Structure of the cascade 3-stage delay circuit. The circuit includes three tunable DC sources and three delay elements, and has three output ports that have different delay ranges.

DC voltage source and the all-pass filter delay element are described. In section 4.2.4, the memristor programming controller for memristor resistance adjustment are introduced. Section 4.2.5 summarizes the block diagram of the whole circuit and the connections between different elements.

4.2.2 Voltage-Controlled All-Pass Filter Delay Element

In the delay element, NMOS transistors $M1$ to $M3$ have the same width and length, while the width of PMOS transistor $M5$ is twice that of the width of $M4$. The gain function of the delay element is shown below, in which gm_1 to gm_4 are the transconductance of transistors $M1$ to $M4$, $I_{D(M5)}$ is the current flow through $M5$, C is the capacitance of the capacitor $C1$. The current flowing through M5 is two times the current through $M4$ and equals the sum of the currents on $M2$ and $M3$, as shown in equation 4.1. The currents on $M1$ to $M3$ are ideally the same. In this case, $M1$ to $M3$ have the same transconductance, and $M5$ has two times the transconductance of $M4$. Equation 4.2 shows the gain function of the delay element is the same as an all-pass filter when gm_1=gm_2=gm_3. The delay time offered by the circuit relates to frequency: At low frequency, the delay is approximately the time constant of the all-pass filter, as shown in equation 4.3, where dφ is the phase shift, dω is the change in frequency, and D is the delay time at the output. For high-frequency conditions, the delay starts to reduce fast when the frequency approaches the pole of equation 4.3, and reduces to half of the maximum delay value at the frequency pole. The functions shown in equation 4.1 to 4.3 are the basic functions of the circuit as an all-pass filter. To expand the working frequency range of the delay element, resistors $R1$ and $R2$ are added in the circuit as shown in Figure 4.1 (a). Resistor $R1$ helps increase the output phase linearity by creating an inductive peak at the cut-off frequency similar to the nulling resistor in OpAmp [110], and resistor $R2$ combines with the parasitic capacitance at the output port acts as an active inductor which expands the bandwidth [109] [111].

$$I_{D(M5)} = \frac{2 \times gm_1 \times V_{in}}{1 + \frac{sC}{gm_4}} = V_{in} gm_2 + V_{out} gm_3 \tag{4.1}$$

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{2gm_1}{gm_3 \times (1 + \frac{sC}{gm_4})} - \frac{gm_2}{gm_3} \tag{4.2a}$$

$$= \frac{2}{1 + \frac{sC}{gm_4}} - 1 = \frac{1 - s\frac{C}{gm_4}}{1 + s\frac{C}{gm_4}} \tag{4.2b}$$

$$D = \frac{d\varphi}{d\omega} = \frac{\frac{2C}{gm_4}}{1 + (\frac{2\pi fC}{gm_4})^2} \approx \frac{2C}{gm_4} \tag{4.3}$$

$$gm_4 = \sqrt{\beta_1 \beta_4} \times (V_{in} - V_{T1}) = \sqrt{\beta_1 \beta_4} \times V_{OV1} \tag{4.4}$$

$$\frac{d_D}{d_{V_{OV1}}} \approx \frac{-2C}{\sqrt{\beta_1 \beta_4} \times {V_{OV1}}^2} \tag{4.5}$$

In this research, the input DC voltage of transistor $M1$ V_{in} is used to (indirectly) control gm_4. Equation 4.4 is the relationship between V_{in} and gm_4. β_1, β_4 are the gain factors of the $M1$ and $M4$, V_{T1} is the threshold voltage of $M1$, and V_{OV1} is the overdrive voltage of $M1$. Based on equation 4.2 4.3 and 4.4, V_{in} can then control the gain and delay of the circuit. With larger V_{in}, the delay at the output will be smaller. When V_{in} close to the V_{T1} of the transistor, the delay is larger, and the delay variation with the change of V_{in} also becomes larger. Equation 4.5 is the derivative equation of delay time D and overdrive voltage V_{OV1}, shows that at low frequency, when V_{OV1} is close to 0, the trade of delay variation becomes very huge.

The delay elements can be cascaded to get a larger delay range. Figure 4.1 (b) shows a 3-stage delay circuit. The number of stages the circuit should include is decided by the required gain variation range. Although connecting three first-order all-pass filters in series can not improve their performance as all-pass elements, this method is still a simple method for expanding the delay range. A problem is, that a circuit can never form an ideal all-pass filter, as there are always errors between its poles and zeros. Cascading three all-pass elements that are the same makes the error grow exponentially. To deal with it, the input DC voltages of the three all-pass stages can be set slightly differently, hence the errors in the three stages can counteract each other.

With more stages of delay element, the output delay range is expanded, but the gain variation range is also larger and the minimum delay at the end of the cascade also accumulates. The DC input offered by the memristor-based DC sources lies in a voltage range larger than the threshold voltage of the transistors. As we seek to maintain the gain variation to $< \pm$ 3 dB, the voltage range of the DC input will also be limited by the output gain variation. To improve the minimum delay step of the delay circuit, each stage of the delay element combines with a memristor-based DC source to control the input DC voltage. The 3-stage delay circuit has three output ports, Output 1, 2 and 3, corresponding to the different output delay ranges. The minimum delay offered by the whole delay circuit is in Output 1, with DC Input 1 set to the maximum value; The maximum delay is in Output 3, when all the DC Inputs are set to the minimum value.

4.2.3 Memristor-Controlled Tuneable DC Source with memristor programming interface

The red region in Figure 4.1 (a) is the memristor-based DC source. Transistors $Q1$ to $Q4$ are the programming circuit, resistor RD, transistor MD and memristor form a DC voltage source. Transistor $Q5$ is a switch which turns off when the memristor is in programming. R_H is a resistor with very high resistance to avoid AC signal flows into the DC source.

The delay circuit works with a voltage supply of 1.8V. However, based on the technological reason the memristor in this research needs 5V pulses for programming. In this case, only the transistors in the DC source (MD and $Q1$ - $Q5$) and memristor digital programming controller are high-voltage MOSFETs which are suitable for working with 5V power supply. The whole circuit is able to work with all transistors at the same voltage rate if the memristor is capable of programming at low voltage.

When the DC source is working, Vn is set to a specific value to turn on transistor MD, $VDD_{Program}$ set to 0V. Transistor $Q1$, $Q5$ opens, $Q2$ to $Q4$ close. As the resistance of $Q1$ in the open state is very small, in this case, the voltage output is decided by the ratio between the resistance of transistor MD and the resistance of [RD + Memristor]. To program the memristor, Vn will first be set to 1.8V to turn off PMOS MD, $VDD_{Program}$ set to pulse signal with peak value around 5V. Program the memristor from the direction up to down needs $Q1$, $Q3$ open, and $Q2$, $Q4$ close. Program the memristor down to up will need $Q2$, $Q4$ open and $Q1$, $Q3$ down. The four transistors $Q1$ to $Q4$ are controlled by programming signals S1 and S2. Table 4.1 shows the relationship between the working mode of the DC source and the signal S1, S2. It can be found that in default condition both S1 and S2 are set to low voltage level, and the DC source is in normal work mode. To program the memristor, depending on the programming direction, S1 or S2 is set to the high voltage level. In up-to-down programming mode, the output of the DC source offers a high DC voltage to the input of the delay element, reducing gain and increasing power dissipation. To avoid this situation, a specific programming procedure is followed: a) Shut down MD, which limits the current flow through MD route in programming, b) Shut down switch $Q5$. c) Proceed with programming.

4.2.4 Memristor Programming Controller

The block diagram of the memristor programming controller is shown in Figure 4.2. For the 3-stage delay circuit, 3 memristor-based DC sources are used. The programming controller controls activity at switches S1 and S2 for all 3 stages. When the $VDD_{Program}$ ports of the memristor-based DC sources shown in Figure 4.1 (a) are connected to the programming pulses, the chosen memristor can be programmed. Combined with the red region of Figure 4.1 (a), to program the three memristors separately, 3 groups of S1 and S2 signals, in total

Table 4.1: Memristor-based DC source working modes with different input control signals

Working Mode	Signal S1	Signal S2
Normal work	Low	Low
Programming (up to down)	Low	High
Programming (down to up)	High	Low

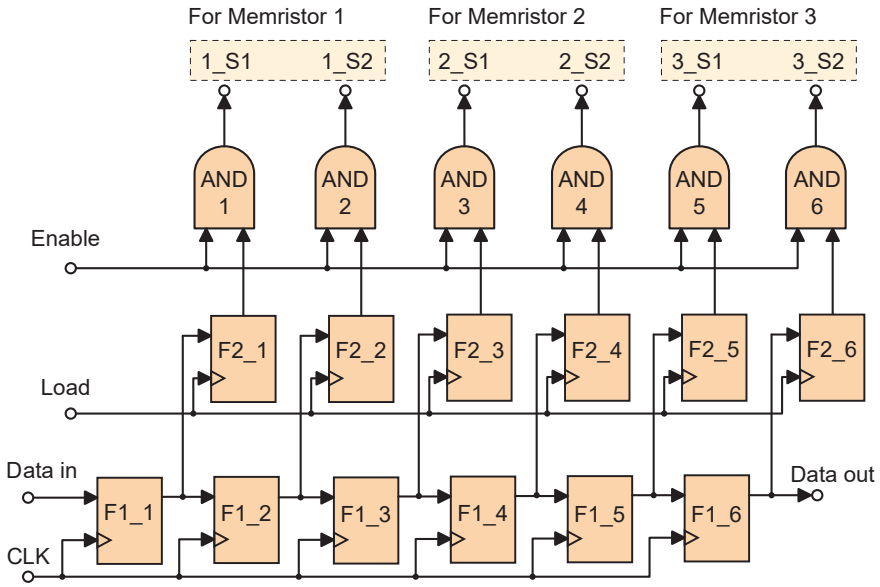


Figure 4.2: The memristor digital programming controller. In one programming process, only one memristor should be programmed. Data In is the 6-bit programming command, and 6 output signals 1_S1 to 3_S2 are the control signals S1&S2 for the three memristor-based DC sources.

6 control signals are needed. The structure of the memristor programming controller can be divided into three layers, the bottom layer is a scan-chain configuration, while the bottom and middle register layers form a serial-to-parallel register configuration, and finally, the third layer has 6 AND gates whose outputs connect to memristor-based DC sources.

The controller programs a single memristor at a time and only one of the 6 outputs should be high at any time (see table 4.1). The programming procedure begins by serially feeding the correct 6-number binary codes to the input register via Data In with a serial clock CLK. At the same time, Data Out starts to receive the Data in code from the output of the register F1_6 at the sixth clock signal. Next, the Load signal rises and activates the serial-to-parallel register block. Thereafter, the first layer registers are reset to all-0 in the process. Finally, to control the timing of the bias, an asynchronous Enable signal is used. In the tuneable DC sources, the $VDD_{Program}$ port in Figure 4.1 (a) offers pulse to the memristor, and MD, $Q5$ turn off. Once the programming of one memristor is finished, $VDD_{Program}$ is set to 0V first to reset the voltage at the DC Output node and then the Enable signal closes.

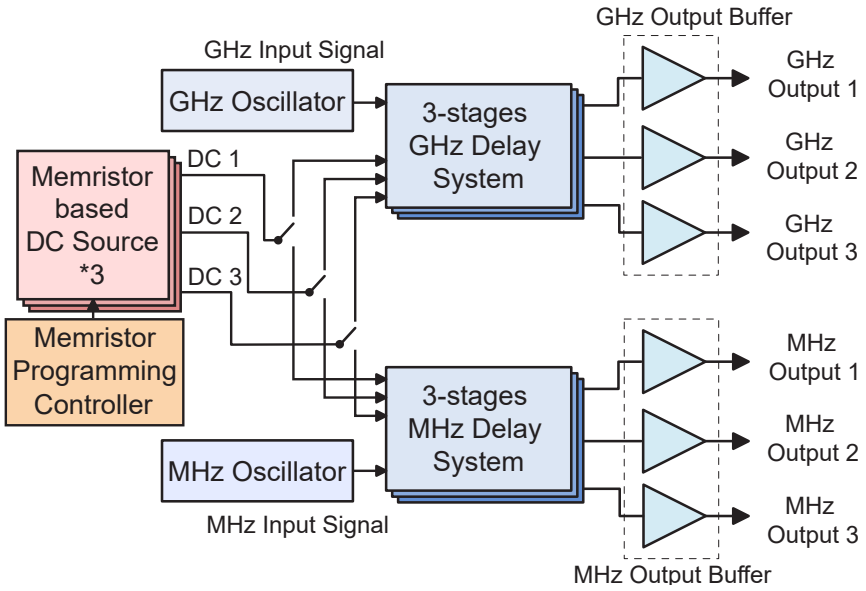


Figure 4.3: Block diagram of the whole circuit. The whole tunable delay circuit includes a GHz delay circuit with output buffers, a MHz delay circuit with output buffers, three memristor-based DC sources, a memristor programming controller, and two oscillators for input signal generation. Memristor programming controller adjusts the resistance of memristors, to control the ouput delay time of the delay systems.

4.2.5 Memristor-Controlled GHz / MHz tuneable Delay Circuit Block Diagram

The block diagram of the whole circuit is shown in Figure 4.3. The delay circuit includes both a 3-stage delay circuit part that works in low GHz and a 3-stage delay circuit part that works in MHz. This is to research on the performance of the delay schematic in low-frequency application, and compare the performance of the low and high-frequency delay circuits. Both of the delay circuits use the same memristor-based DC sources group to get DC voltage inputs. DC1, DC2, DC3 are the outputs of the three tuneable DC sources, corresponding to the three input DC voltages of 3-stage delay circuits. To reduce the power consumption and avoid signal interference between different delay parts, the GHz delay part and MHz delay part will not work at the same time. Only one delay part can get the DC voltage from the memristor-based DC sources, another delay part will be turned off. Furthermore, a GHz oscillator and a MHz oscillator are designed as signal generators for the two delay parts. The frequency of their output signal can be adjusted in a small range, and the centre frequencies of the two oscillators are 1.6GHz and 10MHz. The memristor programming controller connects to the three tuneable DC sources as shown in section 4.2.4. The whole circuit is integrated on chip in the area of $1mm^2$, which will be shown in the section 4.3.

The working procedure of the entire circuit is as follows: First, the connections between the memristor-based DC source and the Delay element module are cut off, and the memristor programming controller adjusts the resistance of each memristor according to external control signals. Second, the desired delay module(MHz or GHz) is selected, and the DC source is connected to this delay module, while the corresponding oscillator outputs an AC signal as the input signal for the delay module. Finally, the output signal from the delay module is connected to a vector network analyzer(VNA) through the output buffer. At the same time, the AC signal generated by the oscillator also outputs to the VNA. The VNA will compare the two signals to calculate the delay time offered by the delay circuit.

4.3 Simulation Results

All simulations of the memristor-based tuneable delay in this section were performed at post-layout. Delay data was simulated at the outer pins of the corresponding pads (i.e. including pad ring effects). The memristor resistance range chosen in the simulation is 10kΩ to 17kΩ, which is the range that has the best linearity in the whole resistance range of the memristor model used in this research [112]. This resistance range is small compared with other RRAM models, but it is sufficient to support a good delay range as we shall see below. The minimum step for memristor resistance variation is approximated at 1% of the current resistance value [112]. Simulation results of the GHz delay circuit indicate a working range of up to 1.6GHz where gain remains within 3dB of nominal. We thus quote a working range of 50MHz to 1.6GHz and show performance result plots in the [0.05, 2]GHz frequency range.

4.3.1 Results of memristor-based DC source

The voltage output of a memristor-based DC source is shown in Figure 4.4. It can be found that the DC voltage output increases with the memristor resistance nearly linearly. We empirically find that to maintain the maximum gain variation from Output 1 to Output 3 of the delay circuit smaller than 3dB, the best input DC voltage range is around 600mV to 700mV. Using Vn = 850mV our memristors support minimum and maximum output voltages of 584mV and 711mV, with a tuneable voltage range of 127mV. These voltage values also yield the maximum delay range of delay elements; it is no accident that these voltages are close to the threshold voltage of $M1$ - $M2$. The Vn value is chosen based on the resistance range of the memristor, the resistance value of resistor RD and the width-length ratio of transistor MD. To make sure the memristor value is constant during the delay working mode, the voltage on the memristor is maintained smaller than 0.6V. We note that Vn is an important tuning parameter: reducing Vn, the output voltage values are increased and the tuneable voltage range can also be expanded. Next, based on the minimum resistance variation step of the memristor, the resolution of the DC output can be inferred. Table 4.2 shows the minimum voltage step of the DC source at

different memristor values. The resolution data is calculated from the difference between the nominal output voltage (at the chosen memristor value) and the output voltage at 101% of that memristor value. Simulated results show that with increasing memristor resistance the DC voltage output value increases. Voltage resolution remains <3mV for the whole memristor resistance range.

During simulation, the voltage on the memristor stays within the [0.3, 0.5]V range, which will neither destroy the memristor element nor change its resistance level. When the memristor-based DC source switches to memristor programming mode, the programming pulse has a maximum theoretical peak value of 5V. The maximum current flowing through the memristor is 3.38mA with $VDD_{program}$=5V and memristor value 10$k\Omega$. In contrast, the current flow through the RD and MD is around 7μA. The maximum voltage at the DC Output node of the DC source in programming mode (up to down) is around 2.5V, which will be cut off from sending to the input of the delay element by $Q5$.

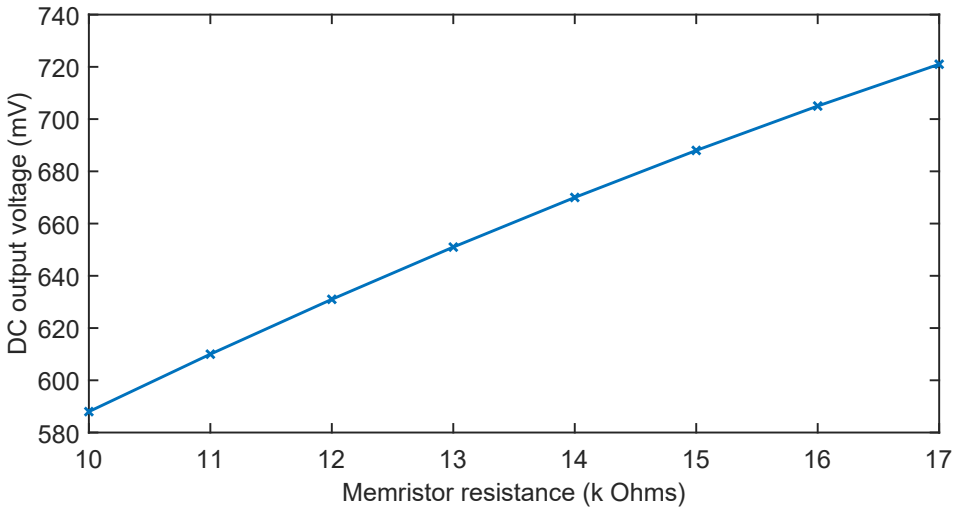


Figure 4.4: Memristor-based DC source output voltage with vary memristor values. Memristor resistance varies from 10kΩ to 17kΩ, and the output DC voltage changes in a range of [584, 711]mV.

Table 4.2: Minimum voltage step of the tuneable DC source at different memristor value

Memristor (kΩ)	10	11	12	13	14	15	16	17
Resolution (mV)	2.4	2.5	2.6	2.6	2.7	2.7	2.8	2.8

The Monte Carlo simulation results of the minimum and maximum voltage outputs with memristor value at 10kΩ and 17kΩ are shown in Table 4.3. Simulation results show the maximum and minimum voltage outputs may change in a fabricated integrated circuit, with the voltage tuneable range maintained between 104mV to 126mV. However, the tuneable DC source can adjust the output voltage range by changing the gate voltage Vn of transistor MD in Figure 4.1 (a), hence this problem can be relieved in the measurement of the taped-out circuit.

The corner analysis results of the minimum and maximum voltage outputs with different transistor corners, different temperatures and different supply voltage VDD are shown in Table 4.4. The front end of line(FEOL) process corner shows conditions that NMOS and PMOS transistors switch faster or slower compare with typical speed, including tt(typical-typical, which is the normal case), ff(fast-fast), ss(slow-slow), sf(slow-fast) and fs(fast-slow). In these corners, ff and ss represent the most extreme variations in performance. Besides, in normal semiconductor manufacturing process both NMOS and PMOS are form by the same etching step, hence ff and ss corners are more likely to occur compare with sf and fs corners. Because of that, in this research only ff and ss corners are shown in the results. Temperature analysis chooses -20°C and 85°C as the minimum and maximum work temperature the device may face.By setting the temperature parameters in the Cadence simulation environment, each model will operate according to its performance at the corresponding temperature. The white regions of the table show the analysis results with the same Vn voltage in Figure 4.1 (a) as a normal condition. Results show that the transistor corner and supply voltage variation significantly change the output voltage value, but the effect of temperature is comparatively small. This may be because the V_{ds} on transistor MD in Figure 4.1 (a) is strongly affected by the supply voltage and the transistor ff, ss corner effect. Also, the effect of corner, temperature and voltage supply can be relieved by adjusting the gate voltage Vn. The green regions in Table 4.4 show the output voltage range variations can be fixed by adjusting Vn.

Table 4.3: Monte Carlo result of the minimum and maximum voltage output of the DC source

	Mean	Max	Min	Std Dev
Min Output (mV)	594	841	432	123
Max Output (mV)	720	945	545	123

Table 4.4: Corner, temperature and voltage supply variation analysis of Memristor-based DC source

Condition	Output Voltage (mV)
Normal (Vn = 850mV)	588 $\sim$ 721
ff	953 $\sim$ 1107
ff (Vn = 942mV)	590 $\sim$ 727
ss	291 $\sim$ 366
ss (Vn = 752mV)	590 $\sim$ 720
T: -20°C	430 $\sim$ 539
T: -20°C (Vn = 810mV)	589 $\sim$ 719
T: 85°C	760 $\sim$ 908
T: 85°C (Vn = 900mV)	591 $\sim$ 727
VDD 1.7V	280 $\sim$ 356
VDD 1.7V (Vn = 749mV)	588 $\sim$ 721
VDD 1.9V	1009 $\sim$ 1158
VDD 1.9V (Vn = 950mV)	591 $\sim$ 725

4.3.2 Result of GHz delay elements

The width/length(W/L) of transistors $M1$ to $M4$ in the GHz delay elements are 20μm/180nm, while the W/L of $M5$ is 40μm/180nm, and the value of capacitance $C1$ is 33fF. The gain, phase and delay curves of the GHz delay circuit Output 1 port with different memristor values are shown in Figure 4.5. The delay value reduces with increasing memristor resistance via higher input DC voltage in the delay circuit. The delay time changes with memristor resistance non-linearly. This is because the relationship between the delay and input DC voltage of the circuit is non-linear. Corresponding to equation 4.4, when the input voltage is small and close to the threshold voltage of the input transistor, the variation of the input voltage will cause a larger change in gm_4 and thus the final delay time. The gain and delay curves with high memristor value show an upward trend at f > 1GHz as shown in Figure 4.5(c) (in fact peaking at approximate 2.2GHz, which is outside both our working and display ranges). The peaks are caused by the resistor $R1$ and $R2$ in Figure 4.1 (a), which expand the working frequency range (nulling resistor effect). Resistor $R1$ can make the phase curve more linear in low frequency. It causes a constant delay time reduction at low frequency, but does not influence the delay time at a higher frequency close to the cut-off frequency of the curve, hence the difference between delay values at low and high frequencies is reduced. Resistor $R2$ combines with output capacitance and parasitic capacitance of the delay circuit and generates a peak at the high frequency of the gain curve to expand the bandwidth of the delay element. The curve rising has a larger impact on the signal with higher input DC voltage.

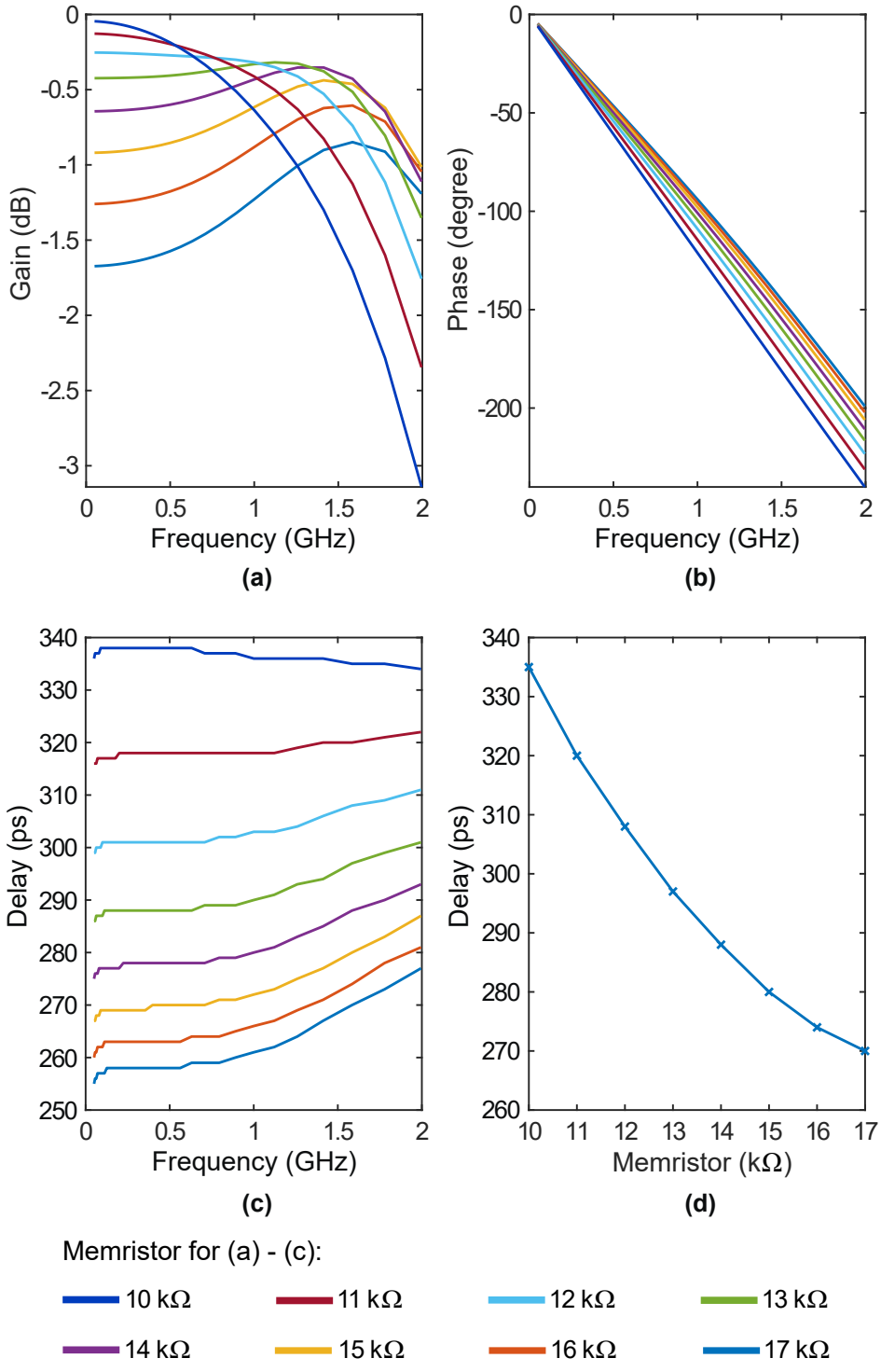


Figure 4.5: (a) Gain, (b) phase and (c) delay time of the GHz delay circuit Output 1 port with different memristor value. The gain variation in Output 1 is [-2.2, 0]dB in the range of [0.05, 1.6]GHz. Delay range reduces when frequency increases. At 1.6GHz, the delay range offered by Output 1 is [269, 335]ps. (d) The delay time with different memristor values at 1.6GHz.

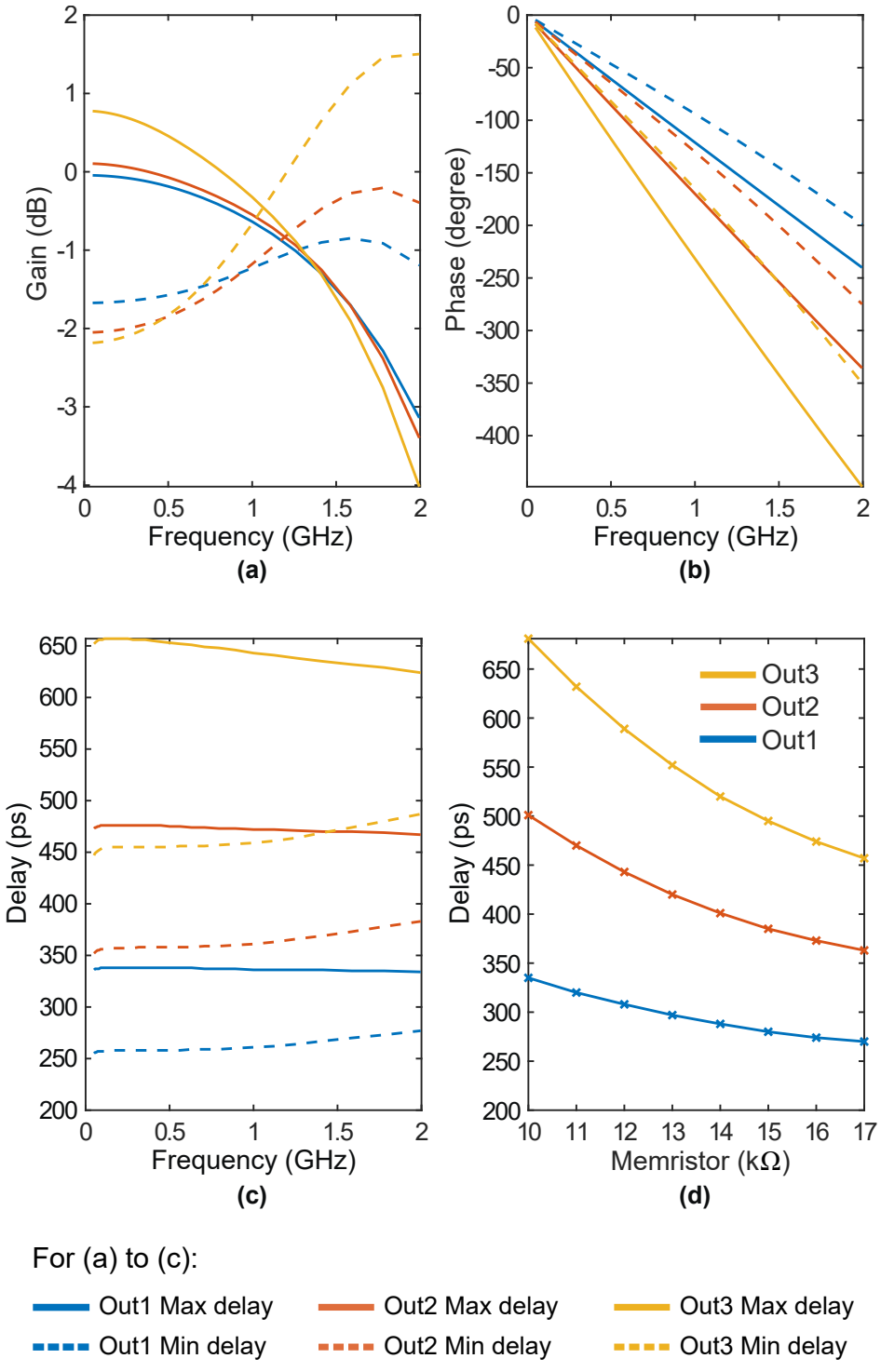


Figure 4.6: (a) Gain, (b) phase and (c) delay time of the GHz delay circuit. Gain varies from -2 to 1dB in the whole GHz delay circuit. The delay offered by the GHz circuit at 1.6GHz is [269, 632]ps, except a space between 335ps and 373ps can not be covered by the delay circuit. (d) The delay time with different memristor values at 1.6GHz.

The gain, phase and delay of the three output ports in the GHz delay circuit are shown in Figure 4.6, with the detailed data recorded in Table 4.5. In a cascade circuit, the later-stage circuit will have a larger gain variation. The 3dB gain variation limit is not violated if the second and third stages of the delay circuit use a memristor in the range [11, 16]kΩ, whilst the first stage delay uses the full [10, 17]kΩ resistance range. The working frequency range of the GHz delay circuit is 50MHz to 1.6GHz with gain variation smaller than 3dB. For gain values, the circuit should maintain a gain variation smaller than 3dB in all the working frequency ranges. To summarise, Table 4.5 records the gain variation from 50MHz to 1.6GHz of the cascade delay circuit, and the Phase and Delay data with different memristor values at 1.6GHz. At 1.6GHz, the GHz delay circuit can offer 269ps to 632ps delay time, which is 154° to 360° phase shift, with gain variation from -2dB to 1dB. The tuneable phase shift range at 1.6GHz is 206°. It can be observed from Figure 4.6 and Table 4.5 that there is a delay gap between 335ps and 373ps, which is larger than the maximum delay offered by Output 1 but smaller than the minimum delay offered by Output 2. Thus, in the case where the downstream user of the delayed signals can access whichever tap they choose (e.g. via MEMS switches) the circuit can offer nearly continuous delay coverage between approximate [270, 600]ps throughout its operating range, corresponding to phase delays between [180, 400]degree at 1.6GHz.

Table 4.5: Gain, phase and delay of the GHz delay circuit

	Gain (dB)	Phase (deg) @ 1.6GHz	Delay (ps) @ 1.6GHz
Output 1	-1.7 $\sim$ -0.1	-154 $\sim$ -191	269 $\sim$ 335
Output 2	-1.7 $\sim$ 0.1	-212 $\sim$ -268	373 $\sim$ 470
Output 3	-1.9 $\sim$ 1.1	-270 $\sim$ -360	474 $\sim$ 632

Table 4.6: Minimum delay step of the GHz delay circuit with different memristor value

Memristor (kΩ)	Output1 (ps)	Output2 (ps)	Output3 (ps)
10	2.7	5.7	8.7
11	2.3	4.7	7.4
12	1.8	3.9	6.2
13	1.4	2.9	4.8
14	1.1	2.3	3.8
15	0.8	1.8	2.9
16	0.6	1.3	2.2
17	0.4	0.9	1.5

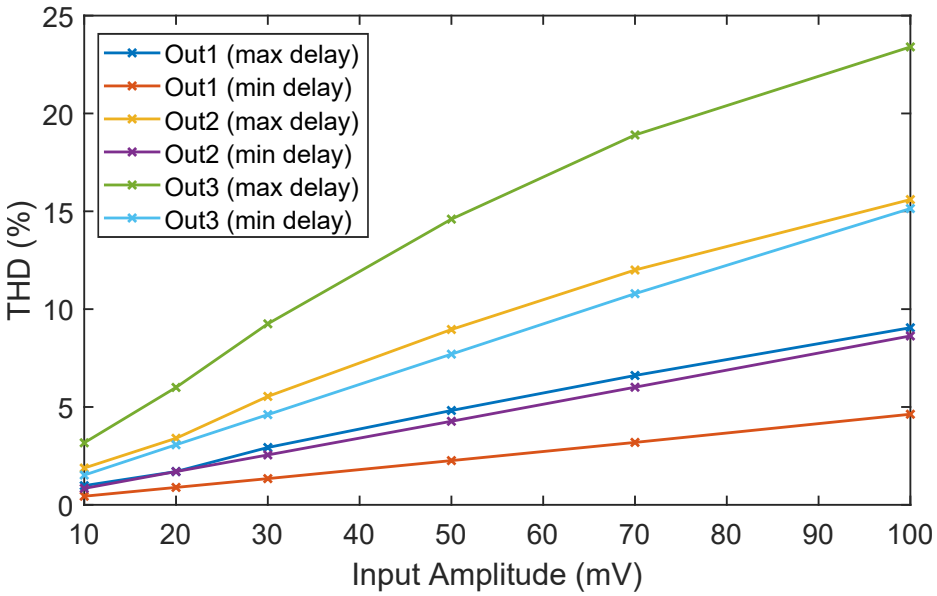


Figure 4.7: Total harmonic distortion of the GHz delay circuit. Signal distortion increases with the cascade output port number. To make sure all the output ports have signal distortion smaller than 10%, the input signal amplitude should be smaller than 30mV.

The minimum tuneable steps of the delay time at each output port with different memristor values are shown in Table 4.6. As the uncertainties of the delay circuit are compounded across the cascade architecture, the worst minimum delay step is at Output 3 with memristor value 10kΩ, which is 8.7ps, equals to 1.4% of the delay at that output port with that memristor value. The smallest minimum step is at Output 1 with memristor value 17kΩ, the value is 0.4ps and equals to 0.15% of the delay time at that output port and memristor resistance. It can be observed that with the same memristor value, the minimum delay step in Output 2 is a little higher than twice the minimum step in Output 1. This is because the signal connection wires and capacitors in between different delay stages also add small delay values to the signal.

The total harmonic distortion (THD) results of the GHz delay circuit are shown in Figure 4.7. With the same memristor value, Output 3 has the largest distortion while Output 1 has the lowest distortion. For all the output ports, output signals with larger delay values, which also have lower memristor values, have worse distortion curves. This is because when the input DC voltage is low, the transconductance of the transistor is also low, which makes the harmonic distortion worse. To guarantee THD <10%, the input signal amplitude should always be <30mV.

Table 4.7: Monte Carlo analysis results of the GHz delay circuit

	Mean	Max	Min	Std Dev
Max gain (dB)	1.1	2.31	-1.33	0.6
Min gain (dB)	-1.9	1.58	-6	1.22
Max delay (ps)	633	892	415	80
Min delay (ps)	255	301	199	17

Monte Carlo analysis results are shown in Table 4.7. The min/max gain and delay data is collected at a frequency of 1.6GHz. As voltage Vn controls the resistance of transistor M_D in Figure 4.1, reference to the green parts of Table 4.4, the deviation in the output voltage range of the DC source can be corrected by adjusting Vn. Because of that, in this simulation the DC input voltages were chosen to be constant values [605mV, 695mV, 711mV], which are the nominal voltage outputs of the DC source when memristor is 11kΩ, 16kΩ and 17kΩ. In these three values, input voltage 605mV corresponds to the maximum delay and the minimum gain at 1.6GHz in Output 3; Input voltage 695mV corresponds to the maximum gain at 1.6GHz in Output 3, and input voltage 711mV corresponds to the minimum delay in Output 1. The standard deviation (σ) shows the variation of the data. The ratio of [Std Dev/ Mean value] for the maximum delay is 12.6$\%$, and for the minimum delay is 6.7$\%$. Results show the minimum value of the maximum delay time is 415ps, and the maximum value of the minimum delay is 301ps. As the period at 1.6GHz is 625ps, the delay circuit can always offer phase shift around 173° to 239° at 1.6GHz. It can be found the minimum gain and maximum delay values have larger variations, which is because they are measured with low input DC voltage. When input DC voltage is low, a small variation in DC voltage can generate a large change of gain and delay in the output signal.

The corner, temperature and voltage supply variation analysis results are shown in Table 4.8. As with the Monte Carlo simulation setting above, the data in Table 4.8 is collected in the condition when fixed DC voltage is applied on the input of delay circuit with value [605mV, 695mV, 711mV]. Results show that transistor corners strongly affect the performance of the circuit, while temperature and supply voltage variation have a smaller influence. Transistor corner ff increases the gain variation and the cut-off frequency, but reduces the gain value, delay value and delay variation range. Corner ss reduces the gain variation at low frequency and the cut-off frequency, but increases the gain value, and offers a larger delay value and delay range. In this simulation, the gain variation of the ff corner and temperature 85°C become larger than 3dB at all frequencies, hence at the chosen bias voltages the operating bandwidth is reduced to 0. To deal with the large gain variation caused by the ff corner, the input voltage range needs to be reduced. The green regions show the results of the ff corner simulated with input voltage [0.59, 0.65]V, and the circuit at temperature 85°C with

input voltage [0.6,0.69]V. Both of the changed input ranges are affordable for the memristor-based DC voltage source. Combined with the Monte Carlo analysis results above, it shows the process variation in transistor functions is one of the largest problems in the performance reduction of the GHz delay circuit.

The area of the GHz delay circuit is $164\times181\mu m^2$, in which the 3 stages delay elements have an area of 82*104μm^2, while the rest of the area is occupied by the GHz output buffers. The power consumption of the GHz delay part with memristor value [10, 17]kΩ are [7.56, 18]mW, and the power consumption of one GHz output buffer is 68.4mW. To reduce power consumption, the output buffers in the delay circuits can be turned off when the output ports of these buffers are not used.

4.3.3 Result of MHz delay elements

The W/L of transistors $M1$ to $M4$ in the MHz delay elements are 12μm/2μm, while the W/L of $M5$ is 24μm/2μm, and the value of capacitor $C1$ is 33fF. The MHz delay circuit and GHz delay circuit have the same $C1$ capacitance value, to eliminate the difference of performance caused by the capacitors. The gain, phase and delay data of the MHz delay element part are recorded in Figure 4.8 Table 4.9. All data in Table 4.9 is collected with a 10MHz input signal. As the gain variation of the MHz delay circuit is smaller than the GHz circuit, all the three ports of the MHz circuit can use the full resistance variation range [10, 17]kΩ of the memristor to generate a larger delay range. The -3dB frequency of the MHz circuit is around 23MHz, well above the design operating frequency of 10MHz. Table 4.9 shows that the whole 10MHz delay circuit offers -46° to -198° phase shift, which equals to 13ns to 55ns time delay at 10MHz, with gain variation from -0.5dB to -1.89dB. The tuneable phase shift range is 152°.

Table 4.8: Corner, temperature and voltage supply variation analysis of GHz delay circuit. See text for modified versions.

	Gain(dB)	Delay(ps)	Bandwidth(Hz)
Normal	-1.9 $\sim$ 1.1	269 $\sim$ 632	50M $\sim$ 1.6G
ff	-6.3 $\sim$ -1.1	230 $\sim$ 461	None
ff (modified)	-4 $\sim$ -1	239 $\sim$ 471	50M $\sim$ 2.1G
ss	-0.9 $\sim$ 2.1	335 $\sim$ 1126	50M $\sim$ 550M
T: -20°C	-2 $\sim$ 1	258 $\sim$ 664	50M $\sim$ 1.2G
T: 85°C	-3.6 $\sim$ -0.5	299 $\sim$ 677	None
T: 85°C (modified)	-3.2 $\sim$ -0.5	299 $\sim$ 656	50M $\sim$ 1.25G
VDD 1.7V	-3 $\sim$ 0	288 $\sim$ 675	50M $\sim$ 1.26G
VDD 1.9V	-2.5 $\sim$ 0.5	272 $\sim$ 627	50M $\sim$ 1.41G

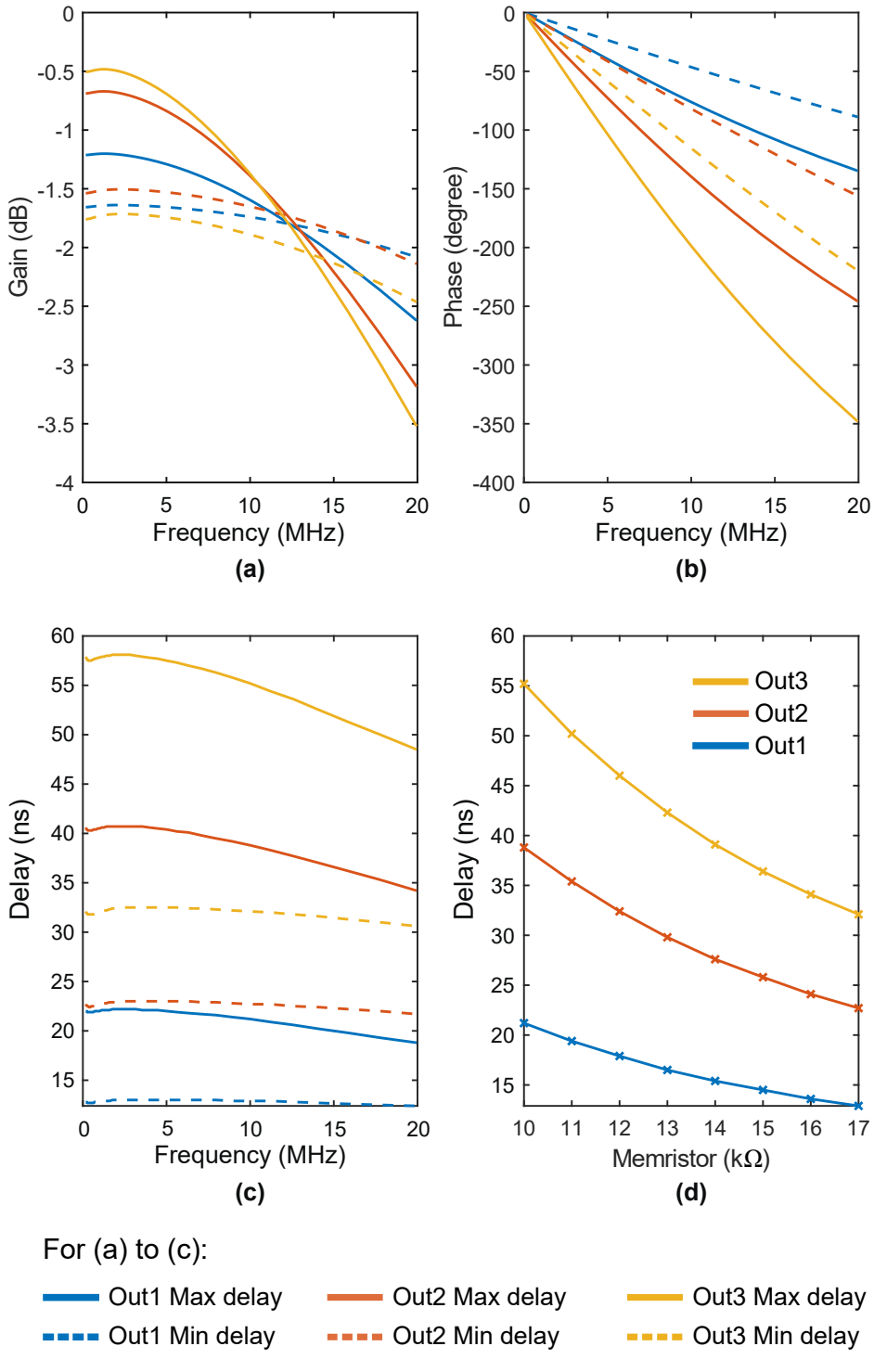


Figure 4.8: (a) Gain, (b) phase and (c) delay time of the MHz delay circuit. This MHz delay circuit is assumed to work at 10MHz. The circuit has a gain variation of [-1.89, -0.5]dB from 200k to 10MHz, and offers a delay range of [13, 55]ns at 10MHz. (d) The delay time with different memristor values at 10MHz.

The delay resolutions of the MHz delay circuit at different memristor values are recorded in Table 4.10. The best delay resolution is at Output 1 with memristor 17kΩ, yielding 0.38% of the delay. The worst delay minimum step is at Output 3 with the memristor at 10kΩ, yielding 1.62% of the delay value.

The MHz THD results are shown in Figure 4.9. Similar to the trend of GHz THD curves, with a higher stage of output port and lower memristor value, the THD values are also higher. To make sure the THD <10% in all the conditions, the input signal amplitude should be smaller than 20mV.

The Monte Carlo simulation results of the 10 MHz delay circuit are recorded in Table 4.11. Results show that gain variation remains low (well within 3dB). The minimum delay of the delay circuit has a change smaller than 1.8ns, but the maximum delay value varies up to 11ns. In the worst case, the delay circuit may not be able to offer 50ns delay time, which

Table 4.9: Gain, phase and delay of the MHz delay circuit

	Gain (dB)	Phase (deg) @ 10MHz	Delay (ns) @10MHz
Output 1	-1.74 ∼ -1.2	-46 ∼ -76	13 ∼ 21
Output 2	-1.65 ∼ -0.7	-81 ∼ -140	23 ∼ 38
Output 3	-1.9 ∼ -0.5	-115 ∼ -198	32 ∼ 55

Table 4.10: Minimum delay step of the MHz delay circuit at different memristor value

Memristor (kΩ)	Output1 (ns)	Output2 (ns)	Out3put (ns)
10	0.32	0.62	0.89
11	0.27	0.52	0.74
12	0.21	0.41	0.59
13	0.18	0.35	0.51
14	0.1	0.2	0.29
15	0.09	0.17	0.25
16	0.09	0.17	0.24
17	0.05	0.1	0.15

Table 4.11: Monte Carlo analysis results of the MHz delay circuit

	Mean	Max	Min	Std Dev
Max gain (dB)	-0.5	0.36	-1.56	0.36
Min gain (dB)	-1.96	-0.96	-3.16	0.4
Max delay (ns)	55	66	48	2.9
Min delay (ns)	13.7	15.5	12.6	0.5

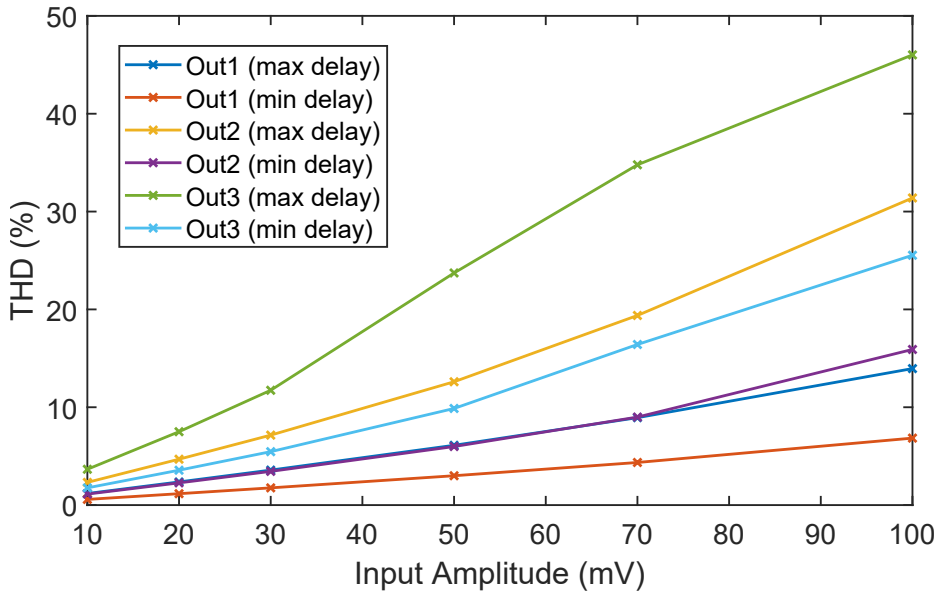


Figure 4.9: Total harmonic distortion of the MHz delay circuit. To make sure the signal distortion smaller than 10% in all the output ports, the input signal amplitude should be smaller than 20mV.

Table 4.12: Corner, temperature, and voltage supply variation analysis of MHz delay circuit

	Gain (dB)	Delay (ns)	Bandwidth (Hz)
Normal	-0.5 ∼ -1.89	13 ∼ 55	40k ∼ 23M
ff	-2.3 ∼ -3.6	12 ∼ 48	40k ∼ 28M
ss	1 ∼ -0.35	15 ∼ 63	40k ∼ 18M
T: -20°C	-0.05 ∼ -2.37	13 ∼ 55	40k ∼ 23M
T: 80°C	-0.95 ∼ -2.65	15 ∼ 57	40k ∼ 20M
VDD 1.7V	-0.2 ∼ -2.45	14 ∼ 57	40k ∼ 23M
VDD 1.9V	-0.64 ∼ -2.5	14 ∼ 56	40k ∼ 23M

equals to 180° phase shift at 10MHz. The standard deviation results of the gain value in the MHz circuit are much better than the GHz circuit. One of the main reasons is the circuit works at a lower frequency and is therefore less influenced by parasitic capacitance. Another reason is the cut-off frequency of the MHz circuit is at around 20MHz, while the Monte Carlo analysis of the circuit was done at 10MHz. Finally, the gain variation of the MHz delay circuit at low frequency is smaller compared to the GHz circuit, which means the input DC voltage range in this research has not reached the extreme working condition of the MHz circuit.

The transistor corner, temperature variation and voltage supply variation analysis results are recorded in Table 4.12. The delay and bandwidth vary in a small range, the circuit being able to reliably restrict gain within [0, -3]dB, support delays between [15, 48]ns and cover a bandwidth of [0.04, 18]MHz. The gain variation in percentage is larger compared with the delay and bandwidth but still affordable. It is found the MHz circuit has better stability than the GHz circuit when dealing with transistor corner effect, variation of temperature and supply voltage.

The area of the MHz delay circuit is $104\times138\mu m^2$. The power consumption of the MHz delay part with memristor value [10, 17]kΩ is [398, 954]μW, while the power of each MHz output buffer is 4.6mW.

4.3.4 Overview of the Circuit

Figure 4.10 shows the layout of the core circuit. The core circuit without the pad ring and connection wires is around $270\times300\mu m^2$, while the total area of the circuit including the pad ring is $1.078\times1.078mm^2$. The area framed in red is the GHz delay circuit including output buffers, the area framed in blue is the MHz delay circuit, the purple region has three memristor-based DC sources, and the orange region is the memristor programming controller. Other parts in the circuit include the switches between delay circuits and DC sources, the memristor-based DC sources, the oscillators to generate 1.6GHz and 10MHz signals, and the digital memristor programming circuit. The whole circuit layout including the padring is shown in Appendix A Figure B.5. In the padring, there are 4 VDD pads for the 1.8V power supply, and 4 VSS pads for ground. The multiple power supply pads ensure the high-power-consuming analog circuits receive a sufficient current supply. The main power consumption of the whole circuit is in the GHz output buffers. As expected, the GHz circuit uses much more power than the MHz circuit. The power consumption with a memristor value 17kΩ is larger than the power with a 10kΩ memristor because the memristor value controls the input gate voltage of the transistors in delay elements, thus controls the drain currents flowing through the delay circuits indirectly. Figure 4.11 shows the die photo of the tapped out tuneable delay circuit. In the next step, this wafer will be sent to the laboratory to integrate memristors onto the top metal layer.

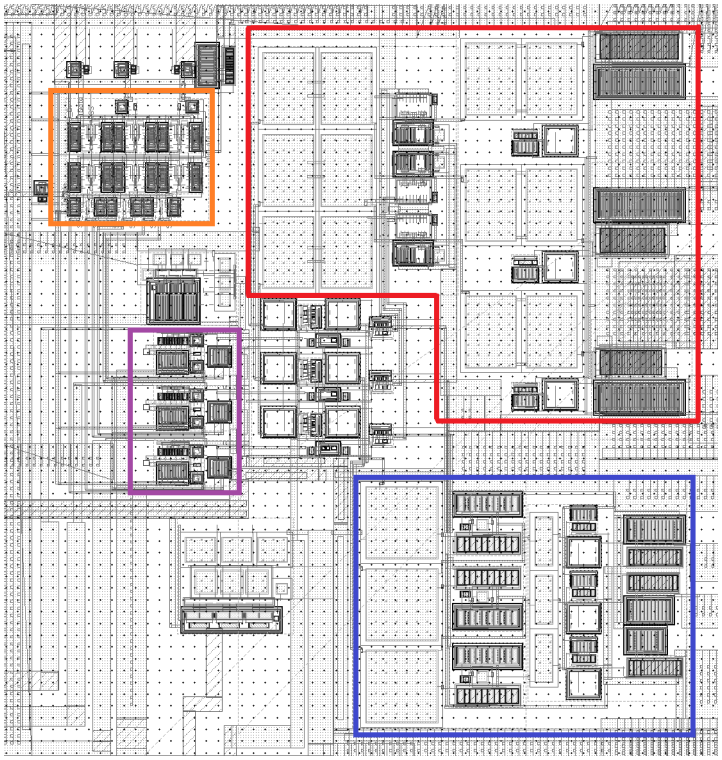


Figure 4.10: Layout of the tuneable delay core circuit. The red region is the GHz delay circuit, the blue region is the MHz delay circuit, the purple region is the memristor-based DC sources, and the orange region is the memristor programming controller.

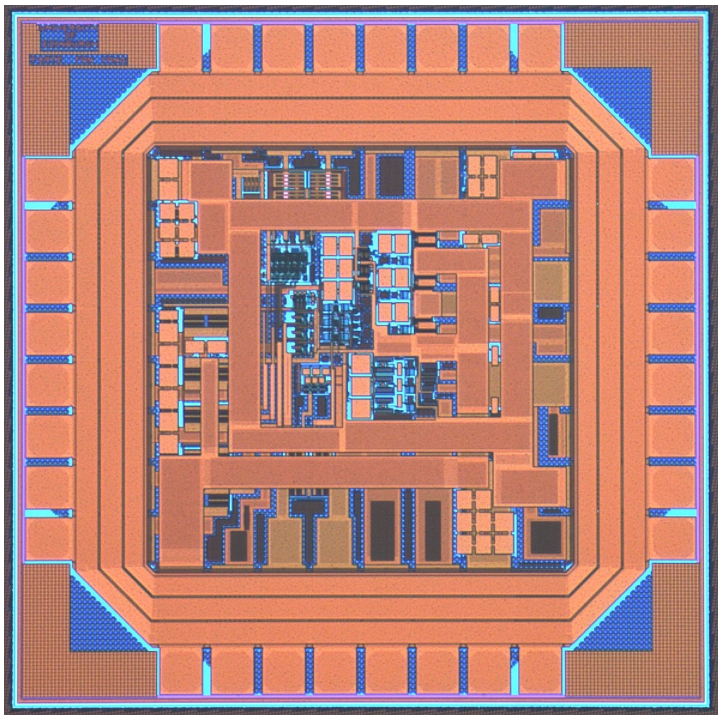


Figure 4.11: Die photo of the tapped-out tuneable delay circuit.

4.4 Discussion

4.4.1 Performance Analysis of the Tuneable Delay Circuits

Comparing the data of the GHz delay circuit with the MHz delay circuit, it is found that both the maximum and the minimum phase shift offered by the GHz delay circuit are larger than the MHz circuit. For the maximum phase shift, the reason is the data is simulated with 10MHz frequency while the cut-off frequency of the MHz delay circuit is around 23MHz. For the minimum phase shift, this result is mainly caused by the peripheral circuits of the GHz delay elements, including the output buffers, wide connecting wires, electrostatic discharge devices (ESD) and the pad ring around the whole circuit. When the signal flows through the buffers and the pads, there is a delay added to the signal. Besides, the parasitic capacitance of the peripheral circuits will also reduce the gain and increase the delay time of the delay circuit. For the delay circuit that works in 10MHz and output delay time in the range of ns, the effect of peripheral circuits is not obvious. However, for GHz delay elements that offer ps delay, the delay time caused by the peripheral devices is very significant.

The THD values of the MHz circuit are fully larger than the data of the GHz circuit at the same signal amplitude and output port. This is currently attributed to the smaller width/length ratio of transistors $M1$ to $M5$ (and therefore smaller transconductance g_m) required for MHz operation. Part of the effect can also be attributed to the MHz circuit using the full [10, 17]kΩ memristor range for DC voltage input, when the GHz circuit only uses memristor value 11kΩ for the maximum delay value, improving its THD figure. The smaller transconductance in the transistor $M1$ to $M5$ increase the harmonic distortion of the MHz circuit.

The performance comparison between the GHz delay circuit in this paper and other delay circuits is shown in Table 4.13. Both the size data of the GHz and MHz work in the table include the area of the memristor-based DC source, memristor programming controller and the oscillators for input signal generation, hence the sizes shown in this table are larger than the values that are recorded in the result chapter. The delay circuit in this research uses a small area, and reaches a very fine delay resolution when the output delay time is low. When the output delay value is high, the resolution reduces but also remains relatively high compared with other designs. The resolution of the design in this research changes as the delay time varies with the memristor value non-linearly. The power of this design also varies in a range, because the input DC voltages of delay elements change and vary the currents in the circuits.

There are still aspects that can be optimized. First, the delay range of this delay circuit strongly relates to the voltage Vn in the memristor-based DC voltage source, as shown in Figure 4.1 (a). Even if circuit performance is affected by the environment, by changing Vn the output DC voltage of the tuneable DC source can be adjusted to a suitable range-restoring function. However, it also means the accuracy of voltage Vn needs to be very high, otherwise the

Table 4.13: Comparison between the works in this research and other literature

	[109]	[113]	[114]	[115]	This Work (GHz)	This work (MHz)
Technology	0.14μm CMOS	65nm CMOS	0.13μm CMOS	65nm CMOS	0.18μm CMOS	0.18μm CMOS
Supply Voltage (V)	1.5	1.2	1.5	1.2	1.8	1.8
Gain (dB)	12 $\sim$ 15	-4.5 $\sim$ -0.8	5 $\sim$ 11	-4.8 $\sim$ 7.4	-2 $\sim$ 1	-1.9 $\sim$ -0.5
Gain Variation (dB)	$\pm$1.4	$\pm$0.5	$\pm$3	0.14	$\pm$1.5	$\pm$1.2
Max. Delay (ps)	550	2000	225	1000	632	55000
Frequency (Hz)	1G $\sim$ 2.5G	0.1G $\sim$ 0.5G	1G $\sim$ 15G	0.2G $\sim$ 3G	0.05G $\sim$ 1.6G	0.2M $\sim$ 10M
Delay Variation	1.8%	0.5%	14%	1%	4.1%	5.4%
Power (mW)	90	9.6	78	30	76 $\sim$ 86	5 $\sim$ 5.6
Resolution (ps)	13	-	15	2	0.4 $\sim$ 8.7	50 $\sim$ 890
Size (mm^2)	0.07	0.12	1.5	0.185	0.052	0.05

variation of Vn will change the performance of the circuit. On the other hand, engineers still necessary to calibrate the Vn value by themselves, which makes the operation of this circuit more complex. To solve these problems, an automatic negative feedback circuit that can adjust the output range of DC sources might be helpful. As memristors show varying static resistance as a function of bias voltage, it might be possible to use memristors to design such a feedback circuit. Second, the circuit is designed to be able to choose one of the three output buffers open and the other two close for lower power consumption, i.e. different delay ranges are made available at different, buffered output ports. A better method may be to use only one buffered output port, with a switch group to select which tap controls the buffer. The challenge in this method is designing high-frequency switches. They also need low gain distortion to allow high-speed signals to pass when they turn on, and isolate the signal effectively to avoid signal mixing via cross-talk. Third, this delay circuit cascades three 1^{st}-order all-pass filters. This method helps expand the delay range, but does not make the whole delay circuit become a higher order filter. To improve the circuit structure, the 3-stage delay circuits can include one 1^{st}-order all-pass filter and two 2^{nd}-order all-pass filter, to generate a 5^{th}-order all-pass filter. These three directions can be considered to improve the design in further work.

4.4.2 Consideration of Other Design Feasibility

During this research, many circuits based on memristor applications are considered. However, only a small quantity of circuits which are necessary for the final tuneable delay chip are used. In this section, two types of circuit structures that are not adopted in the chip are discussed. The first topic is the different structures of memristor-based DC voltage sources. The comparisons of output voltage ranges, corner analysis results and Monte Carlo results of different voltage sources are discussed. The second topic is an unused memristor-based tuneable delay element structure. Different from the method of using a memristor to generate tuneable DC voltage and control the delay element indirectly by this voltage, the delay element in this section is directly controlled by a memristor. Performance analysis of this delay element is shown in this section, and the reason for abandoning this design is explained.

Different Structures of Memristor-Based DC Voltage Sources

Referring to Figure 4.12 (a) and the red region of Figure 4.1 (a), the memristor-based tuneable DC voltage source can be separated into two parts, which are the memristor programming part and the DC voltage source part. In the memristor programming part, transistor $Q1$ turns on and $Q2$ to $Q4$ turn off when the voltage source is in normal work, hence in this part, only the memristor device affects the output voltage. The DC voltage source part plus the memristor undertake the primary role of this circuit as a DC voltage source. The ratio between the resistance of [Position 1] and [Position 2 + memristor] decides the output voltage. In Figure 4.1, Position 1 is a PMOS transistor controlled by external voltage Vn, and Position 2 is a resistor. By placing different combinations of circuit components at positions 1 and 2, the range of output voltage will vary.

Figure 4.12 (b) shows four designs of the adjustable DC source part which are different from the original design in Figure 4.1. Designs 1 and 2 place Vn-controlled PMOS at Position 1, and use one NMOS / PMOS with the gate connects to the drain at Position 2. Designs 3 and 4 place Vn-controlled NMOS at Position 2, and use a resistor / PMOS whose gate connects to the drain at Position 1. Table 4.14 lists the devices in Position 1 and Position 2 of each design, including the width and length (W/L) ratio of each transistor and the value of external control voltage Vn. In the condition of a resistor, the resistance value is recorded.

Comparing the data of Design 1 and Design 2 with the Original design in Table 4.14, it can be found both Design 1 and Design 2 use a large-size transistor at Position 2. To output a voltage with a range of 0.6 to 0.7V and maintain a voltage of around 0.5V on the memristor, Position 1 should have a large resistance, and Position 2 needs to have a small resistance. However, in the condition of Design 1 and Design 2, the drain-to-source voltage on the transistors in Position 2 becomes very small. When the gate of this transistor connects to its drain, the input

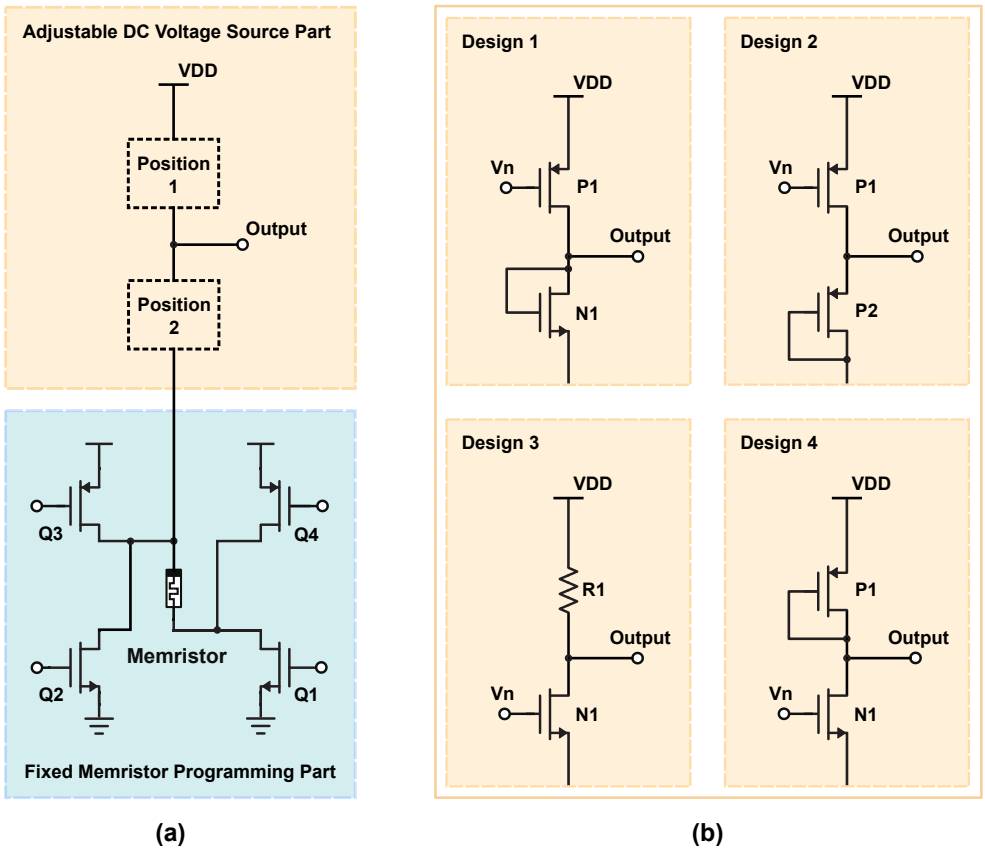


Figure 4.12: (a) The Basic structure of the memristor-based DC source in this research. (b) Four additional designs of the adjustable part in the DC source. Different designs have different output voltage ranges and abilities to maintain the output voltage amidst variations in corners, temperature, supply voltage, and other random variables.

Table 4.14: Different designs of memristor-based tuneable DC voltage source, and the size/resistance of their transistors/resistors.

Designs	Position 1	Position 2
Original Design	PMOS (Vn = 0.85V) W/L: 20μm/600nm	Resistor 10kΩ
Design 1	PMOS (Vn = 0.95V) W/L: 5μm/600nm	NMOS W/L: 300μm/600nm
Design 2	PMOS (Vn = 0.9V) W/L: 5μm/600nm	PMOS W/L: 300μm/600nm
Design 3	Resistor 40kΩ	NMOS (Vn = 1.35V) W/L: 20μm/600nm
Design 4	PMOS W/L: 5μm/600nm	NMOS (Vn = 1.35V) W/L: 20μm/600nm

Table 4.15: Output voltage range of each design in normal work, ff/ss corners, -20/85°C temperatures and 1.7/1.9V supply voltages.

Condition	Original Design (mV)	Design 1 (mV)	Design 2 (mV)	Design 3 (mV)	Design 4 (mV)
Normal	588 ∼ 721	652 ∼ 692	679 ∼ 725	601 ∼ 1010	601 ∼ 697
ff	953 ∼ 1107	666 ∼ 757	719 ∼ 810	436 ∼ 741	644 ∼ 749
ss	291 ∼ 366	670 ∼ 683	671 ∼ 687	908 ∼ 1220	552 ∼ 640
T: -20°C	430 ∼ 539	677 ∼ 698	705 ∼ 733	712 ∼ 1090	606 ∼ 690
T: 85°C	760 ∼ 908	629 ∼ 698	647 ∼ 716	509 ∼ 904	596 ∼ 705
VDD 1.7V	280 ∼ 356	559 ∼ 571	578 ∼ 595	518 ∼ 910	505 ∼ 599
VDD 1.9V	1009 ∼ 1158	776 ∼ 867	799 ∼ 887	691 ∼ 1100	699 ∼ 796

voltage of this transistor is small, hence its resistance tends to be a large value. To avoid that, the W/L ratio of this transistor has to be very large, to reduce the resistance. Because of these reasons, Design 1 and Design 2 are not suitable for DC voltage sources with low output voltage.

Table 4.15 records the output voltage ranges of each design in the normal condition, ff/ss corners, low/high temperatures, and smaller/larger supply voltages. It is found that Design 1 has the smallest tuneable voltage range, which is only 40mV. Design 2 is similar to Design 1, the tuneable output voltage range is 46mV. Design 3 has over 400mV tuneable voltage range, which is the largest range, and Design 4 has a 96mV voltage range, similar to the 133mV range of the original design. The small voltage ranges of Design 1 and Design 2 are caused by the transistors at Position 2 with gates connected to the drains. For a transistor whose gate connects to its drain, when the voltage on it rises, its gate-source voltage(Vgs) increases and reduces its resistance, hence the rising voltage on it will be suppressed; Same, when the voltage on it decreases, its Vgs value reduces and increase the resistance. Because of that, the transistor with the gate connected to the drain will suppress the change of voltage. For Design 3, the gate voltage of transistor $N1$ is controlled by Vn. When memristor resistance increases, the voltage on the memristor, which is also the source voltage of $N1$ increases, which makes the Vgs of $N1$ reduce, and further increases the resistance of $N1$. Because of that, the Vn-controlled transistor at Position 1 increases the change of voltage, which makes Design 3 has the largest tuneable voltage range. Design 4 has both the transistor whose gate connects to the drain and the Vn-controlled transistor at Position 1, hence their impacts on the tuneable voltage range cancel each other.

Table 4.16: Minimum voltage step of different voltage source designs with varying memristor values.

Memristor (kΩ)	Original Design (mV)	Design 1 (mV)	Design 2 (mV)	Design 3 (mV)	Design 4 (mV)
10	2.4	0.6	0.7	8.6	2
11	2.5	0.6	0.7	8.4	1.9
12	2.6	0.7	0.8	7.7	1.8
13	2.6	0.7	0.8	8	1.9
14	2.7	0.8	0.9	7.3	1.8
15	2.7	0.8	0.9	6.9	1.7
16	2.8	0.9	1	6.6	1.7
17	2.8	1	1	6	1.6

It can be observed that for all the corners, temperatures, and supply voltage variation conditions, Design 3 and Design 4 have smaller variations in output voltage ranges compared with the Original Design results. The voltage ranges of Design 1 and Design 2 reduce in the conditions of ss corner, T = -20°C, and VDD = 1.7V, but also increase in conditions ff corner, T = 85°C, and VDD = 1.9V. The minimum/maximum voltage range of Design 1 is [12, 99]mV, and the minimum/maximum output range of Design 2 is [17, 98]mV. These results show the stability of Design 1 and Design 2 are low. Design 3 also shows reduced voltage ranges in the ff and ss corners, which are around 300mV compared with the 400mV range in normal work. Design 4 has the best stability. In all the conditions, it has a maximum voltage range of 105mV and a minimum voltage range of 84mV. Besides, the output voltage shift of Design 4 is also the minimum one, which is always smaller than 100mV, while the maximum voltage shift for the original design is 421mV.

Table 4.16 records the voltage resolutions for each design with different memristor values. The voltage resolutions for all the designs are different, which is mainly caused by the difference in tuneable voltage range. As all of them use memristors to adjust the output voltage, with fixed resistance range and minimum step of memristor programming, the voltage resolutions calculated as percentages should be similar for all the designs.

One thing that can be observed from Table 4.16 is, that for the designs that place Vn-controlled transistors at Position 1 (Original Design, Design 1, Design 2), the minimum voltage steps increase with the memristor resistance. However, for the designs that set Vn-controlled transistors at Position 2 (Design 3, Design 4), the minimum voltage steps reduce with the memristor resistance. This phenomenon can be explained by the variation in Vds (drain-source voltage) on the Vn-controlled transistors. When the memristor value is small, Vds on the Vn-controlled transistor is large, which makes the transistor work in the saturation region. In this case,

Table 4.17: Monte Carlo results of different voltage source designs.

	Memristor (Ω)	Mean (mV)	Max (mV)	Min (mV)	Std Dev (mV)
Original Design	10k	594	841	432	123
	17k	720	945	545	123
Design 1	10k	653	758	556	43
	17k	695	821	577	51
Design 2	10k	680	708	671	7
	17k	727	791	694	19
Design 3	10k	607	850	453	92
	17k	1003	1180	823	76
Design 4	10k	601	688	511	37
	17k	696	776	608	35

an increase in memristor value, which also means a reduction of Vgs of the Vn-controlled transistor, will strongly increase the resistance of the transistor, and hence the output voltage is strongly increased. However, when the memristor resistance is large, the Vds of the transistor becomes smaller, making the transistor exit the saturation region. The reduction of Vds will reduce the resistance of the transistor. Because of that, when the memristor resistance is large, the rising trend of the output voltage slows down.

Table 4.17 shows the Monte Carlo results of each design. The 4 new designs have smaller standard deviation values compared with the original design. Design 1 has the minimum tuneable voltage range, but the Std Dev values are still large, which means it has low stability, and the actual performance of the circuit after fabrication may differ significantly from the simulated results. Design 3 also has large Std Dev values. However, it has the largest tuneable voltage range, hence the large deviation values are acceptable. Design 2 has one of the smallest tuneable voltage ranges, but also the lowest deviation values. Overall, Design 4 achieved the best balance between performance and stability. It has a tuneable voltage range slightly smaller than the Original Design, but the Std Dev values are smaller than all the other designs except Design 2.

Combining all the comparison results, including the transistor sizes, output voltage range, and stability, the designs that have great overall exhibitions can be found. Design 1 has the lowest tuneable voltage range and low stability, which is not suitable for use in practice. Design 2 can be used for very fine small-range voltage control. Design 3 can be applied in circuits that need a larger tuneable delay range compared with the delay elements in this research. Design 4 has a small size and good stability, which is suitable for use in voltage-controlled circuits that

need a voltage range of around 90mV. However, as Design 4 has good stability, it is also hard to increase its tuneable voltage range. Because of that, Design 4 has a voltage range that is slightly smaller than the requirement of the tuneable delay circuit in this research, and finally not be used in the chip.

Memristor Directly-Controlled Tuneable Delay Circuit

Referring to Figure 4.1, in this research, the tuneable delay elements are controlled by the DC input voltages of the NMOS transistors $M1$ and $M2$, and the DC voltages are controlled by a memristor-based tuneable DC voltage source. However, this is not the only way of using memristors in the design of a reconfigurable delay circuit. Figure 4.13 (a) shows another structure of the tuneable delay element. In this structure, the input DC voltages of NMOS transistors $M1$ and $M2$ are constant, a memristor is placed between the ground and the sources of NMOS transistors. When the memristor resistance changes, the Vgs values of the three NMOS transistors $M1$ to $M2$ also change, and hence the output delay time is changed. By doing this, the memristor can adjust the output delay directly, instead of placing the memristor in an extra DC voltage source and control the delay element indirectly. Figure 4.13 (b) shows a 3-stage tuneable delay circuit generated by 3 memristor-directly-controlled delay elements in cascade. Different from the circuit in Figure 4.1 (a), this delay circuit doesn't need DC sources for delay time adjustment, hence the structure is simpler and the circuit area will be smaller.

This delay circuit was also simulated under the same test environment of the GHz circuit and MHz circuit in the research of this chapter. Figure 4.14 shows the simulation results of the gain, phase, delay of the memristor-directly-controlled delay circuit, and also the delay time at 120MHz related to the memristor value. The data in detail is recorded in Table 4.18. In this delay circuit, all the 3 delay elements can work with the whole resistance range [10, 17]kΩ of memristors. The memristor is assumed to have a parasitic capacitance of 10pF. The input DC voltages of the NMOS transistors are 1.2V, and the capacitor C has a value of 10fF. As the functions of the phase linearity resistor R1 and bandwidth expand resistor R2 only work at high frequency(>GHz), in this circuit simulation these two resistors are deleted. This delay circuit can work in a frequency range from 1MHz to 120MHz, with gain varying between -

Table 4.18: Gain, phase and delay of the memristor-directly-controlled delay circuit

	Gain (dB)	Phase (deg) @ 120MHz	Delay (ns) @ 120MHz
Output 1	-1.67 $\sim$ -0.33	-62 $\sim$ -78	1.43 $\sim$ 1.82
Output 2	-2.8 $\sim$ -0.2	-105 $\sim$ -138	2.41 $\sim$ 3.22
Output 3	-2.95 $\sim$ -0.05	-139 $\sim$ -187	3.22 $\sim$ 4.38

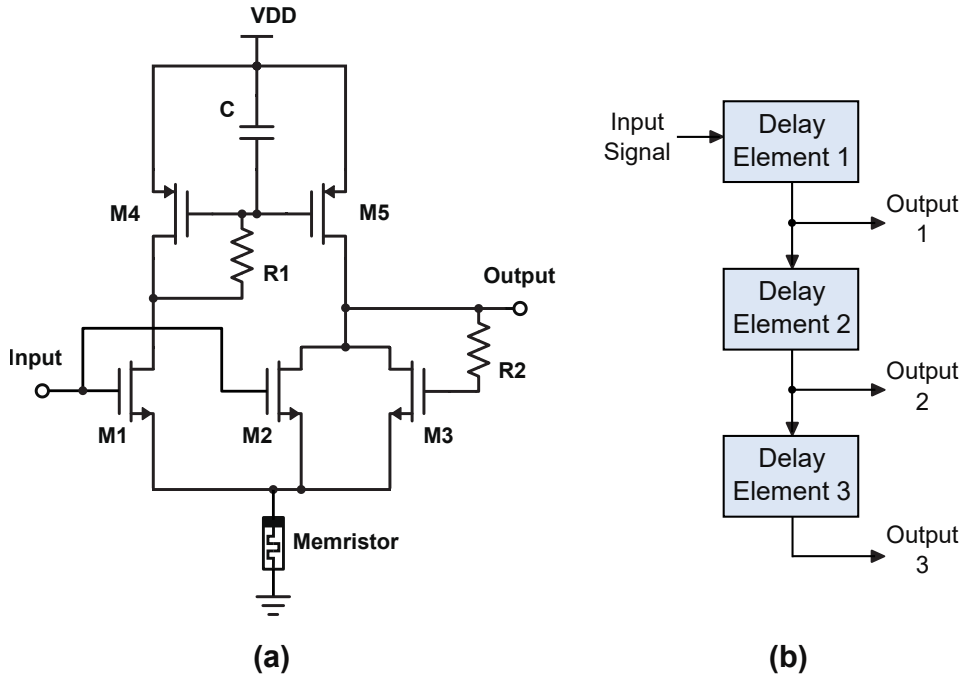


Figure 4.13: (a) A tuneable delay element structure directly controlled by a memristor. A memristor is placed between the source of NMOS transistors and the ground, to adjust the V_{gs} of NMOS transistors and then change the output delay. (b)A tuneable Delay circuit based on the memristor-directly-controlled delay elements.

Table 4.19: Minimum delay step of the memristor-directly-controlled delay circuit.

Memristor (kΩ)	Output1 (ps)	Output2 (ps)	Output3 (ps)
10	6	13	18
11	6	13	19
12	7	14	21
13	8	15	21
14	8	15	23
15	8	17	24
16	9	17	25
17	9	18	26

2.95V and -0.05V. At 120MHz, this circuit offers a tuneable phase in a range [62, 187]°, which is [1.43, 4.38]ns in delay time. It can be observed from Figure 4.14 and Table 4.18 that there is a delay gap between 1.82ns and 2.41ns because the minimum output delay of Output 2 is larger than the maximum delay offered by Output 1.

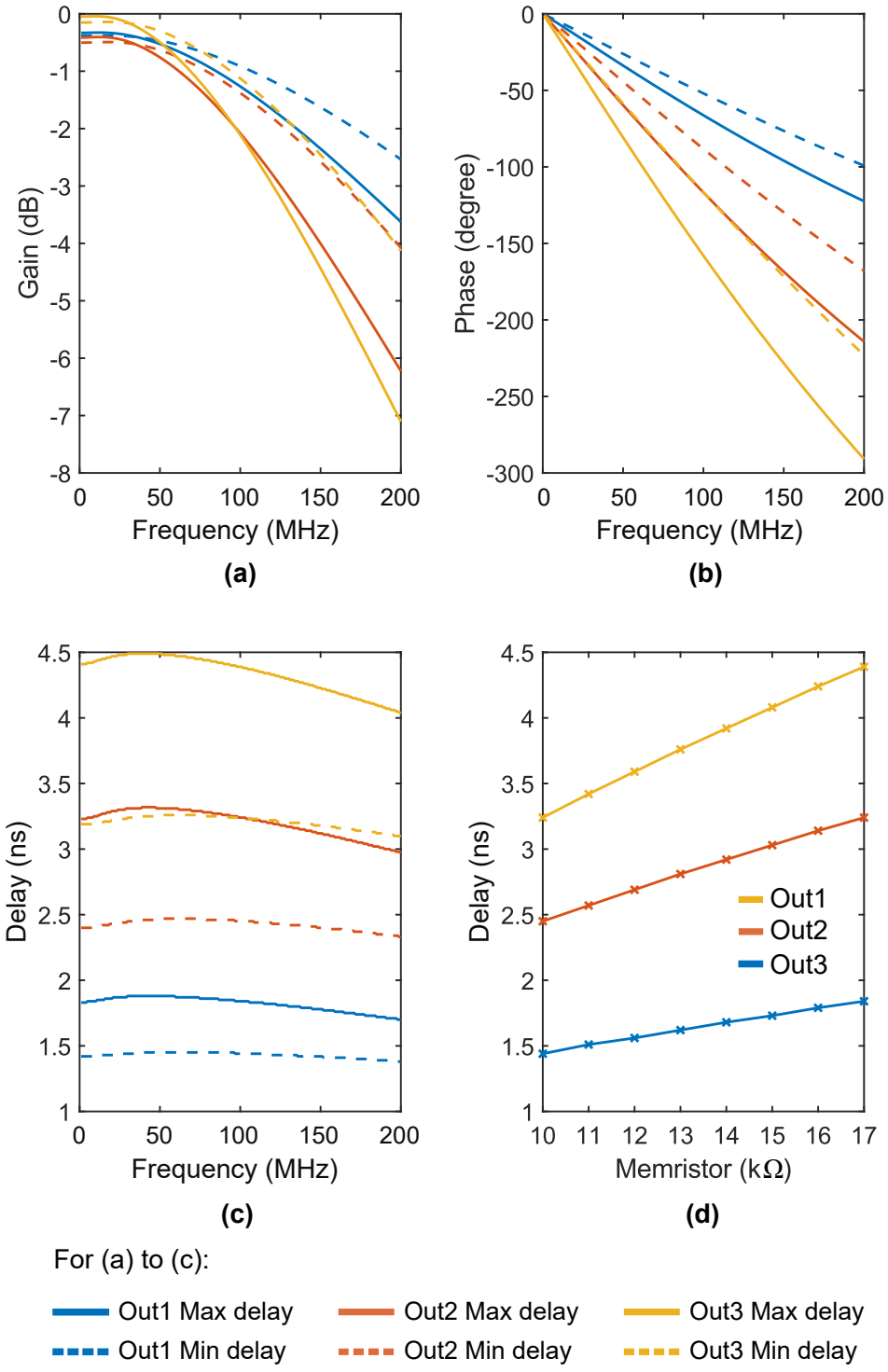


Figure 4.14: (a) Gain, (b) phase and (c) delay time of the memristor-directly-controlled delay circuit. This delay circuit can work from 1MHz to 120MHz. The tuneable delay circuit has a gain variation of [-2.95, -0.05]dB, and offers a tuneable delay range of [1.43, 4.38]ns at 120MHz. (d) The delay time with different memristor values at 120MHz.

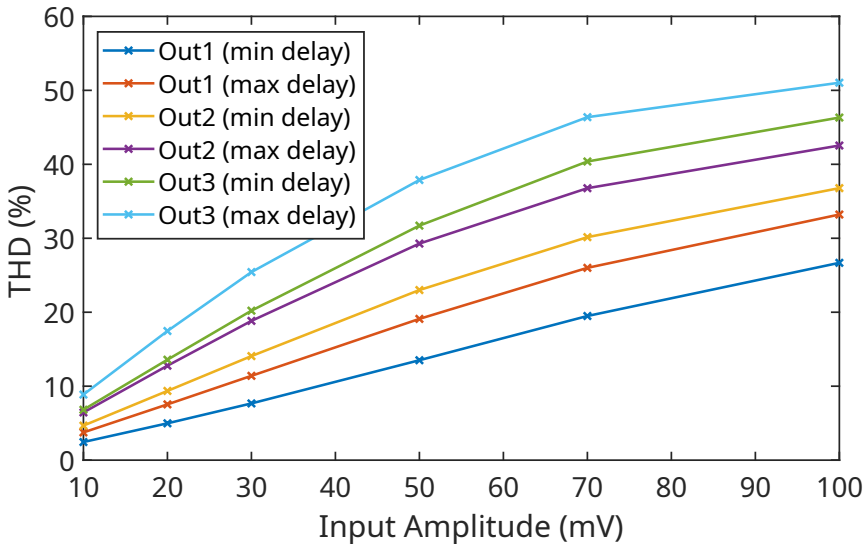


Figure 4.15: THD of the memristor-directly-controlled delay circuit. To maintain the signal distortion smaller than 10% in all the output ports, the input signal amplitude should $\leq$10mV.

Comparing Figure 4.14 (d) with Figure 4.6 and Figure 4.8 (d), it can be found that the delay time offered by the memristor-directly-controlled circuit is more linear than the DC voltage controlled GHz and MHz delay circuits. The detailed minimum delay steps offered by the memristor-directly-controlled delay circuit at different memristor values are recorded in Table 4.19. In the memristor-directly-controlled delay circuit, the ratio between the largest and smallest [minimum delay step] offered by the same output port is around 1.5, while this ratio in the GHz and MHz delay circuit is around 6. This means the user of the memristor-directly-controlled delay circuit can estimate the required memristor value from the wanted delay time more accurately.

Figure 4.15 shows the THD curves of the delay circuit. With a higher stage of output port and higher memristor value, the signal distortion will also be higher. For those curves that rise very fast with the increase of the input amplitude, their rising trends slow down at high input amplitudes, which is because when the signal distortion is large, the influence of signal deformation to the THD value becomes smaller compared with the condition when the signal distortion is small. Compared with the THD results of the GHz and MHz delay circuits, it is found the signal distortion in the memristor-directly-controlled circuit is worse. To make the THD of all the output ports smaller than 10%, the input signal amplitude should be maintained under 10mV.

The Monte Carlo simulation results of the memristor-directly-controlled delay circuit are listed in Table 4.20. Comparing the standard deviation values of this circuit with the GHz and MHz circuits, it is found that this circuit is more stable compared with the GHz and MHz circuits. This is because a voltage-controlled delay circuit includes a tuneable DC voltage source and a delay element, which has more circuit elements and more complex operation steps compared with a memristor-directly-controlled delay circuit. When more circuit elements join the work of the circuit, there will be a larger deviation in the fabricated circuit chip.

Table 4.21 records the change of the performance for the memristor-directly-controlled circuit in the conditions of transistor corners, temperature variation, supply voltage variation, and input DC voltage variation. The transistor ff corner will expand the working frequency range of the circuit, but reduce the tuneable delay range; By contrast, the transistor ss corner expands the tuneable delay range but reduces the working frequency range. The circuit shows good stability under different temperatures, with the gain, delay, and bandwidth having only very small changes. When the supply voltage reduces, the gain value and the frequency range of the circuit will be reduced, and the delay value increases; When the supply voltage increases, the gain and frequency range of the circuit increases, while the delay value reduces. Finally, increasing the DC input voltage will reduce the gain value and delay range but increase

Table 4.20: Monte Carlo results of the memristor-directly-controlled delay circuit

	Mean	Max	Min	Std Dev
Max gain (dB)	-0.06	0.26	-0.45	0.12
Min gain (dB)	-3	-2.47	-3.79	0.28
Max delay (ns)	4.38	5.28	3.39	0.34
Min delay (ns)	1.44	1.91	1.05	0.16

Table 4.21: Corner, temperature and voltage supply variation analysis of the memristor-directly-controlled delay circuit

	Gain (dB)	Delay (ns)	Bandwidth (MHz)
Normal	-3 $\sim$ 0	1.44 $\sim$ 4.38	1 $\sim$ 120
ff	-2.95 $\sim$ 0.05	1.03 $\sim$ 3.33	1 $\sim$ 142
ss	-2.63 $\sim$ 0.37	2.16 $\sim$ 5.78	1 $\sim$ 97
T:-20°C	-2.82 $\sim$ -0.18	1.51 $\sim$ 4.37	1 $\sim$ 118
T:85°C	-3 $\sim$ 0	1.42 $\sim$ 4.43	1 $\sim$ 116
VDD 1.7V	-4.42 $\sim$ -1.42	2.1 $\sim$ 5.21	1 $\sim$ 102
VDD 1.9V	-2.28 $\sim$ 0.72	1.19 $\sim$ 3.91	1 $\sim$ 130
Vin DC 1.15V	-2.66 $\sim$0.34	1.38 $\sim$ 4.48	1 $\sim$ 115
Vin DC 1.25V	-3.57 $\sim$ -0.57	1.59 $\sim$ 4.38	1 $\sim$ 124

the frequency range, and vice versa. In a word, the circuit is stable with the variation of temperature and input DC voltage, while the transistor corners and supply voltage variation will have more impact on the circuit performance. Comparing the results of this circuit with the voltage-controlled GHz and MHz circuits, the overall stability of the memristor-directly-controlled circuit is better than the voltage-controlled delay circuits. However, the voltage-controlled delay circuits can adjust their performance by changing the value of voltage Vn in the tuneable DC source(as shown in Figure 4.1 (a)). By doing this, they can maintain their characteristics at affordable values in nearly all the conditions, as shown in Table 4.8. Because of that, the stability of these two structures can not be compared directly.

As a conclusion, the memristor-directly-controlled delay circuit has a simpler structure, more linear output delay value, and better stability compared with the [memristor-controlled DC voltage source + voltage-controlled delay elements] structure in the previous sections. Besides, in the voltage-controlled delay circuits, to adjust the input DC voltage of the delay elements, there are capacitors between the output of the first stage delay element and the input of the second stage delay element, as shown in Figure 4.1. As the output DC voltages of the delay elements are float(from 600 to 700mV) and not suitable for the input of their output buffers, there are also capacitors to separate delay elements and their corresponding output buffers, hence for the 3-stage voltage-controlled delay circuit, there are totally 6 capacitors been used, which takes up a large space in the whole area of the circuit, as shown in the Appendix A Figure B.3. However, in the memristor-directly-controlled delay circuit, as the input DC voltage is constant, there is no capacitor needed to separate the different stage delay elements and their output buffers. As a result, the size of the memristor-directly-controlled delay circuit is only half of the [memristor-controlled DC voltage source + voltage-controlled delay elements] circuit.

The reason for not applying this memristor-directly-controlled delay circuit into the final tuneable delay circuit design is, that the working frequency of this structure is limited lower than around 100MHz by the memristor. As this chapter aims to research the applications of memristors in radio frequency devices whose working frequencies are higher than GHz, the memristor-directly-controlled delay circuit that works under 100MHz is finally abandoned. Besides, the high THD rising trend of this circuit structure also makes the circuit hard to work in practice. However, the research on the memristor-directly-controlled delay circuit expands the working frequency of applying multi-stage memristors in high-frequency environments from under 10MHz to around 100MHz. This circuit shows it is worth continuing the research on this type of memristor-directly-controlled high-frequency device in the future.

4.5 Design and Operation for Chip Testbench PCB

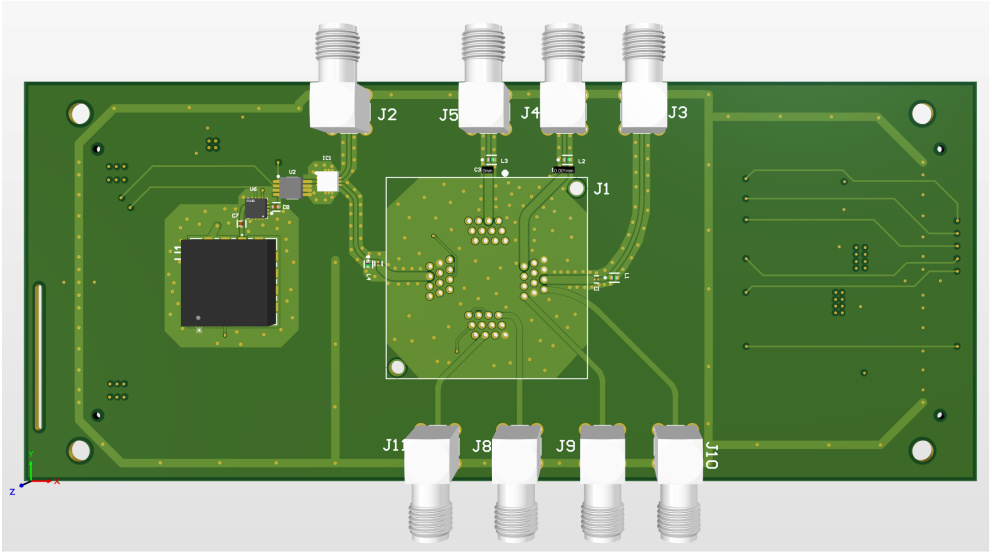
4.5.1 Introduction of the Testbench

This section introduces the PCB test bench designed for the tuneable delay circuit chip. To measure the circuit works in radio frequency, the PCB is designed with RF PCB rules instead of normal PCB rules. Except for the test bench PCB, the measurement of the tuneable delay chip also needs other instruments, including oscilloscope, tuneable DC voltage source, measurement FPGA ArCTwo, and vector network analyzer (VNA). In the following section, the structure and elements of the PCB are going to be discussed, and in the subsection Measurement Instrument Setting, the connection between the tuneable delay chip, test bench PCB and other instruments in the chip measurement will be introduced. The operations of different instruments in the measurement of the chip will also be discussed.

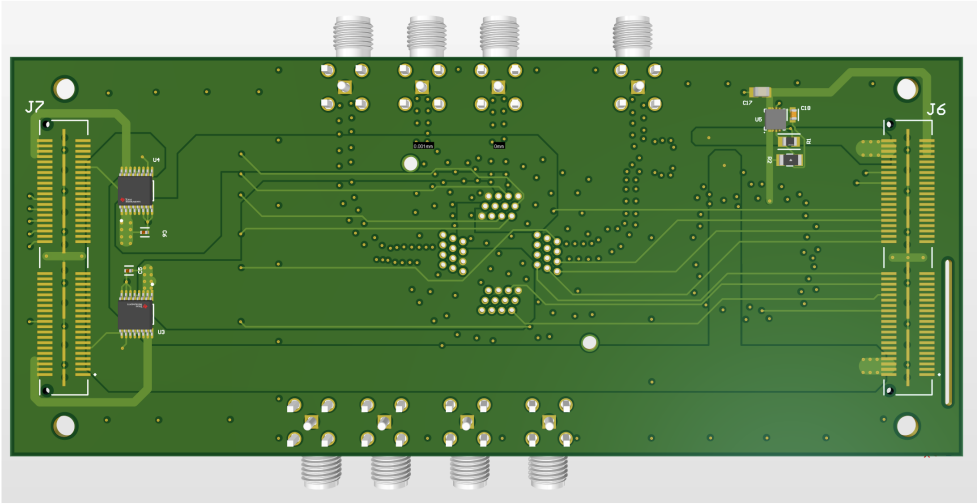
4.5.2 Testbench PCB Structure

Figure 4.16 shows the top and bottom view of the PCB layout. Table 4.22 lists all the components on the PCB. The tuneable delay chip has 32 pins and includes 4 pins with RF signals flowing through. The package of the chip in this project is QFN48. Quad-flat no-lead (QFN) package has a small size, low cost, good electrical and thermal performance. It reduces lead inductance and self-impedance compared with leaded packages, and is widely used in RF devices. A 48-pin package is chosen for the chip, as the space pins can separate the sensitive pins from other pins close to them. The chip hold socket is 248-5205-00, which is manufactured by 3M for 48-connect QFN packages. The chip socket $J1$ is only shown as a footprint in Figure 4.16. The PCB is designed with 4 stack layers, including top $\&$ bottom signal layers, and power $\&$ ground plane layers. The analog signals flow on the top layers, while digital signals and biasing voltages flow on the bottom layer. The ground and power plane are set in the middle to avoid the influence of digital signals on RF signals. To isolate the two signal layers comprehensively, dielectric layers are placed between the [top layer] / [ground plane] and the [power plane] / [bottom layer], and 3 dielectric layers are placed between the [ground plane] / [power plane].

The MHz part of the tuneable delay circuit has 4 AC signal pins, which are one MHz signal input pin and three output pins. The delay circuit includes a built-in voltage control oscillator (VCO) that works at around 10MHz to offer the input signal for the MHz delay part. If the built-in MHz VCO works well, the MHz signal input pin will send the signal generated by the MHz VCO to an external oscilloscope for measurement. However, if the built-in VCO doesn't work, the VCO will be turned off and the MHz signal input pin will send the input signal to the delay circuit from an external signal generator. The MHz external input signal can be generated by the oscilloscope or waveform generator. All the AC signal pins on the PCB connect to SMA connectors, which can connect to the cables of the oscilloscope easily.



(a)



(b)

Figure 4.16: (a) Top view and (b) bottom view of the PCB layout. The RF signal connectors and high-frequency-signal-related circuit elements are placed on the top layer, while the power supplies, digital signal paths, and connectors to ArC Two are placed on the bottom layer.

The GHz delay circuit also has 4 AC signal pins, with 1 input pin and 3 output pins. As the 4 pins work with RF signals, the design of the GHz test bench is more complex than the MHz test bench. In an RF device, the input and output impedance of the devices are normally set to 50Ω. In this project, at 1.6GHz, the input impedance of the GHz delay circuit is 9Ω, and the output impedance of the GHz delay circuit is 28Ω. All the GHz input and output pins are combined with impedance-matching networks consisting of inductors and capacitors, to match the impedance to 50Ω. All the GHz AC signal pins connect to SMA connectors with coplanar waveguides, to reduce the signal interference from the environment and other high-frequency signal routes. The GHz delay circuit has a built-in VCO on the chip as signal input, and another

Table 4.22: Components on the PCB

Component	Manufacturer	Description	Identifier
248-5205-00	3M	Chip socket	J1
73100-0114	Molex	SMA connector	J2 to J9
QSE-040-01-C-D-A	Samtec	ArCTwo Connector	J10, J11
CVCO55CW-0800-1600	Crystek Corporation	0.8 $\sim$ 1.6GHz VCO	U1
ADG918BRMZ-REEL7	Analog Devices	RF switch	U2
INA250A4PWR	Texas Instruments	Current Sense Amp	U3, U4
LT1964EDDPBF	Analog Devices	Voltage regulator	U5
HMC973ALP3E	Analog Devices	RF attenuator	U6
GRM0335C1E5R1CA01D	Murata Electronics	5.1pF capacitor	C1 to C3
GJM0335C1E3R9BB01D	Murata Electronics	3.9pF capacitor	C4
GRM155R71H103KA88	Murata Electronics	10nF capacitor	C5, C6, C10
C1005C0G1H101J050BA	TDK	100pF capacitor	C7, C8
GRM21BR61A106KE19	Murata Electronics	10uF capacitor	C9
RC2012F1152CS	Samsung	11.5kΩ resistor	R1
MCA1206MD1003BP100	Vishay/Beyschlag	100kΩ resistor	R2
LQG15HN2N4S02D	Murata Electronics	2.4nH inductor	L1 to L3
LQG15HS5N6S02D	Murata Electronics	5.6nH inductor	L4

VCO offers signals from 800 MHz to 1.6GHz is set on the PCB as an auxiliary input signal generator. An RF switch is placed at the output of the auxiliary VCO. When the built-in VCO of the GHz delay circuit works well, the RF switch and the auxiliary VCO turn off, the signal from the built-in VCO flows to the delay circuit and the SMA connector for measurement. If the built-in VCO doesn't work, the RF switch and auxiliary VCO turn on, and the signal from the VCO flows to both the chip and the SMA connector. As the signal from the auxiliary VCO needs to flow in two directions, a power splitter is placed between the RF switch, SMA connector and the input pin of the chip, to reduce signal distortion and reflection. The peak-to-peak signal amplitude of the auxiliary VCO output is 3V. This voltage is reduced by half when it passes through the power splitter and flows in two directions. However, the 1.5V peak-to-peak signal is still too large for the input of the chip. To deal with it, an RF attenuator is added to the VCO output. when offering 2.8V biasing voltage to the attenuator, it can offer around -18dB to the signal, making the input signal amplitude of the chip reduce to around 25mV.

Both the tuneable delay chip and the PCB use two supply voltage levels 1.8V and 5V. To separate the power supply of the chip from the PCB, two power ports are used to offer the two voltage levels for the chip, and the other two power ports are set to supply power for PCB circuit components. Two current sense amplifiers with shunt resistors are placed at the power ports for the chip. The current sense amplifier can measure the current flows through the shunt resistor without affecting the work of the chip. The measured current value is shown as a voltage value with a gain of 2V/A. Combine the measured voltage level of 1.8V or 5V with the current in the roads, the power consumption of the 1.8V circuit and 5V circuit in the chip can be measured.

The power supply, control signal and biasing voltage of the PCB are offered by FPGA board ArCTwo. ArcTwo is a measurement instrument which suitable for reading and writing RRAM crossbar arrays. It can also offer biasing voltage from the analog channel signal ports, 1.8V & 5V voltage from power supply ports, and -15/+15V fixed voltage supplies. In this research, the biasing voltages, and 1.8V control signals are offered by the analog channel signal ports of ArCTwo, 5V digital signal input and output are connected to the digital channel ports. The programming of memristor, including the writing pulse generation and reading of memristor value, is also supplied by ArCTwo. The work of the GHz auxiliary VCO on the PCB needs a supply voltage of 11.5V and a frequency turning voltage of up to 19V. To supply the large voltage, the power pin of VCO is connected to the ground of ArCTwo, the -15V port of ArCTwo combines with a -11.5V voltage regulator connected to the ground of VCO, and uses an analog channel to offer 0 to 7.5V turning voltage. In this case, the voltage difference between the power and ground port of the VCO is 11.5V, and the turning voltage on the VCO is 11.5V to 19V, allowing the output signal frequency of the VCO to vary from 1.2MHz to 1.6MHz. $J10$ and $J11$ are the connectors between the PCB and ArCTwo, which are set at the bottom layer of the PCB and shown as footprints.

4.5.3 Measurement Instrument Setting

The tuneable delay circuit has mainly two work modes, which are memristor programming mode and delay circuit working mode. The delay circuit working mode can also be separated into GHz delay mode and MHz delay mode. For all these working modes, the PCB connects with ArCTwo to get power and control signals. In memristor programming mode, the PCB board only connects to ArCTwo, leaving all the SMA connectors space. In GHz delay mode, the four GHz signal SMA connectors connect to the vector network analyzer, to measure the gain and phase change between the input and 3 outputs, with all the MHz SMA connectors space. In MHz delay mode, the four MHz signal SMA connectors connect to an oscilloscope for measurement, leaving all the GHz SMA connectors space.

Table 4.23: Input and output signal of ArCTwo

	Signal	Description	Value
ArCTwo Output Power Supply	VDD1.8	Power supply for chip	1.8V
	VDD5	Power supply for chip	5V
	VDD1.8PCB	Power supply for PCB	1.8V
	VDD5PCB	Power supply for PCB	5V
ArCTwo Output Signal	Osc Ctrl	Turning voltage for VCO	0 to 7.5V
	GHz input Ctrl	Control signal for RF switch	0 / 5V
	Vregulator	Voltage bias for regulator	2.8V
	Switch	Switch MHz/GHz circuit	0 / 1.8V
	Switch OscGHz	Integrated oscillator switch	0 / 1.8V
	Switch OscMHz	Integrated oscillator switch	0 / 1.8V
	DC 1	Biasing voltage for chip	0.55 $\sim$ 0.75V
	DC 2	Biasing voltage for chip	0.55 $\sim$ 0.75V
	DC 3	Biasing voltage for chip	0.55 $\sim$ 0.75V
	Vn	Biasing voltage for chip	0.85V
	Pulse	Memristor programming pulse	0 / 5V pulse
	Data IN	Memristor programming code	0 / 5V digital
	CLK	Clock signal	0 / 5V digital
	Load	One pulse digital signal	0 / 5V
	Enable	Enable switch signal	0 / 5V
ArCTwo Iuput Signal	Data OUT	Programming code feedback	0 / 5V digital
	I result1.8	Current value in 1.8V circuit	0$\sim$1V
	I result5	Current value in 5V circuit	0$\sim$1V

All the control signals and biasing voltages are offered by the ArCTwo. Besides, the digital data output of the chip and the measured currents in the 1.8V and 5V circuits are also read by ArCTwo. Table 4.23 lists the input and output signal and biasing voltages of ArCTwo.The power supplies offered by ArCTwo are constant, and the input/output signal operations change with different working modes of the tuneable delay circuit.

Table 4.24: Signal operation in memristor programming mode

	Signal	Step 0	Step 1	Step 2	Step 3
Changed Signal	Pulse	Off	Off	Off	On
	Data IN	Off	On	On	Off
	CLK	Off	On	On	Off
	Load	Off	Off	On	Off
	Enable	Off	Off	Off	On
	Data OUT	Off	Off	On	Off
Constant Signal	Osc Ctrl	0	0	0	0
	GHz input Ctrl	0	0	0	0
	Vregulator	2.8	2.8	2.8	2.8
	Switch	0	0	0	0
	Switch OscGHz/MHz	1.8	1.8	1.8	1.8
	DC1∼3	0	0	0	0
	Vn	5	5	5	5
	I result1.8/5	On	On	On	On

Memristor Programming Mode

The signal operation in memristor programming mode is shown in Table 4.24. Step 0 turns off the delay circuits, the built-in oscillators and the external VCO on the PCB, making the circuit ready for memristor programming. Referring to Figure 4.2, in Step 1, [CLK] and [Data IN] turn on to send commands into the programming controller circuit. [Data OUT] starts reading the code at the sixth clock signal. In Step 2, [Load] turns on for one pulse to save the previous command to the second flip-flop layer. [Data OUT] finishes the code reading. [Data IN] sends an all-0 command to the programming controller and resets the first layer flip-flops. After the command from [Data OUT] is checked correctly, in step 3, the [Enable] signal turns on and then [Pulse] turns on to start the programming for the chosen memristor. The memristor value is measured in real-time by measuring the voltage / current ratio in the Pulse port of ArCTwo. When the memristor reaches the wanted resistance, the [Pulse] signal turns off first to set the voltage on the memristor to a low value, and then [Enable] turns off to finish the programming. In this case, the circuit back to the Step 0 condition and waits for other operations. Figure 4.17 shows an example of signal operations with input code 100000, which programs the third memristor from the direction up to down. This research does not aim to reach high-speed memristor programming, hence signals [Data IN], [CLK], and [Lord] are set with 500ns pulse width, and the memristor programming pulse has 100ns pulse width.

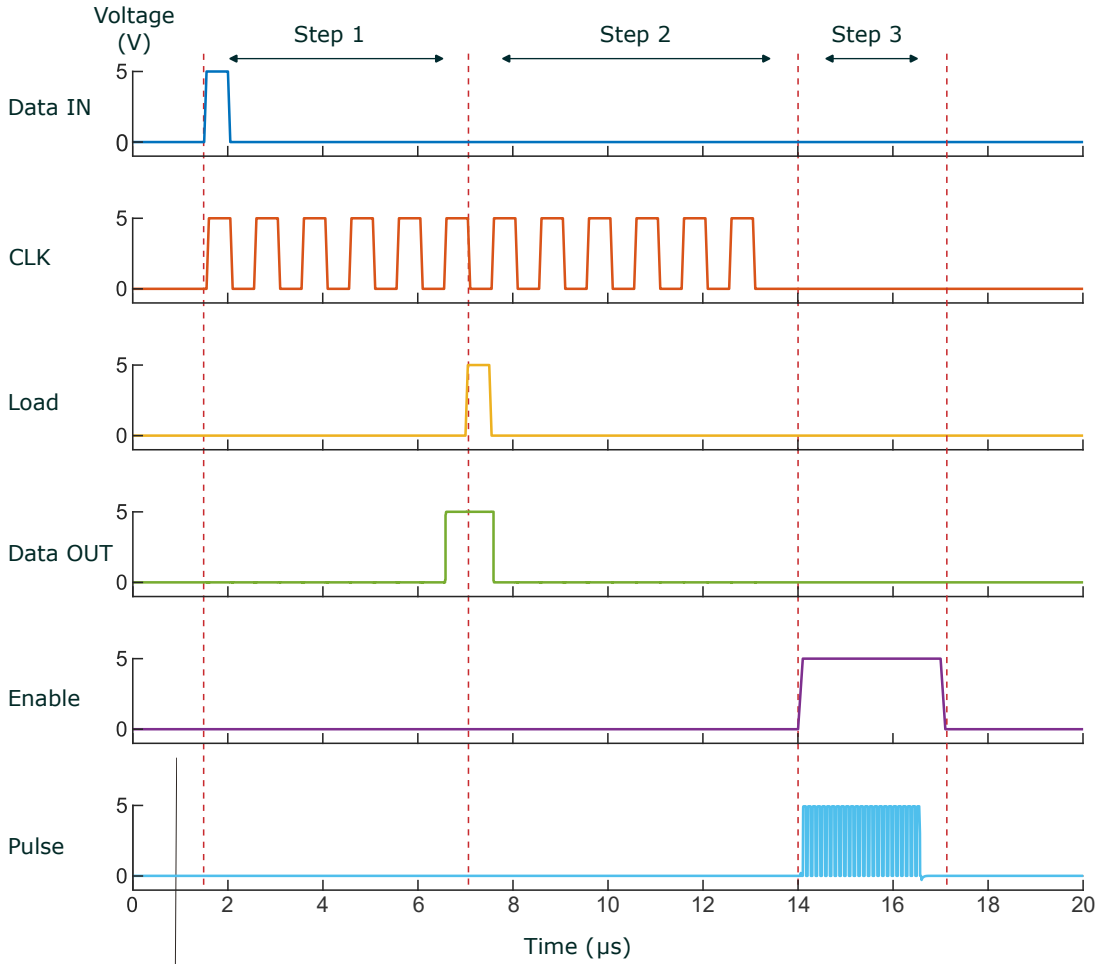


Figure 4.17: Memristor programming signals with input code 100000. Step 1: [Data IN] sends the command to the first flip-flop layer. Step 2: [Load] save the command to the second flip-flop layer. Step 3: [Enable] starts the programming of the chosen memristor.

Delay Circuit Working Mode

Table 4.25 shows the signal operation when the circuit is in delay circuit working mode. During the working of the delay circuit, all the signals remain constant. Some of the signals are fixed in all the conditions. [Vregulator] signal always offers 2.8V DC voltage to the regulator on the PCB, and maintains the negative voltage level for the VCO on PCB. Digital signals turn off in delay circuit working mode, and [I result] ports turn on to measure the currents, hence the power consumption can be calculated. However, 3 working conditions need to be set up before the circuit starts working, and some signal values vary with different conditions.

First, the circuit should be set to work with the MHz delay circuit or GHz delay circuit. Second, the engineer should choose to use the built-in MHz / GHz oscilloscope to offer the input AC signal, or use external signal sources to generate the input AC signal. Two built-in VCOs work in 10MHz and 1.6GHz are integrated into the tuneable delay circuit, which can generate the

Table 4.25: Signal operations on delay working mode

	Signal	Value
Signal Vary with Condition	Switch	Depends on MHz/GHz circuit selection
	Osc Ctrl	Depend on built-in Oscillator / PCB VCO selection
	GHz input Ctrl	
	Switch OscGHz	
	Switch OscMHz	
	DC 1∼3	Depend on built-in DC source/ArcTwo DC voltage reference selection
	Vn	
Fixed Signal	Vregulator	2.8V
	Pulse	Off
	Data IN	Off
	CLK	Off
	Load	Off
	Enable	Off
	Data OUT	Off
	I result1.8	On
	I result5	On

wanted input signal for the delay circuits. However, if the built-in VCOs don't work, auxiliary external signal sources are prepared to offer input AC signals. Third, a decision needs to be made about using built-in memristor-based DC sources to generate DC voltage for the delay circuit or using ArCTwo channels to offer DC voltages to the circuit. Generally, the memristor-based DC sources can offer DC voltages to the delay circuit, and the DC voltage levels are measured by ArCTwo from DC 1∼3 ports. When the memristor-based DC sources don't work, ArcTwo would output DC voltages to the delay circuit from DC 1∼3 ports, to maintain the normal functions of the remaining circuits and allow their performance to be tested.

The signal operations in the first and second working condition settings are shown in Table 4.26. The [Switch] signal controls the circuit to work in the GHz or MHz frequency range. When the [Switch] signal is 0V, the GHz delay circuit turns on and the MHz part turns off; When the [Switch] is 1.8V, the MHz circuit turns on and the GHz part turns off. [Switch OscGHz] and [Switch OscMHz] control the built-in GHz/MHz VCOs. when they are set to 1.8V, the built-in VCOs turn off; Oppositely when they are 0V, the built-in VCOs they control are turned on. [Switch OscGHz] sets to 0V only when the circuit works in GHz and built-in GHz VCO is chosen. In the same way, [Switch OscMHz] sets to 0V only when the circuit works in MHz and built-in MHz VCO is chosen. The external signal source for the GHz circuit is the GHz VCO on the PCB, and the external signal source for the MHz circuit is a waveform generator

Table 4.26: Signal operations in GHz/MHz circuit selection and built-in/external signal source chosen

	Built-in VCO		External signal source	
	GHz work	MHz work	GHz work	MHz work
Switch	0V	1.8V	0V	1.8V
Osc Ctrl	0V	0V	0 $\sim$ 7.5V	0V
GHz in Ctrl	0V	0V	1.8V	0V
Switch OscGHz	0V	1.8V	1.8V	1.8V
Switch OscMHz	1.8V	0V	1.8V	1.8V

Table 4.27: Signal operations in DC source chosen

Signal	Built-in DC Source	ArcTwo as DC Source
DC 1$\sim$3	Measure DC voltage	0.55 $\sim$ 0.75V
Vn	0.85V	1.8V

instrument in the laboratory. When an external signal source is needed for the GHz circuit, the [GHz input Ctrl] signal is set to a high voltage level to turn on the RF switch at the output of the GHz VCO on the PCB, and the [Osc Ctrl] signal varies to adjust the frequency of the signal. When using a waveform generator instrument as the external MHz signal source, the [Osc Ctrl] and [GHz input Ctrl] signals turn off, [Switch OscGHz/MHz] signal set to 1.8V, and the SMA connector of the MHz input port on the PCB connects to both the waveform generator and the oscillator, to measure the input signal of the delay circuit.

The signal operations related to the third working condition setting are shown in Table 4.27. When built-in memristor-based DC sources are working, the [Vn] signal is set to 0.85V to maintain the wanted output voltage range of the DC sources, and ArcTwo measures the output voltage levels of the DC sources from [DC 1$\sim$3] ports. When built-in DC sources don't work, [Vn] sets to 1.8V to turn off the DC sources. At the same time, ArcTwo offers DC voltages to the delay circuit from the [DC 1$\sim$3] ports.

4.6 Conclusion

In this chapter, a reconfigurable delay circuit controlled by memristor-based DC voltage sources is reported. The memristor-based DC source offers DC voltage from 584mV to 711mV with high resolution. The GHz delay circuit works in a frequency range from 50MHz to 1.6GHz, and it offers an output delay range from 269ps to 632ps, with only 0.4ps minimum resolution. A delay circuit working at low MHz was also simulated to compare with the GHz circuit. The MHz delay circuit can work from 200kHz to 10MHz, and offers a tuneable delay in a range of [13, 55]ns, with 50ps minimum resolution. The memristor programming circuit for changing the memristor resistance is also introduced. This research shows the potential of memristors in reconfigurable analogue and RF devices: by using memristors in tuneable voltage or current sources, and designing circuits which can be controlled by voltage/current, memristors can introduce elegant and fine-grained reconfigurability even in circuits operating at very high frequencies.

The tuneable delay circuit chip has been sent to the factory and is now in tape-out progress. The design of a PCB board for measuring this chip is also discussed. The necessary elements, the power supplies & control signals of the PCB, and the required external measurement devices are listed, and the operations of the PCB in measurement progress with different models are also discussed. ArC Two board is chosen to offer all the power and control signals for the PCB, vector network analyzer and oscilloscope are used to measure the output signal from the chip.

For further work, the next step of this research is to measure the chip with the PCB in the laboratory after the chip is sent back. After the performance of the chip is measured, the delay circuit can be improved to get a larger delay range, or work at higher frequencies. If the chip didn't work well in the measurement, first the PCB design needs to be checked, and then the delay circuit may need to be redesigned to make it work in practice. The experience of chip measurement in practice is important for circuit designers, and can help me a lot in my studying and working career. Besides, Chapter 5.4.2 discussed a memristor-directly-controlled delay element structure that uses a memristor in the high-frequency circuit directly, which also shows good potential. In the future, by using memristor elements that have small parasitic capacitance, research in memristor-directly-controlled high-frequency devices will also get good results.

Chapter 5

Memristor-based N-path Filter

5.1 Introduction

With the development of modern wireless communication technologies, reconfigurable filters are widely used in radio transceivers. In all the filter design solutions, the N-path filter structure is one of the designs which have high linearity, high quality factor suitable for integrating on-chip with CMOS technology and a high potential for transformation [116] [117] [118]. A large amount of research has been done to design reconfigurable band-pass filters based on the original N-pass filter structure, including using a tunable local oscillator to adjust the centre frequency of the filter and using switched-capacitor or other structures to adjust the bandwidth [119] [120] [121] [122] [123] [124].

Memristors are a type of two-terminal non-volatile electronic circuit element, which can save the history of the voltage applied to it in its resistance level. Because of this characteristic, it can be used as a programmable resistor. Some of the research has been done to combine memristor crossbars with reconfigurable filters [125] [126]. In this research, instead of using memristor crossbars and arrays, one or a small number of memristors are applied to the basic N-path filter structure, to adjust the bandwidth of the filter.

In this chapter, the methodology part shows two different schematics of the N-path filter combined with the memristor, and discusses the functions of the N-path filter after adding the memristor. In the Result section, first, the simulation results of the two structures of the N-path filter were compared. Then one of the N-path filters was built on a stripboard and combined with a memristor package in the laboratory, the measurement results were recorded. In the discussion section, the drawbacks of the measured N-path filter structure with memristor were listed, and the third N-path filter structure which combines multiple memristors was discussed, and the simulation results were listed.

5.2 Design and Methodology

5.2.1 Functions of Basic N-path Filter

The basic schematic of a 4-path filter is shown in Figure 5.1 [127]. For convenience, this circuit is called Schematic 1 in the following sections. Capacitors C1 to C4 have the same value. Switches S1 to S4 turn on sequentially as shown in Figure 5.1, with all the pulse widths T_{on} the same and equal to 1/4 period of the switch control signals. As only one switch turns on at any moment, the basic working model of the circuit is an RC low pass filter in transient.

When the input signal frequency f_{in} equals the switch signal frequency f_s, every time one of the switch S turns on, the corresponding capacitor C faces the same part of the input sine wave, as shown in Figure 5.1 (b). Assume RC $\gg T_{on}$, with enough time pass, the voltage on the capacitor will be a constant DC value which equals the average voltage of that part of the sine wave. Combining the voltages on the 4 capacitors in sequence, a sampled wave is

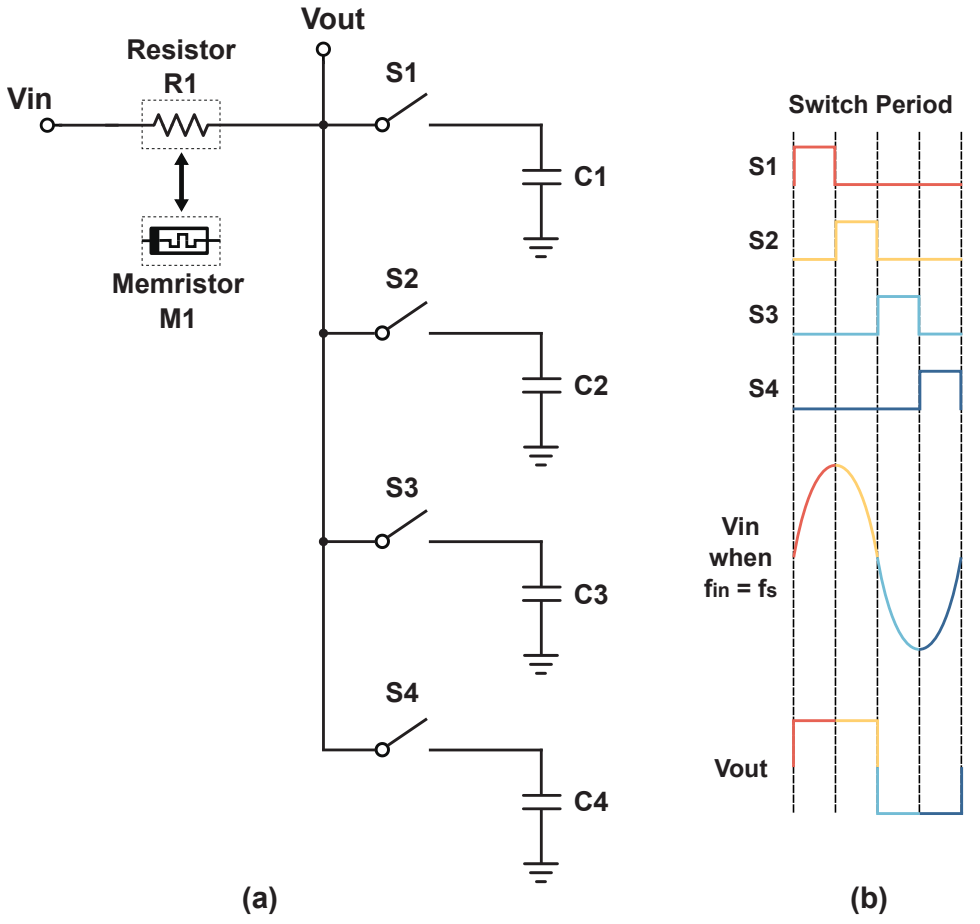


Figure 5.1: (a) Schematic of a 4-path filter and the condition of replacing the resistor with a memristor. (b) Waveform of the switches S1 $\sim$ S4, Vin when $f_{in} = f_s$, and Vout in one period of switch signal.

generated at the Vout node [117]. A simple 4-path filter samples the signal with 4 parts per period. To sample the signal finer, a higher-order N-path filter, like an 8-path or 16-path filter can be chosen. When the f_{in} is different from f_s, capacitors will face different parts of the input sine wave at different periods. The different parts of the wave will neutralize each other, hence the average DC voltage stored on the capacitors will be smaller, resulting in a smaller gain at the Vout node compared with the condition when f_{in}=f_s. Because of this characteristic, the N-path filter works as a band pass filter whose centre frequency equals the switch frequency f_s, while the bandwidth is decided by the value of R, C, and the number of paths.

Equation 5.1 shows the relationship between resistor value, capacitor value, path number and -3dB bandwidth of the N-path filter [128] [129] [130]. The function of quality factor Q is shown in Equation 5.2, which equals to the ratio between centre frequency and -3dB bandwidth. The benefit of the N-path filter is the centre frequency controlled by the digital clock can be very high, which forms a very large quality factor value when combined with a small bandwidth decided by the resistor and capacitor values.

Although the centre frequency of an N-path filter can be controlled by adjusting the digital clock, the bandwidth is fixed by the values of the resistor and capacitor, thus the quality factor of an N-path filter varies when the centre frequency changes. To make the bandwidth adjustable, one memristor is used to replace the resistor in the N-path filter, to generate a reconfigurable N-path filter whose bandwidth can be adjusted by the memristor resistance, as shown in Figure 5.1 (a). By changing the memristor value, the quality factor of the filter can be maintained at a constant value in a range of centre frequency. The range of the centre frequency in which the reconfigurable N-path filter can maintain a constant Q factor is decided by the tuneable range of the memristor.

$$f_{-3dB} = \frac{1}{\pi NRC} \tag{5.1}$$

$$Q = \frac{f_s}{f_{-3dB}} = \pi NRCf_s \tag{5.2}$$

Before adding the memristor to the N-path filter, the transfer function of the original N-path filter needs to be explained. Assume the switch S1 turns on, at this moment, the memristor works as a low pass filter with resistor R and capacitor C. The function of an ideal filter in which the ON resistance of the switch is ignored is shown as equation 5.4. For a filter in reality in which the ON resistance R_o of the switch is included, the transfer function shows in equation 5.5. When the frequency is very large, the gain of the filter will tend to a constant value which equals the ratio R_o/R. Combine equation 5.3 and 5.5, the memristor-controlled filter bases on the schematic in Figure 5.1 has the transfer function shown as equation 5.6. Equation 5.7 expresses the condition of equation 5.6 when the frequency is very large, which

shows the gain tends to 1 when the frequency approaches infinite, and the circuit becomes a band-stop filter instead of a low pass filter. On the other hand, this schematic also does not allow the memristor to be programmed. To combine the memristor with the N-path filter, some adjustments need to be made to the schematic.

$$Z_m = \frac{1}{\frac{1}{R} + sC_p} \tag{5.3}$$

$$H(s)_{[ideal]} = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} = \frac{1}{1 + sRC} \tag{5.4}$$

$$H(s)_{[+R_o]} = \frac{R_o + \frac{1}{sC}}{R + R_o + \frac{1}{sC}} = \frac{\frac{1+sR_oC}{sC}}{R + \frac{1+sR_oC}{sC}} = \frac{1}{1 + \frac{sRC}{1+sR_oC}} \tag{5.5}$$

$$H(s)_{[+Memristor]} = \frac{1}{1 + \frac{sZ_mC}{1+sR_oC}} = \frac{1}{1 + \frac{sRC}{(1+sR_oC)(1+sRC_p)}} \tag{5.6}$$

$$H(s)_{[+Memristor][f\to\infty]} \approx \frac{1}{1 + \frac{1}{sR_oC}} \tag{5.7}$$

There are mainly two things that need to be considered when combining memristors in the existing circuits. First, memristors are not ideal tuneable resistors. The lumped element model of a memristor can be seen as a resistor R in parallel with a parasitic capacitor C_p. The impedance Z_m of a memristor can be expressed by equation 5.3. Second, the memristor has both dynamic and static resistance variation characteristics. The dynamic characteristic means the memristor resistance will change when a large voltage is applied to it from the same direction continuously. This characteristic is the base of using a memristor as a tuneable resistor. The static characteristic is, when the voltage on the memristor is relatively large, the memristor will show a non-linear I-V curve, which means the memristor will show different resistances with different voltage on it. The larger the voltage on the memristor, the smaller the resistance level that memristor shows. Because of these characteristics, a memristor requires a small voltage (the best $\leq$0.5V) on it to have a constant resistance value in normal work, and large voltage pulses ($\geq$1.2V) for resistance stage programming.

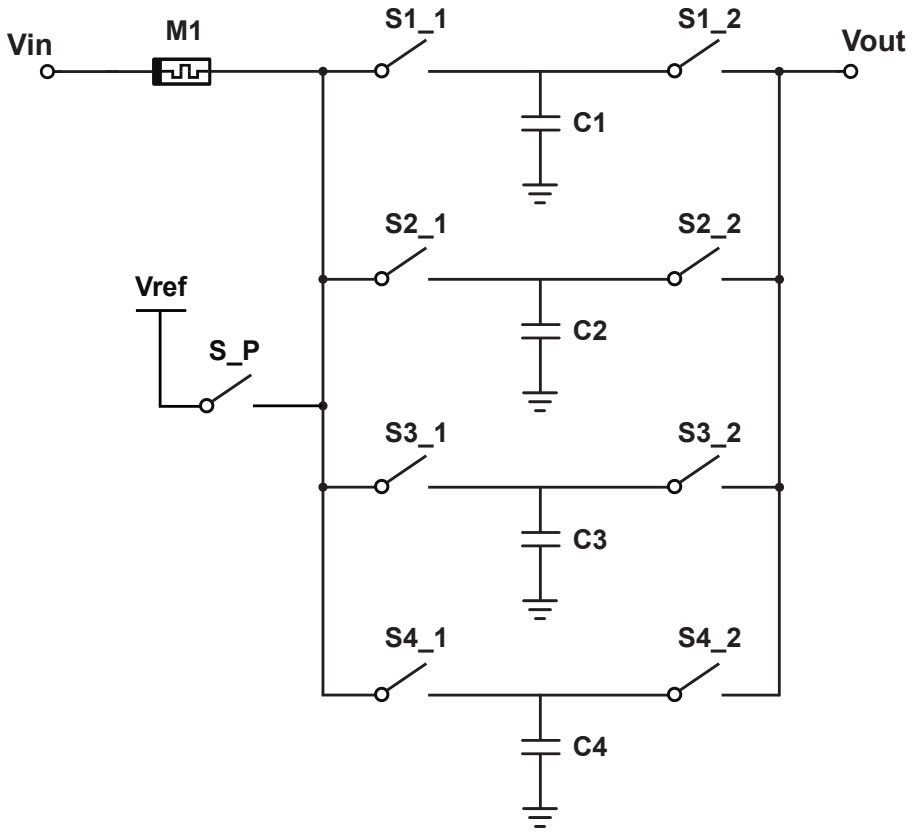


Figure 5.2: Schematic of memristor-based reconfigurable 4-path filter. A memristor is used to take the place of the resistor in a normal N-path filter structure, and a pair of switch elements are used in each signal path.

5.2.2 One-memristor-based N-path Filter

Figure 5.2 shows the modified memristor-based 4-path filter, which is called Schematic 2 in the following sections. The basic concept of the schematic in Figure 5.2 is the unsimplified version of the N-path filter [127]. As the capacitors will get most of the DC voltage from the input signal, the DC voltage on the memristor should be very small, hence the memristor can maintain a constant resistance level in normal work. To make sure the memristor works in a safe environment, the DC voltage of the input signal is set to 0.5V. The circuit also adds 4 extra switches S1_2 $\sim$ S4_2, and the position of output node Vout is varied. The switches Sx_1 and Sx_2 are controlled with the same signal, and will turn on and off simultaneously. With the schematic shown in Figure 5.2, when a pair of switches Sx_1 and Sx_2 turn on, the transfer function of the filter is shown in equation 5.8, where R_{out} is the output resistance of Vout node. As Vout is assumed to connect with the gate of transistors, R_{out} will be very large and can be considered as open circuit. In this condition, when the parasitic capacitance of memristor C_p is very small and frequency is not very large, the circuit transform function is approximate to equation 5.9, which shows the circuit is working as a low pass filter.

Table 5.1: Vin, Vref, S_P and switches group operations of memristor-based 4-path filter Schematic 2.

	Vin	Vref	S_P	S1 to S4
Normal Work	0.5V DC + AC signal	0V	OFF	ON in sequence
Programming Mode 1	2.5V Pulse	0V	ON	OFF
Programming mode 2	0V	2.5V Pulse	ON	OFF

$$H(s)_{new} = \frac{1}{1+sR_oC+\frac{sRC}{1+sRC_p}} \times \frac{R_{out}}{R_o+R_{out}} \approx \frac{1}{1+sR_oC+\frac{sRC}{1+sRC_p}} \tag{5.8}$$

$$H(s)_{new[C_p \to 0]} \approx \frac{1}{1+s(R+R_o)C} \tag{5.9}$$

$$H(s)_{new[f \to \infty]} \approx \frac{1}{1+sR_oC+\frac{C}{C_p}} \tag{5.10}$$

An additional voltage node Vref is placed with a switch S_P for memristor programming. In normal work, Vin inputs an AC signal with an offset DC voltage of 0.5V, S_P turns off and Vref is set to 0V. In this case, ideally the Vref and S_P path is considered as an open circuit, and the filter works as a normal N-path filter. In memristor programming mode, all the switches S1_1 to S4_2 turn off, S_P turns on, and high-voltage pulses can flow between Vin and Vref, to change the resistance value of the memristor. The operations of the Vin, Vref ports, S_P, and S1 to S4 switches groups are listed in Table 5.1. Programming mode 1 shows the condition of programming the memristor from left to right, and programming mode 2 is the condition of programming the memristor from right to left. There is no speed requirement for the memristor programming in this research, hence the memristor programming pulse is set to have a duty of $100\mu s$.

In theory, the Schematic 2 circuit in Figure 5.2 can work at a higher frequency compared with the Schematic 1 in Figure 5.1. However, Equation 5.10 shows that when C_p is large, the gain of the filter is no longer influenced by the resistance of the memristor but is determined by the values of R_o, C and C_p. In this case, the Schematic 2 circuit still can not be used in radio frequency.

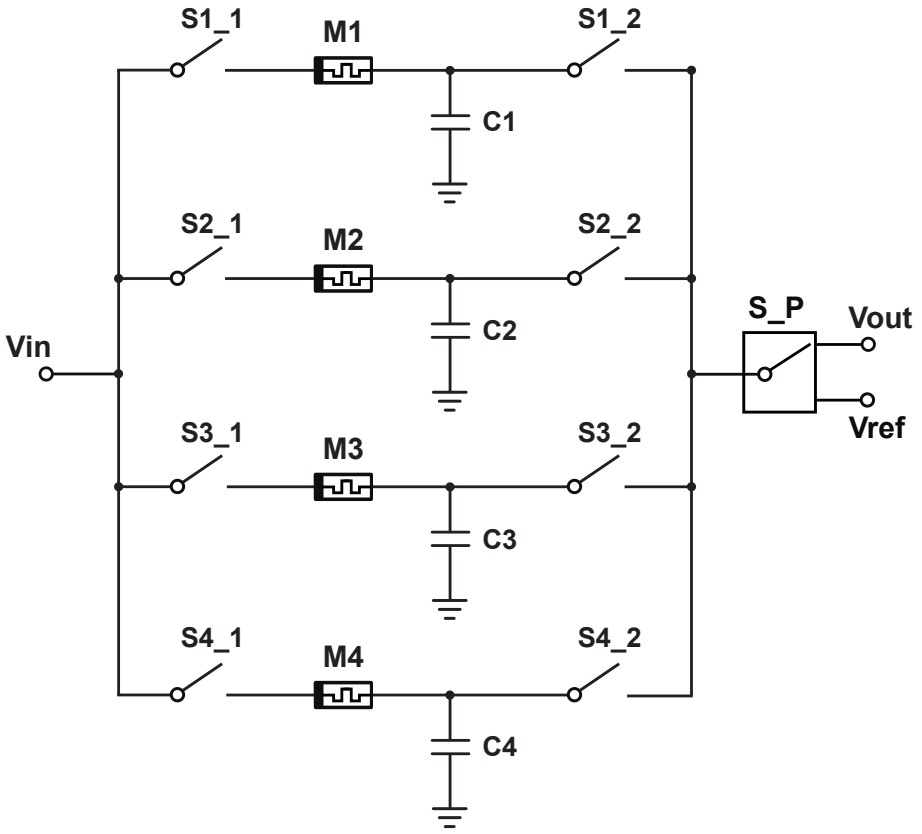


Figure 5.3: Schematic of high frequency memristor-based reconfigurable 4-path filter. Memristors are placed in all the signal paths, in between the switch groups, to make sure they can work in the DC environment when the input signal frequency equals the centre frequency of the filter.

5.2.3 Multiple-memristor-based N-path Filter

To make the memristor-based N-path filter work at high frequency, one of the solutions is to add memristors in between each of the switch groups, as shown in Figure 5.3, which is called Schematic 3 in the paragraphs below. Referring to the concept of memristor discussed above, the N-path filter "moves" the RC low pass filter to high frequency. When the input signal frequency equals the switching frequency, by controlling the switches and making each of the capacitors "see" the same part of the signal, the capacitors work in DC condition and save the average DC voltage of the parts of the signal they face. However, in Schematic 1 and Schematic 2, the resistor is still working with the original high-frequency signal. When replacing the resistor with a memristor in Figure 5.2, the impedance of the memristor reduces with the increases of signal frequency, hence the tuneable f_{-3dB} range will be smaller than expected. In Figure 5.3, by placing memristors in between [Sx_1, Sx_2] switch groups, memristors also only face a part of the signal and work in DC condition, hence the influence of C_p is nearly eliminated.

When Programming the memristors in Figure 5.3, the Vin and Vref settings are the same as the conditions shown in Table 5.1. However, S_P becomes a single-port-double-through(SPDT) switch, to choose the connection between the main circuit to the output port in normal work or to the Vref port in the programming mode. Besides, different from the programming operations in Schematic 2, when programming one memristor in Schematic 3, the corresponding switch groups need to be turned on, and all the other switch groups should be turned off.

5.3 Simulation and Measurement Results

In the result section, first the simulation results of Figure 5.1 and 5.2 Schematics with resistor and memristor will be shown and compared, to see the difference in the high-frequency performance of these two structures. Next, a 4-path filter built on a stripboard with the Schematic 2 circuit structure was measured in the laboratory with a 1MHz input signal and memristor array package. Finally, the simulation results of a memristor-based 4-path filter with the Schematic 3 circuit structure and 1GHz switch signal will be analyzed.

The switches in all the simulations have 500Ω ON state resistance without otherwise specified. The memristor model used in the simulations of this research has 10kΩ to 17kΩ resistance under 0.5V DC voltage [112], and is assumed to have a parasitic capacitance of 10pF.

5.3.1 Simulation Result with 1MHz centre frequency

The gain of the circuits built with normal resistor and memristor, and with different Schematic structures are shown in Figure 5.4. The results are simulated with resistor and memristor at 10kΩ, with capacitors 6nF and 1MHz switch frequency. It can be found that except the gain pass band at 1GHz, there are extra gain peaks at 2GHz, 3GHz and 5GHz. These are the 2nd, 3rd and 5th harmonic frequencies of the fundamental frequency. Reference to Figure 5.1 (b), when the input signal frequency equals to twice the switching frequency(f_{in}=2f_s), S1 and S3 will always record the average value of the positive cycle of the sine wave, S2 and S4 will always record the value of the negative cycle of the sine wave, hence the gain at f_{in}=2f_s is also high compares to the other frequencies. Same thing happens when f_{in} equals to 3f_s and 5f_s. However, when f_{in}=4f_s, every switches record the average value of a whole sine wave cycle, which equals to 0V. Because of that, there is no gain peak at 4GHz in Figure 5.4. For the original N-path filter with a resistor, Schematic 1 has a higher noise floor (at around -28dB) compared with Schematic 2, but also has a simplified circuit structure which reduces the number of switches. However, when replacing the resistor with the memristor, the result shows the noise floor of the gain in Schematic 1 will continue to increase with frequency, which means Schematic 1 with the memristor works as a high pass filter at high frequency.

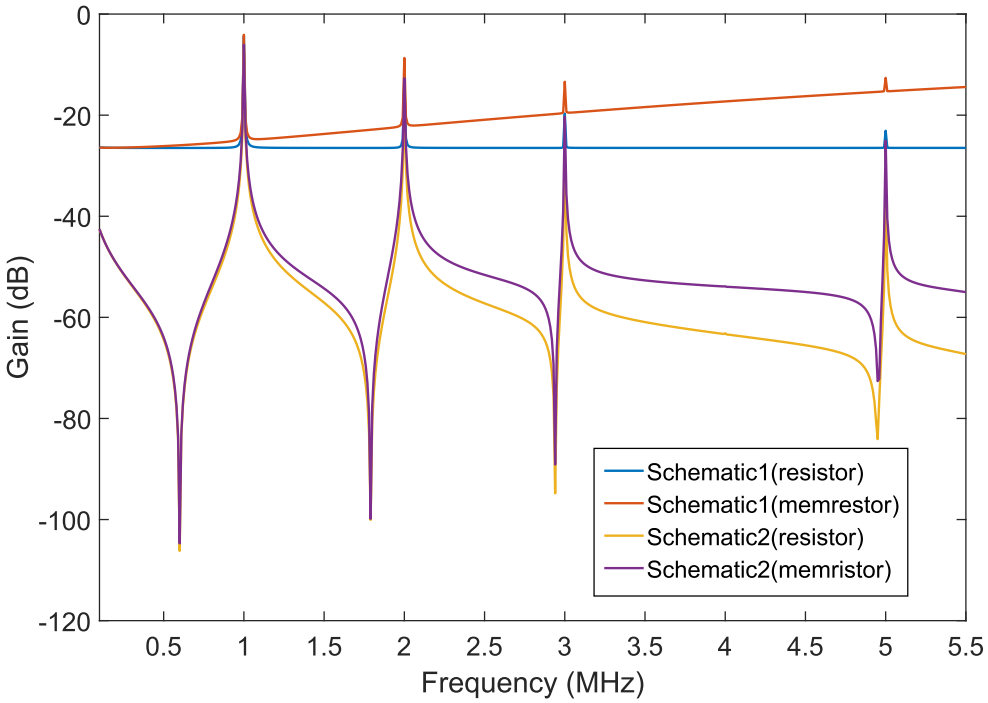


Figure 5.4: Gain of the circuits with Schematic 1 / Schematic 2, and with resistor / memristor. The [Schematic 1 + memristor] structure has a noise floor that increases with frequency. Schematic 2 structure shows a better noise floor than Schematic 1.

In Schematic 2, the memristor result has a higher noise floor compared with the resistor result, but the noise floor of the curve with the memristor maintains a constant value smaller than -40dB. The comparison results show Schematic 2 is more suitable for combining with a memristor to generate a reconfigurable device.

Table 5.2: Cut off frequency (f_{-3dB}) & quality factor (Q) with different memristor value, and centre frequency (f_c) range when quality factor maintains at 1000.

Memristor (Ω)	f_{-3dB} with resistor (Hz)	Actual f_{-3dB} (Hz)	Q factor	f_c with Q=1k (Hz)
10k	1105	1191	839	1.19M
11k	1053	1140	877	1.14M
12k	1007	1095	913	1.1M
13k	964	1059	944	1.06M
14k	935	1027	973	1.03M
15k	906	1000	1000	1M
16k	880	975	1025	975k
17k	857	954	1048	954k

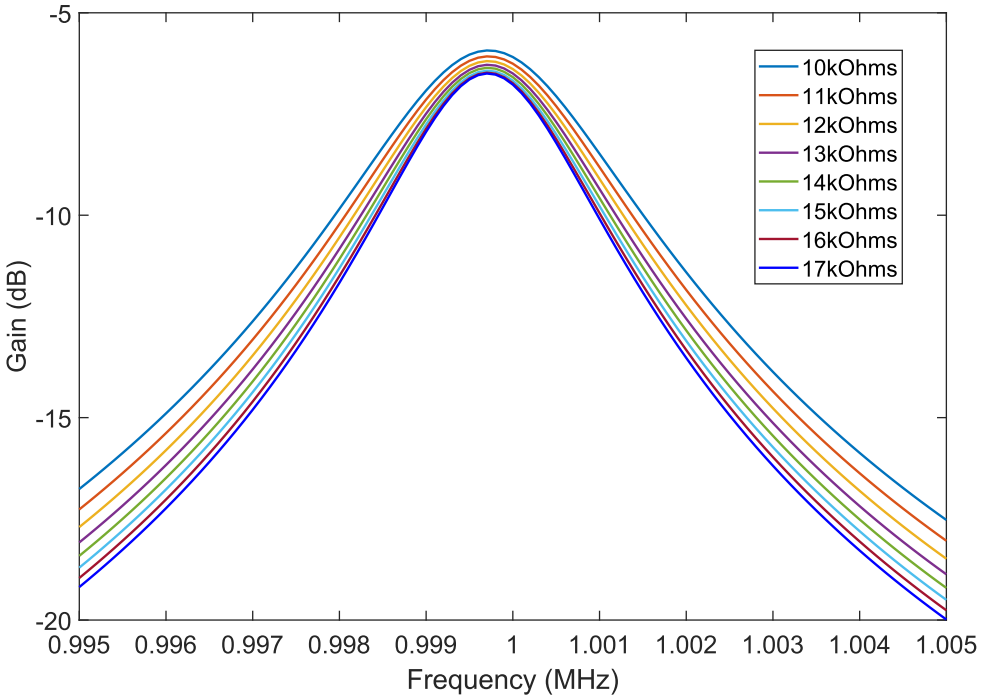


Figure 5.5: Gain of Schematic 2 circuit with different values of the memristor. The bandwidth values changes in the range of [0.954, 1.191]kHz.

Table 5.3: Minimum f_{-3dB} turning step at different memristor resistance values of the Schematic 2 structure at 1MHz f_c.

Memristor(Ω)	10k	11K	12k	13k	14k	15k	16k	17k
Min f_{-3dB} step(Hz)	6.7	5	5	4.5	4.5	3.4	4	3

The gain values of the 4-path filter at 1MHz with Schematic 2, 6nF capacitors and different memristor values are shown in Figure 5.5. Results show the centre frequency is not accurate 1MHz, but moves to 999.7KHz. This small centre frequency shift is caused by the parasitic capacitance C_p of the memristor. The larger the C_p, the larger the centre frequency shift. The maximum gain of curves with varying memristor values has around 0.5dB difference, which is caused by the change in the ratio between the memristor value and the ON state resistance of switches. The larger the ratio [$R_{memristor}/R_{switch}$], the smaller the maximum gain. The trends of the curves in Figure 5.5 are the same as expected, and the detailed data is recorded in Table 5.2. As Table 5.2 shows, for a 4-path filter works at around 1MHz with an original quality factor Q of around 1000, a memristor with resistance range [10k, 17k]Ω can generate a tunable cut-off frequency range [954, 1191]Hz, results as a tuneable quality factor range [839, 1048]. When maintaining the Q factor constant at 1000, with the change of memristor value, the centre frequency can change in a range [0.95, 1.19]MHz. Compared with the original centre frequency 1MHz, the achievable changing rate of the centre frequency without Q factor variation is around 24%. The actual cut-off frequency when using a memristor is different

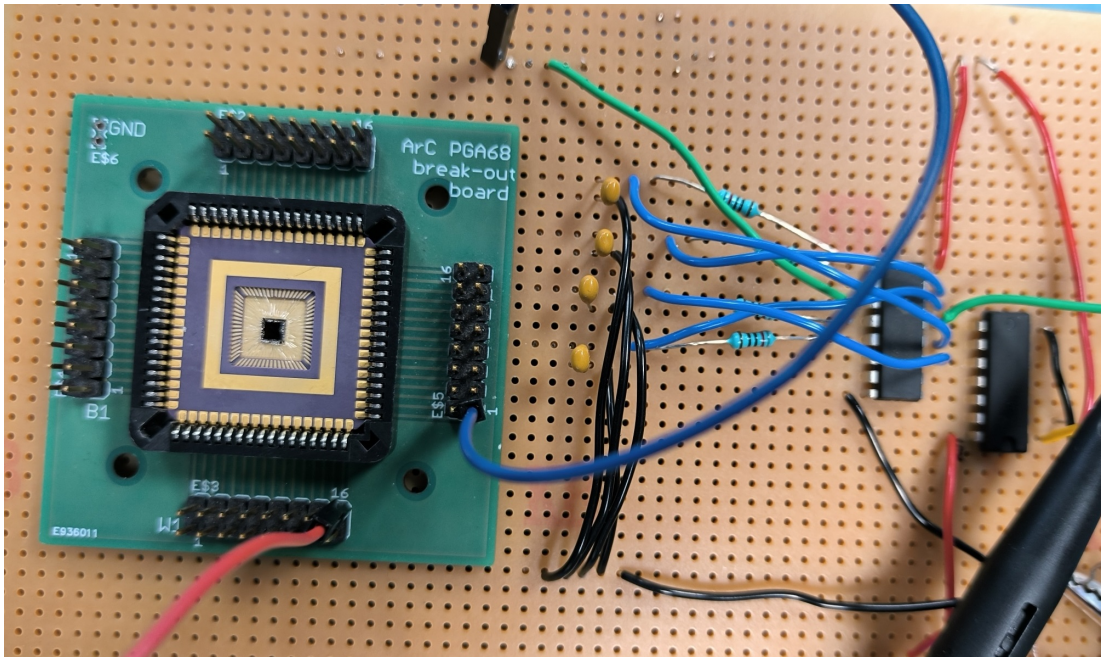


Figure 5.6: 4-path filter on a stripboard with memristor package. The memristor package is integrated on a break out board of ArC Two, and connects with the 4-path filter on a stripboard. The ArC Two is not shown in this picture.

from the f_{-3dB} when using a resistor. The differences are caused by the parasitic capacitance C_p of the memristor. Referring to equations 5.3 and 5.8, C_p changes the impedance of the memristor when the frequency is high, increases the f_{-3dB} value and reduces the tuneable f_{-3dB} range.

As the minimum step of the memristor resistance programming is ideally 1% of the current value, the minimum bandwidth turning steps at different memristor values are recorded in Table 5.3. It can be found that the minimum bandwidth tuning step is smaller than 6.7Hz, which means this tuneable filter has a very fine bandwidth step that is smaller than 2.7% of the whole bandwidth tuneable range.

5.3.2 Measurement Result with 1MHz centre frequency

The memristor package used in the laboratory measurement is TiO_x/Al_2O_3 device. The electrode overlap area of one memristor in the package is $10\times10\mu m^2$, and the thickness of the material in between the overlap electrodes is 4nm. The memristor package is programmed by ArC Two, which is a measurement instrument for working with RRAM arrays. The memristor package will first integrate to a daughter-board of ArC Two, be programmed to wanted resistance, then be placed on a break-out board and connected to the 4-path filter. The memristor chosen to combine with the 4-path filter has [10, 30]kΩ tuneable resistance range. CD4024B CMOS ripple-carry binary counter combined with waveform generator to offer the

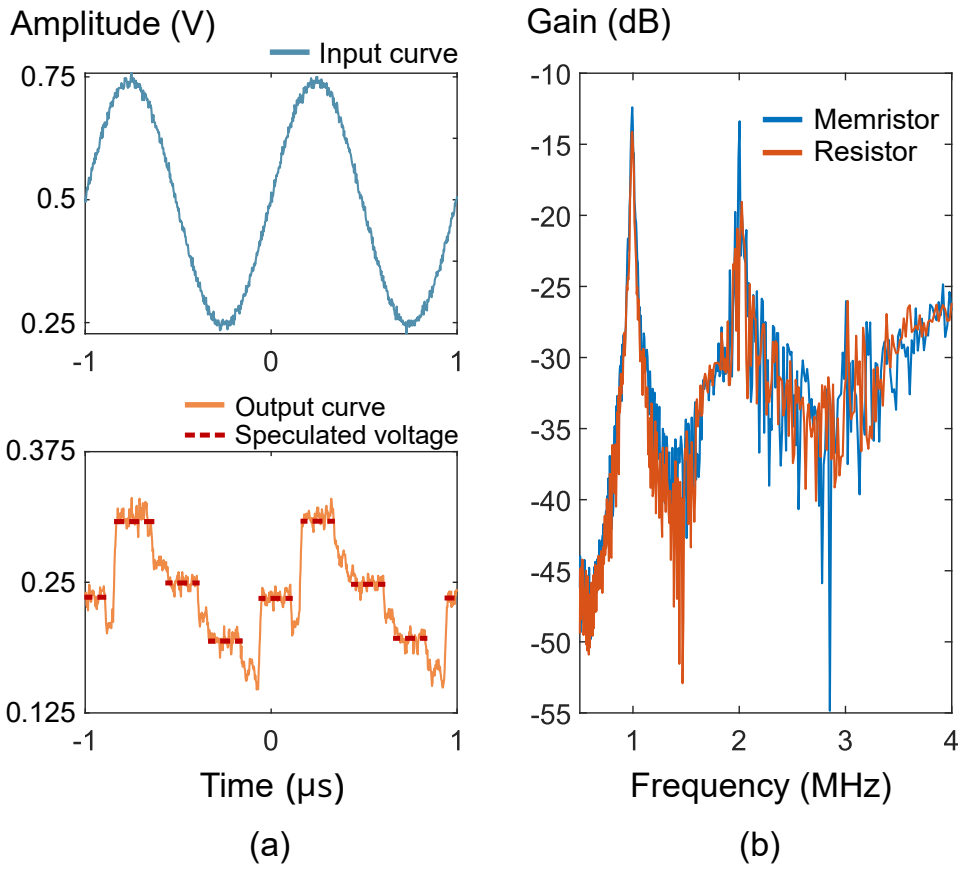


Figure 5.7: (a) Transient result of input curve(blue line), output curve(orange line) and speculated output DC voltage value(red dotted line). (b) Gain curves of the 4-path filter when using a memristor and a resistor.

switch's control signals. CD4052B analog multiplexer is used as 4 switch groups. As the memristor package is programmed by ArC Two, switch S_P and Vref are not included in the stripboard circuit. The capacitors used in the measurement are 6nF. The centre frequency of the multiplexer is set to 1MHz. The picture of the 4-path filter on the stripboard with the memristor package is shown in Figure 5.6.

The measured transient waveform of the input sine wave and output of the 4-path filter with 10Ω memristor is shown in Figure 5.7 (a). The red dotted lines show the speculated output DC voltage level based on the output curve. Combining the input curve with speculated output voltage values, it can be observed that one period of the input sine wave is sampled to four DC voltage values by the 4-path filter. The output curve is noisy compared with the ideal output in Figure 5.1 (b), besides, unwanted voltage drops between constant voltage levels can be observed in the measured output curve. The first reason is the switching time of the counter and multiplexer. In simulation, the switches turn at the same moment. however, in reality, it is found from the datasheets that the counter has an output Q_n to Q_{n+1} switching delay of

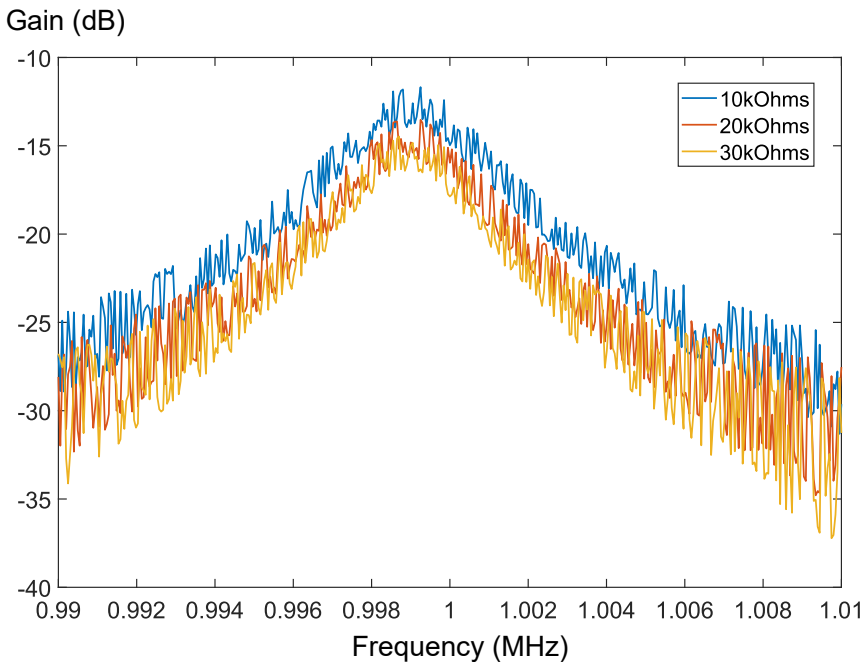


Figure 5.8: Gain of the 4-path filter with different memristor values. With memristor resistance [10, 30]kΩ, the tuneable bandwidth range is [1.5, 2]kHz. The noisy gain curves are mainly caused by the switching of the multiplexer.

40ns, while both the counter and the multiplexer has a rise&fall time of 20ns. Because of that, there is around 80ns switching time during the turning of the switches, which is closes to the switching gaps observed from Figure 5.7 (a). Second, in the ideal condition when the input frequency equals the centre frequency, the voltage on each capacitor is constant. However, in practical measurement, it is not possible to precisely match the input signal frequency to the centre frequency. The higher the frequency, the larger the error of frequency matching. Because of that, in measurement the voltages on the capacitors in the 4-path filter change continually. When one group of switches turn on, the voltage on the corresponding capacitor undergoes a period of oscillation before stabilizing. These two reasons make the voltage unstable during the switching times.

Figure 5.7 (b) compares the gain-frequency responses when using 10kΩ resistor and memristor. It can be found the curves of the 4-path filter when with resistor and memristor are similar. At the centre frequency, the maximum gain when using a memristor is larger than the condition when using a resistor, which is because the parasitic capacitance reduces the impedance of the memristor, hence the impedance of the memristor at 1MHz is not actually 10kΩ but a lower value. Also, at the second harmonic frequency which is 2MHz, the difference between the gains of using a memristor or a resistor is larger, as the impedance of the memristor further reduces.

Table 5.4: Measured f_{-3dB} & Q factor with different memristor value, and f_c range when Q factor maintains at 600.

Memristor (Ω)	f_{-3dB} (Hz)	Q factor	f_c with Q=600 (Hz)
10k	2k	500	1.2M
15k	1.8k	556	1M
20k	1.6k	625	0.96M
30k	1.5k	667	0.9M

The gain curves of the 4-path filter at 1MHz centre frequency with different memristor values are shown in Figure 5.8. The gain values fluctuate sharply at similar frequencies, which is caused by the noise in the output signal as shown in Figure 5.7 (a). Comparing Figure 5.8 with Figure 5.5, it is found the trend of the curve in the measurement result is the same as the simulation result. The detailed data of the measured f_{-3dB}, Q factor, and the tuneable f_c range when maintaining a constant Q factor value are recorded in Table 5.4. The f_{-3dB} at 20kΩ and 30kΩ memristor values are similar when the f_{-3dB} with memristor values between 10kΩ and 20kΩ has a relatively large variation. This is mainly because the parasitic capacitance has a greater impact on reducing impedance when associated with a larger resistor. In the mathematical simulation, with 10pF parasitic capacitance at 1MHz, 10kΩ memristor has 8.5kΩ impedance, 20kΩ memristor has 13kΩ impedance, but 30kΩ memristor only has 14kΩ impedance. Comparing the data in Table 5.4 with Table 5.2, it is found that the measured f_{-3dB} values are overall larger than the simulation results. It shows that the parasitic capacitance in the measurement is larger than the value of 10pF in the simulation. The Q factor in the measurement is small and can not reach 1000, hence the tuneable f_c range is set at Q equals 600. With a constant Q at 600, f_c can change in the range of [0.9, 1.2]MHz without varying the cut-off frequency.

The measurement results show there is a larger parasitic capacitance in the actual memristor device compared with the simulation, and the curves in the measurement result are noisy. One of the reasons is the interference from the stripboard and laboratory surroundings. The components on the stripboard use electrical solid wires for connection, which is bad for high-frequency signal transmission. It was observed that when moving the probes between the oscilloscope and stripboard in measurement, the noise condition of the transient curves also changes, which means the laboratory environment can affect the measurement results. On the other hand, as the memristor package has to be placed on the specific break board, the connection between the signal source, memristor and 4-path filter is also based on long jumping cables, which have large parasitic components and also large high-frequency-signal distortion.

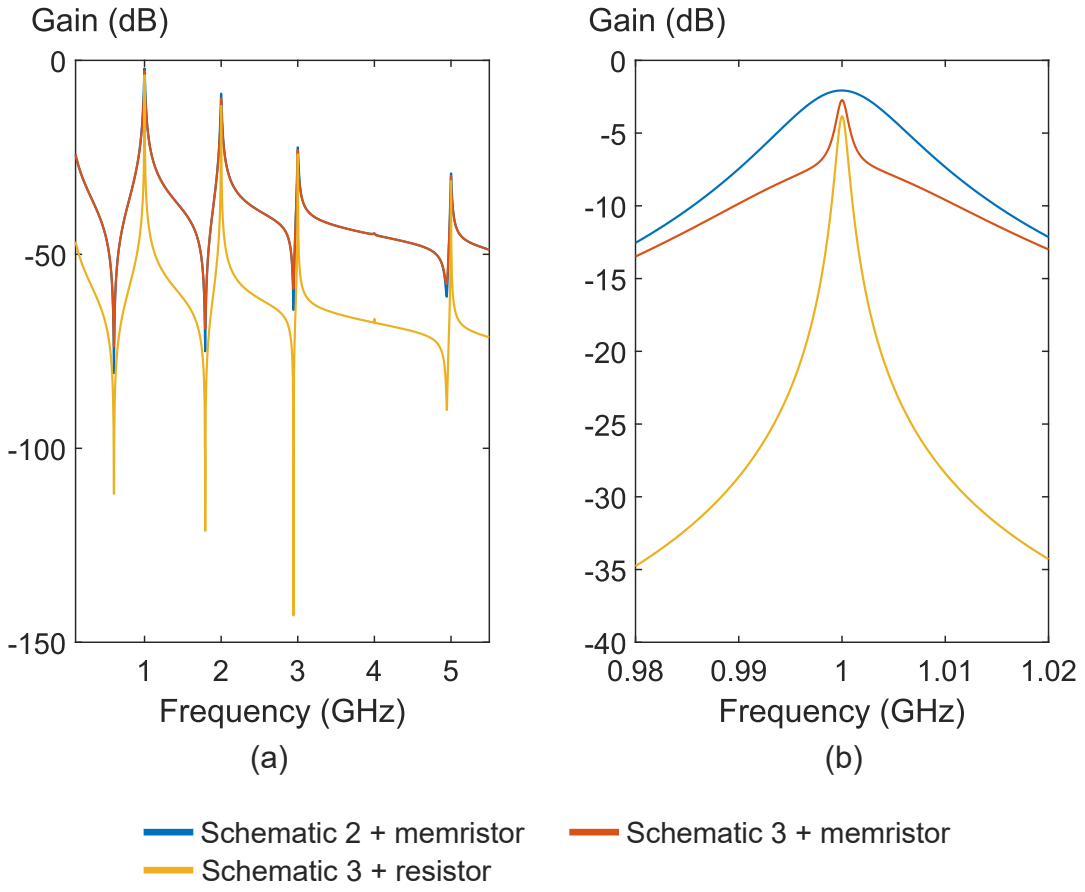


Figure 5.9: (a) The gain curves comparison result of [Schematic 2 + memristor], [Schematic 3 + memristor] and [Schematic 3 + resistor] in the [0, 5.5]GHz frequency range. (b) The gain curves of the three conditions in the [0.98, 1.02]GHz frequency range.

Due to the noise curves of the gain-frequency response, the bandwidth variation is hard to observe when the change of memristor resistance is small. Because of that, the minimum bandwidth turning step was not measured with the memristor package and 4-path filter on the stripboard. The power consumption of the 4-path filter is 38mW. Energy is mainly used to supply the work of the binary counter and multiplexer. As the binary counter and multiplexer need a 10V voltage supply, the power consumption of the circuit is also large.

5.3.3 Simulation results with 1GHz centre frequency

Figure 5.9 compares the gain curves of [the Schematic 2 structure with memristor], [the Schematic 3 structure with memristor], and [the Schematic 3 structure with resistor]. It can be observed from Figure 5.9 (a) that, first, the curves of the two Schematics with memristor are nearly overlapping, and second, the resistor curve has a smaller noise floor and narrower bandwidth compared with the memristor curves. Figure 5.9 (b) shows the [Schematic 2 + memritor] curve has a wider bandwidth compared with the [Schematic 3 + resistor] curve. The

[Schematic 3 + memristor] curve has a narrow bandwidth which is similar to the [Schematic 3 + resistor] curve when the input frequency closes to the centre frequency, but the bandwidth becomes larger and similar to the [Schematic 2 + memristor] curve when the input frequency far from the centre frequency.

Referring to the concept of Schematic 3 in the Methodology section, when the input frequency is the same as the centre frequency of the N-path filter, signals through the memristors and capacitors approach constant DC voltages. However, when the input frequency is different from the centre frequency, the voltages saved on the capacitors will change whenever the switches turn. The larger the difference between the input signal frequency and the switch centre frequency, the faster the voltages on the capacitors change. Because of that, only when the input signal frequency equals the centre frequency, the memristors work in absolute DC environments, which makes the gain curve have a narrow bandwidth similar to the condition of using resistors. When the input frequency is far from the centre frequency, memristors work in high-frequency environments, hence the curves of [Schematic 2 + memristor] and [Schematic 3 + memristor] are similar at these frequencies as shown in Figure 5.9.

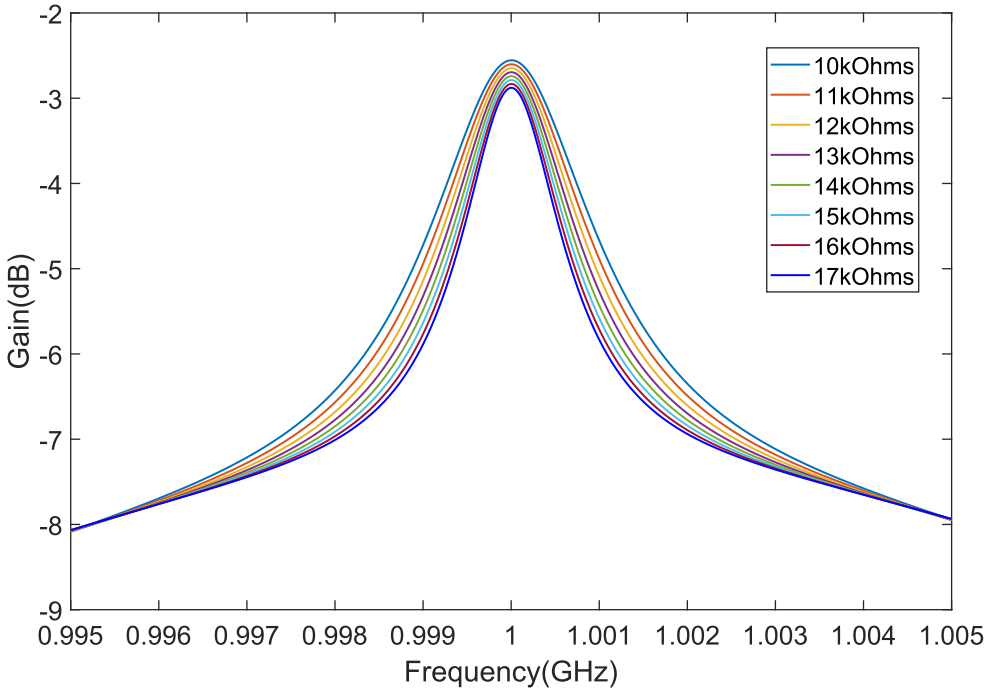


Figure 5.10: Gain curves of Schematic 3 with different memristor values. The tuneable bandwidth range offered by the Schematic 3 structure memristor-based 4-path filter is [0.99, 1.38]MHz.

Figure 5.10 shows the simulation results of Schematic 3 at 1GHz centre frequency with capacitor values C=8pF, and switches R_o=800Ω. Compare Figure 5.10 with Figure 5.5, it is found the downward trend for curves in Figure 5.10 slowing down at frequency far from the centre frequency f_c. Also, at frequency away from the f_c (lower than 996MHz and higher than 1.001GHz), the gain values of all the curves converge to the same value regardless of the memristor value. This is because the parasitic capacitor still dominates the memristor impedance at frequencies that are too far away from the f_c, and makes the memristor value variation lose its original function. The frequency that curves converge together is decided by C_p. The detailed data of Figure 5.10 is recorded in Table 5.5. The f_{-3dB} values when using memristors are higher than the f_{-3dB} values when using resistors. Different from the assumption that memristors work in ideal DC conditions when it is placed in between the switch groups, results show that the memristor impedance is still affected by the parasitic capacitor C_p. However, the influence of C_p in Schematic 3 is much smaller than in Schematic 2. For the gain results of Schematic 2 at 1GHz, no variation can be observed between different curves with varying memristor values. For Schematic 3, Table 5.5 shows the f_{-3dB} value can vary in a range of [0.99, 1.38]MHz, which results as a tuneable Q factor range 725 to 1010, and a tuneable f_c range [0.99, 1.38]GHz when maintaining Q factor at 1000. The achievable changing rate of f_c without changing the Q factor is 39%, which is even better than the result of Schematic 2 at 1MHz.

The minimum bandwidth changing steps of the Schematic 3 circuit at 1GHz with different memristor values are recorded in Table 5.6. Due to the large centre frequency and small bandwidth changing step, the bandwidth step values are not absolute precision, but the trend of bandwidth step changing can still be observed. The Schematic 3 circuit has a minimum

Table 5.5: f_{-3dB} & Q factor with different memristor value, and f_c range when Q factor maintains at 1000 in Schematic 3 circuit with 1GHz original f_c.

Memristor (Ω)	f_{-3dB} with resistor (Hz)	Actual f_{-3dB} (Hz)	Q factor	f_c with Q=1k (Hz)
10k	590k	1380k	725	1.38G
11k	543k	1310k	763	1.31G
12k	510k	1230k	813	1.23G
13k	480k	1170k	855	1.17G
14k	456k	1120k	893	1.12G
15k	436k	1070k	935	1.07G
16k	413k	1030k	971	1.03G
17k	395k	990k	1010	0.99G

bandwidth changing step smaller than 8.4kHz, which means it can turn the bandwidth with a step smaller than 2.2% of the whole tuneable bandwidth range. Similar to the Schematic 2 circuit at 1MHz, the Schematic 3 circuit works at 1GHz also shows the ability of very fine bandwidth turning.

Table 5.6: Minimum f_{-3dB} turning step at different memristor resistance values of the Schematic 3 structure at 1GHz f_c.

Memristor(Ω)	10k	11K	12k	13k	14k	15k	16k	17k
Min f_{-3dB} step(Hz)	7k	6.5k	8.4k	5.6k	5k	4k	3k	3.7k

5.4 Discussion

The N-path filter is designed for high-frequency applications. However, the influence of the parasitic capacitance of the memristor on the filter increases with frequency, which limits the operation of this memristor-based N-path filter at high frequencies. When simulating the Schematic 2 circuit with 10pF parasitic capacitance C_p and 1GHz centre frequency f_c, the variation of memristor value nearly doesn't change the cut-off frequency of the filter, as at frequency up to 1GHz, the impedance of the memristor is dominated by the fixed C_p value instead of the tuneable memristor resistance.

The circuit with Schematic 3 structure solves the problem of designing a high-frequency memristor-based reconfigurable N-path filter. However, it also some some limitations. The main drawback of the schematic 3 circuit is the high quantity of memristors being used. The required amount of memristors equals the number of paths in the N-path filter, which will be a large value for high high-precision N-path filter. Only one memristor can be programmed in one programming process, hence for a memristor-based 4-path filter, the memristor programming process needs to be done four times to change all the memristors to a specific value, which increases the complexity of operations. Besides, it is hard to program all the memristors to the same accurate resistance. The resistance difference between memristors in each path will reduce the accuracy of the output waveform. On the other hand, for N-path filter works with a 17kΩ resistor, to make Q=1000, the capacitor value needs to be around 5pF. The reduction of capacitor value increases f_{-3dB}, but the frequency in which curves converge together is decided by C_p, As shown in Figure 5.10, which is nearly constant. When using a memristor with C_p=10pF, capacitors with capacitance too small will make f_{-3dB} close to the convergence frequency, which reduces the tuneable f_{-3dB} range. When f_{-3dB} is larger than the convergence frequency, the filter will lose the function of f_{-3dB} adjustment. Because of that, the f_{-3dB} value of Schematic 3 at 1GHz is limited to around 2MHz or below. It can also be found from Figure 5.10 that the maximum f_{-3dB} variation range is located on the frequency range between around 998kHz and 999kHz, and the location of this [maximum f_{-3dB} range]

Table 5.7: Bandwidth(f_{-3dB}) of Schematic 2 and Schematic 3 at 1GHz with different parasitic capacitance values.

C_p (F)	Memristor(Ω)	Schematic 2 f_{-3dB} (Hz)	Schematic 3 f_{-3dB} (Hz)
500f	10k	10.16M	3.01M
	17k	10.13M	1.98M
100f	10k	3.24M	2.91M
	17k	3.1M	1.97M
50f	10k	2.1M	2.33M
	17k	1.9M	1.88M
10f	10k	1.2M	1.59M
	17k	946k	1.22M
0	10k	1.11M	1.25M
	17k	865k	800k

remains almost unchanged with the variation of C. This means when using larger capacitors C, the tuneable f_{-3dB} range will reduce. As a result, when using 16pF capacitors instead of the 8pF capacitors in Figure 5.10 and Table 5.5 to simulate the Schematic 3 circuit, the tunable f_{-3dB} range reduces to [450, 671]kHz.

In the result section, the memristor model is assumed to have 10pF parasitic capacitance. This is a relatively high hypothetical value. The memristor packages used in the measurement have an electrode area of $10 \times 10\mu m^2$ for each memristor, which is also not the smallest area the technique can achieve. With more advanced manufacturing processes, memristor can have smaller size, and also smaller parasitic capacitance. Table 5.7 shows the results of f_{-3dB} and Q factor with [Schematic 2]&[Schematic 3] circuit structures and different memristor C_p values. All the values are simulated with R_o=800Ω and C=3pF. It can be observed that for the Schematic 2 circuit at 1GHz f_c, with a high C_p value, the bandwidth can not be maintained at a small value. When C_p increases, the bandwidth value increases but the tuneable bandwidth range reduces. Referring to equation 5.2, high frequency and C_p values reduce the impedance of the memristor (R value in equation 5.2), which limits the range of bandwidth. Table 5.7 shows with C_p at around 10fF, the tunable bandwidth range is similar to the condition that uses a tuneable resistor in the N-path filter. Different from the results of Schematic 2, the bandwidth of the Schematic 3 structure is not affected too much by the parasitic capacitance value. With the increase of parasitic capacitance value, the bandwidth values slightly rise, and the tuneable bandwidth ranges are even expanded. This phenomenon can also be observed from Table 5.6. This may be because the memristor at different resistance levels has different

time constants, which expands the difference of gain in a specific frequency range, and hence expands the tuneable cut-off frequency range. Although can not be observed from the table, the reduction of C_p improves the noise floor in the stop-band of the Schematic 3 structure N-path filter.

5.5 Conclusion

This work reports the application of memristors in reconfigurable N-path filters whose cut-off frequency can be adjusted by memristor value. The frequency responses of three types of memristor-based N-path filter circuit structures were compared. A memristor-based 4-path filter was measured in the laboratory with a memristor package at 1MHz centre frequency. The simulation results of different memristor-based 4-path filters at 1GHz were also recorded.

Simulation results show the reconfigurable 4-path filter designed with Schematic 2 in Figure 5.2 can work well at 1MHz with memristor value [10k, 17k]Ω, which has tuneable f_{-3dB} range [954, 1191]Hz and tuneable Q factor range [839, 1048], with minimum bandwidth turning step smaller than 2.7% of the whole tuneable bandwidth range. A [Schematic 2] structure 4-path filter was built on a stripboard, and measured with a memristor which has [10k, 30k]Ω resistance. The 4-path filter has a tuneable f_{-3dB} range [1.5, 2]kHz and a tuneable Q factor range [500, 667]. A N-path filter that uses multiple memristors (Schematic 3) and can work at 1GHz is also designed. Simulation results show the Schematic 3 structure N-path filter has a tuneable f_{-3dB} range of [0.99, 1.38]GHz, which means a tuneable f_c range of [0.99, 1.38]GHz when maintaining Q=1000, with minimum f_{-3dB} turning step smaller than 2.2% of its whole tuneable bandwidth range. The research in this chapter shows the very fine bandwidth-changing ability of the memristor-based N-path filter structures.

Memristor-based bandwidth-controllable N-path filter can widely be used in RF and communication systems. As an example, by integrating the N-path filter with a LNA at the RF front-ends, it can reduce the noise floor by filtering out unwanted frequencies. If the LNA itself is reconfigurable(reference to Figure 2.14 (b)), the bandwidth-controllable N-path filter can maintain the bandwidth of the circuit while changing the center frequency. In system level, the memristor-based N-path filter can be used in phase array system for beamforming by adjusting the bandwidth and phase of signals in different paths. When using in receiver, it can also allow the receiver to filter out unwanted interference adaptively.

As memristors are non-volatile elements, it doesn't cost power to maintain its resistance level. Besides, the size of the memristor element can be quite small (smaller than $300 \times 300 nm^2$), which also reduces the size of a memristor-based reconfigurable device. However, as this study only researches the possibility of combining memristors with different N-path filter structures, the switches used in the simulations are ideal elements with specific ON/OFF resistances. Because of that, the low-power and small-area benefits of memristor-based devices are not shown in this chapter.

For further work, first, the schematic and layout of the memristor-based N-path filter structures need to be designed. After that, the performance of the circuit structures in this research can be compared with other works. Second, in the measurement of this research, the 4-path filter on the stripboard shows large parasitic capacitance which reduced the performance of the circuit when working with 1MHz centre frequency. To measure the performance of a memristor-based N-path filter at MHz frequency, a circuit built on a PCB board is needed. Also, the connection between the memristor and the N-path filter should be achieved by a specific connector instead of jumping wires. Third, the memristor package used in this research includes several memristors with different resistance ranges. However, it was hard to find 4 similar memristors that have the same resistance ranges and current-voltage characteristics. Because of that, Schematic 3 in Figure 5.3 wasn't measured in the laboratory with real memristor components. In the future, if there were suitable memristors, Schematic 3 should also be measured with RF PCB at high frequency.

Chapter 6

Conclusion

6.1 Contribution

The application of multi-stage analogue memristors in high frequency is a problem in the research of memristive devices, and there is still less research in this direction compared with other memristor applications. In the RF applications of memristors that have been published until now, most of the reconfigurable RF devices use memristor RF switches which can work at very high frequency but only have ON and OFF two stages. Some of the researchers tried to use multiple-stage memristors in high-frequency tuneable devices. However, many researchers ignore the effect of parasitic capacitance in the memristor in the articles and consider the memristor as a purely resistive element. In this thesis, I am attempting to expand the applications of multi-stage analogue memristors at high frequency when incorporating parasitic capacitance of memristors into the analysis at the same time. Three types of memristor-based reconfigurable circuits are designed in this study, to expand the applications of multi-stage analogue memristors at different frequency ranges.

1. Memristor-based Reconfigurable Instrumentation Amplifier In Chapter 3, a reconfigurable memristor-based instrumentation amplifier whose gain value can be adjusted by the memristor is discussed. This reconfigurable amplifier was measured with a memristor package in the laboratory. Measurement results show the memristor-based reconfigurable instrumentation amplifier can work at frequencies lower than 450kHz, with a tuneable gain range [9.5, 16]dB.

2. Memristor-based Tuneable Delay Circuit In Chapter 4, a memristor-based reconfigurable delay circuit is designed. Memristors are used in tuneable DC voltage sources, to control the output delay time of delay elements indirectly. The memristor-based DC source can offer DC voltage output [594, 720]mV with a very small voltage turning step, which is 2.2mV at maximum. The whole delay circuit is designed as a chip, includes a MHz delay part, a GHz delay part, a memristor programming controller, input signal generators and output

buffers. The MHz delay part can offer a range of delay time [14, 55]ns in a frequency range [0.2, 10]MHz, and the GHz delay part can output a range of delay time [255, 633]ps, in the frequency range [0.05, 1.6]GHz. To measure the chip, a PCB board is designed, and the operations of the chip measurement progress with the PCB are also discussed in Chapter 4.

3. Memristor-based Reconfigurable N-path Filter In Chapter 5, the possibility of combining memristors with N-path filter structures is discussed. Different memristor-based N-path filter structures are compared. One memristor-based reconfigurable 4-path filter was measured with a memristor package in the laboratory. This memristor-based 4-path filter has a tuneable bandwidth of [1.5, 2]kHz, and can work at 1MHz. A memristor-based N-path filter which can adapt to work at radio frequency is also developed. Simulation results show an N-path filter structure with 4 memristors can work at 1GHz, with a tuneable bandwidth of [0.99, 1.38]MHz.

The research in this thesis explores the applications of memristor from two perspectives, which are measuring the fabricated memristor package with circuits in practice, and using the memristor model to design high-frequency reconfigurable circuits in simulation. In the measurement with memristor packages, the studies in this thesis tested the combination of memristors with analogue and middle-frequency circuits in real-world working conditions, accumulating valuable experimental data for the practical application of memristors. In simulation work, different from many articles that consider the memristive devices as pure resistive elements, this thesis assumes a relatively large parasitic capacitance value(10pF) in the memristor, to research the worst case of applying multi-stage memristors in high-frequency signal environments. The memristor-based tuneable delay circuit in Chapter 4 is approximately 25% smaller in area compared to similar tuneable delay devices, while the minimum step size for the change in delay values is finer than at least 50% of the tuneable delay circuits that have a similar delay range. The memristors are applied in tuneable DC voltage sources, this structure has a strong potential for expansion and can be applied to any circuit where performance can be altered by voltage, without concerns about the parasitic capacitance of the memristor affecting the signal flow in the modified circuit. In the design of the multiple-memristor N-path filter (Chapter 5), the scheme of placing memristors in high-frequency signal paths was attempted. Simulation shows this design expands the frequency range of multi-stage memristor operation in high-frequency environments from around 10MHz to over 1GHz. All these results show the good potential of multi-stage analogue memristors in the design of reconfigurable radio frequency circuits.

6.2 Discussion

This section highlights some of the common problems that are encountered during the research. First, the methods of utilizing memristors in reconfigurable RF circuits are discussed. It then considers the influences of memristor parasitic capacitance and argues the circuit measurements that are restricted by the memristor testing platform. Last but not least, the parameters missing in some of the memristor models and their influences are argued.

6.2.1 Methods of Applying Memristor in Reconfigurable RF Circuits

The research in this study shows the parasitic capacitor of the memristor does indeed have a significant impact on the application of memristors in high-frequency-signal environments. Despite being somewhat contradictory, one of the methods to effectively operate a memristor with a large parasitic capacitance in high-frequency signal circuits is to place it in a localized low-frequency signal environment. For example, in Chapter 4, to control the GHz delay circuit by memristors, the memristors are placed in DC voltage sources, and use the tuneable DC voltages to adjust the voltage-control delay elements indirectly. Chapter 5 simulated a high-frequency memristor-based 4-path filter that can work at 1GHz. In this 4-path filter, memristors are placed in environments that face the same 1/4 part of a sine wave, hence the voltage on each memristor is nearly constant DC voltage when the input signal frequency equals the centre frequency of the filter. Based on the experience of memristor-based DC voltage source and memristor-based N-path filter, other circuit structures that allow the memristor to operate in an approximating baseband frequency environment are worth exploring. Besides, apart from placing the memristor at baseband frequencies, other methods of applying memristors to high-frequency signal circuits are also worth researching.

In this thesis, the operations of memristors are separated into two modes, which are normal work mode and programming mode. In normal work mode, memristors are applied with constant low DC voltage, to make the memristive devices show constant resistance levels; In programming mode, high-voltage pulses are applied on memristors, to change the resistance of memristors. This approach treats the memristor as a regular resistive element in normal work mode, while in programming mode, it uses the memristor's non-linear I-V characteristics to alter its resistance value. This is not the only way of using memristor. Due to the non-linear I-V characteristic, the memristor exhibits different resistance values based on the applied voltage. This characteristic might be directly applied in computing systems without the need for a specifically designed programming mode for memristors. Alternatively, a computing system could pre-adjust the resistance values of memristors significantly through a programming mode, to make memristors represent different weight values. Subsequently, in computations, different voltages could be applied to the memristors, allowing them to adjust their output based on various input signals. More approaches to applying memristors can be considered in reconfigurable circuit designs.

6.2.2 Parasitic Capacitance Value of Memristors

The method of applying memristors in high-frequency environments strongly depends on the technologies and parasitic capacitance of memristors. In the research of this thesis, the practice memristor packages have around 10pF parasitic capacitance, and all the simulations in Cadence also assume the memristor model has 10pF parasitic capacitance. This parasitic capacitance value is quite large for RF devices. However, this value is estimated from the $10\times10\mu m^2$ memristor device, which can be considered as the worst condition of applying memristors in high-frequency devices. In the research of the tuneable delay circuit(Chapter 4), the size of the memristive element integrated with CMOS circuits is around $250\times250nm^2$, hence the integrated memristor will have a parasitic capacitance value much smaller than 10pF. In memristor RF switches which are specially designed for RF applications, the parasitic capacitance is only around 1.6fF [6], which is 6250 times smaller than the parasitic capacitance value assumed in this thesis. With the development of memristor technologies, multi-stage analogue memristors will have smaller sizes, and also smaller parasitic capacitance, hence the applications of multi-stage analogue memristors in reconfigurable RF devices will become easier in the future.

6.2.3 The Challenges of Applying and Measuring one Memristor from A Memristor Array Package

In the research of Chapter 3 and Chapter 5, a memristor package is combined with circuits on breadboard/stripboard, and measured in the laboratory. As memristors are predominantly used in the form of arrays in neural networks and computing systems, the memristor package used in the experiments is also a memristor array. However, when using only one memristor from the array, the connection between the memristor package and the circuit under test becomes a challenge.

When programming the memristor, the memristor package needs to be integrated on the daughter board of ArC Two. After the programming is finished, the memristor is removed from ArC Two and placed into a breakout board serving as a base and connector. Subsequently, two ports on the breakout board are connected to the circuit under test using jumper wires. The intricate operational steps make the integration and testing of the memristor with the circuit challenging. Additionally, the connection between the memristor and the circuit involves a breakout board and jumper wires, causing significant signal attenuation through the memristor. Even if built the circuit on PCB and set a specific connector for the memristor package, as the programming of the memristor is based on ArC Two, the connection between ArC Two, the memristor package and the circuit is still a problem.

The best way to measure a memristor-controlled circuit which has separate memristors instead of a memristor array, is to integrate the memristor with the CMOS circuit which has the on-chip memristor programming system, and measure the taped-out circuit in the laboratory. However, this method simultaneously increases the difficulty of testing the combination of memristor components with circuits in practice. This is also one of the reasons why most articles on the application of memristors with circuits can only provide simulation data.

6.2.4 Missing Parameters in Memristor Models

When reviewing the literature about memristor applications in RF devices, it is found that many designers ignore the existence of parasitic capacitance in the memristor, and it is hard to determine whether these designs that incorporate memristors can truly function in high-frequency environments as indicated by simulation results. Some of the examples have been discussed in Section 2.2.3 of Chapter 2.

One of the reasons is the memristor models they use are not designed for high-frequency applications, hence the descriptions of these models also don't include the parasitic capacitance in the memristor. Many memristive devices are designed for applications in neural networks and analog computing, so the description of their performance is more focused on their I-V characteristics, switching speed and resistance range. As the value of the parasitic capacitance does not affect their main functions, it is understandable that the parasitic capacitance may not be mentioned in some of the literature about them. However, many designers who are not familiar with memristor technologies may apply unsuitable types of memristors to their circuits, which can make their designs difficult to work well in reality.

The core reason for this phenomenon is that memristors do not have a unified model framework that includes all parameters. When a model covers all parameters that may affect performance, such as parasitic capacitance, signal distortion, switching speed, resistance range, etc., designers in various fields can intuitively understand whether this memristor is suitable for their design. Although this approach is difficult to implement, after all, describing too many parameters that do not affect the main function of a memristor will make the article appear messy, it is still necessary to mention the parameters that are not included in a memristor model.

6.3 Future work

This thesis researched the methods of applying analogue multi-stage memristors in the designing of reconfigurable analogue and RF integrated circuit, and discussed 3 types of different memristor-based reconfigurable devices, which are memristor-controlled instrumentation amplifier, memristor-based tunable delay circuit, and memristor-based N-path filter. The researches in this thesis provide feasible methods of using analogue memristors with high frequency devices, and offer valuable data of measuring analogue memristors with analogue circuits in the laboratory. Further research on multi-stage memristor based reconfigurable analogue and RF applications can be done in mainly three directions:

1. Memristor Modeling: Memristor models are still imperfect and in development. Most of the analogue multi-stage memristor models focus on the nonlinear I-V characteristics of memristor, but ignore the parasitic capacitance parameters that affect the high frequency performance. On the other hands, memristor RF switch models always consider a memristor as a resistor at ON-state and a capacitance at OFF-state. To apply analogue memristor at high frequency, the influence of parameters that may affect frequency response of the device must be included in the model.

2. Memristor Measurement: Until now, the measurement data about using multi-stage memristor with analogue and RF circuits is rare compare with the designs and simulations of memristor-based analogue/RF devices. The insufficiency of measurement data makes it difficult to explore the potential of memristor-based analogue/RF applications, and also hinders the possible issues that may happen in the practical combination of memristors and analogue/RF circuits. For example, there may be some undiscovered characteristics of memristors, similar to parasitic capacitance, that could affect the usage of memristors in high-frequency environments.

3. Suitable methods of memristor application: This paper explores the use of memristors primarily by adjusting their resistance to change the DC voltage/current, thereby indirectly controlling other voltage- or current-based tuneable circuit elements. This method avoids the influence of parasitic capacitance of memristors on the high frequency signals, and can widely be used in other voltage or current controlled analogue circuits. Besides, other methods of using memristors in high-frequency circuits are also worth investigating.

All the three future work directions will meet some challenges. In terms of memristor modeling, as memristors with different structures have totally different I-V curves, resistance range, parasitic elements and many other characteristics, It is difficult to establish a universal model applicable to all memristors. For memristor-based circuit measurement, as memristor techniques are still in development, only a few laboratories have the capability to produce memristors, and the performance of memristors varies between different laboratories. It causes a problem that research groups developing memristors lack the capability to use them for integrated circuit

design, while researchers needing to utilize memristors in circuits do not have access to memristor devices for measurement. Finally, to use memristors in high-frequency devices without affecting the performance of the circuits, the parasitic capacitance of memristors need to be as small as possible. In the case of using memristor devices with large parasitic capacitance($\geq$pF level), controlling voltage and current with memristors remains the most suitable method. However, with the advancement of memristor technology, multi-stage memristor devices with low parasitic capacitance($\sim$single-digit fF level) will be able to directly integrate with RF circuits to design adjustable high-frequency circuits.

In this thesis, some of the research works haven't been fully finished yet, or have the possibility of improvement. These works can be continued in the future.

For the memristor-based tuneable delay circuit in Chapter 4, the chip has been sent to tape out, and the wafer might be returned after several months. The measurement PCB board has been designed but has not been sent to the company for fabrication. In the future, if there is a chance, I would like to measure my chip on the PCB by myself. If not, I will write a specification to talk about the chip and the measurement operation and give it to someone who can help me test the circuits.

For the N-path filter research in Chapter 5, the high-frequency memristor-based 4-path filter is only simulated in Cadence, and all the switches are ideal components with specific resistance values. This is because this project mainly researches the suitable structure of a memristor-based N-path filter, excluding the detailed design of the switch groups. On the other hand, the multiple-memristor-based N-path filter was also not measured in the laboratory, because the memristor package in my research doesn't have 4 memristors that can be programmed to the same memristor values with high accuracy. Besides, to generate a circuit that can work in GHz, both breadboard and stripboard are not suitable. In the future, first, the multiple-memristor-based N-path filter should be fully designed, including a comprehensive schematic and layout. After that, the memristors and the circuit need to be taped out and measured in the laboratory.

Finally, the simulations of memristors in these works assume the memristors have 10pF parasitic capacitance, which is a very large value for high-frequency applications. The parasitic capacitance value mainly depends on the material, electrode area, and fabrication technology. It has been proved that a 2-stage memristor can have a very low parasitic capacitance down to 2fF [6]. With the development of new memristor structures and technologies, multi-stage memristor will also have smaller parasitic capacitance. In the future, by using multi-stage memristors with a larger resistance range and small parasitic capacitance, applications of memristors in reconfigurable high-frequency designs will become easier.

Appendix A

Publication

All the research projects in Chapter 3 to Chapter 5 are in the publishing process, or have already been published. This Appendix B chapter documents the publication status of the research projects discussed in this thesis.

1. Chapter 3: Memristor-based Reconfigurable Instrumentation Amplifier This project has been published [18]: F. Yang, A. Serb, and T. Prodromakis, "Measured behaviour of a memristor-based tuneable instrumentation amplifier," Electronics Letters, vol. 58, no. 15, pp. 570–572, 2022.

2. Chapter 4: Memristor-based Reconfigurable True Time Delay Circuit This project has been submitted and is in the reviewing process.

3. Chapter 5: Memristor-based Reconfigurable N-path Filter This project is in preparation and going to be submitted.

Appendix B

Detailed Layout of the Memristor-based Reconfigurable Delay System

This appendix A chapter lists the detailed layout diagrams of each part of the memristor-based reconfigurable delay system in Chapter 4.

Figure B.1 shows the layout of one memristor-controlled DC voltage source. The size of one memristor-controlled DC voltage source is $19\times38\mu m^2$. The size of the memristor block is $2.35\times2.35\mu m^2$, and the actual memristor size at the crosspoint of the two electrodes is around $350\times350nm^2$.

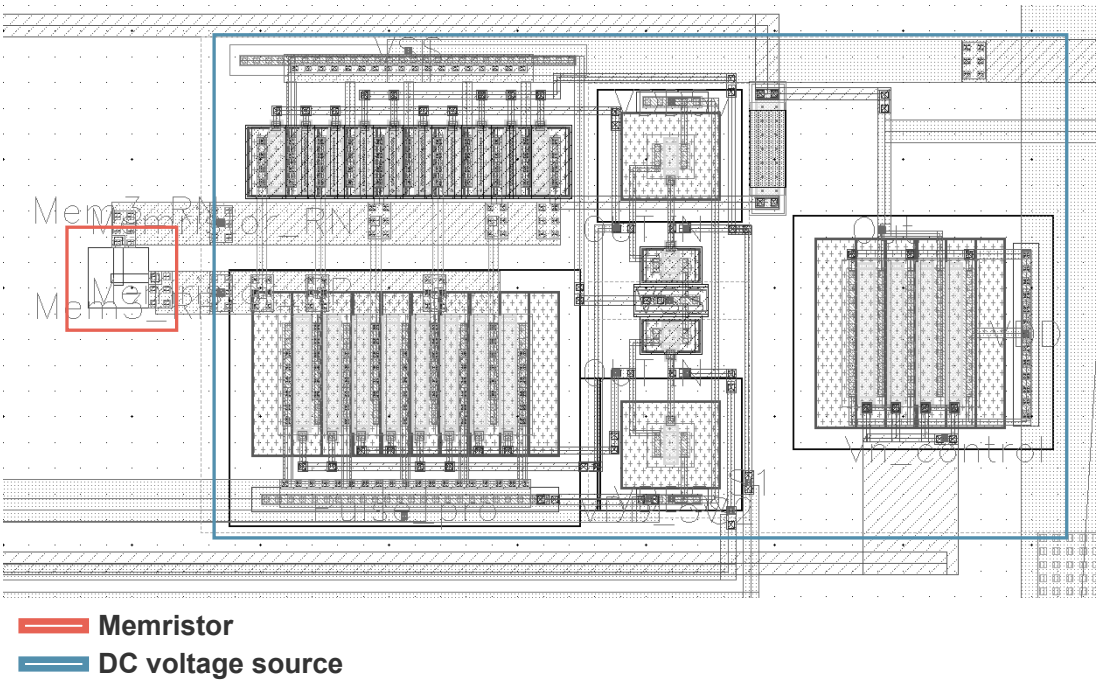


Figure B.1: Layout of one of the memristor-based DC voltage sources.

Figure B.2 shows the layout of the memristor programming controller. The size of the memristor programming controller is $54 \times 64 \mu m^2$. Referring to Figure 5.2 and Section 5.2.4 in Chapter 5, the three layers of flip-flops are labeled in the diagram, where the first layer is the command input layer, and the third layer is the output layer.

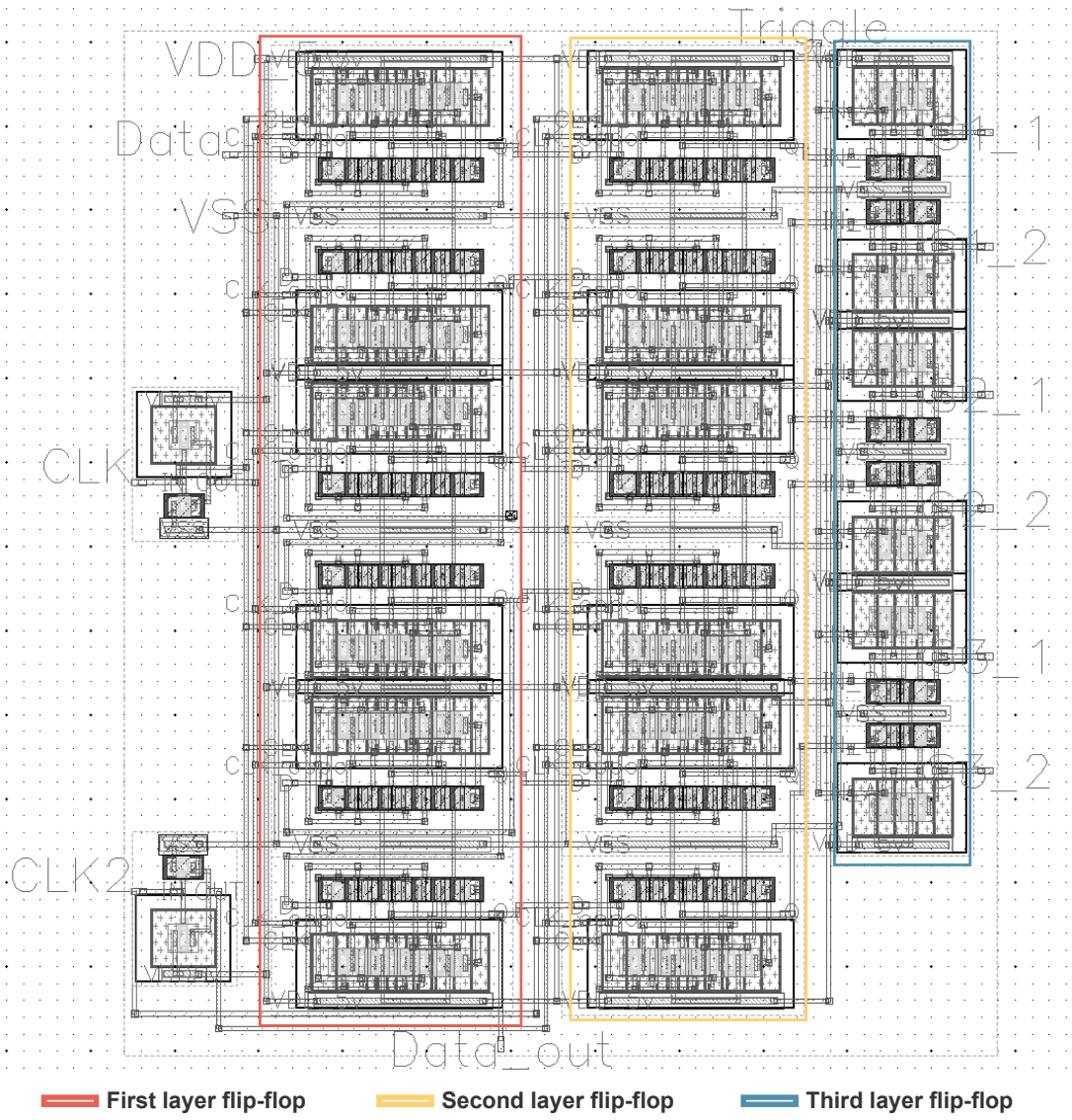


Figure B.2: Layout of the memristor programming controller.

Figure B.3 shows the layout of the GHz delay system. The size of the whole GHz delay system is $164 \times 181 \mu m^2$. The circuit elements in the GHz delay system are labeled with different colors. It can be found that the size of the delay elements part is small, which is only $25 \times 74 \mu m^2$. Close to half of the area in the GHz delay system is occupied by capacitors at the input of the delay elements(red region) and output buffers(yellow regions).

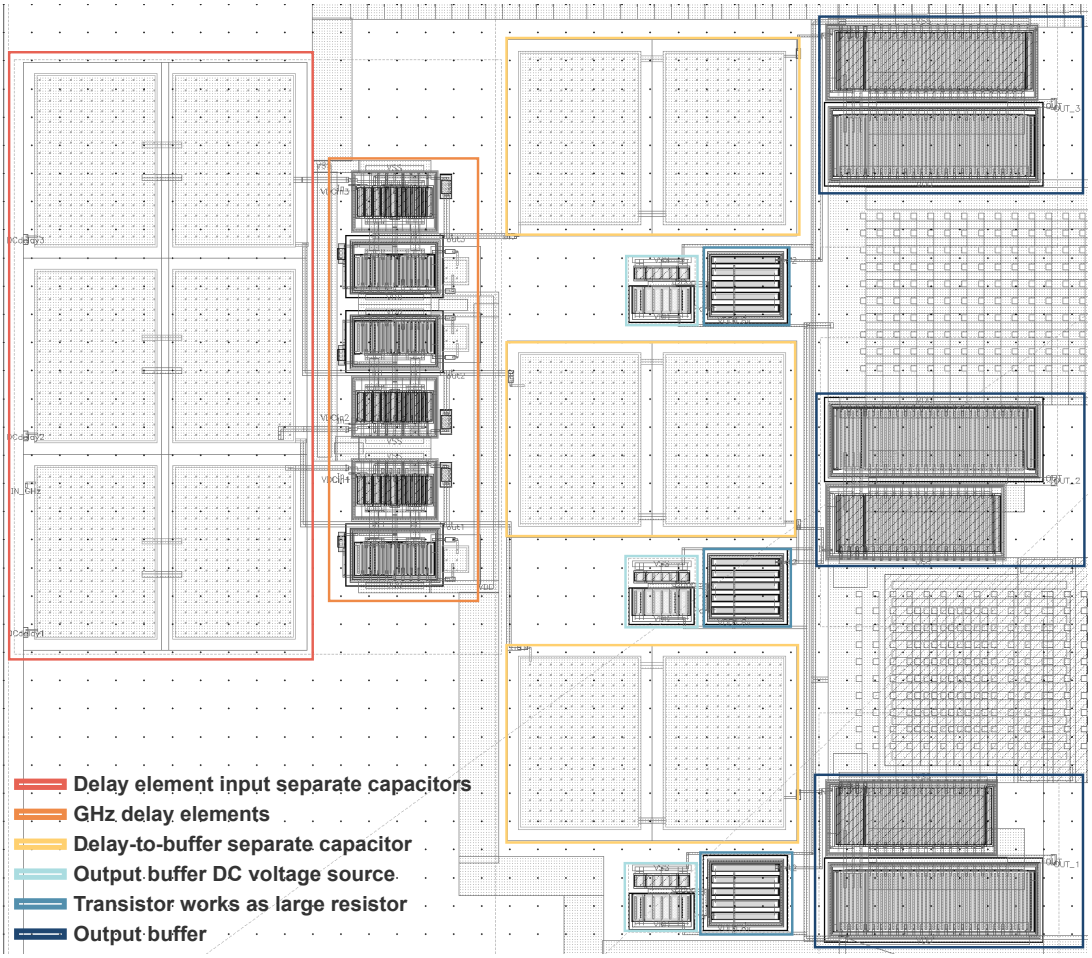


Figure B.3: Layout of the GHz delay system.

Figure B.4 shows the layout of the MHz delay system. The size of the MHz delay system is $104 \times 138 \mu m^2$. The circuit structure is the same as the GHz system, only the sizes of transistors and capacitors are different.

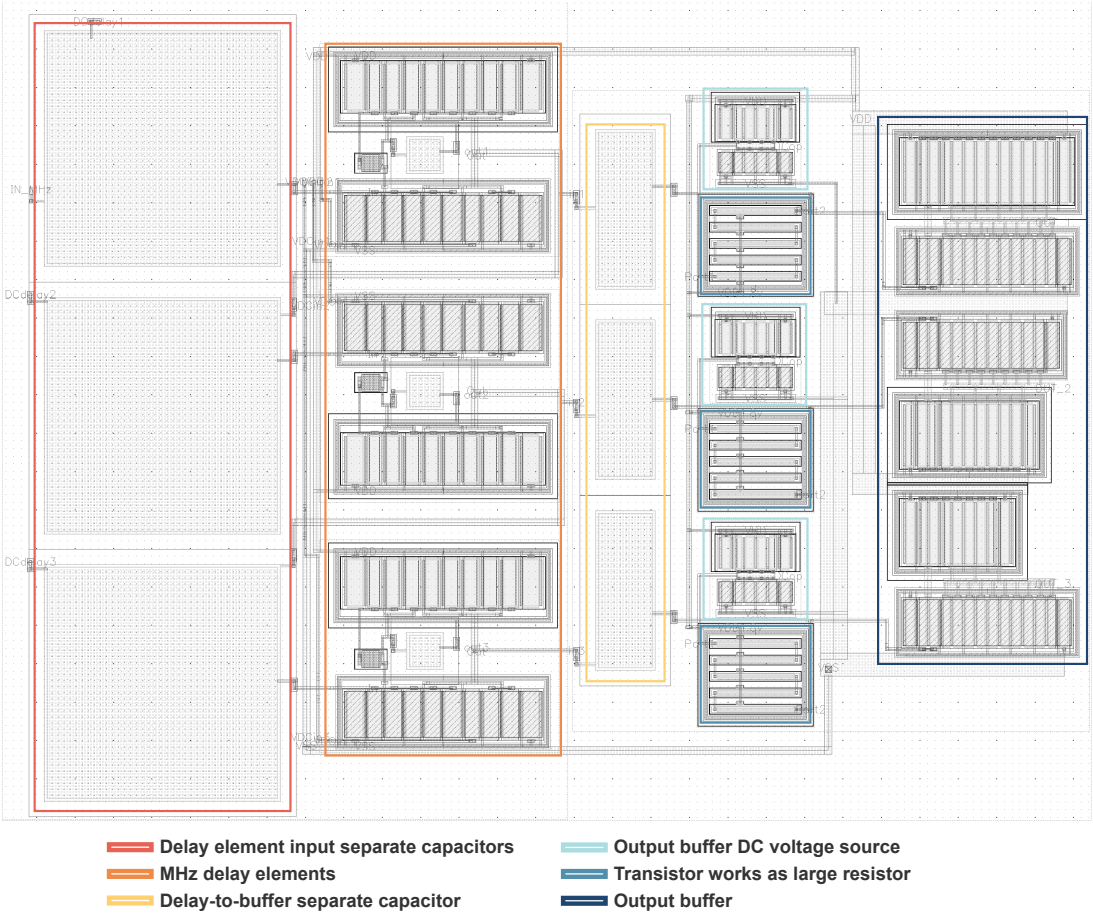


Figure B.4: Layout of the MHz delay system.

Figure B.5 shows the layout of the whole tuneable delay system with the padring. The system includes a GHz delay system(red region), a MHz delay system(blue region), memristor-based DC sources(purple region), memristor programming controller(orange region), oscillators for GHz signal input(yellow region)&MHz signal input(green region), and switch groups(brown region) between DC sources and delay systems. Other elements include ESD devices and the padring. The signals that different pads connect with are shown in different colors, whereas the power ports are shown in black.

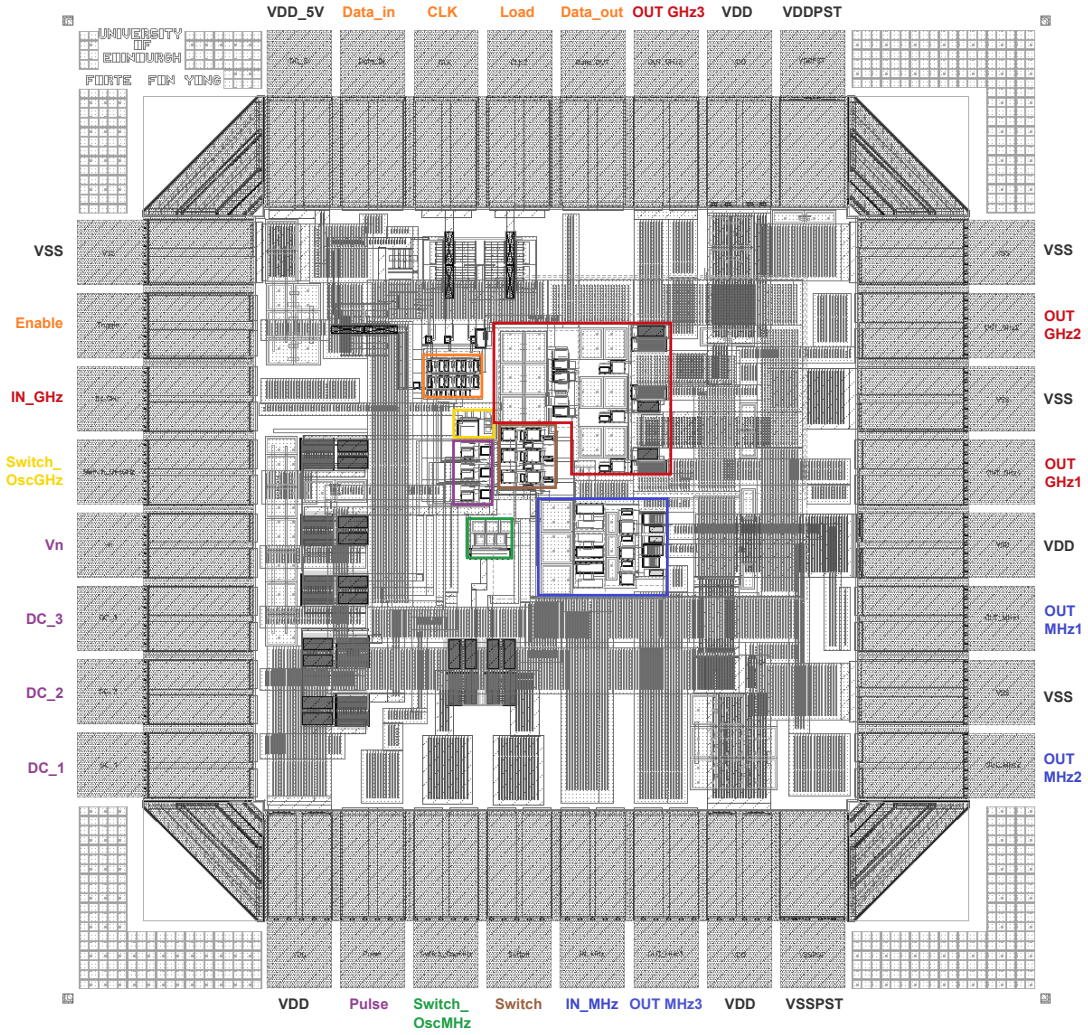


Figure B.5: Layout of the whole tuneable delay system includes padring.

References

[1] P. Taxel, "Two terminal non linear circuit elements.svg," https://upload.wikimedia.org/wikipedia/commons/thumb/1/15/Two-terminal_non-linear_circuit_elements.svg/1024px-Two-terminal_non-linear_circuit_elements.svg.png.

[2] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *nature*, vol. 453, no. 7191, p. 80, 2008.

[3] C. Yakopcic, S. Wang, W. Wang, E. Shin, J. Boeckl, G. Subramanyam, and T. M. Taha, "Filament formation in lithium niobate memristors supports neuromorphic programming capability," *Neural Computing and Applications*, vol. 30, pp. 3773–3779, 2018.

[4] S. Maheshwari, S. Stathopoulos, J. Wang, A. Serb, Y. Pan, A. Mifsud, L. B. Leene, J. Shen, C. Papavassiliou, T. G. Constandinou *et al.*, "Design flow for hybrid cmos/memristor systems—part i: Modeling and verification steps," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 12, pp. 4862–4875, 2021.

[5] V. Manouras, S. Stathopoulos, S. K. Garlapati, A. Serb, and T. Prodromakis, "Frequency response of metal-oxide memristors," *IEEE Transactions on Electron Devices*, vol. 68, no. 7, pp. 3636–3642, 2021.

[6] S. Pi, M. Ghadiri-Sadrabadi, J. C. Bardin, and Q. Xia, "Nanoscale memristive radiofrequency switches," *Nature communications*, vol. 6, no. 1, p. 7519, 2015.

[7] T. Wey and W. Jemison, "An automatic gain control circuit with tio 2 memristor variable gain amplifier," *Analog Integrated Circuits and Signal Processing*, vol. 73, pp. 663–672, 2012.

[8] I. Marković, M. Potrebić, and D. Tošić, "Memristors as candidates for replacing digital potentiometers in electric circuits," *Electronics*, vol. 10, no. 2, p. 181, 2021.

[9] J. Shen, S. Stathopoulos, T. Prodromakis, and C. Papavassiliou, "A reconfigurable cmos-memristor active inductor," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2020, pp. 1–5.

[10] N. Wainstein and S. Kvatinsky, "A lumped rf model for nanoscale memristive devices and nonvolatile single-pole double-throw switches," *IEEE Transactions on Nanotechnology*, vol. 17, no. 5, pp. 873–883, 2018.

[11] M. D. Gregory and D. H. Werner, "Application of the memristor in reconfigurable electromagnetic devices," *IEEE Antennas and Propagation Magazine*, vol. 57, no. 1, pp. 239–248, 2015.

[12] M. Potrebić, D. Tošić, and D. Biolek, "Rf/microwave applications of memristors," *Advances in memristors, memristive devices and systems*, pp. 159–185, 2017.

[13] N. Wainstein, T. Tsabari, Y. Goldin, E. Yalon, and S. Kvatinsky, "A dual-band cmos low-noise amplifier using memristor-based tunable inductors," in *2019 IEEE Computer Society Annual Symposium on VLSI (ISVLSI)*. IEEE, 2019, pp. 290–295.

[14] M. Potrebić, D. Tošić, and D. Biolek, "Reconfigurable microwave filters using memristors," *International Journal of Circuit Theory and Applications*, vol. 46, no. 1, pp. 113–121, 2018.

[15] I. L. Marković, M. M. Potrebić, and D. V. Tošić, "Main-line memristor mounted type loaded-line phase shifter realization," *Microelectronic Engineering*, vol. 185, pp. 48–54, 2018.

[16] G. Zhao and B. You, "A tunable negative group delay filter using memristors," in *2020 IEEE MTT-S International Wireless Symposium (IWS)*. IEEE, 2020, pp. 1–3.

[17] I. Barraj, M. A. Bahloul, and M. Masmoudi, "Design of 3–5 ghz tunable memristor-based ook-uwb transmitter," *AEU-International Journal of Electronics and Communications*, vol. 132, p. 153664, 2021.

[18] F. Yang, A. Serb, and T. Prodromakis, "Measured behaviour of a memristor-based tuneable instrumentation amplifier," *Electronics Letters*, vol. 58, no. 15, pp. 570–572, 2022.

[19] L. Chua, "Memristor-the missing circuit element," *IEEE Transactions on circuit theory*, vol. 18, no. 5, pp. 507–519, 1971.

[20] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nature materials*, vol. 6, no. 11, pp. 833–840, 2007.

[21] Q. Li, I. Salaoru, A. Khiat, H. Xu, and T. Prodromakis, "Correlated resistive/capacitive state variability in solid tio 2 based memory devices," *Applied Physics A*, vol. 123, pp. 1–5, 2017.

[22] M. Trapatseli, S. Cortese, A. Serb, A. Khiat, and T. Prodromakis, "Impact of ultra-thin al2o3–y layers on tio2–x reram switching characteristics," *Journal of applied physics*, vol. 121, no. 18, 2017.

[23] H. Kim, M. P. Sah, C. Yang, and L. O. Chua, "Memristor-based multilevel memory," in *2010 12th International Workshop on Cellular Nanoscale Networks and their Applications (CNNA 2010)*, 2010, pp. 1–6.

[24] S. Stathopoulos, A. Khiat, M. Trapatseli, S. Cortese, A. Serb, I. Valov, and T. Prodromakis, "Multibit memory operation of metal-oxide bi-layer memristors," *Scientific reports*, vol. 7, no. 1, p. 17532, 2017.

[25] J. Borghetti, G. S. Snider, P. J. Kuekes, J. J. Yang, D. R. Stewart, and R. S. Williams, "'memristive'switches enable 'stateful'logic operations via material implication," *Nature*, vol. 464, no. 7290, pp. 873–876, 2010.

[26] L. Zhou, S. Yang, G. Ding, J.-Q. Yang, Y. Ren, S.-R. Zhang, J.-Y. Mao, Y. Yang, Y. Zhou, and S.-T. Han, "Tunable synaptic behavior realized in c3n composite based memristor," *Nano Energy*, vol. 58, pp. 293–303, 2019.

[27] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano letters*, vol. 10, no. 4, pp. 1297–1301, 2010.

[28] D. Querlioz, O. Bichler, and C. Gamrat, "Simulation of a memristor-based spiking neural network immune to device variations," in *The 2011 International Joint Conference on Neural Networks*. IEEE, 2011, pp. 1775–1781.

[29] A. Afifi, A. Ayatollahi, and F. Raissi, "Implementation of biologically plausible spiking neural network models on the memristor crossbar-based cmos/nano circuits," in *2009 European Conference on Circuit Theory and Design*. IEEE, 2009, pp. 563–566.

[30] M. Hu, Y. Chen, J. J. Yang, Y. Wang, and H. H. Li, "A compact memristor-based dynamic synapse for spiking neural networks," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 36, no. 8, pp. 1353–1366, 2016.

[31] M. A. Zidan, H. A. H. Fahmy, M. M. Hussain, and K. N. Salama, "Memristor-based memory: The sneak paths problem and solutions," *Microelectronics journal*, vol. 44, no. 2, pp. 176–183, 2013.

[32] M. J. Sharifi and Y. M. Banadaki, "General spice models for memristor and application to circuit simulation of memristor-based synapses and memory cells," *Journal of Circuits, Systems, and Computers*, vol. 19, no. 02, pp. 407–424, 2010.

[33] P. Rabbani, R. Dehghani, and N. Shahpari, "A multilevel memristor–cmos memory cell as a reram," *Microelectronics Journal*, vol. 46, no. 12, pp. 1283–1290, 2015.

[34] B. Mohammad, D. Homouz, and H. Elgabra, "Robust hybrid memristor-cmos memory: Modeling and design," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 11, pp. 2069–2079, 2013.

[35] Y. Pan, P. Foster, A. Serb, and T. Prodromakis, "A rram-based associative memory cell," in *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2021, pp. 1–5.

[36] T. Raja and S. Mourad, "Digital logic implementation in memristor-based crossbars," in *2009 International Conference on Communications, Circuits and Systems*. IEEE, 2009, pp. 939–943.

[37] K. Cho, S.-J. Lee, and K. Eshraghian, "Memristor-cmos logic and digital computational components," *Microelectronics Journal*, vol. 46, no. 3, pp. 214–220, 2015.

[38] M. F. Tolba, M. E. Fouda, H. G. Hezayyin, A. H. Madian, and A. G. Radwan, "Memristor fpga ip core implementation for analog and digital applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 8, pp. 1381–1385, 2018.

[39] S. Shin, K. Kim, and S.-M. Kang, "Memristor applications for programmable analog ics," *IEEE Transactions on Nanotechnology*, vol. 10, no. 2, pp. 266–274, 2010.

[40] Z. Wang, C. Li, W. Song, M. Rao, D. Belkin, Y. Li, P. Yan, H. Jiang, P. Lin, M. Hu *et al.*, "Reinforcement learning with analogue memristor arrays," *Nature electronics*, vol. 2, no. 3, pp. 115–124, 2019.

[41] R. Berdan, T. Marukame, K. Ota, M. Yamaguchi, M. Saitoh, S. Fujii, J. Deguchi, and Y. Nishi, "Low-power linear computation using nonlinear ferroelectric tunnel junction memristors," *Nature Electronics*, vol. 3, no. 5, pp. 259–266, 2020.

[42] D. H. Werner and M. D. Gregory, "The memristor in reconfigurable radio frequency devices," in *Proceedings of the 2012 IEEE International Symposium on Antennas and Propagation*. IEEE, 2012, pp. 1–2.

[43] R. Marani, G. Gelao, and A. G. Perri, "A review on memristor applications," *arXiv preprint arXiv:1506.06899*, 2015.

[44] C. Li, Y. Li, H. Jiang, W. Song, P. Lin, Z. Wang, J. J. Yang, Q. Xia, M. Hu, E. Montgomery *et al.*, "Large memristor crossbars for analog computing," in *2018 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2018, pp. 1–4.

[45] G. M. Rebeiz, K. Entesari, I. C. Reines, S.-J. Park, M. A. El-Tanani, A. Grichener, and A. R. Brown, "Tuning in to rf mems," *IEEE microwave magazine*, vol. 10, no. 6, pp. 55–72, 2009.

[46] W. Yang, W. Che, H. Jin, W. Feng, and Q. Xue, "A polarization-reconfigurable dipole antenna using polarization rotation amc structure," *IEEE Transactions on Antennas and Propagation*, vol. 63, no. 12, pp. 5305–5315, 2015.

[47] M. D. Pickett and R. S. Williams, "Sub-100 fj and sub-nanosecond thermally driven threshold switching in niobium oxide crosspoint nanodevices," *Nanotechnology*, vol. 23, no. 21, p. 215202, 2012.

[48] A. C. Torrezan, J. P. Strachan, G. Medeiros-Ribeiro, and R. S. Williams, "Sub-nanosecond switching of a tantalum oxide memristor," *Nanotechnology*, vol. 22, no. 48, p. 485203, 2011.

[49] S. Poddar, Y. Zhang, L. Gu, D. Zhang, Q. Zhang, S. Yan, M. Kam, S. Zhang, Z. Song, W. Hu *et al.*, "Down-scalable and ultra-fast memristors with ultra-high density three-dimensional arrays of perovskite quantum wires," *Nano Letters*, vol. 21, no. 12, pp. 5036–5044, 2021.

[50] S. Pi, C. Li, H. Jiang, W. Xia, H. Xin, J. J. Yang, and Q. Xia, "Memristor crossbar arrays with 6-nm half-pitch and 2-nm critical dimension," *Nature nanotechnology*, vol. 14, no. 1, pp. 35–39, 2019.

[51] Q. Xia, W. Robinett, M. W. Cumbie, N. Banerjee, T. J. Cardinali, J. J. Yang, W. Wu, X. Li, W. M. Tong, D. B. Strukov *et al.*, "Memristor- cmos hybrid integrated circuits for reconfigurable logic," *Nano letters*, vol. 9, no. 10, pp. 3640–3645, 2009.

[52] C. Wang, Z. Si, X. Jiang, A. Malik, Y. Pan, S. Stathopoulos, A. Serb, S. Wang, T. Prodromakis, and C. Papavassiliou, "Multi-state memristors and their applications: An overview," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, 2022.

[53] S. Maheshwari, S. Stathopoulos, J. Wang, A. Serb, Y. Pan, A. Mifsud, L. B. Leene, J. Shen, C. Papavassiliou, T. G. Constandinou *et al.*, "Design flow for hybrid cmos/memristor systems—part ii: Circuit schematics and layout," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 12, pp. 4876–4888, 2021.

[54] S. Pi, M. Ghadiri-Sadrabadi, J. C. Bardin, and Q. Xia, "Memristors as radiofrequency switches," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2016, pp. 377–380.

[55] Y. G. Song, J. M. Suh, J. Y. Park, J. E. Kim, S. Y. Chun, J. U. Kwon, H. Lee, H. W. Jang, S. Kim, C.-Y. Kang *et al.*, "Artificial adaptive and maladaptive sensory receptors based on a surface-dominated diffusive memristor," *Advanced Science*, vol. 9, no. 4, p. 2103484, 2022.

[56] W. Sun, B. Gao, M. Chi, Q. Xia, J. J. Yang, H. Qian, and H. Wu, "Understanding memristive switching via in situ characterization and device modeling," *Nature communications*, vol. 10, no. 1, p. 3453, 2019.

[57] T. D. Dongale, P. Patil, N. Desai, P. P. Chougule, S. Kumbhar, P. Waifalkar, P. Patil, R. Vhatkar, M. Takale, P. Gaikwad *et al.*, "Tio 2 based nanostructured memristor for rram and neuromorphic applications: A simulation approach," *Nano convergence*, vol. 3, pp. 1–7, 2016.

[58] P. R. Somani and S. Radhakrishnan, "Electrochromic materials and devices: present and future," *Materials chemistry and physics*, vol. 77, no. 1, pp. 117–133, 2003.

[59] Y.-L. Zhu, K.-H. Xue, X.-M. Cheng, C. Qiao, J.-H. Yuan, L.-H. Li, and X.-S. Miao, "Uniform and robust tin/hfo2/pt memristor through interfacial al-doping engineering," *Applied Surface Science*, vol. 550, p. 149274, 2021.

[60] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-based resistive switching memories-nanoionic mechanisms, prospects, and challenges." *Advanced Materials (Deerfield Beach, Fla.)*, vol. 21, no. 25-26, pp. 2632–2663, 2009.

[61] A. Serb, A. Khiat, and T. Prodromakis, "An rram biasing parameter optimizer," *IEEE Transactions on Electron Devices*, vol. 62, no. 11, pp. 3685–3691, 2015.

[62] M. P. Sah, C. Yang, H. Kim, B. Muthuswamy, J. Jevtic, and L. Chua, "A generic model of memristors with parasitic components," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 3, pp. 891–898, 2015.

[63] K. J. Chandía, M. Bologna, and B. Tellini, "Analytical study on the influence of parasitic elements in a memristor," *Mathematical Problems in Engineering*, vol. 2018, no. 1, p. 2640591, 2018.

[64] A. Mazady and M. Anwar, "Memristor: part ii–dc, transient, and rf analysis," *IEEE Transactions on Electron Devices*, vol. 61, no. 4, pp. 1062–1070, 2014.

[65] M. Kim, E. Pallecchi, R. Ge, X. Wu, G. Ducournau, J. C. Lee, H. Happy, and D. Akinwande, "Analogue switches made from boron nitride monolayers for application in 5g and terahertz communication systems," *Nature Electronics*, vol. 3, no. 8, pp. 479–485, 2020.

[66] N. Wainstein and S. Kvatinsky, "An rf memristor model and memristive single-pole double-throw switches," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2017, pp. 1–4.

[67] Y. Xiao, B. Jiang, Z. Zhang, S. Ke, Y. Jin, X. Wen, and C. Ye, "A review of memristor: material and structure design, device performance, applications and prospects," *Science and Technology of Advanced Materials*, vol. 24, no. 1, p. 2162323, 2023.

[68] B. J. Choi, A. C. Torrezan, K. J. Norris, F. Miao, J. P. Strachan, M.-X. Zhang, D. A. Ohlberg, N. P. Kobayashi, J. J. Yang, and R. S. Williams, "Electrical performance and scalability of pt dispersed sio2 nanometallic resistance switch," *Nano letters*, vol. 13, no. 7, pp. 3213–3217, 2013.

[69] T. A. Wey and W. D. Jemison, "Variable gain amplifier circuit using titanium dioxide memristors," *IET circuits, devices & systems*, vol. 5, no. 1, p. 59, 2011.

[70] S. Kvatinsky, M. Ramadan, E. G. Friedman, and A. Kolodny, "Vteam: A general model for voltage-controlled memristors," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 62, no. 8, pp. 786–790, 2015.

[71] J. J. Yang, D. B. Strukov, and D. R. Stewart, "Memristive devices for computing," *Nature nanotechnology*, vol. 8, no. 1, pp. 13–24, 2013.

[72] M. Goswami and S. Khanna, "Dc suppressed high gain active cmos instrumentation amplifier for biomedical application," in *2011 International Conference on Emerging Trends in Electrical and Computer Technology*. IEEE, 2011, pp. 747–751.

[73] R. Pandey, N. Pandey, S. K. Paul *et al.*, "Electronically tunable transimpedance instrumentation amplifier based on otra," *Journal of Engineering*, vol. 2013, 2013.

[74] C. Psychalinos, S. Minaei, and L. Safari, "Ultra low-power electronically tunable current-mode instrumentation amplifier for biomedical applications," *AEU-International Journal of Electronics and Communications*, vol. 117, p. 153120, 2020.

[75] U. Bassembek and O. Krestinskaya, "Instrumentation amplifier design: Comparison of cmos-memristive to cmos design," *arXiv preprint arXiv:1805.07675*, 2018.

[76] C. Kołaciński and D. Obrębski, "Design of cmos analog integrated readout circuit for nmos thz detectors," in *Proceedings of the 20th International Conference Mixed Design of Integrated Circuits and Systems-MIXDES 2013*. IEEE, 2013, pp. 222–228.

[77] T. Kugelstadt, "Getting the most out of your instrumentation amplifier design," *SAT*, vol. 1, no. 2, p. 2, 2005.

[78] O. A. Olumodeji and M. Gottardi, "Behavioural modelling of memristive devices targeted to sensor interfaceswa," in *2015 XVIII AISEM Annual Conference*. IEEE, 2015, pp. 1–4.

[79] R. Berdan, A. Serb, A. Khiat, A. Regoutz, C. Papavassiliou, and T. Prodromakis, "A μ-controller-based system for interfacing selectorless rram crossbar arrays," *IEEE Transactions on Electron Devices*, vol. 62, no. 7, pp. 2190–2196, 2015.

[80] P. Foster, J. Huang, A. Serb, T. Prodromakis, and C. Papavassiliou, "An fpga based system for interfacing with crossbar arrays," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2020, pp. 1–4.

[81] I. Valov, R. Waser, J. R. Jameson, and M. N. Kozicki, "Electrochemical metallization memories—fundamentals, applications, prospects," *Nanotechnology*, vol. 22, no. 25, p. 254003, 2011.

[82] R. Berdan, "Applications of memristors in conventional analogue electronics," 2016.

[83] Y. Chen, G. Liu, C. Wang, W. Zhang, R.-W. Li, and L. Wang, "Polymer memristor for information storage and neuromorphic applications," *Materials Horizons*, vol. 1, no. 5, pp. 489–506, 2014.

[84] C. Chanapromma, C. Tanaphatsiri, and M. Siripruchyanun, "An electronically controllable instrumentation amplifier based on cccctas," in *2008 International Symposium on Intelligent Signal Processing and Communications Systems*. IEEE, 2009, pp. 1–4.

[85] L. Safari, S. Minaei, G. Ferri, and V. Stornelli, "Analysis and design of a new coa-based current-mode instrumentation amplifier with robust performance against mismatches," *AEU-International Journal of Electronics and Communications*, vol. 89, pp. 105–109, 2018.

[86] A. Hajimiri, H. Hashemi, A. Natarajan, X. Guan, and A. Komijani, "Integrated phased array systems in silicon," *Proceedings of the IEEE*, vol. 93, no. 9, pp. 1637–1655, 2005.

[87] D. Parker and D. C. Zimmermann, "Phased arrays-part 1: theory and architectures," *IEEE transactions on microwave theory and techniques*, vol. 50, no. 3, pp. 678–687, 2002.

[88] Z. Rongzhi and Y. Kaizhong, *Spacecraft collision avoidance technology*. Academic Press, 2020.

[89] R. Rotman, M. Tur, and L. Yaron, "True time delay in phased arrays," *Proceedings of the IEEE*, vol. 104, no. 3, pp. 504–518, 2016.

[90] M. Longbrake, "True time-delay beamsteering for radar," in *2012 IEEE National Aerospace and Electronics Conference (NAECON)*. IEEE, 2012, pp. 246–249.

[91] I. Frigyes and A. Seeds, "Optically generated true-time delay in phased-array antennas," *IEEE Transactions on Microwave Theory and Techniques*, vol. 43, no. 9, pp. 2378–2386, 1995.

[92] J. Perruisseau-Carrier, R. Fritschi, P. Crespo-Valero, and A. K. Skrivervik, "Modeling of periodic distributed mems-application to the design of variable true-time delay lines," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 1, pp. 383–392, 2006.

[93] P. Yu and D. Zhao, "Design considerations for wideband hybrid large-scale antenna array and implementation of a 5–23-ghz cmos true-time-delay circuit," *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2023.

[94] A. Nagulu, A. Gaonkar, S. Ahasan, S. Garikapati, T. Chen, G. Zussman, and H. Krishnaswamy, "A full-duplex receiver with true-time-delay cancelers based on switched-capacitor-networks operating beyond the delay–bandwidth limit," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 5, pp. 1398–1411, 2021.

[95] M. H. Ghazizadeh and A. Medi, "Novel trombone topology for wideband true-time-delay implementation," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 4, pp. 1542–1552, 2019.

[96] S. Barker and G. M. Rebeiz, "Distributed mems true-time delay phase shifters and wide-band switches," *IEEE Transactions on Microwave Theory and Techniques*, vol. 46, no. 11, pp. 1881–1890, 1998.

[97] F. Hu and K. Mouthaan, "A 1–20 ghz 400 ps true-time delay with small delay error in 0.13 μm cmos for broadband phased array antennas," in *2015 IEEE MTT-S International Microwave Symposium*. IEEE, 2015, pp. 1–3.

[98] S. Park and S. Jeon, "A 15–40 ghz cmos true-time delay circuit for uwb multi-antenna systems," *IEEE microwave and wireless components letters*, vol. 23, no. 3, pp. 149–151, 2013.

[99] I. Mondal and N. Krishnapura, "A 2-ghz bandwidth, 0.25–1.7 ns true-time-delay element using a variable-order all-pass filter architecture in 0.13μ m cmos," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 8, pp. 2180–2193, 2017.

[100] Y. Chen and W. Li, "Compact and broadband variable true-time delay line with dll-based delay-time control," *Circuits, Systems, and Signal Processing*, vol. 37, pp. 1007–1027, 2018.

[101] M. Li, N. Li, H. Gao, Z. Zhang, S. Wang, Y.-C. Kuan, C. Song, X. Yu, Q. J. Gu, and Z. Xu, "An 800-ps origami true-time-delay-based cmos receiver front end for 6.5–9-ghz phased arrays," *IEEE Solid-State Circuits Letters*, vol. 3, pp. 382–385, 2020.

[102] M. H. Ghazizadeh and A. Medi, "A 125-ps 8–18-ghz cmos integrated delay circuit," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 1, pp. 162–173, 2018.

[103] D. Liu, N. Wang, G. Wang, Z. Shao, X. Zhu, C. Zhang, and H. Cheng, "Nonvolatile bipolar resistive switching in amorphous sr-doped lamno3 thin films deposited by radio frequency magnetron sputtering," *Applied Physics Letters*, vol. 102, no. 13, 2013.

[104] O. Kavehei, A. Iqbal, Y. Kim, K. Eshraghian, S. Al-Sarawi, and D. Abbott, "The fourth element: characteristics, modelling and electromagnetic theory of the memristor," *Proceedings of the Royal Society A: Mathematical, Physical and Engineering Sciences*, vol. 466, no. 2120, pp. 2175–2202, 2010.

[105] A. Thomas, "Memristor-based neural networks," *Journal of Physics D: Applied Physics*, vol. 46, no. 9, p. 093001, 2013.

[106] S. K. Garakoui, E. A. Klumperink, B. Nauta, and F. E. van Vliet, "Time delay circuits: A quality criterion for delay variations versus frequency," in *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*. IEEE, 2010, pp. 4281–4284.

[107] A. Ulusoy, B. Schleicher, and H. Schumacher, "A tunable differential all-pass filter for uwb true time delay and phase shift applications," *IEEE Microwave and Wireless Components Letters*, vol. 21, no. 9, pp. 462–464, 2011.

[108] M. B. Elamien, B. J. Maundy, L. Belostotski, A. S. Elwakil, and S. A. Mahmoud, "A wideband delay-tunable fully differential allpass filter in 65-nm cmos technology," in *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2019, pp. 1–5.

[109] S. K. Garakoui, E. A. Klumperink, B. Nauta, and F. E. van Vliet, "Compact cascadable gm-c all-pass true time delay cell with reduced delay variation over frequency," *IEEE journal of solid-state circuits*, vol. 50, no. 3, pp. 693–703, 2015.

[110] B. Razavi, "Prospects of cmos technology for high-speed optical communication circuits," *IEEE journal of solid-state circuits*, vol. 37, no. 9, pp. 1135–1145, 2002.

[111] T. H. Lee, *The design of CMOS radio-frequency integrated circuits*. Cambridge university press, 2003.

[112] I. Messaris, A. Serb, S. Stathopoulos, A. Khiat, S. Nikolaidis, and T. Prodromakis, "A data-driven verilog-a reram model," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. 12, pp. 3151–3162, 2018.

[113] E. Zolkov, A. Madjar, R. Weiss, and E. Cohen, "Analysis and design of n-path true-time-delay circuit," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 12, pp. 5381–5394, 2020.

[114] T.-S. Chu, J. Roderick, and H. Hashemi, "An integrated ultra-wideband timed array receiver in 0.13 μm cmos using a path-sharing true time delay architecture," *IEEE Journal of solid-state circuits*, vol. 42, no. 12, pp. 2834–2850, 2007.

[115] E. Zolkov and E. Cohen, "A 0.2–3-ghz n-path true time delay circuit achieving $<$ 1% delay variation over frequency," *IEEE Transactions on Microwave Theory and Techniques*, vol. 70, no. 6, pp. 3224–3233, 2022.

[116] L. Franks and I. Sandberg, "An alternative approach to the realization of network transfer functions: the n-path filter," *Bell System Technical Journal*, vol. 39, no. 5, pp. 1321–1350, 1960.

[117] E. Klumperink and B. Nauta, "N-path filters and mixer-first receivers–a review," *IC Design Insights-from Selected Presentations at CICC 2017*, pp. 221–264, 2022.

[118] C.-k. Luo, P. S. Gudem, and J. F. Buckwalter, "A 0.2–3.6-ghz 10-dbm b1db 29-dbm iip3 tunable filter for transmit leakage suppression in saw-less 3g/4g fdd receivers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 10, pp. 3514–3524, 2015.

[119] Z. Lin, P.-I. Mak, R. P. Martins, Z. Lin, P.-I. Mak, and R. P. Martins, "Analysis and modeling of a gain-boosted n-path switched-capacitor bandpass filter," *Ultra-Low-Power and Ultra-Low-Cost Short-Range Wireless Receivers in Nanoscale CMOS*, pp. 57–80, 2016.

[120] Y. Xu and P. R. Kinget, "A switched-capacitor rf front end with embedded programmable high-order filtering," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 5, pp. 1154–1167, 2016.

[121] S. Krishnamurthy and A. M. Niknejad, "Design and analysis of enhanced mixer-first receivers achieving 40-db/decade rf selectivity," *IEEE Journal of Solid-State Circuits*, vol. 55, no. 5, pp. 1165–1176, 2019.

[122] J. Bonner-Stewart, C. Wilson, and B. A. Floyd, "Tunable 0.7–2.8-ghz reflection-mode n-path filters in 45-nm soi cmos," *IEEE Transactions on Microwave Theory and Techniques*, vol. 68, no. 6, pp. 2343–2357, 2020.

[123] Y.-C. Lien, E. A. Klumperink, B. Tenbroek, J. Strange, and B. Nauta, "Enhanced-selectivity high-linearity low-noise mixer-first receiver with complex pole pair due to capacitive positive feedback," *IEEE journal of solid-state circuits*, vol. 53, no. 5, pp. 1348–1360, 2018.

[124] C.-k. Luo, P. S. Gudem, and J. F. Buckwalter, "A 0.4–6-ghz 17-dbm b1db 36-dbm iip3 channel-selecting low-noise amplifier for saw-less 3g/4g fdd diversity receivers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 4, pp. 1110–1121, 2016.

[125] A. Korkmaz, C. He, L. P. Katehi, R. S. Williams, and S. Palermo, "Design of tunable analog filters using memristive crossbars," in *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2021, pp. 1–5.

[126] C. He, A. Korkmaz, S. Palermo, R. S. Williams, and L. P. Katehi, "Analog signal processing in high frequency circuits using crossbar configurations," in *2021 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS)*. IEEE, 2021, pp. 116–121.

[127] A. Ghaffari, E. A. Klumperink, M. C. Soer, and B. Nauta, "Tunable high-q n-path band-pass filters: Modeling and verification," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, 2011.

[128] R. Fischl, "Analysis of a commutated network," *IEEE Transactions on Aerospace and Navigational Electronics*, no. 2, pp. 114–123, 1963.

[129] W. LePage, C. Cahn, and J. Brown, "Analysis of a comb filter using synchronously commutated capacitors," *Transactions of the American Institute of Electrical Engineers, Part I: Communication and Electronics*, vol. 72, no. 1, pp. 63–68, 1953.

[130] B. Smith, "Analysis of commutated networks," *Transactions of the IRE Professional Group on Aeronautical and Navigational Electronics*, pp. 21–26, 1953.